# NAU88L21C
## Ultra-Low Power, Low Latency Signal Path, High Quality Stereo Audio CODEC

### GENERAL DESCRIPTION

The NAU88L21C is an ultra-low power high performance audio CODEC that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital microphone interface, one digital mixer, two high quality DACs, low latency ADCs, and one stereo class-G headphone amplifier. The advanced on-chip signal processing engine that includes dynamic range compressor (DRC), programmable biquad filter, as well as an integrated frequency locked loop (FLL) to support various input clocks.

### FEATURES

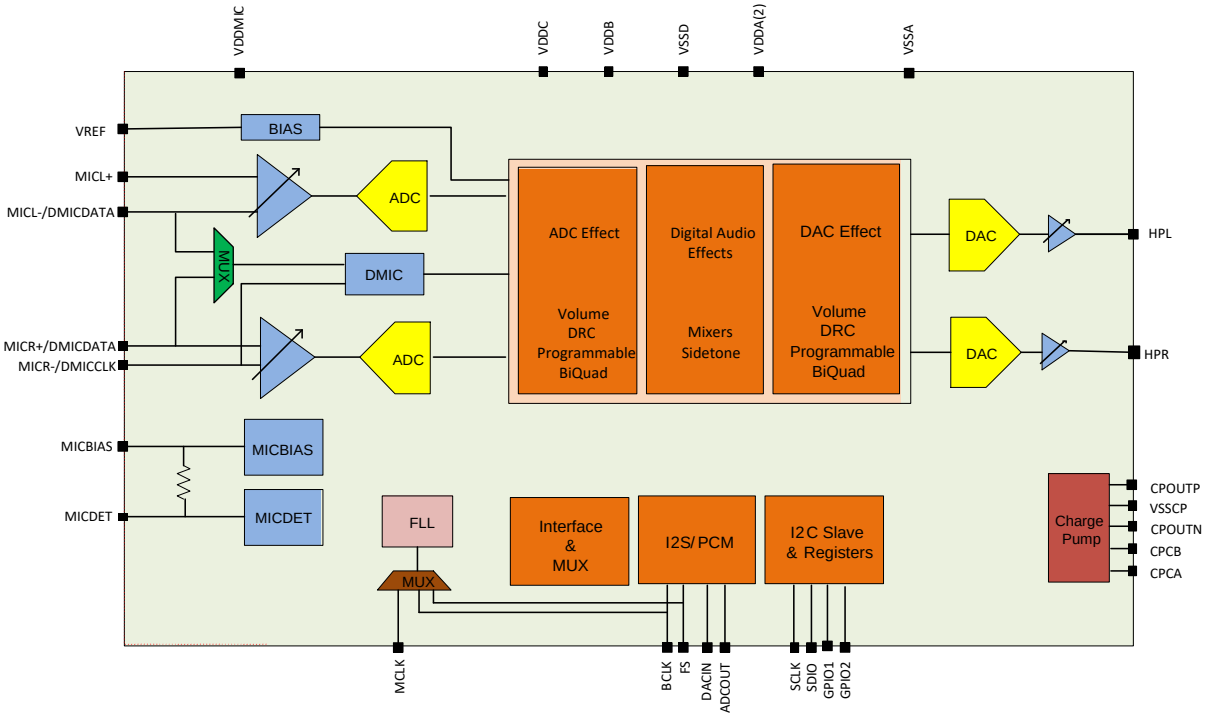
- 1 Digital I2S/PCM I/O port
- Two mono differential or one stereo differential analog microphone inputs, two single-ended microphone inputs or one stereo digital microphone input
- Cap-free low noise microphone bias with 7uVrms noise between 20Hz-20kHz, internal pull high resistor for microphone
- Class G Headphone Amplifier (28mW @ 32Ω, 1% THD+N)
- DAC: 105dB SNR, (A-weighted) @ 0dB gain, 1.8V and -82dB THD @ 20mW and RL= 32Ω, DAC playback to headphone output mode
- ADC: 103dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48kHz and -93dB THD, 1.8V, MIC gain 0dB, OSR 256x

- Sampling rate from 8K to 192 KHz
- Low latency signal path
- Dynamic Range Compressor (DRC)Programmable Biquad filter Integrated DSP with specific functions:Input automatic level control (ALC/AGC)/limiter
- Output dynamic-range-compressor/limiter
- Package: QFN-32
  Package is Halogen-free, RoHS-compliant and TSCA-compliant

### APPLICATIONS

- Gaming controller
- Wireless Headset
- Smart Remote Controller

## Block Diagram - QFN32



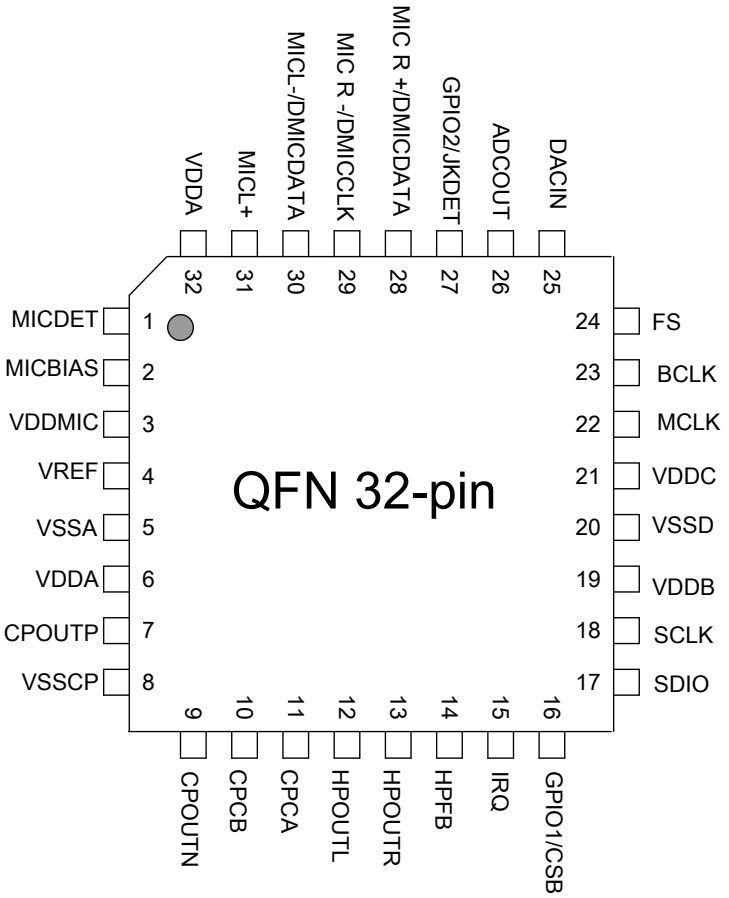
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## Pin Diagram




Note:

(1)
VDDA & VDDC must be tied together.
VSSA & VSSD must be tied together.

(2)
DMICDATA pin option reference REG0x69[3]=0, DMICDATA is pin 30. Analog MiC single-ended; when REG0x69[3]=1, DMICDATA is pin 28. Analog MICL can configure differential.

## Pin Description

| Pin # | Name | Type | Functionality |
|---|---|---|---|
| 1 | MICDET | Analog IO | Microphone/button detect, 2kOhm between Mic and Mic Bias |
| 2 | MICBIAS | Analog Output | Microphone Bias Output |
| 3 | VDDMIC | Supply | Microphone supply |
| 4 | VREF | Analog I/O | Internal DAC & ADC voltage reference decoupling I/O |
| 5 | VSSA | Ground | Analog Ground |
| 6 | VDDA | Supply | Analog Supply |
| 7 | CPOUTP | Analog I/O | Charge Pump positive voltage |
| 8 | VSSCP | Ground | Charge Pump Supply ground |
| 9 | CPOUTN | Analog I/O | Charge Pump negative voltage |
| 10 | CPCB | Analog I/O | Charge Pump switching capacitor node B |
| 11 | CPCA | Analog I/O | Charge Pump switching capacitor node A |
| 12 | JKTIP(HPL) | Analog Output | Jack Tip; Headphone left channel output |
| 13 | JKR1(HPR) | Analog Output | Jack Ring1; Headphone right channel output |
| 14 | HPFB | Ground | Headphone Ground |
| 15 | IRQ | Digital I/O | IRQ |
| 16 | GPIO1/CSB | Digital I/O | General Purpose IO/CSB |
| 17 | SDIO | Digital I/O | Serial Data for I2C |
| 18 | SCLK | Digital Input | Serial Data Clock for I2C |
| 19 | VDDB | Supply | Digital IO Supply |
| 20 | VSSD | Ground | Digital IO Ground |
| 21 | VDDC | Supply | Digital Core Supply |
| 22 | MCLK | Digital Input | CODEC Master clock input |
| 23 | BCLK | Digital I/O | Serial data bit clock input or output for I2S or PCM data |
| 24 | FS | Digital I/O | Frame Sync input or output for I2S or PCM data |
| 25 | DACIN | Digital Input | Serial Audio data input for I2S or PCM data |
| 26 | ADCOUT | Digital Output | Serial Audio data Output for I2S or PCM data |
| 27 | JKDET/GPIO2 | Analog Input | Jack detect input supplied by VDDA |
| 28 | MICR+/DMICDATA | Analog Input | PGA MICR+ Analog Input / Digital Microphone Data input |
| 29 | MICR-/DMICCLK | Analog/Digital Output | PGA MICR- Analog Input / Digital Microphone Clk output |
| 30 | MICL- | Analog Input/Digital Input | PGA MICL- Analog Input |
| 31 | MICL+ | Analog Input | PGA MICL+ Analog Input |
| 32 | VDDA | Supply | Analog Supply |

## Electrical Characteristics

Conditions: $V_{DD}A = V_{DD}B = 1.8V$; $V_{DD}MIC = 3.6V$.
$R_L$(Headphone) = 32 Ω, f = 1kHz, MCLK=12.288MHz, unless otherwise specified. Limits apply for $T_A$ = 25°C

| Symbol | Parameter | Conditions | Typical | Limit | Units |
|---|---|---|---|---|---|
| ISD | Shutdown Current | $V_{DD}A$ | 4 | 10 | µA |
| | | $V_{DD}B$ | 0.2 | 1 | |
| | | $V_{DD}MIC$ | 0.2 | 1 | |
| $I_{DD}$ | Headset Detection Standby Mode | MCLK off, Jack Insertion, IRQ enabled | | 10 | µA |
| | Active Current Normal Playback Mode | fS = 48kHz, Stereo HP DAC On, HP On, POUT = 0mW. RL(HP) = 32Ω | | 5 | mA |
| | | **Headphone Amplifier** | | | |
| $P_O$ | Output Power | Stereo RL = 32Ω, DAC Input, CPVVDD = 1.8V, f=1020Hz, 22kHz BW, THD+N = 1% (QFN package) | 28 | | mW |
| | | Stereo RL = 16Ω, DAC Input, CPVVDD = 1.8V, f=1020Hz, 22kHz BW, THD+N = 1% (QFN Package) | 33 | | mW |
| THD+N | Total Harmonic Distortion + Noise | RL = 32Ω, f=1020Hz, PO = 20mW | -82 | | dB |
| SNR | Signal to Noise Ratio | VOUT = 1VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted) | 105 | | dB |
| | | VOUT = 1 VRMS, DAC Input, DAC_Gain = 0dB, HP_Gain = 0dB, Digital Zero Input, f=1020Hz, A-Weighted, auto attenuate enabled | 108 | | dB |
| PSRR | Power Supplys Rejection Ratio | $f_{RIPPLE}$ = 217Hz, $V_{RIPPLE}$ = 200m$V_{P_P}$ Input Referred, HP_GAIN = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to $V_{DD}A$ | 85 | | dB |
| $X_{TALK}$ | Channel Crosstalk | Left Channel to Right Channel, -1dBFS, Gain = 0dB, f = 1020Hz | 70 | | dB |
| | Interchannel Level Mismatch | | +/- 0.1 | | dB |
| | Frequency Response | F = 20Hz ~ 20kHz | +0.1/-0.2 | | dB |
| $e_{OS}$ | Output Noise | DAC_Gain = 0dB, HP_Gain = 0dB, fS=48kHz, OSRDAC = 128, A-Weighted | 4.4 | | $uV_{RMS}$ |
| | Out of Band Noise Level | | -60dB | | |
| $V_{OS}$ | Output Offset Voltage | HP_Gain = 0dB, DAC_Gain= 0dB, DAC Input | | ±1 | mV |
| | Power Consunption MP3 Mode | No Load, No Signal, Amp on fs = 48kHz, Stereo DAC On, Amp On, POUT = 0mW. RL = 32Ω | 6.5 | | mW |
| | Fs Accuracy (44.1 / 48 kHz) | | +/- 0.02% | | |

| Symbol | Parameter | Conditions | Typical | Limit | Units |
|---|---|---|---|---|---|
| | Pop and Click Noise | | 1 | | mVrms |
| | | **ADC** | | | |
| THD+N | ADC Total Harmonic Distortion + Noise | MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1020Hz, fs = 48KHz, Mono Differential Input | -91 | | dB |
| | | MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=28.5mVrms, f=1020Hz, Digital Gain = 0dB, Mono Differential Input | -80 | | dB |
| SNR | Signal to Noise Ratio | Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 48kHz, Mono Differential Input | 102 | | dB |
| | | Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 48kHz, Mono Differential Input | 100 | | dB |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{PP}$ applied to $V_{DD}$A, $f_{RIPPLE}$ = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input | 80 | | dB |
| CMRR | Common Mode Rejection Ratio | Differential Input 100mVrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz | 65 | | dB |
| $FS_{ADC}$ | ADC Full Scale Input Level | $V_{DD}$A= 1.8V, ADC VREFSEL = 01'b, DGAINR_ADC = DGAINL_ADC = D0'b Differential Input | 1 | | $V_{RMS}$ |
| | Minimum Input Impedance | | 10 | | kOhm |
| | Frequency Response | f = 20Hz ~ 20kHz | +0.1/-0.2 | | dB |
| | Power Consumption | No Signal, ADC on $f_s$ = 44.1kHz | 7.9 | | mW |
| | Group Delay Distortion | Delta Group Delay - Non-linear 0~40kHz | 0.4 | | 1/fs |
| | Group Delay Distortion | Delta Group Delay – Linear 0~40kHz | 0 | | 1/fs |
| | Group Delay (Latency) | No BIQ, No DRC. SR=48kHz | 5.6 | | 1/fs |
| | | **MICBIAS** | | | |
| $I_{OUT}$ | Output Current | Low Power Mode, MICBIAS=VDDA*1.53V | | 27 | mA |
| $e_{os}$ | Output Noise | Low Noise Mode, f = 20Hz ~ 20kHz MICBIAS=2.7V | | 10 | uVrms |

**Digital I/O**

| Parameter | Symbol | Comments/Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| Input LOW level | $V_{IL}$ | $V_{DD}$B = 1.8V | | | 0.33*$V_{DD}$B | V |
| | | $V_{DD}$B = 3.3V | | | 0.37*$V_{DD}$B | |
| Input HIGH level | $V_{IH}$ | $V_{DD}$B = 1.8V | | 0.67*$V_{DD}$B | | V |
| | | $V_{DD}$B = 3.3V | | 0.63*$V_{DD}$B | | |
| Output HIGH level | $V_{OH}$ | $I_{Load}$= 1mA | $V_{DD}$B=1.8V | 0.9*$V_{DD}$B | | V |
| | | | $V_{DD}$B = 3.3V | 0.95*$V_{DD}$B | | |
| Output LOW level | $V_{OL}$ | $I_{Load}$= 1mA | $V_{DD}$B = 1.8V | | 0.1*$V_{DD}$B | V |

| Parameter | Symbol | Comments/Conditions | | Min | Max | Units |
|---|---|---|---|---|---|---|
| | | | $V_{DD}B$=3.3V | | 0.05*$V_{DD}B$ | |

**Recommended Operating Conditions**

| Condition | Symbol | Min | Typical | Max | Units |
|---|---|---|---|---|---|
| Digital I/O Supply Range | $V_{DD}B$ | 1.62 | 3.3 | 3.6 | V |
| Analog Supply Range | $V_{DD}A$ | 1.62 | 1.8 | 1.98 | V |
| Headphone Supply Range | $V_{DD}A$ | 1.62 | 1.8 | 1.98 | V |
| Microphone Bias Supply Voltage | $V_{DD}MIC$ | 3.0 | 3.3 | 3.6 | V |
| Temperature Range | $T_A$ | -40 | | +85 | °C |

**Absolute Maximum Ratings**

| Parameter | Min | Max | Units |
|---|---|---|---|
| Digital Supply Range | -0.3 | 2.2 | V |
| Digital I/O Supply Range | -0.3 | 4.0 | V |
| Analog Supply Range | -0.3 | 2.2 | V |
| Headphone Supply Range | -0.3 | 2.2 | V |
| Microphone Bias Supply Voltage | -0.3 | 4.0 | V |
| Voltage Input Digital Range | DGND - 0.3 | $V_{DD}$ + 0.3 | V |
| Voltage Input Analog Range | AGND - 0.3 | $V_{DD}$ + 0.3 | V |
| Junction Temperature, $T_J$ | -40 | +150 | °C |
| Storage Temperature | -65 | +150 | °C |

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.*

# 1. General Description

NAU88L21C is an ultra-low power CODECs that has both analog and digital blocks operating at 1.8V. This CODEC includes DSP functions including DRCs (Dynamic Range Compression) and programmable biquad filters. Mic bias supply is upgraded to support voltages up to 3V.

## 1.1 Inputs

The NAU88L21C provides analog inputs to acquire and process audio signals from microphones with high fidelity and flexibility. There is a stereo input path that can be used to capture signals from single-ended or differential sources. The channel has a fully differential programmable gain amplifier (PGA). The outputs of the PGA connect to the ADC.

The NAU88L21C also has an input for one digital microphone. The NAU88L21C provides a DMCLK, the clock signal for the digital microphones.

The analog and the digital microphone inputs cannot be used simultaneously.

## 1.2 Outputs

NAU88L21C has one pair of ground-referenced Class G headphone outputs that are fed by two DACs. The headphone amplifier has a gain range of -9dB to 0dB.

The Class G headphone amplifier is powered by the charge pump output voltages CPOUTP and CPOUTN.
This headphone output can also be used as a lineout.

## 1.3 ADC, DAC and Digital Signal Processing

The NAU88L21C has two independent high quality ADC's and DACs. These are high performance 24-bit sigma-delta converters, which are suitable for a very wide range of applications.

The ADCs and DACs have functions that individually support digital mixing and routing. The ADCs and DACs blocks also support advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and maximize the audio dynamic range supported by the NAU88L21C.

The ADCs and DACs digital signal process can support two-point dynamic range compressors (DRCs), programmable biquad filters configurable for low pass filters, high pass filters, Notch filter, Bell, low shelf, and high shelf filters with various gain, Q, and frequency controls. Two-point DRCs can be programmed to limit the maximum output level and/or boost a low output level. The biquad filters can be configured as high pass filters intended for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or "wind noise" on a microphone inputs.

Zero-crossing enable for filter types 3'b1xx switching added for ADCFLT_TYPESEL and DAC FLT_TYPESEL. Internal function checks input signal zero crossing points as switching point.

## 1.4 Digital Interfaces

Command and control of the device is accomplished by using the I2C interface.

The digital audio I/O data streams transfer separately from command and control using either I2S or PCM audio data protocols

These simple but highly flexible interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I2S and PCM devices.

# 2. Power Supply

This NAU88L21C has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. Because of this, there are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harming the device. However, pops and clicks may result from some sequences. Pop-sound protection can be enabled while filter type selection changes or MCLKDET down(check MCLKDET_CTRL_EN if it is on), digital filter auto-mute to zero with 30fs.

## 2.1 Power On and Off Reset

The NAU88L21C includes a power on reset circuit on chip. The circuit resets the internal logic control at VDDA supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 1.0Vdc for VDDA. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power level for VDDA is below its threshold. Once the power level rises above its threshold, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.

For reliable operation, it is recommended to write any value to register REG0x00 upon power up. This will reset all registers to the known default state.

Note that when VDDA is below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

## 2.2 Power up and Start Sequence

The power up sequence to bring up the analog blocks smoothly is illustrated below and involves three different time segments (T1 – T4). The power supply ramp rate depends on a number of factors such as the power source drive strength, board parasitics and the decopling capacitor size on the supply line. Typically, a power supply ramp time can be as fast as 5mS or as slow as 200mS.

During time T1, the power supply ramps-up. The internal PORB reset is generated when $V_{DDA}$ is lower than 1.1V for reliable maintenance of internal logic circuits. While PORB signal is low, it clears internal digital flops. Most of the flops will be cleared to ‘0’ while some flops can be set to ‘1’ during the PORB pulse depending on the required default state of the register. For extreme cases, VDDA and VDDC are derived from different power supply sources, VDDA needs to be earlier ramping up than VDDC at least 10ms.

After time T1, wait another time 1mS so that the power supply is stable before writing to the registers. During time T2, the chip is in stand-by mode and all registers are in a default state. In stand-by, the chip only consumes leakage current and all analog blocks are turned-off. At time T3, the user can start to write data into the registers via the I2C serial bus to setup the chip for their application.

When I2C finished loading register in T3 period, waiting for T4, 1ms period, I2S clocks could input to device.

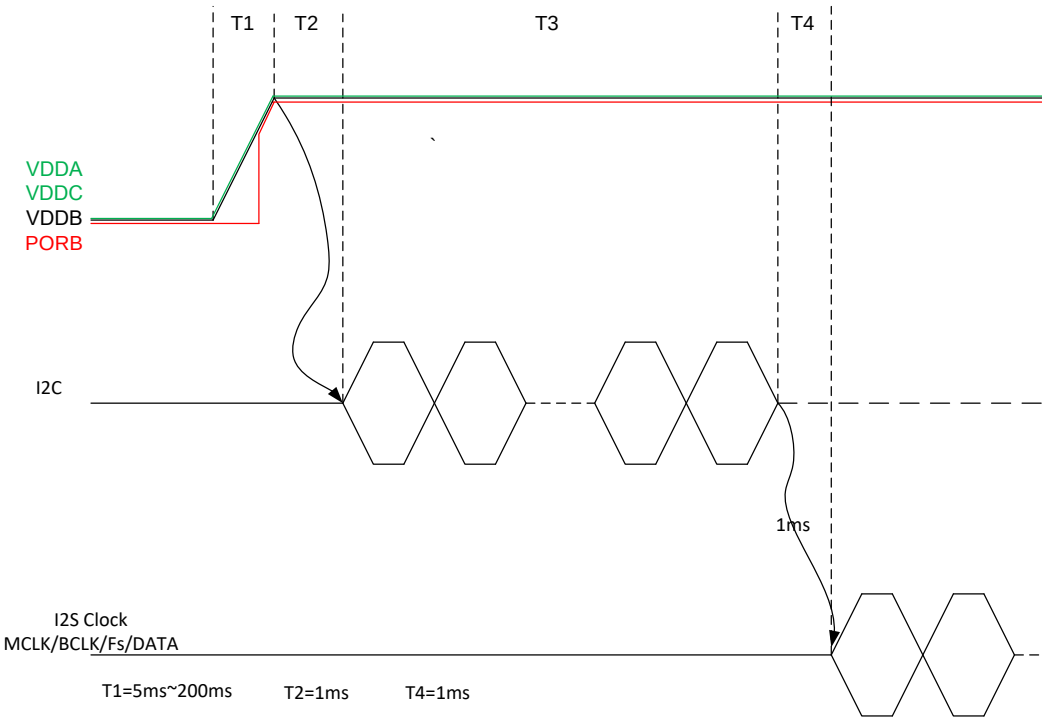



Figure 1: Power up sequence

# 3. Input Path Detailed Descriptions

NAU88L21C has two low noise, high common mode rejection ratio analog microphone differential input. The microphone inputs MICL+/- & MICR+/- which are followed by -1dB to 36dB PGA gain stages that have a fixed 12kOhm input impedance.

Inputs are maintained at a DC bias of approximately ½ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of external DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

## 3.1 Analog Microphone Inputs

The analog microphone inputs are routed to the FEPGA (Front End Programmable Gain Amplifier). The input stage can be configured in different modes. The FEPGA gain can be varied from -1dB to 36dB in 1dB steps. The gain stage has a fixed 12kOhm input impedance and can be individually enabled or disabled by using register.

As shown in Figure 1,
For left channel input path
SL1, it is controlled by 0x76[11]DISCHRG and 0x77[14]ACDC_CTRL[0],
SL2, it is controlled by 0x76[11]DISCHRG and 0x77[15]ACDC_CTRL[1],
SL3 and SL4, they are controlled by 0x77[5]FEPGA_MODEL,
SL5 and SL6, they are controlled by 0x77[7]FEPGA_MODEL,
SL7, it is controlled by 0x6B[3],
SL8, it is controlled by 0x6B[5].

For right channel input path
SR1, it is controlled by 0x76[11]DISCHRG and 0x77[14]ACDC_CTRL[0],
SR2, it is controlled by 0x76[11]DISCHRG and 0x77[15]ACDC_CTRL[1],
SR3 and SR4, they are controlled by 0x77[1]FEPGA_MODER,
SR5 and SR6, they are controlled by 0x77[3]FEPGA_MODER,
SR7, it is controlled by 0x6B[2],
SR8, it is controlled by 0x6B[4].

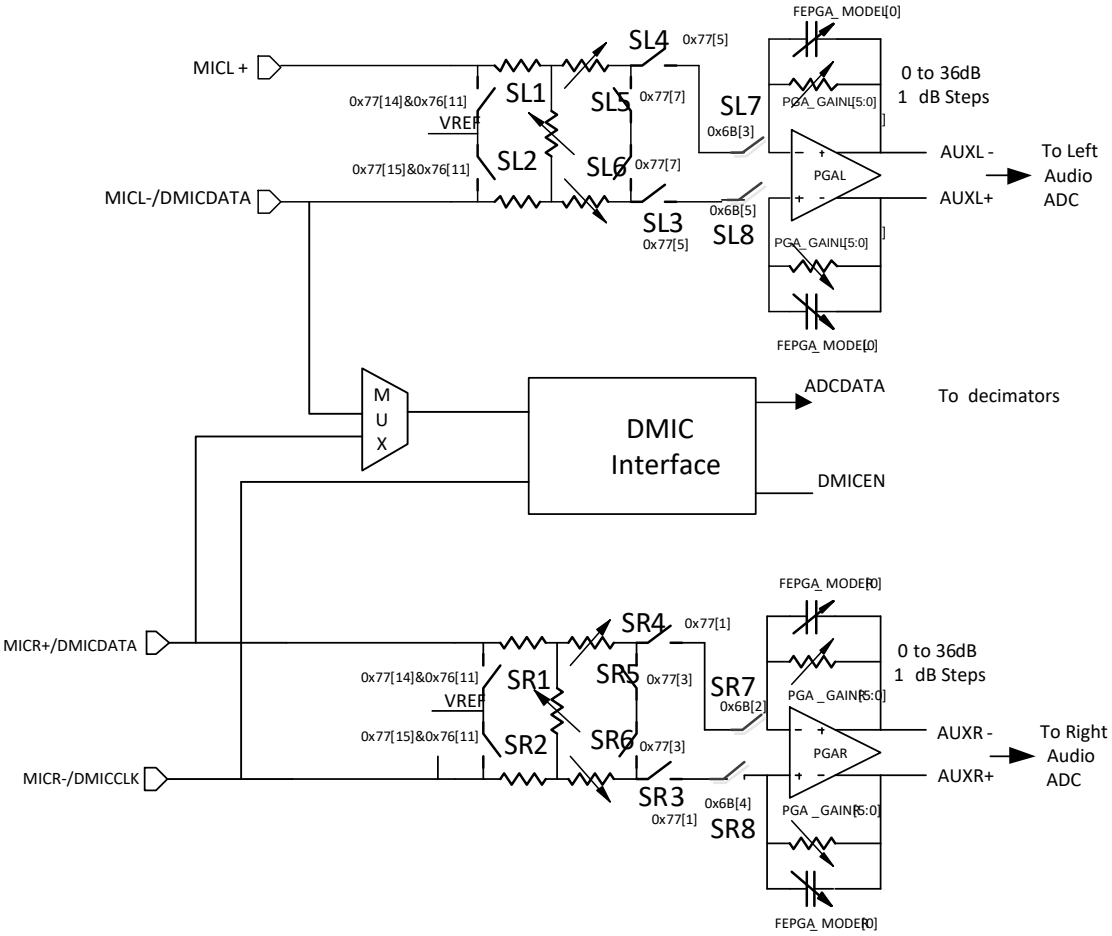



Figure 2: Microphone Input Block Diagram with Registers

## 3.2 Digital Microphone Input

MICL- and MICR+ pins is for the digital microphone data input.
MICR- pin is for the digital microphone clock.

## 3.3 VREF

The NAU88L21C includes a mid-supply reference circuit that produces a voltage close to VDDA/2. This “VREF” pin should be decoupled to VSS through an external bypass capacitor. Because VREF is used as a reference voltage inside the NAU88L21C, a large capacitance is required to achieve good power supply rejection at low frequency. Typically, a value of 4.7µF should be used. This larger capacitance may introduce longer rise time of VREF and delay the line output signal. However, a pre-charge circuit can be supported to help reduce the rise time. Due to the high impedance of the VREF pin, it is important to use a low leakage capacitor. A pre-charge circuit has been implemented to reduce the VREF rise time. Once charged, this can be disabled using to save power or prevent rapid changes in level due to fluctuations in VDDA. The below Table 1 shows the VREF tie-off resister selection.

| VMIDSEL | VREF Resistor Selection | VREF Impedance |
|---|---|---|
| 00 | Open, no resistor selected | Open, no impedance installed |
| 01 | 50kOhm | 25kOhm |
| 10 | 250kOhm | 125kOhm |
| 11 | 5kOhm | 2.5kOhm |

Table 1: VREF Impedance Selection

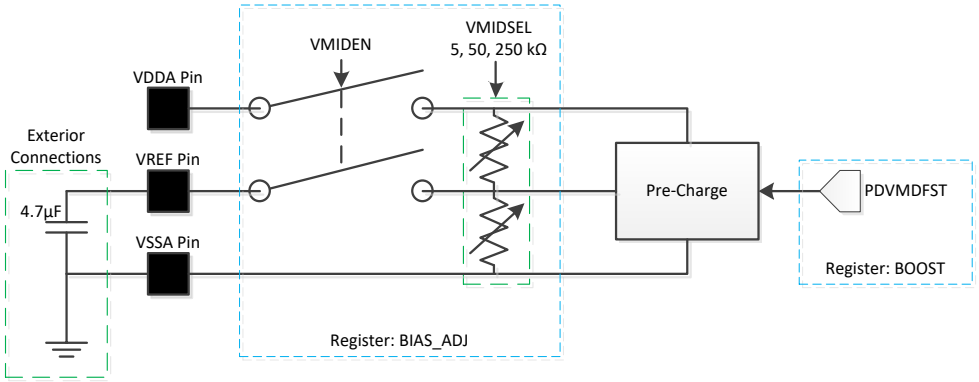



Figure 3: $V_{REF}$ Circuitry

## 3.4 MIC Bias

The NAU88L21C provides one MIC bias pin, which can be used to power various microphones. The output level of MIC Bias can be set between VDDA and 1.53 X VDDA using register settings.

It is recommended that the microphones do not draw more than 4mA from the MICBIAS pin. There are options for connecting internal 2 Kohm resistor to the microphone and for low noise or low power mode. If MICBIAS is used in low power mode, typically 100nF or 200nF capacitor can be used along with MIC Bias level at VDDA. In the low noise mode, external 1uF or 4.7uF capacitor can be omitted by register settings when MIC Bias is used to power analog microphones.

## 3.5 MIC detect

The MIC detect block can detect whether a microphone is connected between the MICBIAS output and the MICDET pin. Either the internal 2kOhm resistor or an external 2kOhm resistor can be used to connect the microphone to the MICDET pin and MICBIAS. See Figure 4, where the internal hookup of the MICDET and MICBIAS blocks is shown.
MICDET de-bounce mode design two options : de-bounce mode and non-debound mode.
de-bounce mode : delay time 16 options, minimum 4ms, maximum 64ms.

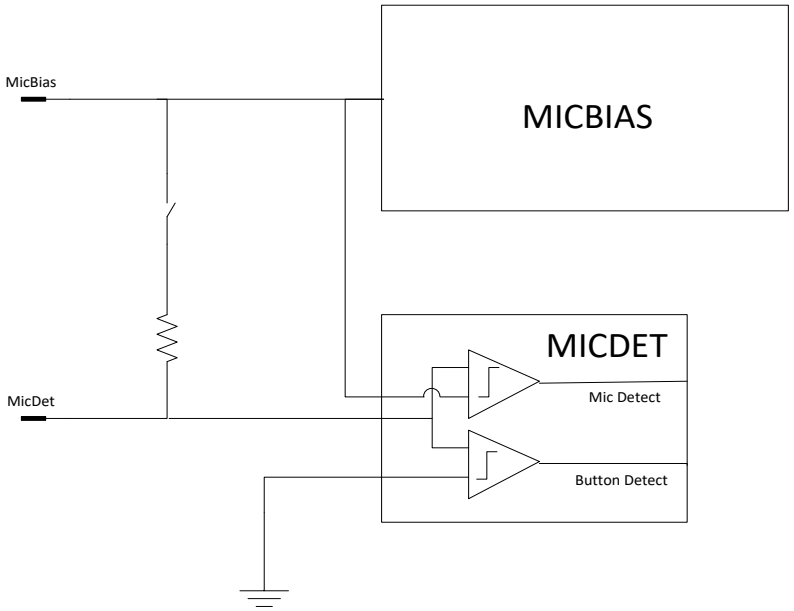



Figure 4 Mic Detect and MICBIAS blocks

Application note: Adding a simple RC on the MICDET pin can help reduce noise coupling. These may be board level related, or component related effects.

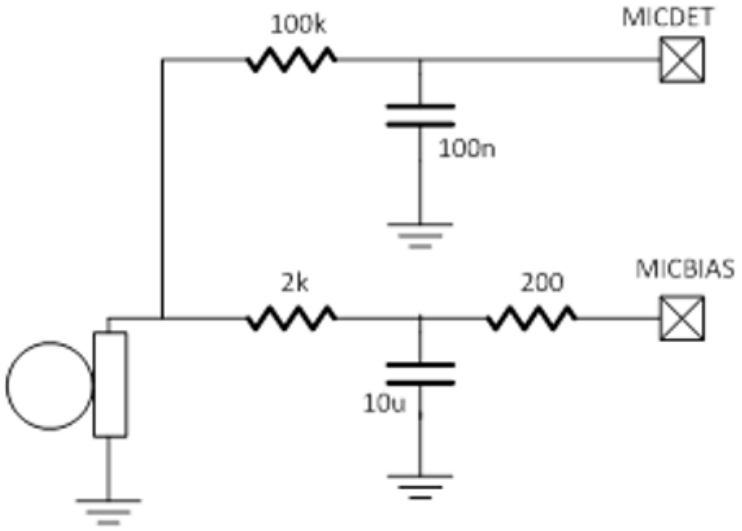



Figure 5 Reducing noise coupling effects

If the optional external 2KOhm resistor is used, then the internal 2K Ohm resistor (Between MICBIAS and MICDET) should be disabled.

### 3.5.1 Key Release

This feature detects the edge case where the key press interrupt is not followed by a release interrupt until later on in the sequence and clears the x11 register to prepare for further interrupts.

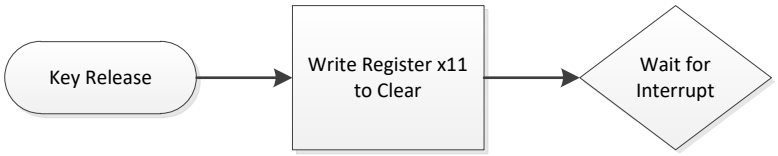



Figure 6. Key Release Flowchart

**Note:**

1. Mic detect current threshold ~ 12.5uA, and voltage threshold = MICBIAS - 26mV. Either condition trigger mic detectons
2. Button (key) detection current throushold larger than 800uA and voltage threshold is GND + 85mA. Either condition trigger button detection.

# 4. ADC Digital Block

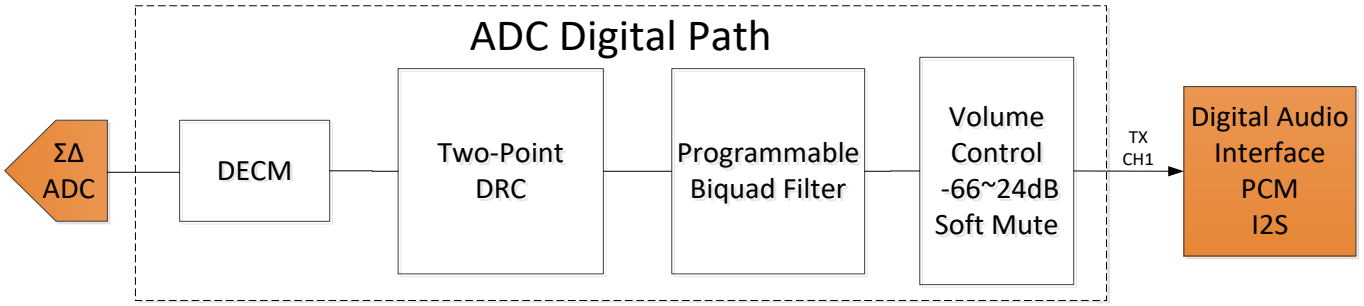



Figure 7: ADC Digital Path

The ADC digital block takes the output of the 24-bit Analog-to-Digital converter and performs signal processing aimed at producing a high quality audio sample stream to the audio path digital interface. The Figure 7 shows the various steps associated with the ADC digital path.

Oversampling is used to improve noise and distortion performance; however this does not affect the final audio sample rate. The oversampling rate configured between 32X and 256X using register settings.
The polarity of either ADC output signal can be changed independently on either ADC logic output as a feature sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data is passed to other stages in the system.
A low latency signal path is supported. Depending on the functional blocks included in the path a min of 4.5/fs may be expected. With all blocks active 6/fs should be expected.

The full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0VRMS.

## 4.1 ADC Dynamic Range Compressors (DRC)

The ADC's in the digital signal path each support a two-point dynamic range compressor (DRC) for advanced signal processing. Each DRC can be programmed to limit the maximum output level and/or boost a low output level signal. The DRC's function consists of level estimation and static curve control.

### 4.1.1 Level Estimation

The NAU88L21C uses Peak level estimation that depends on the attack and decay time settings, which can be programmable by register settings as shown in the Table 2.

| BITS | DRC_PK_COEF1_ADC | DRC_PK_COEF2_ADC |
|---|---|---|
| 0000 | Ts | 63*Ts |
| 0001 | 3*Ts | 127*Ts |
| 0010 | 7*Ts | 255*Ts |
| 0011 | 15*Ts | 511*Ts |
| 0100 | 31*Ts | 1023*Ts |
| 0101 | 63*Ts | 2047*Ts |
| 0110 | 127*Ts | 4095*Ts |
| 0111 | 255*Ts | 8191*Ts |

Table 2: ADC Level Estimation - Attack and Decay Time Register Settings

Please note that Ts is the sampling time given by 1/(Sampling Frequency)

### 4.1.2 Static Curve

The DRC static curve supports up to five programmable sections as shown in the Figure 8.

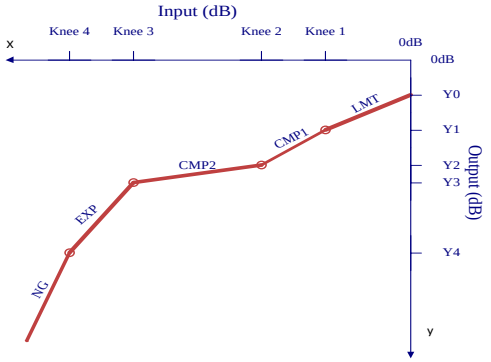



Figure 8: DRC Static Characteristic

Each section on the characteristic (labeled NG, EXP, CMP2, CMP1, and LMT) can be controlled by setting the slope and knee point values, in their respective registers. The table below provides the corresponding register locations.

| Static Curve Section | Slope | Knee Point |
|---|---|---|
| LMT | 0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1 | |
| CMP1 | 0, 1/2, 1/4, 1/8, 1/16, 1 | 0 to -31dB with -1dB step |
| CMP2 | 0, 1/2, 1/4, 1/8, 1/16, 1 | 0 to -63dB with -1dB step |
| EXP | 1, 2, 4 | -18 to -81dB with -1dB step |
| NG | 1, 2, 4, 8 | -35 to -98dB with -1dB step |

Table 3: ADC DRC Static Curve control registers

The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

Y1 = Knee 1
Y0 = Y1 - (Knee 1) * (LMT Slope)
Y2 = (Knee 2 - Knee 1) * (CMP1 Slope) + Y1
Y3 = (Knee 3 - Knee 2) * (CMP2 Slope) + Y2
Y4 = (Knee 4 - Knee 3) * (EXP Slope) + Y3

The attack time and decay time is programmable as shown in the Table 4. And the smooth knee filter can be also enabled by register setting.

| BITS | DRC_ATK_ADC_CH## | DRC_DCY_ADC_CH## |
|---|---|---|
| 0000 | Ts | 63*Ts |
| 0001 | 3*Ts | 127*Ts |
| 0010 | 7*Ts | 255*Ts |
| 0011 | 15*Ts | 511*Ts |
| 0100 | 31*Ts | 1023*Ts |
| 0101 | 63*Ts | 2047*Ts |
| 0110 | 127*Ts | 4905*Ts |
| 0111 | 255*Ts | 8191*Ts |
| 1000 | 511*Ts | 16383*Ts |
| 1001 | 1023*Ts | 32757*Ts |
| 1010 | 2047*Ts | 65535*Ts |
| 1011 | 4095*Ts | |
| 1100 | 8191*Ts | |

Table 4: ADC Attack and Decay Time Register Settings

### 4.1.3 Limitation

Due to DC offsets from the ADC block, DRC performance may have limitation. Especially when DRC is designed with 3 or 4 knee points, output level variation caused by DC offsets should be taken into consideration. Biquad Filter can be set as high pass filter to eliminate DC offsets.

For DRC design with 2 knee points by setting knee2, knee3, knee4 together, DRC output curves of left and right channels typically share the same track as shown below:

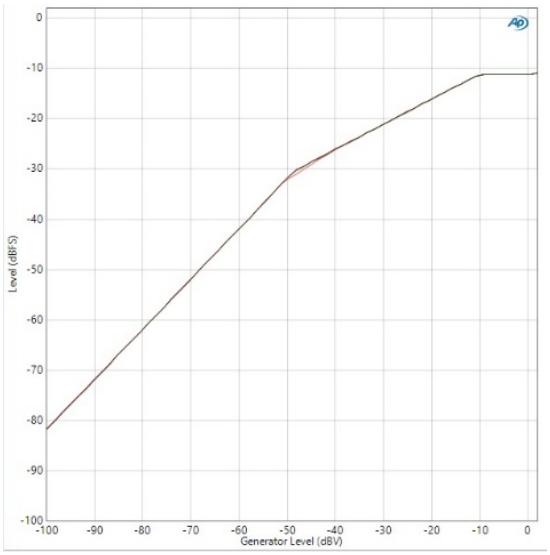



Figure 9: DRC Output Curve with 2 Knee Points

For DRC with 3 or 4 knee points, systematic DC offsets on both channels will become unnegligible. Especially for input level at lower than -50dB, DRC output curves of left and right channels will split into two traces. At -60dB input level, the output level variation may be up to 15dB as shown below:

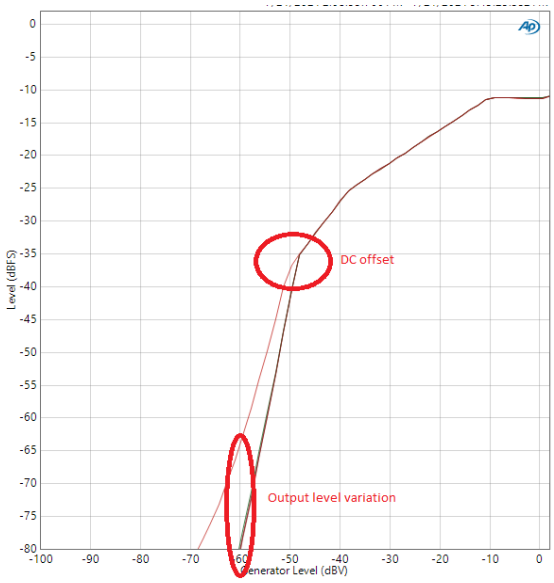



Figure 10: DRC Output Curve with 3 Knee Points

## 4.2 ADC Digital Volume Control

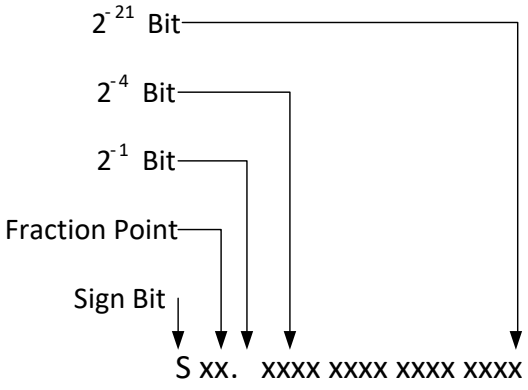
The digital volume control feature allows adjustment of the audio volume coming from ADC using a two-stage volume control. This allows the gain to be adjusted from -66dB to +24dB. Also included is a mute value that will reduce the output signal of the ADCs to zero.

## 4.3 ADC Programmable Biquad Filter

The NAU88L21C has 4 dedicated digital biquad filters. Two for the ADC path, and two for the DAC path. The biquad filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain consists of two quadratic functions:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The coefficients $A_1$, $A_2$, $B_0$, $B_1$, $B_2$ are represented in the 3.21 format described below




Each Biquad Coefficient has 24 bits in Sxx.21 format where

- S is the sign bit (1 bit),
- xx are integers ( 2bits)
- 21 fractional bits (21 bits)

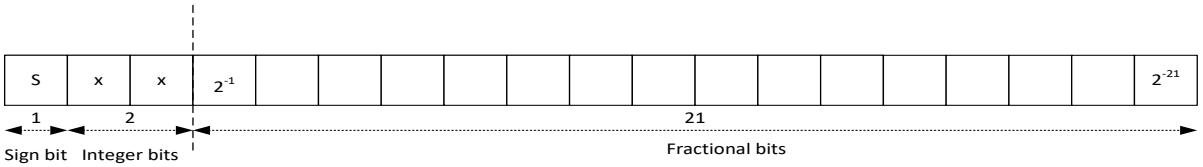



Figure 11: Number format description for biquad filters coefficients

## 4.4 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L21C supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia.

## 4.5 Additional ADC Application Notes

The ADC clock polarity can be inverted if necessary by register setting. It is recommend to match ADC oversampling rate with ADC clock rate as shown in the Table 5.

| 0x2B[2:0]ADC_RATE | 0x3[7:6]CLK_ADC_SRC |
|---|---|
| 000(OSR=32) | 11(CODEC 1/8) |
| 001(OSR=64) | 10(CODEC1/4) |
| 010(OSR=128) | 01(CODEC 1/2) |
| 011(OSR=256) | 00(CODEC CLK) |
| 100(OSR=192) | 01(CODEC 1/2) |
| 101(OSR=384) | 00(CODEC CLK) |

Table 5: ADC_RATE and CLK_ADC_SRC Pairs

# 5. DAC Digital Block

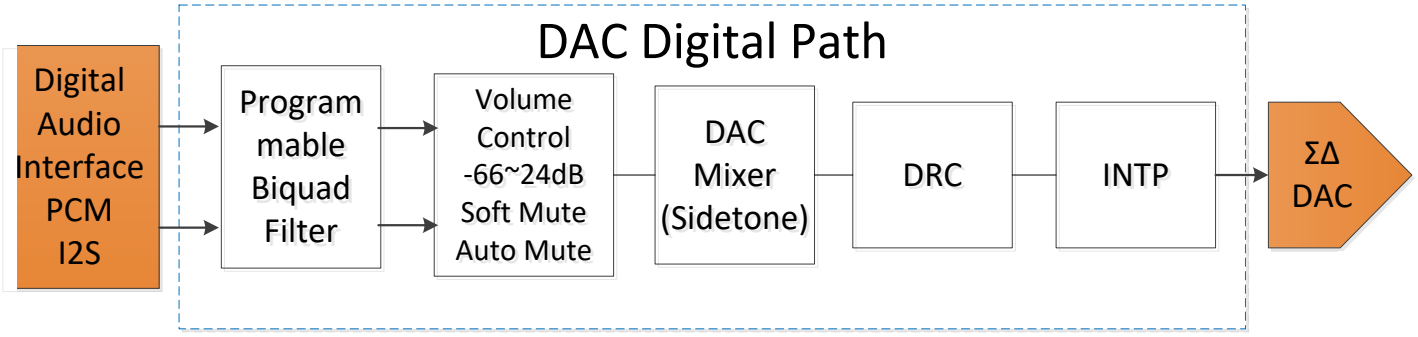



Figure 12: DAC Digital Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, programmable biquad filter, and a DRC. The full-scale output level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0 VRMS. The oversampling rate of the DAC can be changed from 32x to 256x for improved audio performance at higher power consumption. The DAC output signal polarity can be changed using register setting. This can help minimize any audio processing that may be required as the data is passed from other stages of the system.

## 5.1 DAC Dynamic Range Control (DRC)

The DAC DRC functions in the same way as the ADC DRC explained in Section 4.1. However, different control registers are used.

### 5.1.1 Level Estimation

The Table 6 shows the attack and decay times for the peak level estimation. And, the time constant Ts is the the sampling time given by 1/(Sampling Frequency).

| Bits | DRC_PK_COEF1_ADC | DRC_PK_COEF2_ADC |
|---|---|---|
| 0000 | Ts | 63*Ts |
| 0001 | 3*Ts | 127*Ts |
| 0010 | 7*Ts | 255*Ts |
| 0011 | 15*Ts | 511*Ts |
| 0100 | 31*Ts | 1023*Ts |
| 0101 | 63*Ts | 2047*Ts |
| 0110 | 127*Ts | 4095*Ts |
| 0111 | 255*Ts | 8191*Ts |

Table 6: DAC Level Estimation Attack and Decay Time Register Settings

### 5.1.2 Static Curve

The DRC static curve supports five programmable sections, and slope and knee points can be configured as shown in the Table 7.

| Static Curve Section | Slope | Knee Point |
|---|---|---|
| LMT | 0, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1 | |
| CMP1 | 0, 1/2, 1/4, 1/8, 1/16, 1 | 0 to -31dB with -1dB step |
| CMP2 | 0, 1/2, 1/4, 1/8, 1/16, 1 | 0 to -63dB with -1dB step |
| EXP | 1, 2, 4, 8 | -18 to -81dB with -1dB step |
| NG | 1, 2, 4, 8 | -35 to -98dB with -1dB step |

Table 7: DAC DRC Static Curve Control Registers

The Table 8 shows the attack and decay time for DRC. And, it needs to be carefully used combination with cross talk function because DRC is the last blocks in the path after mixer. Small cross-talk signal might be filtered out by DRC. The smooth knee function can be also enabled by register setting.

| BITS | DRC_ATK_DAC | DRC_DCY_DAC |
|---|---|---|
| 0000 | Ts | 63*Ts |
| 0001 | 3*Ts | 127*Ts |
| 0010 | 7*Ts | 255*Ts |
| 0011 | 15*Ts | 511*Ts |
| 0100 | 31*Ts | 1023*Ts |
| 0101 | 63*Ts | 2047*Ts |
| 0110 | 127*Ts | 4095*Ts |
| 0111 | 255*Ts | 8191*Ts |
| 1000 | 511*Ts | 16383*Ts |
| 1001 | 1023*Ts | 32757*Ts |
| 1010 | 2047*Ts | 65535*Ts |
| 1011 | 4095*Ts | |
| 1100 | 8191*Ts | |

Table 8: DAC Static Curve Attack and Delay Time Register Settings

## 5.2 DAC Digital Volume Control, Mute and Channel selection

DACL and DACR both have separate digital volume controls that allow the user to adjust the gain from -66dB to +24dB in 0.5dB steps as well as mutes. Left and Right channels can be adjusted separately and control is accessed through register settings.

## 5.3 DAC Soft Mute

The soft mute function ramps the DAC digital volume down to zero when enabled. When disabled, the volume increases to the register specified volume level for each channel. This feature provides a tool that is useful for using the DAC without introducing pop and click sounds.

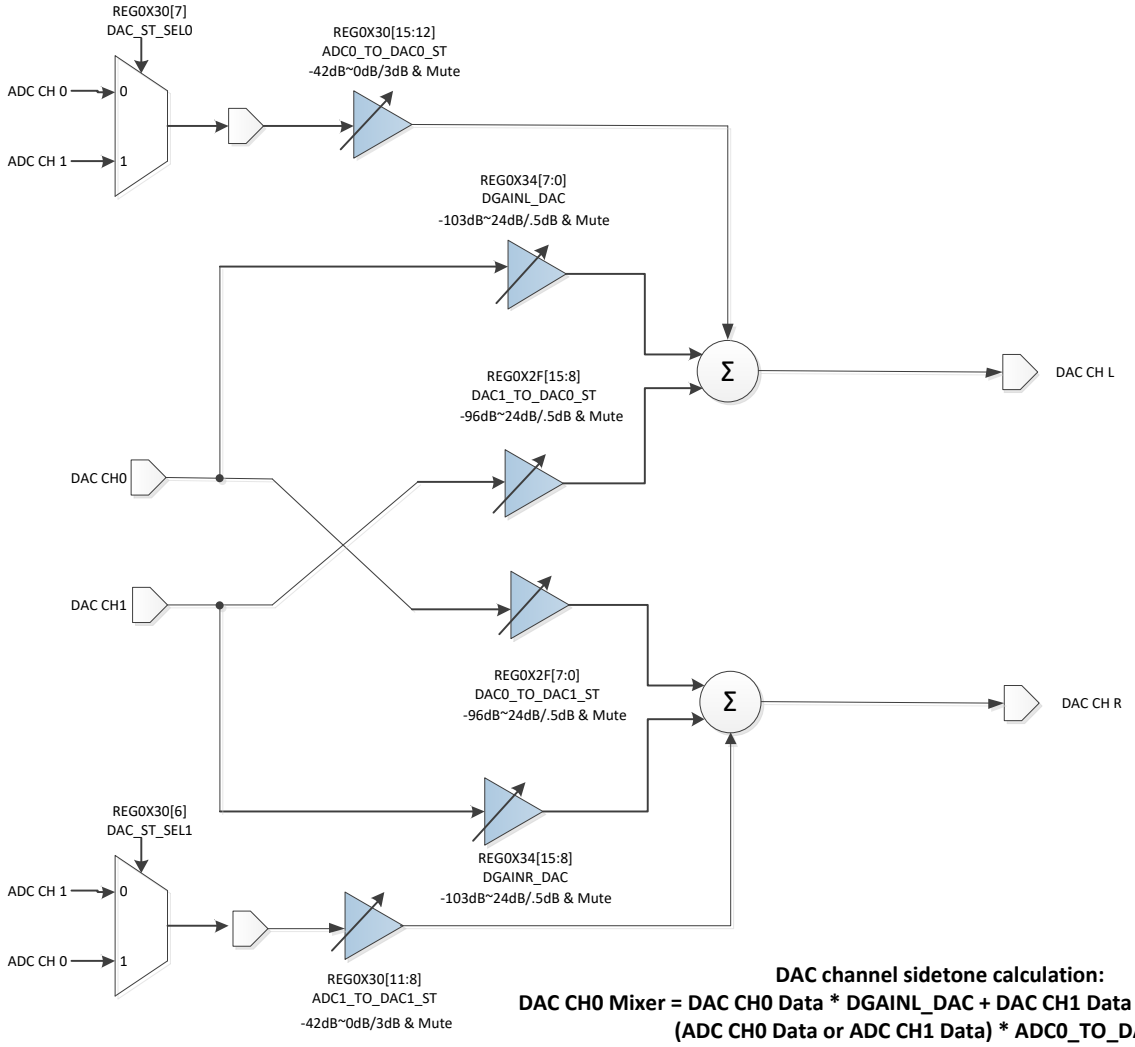
## 5.4 DAC Auto Attenuate

Auto-attenuate can greatly increase the perceived SNR during playback of silence. The last analog output stage is attenuated such that the noise contribution of the preceding stages is eliminated. The use of auto-attenuate by attenuating the analog output on a DAC path when the digital input represents a zero signal needs to be done gradually in order to avoid audible pops due to sudden offset changes. It is desirable to slowly ramp down the gain of the analog output stage to the maximum attenuation level. This function will be referred to as auto-attenuate. The auto-attenuate feature is used to increase the Signal to Noise Ratio. In addition, the auto attenuate logic can be used to attenuate the analog output manually,saving some software routines and allowing pop-less ramp up and down of the analog outputs with little register writes.

The auto-attenuate function can be enabled manually or automatically. In the automatic mode, if both the left and right channel receive 1024 consecutive samples of „0", then it will read and store the value of the headset driver volume control into internal temporary registers and then attenuate the headset driver output by 1dB for every 128 samples, until -54dB is reached (54 steps maximum). If , at any time, the I2S DACIN signal receives non-zero signal samples, the headset output driver gain is increased by 1dB per step and in 1, 16, 32 or 128 samples per step (programmable by register) until the gain will be stepped up until the original gain setting is reached. In the manual mode, once enabled, it will immediately start saving the volume control into temporary registers and attenuate signals by 1dB for every 128 samples untile -54dB is reached. If the manual attenuate is disabled, the gain will be fully recovered by 1dB step in 1, 16, 32, or 128 samples per step.

## 5.5 DAC Path Digital Mixer with Side tone

The NAU88L21C implements a channel based digital mixer architecture. Each DAC outputs can be selected between the different inputs. The ADC input channels, I2S channels are capable of being mixed into either output of the DAC. The figure below shows a block diagram of how the mixer works along with the related registers.




**DAC channel sidetone calculation:**

**DAC CH0 Mixer = DAC CH0 Data * DGAINL_DAC + DAC CH1 Data * DAC1_TO_DAC0_ST + (ADC CH0 Data or ADC CH1 Data) * ADC0_TO_DAC0_ST**

**DAC CH1 Mixer = DAC CH1 Data * DGAINR_DAC + DAC CH0 Data * DAC0_TO_DAC1_ST + (ADC CH1 Data or ADC CH0 Data) * ADC1_TO_DAC1_ST**

Figure 13: DAC Path Digital Mixer with Side tone.

## 5.6 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L21C supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 14 bits (μ-law) or 13 bits (A-law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. When the companding mode is enabled, 8 bit word operation must be enabled.

Sections 5.6.1 and 5.6.2 contain the compression equations set by the ITU-T G.711 standard and implemented in the NAU88L21C.

### 5.6.1 μ-law

$$F(x) = \frac{\ln(1+\mu\times|x|)}{\ln(1+\mu)}, \quad -1 < x < 1$$

$$\mu = 255$$

### 5.6.2 A-law

$$F(x) = \frac{A\times|x|}{(1+\ln(A))}, \quad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1+\ln(A\times|x|)}{(1+\ln(A))}, \quad \frac{1}{A} \le x \le 1$$

$$A = 87.6$$

# 6. ADC and DAC Digital Filter Options

NAU88L21C provides options for various decimation filters selection at ADC path and interpolation filters at DAC path. There are five digital filter types for ADC and DAC: sharp roll-off long delay (SPRFLD), sharp roll-off long delay linear phase (SPRFLD linear), slow roll-off short delay linear phase (SLRFSD linear), sharp roll-off short delay non-linear phase (SPRFSD non-linear), and slow roll-off short delay non-linear phase (SLRFSD non-linear).

ADC filter type selection is located at REG0x2B[13:11], and DAC's is at REG0x2C[10:8]. Default value is 3b'000 for both ADC and DAC, the selection filter has the sharpest roll-off frequency response but the longest group delay. Selected filter with known sampling rate, group delay can be estimated. Group delay estimation is equal to Delay Factor /Fs;

**Estimated Group Delay= Delay Factor / Fs**

For example, at ADC path at Fs=48KHz, if using default filter with Fs=48KHz, then estimated group delay is 29.1/48000Hz=606us. Table 9 shows ADC and DAC group delay vs filter setting.

| ADC path | Group Delay |
|---|---|
| SPRFLD | 29.1/fs |
| SPRFLD linear | 20.5/fs |
| SLRFSD linear | 9.5/fs |
| SPRFSD non-linear | 4.7/fs |
| SLRFSD non-linear | 4.4/fs |
| **DAC path** | **Group Delay** |
| SPRFLD | 32/fs |
| SPRFLD linear | 20.7/fs |
| SLRFSD linear | 9.7/fs |
| SPRFSD non-linear | 7.2/fs |
| SLRFSD non-linear | 5.7/fs |

**Table 9 ADC and DAC Group Delay**

The I2S interface will take 1/fs, so the total group delay without biquad filter and DRC would be (digital filter delay factor+1)/fs.

# 7. Clocking and Sample Rates

The internal clocks for the NAU88L21C are derived from a common internal clock source. This master system clock can set directly by the MCLK pin input or it can be generated from a Frequency Locked Loop (FLL) using the MCLK_PIN, BCLK or FS as a reference. While most of the common audio sample rates can be derived directly from typical MCLK frequencies, the FLL provides additional flexibility for a wide range of MCLK inputs or as a free running clock in the absence of an external reference.

The figures below is a block diagram illustrating how the various register settings can be used to adjust/select the MCLK, BCLK, FS, and ADC_CLK clock frequency.

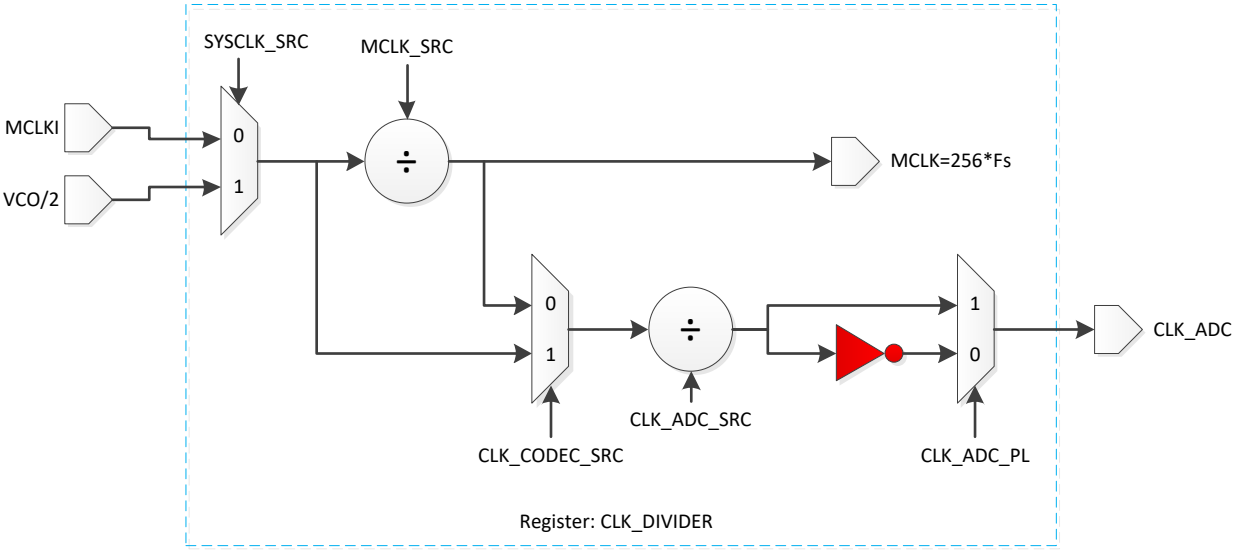



**Figure 14: MCLK and ADC_CLK Frequency Selection**

| Bits | 0x3[3:0]MCLK_SRC |
|---|---|
| 0000 | Divide by 1 |
| 0001 | Invert |
| 0010 | Divide by 2 |
| 0011 | Divide by 4 |
| 0100 | Divide by 8 |
| 0101 | Divide by 16 |
| 0110 | Divide by 32 |
| 0111 | Divide by 3 |
| 1000 | 1 |
| 1001 | Invert |
| 1010 | Divide by 6 |
| 1011 | Divide by 12 |
| 1100 | Divide by 24 |
| 1101 | Divide by 48 |
| 1110 | Divide by 96 |
| 1111 | Divide by 5 |

Table 9: Register Settings

| Bits | CLK_ADC_SRC |
|---|---|
| 00 | Divide by 1 |
| 01 | Divide by 2 |
| 10 | Divide by 4 |
| 11 | Divide by 8 |

**Table 10: Register Settings**

The internal clock frequency MCLK can run at 256, 384, 400, or 500*Fs (Fs = sample rate in Hz) four groups as shown below Table. Available Fs range and maximum MCLK are also shown. Higher than upper bounded MCLK and Fs exceed NAU88L21C operation limitation, and performance cannot guarantee.

Applying the Table 11 with Fs=48 kHz sample rate, MCLK must be set to 256*48k = 12.288MHz for MCLK/Fs ratio=256; 400*48k = 19.2MHz when MCLK/Fs=400; 24MHz when MCLK/Fs=500; however, it is not avialble for MCLK/Fs=384 because 48KHz exceeds the upper bounded Fs, 32KHz is the maximum Fs when MCLK/Fs=384.

| Group1: MCLK /Fs Ratio of 256 | |
|---|---|
| FS | 8/16/24 ..44.1/96KHz |
| MCLK | Fs*256 |
| MCLK(max) | 24.576 MHz |
| **Group2: MCLK/Fs Ratio of 384** | |
| Fs | 8/16/24/32KHz |
| MCLK | Fs*384 |
| MCLK(max) | 12.288MHz |
| **Group3: MCLK/Fs Ratio of 400** | |
| FS | 8/16/24 ..44.1/48KHz |
| MCLK | Fs*400 |
| MCLK(max) | 19.2Mhz |
| **Group 4: MCLK /Fs Ratio of 500** | |
| Fs | 8/16/24 ..44.1/48KHz |
| MCLK | Fs * 500 |
| MCLK(max) | 24Mhz |

**Table 11: Applicable MCLK and Fs information based MCLK/Fs ratio**

OSR (over sampling rate) is defined as CLK_ADC frequency divided by the audio sample rate.

$$OSR = \frac{CLK_ADC}{Fs}$$

Available over-sampling rates are 32, 64, 100, 128, 192, 256, or 384 as set in the **ADC_RATE.ADC_RATE REG0X2B[2:0]** register. CLK_ADC frequency is set by **CLK_DIVIDER.CLK_CODEC_SRC REG0X03[13]** and **CLK_DIVIDER.CLK_ADC_SRC REG0X03[7:6]** registers.
It should be noted that the OSR and Fs must be selected so that the max frequency of CLK_ADC is less than or equal to 6.144MHz. When CLK_ADC is determined, **ADC_RATE.ADC_RATE REG0X2B[2:0]** should be set to provide appropriate down sampling through digital filters.

There are two special cases in which the OSR will be 100. MCLK/Fs=400 or 500. If MCLK is 400 times the input sample rate of the DAC or the output sample rate of the ADC, the OSR will be 100. In the first case, set **CLK_DIVIDER.CLK_ADC_SRC_REG0X3[7:6]**=2'b10 (1/4) for ADC path, and DAC path need to set **CLK_DIVIDER.CLK_DAC_SRC_REG0X3[5:4]**=2'b10 (1/4) and **DAC_RATE.DAC_CTRL1_REG0X2C[2:0]**=3b'000. When MCLK/Fs=500, the clock to the ADC will be adjusted automatically.

| ADC/DAC CLK (OSR*Fs) MHz | OSR / Fs | 8 | 16 | 24 | 32 | 44.1 | 48 | 96 | 192 |
|---|---|---|---|---|---|---|---|---|---|
| | 32 | 0.256 | 0.512 | 0.768 | 1.024 | 1.4112 | 1.536 | 3.072 | 6.144 |
| | 64 | 0.512 | 1.024 | 1.536 | 2.048 | 2.8224 | 3.072 | 6.144 | |
| | 100 | 0.8 | 1.6 | 2.4 | 3.2 | 4.41 | 4.8 | | |
| | 128 | 1.024 | 2.048 | 3.072 | 4.096 | 5.6448 | 6.144 | | |
| | 192 | 1.536 | 3.072 | 4.608 | 6.144 | | | | |
| | 256 | 2.048 | 4.096 | 6.144 | | | | | |
| | 384 | 3.072 | 6.144 | | | | | | |

**Table 12: ADC/DAC operation clocks vs OSR and sampling rate**

**Example 1:**
To configure Fs = 48 kHz, MCLK = (256*Fs) = 12.288MHz, and CLK_ADC = 6.144MHZ
Set:

- SYSCLK_SRC = MCLK
- CLK_ADC_SRC = 1/2
- ADC OSR = 128

**Example 2:**
To configure Fs = 16 kHz, MCLKI = 12.288MHz, and CLK_ADC = 4.096MHz
Set:

- SYSCLK_SRC = MCLK
- MCLK_SRC = 1/3
- CLK_ADC_SRC = 1
- ADC OSR = 256

## 7.1 I2S/PCM Clock Generation

In master mode, BCLK can be derived from MCLK via a programmable divider, and the FS can be derived from BCLK via another programmable divider.

To select specific Fs values, both dividers must be set according to the block diagram and the equation below.

$$BCLK = Fs \times data\ length \times channels$$

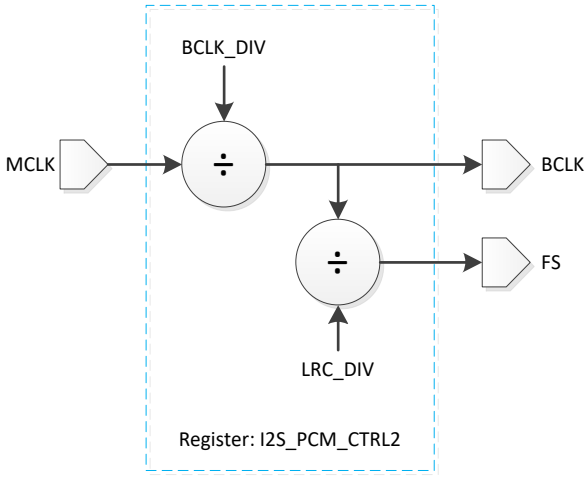



**Figure 15: BCLK and FS Frequency Selection**

| Bits | BCLK_DIV |
|---|---|
| 000 | Divided by 1 |
| 001 | Divided by 2 |
| 010 | Divided by 4 |
| 011 | Divided by 8 |
| 100 | Divided by 16 |
| 101 | Divided by 32 |

**Table 13: Register Settings**

| Bits | LRC_DIV |
|---|---|
| 00 | Divided by 256 |
| 01 | Divided by 128 |
| 10 | Divided by 64 |
| 11 | Divided by 32 |

**Table 14: Register Settings**

**Example 1:**
If we want an Fs of 48 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 48000*16*2 = 1.536MHz and MCLK = 48000*256 = 12.288MHz
- Set BCLK_DIV = 1/8
- Set LRC_DIV = 1/32

Or 32 bit data is to be sent

- BCLK = 48000*32*2 = 3.073MHz and MCLK = 48000*256 = 12.288MHz
- Set BCLK_DIV = 1/4
- Set LRC_DIV = 1/64

**Example 2:**
If we want an Fs of 16 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 16000*16*2 = 512kHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/8
- Set LRC_DIV = 1/32

32 bit data is to be sent,

- BCLK = 16000*32*2 = 1.024MHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/4
- Set LRC_DIV = 1/64
-

**Example 3:**
If we want an Fs of 16 kHz and 32 bit data is to be sent to the I2S TDM bus (4 channels)

- BCLK = 16000*32*4 = 2.048MHz and MCLK = 16000*256 = 4.096MHz
- Set BCLK_DIV = 1/2
- Set LRC_DIV = 1/128

## 7.2 Frequency Locked Loop(FLL)

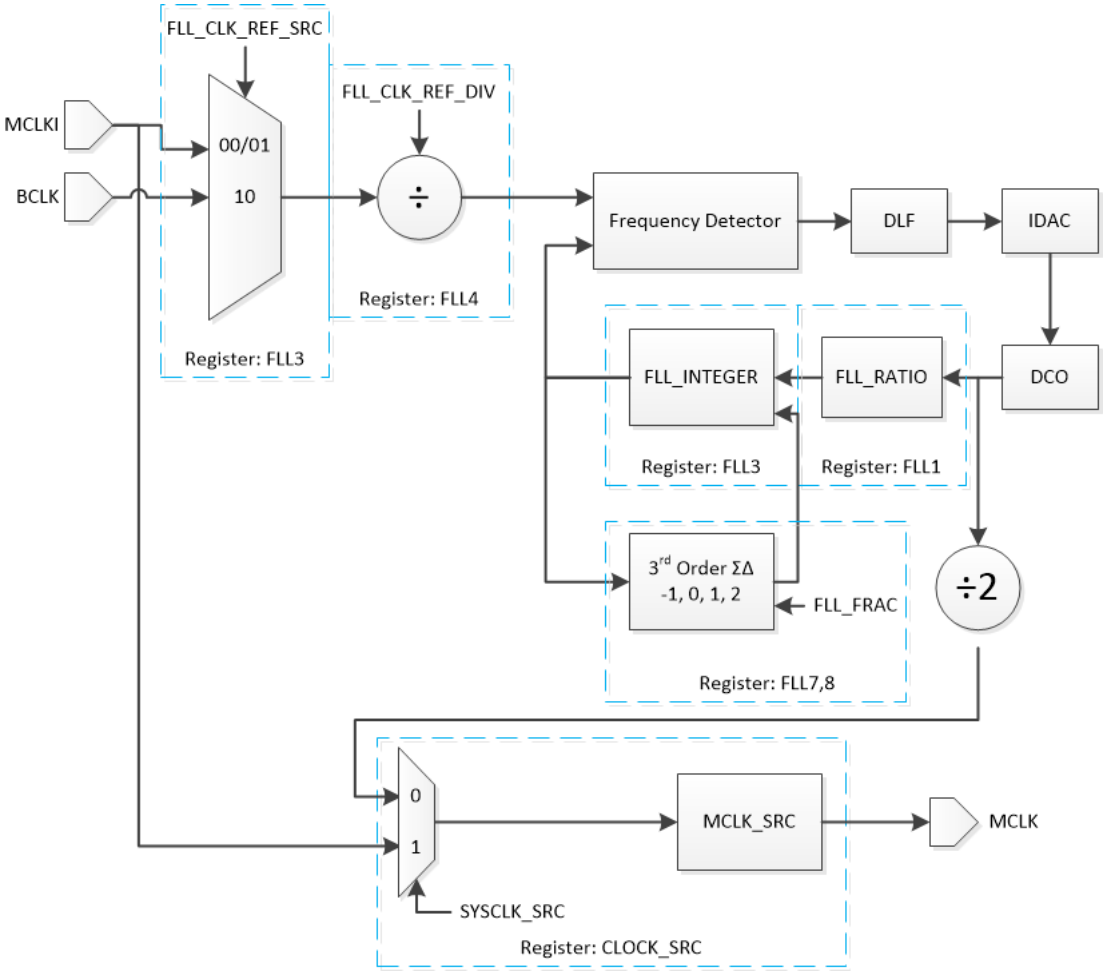



**Figure 16: FLL Block diagram**

The integrated FLL can be used to generate a SYSMCLK from a wide variety of reference sources such as, MCLK, BCLK, and FS or as a free running clock in the absence of an external reference. It can also create a stable SYSMCLK from less stable sources due to its tolerance of jitter.
The FLL output frequency is determined by the following parameters.

- FLL_RATIO based on input clock frequency
- MCLK_SRC Divider

- FLL_INTEGER: 10 bit Integer Input
- FLL_FRAC: 16 bit Fractional Input
- FLL_CLK_REF_DIV Divider

To determine these settings, the following output frequency equations are used.

1. FDCO = (FREF / FLL_CLK_REF_DIV) X FLL_INTEGER.FLL_FRAC X FLL_RATIO
2. MCLK = (FDCO X MCLK_SRC) / 2

Where FREF is the reference clock frequency for FLL, MCLK is the desired system frequency, and FDCO is the frequency of DCO in decimal.

**Example:**
If the reference frequency (FREF) is 12MHz, the desired sampling rate (Fs) is 48 kHz, and SYSCLK = 256Fs, what are the output frequency parameters?

Using these requirements, the following can be determined.

- MCLK = 256 × 48kHz = 12.288MHz
- Using Equation 2:
  - FDCO = 2 X MCLK / MCLK_SRC = 2 X 12.288MHz X MCLK_SRC
    - For FDCO to remain between 90MHz – 100MHz, MCLK_SRC must be chosen to be 1/4. This and other values for MCLK_SRC can be seen on the register tables.
  - FDCO = (2 × 12.288MHz) / (1/4) = 98.304MHz
- Using Equation 1:
  - FLL_INTEGER.FLL_FRAC = FDCO X FLL_CLK_REF_DIV / (FREF X FLL_RATIO)
    - FDCO = 98.304MHz
    - FLL_RATIO = 1 because of FREF ≥ 512 kHz.
    - FLL_CLK_REF_DIV = 1 since FREF = MCLKI (12MHz)
  - FLL_INTEGER.FLL_FRAC = 98.304MHz X 1 / (12MHz X 1) = 8.192
- Now retrieve or convert the parameter values into their corresponding HEX values
  - FLL_RATIO = 1 (for input clock frequency ≥ 512Khz)
  - MCLK_SRC = 1/4
  - FLL_INTEGER = 8
  - FLL_FRAC = 0.192 = 3,221,225 (0.192 x 2^24) = 24'h3126E9

Please Note:

- FLL_CLK_REF_DIV can be used to reduce the reference frequency for SYSMCLK by dividing the input by 1, 2, 4, or 8. Use this to ensure the reference clock frequency is less than or equal to 13.5MHz.
- FDCO must be within the 90MHz – 100MHz or the FLL cannot be guaranteed across the full range of operation.
- FLL_FRAC must be set to 0 for low power mode.

- FLL6.SDM_EN REG0X09[14] to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption.
- When FLL uses free running mode, NAU88L21C needs to be set as a master in I2S_PCM_CTRL2.MS0 REG0X1D[3]=1
- Set FLL6.CHB_FILTER_EN REG0X08[14] = '1' to enable FLL Loop Filter. Select filter clock source by FLL6.CHB_FILTER¬_EN REG0X08[13]. Select DCO input by FLL6.FILTER_SW REG0X08[12]. FLL6.CUTOFF500 REG0X09[13] & FLL6.CUTOFF600 REG0X09[12] can be used to define FLL cuttoff frequency at 500KHz or 600KHz. 500KHz will provide the best FLL performance but consume more power.
- set FLL6.FLL_FLTR_DITHER_SEL REG0X09[7:6] = '01' or '10' or '11' as 1LSB / 2LSB / 3LSB random bits to Randomize the number of Filter Output Bits to average out output noise. If '00', there is no dither.

# 8. Control Interfaces

The NAU88L21C includes a serial control bus that provides access to all the device control registers, it may be configured as a 2-wire interface that conforms to industry standard implementations of the I²C serial bus protocol.

## 8.1 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and any device receiving data as the receiver (or slave). The NAU88L21C can function only as a slave when in the 2-wire interface configuration.
To enable 2-wire I2C Style interface,

(1) Set register 0x1A &= 0xFF00 (Set 0x1A[7:0] = 8'b00000000)
(2) Externally pull GPIO1/CSB pin = LOW (0V) , I2C device address = 0x1B; Or externally pull GPIO1/CSB pin = HIGH (3.3V) , I2C device address = 0x54

## 8.2 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

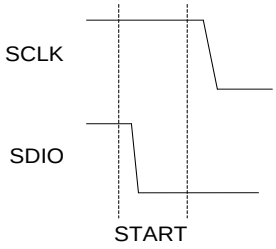



**Figure 17: Valid START Condition**

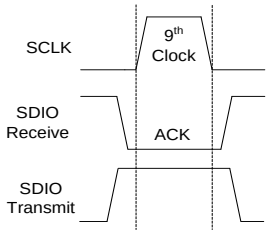



**Figure 18: Valid Acknowledge**

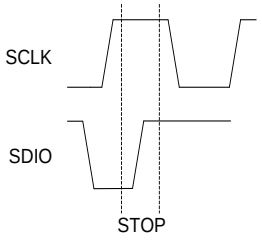



**Figure 19: Valid STOP Condition**

Please Note:

- Sometimes, I2C needs to use level shifter between different supplies domains. During Acknowledge, receiver side (CODEC) will pull low, and transmit side (MCU) is disable and pull high by pull high resistor. Because NAU88L21C SDIO can sink 2mA by default setting (maximum up to 8mA,) shown as below Figure 20, $R_{PU1}$ and $R_{PU2}$ need to be select such that total current VDDB/$R_{PU1}$+ VDD_MCU/$R_{PU2}$ during Acknowledge should not be too large to exceed SDIO sinking capability.

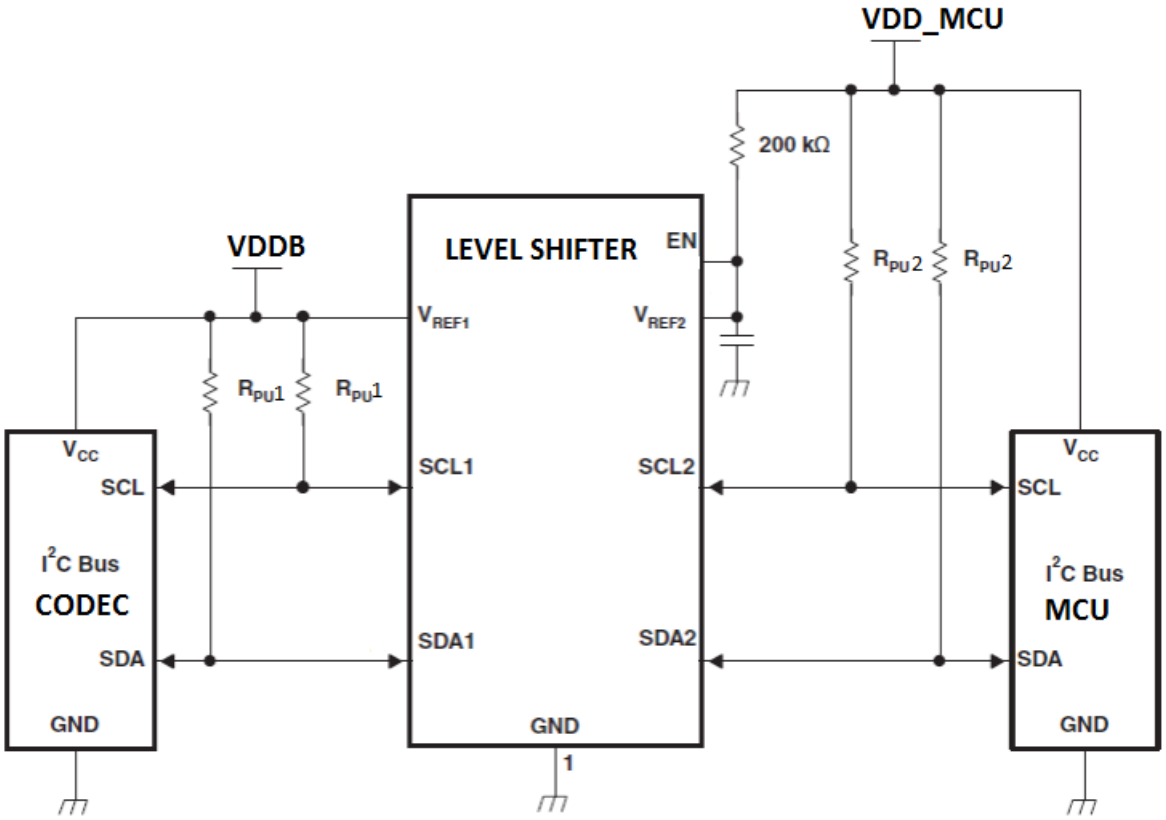



**Figure 20: Typical I2C level shifter circuit**

## 8.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The Device Address of the NAU88L21C is either 0x1B (CSB=0) or 0x54 (CSB=1). If the Device Address matches this value, the NAU88L21C will respond with the expected ACK signaling as it accepts the data being transmitted to it.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 1 | 1 | 0 | 1 | 1 | R/W | Device Address Byte |
| A15 | A14 | A13 | A12 | A11 | A10 | A9 | A8 | Control Address Bytes |
| A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | |
| D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | Data Bytes |
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |

**Figure 21: Slave Address Byte, Control Address Byte, and Data Byte**

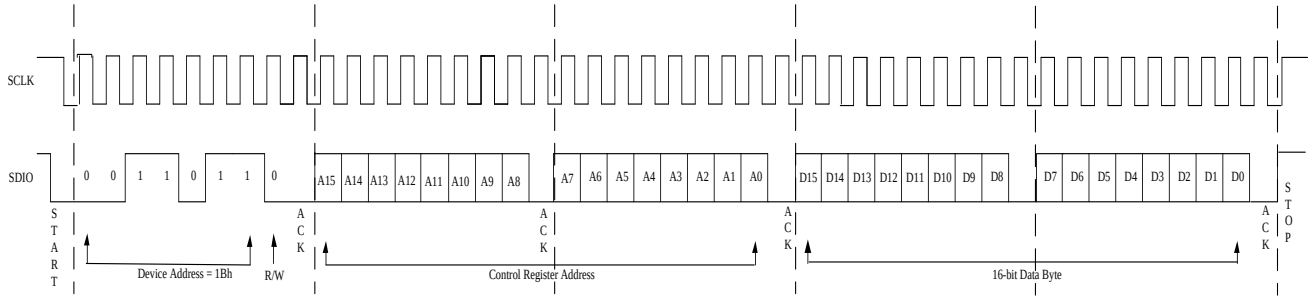



**Figure 22:2-Wire Write Sequence**

## 8.4 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU88L21C will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU88L21C transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU88L21C.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU85L40. If there is no STOP signal from the master, the NAU88L21C will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU88L21C reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

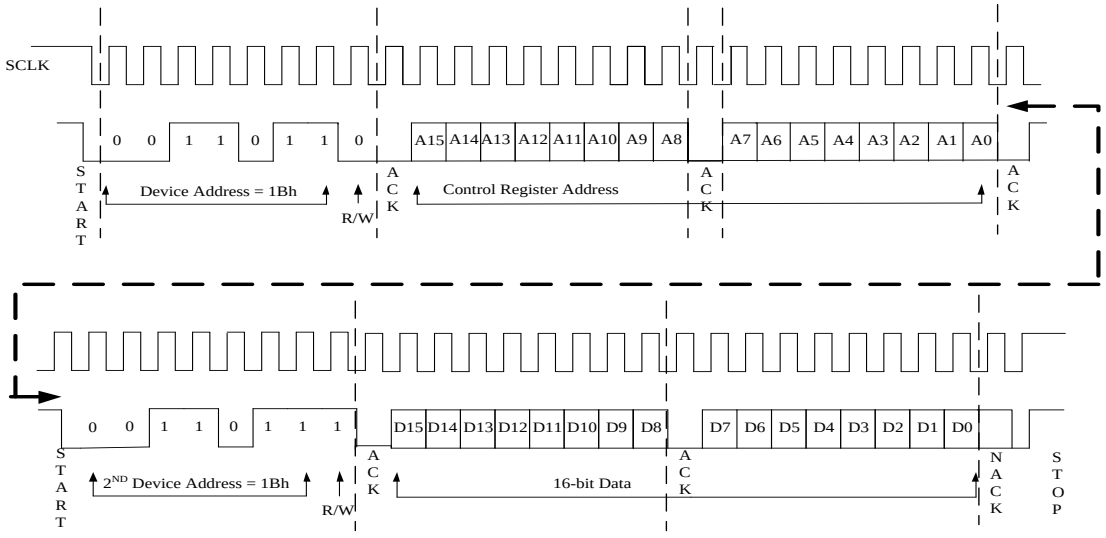



**Figure 23:2-Wire Read Sequence**

## 8.5 Digital Serial Interface Timing

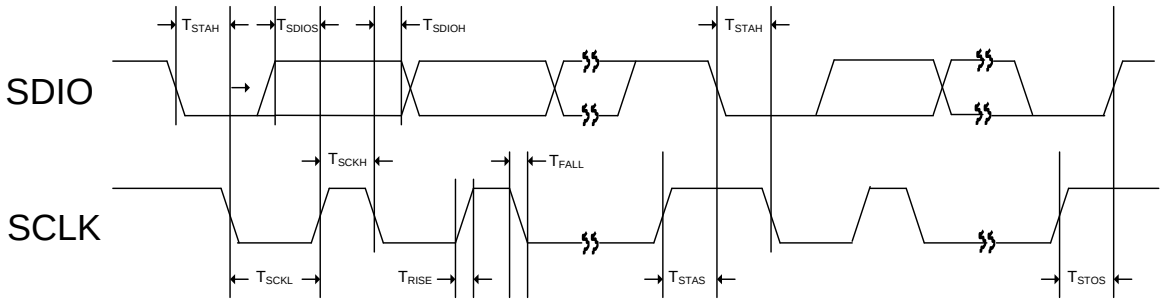



**Figure 24: Two-wire Control Mode Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{STAH}$ | SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition | 600 | - | - | ns |
| $T_{STAS}$ | SCLK rising edge to SDIO falling edge setup timing in Repeat START condition | 600 | - | - | ns |
| $T_{STOS}$ | SCLK rising edge to SDIO rising edge setup timing in STOP condition | 600 | - | - | ns |
| $T_{SCKH}$ | SCLK High Pulse Width | 600 | - | - | ns |
| $T_{SCKL}$ | SCLK Low Pulse Width | 1,300 | - | - | ns |
| $T_{RISE}$ | Rise Time for all 2-wire Mode Signals | - | - | 300 | ns |
| $T_{FALL}$ | Fall Time for all 2-wire Mode Signals | - | - | 300 | ns |
| $T_{SDIOS}$ | SDIO to SCLK Rising Edge DATA Setup Time | 100 | - | - | ns |
| $T_{SDIOH}$ | SCLK falling Edge to SDIO DATA Hold Time | 0 | - | 600 | ns |

**Table 15 Digital Serial Interface Timing Parameters**

## 8.6 Software Reset

The NAU88L21C and all of its control registers can be reset to “default”, initial conditions by writing any value to REG0x00 using the two-wire interface mode.

# 9. Digital Audio Interfaces

The NAU88L21C can be configured as either the master or the slave, and the Slave mode is the default if this bit is not written. In master mode, NAU88L21C outputs both Frame Sync (FS) and the audio data bit clock (BCLK) and has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs.

When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the time slot function is enabled (see below), there are additional output state modes including controlled tristate capability.
NAU88L21C supports six audio formats; right justified, left justified, I2S, PCMA, PCMB, and PCM Time Slot.

## 9.1 Digital Audio Interface

### 9.1.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the image below.

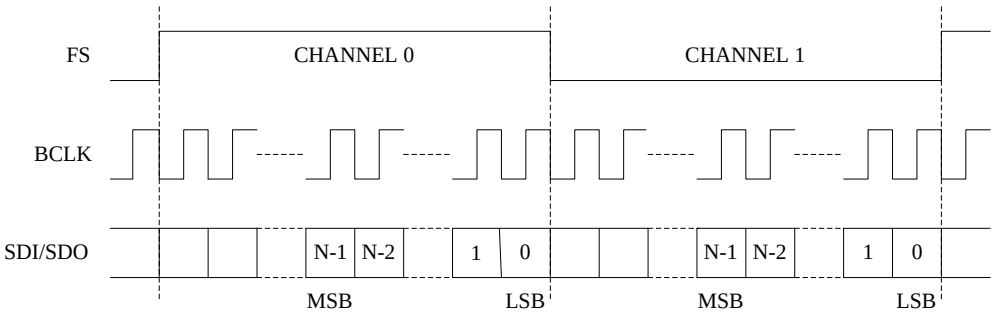



**Figure 25: Right-Justified Audio Interface**

### 9.1.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen in the figure below.

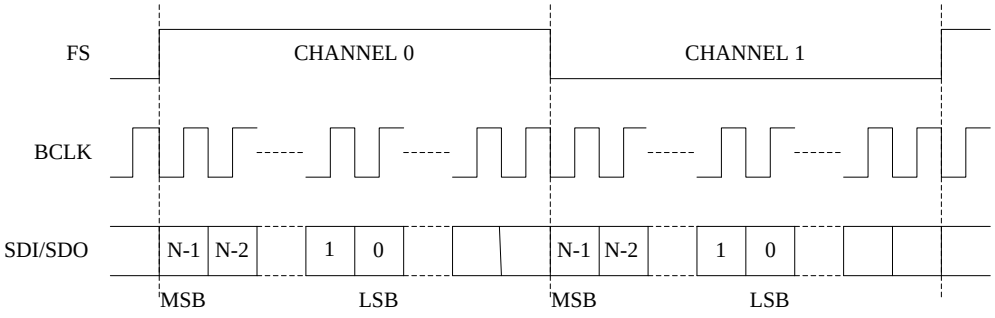



**Figure 26: Left-Justified Audio Interface**

### 9.1.3 I2S Audio Data

In I²S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This can be seen in the figure below.

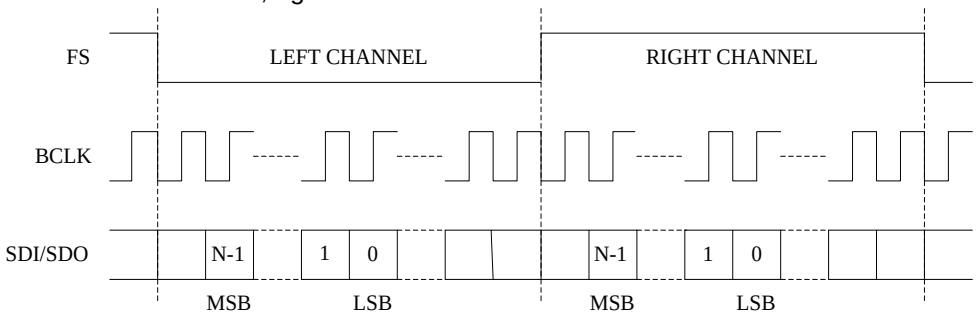



**Figure 27: I2S Audio Interface**

### 9.1.4 PCMA Audio Data

In the PCM A mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after the left channel LSB. This can be seen in the figure below.

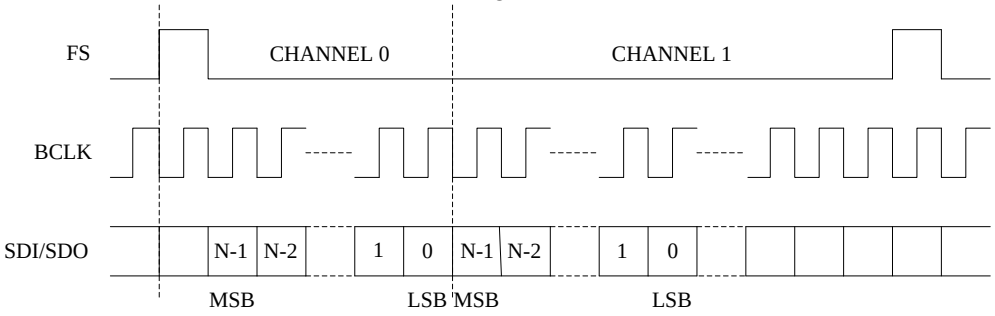



**Figure 28: PCMA Audio Interface**

### 9.1.5 PCMB Audio Data

In the PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next BCLK after channel_0 LSB. This can be seen in the figure below.

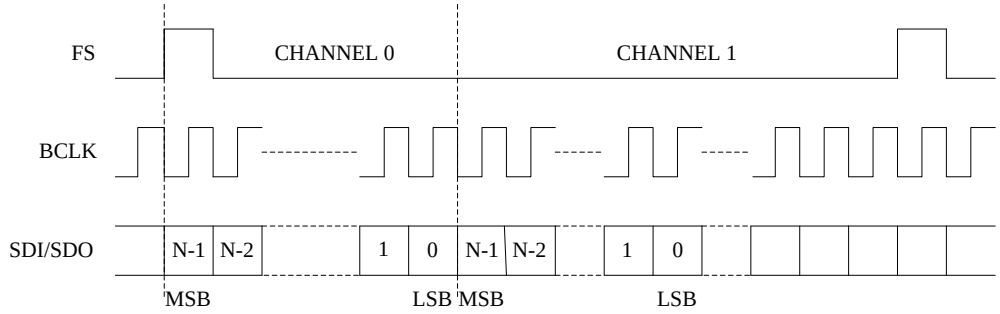



**Figure 29: PCMB Audio Interface**

## 9.1.6 PCM Time Slot Audio Data

The PCM time slot mode is used to allocate different time slots for ADC and DAC data. This can be useful when multiple NAU88L21C chips or other devices are sharing the same audio bus. This will allow each chip"s audio to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode; the audio data can be delayed by left / right channel PCM time slot start value in the registers.
These delays can be seen before the MSB in the figure below.

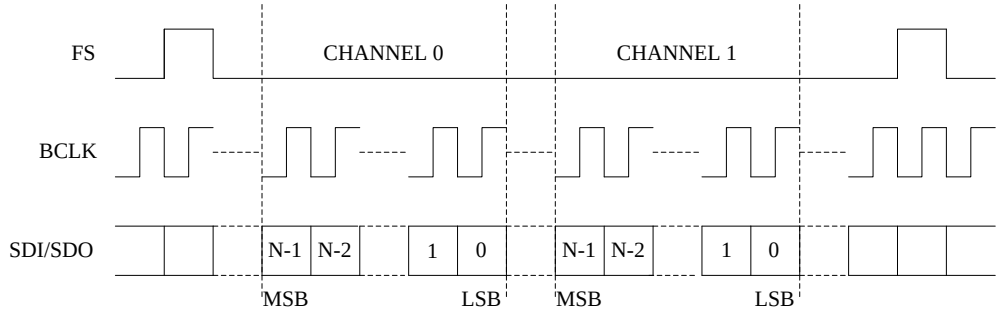



**Figure 30: PCM Time Slot Audio Interface**

The PMC time slot mode can be also used to swap channel 0 and channel 1 audio or cause both channels to use the same data. When using the NAU88L21C with other driver chips, the SDO pin can be set to pull up or pull down or high impedance during no transmission. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

## 9.1.7 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel_0 then channel_2 data is transmitted and when FS is HIGH, channel_1 then channel_3 data is transmitted. This is shown in the figure below.

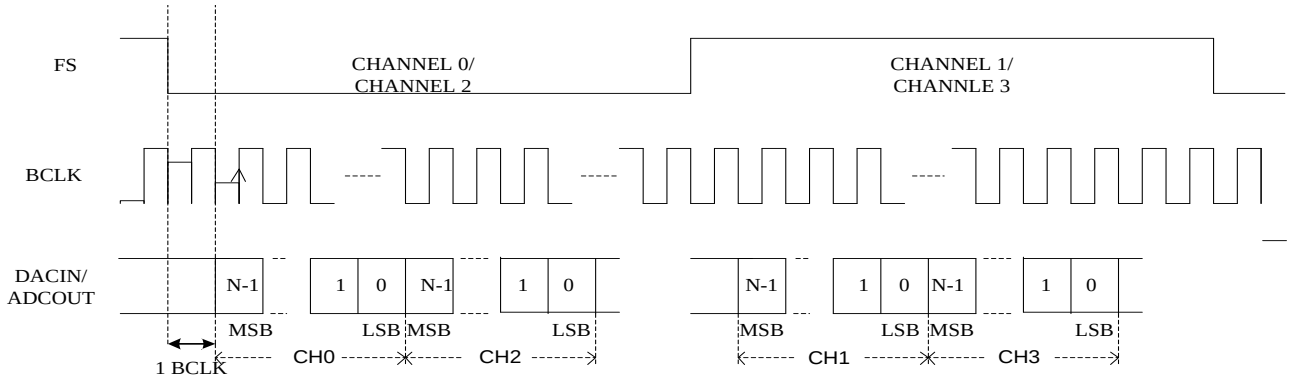



**Figure 31: TDM I2S Audio Format**

## 9.1.8 TDM PCMA Audio Data

In the PCMA mode, channel_0 data is transmitted first followed sequentially by channel_1, 2, and 3 immediately after. The channel_0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

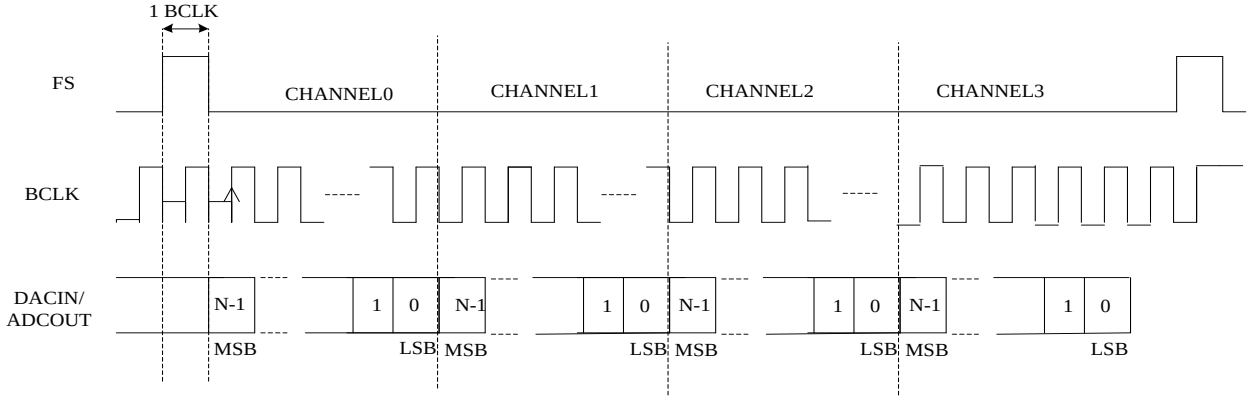



**Figure 32: TDM PCMA Audio Format**

## 9.1.9 TDM PCMB Audio Data

In TDM PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. The channel_0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next SCLK after channel_0 LSB.

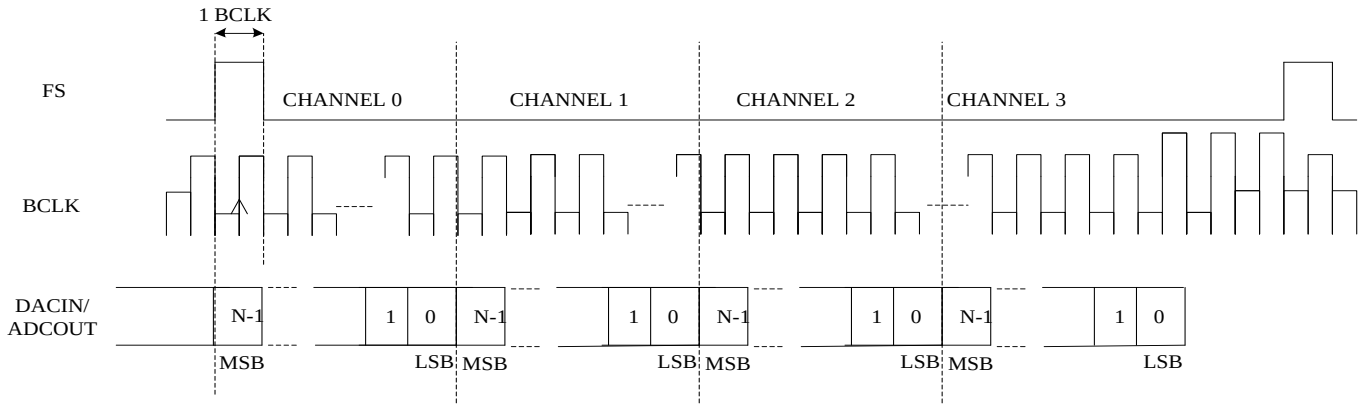



**Figure 33: TDM PCMB Audio Format**

## 9.1.10 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which DAC data is clocked. This increases the flexibility of the NAU88L21C to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU88L21C or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

Normally, the DAC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. The channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in .This can be seen in the figure below.

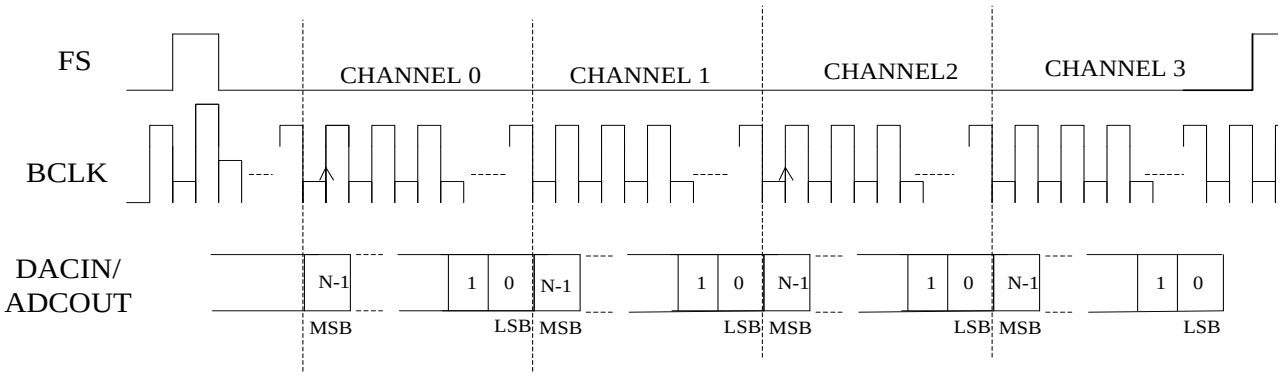



**Figure 34: TDM PCM Offset Audio Format**

## 9.2 Digital Audio Interface Timing Diagrams

### 9.2.1 Digital Audio Interface Slave Mode

Figure 20 provides the timing for Audio Interface Slave Mode.

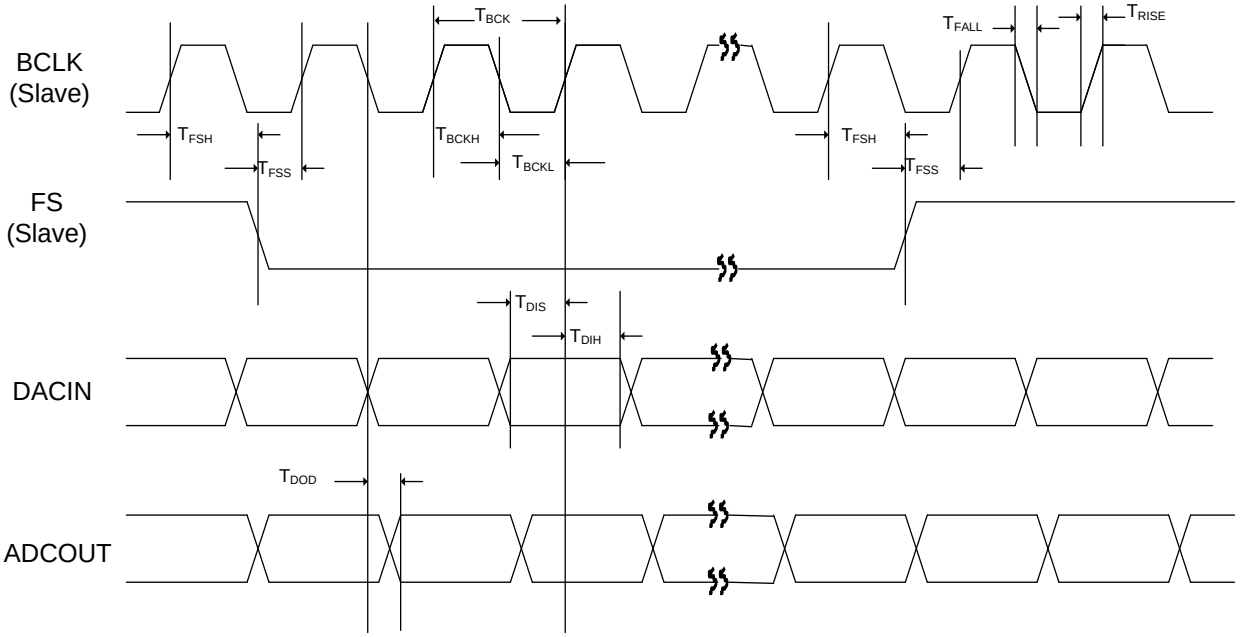



**Figure 35 Audio Interface Slave Mode Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{BCK}$ | BCLK Cycle Time in Slave Mode | 50 | - | - | ns |
| $T_{BCKH}$ | BCLK High Pulse Width in Slave Mode | 20 | - | - | ns |
| $T_{BCKL}$ | BCLK Low Pulse Width in Slave Mode | 20 | - | - | ns |
| $T_{FSS}$ | FS to BCLK Rising Edge Setup Time in Slave Mode | 20 | - | - | ns |
| $T_{FSH}$ | BCLK Rising Edge to FS Hold Time in Slave Mode | 20 | - | - | ns |
| $T_{RISE}$ | Rise Time for All Audio Interface Signals | - | - | $0.135T_{BCK}$ | ns |
| $T_{FALL}$ | Fall Time for All Audio Interface Signals | - | - | $0.135T_{BCK}$ | ns |
| $T_{DIS}$ | DACIN to BCLK Rising Edge Setup Time | 15 | - | - | ns |
| $T_{DIH}$ | BCLK Rising Edge to DACIN Hold Time | 15 | - | - | ns |
| $T_{DOD}$ | BCLK Falling Edge to ADCOUT Delay Time | - | - | 30 | ns |

**Table 16 Audio Interface Slave Mode Timing Parameters**

### 9.2.2 Digital Audio Interface Master Mode

provides the timinig for Audio Interface Master Mode

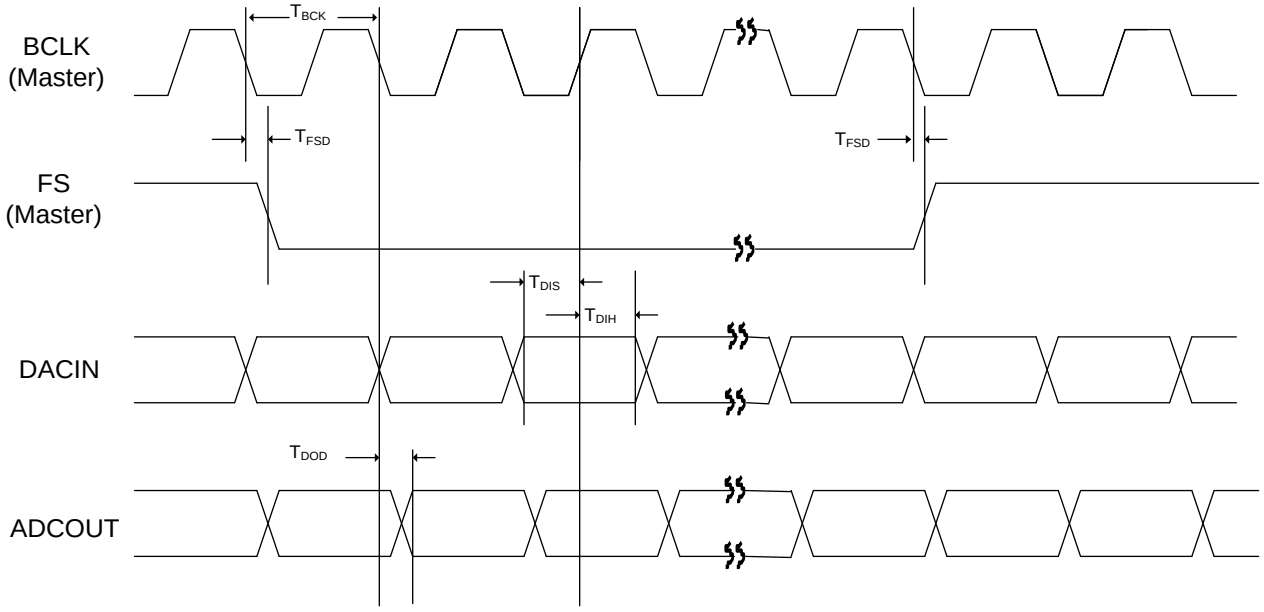



**Figure 36 Audio Interface Master Mode Timing**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $T_{BCK}$ | BCLK Cycle Time in Master Mode | 50 | 60 | - | ns |
| $T_{FSD}$ | BCLK Falling Edge to FS Delay Time in Master Mode | - | - | 10 | ns |
| $T_{DIS}$ | DACIN to BCLK Rising Edge Setup Time | 15 | - | - | ns |
| $T_{DIH}$ | BCLK Rising Edge to DACIN Hold Time | 15 | - | - | ns |
| $T_{DOD}$ | BCLK Falling Edge to ADCOUT Delay Time | - | - | 20 | ns |

**Table 17 Audio Interface Master Mode Timing Parameters**

### 9.2.3 PCM Audio Interface Slave Mode

I2S or PCM Audio Data can be processed using either Slave Mode or Master Mode. The timing diagram for PCM Audio Data in Slave Mode is shown in below.

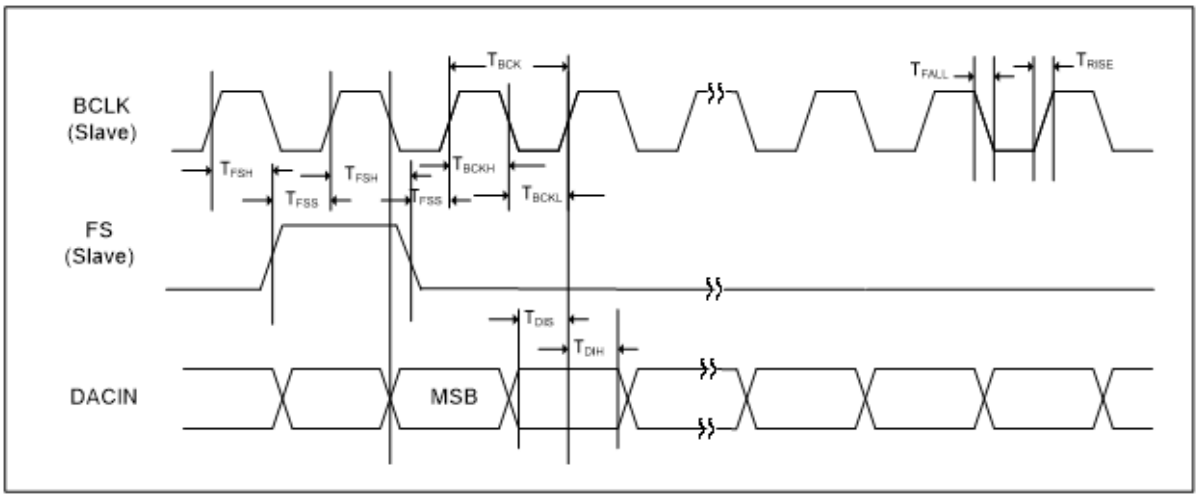



**Figure 37 PCM Audio Interface Slave Mode**

### 9.2.4 PCM Audio Interface Master Mode

I2S or PCM Audio Data can be processed using either Master or Slave Mode. The timing diagram for PCM Audio Data in Master Mode is shown in Figure 37.

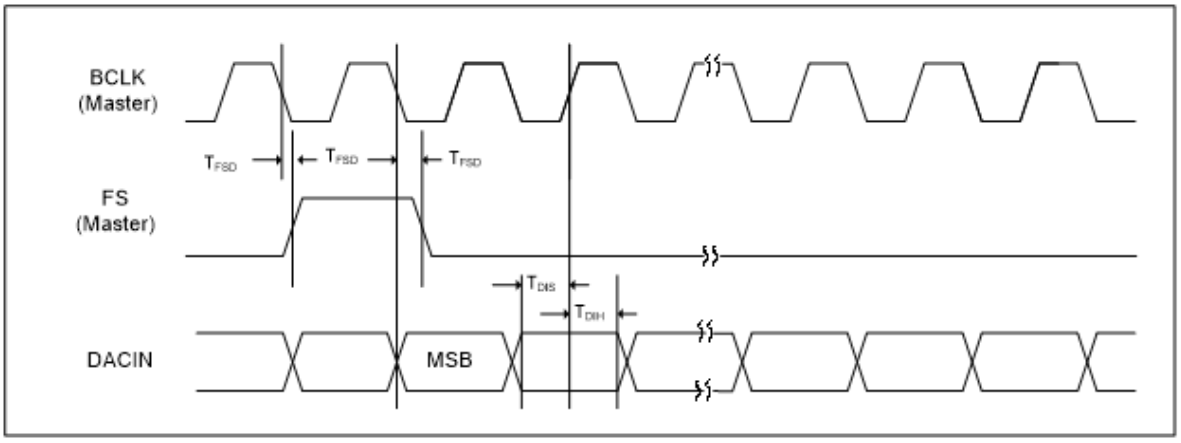



**Figure 38 PCM Audio Interface Master Mode Timing**

### 9.2.5 PCM Time Slot Audio Interface Slave Mode

PCM Time Slot Data can be processed using either Slave Mode or Master Mode. The timing diagram for PCM Time Slot Audio Data in Slave Mode is shown in Figure 38.

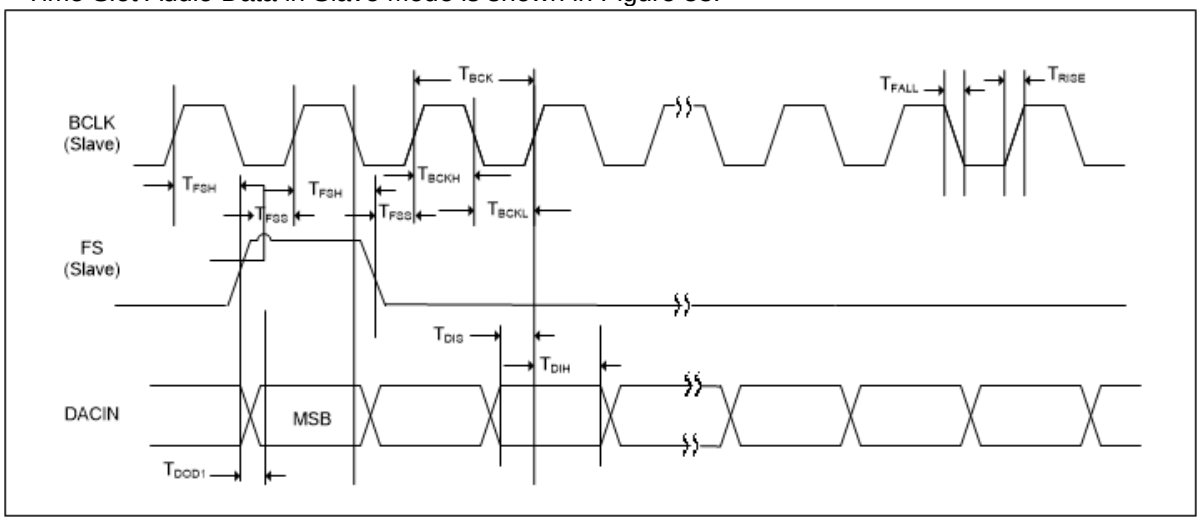



**Figure 39 PCM Time Slot Audio Interface Slave Mode Timing**

### 9.2.6 PCM Time Slot Audio Interface Master Mode

The timing diagram for PCM Time Slot Audio Data in Master Mode is shown in below.

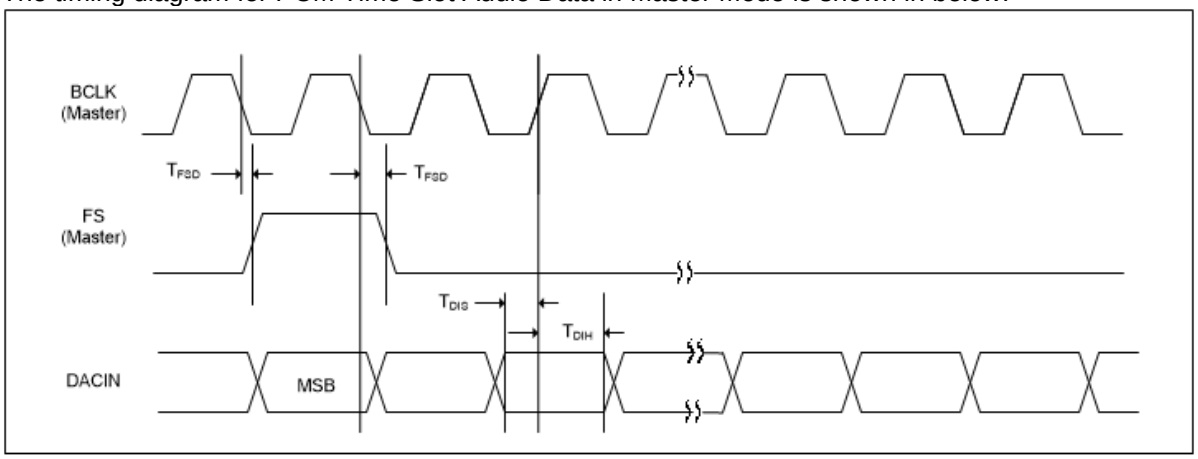



**Figure 40 PCM Time Slot Audio Interface Master Mode Timing**

# 10. Outputs

The NAU88L21C provides a pair of Class G ground-reference headphone outputs.

## 10.1 Class G Headphone Driver and Charge Pump

The NAU88L21C uses Class G speaker drivers powered by a charge pump for the headphones. For typical operation with large and small signals the charge pump provides ±1.8V and ±0.9V, respectively. These output drivers are driven by dedicated left and right DACs and can provide 30mW of power to a 32Ω load (in CSP package).

Three capacitors are needed to generate the negative voltage from the positive 1.8V. Typically, 2μF ceramic capacitors are used.

- The Fly Back capacitor is connected between pins CPCA and CPCB.
- The Positive Output Decoupling capacitor is applied from pin CPVOUTP to ground (VSSCP).
- The Negative Output Decoupling capacitor is applied from pin CPOUTN to ground (VSSCP).

The Class G will be turned on only if DAC signal level is bigger than the threshold in the register settings, and the peak output can be also configured differently by register settings.

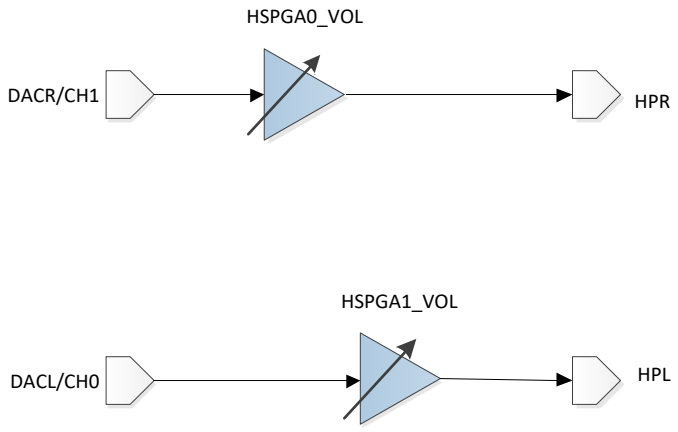



**Figure 41: DAC to Headphone out path diagram**

# 11. Control and Status Registers

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | HARDWARE_RST | HARDWARE_RESET | | | | | | | | | | | | | | | | | **Hardware Reset**<br>(Write any value ***once*** to reset all the registers.) |
| 1 | ENA_CTRL | CMLCK_ENB | | | | | | | | | | | | | | | | | **PGA Common Mode Lock Enable Control**<br>0 = Enable (DEFAULT)<br>1 = Disable |
| | | CLK_DAC_INV | | | | | | | | | | | | | | | | | **DAC Clock Inversion In Analog Domain Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | RDACEN | | | | | | | | | | | | | | | | | **Right Channel DAC Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | LDACEN | | | | | | | | | | | | | | | | | **Left Channel DAC Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | RADCEN | | | | | | | | | | | | | | | | | **Right Channel ADC Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | LADCEN | | | | | | | | | | | | | | | | | **Left Channel ADC Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DCLK_ADC_EN | | | | | | | | | | | | | | | | | **ADC Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | DCLK_DAC_EN | | | | | | | | | | | | | | | | | **DAC Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CLK_IMM_EN | | | | | | | | | | | | | | | | | **IMM Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CLK_I2S_EN | | | | | | | | | | | | | | | | | **I2S Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CLK_BIST_EN | | | | | | | | | | | | | | | | | **BIST Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CLK_OTP_EN | | | | | | | | | | | | | | | | | **OTP (One Time Programming) Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CLK_DRC_EN | | | | | | | | | | | | | | | | | **DRC Clock Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **0x00FF** |
| 3 | CLK_DIVIDER | SYSCLK_SRC | | | | | | | | | | | | | | | | | **Master Clock Source Select**<br>0 = MCLK_PIN (DEFAULT)<br>1 = ½ DCO_CLK |
| | | CLK_CODEC_SRC | | | | | | | | | | | | | | | | | **ADC & DAC Clock Source Select**<br>0 = From internal MCLK (DEFAULT)<br>1 = From MCLK_PIN or ½ DCO_CLK |
| | | CLK_DAC_PL | | | | | | | | | | | | | | | | | **DAC Clock Polarity**<br>0 = Non-inverted<br>1 = Inverted |
| | | CLK_ADC_PL | | | | | | | | | | | | | | | | | **ADC Clock Polarity**<br>0 = Non-inverted<br>1 = Inverted (Recommended) |
| | | CLK_GPIO_SRC | | | | | | | | | | | | | | | | | **Scaling Divider For GPIO Clock From MCLK**<br>00 = 1/8 (DEFAULT)<br>01 = 1 (MCLK)<br>10 = 1/2<br>11 = 1/4 |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLK_ADC_SRC | | | | | | | | | | | | | | | | | **Scaling Divider For ADC Clock From CODEC_SRC**<br>00 = 1<br>01 = 1/2 (DEFAULT)<br>10 = 1/4<br>11 = 1/8 |
| | | CLK_DAC_SRC | | | | | | | | | | | | | | | | | **Scaling Divider For DAC Clock From CODEC_SRC**<br>00 = 1<br>01 = 1/2 (DEFAULT)<br>10 = 1/4<br>11 = 1/8 |
| | | MCLK_SRC | | | | | | | | | | | | | | | | | **Scaling Divider For MCLK From SYSCLK_SRC**<br>0000 = 1 (DEFAULT) 0001 = Inverted<br>0010 = 1/2 0011 = 1/4<br>0100 = 1/8 0101 = 1/16<br>0110 = 1/32 0111 = 1/3<br>1000 = 1 1001 = Inverted<br>1010 = 1/6 1011 = 1/12<br>1100 = 1/24 1101 = 1/48<br>1110 = 1/96 1111 = 1/5 |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **0** | **0** | **0x0050** |
| 4 | FLL1 | FLLISELDAC | | | | | | | | | | | | | | | | | **Increase Drive Strength Of FLL DAC**<br>000 = (DEFAULT) |
| | | ICTRL_LATCH | | | | | | | | | | | | | | | | | **FLL Latch Drive Strength Multiplier**<br>(When FLL running at high frequency with long decimal number, DSP needs to operate at high speed. By adjusting ICTRL_LATCH, FLL DSP can optimize between performance and power consumption (111 has highest power consumption for FLL DSP.)<br>On the other hand, (DCO frequency)/(FLL input reference frequency)=integer, default setting can be used to reduce power. This register is using thermometer coding. )<br>000 = (DEFAULT) 001 = 1x<br>011 = 2x 111 = 3x |
| | | ICTRL_V2I | | | | | | | | | | | | | | | | | **Amp Half Bias-Current Select**<br>(Amp bias current must be reduced to 50% of its nominal value.)<br>00 = No power reduction (DEFAULT)<br>01 = Half bias current on FLL_BIAS_AMP2X<br>10 = Half bias current on FLL_BIAS_AMP<br>11 = Half current on both amps |
| | | FLL_LOCK_BP | | | | | | | | | | | | | | | | | **Manual Force of FLL Lock Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | FLL_RATIO | | | | | | | | | | | | | | | | | **Input Clock Frequency Select**<br>0000001 = For input clock frequency ≥ 512KHz<br>0000010 = For input clock frequency ≥ 256KHz<br>0000100 = For input clock frequency ≥ 128KHz<br>0001000 = For input clock frequency ≥ 64KHz<br>0010000 = For input clock frequency ≥ 32KHz<br>0100000 = For input clock frequency ≥ 8KHz<br>1000000 = For input clock frequency ≥ 4KHz |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 5 | FLL2 | DOUT2DCO_RSV | | | | | | | | | | | | | | | | | **FLL DCO Frequency Free-running Mode** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0x00BC** |
| 6 | FLL3 | GAIN_ERR | | | | | | | | | | | | | | | | | **FLL Gain Error**<br>(The threshold is comparison between DCO and target frequency. 1111 has the most accurate DCO to target frequency. However, the gain error setting conditionally and inversely depends on FLL input reference clock rate. Higher FLL reference input frequency can only set lower gain error, such as 0000 for input reference from MCLK=12.288MHz. On the other side, if FLL reference input is from Frame sync, 48KHz, higher error gain can apply such as 1111.)<br>0000 = (DEFAULT) 0001 = x1<br>0010 = x2 0011 = x3<br>0100 = x4 0101 = x5<br>0110 = x6 0111 = x8 |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | 1000 = x9 1001 = x10<br>1010 = x12 1011 = x16<br>1100 = x17 1101 = x18<br>1110 = x20 1111 = x24 |
| | | FLL_CLK_REF_SRC | | | | | | | | | | | | | | | | | **FLL Reference CLK Source Select**<br>00 & 01 = MCLK pin (DEFAULT)<br>10 = BCLK pin<br>11= LRC pin |
| | | FLL_INTEGER | | | | | | | | | | | | | | | | | **FLL 10-bit Integer Input** |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | **0x0008** |
| 7 | FLL4 | HIGHBWE | | | | | | | | | | | | | | | | | **High Bandwidth Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | FLL_CLK_REF_DIV_4CHK | | | | | | | | | | | | | | | | | **FLL CLK_REF Divider For Accurate Lock Detection**<br>000 = 1 (DEFAULT) 001 = 1/2<br>010 = 1/4 011 = 1/8<br>100 = 1/16 101 = 1/32 |
| | | FLL_CLK_REF_DIV | | | | | | | | | | | | | | | | | **FLL Pre-Scale Divider**<br>00 = 1 (DEFAULT) 01 = 1/2<br>10 = 1/4 11 = 1/8 |
| | | FLL_N2 | | | | | | | | | | | | | | | | | **FLL 10-bit Integer DCO Divider For FLL Filter Clock**<br>(The value is in orders of 2. When 0x8[13]=1, it selects DCO clock as FLL filter clock. The filter clock rate needs to be less than 1Mhz. With setting proper value, filter clock can be divided down from DCO clock. For example, DCO runs at 96Mhz, by setting value 0x60=96, filter clock becomes 1MHz.) |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | **0x0010** |
| 8 | FLL5 | PDB_DACICTRL | | | | | | | | | | | | | | | | | **FLL Loop Filter To Reduce FLL Output Noise Enable Control**<br>(Especially, (DCO frequency)/(FLL input reference frequency) is not an integer.)<br>0 = Disable (DEFAULT)<br>1 = Enable (By REG0x09[13:12]) |
| | | CHB_FILTER_EN | | | | | | | | | | | | | | | | | **Select Filter Clock Source Select**<br>0 = Select REFCLK<br>1 = Select divided DCO clock based on register FLL_N2 (DEFAULT) |
| | | CLK_FILTER_SW | | | | | | | | | | | | | | | | | **IDAC Input Select**<br>0 = Select filter output (DEFAULT)<br>1 = Select accumulator output when feedback divider is integer, it can use for saving power but more jitter |
| | | FILTER_SW | | | | | | | | | | | | | | | | | **FLL Loop Filter Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | FLL_LOCK_LENGTH | | | | | | | | | | | | | | | | | **Set FLL Lock-In Length**<br>(Set the time that FLL must stay within the lock-in range before lock signal goes high.)<br>When 8'h00, the lock lengh is disabled<br>When value larger or equal to 1, it's enabled |
| | | DEFAULT | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x4000** |
| 9 | FLL6 | DCO_EN | | | | | | | | | | | | | | | | | **FLL Free-running Mode Enable Control**<br>(Need to enable 0x76[12] **BIASEN**)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | SDM_EN | | | | | | | | | | | | | | | | | **FLL Sigma-Delta Modulator Enable Control**<br>(To create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer. If the ratio is integer, it still can be on for lower noise output but higher power consumption.)<br>0 = Disable<br>1 = Enable (DEFAULT) |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CUTOFF500 | | | | | | | | | | | | | | | | | **FLL 500KHz Cut-off Frequency Enable Control**<br>(If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give the best FLL performance with the highest power consumption.)<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | CUTOFF600 | | | | | | | | | | | | | | | | | **FLL 600KHz Cut-off Frequency Enable Control**<br>(If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give a moderate FLL performance with moderate power consumption.)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | VREFSEL | | | | | | | | | | | | | | | | | **VREF Select**<br>00 = 1.8V External VDDA supply<br>01 = 1.56V<br>10 = 1.65V (DEFAULT)<br>11 = 1.75V |
| | | CHKFS256_EN | | | | | | | | | | | | | | | | | **Samples/frame Sync Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable the function to check for 256 |
| | | FS8X_SEL | | | | | | | | | | | | | | | | | **Frame Sync Select**<br>0 = Total samples per 4 frame sync<br>1 = Total samples per 8 frame sync (DEFAULT) |
| | | FLL_FLTR_DITHER_SEL | | | | | | | | | | | | | | | | | **Filter Output Random Bit Select**<br>00 = No dither (DEFAULT)<br>01 = The LSB is a random bit<br>10 = Two LSBs are random bits<br>11 = Three LSBs are random bits |
| | | FLL_SD_DITHER_SEL | | | | | | | | | | | | | | | | | **Input Of SD Modulator Random Bit Select**<br>00 = No dither (DEFAULT)<br>01 = The LSB is a random bit<br>10 = Two LSBs are random bits<br>11 = Three LSBs are random bits |
| | | DLR | | | | | | | | | | | | | | | | | **FLL Dynamic Lock Range**<br>0000 = (DEFAULT) |
| | | **DEFAULT** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x6900** |
| **A** | **FLL7** | FLL_FRAC_H | | | | | | | | | | | | | | | | | **MSB Portion Of FLL 24-bit Fractional Input FLL_FRAC[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0** | **0** | **1** | **0x0031** |
| **B** | **FLL8** | FLL_FRAC_L | | | | | | | | | | | | | | | | | **LSB Portion Of FLL 24-bit Fractional Input FLL_FRAC[15:0]** |
| | | **DEFAULT** | **0** | **0** | **1** | **0** | **0** | **1** | **1** | **0** | **1** | **1** | **1** | **0** | **1** | **0** | **0** | **1** | **0x26E9** |
| **D** | **JACK_DET_CTRL** | MANU_SPKR_DWN1R | | | | | | | | | | | | | | | | | **Manual Access SPKR_DWN1R**<br>0 = Pull down (DEFAULT) |
| | | MANU_SPKR_DWN1L | | | | | | | | | | | | | | | | | **Manual Access SPKR_DWN1L**<br>0 = Pull down (DEFAULT) |
| | | JK_2_PL | | | | | | | | | | | | | | | | | **Jack Detection Source 2 Configuration**<br>00 = From JKDET<br>01 = From inverted JKDET<br>10 = Ignore the input and set to 0<br>11 = Ignore the input and set to 1 |
| | | JK_1_PL | | | | | | | | | | | | | | | | | **Jack Detection Source 1 Configuration**<br>00 = From GPIO2JD1 (DEFAULT)<br>01 = From inverted GPIO2JD1<br>10 = Ignore the input and set to 0<br>11 = Ignore the input and set to 1 |
| | | JD_RESTART | | | | | | | | | | | | | | | | | **Manual Restart Jack Detection**<br>(Toggle this bit to 1 and then to 0 to restart the jack detection.) |
| | | DB_BP_MODE | | | | | | | | | | | | | | | | | **Jack Detect De-bounce Bypass**<br>0 = Enable de-bounce circuit (need to set REG4B[0] = 1 to enable the CLK) (DEFAULT)<br>1 = Bypass the de-bounce circuit |
| | | INSERT_DT | | | | | | | | | | | | | | | | | **Insertion De-bounce Time**<br>2^( INSERT_DT +2)-1 ms |
| | | EJECT_DT | | | | | | | | | | | | | | | | | **Ejection De-bounce Time**<br>2^( EJECT_DT +2)-1 ms |

| REG | Function | Name | Bit | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | JKDET_PL | | | | | | | | | | | | | | | | | **Jack Insertion/ Detection Logic Polarity**<br>0 = Falling edge (DEFAULT)<br>1 = Rising edge |
| | | JKDET_LOGIC | | | | | | | | | | | | | | | | | **Jack Detection Logic Control**<br>0 = OR gate (DEFAULT)<br>1 = AND gate |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| E | MIDCET_DET_CTRL | MICDET_DBCLR | | | | | | | | | | | | | | | | | MIC detection debouce mode Clear bit, toggle this bit "1" then clear MIC debouce detection to restart |
| | | MICDET_MODE | | | | | | | | | | | | | | | | | MIC detection mode<br>1 ---- debounce mode<br>0 --- bypass debounce mode |
| | | MICDET_PL | | | | | | | | | | | | | | | | | MIC Detection Logic polarity<br>1 --- invert mic detect bit<br>0 --- do not invert mic detect bit |
| | | MICDET_DT | | | | | | | | | | | | | | | | | MIC detection de-bounce time<br>0000--- 4ms<br>0001--- 8ms<br>-----<br>1110--- 60ms<br>1111--- 64ms<br>(MICDET_DT+1) *4 ms |
| | | **Default** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| F | INTERRUPT_MASK | **IRQ_PL** | | | | | | | | | | | | | | | | | **IRQ Pin Logic Select**<br>0 = Active low (DEFAULT)<br>1 = Active high |
| | | **IRQ_PS** | | | | | | | | | | | | | | | | | **IRQ Pin Pull Select**<br>0 = Pull down (DEFAULT)<br>1 = Pull up |
| | | **IRQ_PE** | | | | | | | | | | | | | | | | | **IRQ Pin Pull Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | **IRQ_DS** | | | | | | | | | | | | | | | | | **IRQ Pin Drive Current Select**<br>0 = Low drive current (DEFAULT)<br>1 = High drive current |
| | | **IRQ_OE** | | | | | | | | | | | | | | | | | **IRQ Pin Output Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | **APR_EMRGENCY_SHTDWN1_INTP_MASK** | | | | | | | | | | | | | | | | | **APR Emergency Shutdown Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[9] (DEFAULT)<br>1 = Mask interrupt; turn on IRQ pad |
| | | **RMS_INTP_MASK** | | | | | | | | | | | | | | | | | **RMS Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[8] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **KEY_RELEASE_INTP_MASK** | | | | | | | | | | | | | | | | | **Key Release Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[7] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **KEY_INTP_MASK** | | | | | | | | | | | | | | | | | **Key Pressed Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[6] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **MCLKDET_INTP_MASK** | | | | | | | | | | | | | | | | | **Missing MCLK Detection Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[5] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **MIC_DET_INTP_MASK** | | | | | | | | | | | | | | | | | **MIC Detection Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[4] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **JK_EJECT_INTP_MASK** | | | | | | | | | | | | | | | | | **Jack Ejection Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[2] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |
| | | **JK_DET_INTP_MASK** | | | | | | | | | | | | | | | | | **Jack Insertion Interrupt Mask**<br>0 = Unmask interrupt; turn off IRQ pad, but interrupt register status is controlled by 0x12[0] (DEFAULT)<br>1 = Mask the interrupt; turn on IRQ pad |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 10 | IRQ_STATUS | APR_EMRG_SHTDWN | | | | | | | | | | | | | | | | | APR Emergency Short Circuit Shutdown IRQ Status |
| | | RMS_INT | | | | | | | | | | | | | | | | | Impedance Measurement IRQ Status |
| | | KEY_RELEASE_INT | | | | | | | | | | | | | | | | | Key Release For Key Detection IRQ Status |
| | | KEY_INT | | | | | | | | | | | | | | | | | Key Detection IRQ Status |
| | | MCLK_DET_INT | | | | | | | | | | | | | | | | | Missing MCLK Detection IRQ Status |
| | | MIC_DET_INT | | | | | | | | | | | | | | | | | MIC Detection IRQ Status |
| | | JACK_EJCT_IRQ | | | | | | | | | | | | | | | | | Jack Ejection IRQ Status<br>00 = Cleared state<br>01 = Jack ejection detected<br>10 = A jack eject interrupt was cleared due to a jack insertion<br>11 = Undefined |
| | | JACK_DET_IRQ | | | | | | | | | | | | | | | | | Jack insertion IRQ status<br>00 = Cleared state<br>01 = Jack insertion detected<br>10 = A jack insert interrupt was cleared due to a jack ejection<br>11 = Undefined |
| | | DEFAULT | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | READ ONLY |
| 11 | INT_CLR_KEY_STATUS | INT_CLR_KEY_STATUS | | | | | | | | | | | | | | | | | Write Operation<br>(Write bits[15:0] clear corresponding REG10 [15:0]<br>Write 1s to bits that you want to reset to 0, except)<br>Bit0 or Bit1 = clear Jack insertion interrupt<br>Bit2 or Bit3 = clear Jack ejection interrupt |
| | | DEFAULT | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | READ/WRITE |
| 12 | INTERRUPT_DIS_CTRL (WRITE MODE) | APR_EMRG_SHTDWN_INT_DIS | | | | | | | | | | | | | | | | | APR Emergency Short Circuit Shutdown Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | RMS_INT_DIS | | | | | | | | | | | | | | | | | RMS Impedance Measurement Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | KEY_RELEASE_INT_DIS | | | | | | | | | | | | | | | | | Key Release Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | KEY_INT_DIS | | | | | | | | | | | | | | | | | Key Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | MCLKDET_INT_DIS | | | | | | | | | | | | | | | | | MCLK Detection Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | MIC_DET_INT_DIS | | | | | | | | | | | | | | | | | MIC Detection/Headset Configuration Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | JACK_EJCT_INT_DIS | | | | | | | | | | | | | | | | | Jack Ejection Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | JACK_DET_INT_DIS | | | | | | | | | | | | | | | | | Jack Insertion/Detection Interrupt Disable Control<br>0 = Enable interrupt; interrupt status read from register or IRQ pad<br>1 = Disable interrupt and IRQ pad (DEFAULT) |
| | | DEFAULT | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0xFFFF |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 13 | DMIC_CTRL | I2C OSC deglitch ON | ■ | | | | | | | | | | | | | | | | **I2C oscillator dglitch on**<br>1 --- on,<br>0 --- off |
| | | I2C OSC PULL | | ■ | | | | | | | | | | | | | | | **I2C oscillator dglitch power up**<br>1 – power up<br>0 – power down |
| | | I2C OSC clock divider | | | ■ | ■ | | | | | | | | | | | | | **I2C oscillator clock divider**<br>00/01 – 1<br>10 -- 1/2<br>11 – 1/4 |
| | | DMIC_DS | | | | | ■ | | | | | | | | | | | | **DMIC Clock Drive Current Select**<br>(For high ***Cload*** > 20pF, enable high drive current.)<br>0 = Low drive current (DEFAULT)<br>1 = High drive current |
| | | DMIC_SLEW | | | | | | ■ | ■ | ■ | | | | | | | | | **DMIC Clock Slew Rate Select**<br>(For high ***Cload*** > 20pF, use faster slew rate.)<br>000 = Slowest slew rate (DEFAULT)<br>▼<br>111 = Fastest slew rate |
| | | CLK_DMIC_SRC | | | | | | | | | | | | | | ■ | ■ | | **DMIC Clock Speed Select**<br>00 = ADC clock (DEFAULT)<br>01 = ADC clock / 2<br>10 = ADC clock / 4<br>11 = ADC clock / 8 |
| | | DMICEN | | | | | | | | | | | | | | | | ■ | **Digital Microphone Mode Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 1A | GPIO12_CTRL | GPIO2OUT | | | | ■ | | | | | | | | | | | | | **GPIO2 Programmable Output** |
| | | GPIO2_PS | | | | | ■ | | | | | | | | | | | | **GPIO2JD1 Pull Select**<br>0 = Pull down (DEFAULT)<br>1 = Pull up |
| | | GPIO2_DS | | | | | | ■ | | | | | | | | | | | **GPIO2JD1 Drive Current Select**<br>0 = Low drive current (DEFAULT)<br>1 = High drive current |
| | | GPIO2_PE | | | | | | | ■ | | | | | | | | | | **GPIO2JD1 Pin Pull Enable Control**<br>0 = Enable (DEFAULT)<br>1 = Disable |
| | | GPIO2_OE | | | | | | | | ■ | | | | | | | | | **GPIO2JD1 Output Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | GPIO1POL | | | | | | | | | ■ | | | | | | | | **GPIO1 Polarity**<br>0 = Non-inverted (DEFAULT)<br>1 = Inverted logic of the CSB/GPIO1 function output selected by GPIO1SEL |
| | | GPIO1SEL | | | | | | | | | | ■ | ■ | ■ | | | | | **CSB/GPIO1 Function Select (output default)**<br>000 = output 0 (DEFAULT)<br>001 = Jack status from the AND/OR logic<br>010 = SCLK_I<br>011 = SD_I<br>100 = output divided FLL clock<br>101 = FLL locked condition (logic 1 = PLL locked)<br>110 = SD_O<br>111 = OSC_CLK |
| | | GPIO1_PS | | | | | | | | | | | | | ■ | | | | **GPIO1CSB Pull Select**<br>(If GPIO1_PE=1)<br>1 = Pull up<br>0 = Pull down (DEFAULT) |
| | | GPIO1_DS | | | | | | | | | | | | | | ■ | | | **GPIO1CSB Drive Current Select**<br>0 = Low drive current (DEFAULT)<br>1 = High drive current |
| | | GPIO1_PE | | | | | | | | | | | | | | | ■ | | **GPIO1CSB Pin Pull Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | GPIO1_OE | | | | | | | | | | | | | | | | ■ | **GPIO1CSB Output Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 1B | TDM_CTRL | TDM | | | | | | | | | | | | | | | | | **TDM Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | PCM_OFFSET_MODE_CTRL | | | | | | | | | | | | | | | | | **PCM Offset In TDM Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | ADCPHS0 | | | | | | | | | | | | | | | | | **ADC Audio Data Left-right Ordering Select**<br>0 = Left ADC data in left phase of LRP (DEFAULT)<br>1 = Left ADC data in right phase of LRP (left-right reversed) |
| | | DACPHS1 | | | | | | | | | | | | | | | | | **DAC Right Channel Audio Data Left-right Ordering Select**<br>0 = Right DAC data in right phase of LRP (DEFAULT)<br>1 = Right DAC data in left phase of LRP (left-right reversed) |
| | | DACPHS0 | | | | | | | | | | | | | | | | | **DAC Left Channel Audio Data Left-right Ordering Select**<br>0 = Left DAC data in left phase of LRP (DEFAULT)<br>1 = Left DAC data in right phase of LRP (left-right reversed) |
| | | DAC_LEFT_SEL | | | | | | | | | | | | | | | | | **DAC Left Channel Source Under TDM Mode (TDM = 1 & PCM_OFFSET_MODE_CTRL = 0)**<br>I2S :<br>000 = From Slot 0 (DEFAULT) 001= From Slot 1<br>010 = From Slot 2 011 = From Slot 3<br>100 = RESERVED 101 = RESERVED<br>110 = RESERVED 111 = RESERVED<br><br>PCM:<br>000 = From slot 0 (DEFAULT) 001 = From slot 1<br>010 = From slot 2 011 = From slot 3<br>100 = From slot 4 101 = From slot 5<br>110 = From slot 6 111 = From slot 7 |
| | | DAC_RIGHT_SEL | | | | | | | | | | | | | | | | | **DAC Right Channel Source Under TDM Mode**<br>I2S:<br>000 = From Slot 0 (DEFAULT) 001 = From Slot 1<br>010 = From Slot 2 011 = From Slot 3<br>100 = RESERVED 101 = RESERVED<br>110 = RESERVED 111 = RESERVED<br><br>PCM:<br>000 = From slot 0 (DEFAULT) 001 = From slot 1<br>010 = From slot 2 011 = From slot 3<br>100 = From slot 4 101 = From slot 5<br>110 = From slot 6 111 = From slot 7 |
| | | ADC_TX_SEL_L | | | | | | | | | | | | | | | | | **ADC Left Channel Source Under TDM/I2S Mode**<br>00 = From slot 0 (DEFAULT)<br>01 = From slot 2<br>10 = From slot 4<br>11 = From slot 6 |
| | | ADC_TX_SEL_R | | | | | | | | | | | | | | | | | **ADC Right Channel Source Under TDM/I2S Mode**<br>00 = From slot 1 (DEFAULT)<br>01 = From slot 3<br>10 = From slot 5<br>11 = From slot 7 |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 1C | I2S_PCM_CTRL1 | DACCM0 | | | | | | | | | | | | | | | | | **DAC Companding Mode Select**<br>00 = Off (DEFAULT - Normal linear operation)<br>01 = RESERVED<br>10 = μ-law companding<br>11 = A-law companding |
| | | ADCCM0 | | | | | | | | | | | | | | | | | **ADC Companding Mode Select**<br>00 = Off (DEFAULT - Normal linear operation)<br>01 = RESERVED<br>10 = μ-law companding<br>11 = A-law companding |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ADDAP0 | | | | | | | | | | | | | | | | | **ADC Output Data Stream Directly Routed To DAC Input Data Path Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | CMB8_0 | | | | | | | | | | | | | | | | | **8-bit Word For Companding Mode Of Operation Enable Control**<br>0 = Normal operation (DEFAULT - No companding)<br>1 = 8-bit operation for companding mode |
| | | UA_OFFSET | | | | | | | | | | | | | | | | | **uLaw Offset Select**<br>0 = 1's complement (DEFAULT)<br>1 = 2's complement |
| | | MCLKSPEED_DETDIS | | | | | | | | | | | | | | | | | **MCLK SPEED DETECTION DISABLE**<br>1 = auto detection disable<br>0 = auto deteciotn enable |
| | | BCP0 | | | | | | | | | | | | | | | | | **Bit Clock Phase Inversion Option For BCLK**<br>0 = Non-inverted (DEFAULT)<br>1 = Inverted |
| | | LRP0 | | | | | | | | | | | | | | | | | **PCMA & PCMB Left-right Word Ordering Select**<br>0 = Right Justified/Left Justified/I2S/PCMA mode (DEFAULT)<br>1 = PCMB Mode Enable - MSB is valid on 1st rising edge of BCLK after rising edge of FS |
| | | MCLKSPEED_SET | | | | | | | | | | | | | | | | | MCLK SPEED setting<br>00 = 256Fs, 01=384Fs, 10=400Fs,11=500Fs |
| | | WLEN0 | | | | | | | | | | | | | | | | | **Word Length of Audio Data Stream Select**<br>00 = 16-bit word length<br>01 = 20-bit word length<br>10 = 24-bit word length (DEFAULT)<br>11 = 32-bit word length |
| | | AIFMT0 | | | | | | | | | | | | | | | | | **Audio Interface Data Format Select**<br>00 = Right justified<br>01 = Left justified<br>10 = Standard I2S format (DEFAULT)<br>11 = PCMA or PCMB audio data format option |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0x000A** |
| **1D** | **I2S_PCM_CTRL2** | **I2S_TRI** | | | | | | | | | | | | | | | | | **I2S Tri State Enable Control**<br>0 = Normal mode<br>1 = Output high Z (DEFAULT) |
| | | **I2S_DRV** | | | | | | | | | | | | | | | | | **I2S Drive Enable Control**<br>0 = Normal mode (DEFAULT)<br>1 = Always out |
| | | **LRC_DIV** | | | | | | | | | | | | | | | | | **LRC(FS) Divider From BCLK Frequency**<br>000= 1/256 (DEFAULT)<br>010 = 1/64<br>100=1/16<br>001 = 1/128<br>011 = 1/32<br>101=1/50 |
| | | **PCM_TS_EN0** | | | | | | | | | | | | | | | | | **PCM Time Slot Function Enable Control**<br>(Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected.)<br>0 = Disable time slot function for PCM mode (DEFAULT)<br>1 = Enable time slot function for PCM mode |
| | | **TRI0** | | | | | | | | | | | | | | | | | **Without TDM Mode**<br>0 = Drive the full clock of LSB (DEFAULT)<br>1 = Tri-state the 2nd half of LSB |
| | | **PCM8BIT0** | | | | | | | | | | | | | | | | | **8-Bit PCM Select**<br>0 = Use I2S_PCM_CTRL.WLEN to select word length (DEFAULT)<br>1 = PCM select 8-bit word length |
| | | **ADCDAT0_PE** | | | | | | | | | | | | | | | | | **ADCDAT IO Pull Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | **ADCDAT0_PS** | | | | | | | | | | | | | | | | | **ADCDAT IO Pull Up/Down Enable Control**<br>0 = Pull down (DEFAULT)<br>1 = Pull up |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ADCDAT0_OE | | | | | | | | | | | | | | | | | **ADCDAT IO Output Enable Control**<br>0 = ADCDAT not always out (when no data out, ADCOUT pin becomes high.)<br>1 = ADCDAT always out (DEFAULT) |
| | | MS0 | | | | | | | | | | | | | | | | | **Master/Slave Mode Enable Control**<br>0 = Slave mode (DEFAULT)<br>1 = Master mode |
| | | BCLK_DIV[2:0] | | | | | | | | | | | | | | | | | **BCLK Divider From MCLK Frequency**<br>000 = 1 (DEFAULT) 001 = 1/2<br>010 = 1/4 011 = 1/8<br>100 = 1/16 101 = 1/32<br>110 = 1/5 111 = 1/10 |
| | | **DEFAULT** | **1** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **0x8010** |
| 1E | LEFT_TIME_SLOT | DIS_FS_SHORT_DET | | | | | | | | | | | | | | | | | **Short Gram Sync Detection Logic Enable Control**<br>0 = Enable (DEFAULT)<br>1 = Disable (When using FLL, it recommend to disable) |
| | | TSLOT_L0 | | | | | | | | | | | | | | | | | **Left channel PCM Time Slot Start Value / PCM TDM Offset Mode Slot Start Value** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 1F | RIGHT_TIME_SLOT | BCLKDIV[4:3] | | | | | | | | | | | | | | | | | **BCLK DIVIDE Setting from MCLK frequency**<br>00 = others for 0x1c[2:0]<br>01 = 1/3 10 = 1/6 |
| | | TSLOT_R0 | | | | | | | | | | | | | | | | | **Right channel PCM Time Slot Start Value / unused for PCM TDM Offset Mode** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 21 | BIQ0_COF1 | BIQ0_A1_L | | | | | | | | | | | | | | | | | **Program ADC BIQ0_A1 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 22 | BIQ0_COF2 | BIQ0_A1_H | | | | | | | | | | | | | | | | | **Program ADC BIQ0_A1 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 23 | BIQ0_COF3 | BIQ0_A2_L | | | | | | | | | | | | | | | | | **Program ADC BIQ0_A2 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 24 | BIQ0_COF4 | BIQ0_A2_H | | | | | | | | | | | | | | | | | **Program ADC BIQ0_A2 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 25 | BIQ0_COF5 | BIQ0_B0_L | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B0 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 26 | BIQ0_COF6 | BIQ0_B0_H | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B0 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 27 | BIQ0_COF7 | BIQ0_B1_L | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B1 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 28 | BIQ0_COF8 | BIQ0_B1_H | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B1 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 29 | BIQ0_COF9 | BIQ0_B2_L | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B2 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 2A | BIQ0_COF10 | BIQ0_EN | | | | | | | | | | | | | | | | | **BIQ0 ADC Path Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BIQ0_B2_H | | | | | | | | | | | | | | | | | **Program ADC BIQ0_B2 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000 R/W** |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2B | ADC_RATE | ADC_L_SRC | | | | | | | | | | | | | | | | | **ADC Left Channel Source Select**<br><br>**In Non-DMIC Mode**<br>0 = Latch left channel analog data input into the left channel filter (DEFAULT)<br>1 = Latch right channel analog data input into the left channel filter<br><br>**In DMIC Mode**<br>0 = Left channel in rising edge (DEFAULT)<br>1 = Left channel in falling edge |
| | | ADC_R_SRC | | | | | | | | | | | | | | | | | **ADC Right Channel Source Select**<br><br>**In Non-DMIC Mode**<br>0 = Latch right channel analog data input into the right channel filter (DEFAULT)<br>1 = Latch left channel analog data input into the right channel filter<br><br>**In DMIC Mode**<br>0 = Right channel in falling edge (DEFAULT)<br>1 = Right channel in rising edge |
| | | ADCFLT_TYPESEL | | | | | | | | | | | | | | | | | **ADC Filter Type Selection**<br>0xx ---- sharp roll-off, long delay(Default)<br>100 ---- sharp roll-off, long delay linear phase<br>101 ---- slow roll-off, short delay linear phase<br>110 ---- sharp roll-off, short delay non-linear phase<br>111 ---- slow roll-off, short delay non-linear phase |
| | | ADCFLT_TYPE_ZCSW | | | | | | | | | | | | | | | | | **Zero-corssing enable for ADC Filter Types Switching (between ADCFLT_TYPESEL 3'b1xx)**<br>1 ---- zero crossing enable,<br>While ADCFLT_TYPESEL is update, internal function siwching checks input signal zero crossing point<br>0 ---- zero crossing disable<br>while ADCFLT_TYPESEL is update, internal function updates immediately |
| | | ADC_POPPROTECT_EN | | | | | | | | | | | | | | | | | **ADC POP-SOUND protection enable**<br>1 ---- function enable. While filter type selection changes or MCLKDET down(check MCLKDET_CTRL_EN(0x2C[14] if it is on), digital filter auto-mute to zero with 30fs.<br>0 ---- function disable |
| | | DIV_Clock2MHzGEN | | | | | | | | | | | | | | | | | **Divider to Generate 2.048MKHz**<br>000=MCLK/6 001=MCLK/4<br>010=MCLK/8 110=MCLK/12<br>111=MCLK/24<br>Others=MCLK/2 |
| | | GAINCMP | | | | | | | | | | | | | | | | | **RESERVED** |
| | | ADC_RATE | | | | | | | | | | | | | | | | | **ADC SINC Down Select**<br>000 = Down 32 001 = Down 64<br>010 = Down 128 011 = Down 256<br>100 = Down 192 101 = Down 384 |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0x0002 |
| 2C | DAC_CTRL1 | DAC_POPPROTECT_EN | | | | | | | | | | | | | | | | | **DAC POP-SOUND protection enable**<br>1 ---- function enable. While filter type selection changes or MCLKDET down(check MCLKDET_CTRL_EN(0x2C[14] if it is on), digital filter auto-mute to zero with 30fs.<br>0 ---- function disable |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MCLKDET_CTRL_EN | | | | | | | | | | | | | | | | | **(MCLKDET) MCLK down controls reference enable**<br>1 ---- function enable<br>While MCLK down to up, align digital filter reference<br>0 ---- function disable |
| | | ADC/DAC filter starting sync | | | | | | | | | | | | | | | | | Reserved 0 |
| | | DACFLT_TYPE_ZCSW | | | | | | | | | | | | | | | | | **Zero-corssing enable for DAC Filter Types Switching (between DACFLT_TYPESEL 3'b1xx)**<br>1 ---- zero crossing enable,<br>While DACFLT_TYPESEL is update, internal function siwching checks input signal zero crossing point<br>0 ---- zero crossing disable<br>while DACFLT_TYPESEL is update, internal function updatse immediately |
| | | DACFLT_TYPESEL | | | | | | | | | | | | | | | | | **DAC Filter Type Selection**<br>0xx ---- sharp roll-off, long delay(default)<br>100 ---- sharp roll-off, long delay linear phase<br>101 ---- slow roll-off, short delay linear phase<br>110 ---- sharp roll-off, short delay non-linear phase<br>111 ---- slow roll-off, short delay non-linear phase |
| | | CICCLP_OFF | | | | | | | | | | | | | | | | | 0 = (DEFAULT) |
| | | CIC_GAIN_ADJ | | | | | | | | | | | | | | | | | **Gain Adjustment**<br>(Fine tunes the DAC output) |
| | | DACOUT_FORMAT | | | | | | | | | | | | | | | | | **DAC output data format**<br>1 --- signed data<br>0 --- unsigned data |
| | | DAC_RATE | | | | | | | | | | | | | | | | | **DAC Oversample Rate Select**<br>000 = 64 or 400Fs 001 = 256<br>010 = 128 100 = 32<br>101 = 192 110 = 384 |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | **0x0082** |
| 2D | DAC_TRL2 | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | SDMOD_DITHER | | | | | | | | | | | | | | | | | **Bit Numbers Of Dithering On SD Modulator**<br>(Step size is 1bit.)<br>00000 = No dithering (DEFAULT)<br>00001 = 1<br>00010 = 2<br>00011 = 3<br>00100 = 4<br>00101 = 5<br>00110 = 6<br>00111 = 7<br>01000 = 8<br>01001 = 9<br>01010 = 10<br>01011 = 11<br>01100 = 12<br>01101 = 13<br>01110 = 14<br>01111 = 15 |
| | | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x0000** |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2F | DAC_DGAIN_CTRL | DAC1_TO_DAC0_ST | | | | | | | | | | | | | | | | | **DAC CH1 to DAC CH0 Crosstalk Suppression Sidetone Select**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB<br>▼<br>0x43 = -70dB<br>0x42 = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute<br>0x00 = Mute (DEFAULT) |
| | | DAC0_TO_DAC1_ST | | | | | | | | | | | | | | | | | **DAC CH0 to DAC CH1 Crosstalk Suppression Sidetone Select**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB<br>▼<br>0x43 = -70dB<br>0x42 = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute<br>0x00 = Mute (DEFAULT) |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 30 | ADC_DGAIN_CTRL | ADC_TO_DAC_ST0 | | | | | | | | | | | | | | | | | **ADC to DAC CH0 Sidetone Select**<br>(Step size is 3dB.)<br>0x00 = Mute (DEFAULT)<br>0x01 = -42dB<br>▼<br>0x0E = -3dB<br>0x0F = 0dB |
| | | ADC_TO_DAC_ST1 | | | | | | | | | | | | | | | | | **ADC to DAC CH1 Sidetone Select**<br>(Step size is 3dB.)<br>0x00 = Mute (DEFAULT)<br>0x01 = -42dB<br>▼<br>0x0E = -3dB<br>0x0F = 0dB |
| | | DAC_ST_SEL0 | | | | | | | | | | | | | | | | | **DAC CH0 Sidetone Source Select**<br>0 = Select ADC CH0 as the side tone source of the DAC CH0 (DEFAULT)<br>1 = Select ADC CH1 as the side tone source of the DAC CH0 |
| | | DAC_ST_SEL1 | | | | | | | | | | | | | | | | | **DAC CH1 Sidetone Source Select**<br>0 = Select ADC CH1 as the side tone source of the DAC CH1 (DEFAULT)<br>1 = Select ADC CH0 as the side tone source of the DAC CH1 |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 31 | MUTE_CTRL | PGA_SMUTE_STEP | | | | | | | | | | | | | | | | | **Analog Attn Mute Step Select**<br>00 = 128 sample 01 = 32 sample (DEFAULT)<br>10 = 16 sample 11 = 1 sample |
| | | DAC_SLOW_UM | | | | | | | | | | | | | | | | | **DAC Slow Soft Unmute Enable Control**<br>0 = Disable (16 MCLK per step soft unmute) (DEFAULT)<br>1 = Enable (512 MCLK per step soft unmute) |
| | | DAC_ZC_UP_EN | | | | | | | | | | | | | | | | | **DAC Zero Crossing Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | AMUTE_EN | | | | | | | | | | | | | | | | | **Auto Mute Enable Control for ADC**<br>(Generate null output to analog circuitry when 1024 |

| REG | Function | Name | Bit | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | | | | | | | | | | | | | | | | | | consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | AMUTE_CTRL | | | | | | | | | | | | | | | | | **Auto Mute Control**<br>0 = Both DAC channels must have 0 values for 1024 samples before AMUTE turns on (DEFAULT)<br>1 = Either Ch0 or Ch1 must have 1024 consecutive zero samples |
| | | SMUTE_EN | | | | | | | | | | | | | | | | | **Soft Mute Enable Control**<br>0 = Gradually increase DAC volume to volume register setting (DEFAULT)<br>1 = Gradually lower DAC volume to zero |
| | | SUMTE_CTRL | | | | | | | | | | | | | | | | | **DAC Limiter Output Enable Control**<br>0 = (DEFAULT)<br>1 = (When soft mute is enabled, DAC limiter output is also muted to remove any DC offset produced by the audio processing block.) |
| | | ADC_ZC_UP_EN | | | | | | | | | | | | | | | | | **ADC Zero Crossing Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | ADC_SMUTE_EN | | | | | | | | | | | | | | | | | **ADC Soft Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | ADC_SMUTE_CTRL | | | | | | | | | | | | | | | | | 0: Default<br>1: When soft mute is enabled, ADC limiter output is also muted to remove any dc offset produced by the audio processing block |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **32** | **HSVOL_CTRL** | HSPGA_ATTN_EN | | | | | | | | | | | | | | | | | **Headphone Diver Manual Attn Enable Control**<br>(With HSPGA_ATTN_EN and AMUTE_EN enabled)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | HSPGA_ATTN_AUTO_MODE | | | | | | | | | | | | | | | | | **Headphone Driver Auto Attn Enable Control**<br>(With HSPGA_ATTN_AUTO_MODE and AMUTE_EN enabled)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTE_HSPGA2 | | | | | | | | | | | | | | | | | **Right Channel Headphone Driver Manual Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTE_HSPGA1 | | | | | | | | | | | | | | | | | **Left Channel Headphone Driver Manual Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | HSPGA1_VOL | | | | | | | | | | | | | | | | | **Left Channel Headphone Driver Volume Control**<br>00 = 0dB (DEFAULT)<br>01 = -3dB<br>10 = -6dB<br>11 = -9dB |
| | | HSPGA2_VOL | | | | | | | | | | | | | | | | | **Right Channel Headphone Driver Volume Control**<br>00 = 0dB (DEFAULT)<br>01 = -3dB<br>10 = -6dB<br>11 = -9dB |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **34** | **DAC_CTRL** | DGAINR_DAC | | | | | | | | | | | | | | | | | **DAC Right Volume Control**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB (DEFAULT)<br>▼<br>0x4B = -66dB<br>0x4A = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | 0x00 = Mute |
| | | DGAINL_DAC | | | | | | | | | | | | | | | | | **DAC Left Volume Control**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB (DEFAULT)<br>▼<br>0x4B = -66dB<br>0x4A = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute<br>0x00 = Mute |
| | | **DEFAULT** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **0xCFCF** |
| **35** | **ADC_DGAIN_CTRL1** | DGAINR_ADC | | | | | | | | | | | | | | | | | **ADC Right Volume Control**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB (DEFAULT)<br>▼<br>0x4B = -66dB<br>0x4A = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute<br>0x00 = Mute |
| | | DGAINL_ADC | | | | | | | | | | | | | | | | | **ADC Left Volume Control**<br>(Step size is 0.5dB.)<br>0xFF = +24dB<br>0xFE = +23.5dB<br>▼<br>0xCF = 0dB (DEFAULT)<br>▼<br>0x4B = -66dB<br>0x4A = RESERVED<br>▼<br>0x0F = RESERVED<br>0x0E = Mute<br>0x00 = Mute |
| | | **DEFAULT** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **1** | **1** | **1** | **0xCFCF** |
| **36** | **ADC_DRC_KNEE_IP12** | DRC_ENA_ADC | | | | | | | | | | | | | | | | | **DRC ADC Channel Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DRC_KNEE2_IP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Knee Point 2 Select**<br>(Step size is 1dB.)<br>0x00 = 0dB<br>0x01 = -1dB<br>▼<br>0x14 = -20dB (DEFAULT)<br>▼<br>0x3E = -62dB<br>0x3F = -63dB |
| | | DRC_SMTH_ENA_ADC | | | | | | | | | | | | | | | | | **DRC ADC Smooth Filter Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | DRC_KNEE1_IP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Knee Point 1 Select**<br>(Step size is 1dB.)<br>0x00 = 0dB<br>0x01 = -1dB<br>▼<br>0x06 = -6dB (DEFAULT)<br>▼ |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | 0x1E = -30dB<br>0x1F = -31dB |
| | | DEFAULT | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | **0x1486** |
| 37 | ADC_DRC_KNEE_IP34 | DRC_KNEE4_IP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Knee Point 4 Select**<br>(Step size is 1dB.)<br>0x00 = -35dB<br>0x01 = -36dB<br>▼<br>0x0F = -50dB (DEFAULT)<br>▼<br>0x3E = -97dB<br>0x3F = -98dB |
| | | DRC_KNEE3_IP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Knee Point 3 Select**<br>(Step size is 1dB.)<br>0x00 = -18dB<br>0x01 = -19dB<br>▼<br>0x12 = -36dB (DEFAULT)<br>▼<br>0x1E = -80dB<br>0x1F = -81dB |
| | | DEFAULT | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | **0x0F12** |
| 38 | ADC_DRC_SLOPES | DRC_NG_SLP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Noise Gate Slope**<br>000 = 1:1 001 = 2:1<br>010 = 4:1 (default) 011 = 8:1<br>1xx = reserved |
| | | DRC_EXP_SLP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Expansion Slope**<br>000 = 1:1 001 = 2:1<br>010 = 4:1 (default) 011 = Reserved<br>1xx = reserved |
| | | DRC_CMP2_SLP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Compressor Slope (Lower Region)**<br>000 = 0 001 = 1:2<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101-110 = RESERVED<br>111 = 1<br>(DEFAULT) |
| | | DRC_CMP1_SLP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Compressor Slope (Higher Region)**<br>000 = 0 001 = 1:2<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101-110 = RESERVED<br>111 = 1<br>(DEFAULT) |
| | | DRC_LMT_SLP_ADC | | | | | | | | | | | | | | | | | **DRC ADC Limiter Slope**<br>000 = 0 001 = 1:2<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101 = 1:32<br>110 = 1:64 111 = 1 (DEFAULT) |
| | | DEFAULT | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | **0x25FF** |
| 39 | ADC_DRC_ATKDCY | DRC_PK_COEF1_ADC | | | | | | | | | | | | | | | | | **DRC ADC Peak Detection Attack Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = Ts 0001 = 3*Ts<br>0010 = 7*Ts 0011 = 15*Ts (DEFAULT)<br>0100 = 31*Ts 0101 = 63*Ts<br>0110 = 127*Ts 0111 = 255*Ts<br>1xxx reserved |
| | | DRC_PK_COEF2_ADC | | | | | | | | | | | | | | | | | **DRC ADC Peak Detection Release Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = 63*Ts 0001 = 127*Ts<br>0010 = 255*Ts 0011 = 511*Ts<br>0100 = 1023*Ts 0101 = 2047*Ts (DEFAULT)<br>0110 = 4095*Ts 0111 = 8191*Ts<br>1xxx reserved |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | DRC_ATK_ADC | | | | | | | | | | | | | | | | | **DRC ADC Attack Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = Ts 0001 = 3*Ts<br>0010 = 7*Ts 0011 = 15*Ts<br>0100 = 31*Ts 0101 = 63*Ts (DEFAULT)<br>0110 = 127*Ts 0111 = 255*Ts<br>1000 = 511*Ts 1001 = 1023*Ts<br>1010 = 2047*Ts 1011 = 4095*Ts<br>1100 = 8191*Ts |
| | | DRC_DCY_ADC | | | | | | | | | | | | | | | | | **DRC ADC Decay Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = 63*Ts 0001 = 127*Ts<br>0010 = 255*Ts 0011 = 511*Ts<br>0100 = 1023*Ts 0101 = 2047*Ts<br>0110 =4095*Ts 0111 = 8191*Ts (DEFAULT)<br>1000 = 16383*Ts 1001 = 32768*Ts<br>1010 = 65535*Ts |
| | | **DEFAULT** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **0x3457** |
| **3A** | **DAC_DRC_KNEE_IP12** | DRC_ENA_DAC | | | | | | | | | | | | | | | | | **DRC DAC Channel Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DRC_KNEE2_IP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Knee Point 2 Select**<br>(Step size is 1dB.)<br>0x00 = 0dB<br>0x01 = -1dB<br>▼<br>0x14 = -20dB (DEFAULT)<br>▼<br>0x1E = -62dB<br>0x1F = -63dB |
| | | DRC_SMTH_ENA_DAC | | | | | | | | | | | | | | | | | **DRC DAC Smooth Filter Enable Control**<br>0 = Disable<br>1 = Enable (DEFAULT) |
| | | DRC_KNEE1_IP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Knee Point 1 Select**<br>(Step size is 1dB.)<br>0x00 = 0dB<br>0x01 = -1dB<br>▼<br>0x06 = -6dB (DEFAULT)<br>▼<br>0x1E = -30dB<br>0x1F = -31dB |
| | | **DEFAULT** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **0** | **1** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0x1486** |
| **3B** | **DAC_DRC_KNEE_IP34** | DRC_KNEE4_IP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Knee Point 4 Select**<br>(Step size is 1dB.)<br>0x00 = -35dB<br>0x01 = -36dB<br>▼<br>0x0F = -50dB (DEFAULT)<br>▼<br>0x1E = -65dB<br>0x1F = -66dB |
| | | DRC_KNEE3_IP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Knee Point 3 Select**<br>(Step size is 1dB.)<br>0x00 = -18dB<br>0x01 = -19dB<br>▼<br>0x12 = -36dB (DEFAULT)<br>▼<br>0x3E = -97dB<br>0x3F = -98dB |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **1** | **1** | **1** | **1** | **0** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **0x0F12** |
| **3C** | **DAC_DRC_SLOPES** | DRC_NG_SLP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Noise Gate Slope**<br>00 = 1:1 01 = 2:1<br>10 = 4:1 (DEFAULT) 11 = 8:1<br>1xx reserved |
| | | DRC_EXP_SLP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Expansion Slope**<br>00 = 1:1 01 = 2:1<br>10 = 4:1 (DEFAULT) 11 = 8:1 |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | | | | | | | | | | | | 1xx reserved |
| | | DRC_CMP2_SLP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Compressor Slope (Lower Region)**<br>000 = 0 001 = 1:2<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101-110 = RESERVED<br>111 = 1 (DEFAULT) |
| | | DRC_CMP1_SLP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Compressor Slope (Higher Region)**<br>000 = 0 001 = 1:2<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101-110 = RESERVED<br>111 = 1 (DEFAULT) |
| | | DRC_LMT_SLP_DAC | | | | | | | | | | | | | | | | | **DRC DAC Limiter Slope**<br>000 = 0 001 = 1:2 (DEFAULT)<br>010 = 1:4 011 = 1:8<br>100 = 1:16 101 = 1:32<br>110 = 1:64 111 = 1 |
| | | **DEFAULT** | **0** | **0** | **1** | **0** | **0** | **1** | **0** | **1** | **1** | **1** | **1** | **1** | **1** | **0** | **0** | **1** | **0x25F9** |
| **3D** | **DAC_DRC_ATKDCY** | DRC_PK_COEF1_DAC | | | | | | | | | | | | | | | | | **DRC DAC Peak Detection Attack Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = Ts 0001 = 3*Ts<br>0010 = 7*Ts 0011 = 15*Ts (DEFAULT)<br>0100 = 31*Ts 0101 = 63*Ts<br>0110 = 127*Ts 0111 = 255*Ts<br>1XXX = RESERVED |
| | | DRC_PK_COEF2_DAC | | | | | | | | | | | | | | | | | **DRC DAC Peak Detection Release Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = 63*Ts 0001 = 127*Ts<br>0010 = 255*Ts 0011 = 511*Ts<br>0100 = 1023*Ts (DEFAULT) 0101 = 2047*Ts<br>0110 = 4095*Ts 0111 = 8191*Ts<br>1XXX = RESERVED |
| | | DRC_ATK_DAC | | | | | | | | | | | | | | | | | **DRC DAC Attack Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = Ts 0001 = 3*Ts<br>0010 = 7*Ts 0011 = 15*Ts<br>0100 = 31*Ts 0101 = 63*Ts (DEFAULT)<br>0110 = 127*Ts 0111 = 255*Ts<br>1000 = 511*Ts 1001 = 1023*Ts<br>1010 = 2047*Ts 1011 = 4095*Ts<br>1100 = 8191*Ts |
| | | DRC_DCY_DAC | | | | | | | | | | | | | | | | | **DRC DAC Decay Time**<br>(Ts = 1/SMPL_RATE)<br>0000 = 63*Ts 0001 = 127*Ts<br>0010 = 255*Ts 0011 = 511*Ts<br>0100 = 1023*Ts 0101 = 2047*Ts<br>0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT)<br>1000 = 16383*Ts 1001 =32757*Ts<br>1010 = 65535*Ts |
| | | **DEFAULT** | **0** | **0** | **1** | **1** | **0** | **1** | **0** | **0** | **0** | **1** | **0** | **1** | **0** | **1** | **1** | **1** | **0x3457** |
| **41** | **BIQ1_COF1** | **BIQ1_A1_L** | | | | | | | | | | | | | | | | | **Program DAC BIQ1_A1 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **42** | **BIQ1_COF2** | **BIQ1_A1_H** | | | | | | | | | | | | | | | | | **Program DAC BIQ1_A1 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **43** | **BIQ1_COF3** | **BIQ1_A2_L** | | | | | | | | | | | | | | | | | **Program DAC BIQ1_A2 Parameter Bit[15:0]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **44** | **BIQ1_COF4** | **BIQ1_A2_H** | | | | | | | | | | | | | | | | | **Program DAC BIQ1_A2 Parameter Bit[23:16]** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 45 | BIQ1_COF5 | BIQ1_B0_L | | | | | | | | | | | | | | | | | Program DAC BIQ1_B0 Parameter Bit[15:0] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 46 | BIQ1_COF6 | BIQ1_B0_H | | | | | | | | | | | | | | | | | Program DAC BIQ1_B0 Parameter Bit[23:16] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 47 | BIQ1_COF7 | BIQ1_B1_L | | | | | | | | | | | | | | | | | Program DAC BIQ1_B1 Parameter Bit[15:0] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 48 | BIQ1_COF8 | BIQ1_B1_H | | | | | | | | | | | | | | | | | Program DAC BIQ1_B1 Parameter Bit[23:16] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 49 | BIQ1_COF9 | BIQ1_B2_L | | | | | | | | | | | | | | | | | Program DAC BIQ1_B2 Parameter Bit[15:0] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 4A | BIQ1_COF10 | BIQ1_EN | | | | | | | | | | | | | | | | | **BIQ1 DAC Path Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BIQ1_B2_H | | | | | | | | | | | | | | | | | Program DAC BIQ1_B2 Parameter Bit[23:16] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 4B | CLASSG_CTRL | CLASSG_CLK_SRC | | | | | | | | | | | | | | | | | **Class G Function Clock Divider**<br>00 = Clock 2MHz (DEFAULT) 01 = 1/3 MCLK<br>10 = MCLK 11 = Disable CLK |
| | | CLASSG_TIMER | | | | | | | | | | | | | | | | | **Define The Number Of Milliseconds**<br>(When a Class-G mode signal to go low after it has been below the threshold.)<br>000001 = 1ms 000010 = 2ms<br>000100 = 8ms 001000 = 16ms<br>010000 = 32ms 100000 = 64ms |
| | | CLASSG_THRSLD | | | | | | | | | | | | | | | | | **Threshold for DAC Signal Level Comparison To Generate Class-G Mode Signal**<br>00 = 1/16 Full Scale (DEFAULT) 01 = 1/8 Full Scale<br>10 = 3/16 Full Scale 11 = 1/4 Full Scale |
| | | CLASSG_CMP_EN | | | | | | | | | | | | | | | | | **Class-G Compare Path Enable Bit**<br>(Each bit enables according DAC path.)<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left DAC<br>Bit1 = Right DAC |
| | | CLASSG_EN | | | | | | | | | | | | | | | | | **Class-G Function Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 4C | IMM_MODE_CTRL | RESERVED | | | | | | | | | | | | | | | | | RESERVED |
| | | IMM_THRESHOLD | | | | | | | | | | | | | | | | | **Impedance Measurement Threshold To Avoid False Detection**<br>(Each increase raises the floor of the ADC requiring higher signal levels before activation.)<br>0x00 = [23:0] Full Range (DEFAULT)<br>0x01 = [23:1]<br>▼<br>0x14 = [23:20]<br>0x15 = [23:21] |
| | | IMM_GEN_VOL | | | | | | | | | | | | | | | | | **Signal Level Of The 23Hz Sinewave Generation For Impedance Measurement**<br>00 = 1/2 Full Scale (DEFAULT) 01 = 1/4 Full Scale<br>10 = 1/8 Full Scale 11 = 1/16 Full Scale |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | IMM_CYCLE_CNT | | | | | | | | | | | | | | | | | **Number Of MCLK**<br>(Used to calculate the impedance)<br>00 = 1024 01 = 2048 (DEFAULT)<br>10 = 4096 11 = 8192 |
| | | IMM_MODE | | | | | | | | | | | | | | | | | **Impedance Measurement Mode Enable Conrol**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | IMM_MODE_CHSEL | | | | | | | | | | | | | | | | | Impedance measuremet channel selection<br>1 --- right channel<br>0 --- left channel |
| | | DACIN_SRC | | | | | | | | | | | | | | | | | **DAC Filter Input Source Selection**<br>(IMM_MODE enabled from built-in sine generator)<br>00 = From DRC DAC Output (DEFAULT)<br>01 = From DAC Mixer Output<br>10 = From u/A-law decode output<br>11 = None |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **4D** | **IMM_RMS_L** | | | | | | | | | | | | | | | | | | **Left Headset Speaker Impedance Readout**<br>(It is recommended to characterize this before use with known Impedance values.) |
| | | **DEFAULT** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **READ ONLY** |
| **4E** | **FUSE_CTRL2** | **FUSEIN_L** | | | | | | | | | | | | | | | | | **The Lower 16 bits Of The FUSEIN**<br>(These register bits are OR ed with the Fuse latches and can be used for test characterization except during reset or after power on reset.) |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **4F** | **FUSE_CTRL3** | **RESERVED** | | | | | | | | | | | | | | | | | **RESERVED** |
| | | **FUSEIN_H** | | | | | | | | | | | | | | | | | **The Higher 2 Bits Of The FUSEIN**<br>(These register bits are OR ed with the Fuse latches and can be used for test characterization except during reset or after power on reset.) |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **51** | **FUSE_CTRL1** | **FUSE_PRG_MODE** | | | | | | | | | | | | | | | | | **Set eFuse mode**<br>0 = Not in the programming mode (DEFAULT)<br>1 = In the programming mode |
| | | **FUSWBNKIN** | | | | | | | | | | | | | | | | | **Set Bank of 32 eFuse Used For Programming The eFuse**<br>0 = Bank 0 (DEFAULT)<br>1 = Bank 1 |
| | | **FUSEPRGBNK** | | | | | | | | | | | | | | | | | (Set this signal to 1 will instantly program the eFuse that selects the bank of 32 eFuses during a read operation.) |
| | | **FUSEPRGEN** | | | | | | | | | | | | | | | | | (Set this signal to 1 will program the selected eFuse.) |
| | | **RUSEREAD** | | | | | | | | | | | | | | | | | (Set this signal to 1 will read the bank of 32 eFuses selected by the fuse bank eFuse.) |
| | | **FUSERESETB** | | | | | | | | | | | | | | | | | (Set this signal to 0 will reset the 32 eFuse latches. This signal should be 1 after any read cycle.) |
| | | **FUSESEL** | | | | | | | | | | | | | | | | | (The eFuse address bus for programming. Only one bit can be programmed at a time. ) |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| **53** | **OTPDOUT_1** | **OTPDOUT_L** | | | | | | | | | | | | | | | | | **OTP Read Out Data Low 16 Bits** |
| | | **DEFAULT** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **READ ONLY** |
| **54** | **OTPDOUT_2** | **OTPDOUT_BANK** | | | | | | | | | | | | | | | | | **OTP bank read out** |
| | | **OTPDOUT_H** | | | | | | | | | | | | | | | | | **OTP Read Out Data High 2 Bits** |
| | | **DEFAULT** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **X** | **READ ONLY** |
| **55** | **IMM_MODE_CHSEL** | **SPI 3-WIRE ENA** | | | | | | | | | | | | | | | | | **3-wire write Mode Control**<br>**1 = Enable**<br>**0 = Disable** |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | ADC Clock out to ANA | | | | | | | | | | | | | | | | | Clock out from digital to analog<br>1 –BCLK<br>0—CLK_ADC |
| | | ADC_ANA_TESTCHSEL | | | | | | | | | | | | | | | | | ADC 5bits analog testing chaneel selection<br>1 --- left channel<br>0 --- right channel |
| | | ADC_ANA_TEST | | | | | | | | | | | | | | | | | ADC 5bits analog testing<br>1 – test on<br>{SD,GPIO2,GPIO1,DACDAT,ADCDAT0} |
| | | RAM_TEST_START | | | | | | | | | | | | | | | | | Ram Test Control<br>1 = Enable<br>0 = Disable |
| | | D2A_LOOP | | | | | | | | | | | | | | | | | 1: Use DAC ~~Left~~ Filter Input as ADC decimation filter output |
| | | DAC_TEST | | | | | | | | | | | | | | | | | DAC 6bits testing<br>1 --- test on<br>[GPIO1, BCLK,LRC,DACDAT,SD,SCLK] |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0x0000 |
| 58 | I2C_DEVICE_ID | I2C_DEVICE_ID | | | | | | | | | | | | | | | | | I2C Device ID Read In |
| | | KEYDET | | | | | | | | | | | | | | | | | Key Detect Status Bit |
| | | MICDET | | | | | | | | | | | | | | | | | MICDETECT Status Bit |
| | | SILICON REVISION ID | | | | | | | | | | | | | | | | | Silicon Revision Bits |
| | | Software ID | | | | | | | | | | | | | | | | | Software ID 00=NAU8821C |
| | | DEFAULT | X | 0 | 0 | 1 | 1 | 0 | 1 | X | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | READ ONLY |
| 59 | SARDOUT_RAM_STATUS | RATM_TEST_FINISH | | | | | | | | | | | | | | | | | RAM Test Status Bit<br>0 = Test not finished<br>1 = Test finished |
| | | RAM_TEST_FAIL | | | | | | | | | | | | | | | | | RAM Test Result Bit<br>0 = Test passed<br>1 = Test failed |
| | | ANALOG_MUTE | | | | | | | | | | | | | | | | | Analog Mute Flag Bit<br>0 = Disable<br>1 = Enable |
| | | DEFAULT | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | READ ONLY |
| 5A | SOFTWARE_RST | SW_RESET | | | | | | | | | | | | | | | | | Software Reset<br>(Write any value ***twice*** to reset all internal states without resetting the config registers.) |
| 66 | BIAS_ADJ | TESTRL | | | | | | | | | | | | | | | | | Headphone Impedance Enable Control<br>(Test/ IMM_MODE)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTEL | | | | | | | | | | | | | | | | | Left PGA Mute Enable Control<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTER | | | | | | | | | | | | | | | | | Right PGA Mute Enable Control<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | TESTDAC | | | | | | | | | | | | | | | | | DAC Right, Left Test Only |
| | | RESERVED | | | | | | | | | | | | | | | | | RESERVED |
| | | VMIDEN | | | | | | | | | | | | | | | | | VMID Enable Control<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | VMIDSEL | | | | | | | | | | | | | | | | | VMID Tie-off Impedance Select<br>00 = Open (DEFAULT)<br>10 = 125 KOhms<br>01 = 25 KOhms<br>11 = 2.5 KOhms |
| | | RESERVED | | | | | | | | | | | | | | | | | RESERVED |
| | | RESERVED | | | | | | | | | | | | | | | | | RESERVED |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | BIASADJ | | | | | | | | | | | | | | | | | **PGA Master Bias Current Power Select**<br>00 = Normal operation (DEFAULT)<br>01 = 9% reduced bias current from normal<br>10 = 17% reduced bias current from normal<br>11 = 11% increased bias current from normal |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 69 | ANALOG_CONTROL_1 | TESTDACIN | | | | | | | | | | | | | | | | | **DAC Test Signal**<br>00 & 11 = GND (DEFAULT)<br>01 & 10 = High & Low |
| | | PULLUP_GPIO2 | | | | | | | | | | | | | | | | | **GPIO2JD1 Pull Up Select**<br>0 = 1MOhm (DEFAULT)<br>1 = 100KOhm |
| | | GPIO2THL | | | | | | | | | | | | | | | | | **GPIO2 JKDET1 Threshold Low Select**<br>00 = 0.22 x VDDA (DEFAULT)<br>10 = 0.40 x VDDA<br>11 = 0.5 x VDDA |
| | | GPIO2THH | | | | | | | | | | | | | | | | | **GPIO2 JKDET1 Threshold High Select**<br>00 = 0.85 x VDDA (DEFAULT)<br>10 = 0.78 x VDDA<br>11 = 0.6 x VDDA |
| | | DMICSEL2 | | | | | | | | | | | | | | | | | **DMIC MUX Select**<br>0 = MICL- (DEFAULT)<br>1 = MICR+ |
| | | JD1POL | | | | | | | | | | | | | | | | | **JKDETL JD1 Polarity**<br>0 = Non-inverted (DEFAULT)<br>1 = Inverted |
| | | JKDETLPOL | | | | | | | | | | | | | | | | | **JKDETL Output Polarity**<br>0 = Non-inverted (DEFAULT)<br>1 = Inverted |
| | | ENJKDETL | | | | | | | | | | | | | | | | | **Enable Jack Tip Insertion Detection Circuit** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 6A | ANALOG_CONTROL_2 | HP_AB_ADJ | | | | | | | | | | | | | | | | | **Headphone Driver Class-AB Bias Current Adjust In Non-Class-G Mode**<br>0 = Normal (DEFAULT)<br>1 = 2x |
| | | HP_G_ADJ | | | | | | | | | | | | | | | | | **Headphone Driver Bias Current Adjust In Class-G Mode**<br>0 = Normal (DEFAULT)<br>1 = 0.5x |
| | | HP_ADJ | | | | | | | | | | | | | | | | | **Headphone Driver Bias Current Adjust In non Class-G Mode**<br>0 = Normal (DEFAULT)<br>1 = 2.5x |
| | | HP_G_BST_ADJ2 | | | | | | | | | | | | | | | | | **Headphone Out Boost Driver Bias Current Adjust in Class-G Mode 1**<br>0 = Normal (DEFAULT)<br>1 = Low |
| | | HP_G_BST_ADJ2 | | | | | | | | | | | | | | | | | **Headphone Out Boost Driver Bias Current Adjust in Class-G Mode 2**<br>0 = Normal (DEFAULT)<br>1 = Low |
| | | HP_AB_ADJ | | | | | | | | | | | | | | | | | **Headphone Driver Bias Adjust In Class-AB**<br>0 = Normal (DEFAULT)<br>1 = Increase bias |
| | | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | CAPMSB | | | | | | | | | | | | | | | | | **DAC Reference Decoupling Capacitor Enable MSB** |
| | | CAPLSB | | | | | | | | | | | | | | | | | **DAC Reference Decoupling Capacitor Enable LSB** |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 6B | | MUTENL | | | | | | | | | | | | | | | | | **MICLN Input to PGA Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>When enabling one of MICNL or MICPL mute, PGAL becomes a single-ended configuration, and PGAL gain becomes doubled. When both MICL and MICLP muted, the PGAL has no input. Same operaton as MUTENR and MUTEPR. |

| REG | Function | Name | Bit | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | MUTENR | | | | | | | | | | | | | | | | | **MICRN Input to PGA Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTEPL | | | | | | | | | | | | | | | | | **MICLP Input to PGA Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MUTEPR | | | | | | | | | | | | | | | | | **MICRP Input to PGA Mute Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x0000** |
| 71 | ANALOG_ADC_1 | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | PDMICDET | | | | | | | | | | | | | | | | | **MIC Detection Power Down Control**<br>0 = Power on MIC detection (DEFAULT)<br>1 = Power down MIC detection |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | **0x0011** |
| 72 | ANALOG_ADC_2 | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | ADC_UPL | | | | | | | | | | | | | | | | | **Left Channel PGA Bias Current Increase Enable Control**<br>(For driving ADC at high sample rates)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | ADC_UPR | | | | | | | | | | | | | | | | | **Right Channel PGA Bias Current Increase Enable Control**<br>(For driving ADC at high sample rates)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BIAS | | | | | | | | | | | | | | | | | **ADC Bias Current Select**<br>00 = Nominal (DEFAULT)<br>01 = Double<br>10 = Half<br>11 = Quarter |
| | | VREFSEL | | | | | | | | | | | | | | | | | **ADC VREF Select**<br>00 = Analog supply (DEFAULT)<br>01 = 1.55<br>10 = 1.65<br>11 = 1.75 |
| | | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | PDNOTL | | | | | | | | | | | | | | | | | **Left ADC Analog Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | PDNOTR | | | | | | | | | | | | | | | | | **Right ADC Analog Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **0x0020** |
| 73 | RDAC | DAC_EN | | | | | | | | | | | | | | | | | **DAC Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left DAC<br>Bit1 = Right DAC |
| | | CLK_DAC_EN | | | | | | | | | | | | | | | | | **DAC Clock Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left DAC<br>Bit1 = Right DAC |
| | | FC_CTR | | | | | | | | | | | | | | | | | **DAC Smoothing Filter On HS Output Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |

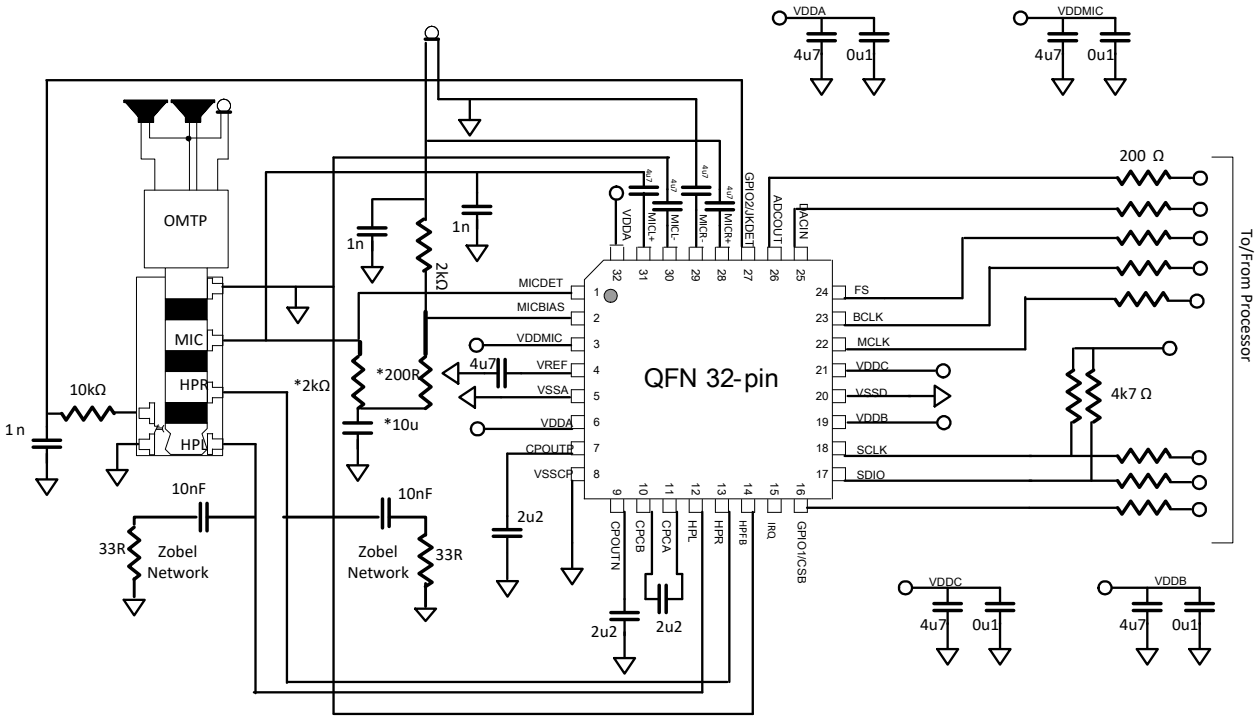
| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CLK_DAC_DELAY | | | | | | | | | | | | | | | | | **DAC Clock Delay Select**<br>000 = Delay 0 nsec (DEFAULT)<br>100 = Delay 4 nsec<br>001 = Delay 1 nsec<br>101 = Delay -3 nsec<br>010 = Delay 2 nsec (Recommended)<br>110 = Delay -2 nsec<br>011 = Delay 3 nsec<br>111 = Delay -1 nsec |
| | | DACVREFSEL | | | | | | | | | | | | | | | | | **DAC Full Scale Reference Voltage Select**<br>(By setting this value, it will change DAC full scale output. For best performance, use default value.)<br>00 = External VDDA<br>01 = 1.55V<br>10 = 1.65V (DEFAULT)<br>11 = 1.75V |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **0** | **0** | **0** | **0x0008** |
| **74** | **MIC_BIAS** | INT2KA | | | | | | | | | | | | | | | | | **MICBIAS1 Internal 2K Ohm Resistor For MCGND Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | LOWNOISE | | | | | | | | | | | | | | | | | **Low Power / Low Noise Mode Select**<br>0 = Low power mode (DEFAULT)<br>1 = Low noise mode |
| | | POWERUP | | | | | | | | | | | | | | | | | **MICBIAS1 Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | MICBIASLVL1 | | | | | | | | | | | | | | | | | **MICBIAS1 Output Level Select**<br>000 = VDDA<br>001 = 1x<br>010 = 1.1x<br>011 = 1.2x<br>100 = 1.3x<br>101 = 1.4x<br>110 = 1.53x<br>111 = 1.53x |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **1** | **1** | **0** | **0x0006** |
| **76** | **BOOST** | CLR_APR_EMRGENCY_SHTDWN | | | | | | | | | | | | | | | | | **Clear Headset Short Circuit Shutdown IRQ**<br>0 = (DEFAULT)<br>1 = Reset (Momentary) |
| | | STG2_SEL | | | | | | | | | | | | | | | | | **PGA In Class-A Mode Of Operation Enable Instead Of Class-AB Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | PDVMDFST | | | | | | | | | | | | | | | | | **VMID Pre-charge Disable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BIASEN | | | | | | | | | | | | | | | | | **Global Analog Bias Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DISCHRG | | | | | | | | | | | | | | | | | **Charge Input Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BYPS_IBCTR | | | | | | | | | | | | | | | | | **Bypass PGA Current Control Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | BOOSTDIS | | | | | | | | | | | | | | | | | **HP Boost Driver Disable Control**<br>0 = Enable (DEFAULT)<br>1 = Disable |
| | | BOOSTGDIS | | | | | | | | | | | | | | | | | **HP Boost Driver In Class-G Mode Disable Control**<br>0 = Enable (DEFAULT)<br>1 = Disable |
| | | SHRT_SHTDWN_DIG_EN | | | | | | | | | | | | | | | | | **Short Circuit Shut Down Digital Part Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |

| REG | Function | Name | Bit | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | EN_SHRT_SHTDWN | | | | | | | | | | | | | | | | | **Automatic Short-circuit Shutdown Enable Control**<br>0 =<br>(Driver shuts down after 16.3 µsec debounce when shortage detected.<br>IRQ pin Interrupt is generated.<br><br>When SHRT_ SHTDWN_ DIG_EN = 0, APR_EMRGNCY_SHTDWN is cleared if the IRQ pin Interrupt cleared.<br>Users need to clear IRQ pin interrupt.<br><br>When SHRT_ SHTDWN_ DIG_EN = 1, APR_EMRGNCY_SHTDWN is cleared 1630 µsec after shortage removed.<br>Users need to clear IRQ pin interrupt.)<br><br>1 =<br>(Headset driver power will be down immediately when shortage detected. No interrupt will be generated.) |
| | | HS_SHRT_THRESHLD | | | | | | | | | | | | | | | | | **Headset Short Circuit Protection Limit**<br>00= 115mA at +FS (DEFAULT)<br>11= 155mA at +FS |
| | | PAMP_THRSHLD | | | | | | | | | | | | | | | | | **Adjust HS Boost P-driver Bias Current**<br>00 = Normal (DEFAULT)<br>11 = Decrease current |
| | | NAMP_THRSHLD | | | | | | | | | | | | | | | | | **Adjust HS Boost N-driver Bias Current**<br>00 = Normal (DEFAULT)<br>11 = Decrease current |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x0000** |
| 77 | FEPGA | ACDC_CTRL | | | | | | | | | | | | | | | | | **Charge Input To VREF Enable Control**<br>(Effective when DISCHRG = 1)<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Charges MICP to VREF<br>Bit1 = Charges MICN to VREF |
| | | CMLCK_ADJ | | | | | | | | | | | | | | | | | **PGA Common Mode Threshold Lock Adjust**<br>00 = (DEFAULT) |
| | | IB_LOOP_CTR | | | | | | | | | | | | | | | | | **PGA Current Trim**<br>0 = (DEFAULT) |
| | | IBCTR_CODE | | | | | | | | | | | | | | | | | **PGA Current Trim**<br>000 = (DEFAULT) |
| | | FEPGA_MODEL | | | | | | | | | | | | | | | | | **Left PGA Mode Select**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>MODE[0] = Anti-aliasing filter adjust<br>MODE[1] = Disconnects MICP & MICN<br>MODE[2] = No function<br>MODE[3] = Shorts the inputs and terminates with 12kOhm differentially to Vref |
| | | FEPGA_MODER | | | | | | | | | | | | | | | | | **Right PGA Mode Select**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>MODE[0] = Anti-aliasing filter adjust<br>MODE[1] = Disconnects MICP & MICN<br>MODE[2] = No function<br>MODE[3] = Shorts the inputs and terminates with 12kOhm differentially to Vref |
| | | DEFAULT | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x0000** |
| 7E | PGA_GAIN | PGA_GAINL | | | | | | | | | | | | | | | | | **Left PGA Gain Control**<br>(Step size is 1dB.)<br>0x00 = -1dB (DEFAULT)<br>0x01 = 0dB<br>▼<br>0x24 = 35dB<br>0x25 = 36dB |

| REG | Function | Name | Bit 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | PGA_GAINR | | | | | | | | | | | | | | | | | **Right PGA Gain Control**<br>(Step size is 1dB.)<br>0x00 = -1dB (DEFAULT)<br>0x01 = 0dB<br>▼<br>0x24 = 35dB<br>0x25 = 36dB |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 7F | POWER_UP_CONTROL | PUPL | | | | | | | | | | | | | | | | | **Left PGA Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | PUPR | | | | | | | | | | | | | | | | | **Right PGA Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | PUP_INTEG | | | | | | | | | | | | | | | | | **Output Integrator Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left HP driver<br>Bit1 = Right HP driver |
| | | PUP_DRV_INSTG | | | | | | | | | | | | | | | | | **Output Driver Power Enable Control**<br>(To reduce pop noise, turn on this ***first***, then turn on PUP_MAIN_DRV)<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left HP driver<br>Bit1 = Right HP driver |
| | | PUP_MAIN_DRV | | | | | | | | | | | | | | | | | **Main Driver Power Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable<br>Bit0 = Left HP driver<br>Bit1 = Right HP driver |
| | | **DEFAULT** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0** | **0x0000** |
| 80 | CHARGE_PUMP_AND_POWER_DOWN_CONTROL | RESERVED | | | | | | | | | | | | | | | | | **RESERVED** |
| | | BCLK_DS | | | | | | | | | | | | | | | | | **BCLK IO Drive Strength Control**<br>0 = Normal (DEFAULT)<br>1 = Stronger |
| | | FS_DS | | | | | | | | | | | | | | | | | **FS IO Drive Strength Control**<br>0 = Normal (DEFAULT)<br>1 = Stronger |
| | | ADCDAT_DS | | | | | | | | | | | | | | | | | **ADCDAT IO Drive Strength Control**<br>0 = Normal (DEFAULT)<br>1 = Stronger |
| | | SDA_DS | | | | | | | | | | | | | | | | | **SDA IO Drive Strength Control**<br>0 = Normal<br>1 = Stronger (DEFAULT) |
| | | JAMNODCLW | | | | | | | | | | | | | | | | | **RESERVED** |
| | | PDB_DAC | | | | | | | | | | | | | | | | | **DAC Right / Left Power Down Bar Enable Control**<br>00 = Disable<br>11 = Enable (DEFAULT) |
| | | JAMFORCE2 | | | | | | | | | | | | | | | | | **Register Output Force 1 Control**<br>(Charge pump clock to fast)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | JAMFORCE1 | | | | | | | | | | | | | | | | | **Register Output Force 2 Control**<br>(Charge pump clock to fast)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | RNIN | | | | | | | | | | | | | | | | | **Charge Pump Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |

| REG | Function | Name | Bit | | | | | | | | | | | | | | | | Description |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | |
| | | PRECHARGE | | | | | | | | | | | | | | | | | **VPOS Pre-charge Enable Control**<br>(For faster startup)<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DISCHARGEVEE | | | | | | | | | | | | | | | | | **VEE Pad Discharge Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | DISCHARGEVPOS | | | | | | | | | | | | | | | | | **VPOS Pad Discharge Enable Control**<br>0 = Disable (DEFAULT)<br>1 = Enable |
| | | SHCIRSEL2 | | | | | | | | | | | | | | | | | **Charge Up Current Limit 2**<br>0 = Low (DEFAULT)<br>1 = High |
| | | SHCIRSEL1 | | | | | | | | | | | | | | | | | **Charge Up Current Limit 1**<br>0 = Low (DEFAULT)<br>1 = High |
| | | DEFAULT | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **0x0B00** |
| 81 | CHARGE_PUMP_INPUT_READ | APR_EMRGNCY_SHTDWN | | | | | | | | | | | | | | | | | **APR Emergency Short Circuit Shutdown IRQ** |
| | | MODE1BUF | | | | | | | | | | | | | | | | | **Monitor MODE1 State Of Charge Pump Block** |
| | | NODCBUF | | | | | | | | | | | | | | | | | **Monitor Charge Pump Drawing DC Current**<br>0 = Drawing<br>1 = Not drawing (DEFAULT) |
| | | RN2BUF | | | | | | | | | | | | | | | | | **Monitor Charge Pump Enable Status**<br>0 = Off (DEFAULT)<br>1 = On |
| | | VPOSOK | | | | | | | | | | | | | | | | | **Monitor High Voltage Status Of VPOS**<br>0 = Possible short circuit (DEFAULT)<br>1 = Max output (Normal operation) |
| | | VCOMPBUF | | | | | | | | | | | | | | | | | **Monitor Low Voltage & Low Current Status Of Charge Pump**<br>0 = No current<br>1 = With current (DEFAULT) |
| | | FORCE1BUF | | | | | | | | | | | | | | | | | **Monitor Charge Pump Frequency Status**<br>0 = Normal<br>1 = Max frequency (DEFAULT) |
| | | DEFAULT | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **READ ONLY 0x0013** |
| 82 | GENERAL_STATUS | MCLK speed indicator | | | | | | | | | | | | | | | | | **MCLK speed indicator**<br>**00 = 256fs 01=384fs 10=400fs,11=500fs** |
| | | I2S FS short_err | | | | | | | | | | | | | | | | | **FS shortage error flag** |
| | | MCLKDET_IN | | | | | | | | | | | | | | | | | **MCLK detection in** |
| | | BUTTONDET_IN | | | | | | | | | | | | | | | | | **Button detection in** |
| | | MICDET_TOINTR | | | | | | | | | | | | | | | | | **MIC detection to interrupt** |
| | | MICDET_IN | | | | | | | | | | | | | | | | | **MIC detection input** |
| | | JKEJECT_INTR | | | | | | | | | | | | | | | | | **JACK Ejection Interrupt** |
| | | JK_INSERT_INTR | | | | | | | | | | | | | | | | | **JACK Insertion Interrupt** |
| | | JKDET_ON | | | | | | | | | | | | | | | | | **Pre-debounce JACK Status** |
| | | JKDETL | | | | | | | | | | | | | | | | | **JKDETL** |
| | | FUSEBNKOUT | | | | | | | | | | | | | | | | | **Fuse Bank Select Output** |
| | | GPIO2_IN | | | | | | | | | | | | | | | | | **GPIO2 Input** |
| | | GPIO1_IN | | | | | | | | | | | | | | | | | **GPIO1 Input** |
| | | DEFAULT | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | X | **READ ONLY** |

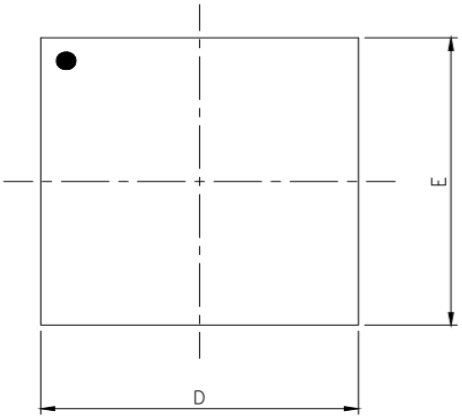
## 12. Typical Application Diagram

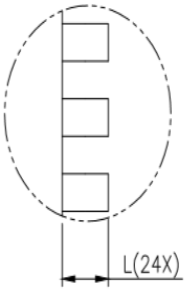


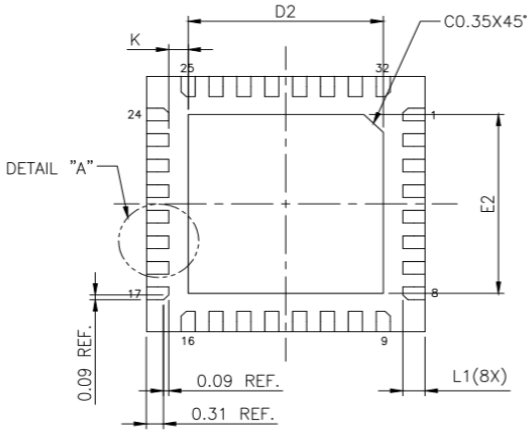

Note: * indicates optional components for improved noise reduction (refer to section 3.5)

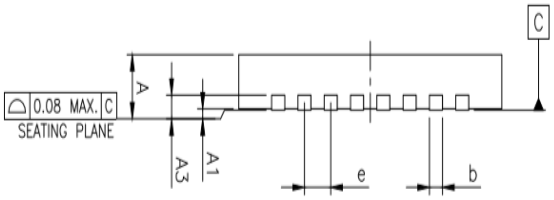
# 13. Package Information

32-lead plastic QFN 32L; 5x5mm2, 0.8mm thickness, 0.5mm lead pitch
(Saw Type) EP SIZE 3.5x3.5mm




| JEDEC OUTLINE | MO-220 | | |
|---|---|---|---|
| PKG CODE | WQFN(X532) | | |
| SYMBOLS | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.203 REF. | | |
| b | 0.18 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| E | 4.90 | 5.00 | 5.10 |
| e | 0.50 BSC | | |
| L | 0.35 | 0.40 | 0.45 |
| L1 | 0.33 | 0.40 | 0.43 |
| K | 0.20 | – | – |

| PAD SIZE | D2 | | | E2 | | | LEAD FINISH | | JEDEC CODE |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | Pure Tin | PPF | |
| 150X15* MIL | 3.45 | 3.50 | 3.55 | 3.45 | 3.50 | 3.55 | V | X | W(V)HHD-5 |

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES :

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

# 14. ORDERING INFORMATION

| Part Number | Dimension | Package | Package Material |
|---|---|---|---|
| NAU88L21CYG | 5x5 mm | QFN-32 | Green |

NAU88L21C _ _

**Package Material:**

**G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant**

**Package Type:**

**Y = QFN-32**

# 15. REVISION HISTORY

| REVISION | DATE | DESCRIPTION |
|---|---|---|
| 1.0 | July 26, 2023 | Initial Release |
| 1.1 | Sep 8, 2023 | Updated pop noise description<br>Updated pin diagram<br>Updated register description |
| 1.2 | Oct 30, 2023 | Updated $T_{DOD}$ description |
| 1.3 | Nov 1, 2023 | Updated package information<br>Updated JKDET pin description<br>Updated Fig 15 FLL diagram<br>Updated REG0x6A[12:8] |
| 1.4 | Feb 29, 2024 | Updated MICBIAS max ouput current |
| 1.5 | Mar 11, 2025 | Updated Block Diagram<br>Updated Pin Diagram |
| 1.6 | May 12, 2025 | Updated $FS_{ADC}$ Description<br>Updated 3.1 Analog Microphone Input<br>Updated 3.2 Digital Microphone Input |
| 1.7 | May 16, 2025 | Updated Block Diagram |
| 1.8 | Feb 9, 2026 | Updated Chapter 5.2 |
| 1.9 | May 22, 2026 | Updated VDDA pin#21 to VDDC pin#21 |

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**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**

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