NAU8325/NAU83U25
DataSheet

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1 FEATURE

- Low SPK_VDD Quiescent Current
  2.1mA at 3.7V for 2 channels
  3.2mA at 5V for 2 channels
- Gain Setting with 2 wire interface
  22dB to -62dB (plus mute)
- Powerful Stereo Class-D Amplifier
  2ch x 3.0W (4Ω @ 5V, 10% THD+N)
  2ch x 1.32W (4Ω @ 3.7V, 1% THD+N)
  2ch x 1.72W (8Ω @ 5V, 10% THD+N)
  2ch x 0.75W (8Ω @ 3.7V, 1% THD+N)
- Low Output Noise: 18 μV_{RMS} @0dB gain
- 80dB PSRR @217Hz
- Low Current Shutdown Mode
- Click-and Pop Suppression
- Package: QFN-20 / Wettable QFN-20
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications

- Notebooks / Tablet PCs
- Personal Media Players / Portable TVs
- MP3 Players
- Portable Game Players

2 GENERAL DESCRIPTION

NAU8325/NAU83U25 is a stereo high efficiency filter-free Class-D audio amplifier, which is capable of driving a 4Ω load with up to 3.0W output power. This device provides I2C control and I2S audio input with low standby current and fast start-up time.

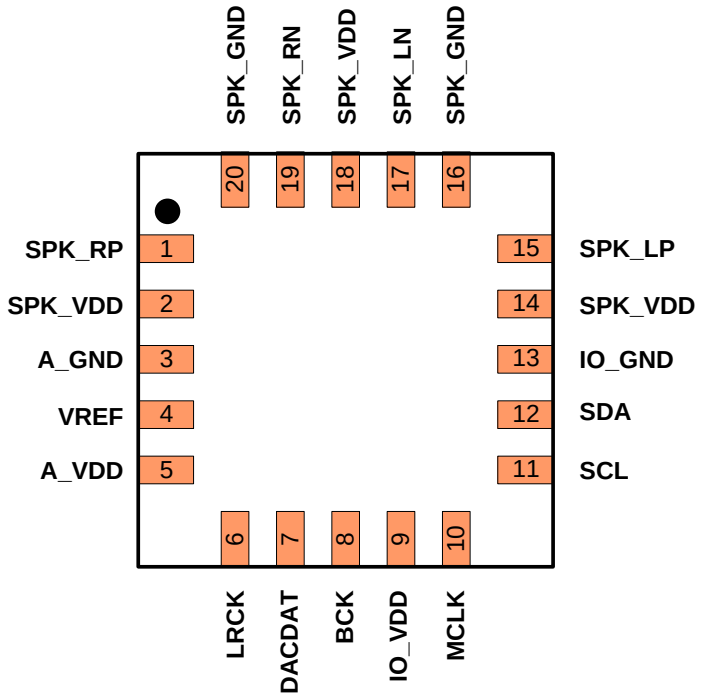
NAU8325/NAU83U25 is ideal for the portable applications of battery drive, as it has advanced features like 80dB PSRR, 90% efficiency, ultra-low quiescent current (i.e. 2.1mA at 3.7V for 2 channels) and superior EMI performance.

NAU8325 is specified for operation from -40℃ ~ +85℃ with QFN-20 / Wettable QFN-20 package.

NAU83U25 is specified for operation from -40℃ ~ +105℃ with QFN-20 package.

NAU83U25 is available for Automotive Grade AEC-Q100 qualification & TS16949 compliant.

3 PART INFORMATION



QFN exposed thermal pad must be connected to A_GND

Figure 1 Pin Configuration of NAU8325/NAU83U25 (TOP VIEW)

Table 1 Pin Descriptions for NAU8325/NAU83U25

Pin #	Name	Type, (Supply Domain)	Description
1	SPK_RP	Analog Output	Right Speaker positive output
2	SPK_VDD	Supply	Supply speaker Driver
3	A_GND	Supply	Ground for Analog
4	VREF	Analog Output	Analog Voltage Reference
5	A_VDD	Supply	Analogue supply
6	LRCK	Digital Input	I2S I/F Frame clock
7	DACDAT	Digital Input	I2S I/F DAC digital audio data
8	BCK	Digital Input	I2S I/F bit clock
9	IO_VDD	Supply	Digital I/F Power supply
10	MCLK	Digital Input	Master clock
11	SCL	Digital I/O	I2C clock
12	SDA	Digital I/O	I2C data
13	IO_GND	Supply	Digital Ground
14	SPK_VDD	Supply	Supply speaker Driver
15	SPK_LP	Analog Output	Left Speaker positive output
16	SPK_GND	Supply	Ground for speaker driver
17	SPK_LN	Analog Output	Left Speaker negative output
18	SPK_VDD	Supply	Supply speaker Driver
19	SPK_RN	Analog Output	Right Speaker negative output
20	SPK_GND	Supply	Ground for speaker driver
21	Ex-Pad	Analog Input	Thermal Tab (must be connected to A_GND)

4 BLOCK DIAGRAM

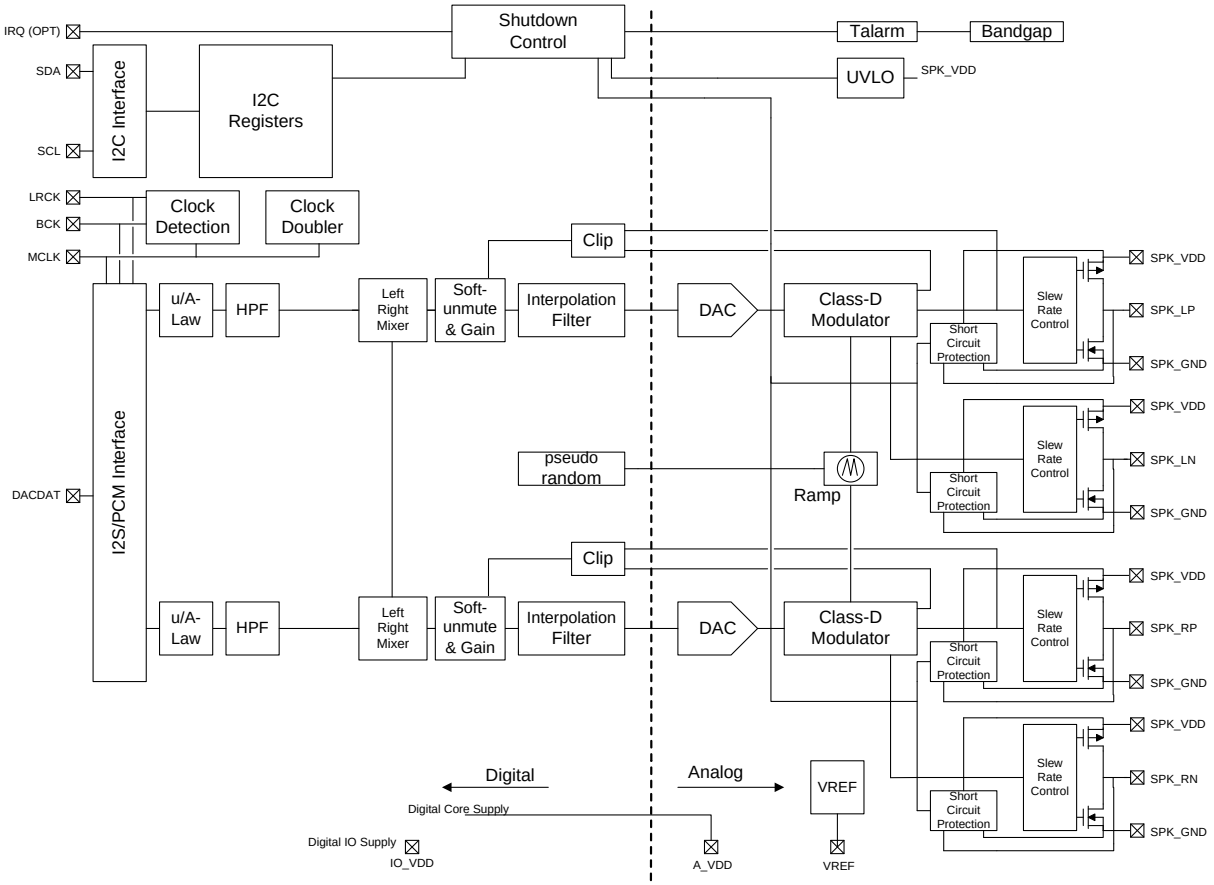


Figure 2 NAU8325/NAU83U25 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
IO_VDD Digital I/O Supply Range	-0.3	4.0	V
SPK_VDD Battery Supply Range	-0.3	6.0	V
A_VDD Analog Supply Range	-0.3	2.2	V
Voltage Input Analog Range	A_GND - 0.3	A_VDD + 0.3	V
Voltage Input I/O Range	IO_GND - 0.3	IO_VDD + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION:

Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

5.2 Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	SPK_VDD	2.50	4.2	5.50	V
Analog Supply Range	A_VDD	1.62	1.8	1.98	V
Digital I/O Supply Range	IO_VDD	1.62	3.0	3.6	V
Ground	A_GND/IO_GND		0		V
Industrial Operating Temperature		-40		+85	°C

CAUTION: The following conditions needed to be followed for regular operation: SPK_VDD > A_VDD -1.2V; IO_VDD > A_VDD – 0.6V.

5.3 Electrical Parameters

Conditions: A_VDD = IO_VDD = 1.8V; SPK_VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, MCLK=12.288MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Shutdown Supply Current	A_VDD, all clocks off	2.0	10	µA
		IO_VDD, all clocks off	0.1	2	
		SPK_VDD, all clocks off	0.2	4	
ISB	Standby Mode Supply Current	A_VDD, clocks off, clock gating on	2.0		µA
		IO_VDD, clocks off, clock gating on	0.1		µA
		SPK_VDD, clocks off, clock gating on	0.2		µA

Symbol	Parameter	Conditions	Typical	Limit	Units
IDD	Operating Mode Supply Current (stereo operation)	A_VDD, idle Channel	3.8		mA
		IO_VDD, idle Channel	0.1		mA
		SPK_VDD, idle Channel	2.8		mA
IDDm	Operating Mode Supply Current (mono operation)	A_VDD, idle Channel	3.0		mA
		IO_VDD, idle Channel	0.1		mA
		SPK_VDD, idle Channel	1.6		mA
Class-D Channel					
P_O	Output Power	SPK_VDD=4.2V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB	0.98		W
		SPK_VDD=5V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=18dB	1.72		W
		SPK_VDD=4.2V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB	1.77		W
		SPK_VDD=5V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB	3.08		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8 Ω + 33 µH, f=1kHz, P_O = 0.5 W, Gain=12dB	0.01		%
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, no Auto Mute or zero detection, no DAC input signal, gain = 0dB	18		µVrms
		A-Weighted, 20Hz-20kHz, no Auto Mute or zero detection, no DAC input signal, gain = 6dB	22		µVrms
PSRR	Power Supply Rejection Ratio (Note 1)	DC, SPK_VDD = 3.2V – 4.2V, amplifier voltage GAIN = 6dB	82		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	82	60	dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	77		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+0.8/-0.3		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 0dB	±1	±5	mV

Symbol	Parameter	Conditions	Typical	Limit	Units
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off, Gain= 6dB	0.03		mVrms
		A-weighted, Idle DAC input, toggling between -120dBFs DAC In & 2048 zero samples, Gain= 6dB	0.03		mVrms
Fsw	Switching Frequency	Average	300	400	kHz
Class-D					
Neff	Power Efficiency	Output Power = 2 x 1W, SPK_VDD = 4.2 V	90		%

***Note 1** : PSRR = 20 x LOG10(GAIN x ΔSPK_VDD/Δ(SPKP-SPKN)) dB*

5.4 Digital I/O Parameters

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	IO_VDD = 1.8V			0.33*IO_VDD	V
		IO_VDD = 3.3V			0.37*IO_VDD	
Input HIGH level	V_{IH}	IO_VDD = 1.8V		0.67*IO_VDD		V
		IO_VDD = 3.3V		0.63*IO_VDD		
Output HIGH level	V_{OH}	I_{Load}= 1mA	IO_VDD=1.8V	0.9*IO_VDD		V
			IO_VDD = 3.3V	0.95*IO_VDD		
Output LOW level	V_{OL}	I_{Load}= 1mA	IO_VDD = 1.8V		0.1*IO_VDD	V
			IO_VDD=3.3V		0.05*IO_VDD	

6 FUNCTIONAL DESCRIPTION

6.1 Inputs

NAU8325/NAU83U25 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. The audio input path is from an I2S/PCM Interface. Additionally, NAU8325/NAU83U25 has a two wire serial interface for control input.

6.2 Outputs

NAU8325/NAU83U25 Stereo Class-D PWM Amplifier has a gain range from 0dB to 22dB and is powered by a separate power supply SPK_VDD, which can go up to 5V. This amplifier is capable of delivering up to 3.0W into a 4Ω load with a 5V supply.

6.3 Digital Interfaces

Command and control of the device is accomplished by using a Serial Control Interface. The simple, but highly flexible, 2-wire Serial Control Interface is compatible with I2C protocol. Audio data is passed to the device through a serial data interface compatible with industry standard I2S and PCM devices.

6.4 Power Supply

This NAU8325/NAU83U25 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. SPK_VDD, A_VDD and IO_VDD can all operate independently of one another. However, the Electrostatic Detection (ESD) protection diodes between the supplies impact the application of the supplies. Because of these diodes, the following conditions need to be met:

$$IO_VDD > A_VDD - 0.6\ V$$

6.5 Power-On-and-Off Reset

NAU8325/NAU83U25 includes a Power-On-and-Off Reset circuit on-chip. The circuit resets the internal logic control at A_VDD supply power-up and this reset function is automatically generated internally when power supplies are too low for reliable operation. Reset threshold is 1.3 V for A_VDD during a power-on ramp and 0.8 V for A_VDD during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held ON while the power levels A_VDD is below the threshold. Once the power level rises above the threshold, the reset is released. Once the reset is released, the registers are ready to be written to.

The preferred power-up sequence is for SPK_VDD and IO_VDD to come up first followed by A_VDD. The preferred power-down sequence is for A_VDD to power down first.

NOTE: It is also important that all the registers should be kept in their reset state for at least 6 µsec.

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates (~3 µsec) and to generate the desired reset period width (~3 µsec at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

For reliable operation, it is recommended to write to register **REG0X00** upon power-up. This will reset all registers to the known default state.

NOTE: When A_VDD is below the power-on reset threshold, the digital IO pins will go to a tri-state condition. IO_VDD is not involved in power-on reset function. It is preferred IO_VDD is available before A_VDD to ensure no glitches occur on SCL/SDA but it is not essential.

6.6 Voltage Reference (VREF)

NAU8325/NAU83U25 includes a mid-supply, reference circuit that produces voltage close to A_VDD/2 that is decoupled to A_GND through the VREF pin by means of an external bypass capacitor. Because VREF is used as a reference voltage for NAU8325/NAU83U25, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7 µF is used. The Reference Voltage circuitry is shown in **Figure 3**.

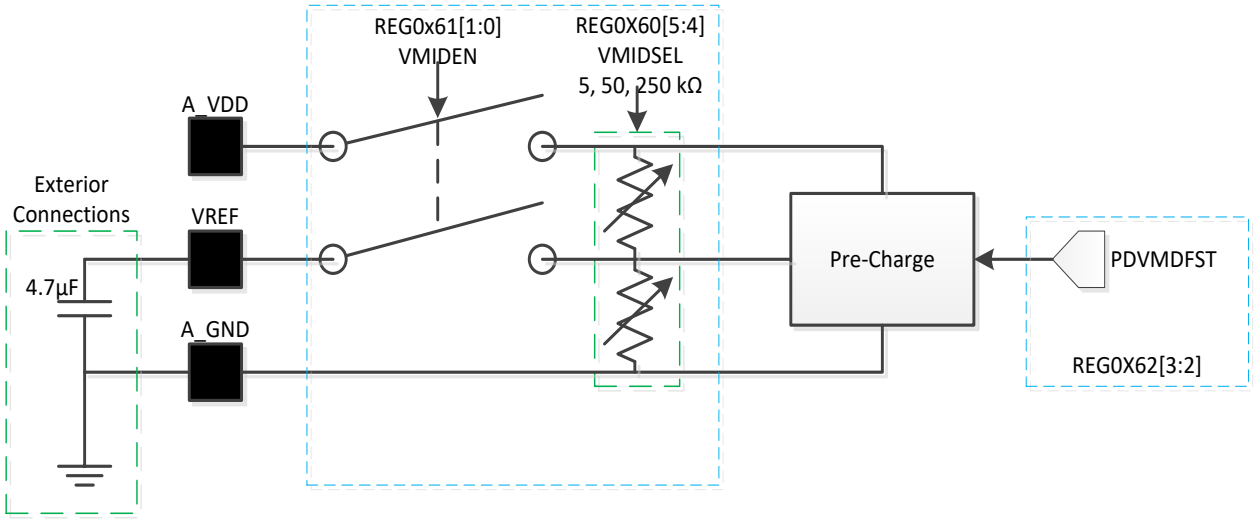


Figure 3 VREF Circuitry

The output impedance can be set using **REG0X60[5:4]**. Refer to **Table 2.**

Table 2 VREF Output Impedance Selection

VMID_SEL REG0X60[5:4]	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50 kOhm	2 5 kOhm
10	250 kOhm	125 kOhm
11	5 kOhm	2.5 kOhm

APPLICATION NOTES:

- Larger capacitances can be used but increase the rise time of VREF and delay the line output signal.
- Due to the high impedance of the VREF pin, it is important to use a low-leakage capacitor.

6.7 DAC Soft Mute

The Soft Mute function ramps down the DAC digital volume to zero when it is enabled by **SMUTE_EN REG0X12[15]**. When disabled, the volume increases to the register-specified volume level for each

channel. This function is beneficial for using the DAC without introducing pop-and-click sounds. When **DACEN_SM REG0X12[13]** is set to '1', the volume will ramp up to the register-specified volume level if the DAC path has been enabled by setting **DACEN REG0X4[3:2**]. The volume goes down to zero directly if the DAC path is disabled.

6.8 Companding

Companding is used in digital communication systems to optimize Signal-to-Noise Ratios (SNR) with reduced data bit rates using non-linear algorithms. NAU8325/NAU83U25 supports the two main telecommunications companding standards -- A-Law and μ-Law -- in both transmit and receive directions. The A-Law algorithm is primarily used in European communication systems; the μ-Law algorithm is primarily used in North American, Japanese, and Australian communications systems.

Companding converts 14 bits (μ-Law) or 13 bits (A-Law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. This option can be enabled for the DAC using the **DACCM0 REG0X0D[15:14]** registers. When the Companding Mode is enabled, **CMB8_0 REG0X0D[10]** must be enabled for 8-bit operation. This will disable the word length selection in **WLEN0 REG0X0D[3:2]** for this port and allow the companding functions to use an 8-bit word length.

The compression equations set by the ITU-T G.711 Standard and implemented in NAU8325/NAU83U25 Amplifier are provided here for reference:

μ-Law

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

A-Law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \qquad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|)}{(1 + \ln(A))}, \qquad \frac{1}{A} \leq x \leq 1$$

$$A = 87.6$$

6.9 Hardware and Software Reset

NAU8325/NAU83U25 and all of its control registers can be reset to initial default power-up conditions by writing any value to **REG0X00** ***once*** using the control interface. Writing to any other valid register address terminates the reset condition, but all registers will be set to their power-on default values. This is typically done during hardware reset.

NAU8325/NAU83U25 can be reset to initialized power-up conditions by writing any value to **REG0X01** ***twice*** using the control interface. Writing to **REG0X01** will reset NAU8325/NAU83U25, but all registers values will be unaffected. This is typically done during operation to quickly force NAU8325/NAU83U25 in the known initialized startup state.

6.10 Clocking and Sample Rates

The internal clocks for NAU8325/NAU83U25 are derived from a common internal clock source. This master system clock can set directly by the MCLK input or it can be generated from a clock multiplier using the MCLK as a reference.

The following sections illustrate how the various register settings can be used to adjust/select the MCLK_SRC and DAC_CLK clock frequencies.

6.10.1 Clock Control and Detection

NAU8325/NAU83U25 includes a Clock Detection circuit that can be used to enable and disable the audio paths, based on an initialized audio path setting. Enable the audio path through the I2C Interface; but, the actual power up/down can be gated by the clock detection circuit. The block diagram of the clock detection circuit is shown in **Figure 4**.

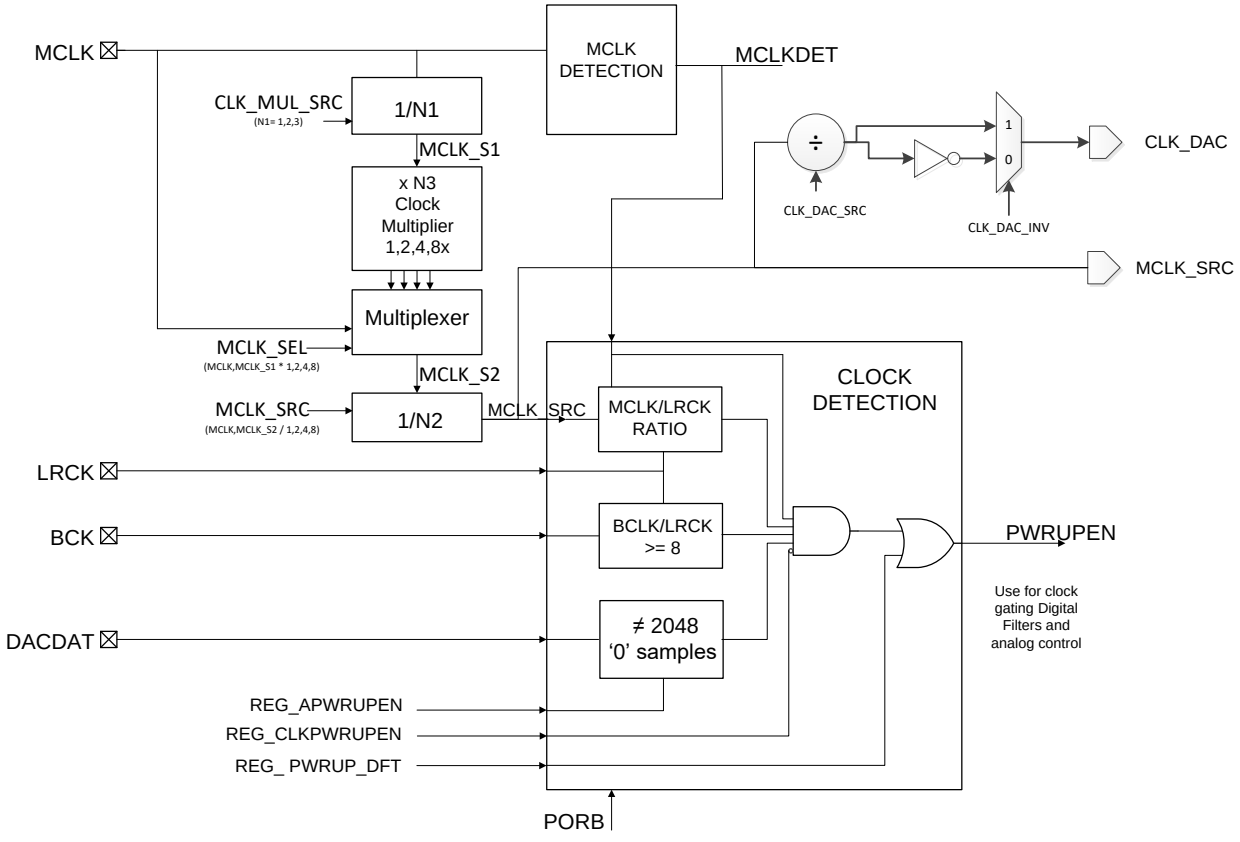


Figure 4 NAU8325/NAU83U25 Clock Detection Circuit

Clock Detection by NAU8325/NAU83U25 uses the MCLK, BCK, LRCK and DACDAT to control the PWRUPEN signal and set the clock divider ratios.

6.10.2 Automatic Power Control and Mute

Clock detection and automatic power control in NAU8325/NAU83U25 is enabled by setting **REG_CLKPWRUPEN** = 0 (default) and meeting three or four conditions, depending on the configuration. If all conditions are met, the PWRUPEN signal will be asserted to 1. If any of the conditions are not met, the PWRUPEN signal is set to 0.

The conditions for generating the PWRUPEN signal are:

1) NAU8325/NAU83U25 has custom logic clock detection circuits that detect if MCLK is present. Upon MCLK detection, the detector output MCLKDET goes to 1. When the MCLK disappears, MCLKDET goes back to 0. Up to 1 µsec is required to detect MCLK and the MCLK release time is about 50 µsec.
2) The clock detection logic also needs to detect the ratio MCLK_SRC/LRCK of 256, 400 or 500.
3) The clock detection logic also needs to detect the BCLK to make sure data is present. There needs to be at least 8 BCLK cycles per Frame Sync.
4) If REG_APWRUPEN is set to '1', the clock detection will require non-zero samples on any channel in order to enable the output power up signal. Any non-zero sample will be sufficient. After power up if 2048 zero samples are detected on both channels the PWRUPEN signal is asserted to '0'. If REG_APWRUPEN is set to '0', this function does not control the PWRUPEN signal.

The PWRUPEN signal is capable of controlling all the analog power consuming blocks such as the Class D driver, the VMID block, the DAC and bias generation. The register **ANALOG_CONTROL_1** determines which blocks are controlled by PWRUPEN.

When PWRUPEN goes high an internal sequence is triggered to bring up analog functions. This includes an analog MUTE to allow stabilization of internal analog blocks, followed by a soft unmute of the DAC. The analog MUTE time is determined by **REG_MUTE_CTRL.ANA_MUTE** and is between 430us and 4ms. The soft mute ramps the gain on the DAC input from MUTE to DAC_VOLUME at a rate determined by **REG_MUTE_CTRL.UNMUTE_CTL**. This register can disable the soft unmute, or ramp the gain at 32 or 512 MCLK_SRC periods per gain step. For the 512 setting, the soft unmute takes 256 * 512 * Tmclk seconds to reach 0dB (10ms for 12.288MHz MCLK_SRC). This ensures pop free startup of the amplifier. An example of this startup is shown in figure below.

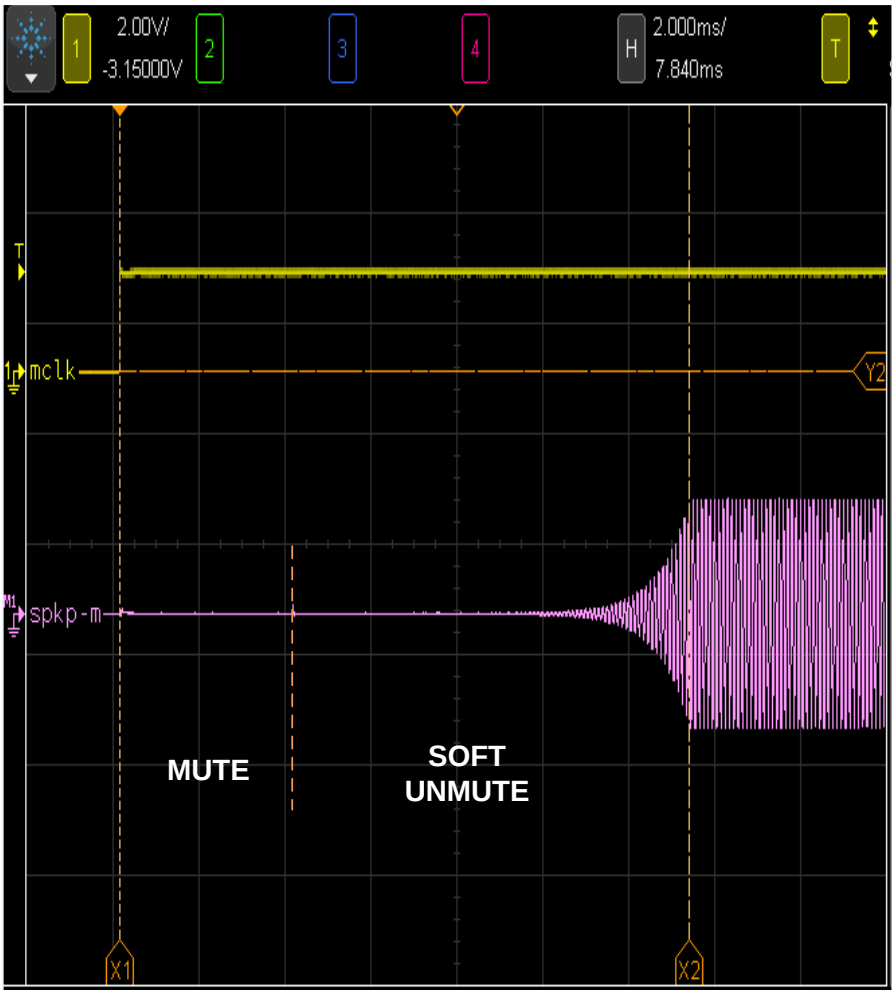


Figure 5 PWRUPEN startup sequence

Before reaching the DAC the incoming PCM signal is processed by a digital signal path. To ensure complete flushing and transient free audio of this path it is recommended that 2048 zero samples are sent to the device before stopping clocks. The DAC soft mute function is also beneficial for eliminating any audio transients from audio path.

The preferred operating scenario is as follows:

1) Initialize I2C registers at power up;
2) Start clocks.
3) Send 1-14ms of zero samples (optional)
4) Play sound.
5) Send 2048 zero samples at the end of a sound file to prevent transients.
6) Stop the clocks.
7) Repeat 2) onwards when required.

In addition to power up control there is an AUTO_MUTE feature. If **REG_MUTE_CTRL.AUTO_MUTE** is set, then when 2048 zero samples are detected the PWM driver is MUTED. Upon reception of further data, the driver is UNMUTED immediately. This mode has no delay apart from the group delay of audio signal path, but also does not have the same power saving benefits as the automatic power control feature described above.

6.10.3 Disabling Clock Detection

Clock detection in NAU8325/NAU83U25 is disabled by setting **REG_CLKPWRUPEN** to 1. In this state, PWRUPEN is no longer controlled by the enabling conditions listed above, but is set to 1. However, the MCLKDET and clock dividers are still active.

Table 3 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	96
Master Clock MCLK (MHz)	2.048	24.576

6.10.4 Sample and Over Sampling Rates

Possible Sample Rate and MCLK_SRC selections are shown in **Table 4** and **Table 5**. Note that **REG_SRATE REG 0X40** must be programmed to identify the target sample rate.

Table 4 Sampling and Over Sampling Rates (Ranges 1-3)

REG_SRATE												
MCLK_SRC/FS Ratio	Range 1 000				Range 2 001				Range 3 010			
	FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)		FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
256	8	12	2.048	3.072	16	24	4.096	6.144	32	48	8.192	12.288
400	8	12	3.2	4.8	16	24	6.4	9.6	32	48	12.8	19.2
500	8	12	4	6	16	24	8	12	32	48	16	24

Table 5 Sampling and Over Sampling Rates (Range 4)

REG_SRATE				
MCLK_SRC/FS Ratio	Range 4 011			
	FS (kHz)		MCLK_SRC (MHz)	
	Min	Max	Min	Max
256	64	96	16,384	24,576
400	64	96	25.6	38.4
500	64	96	32	48

The MCLK_SRC frequency is defined as:

F_MCLK_SRC = F_MCLK / N2 when MCLK_SEL = 0

F_MCLK_SRC = N3 x F_MCLK / (N1 x N2) when MCLK_SEL ≠ 0

Where N1 & N2 are selectable to 1, 2, 3, 4, 5, 6 or 7 and N3 is selectable to 1, 2, 4 & 8.

The only internal MCLK_SRC/FS ratios allowed are: 256, 400 & 500. The clock divider or multiplier in register 0x03 needs to be setup to achieve one these three possible ratios.

Given N1=N2=1, effective MCLK/FS ratios can be achieved with the clock multiplier, as shown in **Table 6**.

Table 6 Effective MCLK/FS Ratios

MCLK_SRC/FS ratio	Clock Multiplier (MCLK_SEL REG0x03)	Effective ratio MCLK/FS
256	8	32
400	8	50
500	8	62.5
256	4	64
400	4	100
500	4	125
256	2	128
400	2	200
500	2	250
256	1	256
400	1	400
500	1	500

For MCLK_SRC/FS ratios of 256 the Over Sampling Ratio (OSR) can be set in register 0x29 to: 32, 64, 128 & 256. Note that the DAC clock needs to be set to the matching values in register 0x03 CLK_DAC_SRC.

For MCLK_SRC/FS ratios of 400 & 500 the Over Sampling Ratio (OSR) is fixed to 100. For MCLK_SRC/FS ratios of 400 the DAC clock divider needs to be set to ¼ in register 0x03. For MCLK_SRC/FS ratios of 500 the DAC clock divider is automatically set to 1/5.

For example if MCLK is provided as 256* Fs, then N2=1 and MCLK_SEL = 0 will set MCLK_SRC as the correct 256*Fs. If MCLK proved is 512*Fs, then N2=2 and MCLK_SEL = 0 will set MCLK_SRC as the correct 256*Fs.

In addition to MCLK_SRC, the clock to the DAC must be configured correctly. For MCLK_SRC/FS ratios of 256 the Over Sampling Ratio (OSR) can be set via DAC_RATE in register REG29 to: 32, 64, 128 & 256. The DAC clocks need to be set to its corresponding value in register 0x03 given by:

F_DAC_CLK = F_MCLK_SRC * CLK_DAC_SRC

And

F_DAC_CLK = DAC_RATE * Fs

CLK_DAC_SRC is 1, ½, ¼, ⅛ and is set to match the desired sample rate Fs and the DAC oversampling setting DAC_RATE in REG29.

.

For MCLK_SRC/FS ratios of 400 & 500 the Over Sampling Ratio (OSR) is fixed to 100. For MCLK_SRC/FS ratios of 400 the DAC clock divider needs to be set to ¼ in register 0x03. For MCLK_SRC/FS ratios of 500 the ADC & DAC clock dividers are automatically set to 1/5.

6.11 Automatic Level Control

The digital Automatic Level Control (ALC) function supports the DAC digital audio path of NAU8325/NAU83U25. This can be used to manage the gain to optimize the signal level at the output of the Class-D Amplifier by automatically amplifying input signals that are too small or automatically decreasing the amplitude signals that are too loud. **Figure 6** illustrates the relationship of the ALC to other major functions of NAU8325/NAU83U25.

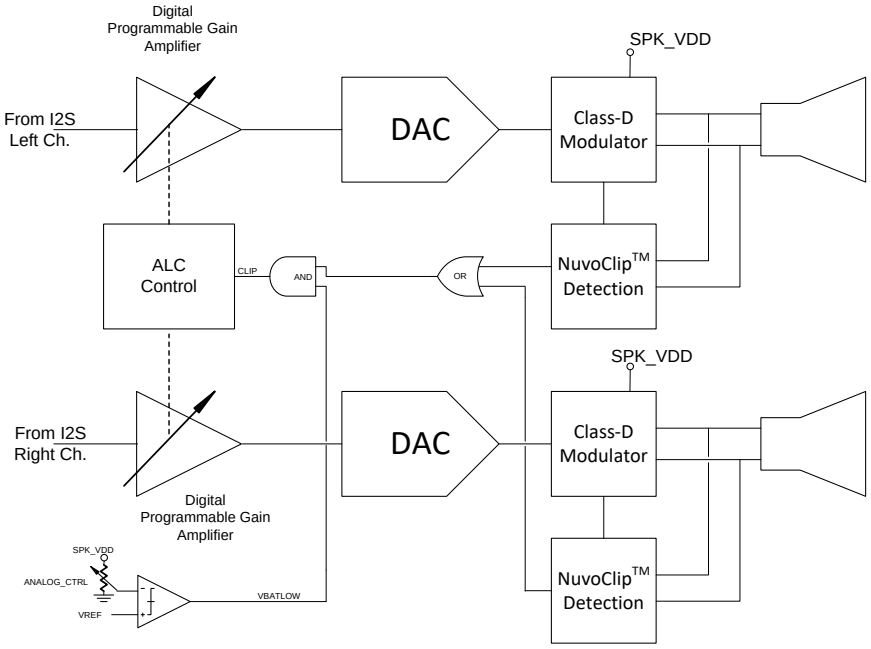


Figure 6 Automatic Level Control

6.11.1 ALC Operation

The DAC digital audio path of NAU8325/NAU83U25 is supported by a digital Automatic Level Control (ALC) function. The ALC can perform as a peak limiter as the ALC can automatically reduce the output level when the output is clipping. Clipping can occur at high output levels when the speaker supply voltage drops due to a battery having a low charge or IR drops between supply and NAU8325/NAU83U25. Each channel (Left and Right) has a dedicated clip detection circuit. The clip detection signals of both channels are combined (OR) and gated (AND) by a low battery indicator before

it is fed into the ALC. The ALC controls both the left and right channel gain simultaneously in order to keep the stereo balance.

A clip detection signal is provided by the clip detection circuit as soon as the input signal is clipping at its peak levels. The ALC block then ramps down the gain at the pre-programmed ALC Attack Time rate. This continues until the clipping detection no longer detects a clipping signal or until the maximum gain decrement per clipping event is reached. When the clipping is no longer occurring, the ALC gain is held for the hold time. The ALC gain is then ramped up to the target following the pre-programmed ALC Release Time rate.

6.11.2 ALC Parameter Definitions

ALC Maximum Gain (ALCMAX): This sets the maximum allowed gain during all modes of ALC operation. This is applied to be the upper limit of the desired range for a given application scenario.

ALC Minimum Gain (ALCMIN): This sets the minimum allowed gain during all modes of ALC operation. This is applied to be the bottom limit of the desired range for a given application scenario.

ALC Attack Time (ALCATK): Attack time refers to how quickly a system responds to a clipping event. Typically, attack time is much faster than decay time.

ALC Decay Time (ALCDCY): Decay time refers to how quickly a system responds after the hold time. Typically, decay time is much slower than attack time. When no more clipping events occur, the gain will increase at a rate determined by this parameter.

ALC Hold Time (ALCHLD): Hold time refers to the duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In NAU8325/NAU83U25, the hold time value is the duration from the last clipping event before there is an actual gain increase during the decay time.

CLIP_GAINADJUST sets the maximum gain decrease per clipping event. During a clipping even the gain decreases by 0.250dB (1-1/64) per attack time step until the clipping event no longer occurs or the maximum gain reduction limit set in CLIP_GAINADJUST has been reached or the ALC Minimum Gain is reached.

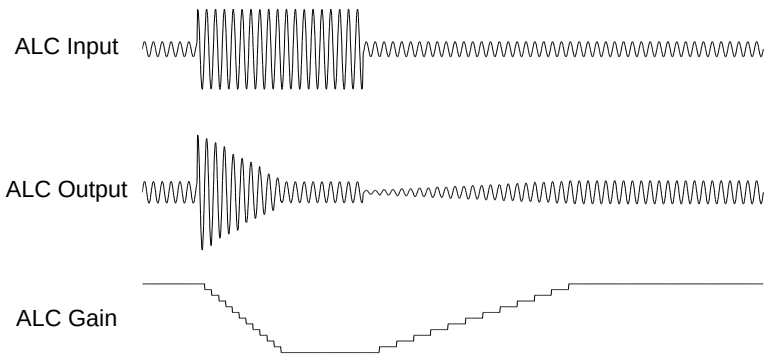


Figure 7 ALC Operation

The waveform below shows the operation of the ALC hold delay time.

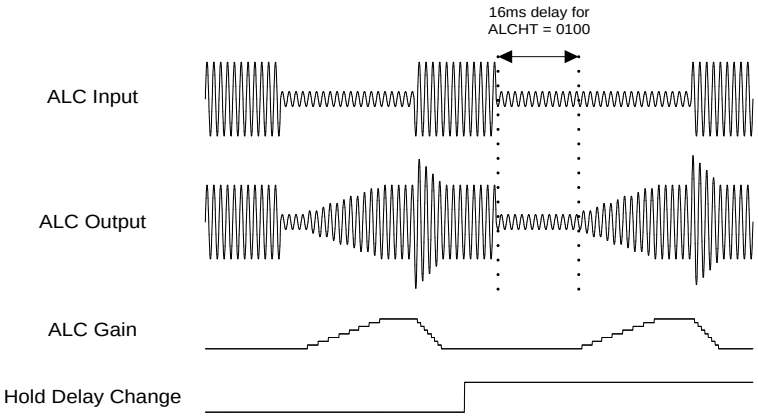


Figure 8 ALC using Hold time

6.12 Device Protection

NAU8325/NAU83U25 includes the following types of device protection:

- Over Current Protection (OCP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in NAU8325/NAU83U25. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 14µs, the output drivers will be disabled for 100ms. The output drivers will then be re-enabled and checked for a short circuit again. If the short circuit is still present for another 14µs, the cycle will repeat until the short circuit has been fixed. The short circuit threshold is set at 2.1A.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in NAU8325/NAU83U25 If the SPK_VDD drops under 2.1V, the output drivers are disabled, however, NAU8325/NAU83U25 control circuitry will still operate. This is useful to help avoid the battery supply voltage dropping before the host processor can safely shutdown the devices on the system. If the SPK_VDD drops below 1.4V, the internal power-on-reset will activate and put the class-D driver in power down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the device internal junction temperature reaches 130°C, NAU8325/NAU83U25 will disable the output drivers. Once the device cools down to a safe operating temperature (115°C) for at least 100us, the output drivers will be re-enabled.

Clock Termination Protection (CTP) is provided in NAU8325/NAU83U25. If the clock stops running, NAU8325/NAU83U25 automatically shuts down the Class-D driver if Clock Detection is enabled.

6.13 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by initializing the registers and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize ‘pops’ on the speaker output. The complete power-up sequence requires about 14 msec. The device will power down in about 30 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize ‘pops’ when the clocks are stopped.

6.14 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 10 µF and 0.1 µF are sufficient to achieve good performance.

6.15 Filters

NAU8325/NAU83U25 is designed for use without any filter on the output line. However, NAU8325/NAU83U25 may be used with or without various types of filters, depending on the needs of the application.

6.15.1 Class D without Filters

NAU8325/NAU83U25 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 9** illustrates this simple configuration.

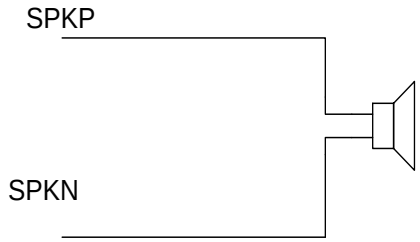


Figure 9 NAU8325/NAU83U25 Speaker Connections without Filter

6.15.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown **Figure 10**.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

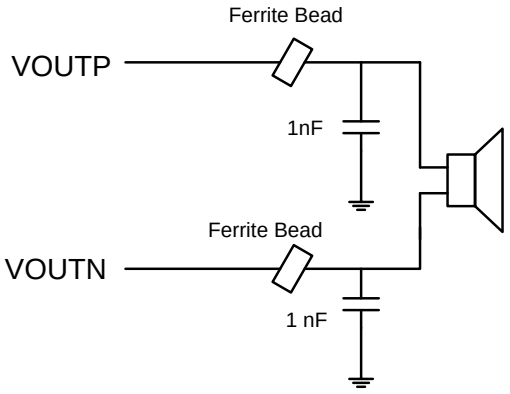


Figure 10 NAU8325/NAU83U25 Speaker Connections with Ferrite Bead Filters

LC Filters are used to suppress low-frequency emissions. The diagram in **Figure 11** shows NAU8325/NAU83U25 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

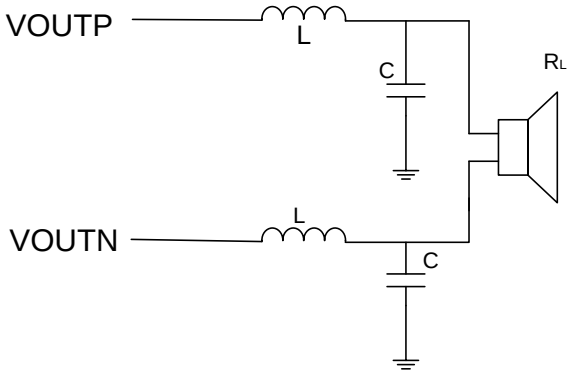


Figure 11 NAU8325/NAU83U25 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 12** shows the speaker connections using standard Low-Pass LCR Filters.

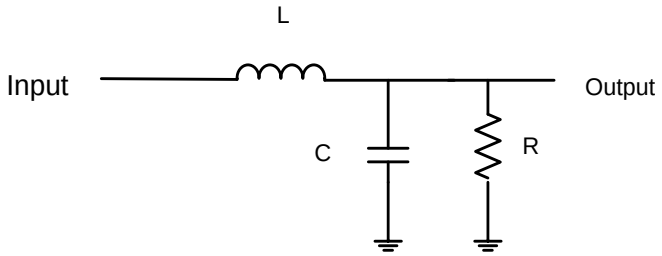


Figure 12 NAU8325/NAU83U25 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped (ζ = 0.707) standard Low-Pass LCR Filters:

$2\pi fc = \frac{1}{\sqrt{(LC)}}$ fc is the cut-off frequency

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting RL = 2R.

High-Pass Filters may also be useful in some applications. There is a High-Pass Filter for each DAC Channel. The High-Pass Filters may be enabled by setting **DAC_HPF_EN REG0X11[15].** The High-Pass Filter has two operation modes that apply to both channels simultaneously. In the Audio Mode, the filter is a simple first-order DC blocking filter, with a cut-off frequency of 3.7 Hz. In the Application-Specific Mode, the filter is a second-order audio frequency filter, with a programmable cut-off frequency. The programmable filter mode may be enabled by setting **DAC_HPF_APP REG0X11[14].**

Table 7 identifies the cut-off frequencies with different sample rates.

Table 7 High-Pass Filter Cut-Off Frequencies

HPFCUT	Sample Rate in KHz (FS)							
	REG_SRATE= 3'b000		REG_SRATE= 3'b001		REG_SRATE= 3'b010		REG_SRATE= 3'b011	
	8	12	16	24	32	48	64	96
000	87	130	87	130	87	130	87	130
001	103	155	103	155	103	155	103	155
010	132	198	132	198	132	198	132	198
011	165	248	165	248	165	248	165	248
100	207	311	207	311	207	311	207	311
101	265	398	265	398	265	398	265	398
110	335	503	335	503	335	503	335	503
111	409	614	409	614	409	614	409	614

6.16 Digital Control

NAU8325/NAU83U25 includes an I2C Control Interface as well as an I2S/PCM Audio Interface. The following sections describe the Control and Audio Interfaces and registers.

6.16.1 Digital Control Interface

NAU8325/NAU83U25 uses a 2-wire I2C Interface for command and control. The I2C Slave address is 0x21.

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). NAU8325/NAU83U25 can functions only as a slave device on the 2-wire interface.

6.16.1.1 2-Wire Protocol Convention

To initiate communication, all 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDA while SCL is HIGH.

Following a START condition, the master must output a device address byte consisting of a 7-bit device address, and a Read/Write control bit in the LSB of the address byte. To read from the slave device,

the R/W bit must be set to 1. To initiate a write to the slave device, the R/W bit must be 0. If the device address matches the address of a slave device, the slave will output an acknowledgement bit.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDA bus after transmitting eight bits and during the ninth clock cycle, the receiver (slave) pulls the SDA line LOW to acknowledge the reception of the eight bits of data.

To terminate a read/write session, all 2-Wire interface operations must end with a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

Application Notes:

- NAU8325/NAU83U25 is permanently programmed with 0x21 “0100001” as the Device Address.

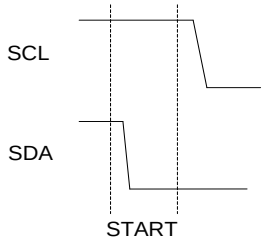


Figure 13 Valid START Condition

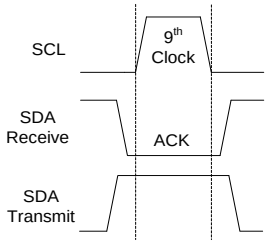


Figure 14 Valid Acknowledge

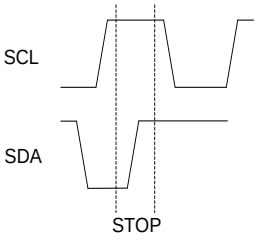


Figure 15 Valid STOP Condition

6.16.1.2 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more data bytes as seen in Figure 16. These instructions consist of the Address byte and two Control Address bytes that precede the START condition and are followed by the STOP condition. Figure 17 shows the data bus and the corresponding clock cycles.

0	1	0	0	0	0	1	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Byte
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Byte
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 16 Slave Address Byte, Control Address Byte, and Data Byte

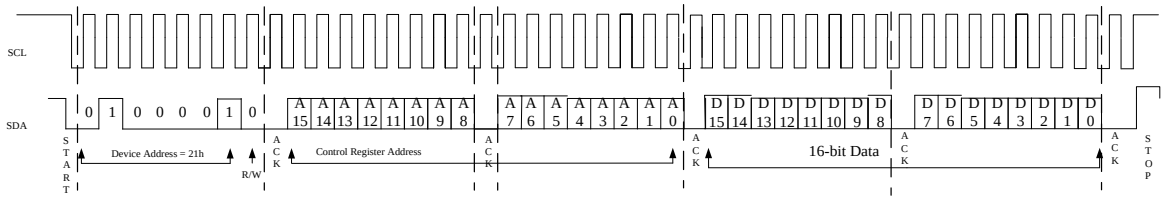


Figure 17 2-Wire Write Sequence

6.16.1.3 2-Wire Read Operation

A Read operation consists of the three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, Device Address byte with the R/W bit set to "0", and a Control Register Address byte. This indicates to NAU8325/NAU83U25 which of its control registers is going to be accessed.

After this, NAU8325/NAU83U25 will respond with an ACK as it accepts the Control Register Address that the master is transmitting to it. After the Control Register Address has been sent, the master will send a second START condition and Device address but with R/W = 1.

After NAU8325/NAU83U25 recognizes its Device Address the second time, it will transmit an ACK followed by a two byte value containing the 16 bits of data in NAU8325/NAU83U25 control registers requested by the master. During this phase, the master generates an ACK with each byte of data transferred.

After the two bytes have been transmitted, the master will send a STOP condition ending the read phase. If no STOP condition is received, NAU8325/NAU83U25 will automatically increment the target Control Register Address and then start sending the two bytes of data for the next register in the sequence. This will continue as long as the master continues to send ACK signals. Once the target register reaches 0xFFFF, it will send the associated data then roll over to 0x0000 and continue as before.

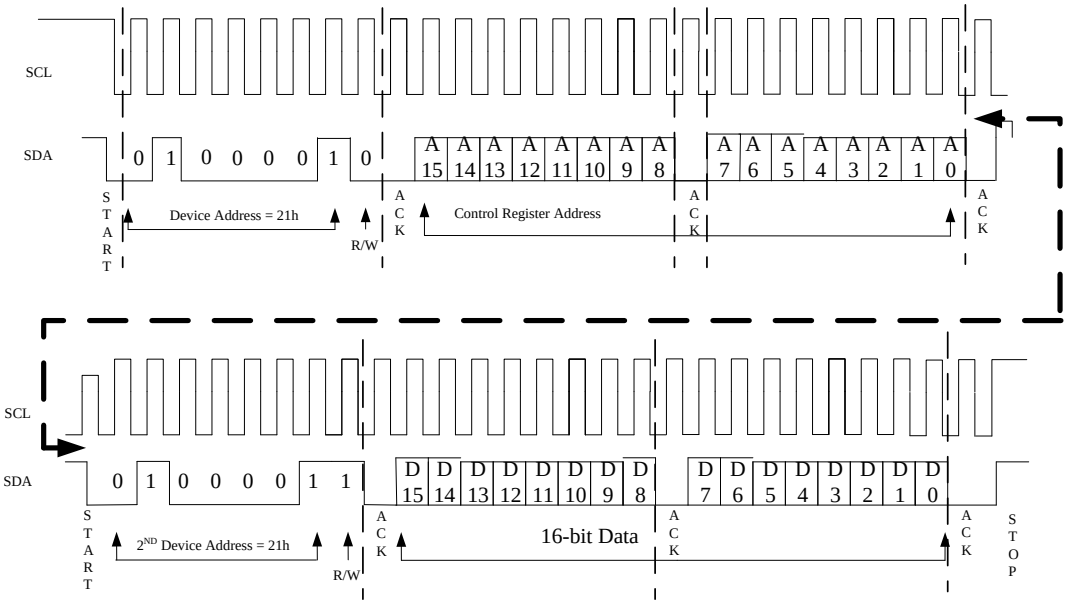


Figure 18 2-Wire Read Sequence

6.16.2 Digital Audio Interface

NAU8325/NAU83U25 is an I2S slave device. In Slave Mode, an external controller supplies BCK (bit clock) and LRCK (the frame synchronization or FS signal). Data is latched on the rising edge of BCK.

NAU8325/NAU83U25 has two DAC channels.

NAU8325/NAU83U25 supports five port data lengths: 8, 16, 20, 24, and 32 bits by setting **REG0XD[4:2]** The chip also supports 8-bit word length for Companding Mode operation by setting **REG0XD** to 1.

NAU8325/NAU83U25 supports audio formats: I2S, Right Justified, Left Justified, TDM I2S, TDM Left Justified, PCM A, PCM B, PCM Offset, and PCM Time Slot.

When operated in the TDM I2S or TDM Left Justified mode and in all PCM modes, NAU8325/NAU83U25 supports 8-channel data transmission on DAC path simultaneously. **REG0XC[15]** should be set = 1 if using TDM I2S or TDM Left Justified modes.

PCM Mode	REG0XD[1:0]	REG0XD[6]	REG0XE[10]	REG0XC[14]
Right Justified	00	0	0	0
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Offset	11	Don’t care	0	1
PCM Time Slot	11	Don’t care	1	0

Table 8 Digital Audio Interface Mode Settings

6.16.2.1 Right-Justified Audio Data

In Right-Justified Mode, the LSB is clocked on the last BCLK rising edge before the FS transitions. When FS is HIGH, Channel 0 data is transmitted; when FS is LOW, Channel 1 data is transmitted. This can be seen in **Figure 19**.

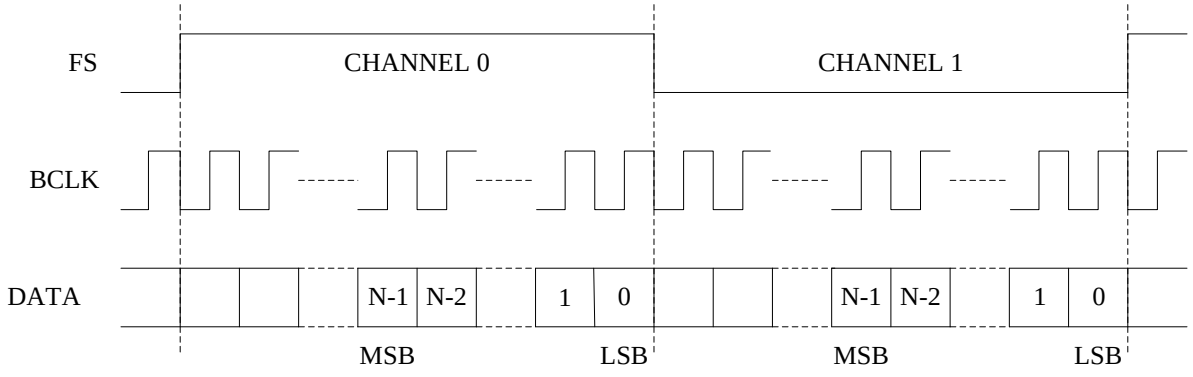


Figure 19 Right-Justified Audio Data

6.16.2.2 Left-Justified Audio Data

In Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is HIGH, Channel 0 data is transmitted; when FS is LOW, Channel 1 data is transmitted. This can be seen in **Figure 20**.

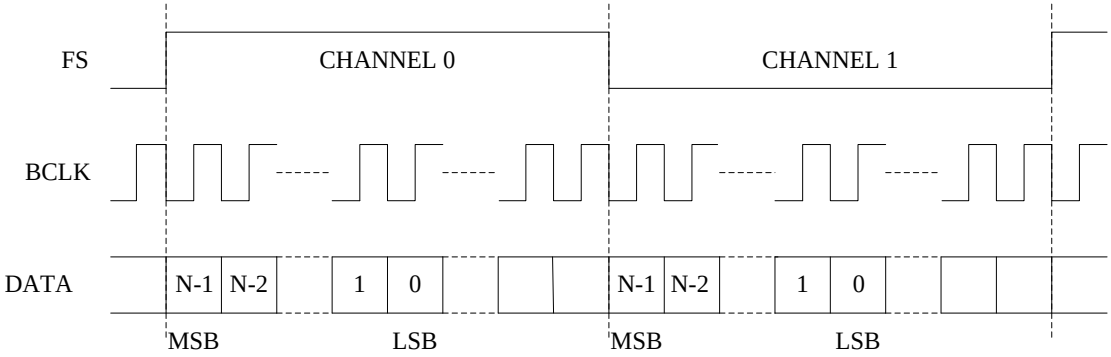


Figure 20 Left-Justified Audio Data

6.16.2.3 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data is transmitted; when FS is HIGH, Right Channel data is transmitted. This can be seen in **Figure 21.**

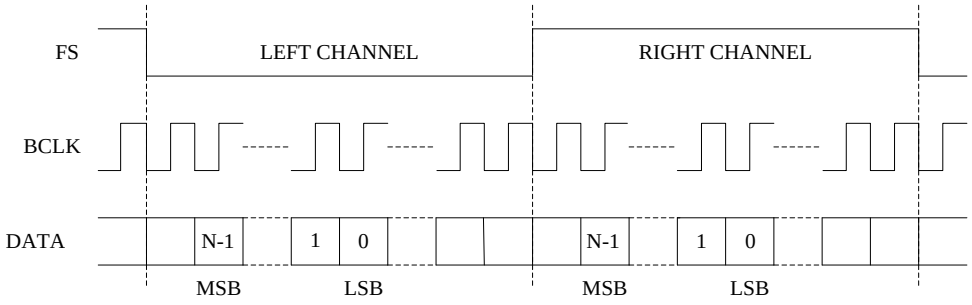


Figure 21 I2S Audio Data

6.16.2.4 TDM Left-Justified Audio Data

In TDM Left-Justified Mode, the MSB is clocked on the first BCLK rising edge after the FS transitions. When FS is LOW, Channel 1 data is transmitted, then Channel 3, 5, and 7 data are transmitted; when FS is HIGH, Channel 0 data is transmitted, then Channel 2, 4, and 6 data are transmitted. This is shown in **Figure 22**.

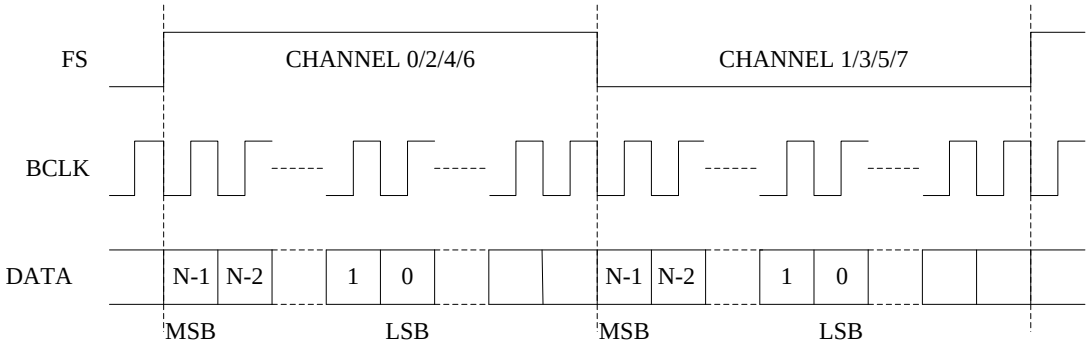


Figure 22 TDM Left-Justified Audio Data

6.16.2.5 TDM I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Channel 0 data is transmitted, then Channel 2, 4, and 6 data are transmitted; when FS is HIGH, Channel 1 data is transmitted, then Channel 3, 5, and 7 data are transmitted. This is shown in **Figure 23.**

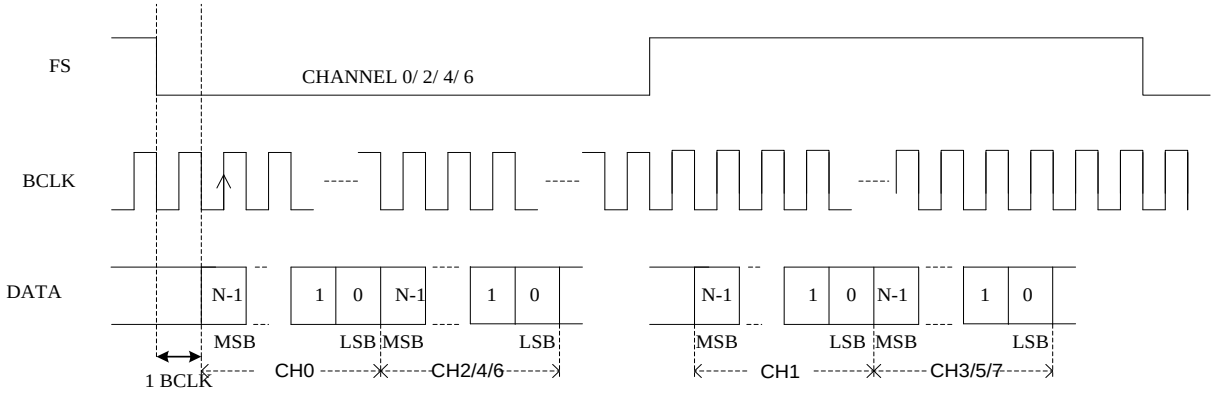


Figure 23 TDM I2S Audio Data

6.16.2.6 PCM A Audio Data

In PCM A Mode, Channel 0 data is transmitted first, followed sequentially by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in **Figure 24.**

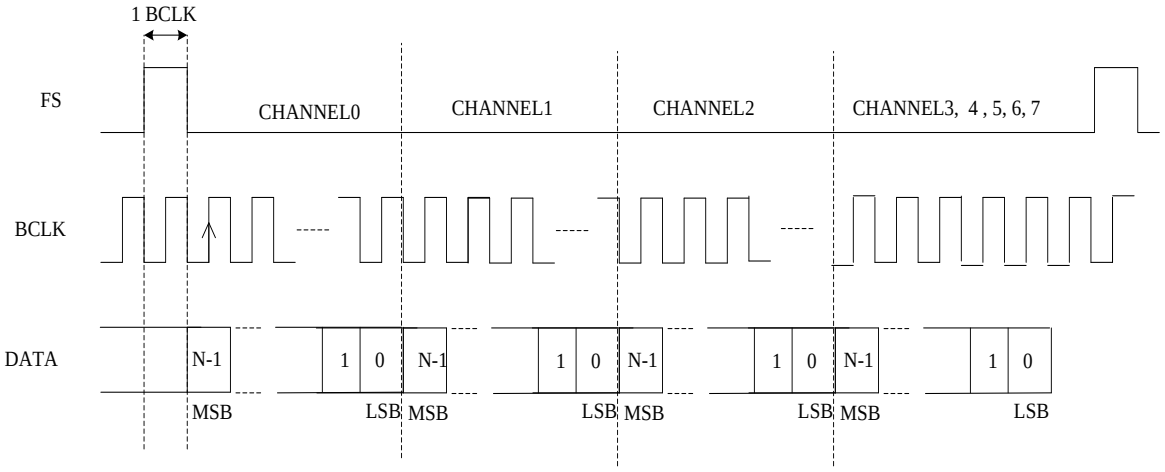


Figure 24 PCM A Audio Data

6.16.2.7 PCM B Audio Data

In PCM B Mode, Channel 0 data is transmitted first, followed immediately by Channel 1, 2, and 3, 4, 5, 6, and 7 data immediately after. The Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the Channel 1 MSB is clocked on the next BCLK after the Channel 0 LSB. This is shown in **Figure 25**.

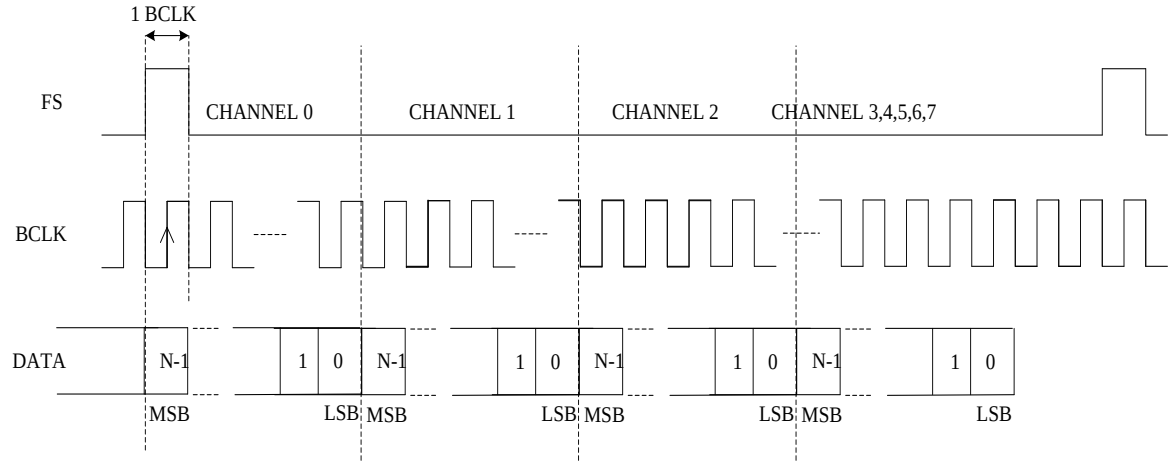


Figure 25 PCM B Audio Data

6.16.2.8 PCM Time Slot Audio Data

PCM Time Slot Mode is used to delay the time at which the DAC data is clocked into the device. This can be useful when multiple NAU8325/NAU83U25 chips or other devices share the same audio bus. This will allow the audio from the chips to be delayed around each other without interference.

Normally, the DAC data is clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed by setting **REG0XF[9:0]** and **REG0X10[9:0]** for the left and right

channels, respectively. **REG0XE[10**] needs to be set to 1. These delays can be seen before the MSB in **Figure 26**.

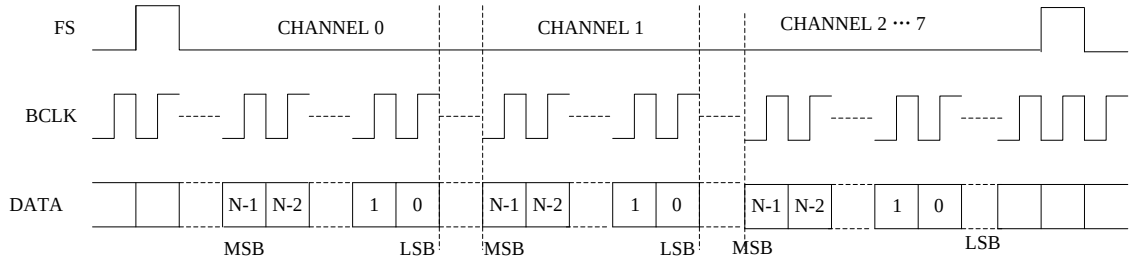


Figure 26 PCM Time Slot Audio Data

6.16.2.9 PCM Time Offset Audio Data

PCM Time Offset Mode is used to delay the time at which the DAC data are clocked. This increases the flexibility of NAU8325/NAU83U25 for use in a wide range of system designs. One key application of this feature is to enable multiple NAU8325/NAU83U25 chips or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. **REG0x0C[14]** must be set to 1 for this application.

Normally, the DAC data is clocked immediately after the Frame Sync (FS). In this mode, audio data is delayed by a delay count specified in the device control registers. The Channel 0 MSB is clocked on the BCLK rising edge defined by the delay count set in **REG0x0F[9:0]**. The subsequent channel's MSB is clocked on the next BCLK after the LSB of the previous channel. This can be seen in **Figure 27**.

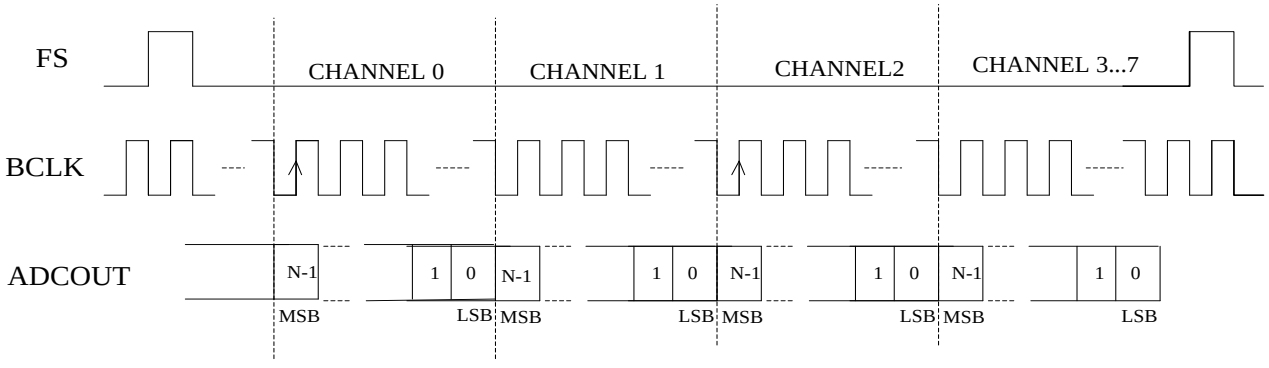


Figure 27 PCM Time Offset Audio Data

Table 9 Digital Audio Interface Timing Parameter

Symbol	Description	Min	Typ	Max	Unit
T_{BCK}	BCLK Cycle Time (Slave Mode)	35	---	---	ns
T_{BCKH}	BCLK High Pulse Width (Slave Mode)	20	---	---	ns
T_{BCKL}	BCLK Low Pulse Width (Slave Mode)	50	---	---	ns
T_{FSS}	Fs to CLK Rising Edge Setup Time (Slave Mode)	20	---	---	ns
T_{FSH}	BCLK Rising Edge to Fs Hold Time (Slave Mode)	40	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	TBD	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	TBD	ns
T_{DIS}	ADCIN to BCLK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	BCLK Rising Edge to DACIN Hold Time	15	---	---	ns
T_{DOD}	Delay Time from SCLK Falling Edge to ADCOUT (Master Mode)	---	---	20	ns
	Delay Time from SCLK Falling Edge to ADCOUT (Slave Mode)	---	---	30	ns

BCLK=3.072MHz, Fs=48KHz, 64Bit, VDD 2.5 -5.25V, Room Temperature

6.17 Control and Status Registers

#	Function	NAME	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0	HARDWARE_RST	RESET_N1																	**Hardware Reset** (Write any value ***once*** to reset all the registers.)
1	SOFTWARE_RST	RESET_N_SOFT_PRE																	**Software Reset** (Write any value ***twice*** to reset all internal states without resetting the config registers.)
2	DEVICE_ID	I2C_DEVICE_ID																	**I2C Slave Address**
		REG_SI_REV																	**Silicon Revision**
		DEFAULT	0	0	1	0	0	0	0	1	1	1	1	1	0	0	1	0	**0x21F2**
3	CLK_CTRL	CLK_DAC_ INV																	**DAC Clock Inversion In Analog Domain Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_ SRC																	**DAC Clock From CODEC_SRC Scaling Divider Select** 00 = 1 (DEFAULT) 01 = 1/2 10 = 1/4 11 = 1/8
		CLK_MUL_SRC (N1)																	**Internal Clock Multiplier Reference Clock Select** (Input: MCLK input pin; output: MCLK_S1) 00 = MCLK input pin (DEFAULT) 01 = MCLK input pin/2 10 = MCLK input pin/3 11 = Off
		MCLK_SEL (N3)																	**Clock Multiplier Outputs Clock Select** (Output: MCLK_S2 Requires Reg 0x65 to be set to enable 4x & 8x multipliers When the clock multiplier is used, it is recommended to set N1 to '10' or '01' to reduce jitter and duty cycle sensitivity. It is also recommended to use a DAC_RATE of 64 or 100 when the clock multiplier is used.) 000 = MCLK input PIN (DEFAULT) 001 = MCLK_S1 010 = 2*MCLK_S1 011 = 4*MCLK_S1** 100 = 8*MCLK_S1** 11X = MCLK off
		MCLK_SRC (N2)																	**MCLK_S2 System MCLK Scaling Select** (Input: MCLK_S2; Output: MCLK_SRC) 000: MCLK_S2 (DEFAULT) 001: MCLK_S2/2 010: MCLK_S2/4 011: MCLK_S2/8 100: MCLK input pin
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
4	ENA_CTRL	DACEN_L																	**DAC Left Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DACEN_R																	**DAC Right Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
5	INTERRUPTMASK	OCP_OR_OTP_SHTDWN1_INTDIS																	**OCP/OTP Shutdown Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		CLIP_INT_ DIS																	**Clip Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		LOVDDDETB_INT_DIS																	**Low Voltage Detection Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		PWRUPEN_INT_DIS																	**Power Up Interrupt Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		OCP_OR_OTP_SHTDWN1_INTP_MASK																	**OCP/OTP Shutdown Interrupt Mask Enable Control** (Over Current/Over Temperature Shutdown) 0 = Disable (DEFAULT) 1 = Enable
		CLIP_INTP_MASK																	**Clip Interrupt Mask Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		LOVDDDET_INTP_MASK																	**Low Voltage Detection Interrupt Mask Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PWRUPEN_INTP_MASK																	**Power Up Interrupt Mask Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0x007F
6	INT_CLR_STATUS	INT_CLR_STATUS																	**Interrupt Status Clear Control** Write Operation: Write bits [6:0] 1s to clear the corresponding Interrupt Status Read Operation: REG6 [6:0] --- RD_INT_STATUS Bit0 = Power Up Bit2 = Low Voltage Detection Bit3 = Clip Bit4 = Over Current/Over Temperature Shutdown
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read/Write**
9	IRQOUT	IRQOUTSEL																	**IRQ Output Function Select** 0000 = IRQ (DEFAULT) 0001 = SDB 0010 = OSC_CLK 0011 = MUTEB 0100 = SHUTDWNDRVRR 0101 = PWRDOWN1B_D 0110 = PDOSCB 0111 = TMTALARM 1000 = SHUTDWNDRVRL 1001 = MCLK 1010 = MCLKDET 1011 = TALARM 1100 = SHORTL 1101 = SHORTR 1110 = PWRUPEN 1111 = TMDET
		DEM_DITH																	**Dither on SD Integrator Feedback** 0 = (DEFAULT) 1= 12x dither level (recommended setting)
		GAINZI3																	**Gain of CRFB 3rd Integrator** 0 = (DEFAULT)
		GAINZI2																	**Gain of O3 CRFB 2nd Integrator**

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			00000 = (DEFAULT)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 (Recommend 0x0080)**
A	IO_CTRL	**IRQ_PL**																	**IRQ Logic Select** 0 = Active Low (DEFAULT) 1 = Active High
		IRQ_PS																	**IRQ Pin Pull Select** 0 = Pull Down (DEFAULT) 1 = Pull Up
		IRQ_PE																	**IRQ Pin Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_DS																	**IRQ Current Drive Select** 0 = Low (DEFAULT) 1 = High
		IRQ_OE																	**IRQ Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_PIN_DEBUG_MODE																	**RESERVED**
		BCLK_DS																	**RESERVED**
		LRC_DS																	**RESERVED**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
B	PDM_CTRL	**PDM_LCH_EDGE**																	**PDM Mode Select** 0 = (DEFAULT) Left channel in falling edge Right channel in rising edge 1 = Left channel in rising edge Right channel in falling edge
		PDM_MODE																	**PDM Mode Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
C	TDM_CTRL	**TDM**																	**TDM Enable Control** (Not for I2S. I2S by definition is not TDM) 0 = Disable (DEFAULT) 1 = Enable
		PCM_OFFSET_MODE_CTRL																	**TDM PCM Offset Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DAC_LEFT_SEL																	**DAC Left Channel Source in TDM Mode Select** I2S 000 = Slot 0 (DEFAULT) 001 = Slot 2 010 = Slot 4 011 = Slot 6 PCM 000 = Slot 0 (DEFAULT) 001 = Slot 1 010 = Slot 2 011 = Slot 3 101 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7

#	Function	NAME	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DAC_RIGHT_SEL																	**DAC Right Channel Source in TDM Mode Select** I2S 000 = Slot 0 (DEFAULT) 010 = Slot 5 001 = Slot 3 011 = Slot 7 PCM 000 = Slot 0 (DEFAULT) 001 = Slot 1 010 = Slot 2 011 = Slot 3 100 = Slot 4 101 = Slot 5 110 = Slot 6 111 = Slot 7
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
D	**I2S_PCM_CTRL1**	**DACCM0**																	**DAC Companding Mode Control** 00 = Off (DEFAULT) 01 = RESERVED 10 = μ-Law Companding 11 = A-law Companding
		CMB8_0																	**8-bit Word Companding Mode Enable Control** 0 = Disable (DEFAULT) 1 = Enable (8-bit operation)
		UA_OFFSET																	**μ Law Offset Select** 0 = 1s complement (DEFAULT) 1 = 2s complement
		BCP0																	**BCLK Bit Clock Phase Inversion Select** 0 = Normal phase (DEFAULT) 1 = Input logic sense inverted
		LRP0																	**PCMA and PCMB Left/Right Word Order Select** 0 = Right justified/Left justified/I2S/PCMA mode (DEFAULT) 1 = PCMB mode (MSB is valid on 1st rising edge of BCLK after rising edge of FS)
		DACPSHS0																	**DAC Left / Right Channel Swap Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		WLEN0																	**Port Word Length of Audio Data Stream Select** 000 = 16-bit word length 001 = 20-bit word length 010 = 24-bit word length (DEFAULT) 011 = 32-bit word length (not for right justified) 100 = 8-bit word length
		AIFMT0																	**Port Audio Interface Data Format Select** 00 = Right justified 01 = Left justified 10 = Standard I2S format (DEFAULT) 11 = PCMA or PCMB
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0x000A**
E	**I2S_PCM_CTRL2**	**PCM_TS_ EN0**																	**PCM Time Slot Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PCM8BIT0																	**PCM 8-Bit Word Length Select** 0 = Use 0x0D[4:2]WLEN0 to select word length (DEFAULT) 1 = PCM 8-bit word length
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
F	**LEFT_TIME_SLOT**	**DIS_FS_SHORT_DET**																	**Short Frame Sync Detection Logic Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		TSLOT_L0																	**Left Channel PCM Time Slot Start Value / PCM TDM Offset Mode Slot Start Value** 0-63 = Legal values 64-1023 = RESERVED

#	Function	NAME	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
10	RIGHT_ TIME_SLOT	TSLOT_R0																	**Right Channel PCM Time Slot Start Value / unused for PCM TDM Offset Mode** 0-63 = Legal values 64-1023 = RESERVED
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
11	HPF_CTRL	DAC_HPF_ EN																	**DAC High Pass Filter Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DAC_HPF_APP																	**DAC High Pass Filter Application Mode**
		DAC_HPF_FCUT																	**DAC High Pass Filter Cut Off Frequency Select** 000 = 130 Hz (DEFAULT) 001 = 155 Hz 010 = 198 Hz 011 = 248 Hz 100 = 311 Hz 101 = 398 Hz 110 = 503 Hz 111 = 614 Hz
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
12	MUTE_CTRL	SOFT_MUTE																	**Soft Mute Enable Control** 0 = Gradually increase DAC volume to volume register setting (DEFAULT) 1 = Gradually lower DAC volume to zero
		DACEN_SM																	**DACEN Soft Mute Control** 0= Disable soft mute (DEFAULT) 1= Enable DAC volume ramping up of a channel on a rising edge of when it is turned on
		DAC_ZC_EN																	**DAC Zero Crossing Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		UNMUTE_CTL																	**Power-up Soft Unmute Select** X0 = No soft digital unmute on PWRUPEN and MUTEB events (DEFAULT) 01 = 512 MCLK per step soft unmute 11 = 32 MCLK per step soft unmute
		ANA_MUTE																	**Time on Power Up of Analog Mute Select** 00 = 430us (DEFAULT) 01 = 860us 10 = 1.7ms 11 = 4ms
		AUTO_MUTE																	**Auto Mute Control** 0 = Enable (DEFAULT - Mute driver after detection of 2048 zero samples) 1 = Disable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x2000
13	DAC_VOLUME	DAC_VOLUME_L																	**DAC Left Channel Volume Control** (Step size is 0.5dB.) 1111 1111 = +6dB 1111 1110 = +5.5dB 1111 1101 = +5dB ▼ 1111 0011 = 0dB (DEFAULT) ▼ 0101 0011 = -80dB ▼ 0101 0010 = RESERVED ▼ 0000 0001 = RESERVED 0000 0000 = Mute
		DAC_VOLUME_R																	**DAC Right Channel Volume Control** (Step size is 0.5dB.) 1111 1111 = +6dB 1111 1110 = +5.5dB

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			1111 1101 = +5dB ▼ 1111 0011 = 0dB (DEFAULT) ▼ 0101 0011 = -80dB ▼ 0101 0010 = RESERVED ▼ 0000 0001 = RESERVED 0000 0000 = Mute
		DEFAULT	1	1	1	1	0	0	1	1	1	1	1	1	0	0	1	1	**0xF3F3**
29	DAC_CTRL1	**DISABLE_ DEM**																	**DAC DEM Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		DEM_DLY_N																	**DAC DEM Delay Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CIC_GAIN_ADJ																	**DAC Output Fine Tuning**
		DAC_RATE																	**DAC Oversample Rate Select** 000 = 64 001 = 256 (DEFAULT) 010 = 128 100 = 32
		DEFAULT	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	**0x0081**
2A	DAC_CTRL2	**DEM_ DITHER**																	**First Order DEM Dithering Probability Select** (Step size is 1/16.) 0000 = No dithering (DEFAULT) 0001 = 1/16 0010 = 1/8 0011 = 3/16 0100 = 1/4 0101 = 5/16 0110 = 3/8 0111 = 7/16 1000 = 1/2 1001 = 9/16 1010 = 5/8 1011 = 11/16 1100 = 3/4 1101 = 13/16 1110 = 7/8 1111 = 15/16
		SDMOD_DITHER																	**SD Modulator Dithering Bit Number Select** (Step size is 1bit.) 0000 = No dithering (DEFAULT) 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 11 1100 = 12 1101 = 13 1110 = 14 1111 = 15
		DACPL																	**DAC Output Polarity Select** 0 = Non-Inverted (DEFAULT) 1 = Inverted
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
2C	ALC_CTRL1	ALC_ZC																	**ALC Zero Crossing Detection Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SCLEN																	**Slow Timer Clock Enable Control** (This bit is used as a timeout for the ALC gain update in zero crossing mode but the input signal won't be zero crossing. It can prevent the ALC gain never update in the never zero crossing situation in zero crossing mode.) 0 = Disable (DEFAULT) 1 = Enable
		ALCMAXGAIN																	**ALC Maximum Gain Select** 000 = 0dB (DEFAULT) 001 = -1dB 010 = -2dB 011 = -3dB 100 = -4dB 101 = -5dB 110 = -6dB 111 = -7dB
		ALCMINGAIN																	**ALC Minimum Gain Select** 000 = -1dB 001 = -2dB 010 = -4dB 011 = -6dB 100 = -8dB 101 = -10dB 110 = -12dB 111 = -14dB (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	**0x000E**
2D	ALC_CTRL2	ALCDCY																	**ALC Decay Timer Select** 0000 = 500 µsec/step 0001 = 1 msec/step 0010 = 2 msec/step 0011 = 4 msec/step 0100 = 8 msec/step 0101 = 16 msec/step 0110 = 32 msec/step 0111 = 64 msec/step 1000 = 128 msec/step (DEFAULT) 1001 = 256 msec/step 1010 = 512 msec/step 1011 = 1024 msec/step 1100 - 1111 = RESERVED
		ALCATK																	**ALC Attack Timer Select** 0000 = 2 µsec/step 0001 = 4 µsec/step 0010 = 8 µsec/step 0011 = 16 µsec/step 0100 = 32 µsec/step (DEFAULT) 0101 = 64 µsec/step 1110 = 128 µsec/step 0111 = 256 µsec/step 1000 = 512 µsec/step 1001 = 1024 µsec/step 1010 = 2048 µsec/step 1011 = 4196 µsec/step 1100 –1111 = RESERVED
		ALCHLD																	**ALC Hold Time Before Automated Gain Increase Select** 0000 = 0 msec (DEFAULT) 0001 = 2 msec 0010 = 4 msec 0011 = 8 msec 0100 = 16 msec 0101 = 32 msec 0110 = 64 msec

#	Function	NAME	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			0111 = 128 msec 1000 = 256 msec 1001 = 512 msec 1010 - 1111 = 1000 msec
		DEFAULT	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0x8400
2E	ALC_CTRL3	ALC_EN																	**ALC Enable Control** 0 = Disable (DEFAULT - fixed gain) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
2F	ALC_CTRL4	DRVRPWR																	**Class-D Driver Power Control Select** 0 = Low power (DEFAULT) 1 = Full power
		LPGAZC																	**Input Channel Zero Cross Detection Control** 0 = Gain changes to PGA register immediately (DEFAULT) 1 = Gain changes to PGA happen pending zero crossing logic
		CLIP_GAINADJUST																	**Clipping Event Maximum Gain Adjustment Select** 000 = No adjustment (DEFAULT) 001 = 0.5dB (2 steps) 010 = 1dB (4 steps) 011 = 2dB (8 steps) 100 = 3dB (12 steps) 101 = 4dB (16 steps) 110 = 5dB (20 steps) 111 = 6dB (24 steps)
		LPGAGAIN																	**Channel Input PGA Volume Control** (Step size is 0.25dB.) 00 0000 = -15.75dB 00 0001 = -15.5dB ▼ 11 1110 = -0.25dB 11 1111 = 0dB (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0x003F
40	CLK_DET_CTRL	REG_APWRUPEN																	**Power Up Enable Control** 0 = DAC data does not gate power up signal 1 = Clock detection requires non-zero samples in order to enable output power-up signal (DEFAULT)
		REG_CLKPWRUPEN																	**Clock Detection Module Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		REG_SRATE																	**Sample Rate Range Select** 000 = 8 – 12K 001 = 16 – 24K 010 = 32 – 48K (DEFAULT) 011 = 64 – 96K 100 = RESERVED
		DISASBLE_BCLK_RATIO																	**BCLK/LRC Ratio Detection Circuit Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		DEFAULT	1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	1	0xA801
4A	ANALOG_READ	L_DRIVER5																	**Left Class-D driver 5** 0 = Disable (DEFAULT) 1 = Enable
		L_DRIVER4																	**Left Class-D driver 4** 0 = Disable (DEFAULT) 1 = Enable
		L_DRIVER3																	**Left Class-D driver 3** 0 = Disable (DEFAULT) 1 = Enable
		L_DRIVER2																	**Left Class-D driver 2** 0 = Disable (DEFAULT)

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
																			1 = Enable
		PWRUPEN																	Raw PWRUPEN Signal
		MCLKDET																	MCLK Detection Bit
		R_DRIVER5																	Right Class-D driver 5 0 = Disable (DEFAULT) 1 = Enable
		LOVDDDETB																	VBAT Under Voltage Lockout Bit
		SAR_TDC[7]																	Clock Multiplier SAR TDC bit 7
		SAR_TDC[6]																	Clock Multiplier SAR TDC bit 6
		SAR_TDC[5]																	Clock Multiplier SAR TDC bit 5
		SAR_TDC[4]																	Clock Multiplier SAR TDC bit 4
		SAR_TDC[3]																	Clock Multiplier SAR TDC bit 3
		SAR_TDC[2]																	Clock Multiplier SAR TDC bit 2
		SAR_TDC[1]																	Clock Multiplier SAR TDC bit 1
		SAR_TDC[0]																	Clock Multiplier SAR TDC bit 0
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	READ ONLY
50	MIXER_CTRL	MIXER_OPTION																	Output Mixer Option Select 00 = bypass (DEFAULT) 01 = (L+R)/2 10 = (L-R)/2 11 = (L-R)/2 on L output; (R-L)/2 on R output
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
60	BIAS_ADJ	VMID_SEL																	VMIDEN Tie-Off Select 00 = Open (DEFAULT) 01 = 25 KOhm 10 = 125 KOhm 11 = 2.5 KOhm
		BIASADJ																	PGA Master Bias Current Power Select 00 = normal operation (DEFAULT) 01 = 9% reduced bias current 10 = 17% reduced bias current 11 = 11% increased bias current
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000
61	ANALOG_ CONTROL _1	VMDFSTENB																	VMIDEN Reference Fast Power Up Circuit Disable Control 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		CLASSDEN																	CLASS-D Enable Control 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		DACCLKEN_RIGHT																	Right Channel DAC Clock Enable Control 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		DACEN_RIGHT																	Right Channel DAC Enable Control 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		DACCLKEN_LEFT																	Left Channel DAC Clock Enable Control 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable

#	Function	NAME	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DACEN_LEFT																	**Left Channel DAC Enable Control** 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		BIASEN																	**Current BIAS Reference Enable Control** 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		VMIDEN																	**VMIDEN Reference Enable Control** 00 = Disable (DEFAULT) 01 = Enable (gated by PWRUPEN signal) 10 = Disable 11 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
63	ANALOG_ CONTROL_3	PD_L																	**Left Channel Power Down Enable Control** (Should only be set in initialization to avoid pops) 0 = Disable (DEFAULT) 1 = Enable
		PD_R																	**Right Channel Power Down Enable Control** (Should only be set in initialization to avoid pops) 0 = Disable (DEFAULT) 1 = Enable
		GAIN_F																	**Class-D Fine GAIN Control** GAIN_F + GAIN_C HEX dB '11 00001' 0x61 -6.9dB '10 00001' 0x41 -4.7dB '01 00001' 0x21 -2.4dB '00 00001' 0x01 +0.0dB '11 00010' 0x62 -0.5dB '10 00010' 0x42 +1.5dB '01 00010' 0x22 +3.6dB '00 00010' 0x02 +5.8dB
		GAIN_C																	'11 00100' 0x64 +6.1dB '10 00100' 0x44 +7.9dB '01 00100' 0x24 +9.8dB '00 00100' 0x04 +11.6dB '11 01000' 0x68 +13.7dB '10 01000' 0x48 +14.8dB '01 01000' 0x28 +16.0dB '00 01000' 0x08 +17.0dB '00 10000' 0x10 +21.9dB '11 11111' 0x7F mute
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
64	ANALOG_ CONTROL_4	CLASSD SLEW																	**Class-D Driver Slew Rate Adjustment Select** 00000000 = Normal (DEFAULT) 00000001 = +25% for low signal levels 00000010 = +25% for low signal levels 00000100 = -25% for low signal levels 00001000 = -25% for low signal levels 00010000 = -25% for low signal levels 00100000 = -25% for low signal levels 01000000 = +25% for low signal levels 10000000 = +25% for low signal levels
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
65	ANALOG_ CONTROL_5	MCLK_RANGE																	**Extended Clock Multiplier Input Range Select** (Enable required for 8x MCLK) 0 = (DEFAULT) 1 = 2x longer period (lower frequencies)

#	Function	NAME	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		MCLK8XEN																	**8x MCLK Multiplier Enable Control** (Requires 0x65[0] = 1) 0 = Disable (DEFAULT) 1 = Enable
		MCLK4XEN																	**4x MCLK Multiplier Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
66	**ANALOG_CONTROL_6**	**VBATLOW_STATUS**																	**VBATLOW Logic Select** (when VBATTHREN = 0) 0 = (VBATLOW = 0) (DEFAULT) 1 = (VBATLOW = 1)
		VDDSPK_LMT_EN																	**VDDSPK Limiter Threshold Enable Control** (Enable comparator with threshold set in VBATTHRES) 0 = Disable (DEFAULT) 1 = Enable
		VDDSPK_CLIPLMT_THRESHOLD																	**VDDSPK Clip Limiter Threshold Select** (VBATLOW= 1 when VDDSPK is lower than) 000 = 4.1V (DEFAULT) 001 = 3.9V 010 = 3.7V 011 = 3.5V 100 = 3.3V 101 = 3.1V 110 = 2.9V 111 = 2.7V
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
69	**CLIP_CTRL**	**ANTI_CLIP_EN**																	**Clip Function Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
73	**RDAC**	**CLK_DAC_DELAY**																	**DAC Clock Delay Select** 000 = delay 0 nsec (DEFAULT) 001 = delay 1 nsec 010 = delay 2 nsec 011 = delay 3 nsec 100 = delay 4 nsec 101 = delay -3 nsec 110 = delay -2 nsec 111 = delay -1 nsec
		DACVREFSEL																	**DAC Reference Voltage Select** (Used for minor tuning of the output level.) 00 = VDDA (unregulated) 01 = VDDA x 1.5/1.8 V 10 = VDDA x 1.6/1.8 V (DEFAULT) 11 = VDDA x 1.7/1.8 V
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0x0008**

7 APPLICATION CIRCUIT

7.1 Typical Application Diagram

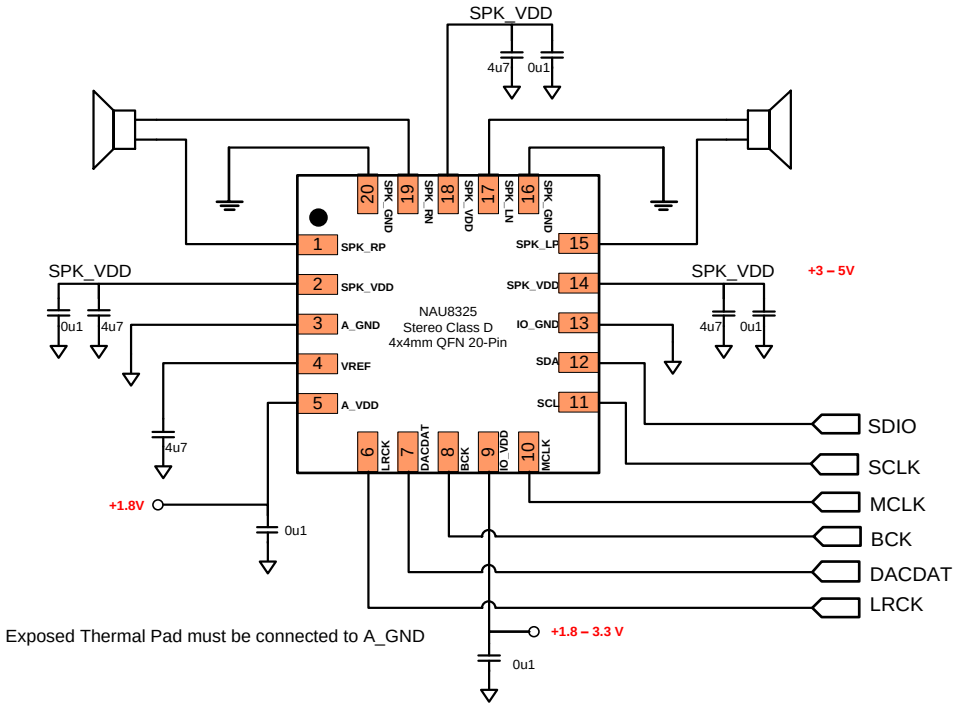


Figure 28 NAU8325/NAU83U25 Typical Application Diagram

7.2 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

7.2.1 PCB Layout Notes

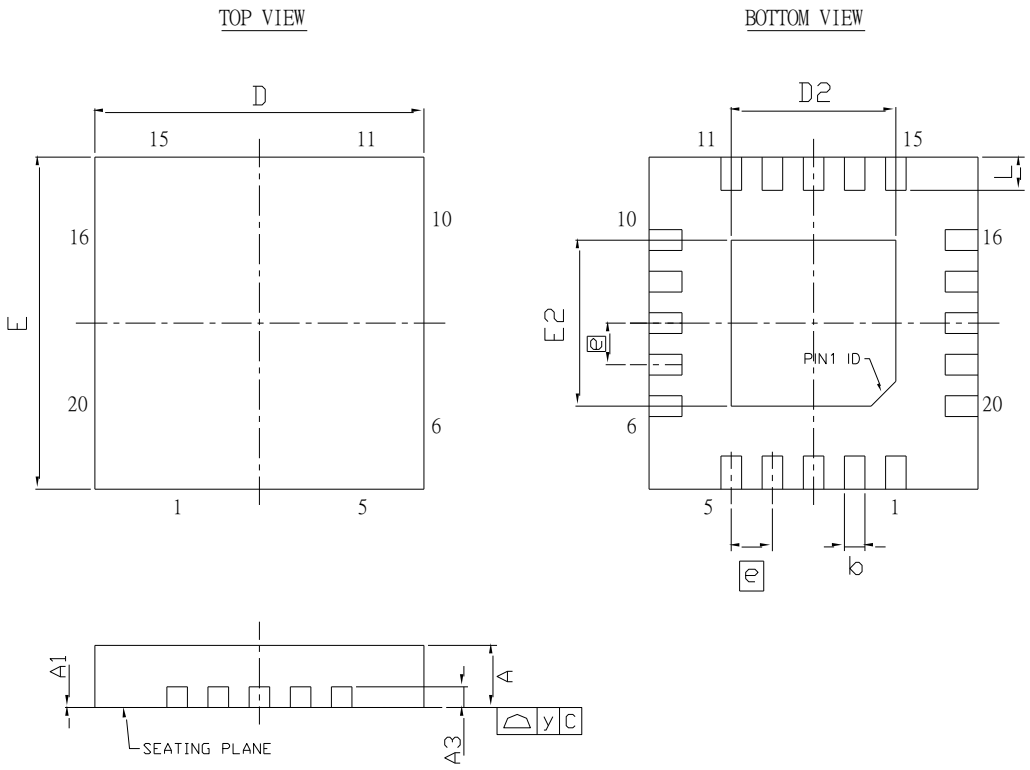
The Class-D Amplifier is a high power switching circuits that can cause Electro Magnetic Interference (EMI) when poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a GND plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the GND pins and have solid connections to the plane
- Planes on A_VDD, IO_VDD & SPK_VDD are optional
- The SPK_VDD connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- Keep the VREF capacitor close to the pin
- For better heat dissipation, use VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect SPK_LP, SPK_LN, SPK_RP & SPK_RN to U1. Use a direct top layer copper connection to the pins. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes

8 PACKAGE DIMENSION

NAU8325/NAU83U25 Stereo Class-D Amplifier is available in a small, QFN20L 4x4mm package, using 0.5 mm pitch



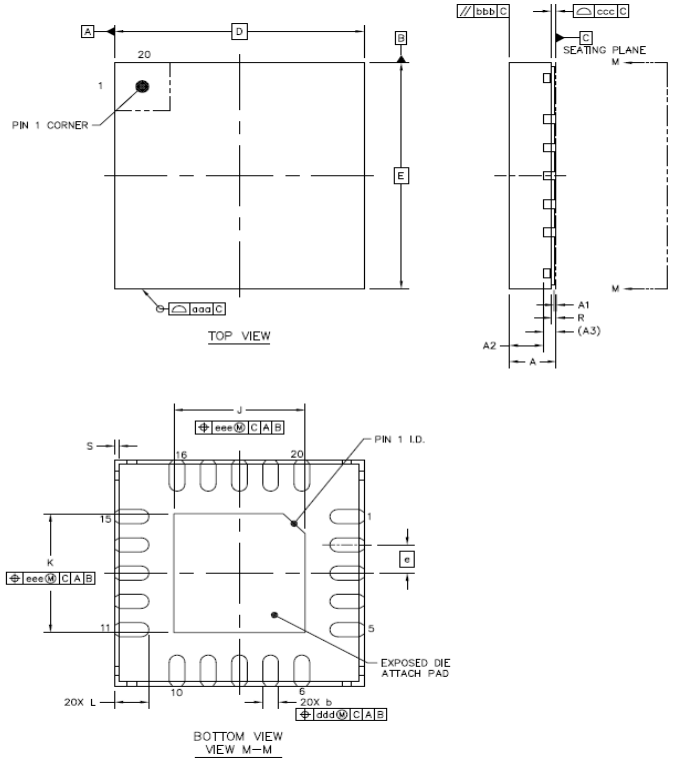
Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

Note:D2,E2 by die size difference .

Figure 29 NAU8325/NAU83U25 Package Specification

Wettable QFN20L 4x4mm package



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	2	2.1	2.2
	Y	K	2	2.1	2.2
LEAD LENGTH		L	0.5	0.55	0.6
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	
HALF-CUT DEPTH		R	0.075	---	---
HALF-CUT WIDTH		S	---	---	0.075

Figure 30 NAU8325 Wettable Package Specification

9 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU8325YG	4mm x 4mm	QFN-20	Green
NAU8325WG	4mm x 4mm	Wettable QFN-20	Green
NAU83U25YG	4mm x 4mm	QFN-20	Green

NAU83_25 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-20
W = Wettable QFN-20

Package Grade:

Blank = Commercial & Industrial Grade

U = Automotive Grade AEC-Q100 qualification & TS16949 compliant

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Apr 04, 2018	Initial Release
1.1	Apr 10, 2018	Internal review Updated expand clock detection/auto power-down description. Updated final register map
1.2	Apr 13, 2018	Release to Alpha
1.3	May 18, 2018	Updated unused right-justified PCM modes Updated digital gain settings to 6dB -- -80dB Updated AUTO_MUTE description Updated clock source description
1.4	Jun, 2018	Updated MCLK_SRC/LRCK possible rations to include 400/500
1.5	Jul, 2018	Updated I2C Slave Address to 0x21 Updated electrical parameters
1.6	Oct, 2018	Updated PDM description Updated CLK_CTRL reg MCLK off. Updated reg 0x02, 0x03, 0x4A, 0x63, 0x65 descriptions Updated PSRR limits & gain
1.7	Oct, 2018	Updated reg 0x0C, 0x0D for PCM options
1.8	Jan, 2019	Updated 7.5 POR Updated ANALOG_CTRL_3 PD bits for mono operation Updated Silicon Rev to xF2
1.9	Feb, 2019	Updated 9.3 Electrical characteristics for mono
2.0	Aug, 2019	Updated digits in I2C slave address in table Updated VSS to GND consistent with pin names
2.1	Jun 16, 2020	Updated format
2.2	Jun 1, 2021	Updated Register 0x9 [7] description
2.3	Jun 21, 2021	Updated Register 0x4 0x5 format correctioin Updated Reg0x9 default setting value
2.4	Feb 28, 2022	Updated Register Table Format
2.5	Feb 1, 2023	Updated Halogen-free, RoHS-compliant and TSCA-compliant description
2.6	Oct 30, 2023	Updated T_{DOD} description
2.7	Nov 9, 2023	Updated Register Table
2.8	Mar 29, 2024	Updated wettable QFN package
2.9	Sep 16, 2024	Updated Format

REVISION	DATE	DESCRIPTION
3.0	Jan 22, 2025	Updated Ordering Information
3.1	Dec 18, 2025	Update ALC description & register

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