NuMicro® Family

Low-Noise 24-bit Delta-Sigma ADC

NADC24 Series
Datasheet

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1 GENERAL DESCRIPTION

NADC24, which stands for NuMicro 24-bit Analog-to-Digital Converter (ADC), is an integrated 24-bit delta-sigma (ΔΣ) analog-to-digital converter. Designed to deliver excellent precision and speed, the NADC24 series achieves outstanding low-noise performance with up to 22-bit Effective-Number-of-Bits (ENOB). This makes it an ideal choice for demanding applications where high-precision analog signal conversion is essential for optimal performance.

The key components of NADC24 include a low-noise programmable gain amplifier (PGA), an internal voltage reference of 1.2V or 2.4V, a delta-sigma modulator, a digital filter and a 49.152 MHz oscillator. The characteristics of these key components ensure NADC24's high precision signal conversion. Furthermore, in order to achieve higher performance and integration, the NADC24 series integrates an input multiplexer with up to 8 single-ended channels, a 12-bit Digital-to-Analog Converter (optional in its portfolio), a temperature sensor and an SPI interface. These integrated features effectively facilitate a compact PCB design and reduce component costs. The NADC24's operating voltage ranges from 2.7 V to 3.6 V while its operating temperature ranges from -40 °C to 105 °C. The NADC24 series offers NADC24D003FA with TSSP20 package and NADC24D004TA with QFN32 package.

As a highly integrated precision ADC, the NADC24 series brings significant values in following applications including:

- Utility meters
- Pressure sensors
- Gas sensors
- Oximeters
- Glucose meters
- Temperature controllers
- Programmable logic controllers (PLC)

2 FEATURES

- Operating Characteristics
  - Voltage range: 2.7 V to 3.6 V
  - Temperature range: -40 °C to 105 °C
  - EFT ±4.4 KV
  - ESD HBM ±4 KV
- Clocks
  - Internal 49.152 MHz HIRC oscillator with a variation of ±2 % across all temperature ranges
- Analog
  - Up to 4 differential or 8 single-ended multiplexed input channels
  - One internal differential channel for internal temperature sensor
  - One external common mode voltage input for single-ended input mode (only with NADC24D004TA)
  - One internal single-end channel for internal DAC (only with NADC24D004TA)
  - Low-Noise PGA with programmable gains of 1, 2, 4, 8, 16, 32, 64 and 128
  - Configurable output data rates: 15.625 SPS to 96 KSPS
  - Internal voltage reference: 1.2 V or 2.4 V, 100 ppm/°C drift
  - Internal temperature sensor with accuracy up to ±2 ˚C accuracy
- Communication
  - One set of SPI interface for external communication

2.1 Applications

- Utility meters
- Power distribution unit (PDU)
- Pressure sensors, Gas sensors
- Oximeters, Glucose meters
- Temperature controllers, Programmable logic controllers (PLC)

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	Package	Body Size
NADC24D003FA	TSSOP20	4.4 mm x 6.5 mm
NADC24D004TA	QFN32	4 mm x 4 mm

3.2 NADC24 Series Naming Rule

NADC	24	D	0	03	F	A
Prefix	**Resolution**	**Architecture**	**Line**	**Differential Channels**	**Package**	**Version**
NADC	24: 24-bit	D: Delta-sigma	0: Reserved	03: 3 Ch 04: 4 Ch	F: TSSOP20 (4.4x6.5 mm) T: QFN32 (4x4 mm)	A

3.3 NADC24 Series Selection Guide

Part Number	NADC24D003FA	NADC24D004TA
V_{DD}	2.7 V ~ 3.6 V	2.7 V ~ 3.6 V
Multi-channel configuration	Multiplexed	Multiplexed
Input Channels (differential)	3	4
ENOB (Bit)	Up to 22	Up to 22
Output Data Rate (SPS)	15.625 ~ 96,000	15.625 ~ 96,000
Sampling Frequency (MHz)	1	1
12-bit DAC	-	1
Temperature Sensor	√	√
Internal V_{REF}	1.2 V or 2.4 V	1.2 V or 2.4 V
SPI	1	1
Package	TSSOP20	QFN32

4 PIN CONFIGURATION

4.1 NADC24 Series QFN 32-Pin Diagram

Corresponding Part Number: **NADC24D004TA**

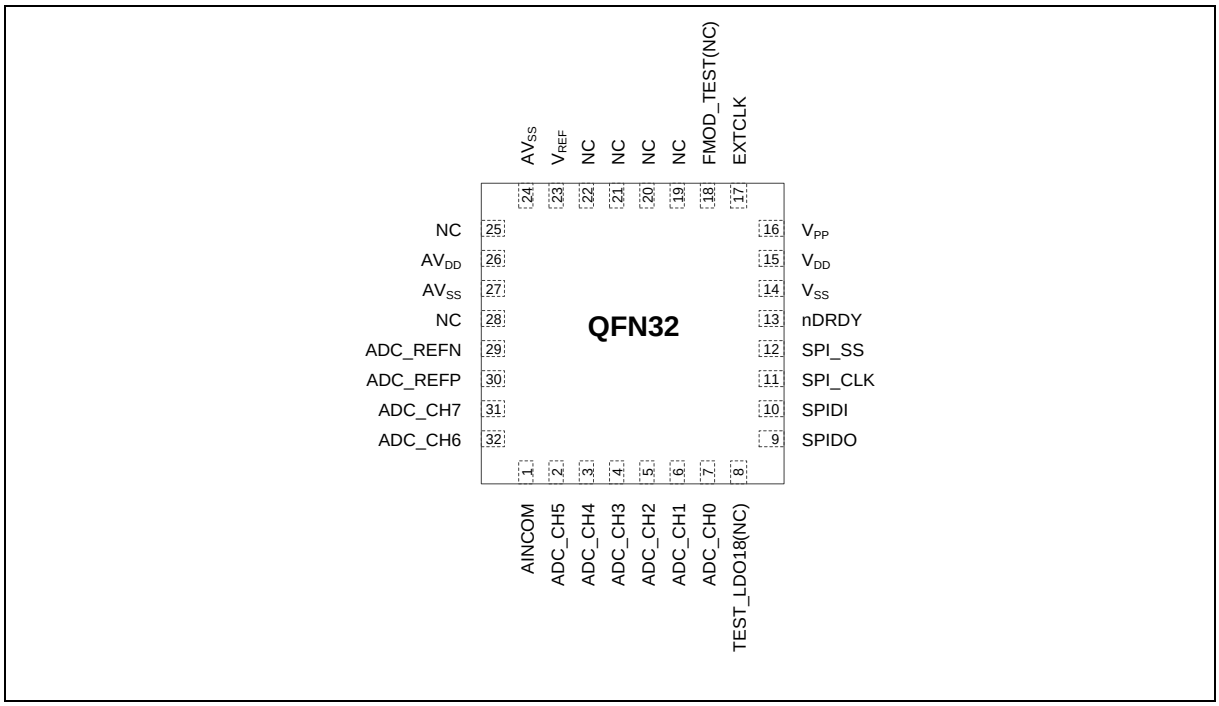


Figure 4.1-1 NADC24 Series QFN 32-Pin Diagram

4.2 NADC24 Series TSSOP 20-Pin Diagram

Corresponding Part Number: **NADC24D003FA**

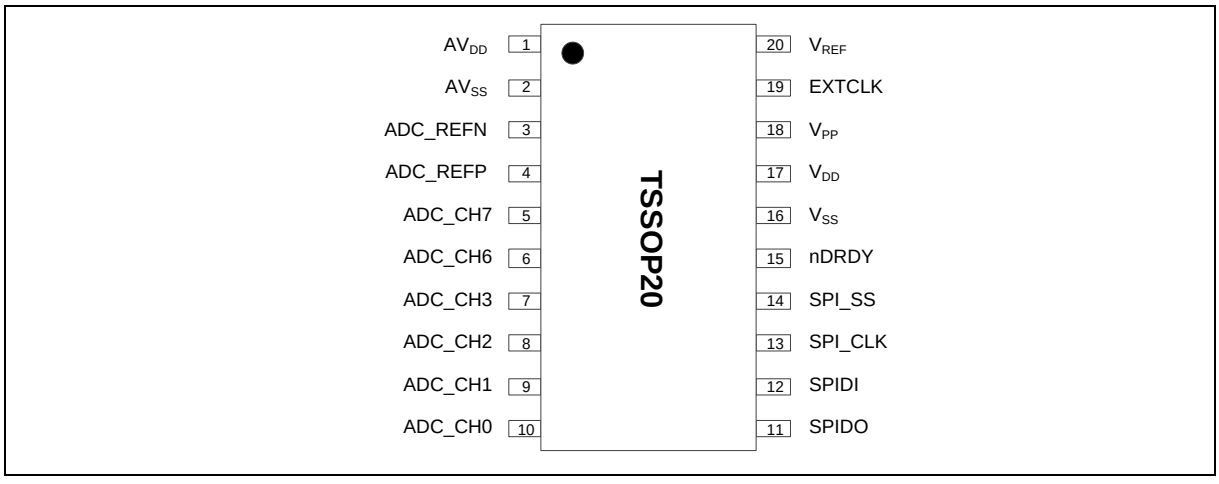


Figure 4.2-1 NADC24 Series TSSOP 20-Pin Diagram

4.3 Pin Description

Pin number		Pin Name	Type	Description
TSSOP20	QFN32			
	1	AINCOM	A	ADC external common voltage input for single ended mode. **Note:** For offset calibration, user must set PGA INP/INN connect to AINCOM (AINCOM = V_{REF}/2) or internal VCM.
	2	ADC_CH5	A	ADC channel pair 2 positive analog input
	3	ADC_CH4	A	ADC channel pair 2 negative analog input
7	4	ADC_CH3	A	ADC channel pair 1 positive analog input
8	5	ADC_CH2	A	ADC channel pair 1 negative analog input
9	6	ADC_CH1	A	ADC channel pair 0 positive analog input
10	7	ADC_CH0	A	ADC channel pair 0 negative analog input
	8	TEST_LDO18(NC)	P	Reserved
11	9	SPIDO	I/O	SPI data output
12	10	SPIDI	I/O	SPI data input
13	11	SPI_CLK	I/O	SPI serial clock input
14	12	SPI_SS	I/O	SPI chip select (Low active)
15	13	nDRDY	I/O	ADC 24-bit data ready (low active)
16	14	V_{SS}	G	Digital 3V ground pin
17	15	V_{DD}	P	Digital 3V power pin
18	16	V_{PP}	P	Must be connected to Vss.
19	17	EXTCLK	I/O	Reserved
	18	FMOD_TEST(NC)	O/-	FMOD clock output for BYPASS_ALL test mde. Leave unconnected for normal mode.
	19	NC	-	Leave unconnected or connected to AVss.
	20	NC	-	Leave unconnected or connected to AVss.
	21	DAC_OUT	A	DAC output voltage
	22	DAC_VREF	A	DAC reference input
20	23	V_{REF}	A	Internal V_{REF} output voltage for user usage
	24	AV_{SS}	G	Analog 3V ground
	25	NC	-	Leave unconnected or connected to AVss.
1	26	AV_{DD}	P	Analog 3V power pin. Connect 0.1uF//10uF capacitors to AVss.
2	27	AV_{SS}	G	Analog 3V ground
	28	NC	-	Leave unconnected or connected to AVss.
3	29	ADC_REFN	A	ADC Negative reference voltage
4	30	ADC_REFP	A	ADC Positive reference voltage

Pin number		Pin Name	Type	Description
TSSOP20	QFN32			
5	31	ADC_CH7	A	ADC channel pair 3 positive analog input
6	32	ADC_CH6	A	ADC channel pair 3 negative analog input

5 BLOCK DIAGRAM

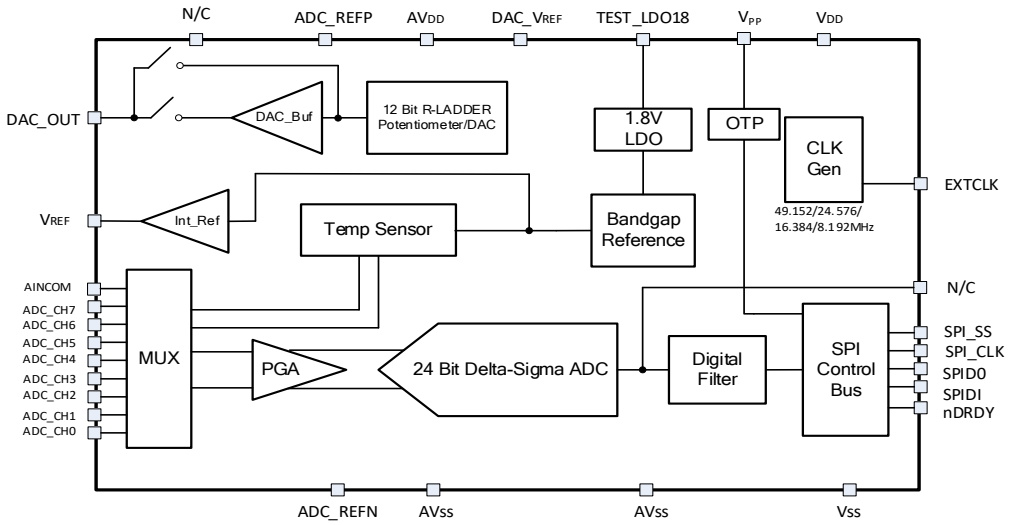


Figure 4.3-1 NADC24 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Overview

The NADC24 series precision 24-bit, up to 8 external input channels delta-sigma (ΔΣ) ADC is equipped with an integrated analog front end (AFE) to simplify precision sensor connections. The ADC provides output data rates from 15.625 SPS to 96000 SPS for flexibility in resolution and data rates over a wide range of applications. The low-noise and low-drift architecture makes these devices suitable for precise measurement of low-voltage sensors, such as load cells and temperature sensors.

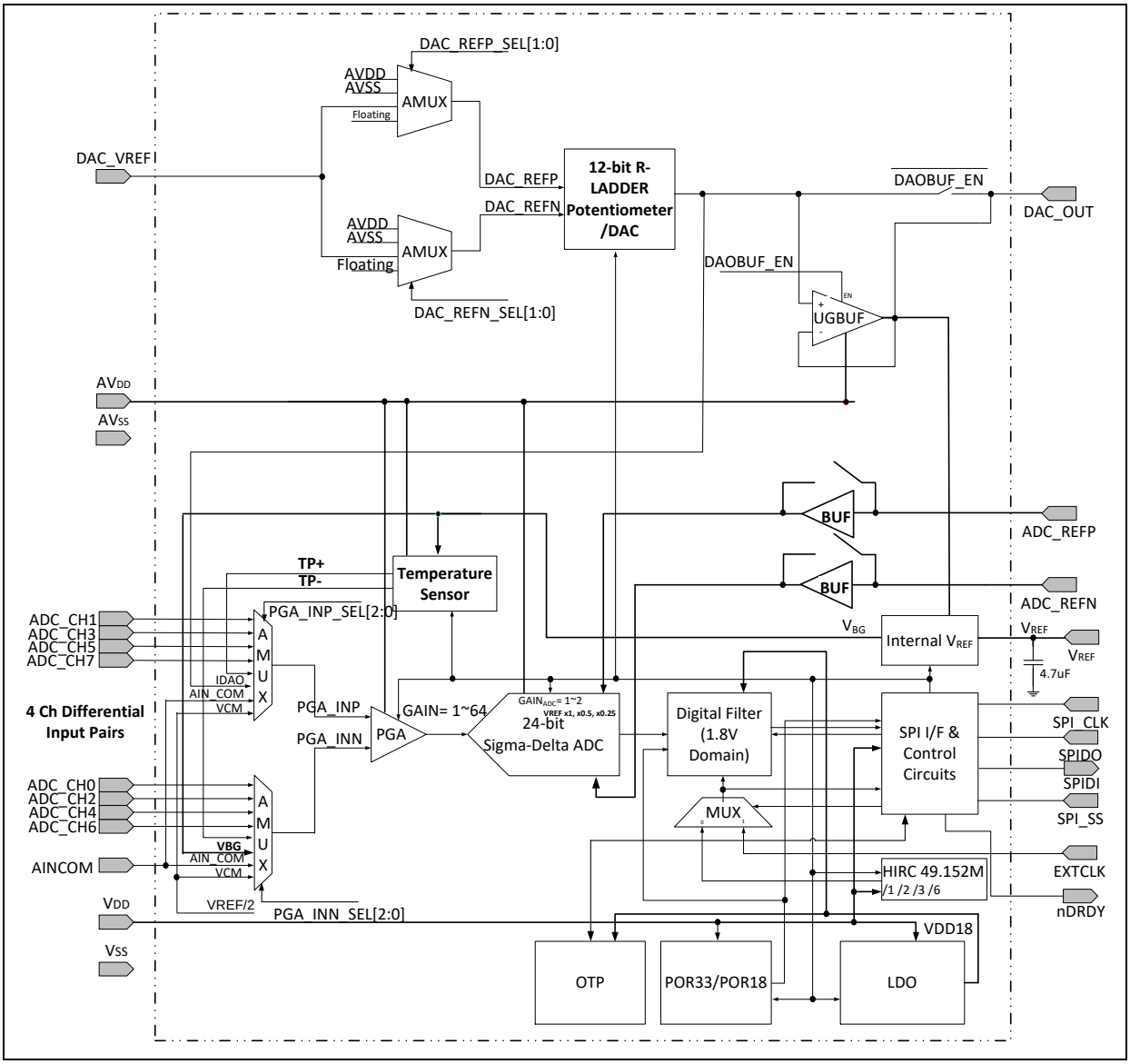


Figure 6.1-1 NADC24 Function Block Diagram

6.1.1 ADC Reference Voltage Input Buffer

- Input offset chopping
- Programmable buffer gain (x1/x0.5/x0.25)

6.1.2 Internal Reference Voltage Generator

- Input offset chopping
- Programmable output driver for 1.2V and 2.4V
- External compensation needs to add 4.7μF capacitor on REFO pin
- Large driving capability ±10mA (from marketing)
- 1.2V or 2.4V output with ±1% after tuning/trimming

6.1.3 Band-gap

- 2nd order curve correction
- Chopper operational amplifier offset reduction
- Output level tuning/trimming
- Vbe compensation tuning/trimming
- Low voltage design enlarges supply range
- Separated outputs for different block to reduce noise/glitch coupling
- Current source chopping

6.1.4 Temperature Sensor

Internal temperature sensor can be used to measure temperature when PWD_TEMPSENSOR = 0. The temperature deviation of this temperature sensor is ± 3˚C accuracy after single point calibration is done in factory test and data (D_{TA} at 25˚C) is written to Temperature Sensor Calibration Data Register 1~3. To calculate the current temperature (Assume get D_{TB} at T_B), $T_B = \{(D_{TB} - D_{TA}) / [D_{TA} / (273+25)]\} + 25$.

6.1.5 LDO 1.8V

- Output 1.8V for digital section
- Accuracy not that important since it supply digital section
- Requires 10mA driving capability
- Line regulation < 100mV 2.7V-3.6V
- Load regulation < 100mV 10mA

6.1.6 Offset Calibration

Offset calibration behavior description:

- SOFTWARE set ADC related registers such as data rate, PGA gain, etc. same as target application.
- SOFTWARE choose PGA input source:
  - Set SEL_PGA_INP = SEL_PGA_INN=b110 for using external common voltage input.
  - Set SEL_PGA_INP = SEL_PGA_INN=b111 for using internal common voltage.
- SOFTWARE set SETLSEL(ADC_CTREL[7:5])=011 or SETLSEL(ADC_CTREL[7:5])=010 & LOW_LAT_EN(DF_CTRL_2[3])=1

- Send offset calibration command (0x10)
- Wait nDRDY = 0
- Read offset value through ADC OCDx
- Set OFFSETDIS = 0 to enable offset calibration function
- Total calibration time is x6 conversion time (reciprocal of output data rate) or x4 conversion time if LOW_LAT_EN(DF_CTRL_2[3])=1 without FIR filter

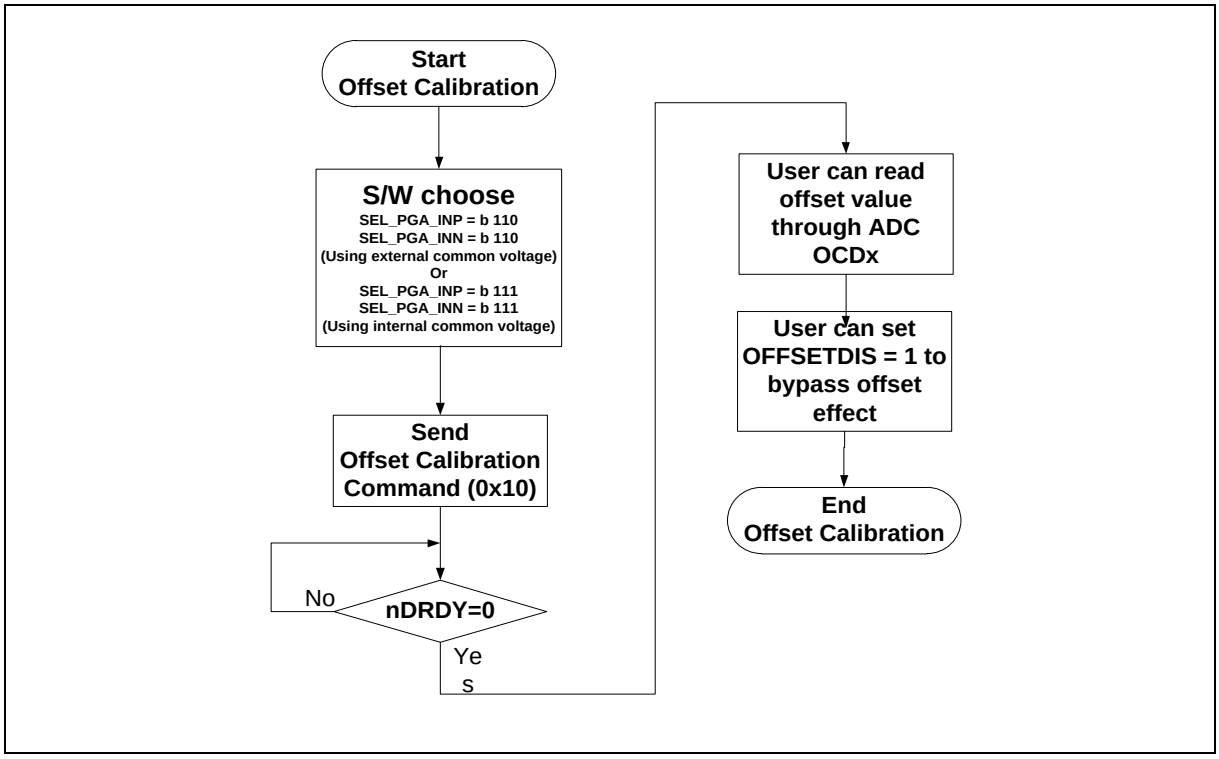


Figure 6.1-2 Offset Calibration Flow Chart

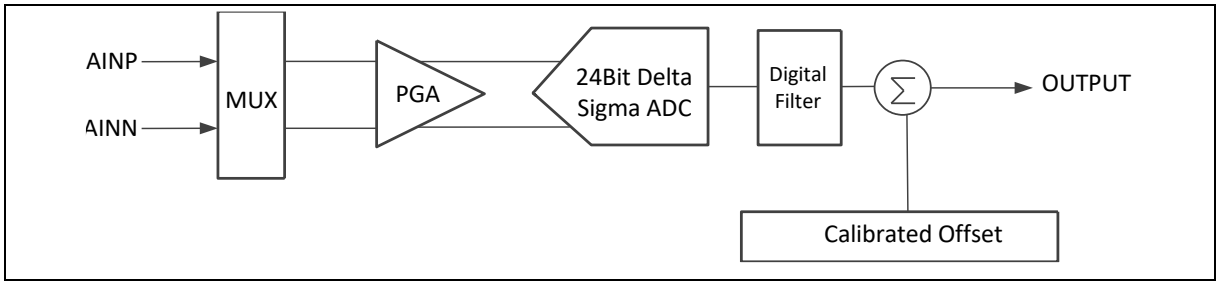


Figure 6.1-3 Offset Calibration Mode

6.2 Feature Description

6.2.1 ADC Modulator and Digital Filters

The ADC modulator outputs 3-bit data, which is the input of the digital filter. The final output is a signed 24-bit data. Digital filter setting for different output data rate is shown bellow.

ADC_CLK_SET	OSR_SEL	FSPS	CLOCK	Fmod	OSR	NOTES
10	0000	15.625sps	8.192Mhz	512 kHz	32768	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0001	31.25sps	8.192Mhz	512 kHz	16384	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0010	62.5sps	8.192Mhz	512 kHz	8192	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0011	125sps	8.192Mhz	512 kHz	4096	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0100	250sps	8.192Mhz	512 kHz	2048	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0101	500sps	8.192Mhz	512 kHz	1024	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0110	1000sps	8.192Mhz	512 kHz	512	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	0111	2000sps	8.192Mhz	512 kHz	256	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	1000	4000sps	8.192Mhz	512 kHz	128	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode.
10	1001	8000sps	8.192Mhz	512 kHz	64	SINC^4 Filter High current mode.
11	0000	31.25sps	8.192Mhz	1.024Mhz	32768	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0001	62.5sps	8.192Mhz	1.024Mhz	16384	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0010	125sps	8.192Mhz	1.024Mhz	8192	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0011	250sps	8.192Mhz	1.024Mhz	4096	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0100	500sps	8.192Mhz	1.024Mhz	2048	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0101	1000sps	8.192Mhz	1.024Mhz	1024	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0110	2000sps	8.192Mhz	1.024Mhz	512	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	0111	4000sps	8.192Mhz	1.024Mhz	256	SINC^4 Filter + 30 Taps FIR (can be bypassed). High current mode 2.
11	1000	8000sps	8.192Mhz	1.024Mhz	128	SINC^4 Filter High current mode 2.
11	1001	16000sps	8.192Mhz	1.024Mhz	64	SINC^4 Filter High current mode 2.

Table 6.2-1 Digital Filter Selection Table

Filter Architecture

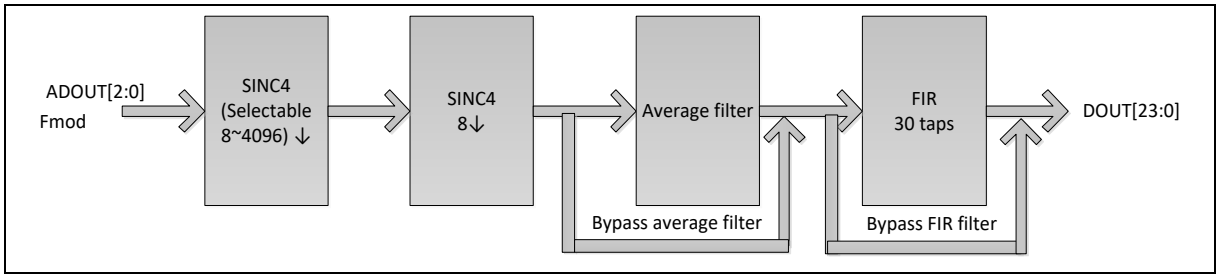


Figure 6.2-1 Filter Architecture

6.2.2 ADC Over-driving Mode

The NADC24 supports an over-driving mode that output data rate can raise up to 96 kSPS. There are some conditions must be met for this mode:

- V_{DD}/AV_{DD} must be higher than 3.15V
- ADC related circuits' bias current control registers must be set to maximum such as VCM_BIAS_SET, MOD_REFP_BIAS_SET, MOD_REFN_BIAS_SET, PGA_BIAS_SET, PGA_BUFF_BIAS_SET, ADC_BIAS_SET, ADC_OP1_BIAS_SET and ADC_OP2_BIAS_SET
- The recommended system setting for over-driving mode is as follows:

CLOCK freq. (HIRC/EXCLK)	ADC_CLK_SET	OSR_SEL	FSPS	Fmod	OSR	NOTES
8.192 MHz	11	0111	4000sps	1.024 MHz	256	By-pass FIR is recommended
8.192 MHz	11	1000	8000sps	1.024 MHz	128	
8.192 MHz	11	1001	16000sps	1.024 MHz	64	
16.384 MHz	11	0111	8000sps	2.048 MHz	256	
16.384 MHz	11	1000	16000sps	2.048 MHz	128	
16.384 MHz	11	1001	32000sps	2.048 MHz	64	
24.576 MHz	11	0111	12000sps	3.072 MHz	256	
24.576 MHz	11	1000	24000sps	3.072 MHz	128	
24.576 MHz	11	1001	48000sps	3.072 MHz	64	
49.152 MHz	11	0111	24000sps	6.144 MHz	256	
49.152 MHz	11	1000	48000sps	6.144 MHz	128	
49.152 MHz	11	1001	96000sps	6.144 MHz	64	

Table 6-2 Digital Filter Selection Table for Over-driving Mode

6.2.3 Low-Noise PGA

The NADC24 features a low-drift, low-noise PGA that provides a complete pre-signal amplification for bridge sensors. Different input impedance must be configured according to different gains. In order to obtain the most stabilized value, the resistors must be accurately-matched to the choice of sensor.

- PGA gain 1x 2x 4x 8x 16x 32x 64x (PGA buffer provides 2x gain)
- PGA input refer noise around 65nVrms for gain=1, 31.25SPS, ENOB=22Bits
- To drive switch capacitor circuit
- High input impedance
- Internal Dominate pole compensation
- Source degeneration design to reduce noise
- Non-inverting fully differential
- Chopping to reduce 1/f noise and offset
- Large input devices gm
- GBW=5 MHz

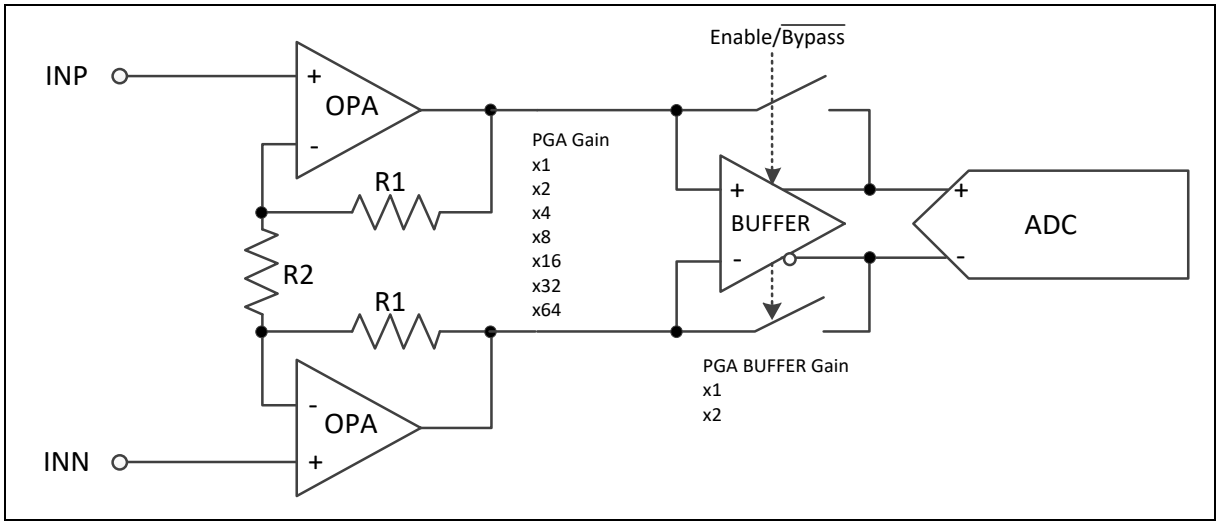


Figure 6.2-2 Internal PGA

6.3 Control Register

The ADC is controlled and configured via a number of on-chip registers, which are described in the following sections. In the descriptions, set implies logic 1 state and cleared implies logic 0 state, unless otherwise noted.

6.3.1 SPI

The communication interface of NADC24 uses SPI Communication Protocol. There are four pins, SPI_SS, SPIDO, SPIDI and SPI_CLK. SPI initiates operation at this stage. First power-on and power-down wake-up needs 250us wait time to start ADC conversion.

SPI_CLK max speed is 20 MHz; duty should control in 40/60. SPIDI is data input channel. When SPIDI data is in SPI_CLK rising edge, the NADC24 receives data from Master devices. One frame of SPI is 8-bit, the first frame is command. Command format is shown in Table 6.3-1.

6.3.2 Command Table

Command	Description	First Command Byte	Second Command Byte
CONTROL COMMANDS			
NOP	No operation	0x00	-
WAKE_UP	Wake-up from Power-down mode	0x02	-
POWER_DOWN	Enter Power-down mode	0x04	-
RESET	Reset whole chip	0x06	-
START	Start ADC conversion	0x08	-
STOP	Stop ADC conversion	0x0a	-
CALIBRATION COMMANDS			
SYSOC	System offset error calibration	0x10	-
DATA READ COMMAND			
READ_DATA	Read ADC data	0x20	-
REGISTER ACCESS COMMANDS			
READ_REG	Read nnnnn registers from address aaaaa	0b 010a aaaa	0b 000n nnnn
WRITE_REG	Write nnnnn registers from address aaaaa	0b 011a aaaa	0b 000n nnnn
FIR COEFFICIENT ACCESS COMMANDS			
READ_COEF	Read coefficient from address aaaaa	0b 100a aaaa	0b 0000 0010
WRITE_COEF	Write coefficient from address aaaaa	0b 101a aaaa	0b 0000 0010
Note: n nnnn = (number of registers to read or write) - 1			

Table 6.3-1 Command Table

6.3.3 Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Address	R/W	Description	Reset Value
Base Address: **UTCPD_BA = 0x00**				
PWD_CTRL 1	0x00	R/W	Power Down Control	0x00
PWD_CTRL 2	0x01	R/W	Power Down Control	0x80
DF_CTRL 1	0x02	R/W	Digital Filter Control 1	0x05
DF_CTRL 2	0x03	R/W	Digital Filter Control 2	0x22
ADC_CTRL	0x04	R/W	ADC Control	0x06
BIAS_CTRL 1	0x05	R/W	Bias Control 1	0xFD
BIAS_CTRL 2	0x06	R/W	Bias Control 2	0x55
CHOP_CTRL	0x07	R/W	CHOP Control	0x01
BG_CTRL 1	0x08	R/W	Band-gap Control 1	0x77
OSC_CTRL 1	0x09	R/W	OSC Control 1	0x00
OSC_CTRL 2	0x0A	R/W	OSC Control 2	0x86
REF_CTRL	0x0B	R/W	Internal Reference Control and 1.8V LDO Control	0x9F
DAC_DATA 1	0x0C	R/W	DAC DATA [7:0]	0x00
DAC_DATA 2	0x0D	R/W	DAC DATA [11:8]	0x20
DAC_CTRL	0x0E	R/W	DAC CTRL	0xA5
PGA_CTRL 1	0x0F	R/W	PGA Control	0x00
PGA_CTRL 2	0x10	R/W	PGA Control	0x40
ADC_OFFSET_CAL1	0x11	R/W	ADC Offset calibration data bits [7:0]	0x00
ADC_OSSFET_CAL2	0x12	R/W	ADC Offset calibration data bits [15:8]	0x00
ADC_OSSFET_CAL3	0x13	R/W	ADC Offset calibration data bits [23:16]	0x00
TEMP_SENSOR_CAL1	0x14	R/W	Temperature Sensor Calibration Data [7:0]	0x00
TEMP_SENSOR_CAL2	0x15	R/W	Temperature Sensor Calibration Data [15:8]	0x00
TEMP_SENSOR_CAL3	0x16	R/W	Temperature Sensor Calibration Data [23:16]	0x00
STATUS	0x17	R/C	Status	0x06
MISC	0x1E	R/W	Miscellaneous Control	0x00
VER_NUM_24BADC_ID	0x1F	R	Device ID Register	0xDA

Table 6.3-2 Register Map

6.3.4 Register Description

Power Down Control Register 1 (PWD_CTRL 1)

Register	Address	R/W	Description	Reset Value
PWD_CTRL 1	0x00	R/W	Power Down Control Register 1	0x00

7	6	5	4	3	2	1	0
PWD_DACBUF	PWD_DAC	PWD_OSC	PWD_VCMGEN	PWD_TEMPSENSOR	PWD_ADC_INT_REF	PWD_POR18	PWD_POR33

Bits	Description	
[7]	**PWD_DACBUF**	**Power Down DAC Buffer Block** 0 = Power up. 1 = Power down. **Note 1:** This bit is ignored if register PWD_CTRL 2 bit 7 is set. **Note 2:** This bit must be set for TSSOP-20.
[6]	**PWD_DAC**	**Power Down DAC Block** 0 = Power up. 1 = Power down. **Note 1:** This bit is ignored if register PWD_CTRL 2 bit 7 is set. **Note 2:** This bit must be set for TSSOP-20.
[5]	**PWD_OSC**	**Power Down Internal Oscillation Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[4]	**PWD_VCMGEN**	**Power Down VCM Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[3]	**PWD_TEMPSENSOR**	**Power Down Temperature Sensor Block** 0 Power up 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[2]	**PWD_ADC_INT_REF**	**Power down Internal Reference Voltage block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[1]	**PWD_POR18**	**Power Down POR18 Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.

Bits	Description	
[0]	**PWD_POR33**	**Power Down POR33 Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.

Power Down Control Register 2 (PWD_CTRL 2)

Register	Address	R/W	Description	Reset Value
PWD_CTRL 2	0x01	R/W	Power Down Control Register 2	0x80

7	6	5	4	3	2	1	0
PWD_CHIP	PWD_BG	PWD_LDO18	PWD_MOD	PWD_PGA	PWD_PGA_BUFF	PWD_MOD_REFP	PWD_MOD_REFN

Bits	Description	
[7]	**PWD_CHIP**	**Whole Chip Power Down** 0 = Power up. 1 = Power down. **Note:** This bit set after power-up reset.
[6]	**PWD_BG**	**Power Down Band-Gap Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[5]	**PWD_LDO18**	**Power Down LDO18 Block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[4]	**PWD_MOD**	**Power down Modulator block** 0 = Power up. 1 = Power down. **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[3]	**PWD_PGA**	**Power Down PGA Block** 0 = Power up. 1 = Power down. **Note 1:** This bit is ignored if register PWD_CTRL 2 bit 7 is set. **Note 2:** This bit is set/reset automatically if PGA CTRL 1 bit 0 (**PGA_BYPASS**) is set/reset
[2]	**PWD_PGA_BUFF**	**Power Down PGA Bandwidth Buffer Block** 0 = Power up. 1 = Power down. **Note 1:** This bit is ignored if register PWD_CTRL 2 bit 7 is set. **Note 2:** This bit is set/reset automatically if PGA CTRL 2 bit 5 (**PGA_BUF_BYPASS**) is set/reset
[1]	**PWD_MOD_REFP**	**Power Down Modulator REFP Buffer Block** 0 = Power up. 1 = Power down (ADC_REFP input buffer is by-passed). **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.
[0]	**PWD_MOD_REFN**	**Power Down Modulator REFN Buffer Block** 0 = Power up. 1 = Power down (ADC_REFN input buffer is by-passed). **Note:** This bit is ignored if register PWD_CTRL 2 bit 7 is set.

Digital Filter Control Register 1 (DF_CTRL 1)

Register	Address	R/W	Description	Reset Value
DF_CTRL 1	0x02	R/W	Digital Filter Control Register 1	0x05

7	6	5	4	3	2	1	0
DF_GAIN		Reserved	BYPASS_FIR	OSR_SEL			

Bits	Description	
[7:6]	**DF_GAIN**	**Digital Filter Gain Control** 00 = 1x gain. 01 = 2x gain. 10 = 4x gain. 11 = 8x gain.
[5]	**Reserved**	Reserved.
[4]	**BYPASS_FIR**	**Bypass FIR Filter Control** 0 = Not bypass. 1 = Bypass FIR Filter. **Note 1:** ADC sampling rate must be 32 times or higher than input signal frequency when FIR filter is enable. **Note 2:** This bit must be set when data rate is set above 4000SPS if 8.192 MHz clock is applied.
[3:0]	**OSR_SEL**	**Select ADC Filter Oversampling Rate (OSR)** 0000 = OSR 32768. 0001 = OSR 16384. 0010 = OSR 8192. 0011 = OSR 4096. 0100 = OSR 2048. 0101 = OSR 1024 (default). 0110 = OSR 512. 0111 = OSR 256. 1000 = OSR 128. 1001 = OSR 64.

Digital Filter Control Register 2 (DF_CTRL 2)

Register	Address	R/W	Description	Reset Value
DF_CTRL 2	0x03	R/W	Digital Filter Control Register	0x22

7	6	5	4	3	2	1	0
FIRCOEFS	AVG_FILT_EN	AVG_FILT_SET		LOW_LAT_EN	AVG_ADAP_EN	AVG_ADAP_SET	

Bits	Description	
[7]	**FIRCOEFS**	**FIR Coefficient Select** 0 = Fix FIR coefficient. 1 = User defined FIR coefficient. **Note:** if FIRCOEFS is 1, user should fill FIN coefficient manually before ADC start conversion.
[6]	**AVG_FILT_EN**	**Enable Extra Average Filter for Low Frequency Signal** 0 = Average filter Disabled (default). 1 = Average filter Enabled.
[5:4]	**AVG_FILT_SET**	**Extra Average Filter Setting for Low Frequency Signal** 00 = Bypass. 01 = Avg 1/2. 10 = Avg 1/4 (default). 11 = Avg 1/16.
[3]	**LOW_LAT_EN**	**Digital Filter Low Latency Time Enable** 0 = Digital filter Disabled (default). 1 = Digital filter Enabled.
[2]	**AVG_ADAP_EN**	**Enable of Adaptive Bandwidth Control for the Average Filter** 0 = Adaptive bandwidth control Disabled (default). 1 = Adaptive bandwidth control Enabled.
[1:0]	**AVG_ADAP_SET**	**Strength of Adaptive Bandwidth Control for the Average Filter** 00 = Strength weakest. 01 = Strength low. 10 = Strength medium (default). 11 = Strength high.

ADC Control Register (ADC CTRL)

Register	Address	R/W	Description	Reset Value
ADC_CTRL	0x04	R/W	ADC Control Register	0x06

7	6	5	4	3	2	1	0
SETLSEL			ADC_MOD_CLEAR	ADC_CLK_SET		MOD_REFPN_GAIN_SET	

Bits	Description	
[7:5]	**SETLSEL**	**ADC Settling Time Selection** 000 = First ADC sinc filter output data is valid when ADC enters conversion mode from standby mode. 001 = First ADC sinc filter output data is waived when ADC enters conversion mode from standby mode. 010 = First three ADC sinc filter output data are waived when ADC enters conversion mode from standby mode. 011 = First five ADC sinc filter output data are waived when ADC enters conversion mode from standby mode. 100 = First six ADC sinc filter output data are waived when ADC enters conversion mode from standby mode. 101 = First seven ADC sinc filter output data are waived when ADC enters conversion mode from standby mode. 110 = First eight ADC sinc filter output data are waived when ADC enters conversion mode from standby mode. 111 = First nine ADC sinc filter output data are waived when ADC enters conversion mode from standby mode.
[4]	**ADC_MOD_CLEAR**	**Clear the ADC Modulator Voltage** 0 = Not clear (default). 1 = Clear. **Note:** This bit is used to shorten response time after channel changed (Using STOP command to reset digital filter, FIR and clear ADC modulator voltage is necessary)
[3:2]	**ADC_CLK_SET**	**Select the ADC Modulator Clock (When Internal RC Clock or External Clock Frequency = 8.192 MHz)** 10 = 512 kHz 11 = 1.024 MHz
[1:0]	**MOD_REFPN_GAIN_SET**	**Select the Modulator Reference P/N Gain Setting** 00 = 0.25X modulator reference voltage. 01 = 0.5X modulator reference voltage. 10 = 1X modulator reference voltage (default). 11 = 1X modulator reference voltage. **Note 1:** Both PWD_MOD_REFP and PWD_MOD_REFN of PWD_CTRL 2 must be reset when 0.25X or 0.5X modulator reference voltage is selected. **Note 2:** Buffers is by-passed when both PWD_MOD_REFP and PWD_MOD_REFN of PWD_CTRL 2 are set.

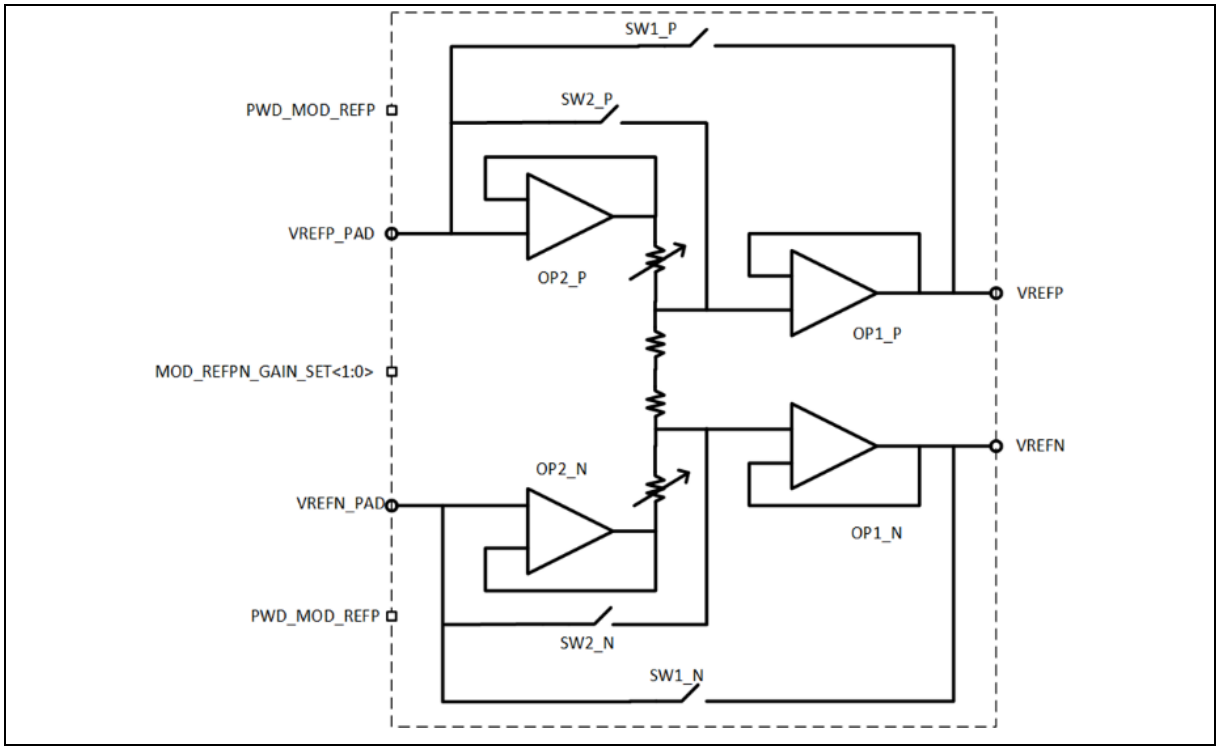


Figure 6.3-1 Block Diagram of ADC_REFP/ADC_REFN Buffers

Bias Control Register 1 (BIAS CTRL 1)

Register	Address	R/W	Description	Reset Value
BIAS_CTRL 1	0x05	R/W	Bias Control Register 1	0xFD

7	6	5	4	3	2	1	0
LDO_BIAS_SET	VCM_BIAS_SET	MOD_REFP_BIAS_SET	MOD_REFN_BIAS_SET	DAC_REF_BIAS_SET	REF_BIAS_SET	PGA_BIAS_SET	

Bits	Description	
[7]	LDO_BIAS_SET	**Set 1.8V LDO Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[6]	VCM_BIAS_SET	**Set VCM Block Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[5]	MOD_REFP_BIAS_SET	**Set Modulator Reference P Block Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[4]	MOD_REFN_BIAS_SET	**Set Modulator Reference N Block Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[3]	DAC_REF_BIAS_SET	**Set DAC Reference Buffer Block Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[2]	REF_BIAS_SET	**Set 1.2V/2.4V Reference Buffer Block Bias Current** 0 = 0.5x bias current. 1 = 1x bias current (default).
[1:0]	PGA_BIAS_SET	**Set PGA Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.

Bias Control Register 2 (BIAS CTRL 2)

Register	Address	R/W	Description	Reset Value
BIAS_CTRL 2	0x06	R/W	Bias Control Register 2	0x55

7	6	5	4	3	2	1	0
PGA_BUFF_BIAS_SET		ADC_BIAS_SET		ADC_OP1_BIAS_SET		ADC_OP2_BIAS_SET	

Bits	Description	
[7:6]	PGA_BUFF_BIAS_SET	**Set PGA Buffer Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.
[5:4]	ADC_BIAS_SET	**Set ADC Modulator Whole Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.
[3:2]	ADC_OP1_BIAS_SET	**Set ADC Modulator Op-Amp 1 Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.
[1:0]	ADC_OP2_BIAS_SET	**Set ADC Modulator Op-Amp 2 Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.

Chop Control Register (CHOP CTRL)

Register	Address	R/W	Description	Reset Value
CHOP_CTRL	0x07	R/W	Chop Control Register	0x01

7	6	5	4	3	2	1	0
DIS_DAC_BUF_CHOP	DIS_MOD_REFPN_CHOP	DIS_PGA_BUFF_CHOP	DIS_PGA_CHOP	DIS_MOD_CHOP	Reserved	DIS_INT_REF_CHOP	DIS_BG_CHOP

Bits	Description	
[7]	**DIS_DAC_BUF_CHOP**	**DAC Buffer Chopper** 0 = DAC buffer chopper Enabled. (default). 1 = DAC buffer chopper Disabled.
[6]	**DIS_MOD_REFPN_CHOP**	**ADC Modulator Reference P/N Buffer Chopper** 0 = ADC modulator reference P/N buffer chopper Enabled (default). 1 = ADC modulator reference P/N buffer chopper Disabled.
[5]	**DIS_PGA_BUFF_CHOP**	**PGA Bandwidth Buffer Chopper** 0 = PGA bandwidth buffer chopper Enabled (default). 1 = PGA bandwidth buffer chopper Disabled.
[4]	**DIS_PGA_CHOP**	**PGA Chopper Mode** 0 = PGA chopper mode Enabled. 1 = PGA chopper mode Disabled.
[3]	**DIS_MOD_CHOP**	**Modulator Chopper Mode** 0 = Modulator chopper mode Enabled. 1 = Modulator chopper mode Disabled.
[2]	**Reserved**	Reserved.
[1]	**DIS_INT_REF_CHOP**	**Internal Reference Voltage Chopper Mode** 0 = Internal Reference Voltage chopper mode Enabled. 1 = Internal Reference Voltage chopper mode Disabled.
[0]	**DIS_BG_CHOP**	**Band-Gap Chopper Mode** 0 = Band-gap chopper mode Enabled. 1 = Band-gap chopper mode Disable.

Band-gap Control Register 1 (BG CTRL 1)

Register	Address	R/W	Description	Reset Value
BG_CTRL 1	0x08	R/W	Band-gap Control Register 1	0x77

7	6	5	4	3	2	1	0
SEL_BG_OUT				SEL_BG_NTAT			

Bits	Description	
[7:4]	SEL_BG_OUT	**Band-Gap Voltage Level Control Bits [3:0]** These are trim bits for VBG and internal V_{REF}=1.2V (Default value from OTP).
[3:0]	SEL_BG_NTAT	**Band-Gap NTAT Control Bits [3:0]** These are temperature drift trim bits for VBG and internal V_{REF}=1.2V (Default value from OTP).

Internal Oscillator Control Register 1 (OSC CTRL 1)

Register	Address	R/W	Description	Reset Value
OSC_CTRL1	0x09	R/W	Internal Oscillator Control Register 1	0x00

7	6	5	4	3	2	1	0
OSC_TRIM[7:0]							

Bits	Description	
[7:0]	**OSC_TRIM[7:0]**	**Internal Oscillator Frequency Trim Bits [7:0] (Default Value from OTP)**

Internal Oscillator Control Register 2 (OSC CTRL 2)

Register	Address	R/W	Description	Reset Value
OSC_CTRL2	0x0A	R/W	Internal Oscillator Control Register	0x86

7	6	5	4	3	2	1	0
SEL_INT_OSC	Reserved	SEL_INT_OSC_F		OSC_BIAS		OSC_TRIM[9:8]	

Bits	Description	
[7]	**SEL_INT_OSC**	**Select Internal Oscillator Clock** 0 = Select external input clock. 1 = Select Internal oscillator clock.
[6]	**Reserved**	Reserved.
[5:4]	**SEL_INT_OSC_F**	**Select Internal Oscillator Clock Frequency** 00 = 8.192 MHz (default). 01 = 16.384 MHz. 10 = 24.576 MHz. 11 = 49.152 MHz.
[3:2]	**OSC_BIAS**	**Set Internal Oscillator Bias Current** 00 = 0.5x bias current. 01 = 1x bias current (default). 10 = 2x bias current. 11 = 3x bias current.
[1:0]	**OSC_TRIM[9:8]**	**Internal Oscillator Frequency Trim Bits [9:8] (Default Value from OTP)**

Reference Voltage Control Register (V_{REF} CTRL)

Register	Address	R/W	Description	Reset Value
VREF_CTRL	0x0B	R/W	Reference Voltage Control Register	0x9F

7	6	5	4	3	2	1	0
SEL_INT_REF_DRV		SEL_INT_REF				EN_CAPLESS	SEL_24V_INT_REF

Bits	Description	
[7:6]	SEL_INT_REF_DRV	**Select Internal Reference Voltage Driving Strength** 00 = Lowest drive strength. 01 = Medium low drive strength. 10 = Medium high drive strength (default, 10mA). 11 = Highest drive strength.
[5:2]	SEL_INT_REF	**Select Internal V_{REF}=2.4 Trim Value (Default Value from OTP)**
[1]	EN_CAPLESS	**Enable 1.8V LDO as Capless** 0 = Use external decoupling Cap. 1 = Capless.
[0]	SEL_24V_INT_REF	**Voltage Reference Level Control** 0 = Select V_{REF}=1.2V. 1 = Select V_{REF}=2.4V.

PGA Control Register 1 (PGA CTRL 1)

Register	Address	R/W	Description	Reset Value
PGA_CTRL 1	0x0F	R/W	PGA Control Register	0x00

7	6	5	4	3	2	1	0
SEL_PGA_INN			SEL_PGA_INP			DIS_INMUX_DIG	PGA_BYPASS

Bits	Description	
[7:5]	**SEL_PGA_INN**	**PGA Input Negative MUX Select Control Bits [2:0]** 000 = ADC_CH0. 001 = ADC_CH2. 010 = ADC_CH4. 011 = ADC_CH6. 100 = TP-. 101 = VBG. 110 = AIN_COM. 111 = VCM.
[4:2]	**SEL_PGA_INP**	**PGA Input Positive MUX Select Control Bits [2:0]** 000 = ADC_CH1. 001 = ADC_CH3. 010 = ADC_CH5. 011 = ADC_CH7. 100 = TP+. 101 = DAC. 110 = AIN_COM. 111 = VCM.
[1]	**DIS_INMUX_DIG**	**PGA Input Mux Control** 0 = PGA input mux enabled and can select different input channel. 1 = PGA input mux is closed (all channels).
[0]	**PGA_BYPASS**	**Bypass PGA Control** 0 = Use PGA in signal path. 1 = PGA is bypassed in signal path.

PGA Control Register 2 (PGA CTRL 2)

Register	Address	R/W	Description	Reset Value
PGA_CTRL 2	0x10	R/W	PGA Control Register	0x40

7	6	5	4	3	2	1	0
OFFSETDIS	PGA_BUF_AUTO_EN	PGA_BUF_BYPASS	PGA_BUF_GAIN	PGA GAIN			DIS_DWA

Bits	Description	
[7]	**OFFSETDIS**	**ADC Output Data is always Subtracted by ADC_OCD Automatically** 0 = ADC offset calibration Enabled. 1 = ADC offset calibration Disabled.
[6]	**PGA_BUF_AUTO_EN**	**Auto Enable the PGA Bandwidth Buffer Depending on PGA High Gain** 0 = Manual mode setting of PGA buffer. 1 = Auto enable the PGA bandwidth buffer if PGA gain >=8 (default).
[5]	**PGA_BUF_BYPASS**	**Bypass PGA Bandwidth Buffer Control** 0 = Use PGA bandwidth buffer in signal path (default). 1 = PGA bandwidth buffer is bypassed in signal path.
[4]	**PGA_BUF_GAIN**	**PGA Bandwidth Buffer Gain Control** 0 = 1x gain (default). 1 = 2x gain.
[3:1]	**PGA_GAIN**	**Analog PGA Gain Control Bits [2:0]** 000 = 1x. 001 = 2x. 010 = 4x. 011 = 8x. 100 = 16x. 101 = 32x. 11x = 64x.
[0]	**DIS_DWA**	**DWA (Data Weighted Averaging) Control** 0 = DWA Enabled. 1 = DWA Disabled.

ADC Offset Calibration Data Register 1 (ADC OCD1)

Register	Address	R/W	Description	Reset Value
ADC OCD1	0x11	R/W	ADC Offset Calibration Data Register Bits [7:0]	0x00

7	6	5	4	3	2	1	0
ADC OCD1							

Bits	Description	
[7:0]	**ADC OCD1**	**ADC Offset Calibration Data Register Bits [7:0]**

Note: ADC Offset Calibration Data is a signed 24-bit data.

ADC Offset Calibration Data Register 2 (ADC OCD2)

Register	Address	R/W	Description	Reset Value
ADC OCD2	0x12	R/W	ADC Offset Calibration Data Register bits [15:8]	0x00

7	6	5	4	3	2	1	0
ADC OCD2							

Bits	Description	
[7:0]	**ADC OCD2**	**ADC Offset Calibration Data Register Bits [15:8]**

ADC Offset Calibration Data Register 3 (ADC OCD3)

Register	Address	R/W	Description	Reset Value
ADC OCD3	0x13	R/W	ADC Offset Calibration Data Register bits [23:16]	0x00

7	6	5	4	3	2	1	0
ADC OCD3							

Bits	Description	
[7:0]	**ADC OCD3**	**ADC Offset Calibration Data Register Bits [23:16]**

Temperature Sensor Calibration Data Register 1 (TS CD1)

Register	Address	R/W	Description	Reset Value
TS CD1	0x14	R/W	Temperature Sensor Calibration Data [7:0]	0x00

7	6	5	4	3	2	1	0
TS CD1							

Bits	Description	
[7:0]	**TS CD1**	**Temperature Sensor Calibration Data [7:0] (Default Value from OTP)**

Note: Temperature Sensor Calibration Data is a signed 24-bit data.

Temperature Sensor Calibration Data Register 2 (TS CD2)

Register	Address	R/W	Description	Reset Value
TS CD2	0x15	R/W	Temperature Sensor Calibration Data [15:8]	0x00

7	6	5	4	3	2	1	0
TS CD2							

Bits	Description	
[7:0]	TS CD2	Temperature Sensor Calibration Data [15:8] (Default Value from OTP)

Temperature Sensor Calibration Data Register 3 (TS CD3)

Register	Address	R/W	Description	Reset Value
TS CD3	0x16	R/W	Temperature Sensor Calibration Data [23:16]	0x00

7	6	5	4	3	2	1	0
TS CD3							

Bits	Description	
[7:0]	**TS CD3**	**Temperature Sensor Calibration Data [23:16] (Default Value from OTP)**

Status Register (STATUS)

Register	Address		R/W	Description	Reset Value
STATUS	0x17		R/W	Status Register	0x06

7	6	5	4	3	2	1	0
Reserved				SWRST	POR33	POR18	DRDY

Bits	Description	
[7:4]	**Reserved**	Reserved.
[3]	**SWRST**	**Software Reset Flag** 0 = No software reset. 1 = Software reset occurs. **Note:** This bit is cleared by write “1” to this bit.
[2]	**POR33**	**POR33 Reset Flag** 0 = No POR33 reset. 1 = POR33 reset occurs. **Note:** This bit is cleared by write “1” to this bit.
[1]	**POR18**	**POR18 Reset Flag** 0 = No POR18 reset. 1 = POR18 reset occurs. **Note:** This bit is cleared by write “1” to this bit.
[0]	**DRDY**	**Data Ready Flag** 0 = ADC output data is invalid. 1 = ADC output data is ready. **Note:** This bit is set/reset by ADC automatically.

6.4 Timing Diagram

Reset Timing

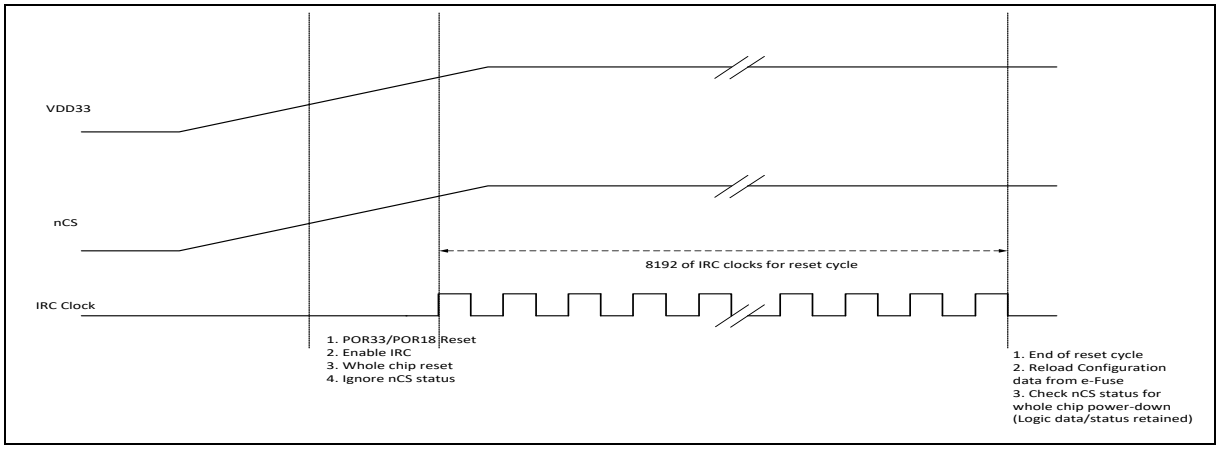


Figure 6.4-1 Reset Timing

SPI Interface Timing

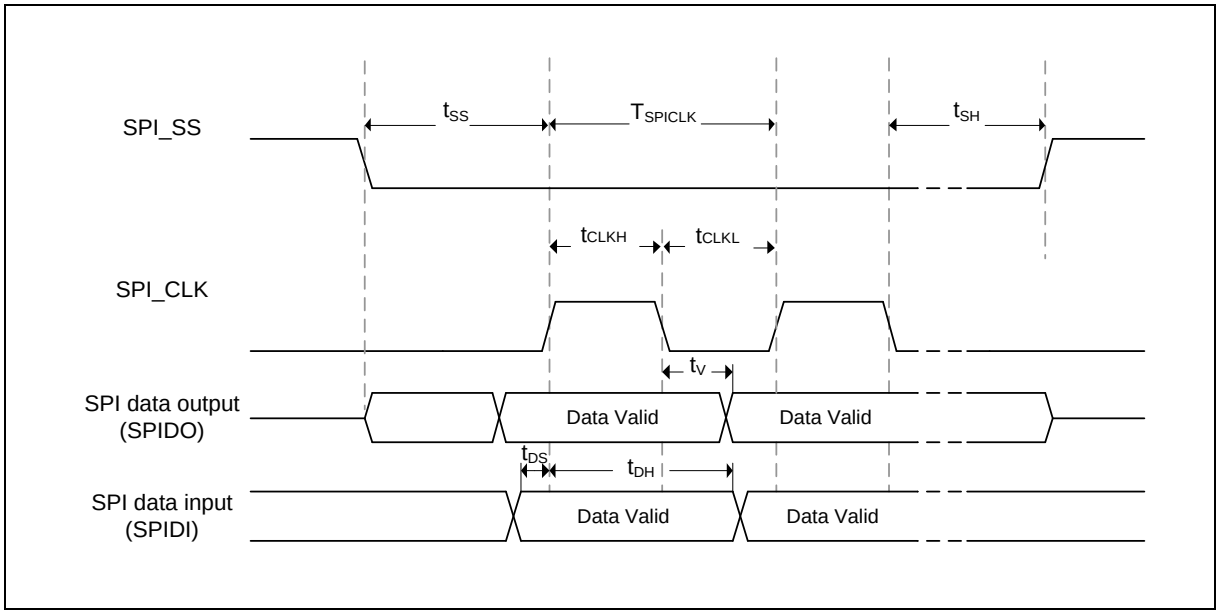


Figure 6.4-2 SPI Timing

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD} = 2.7V~3.6V					
T_{SPICLK}	SPI Clock Cycle Time	50			ns
t_{CLKH}	Clock output High time	25	T_{SPICLK} / 2		ns
t_{CLKL}	Clock output Low time	25	T_{SPICLK} / 2		ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3			ns
t_{SH}	Slave select hold time	1 T_{SPICLK}			ns

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
t_{DS}	Data input setup time	0			ns
t_{DH}	Data input hold time	5			ns
t_V	Data output valid time			15	ns

Table 6.4-1 SPI Interface Timing Table

Single Byte Command Timing

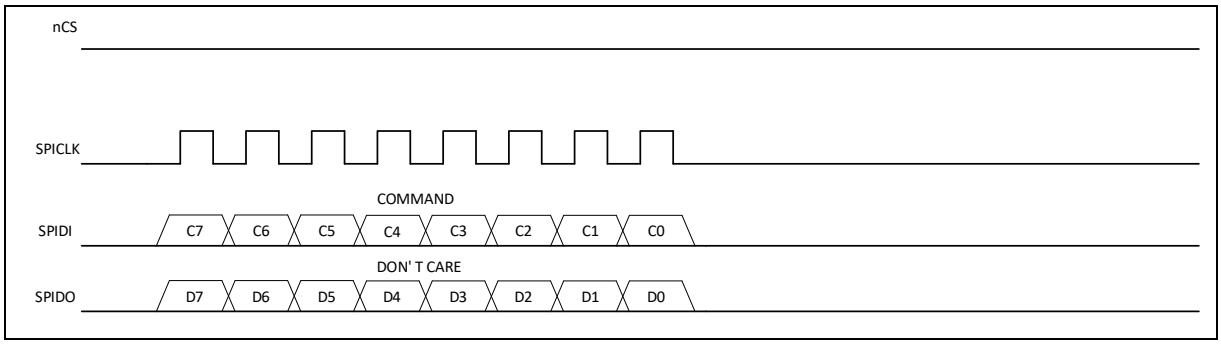


Figure 6.4-3 Single Byte Command Timing

Multiple Bytes Command Timing

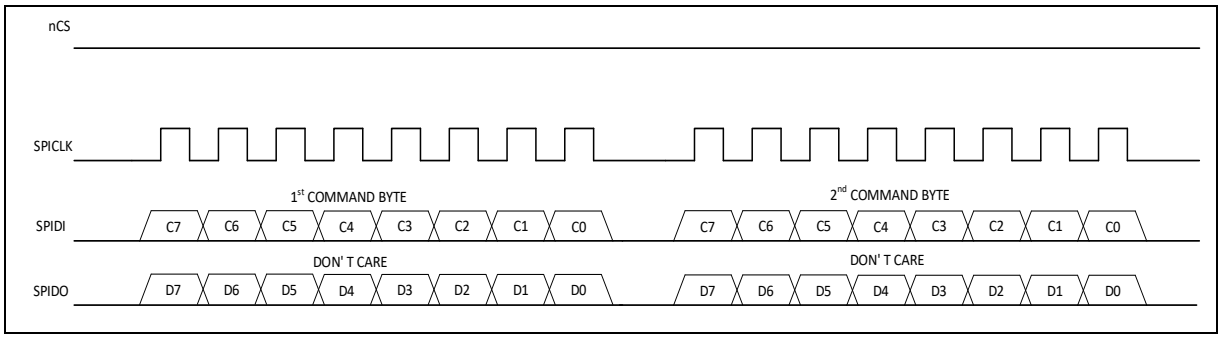


Figure 6.4-4 Multiple Byte Command Timing

Single Shot Conversion Mode Timing

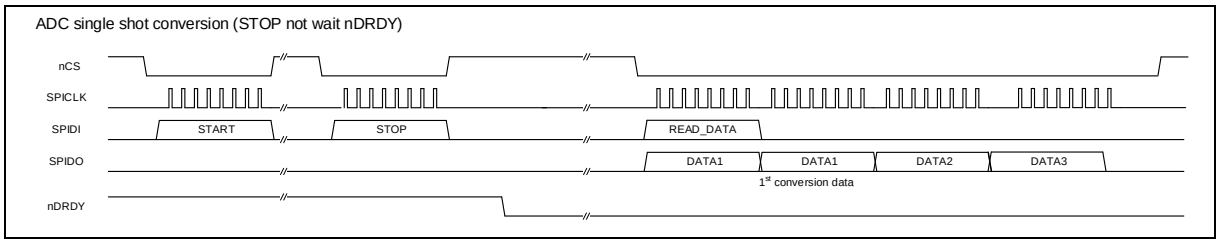


Figure 6.4-5 Single Shot Conversion Mode Timing

Single Shot Conversion Mode Timing with different settling time setting

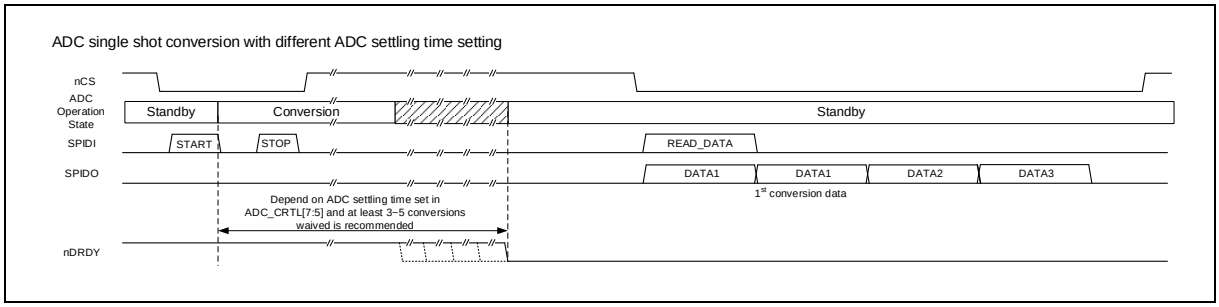
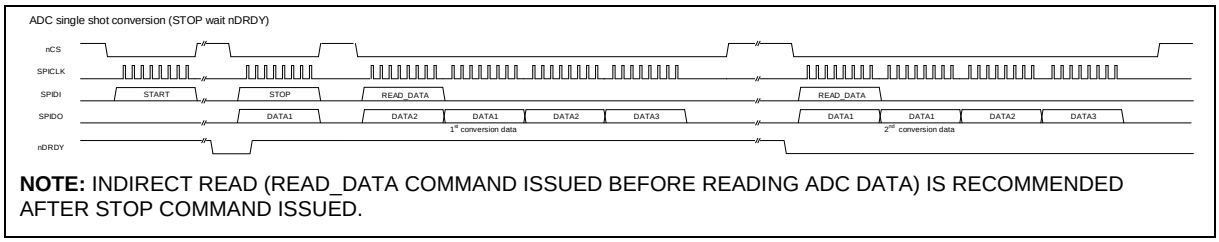


Figure 6.4-6.1 Single Shot Conversion Mode Timing with Different ADC Settling Time Setting



NOTE: INDIRECT READ (READ_DATA COMMAND ISSUED BEFORE READING ADC DATA) IS RECOMMENDED AFTER STOP COMMAND ISSUED.

Figure 6.4-7 Single Shot Conversion Mode Timing

Continuous Conversion Mode Timing

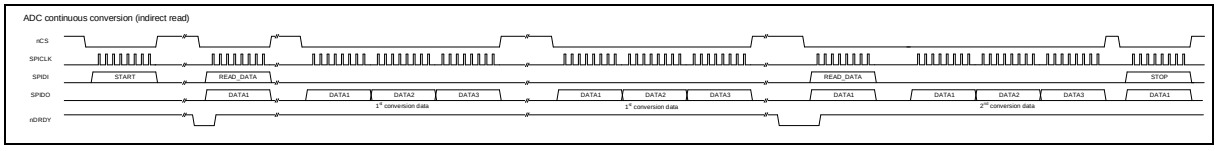
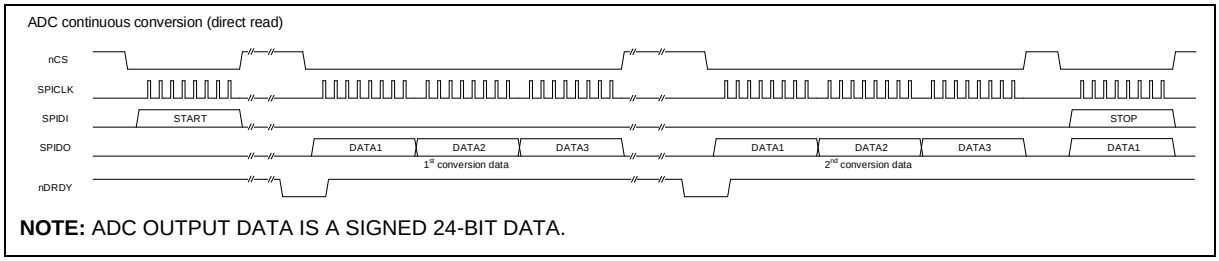


Figure 6.4-8 Continuous Conversion Mode Timing



NOTE: ADC OUTPUT DATA IS A SIGNED 24-BIT DATA.

Figure 6.4-9 Continuous Conversion Mode Timing (MS-Byte First)

Continuous Conversion Mode Timing Without Data Retrieved

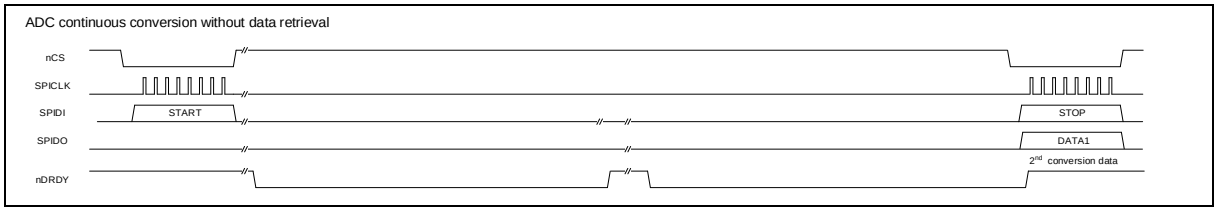


Figure 6.4-10 Continuous Conversion Mode Timing

ADC Offset Calibration Command

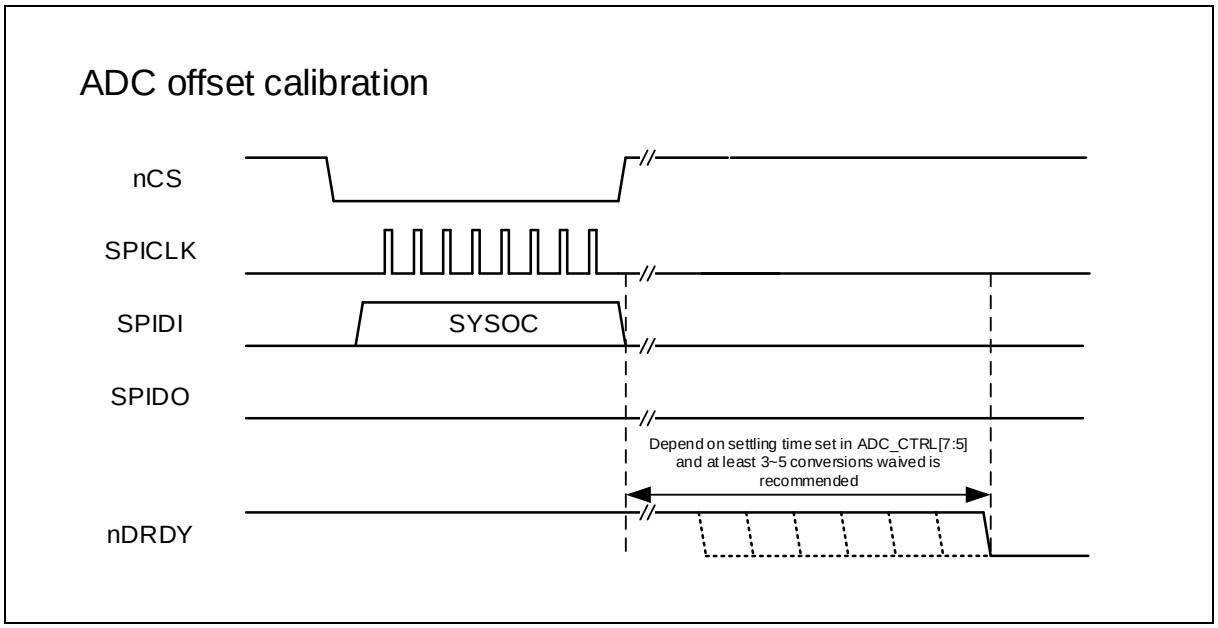


Figure 6.4-11 ADC Calibration Timing

Multiple Channel Scan Using Single Shot Conversion Mode Timing

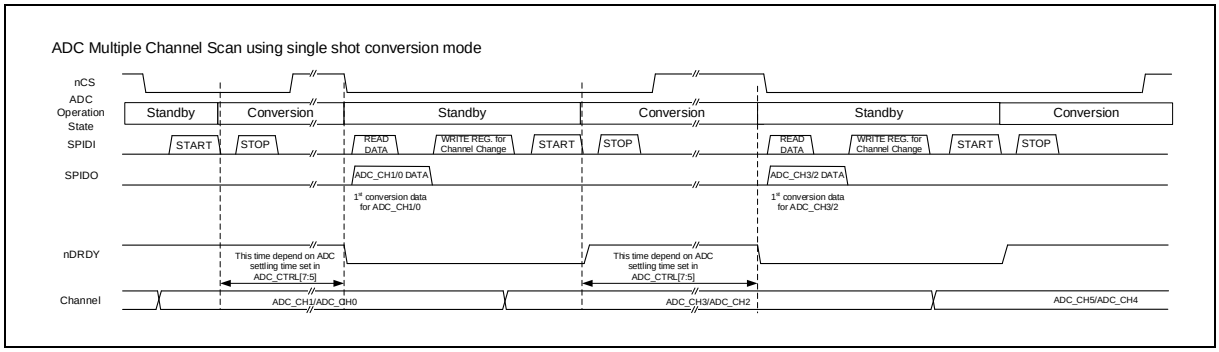


Figure 6.4-11.1 Multiple Channel Scan Using Single Shot Conversion Mode Timing

Channel Change In Continuous Conversion Mode Timing

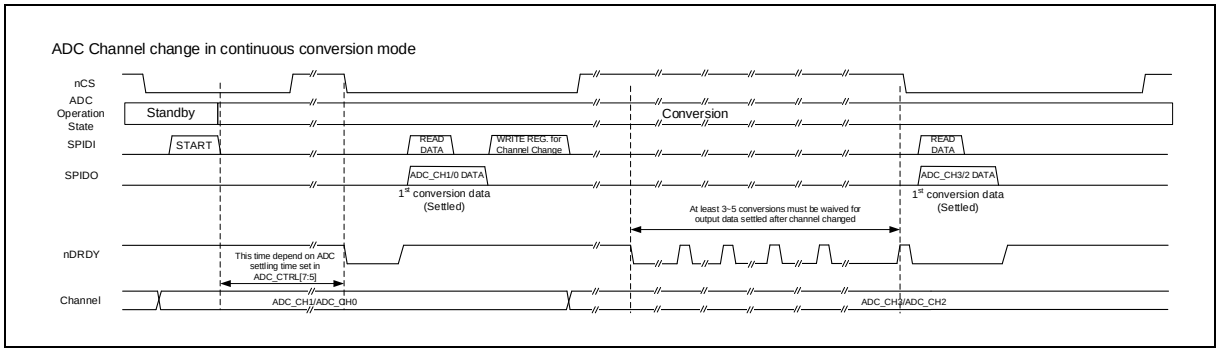


Figure 6.4-11.2 Channel Change In Continuous Conversion Mode Timing

OTP Read Cycle Timing

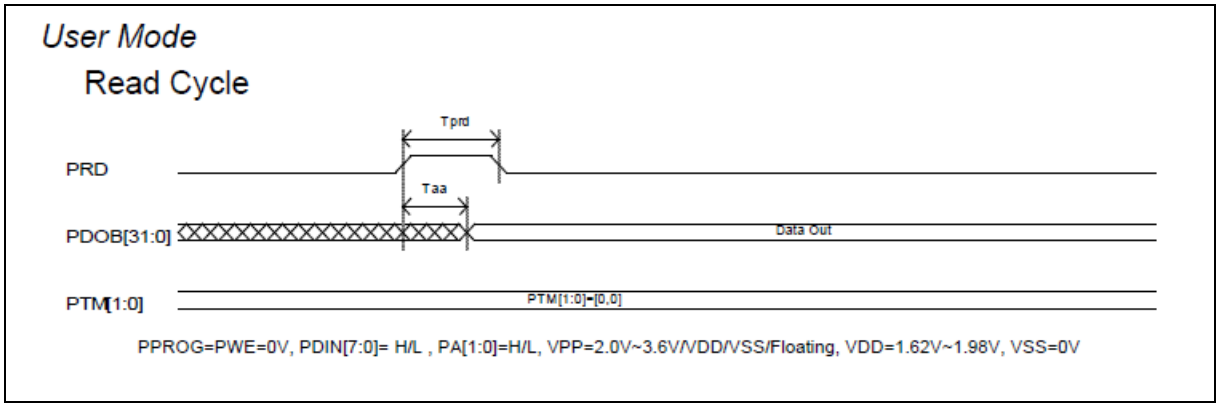


Figure 6.4-12 OTP Read Cycle Timing

OTP Program Cycle Timing

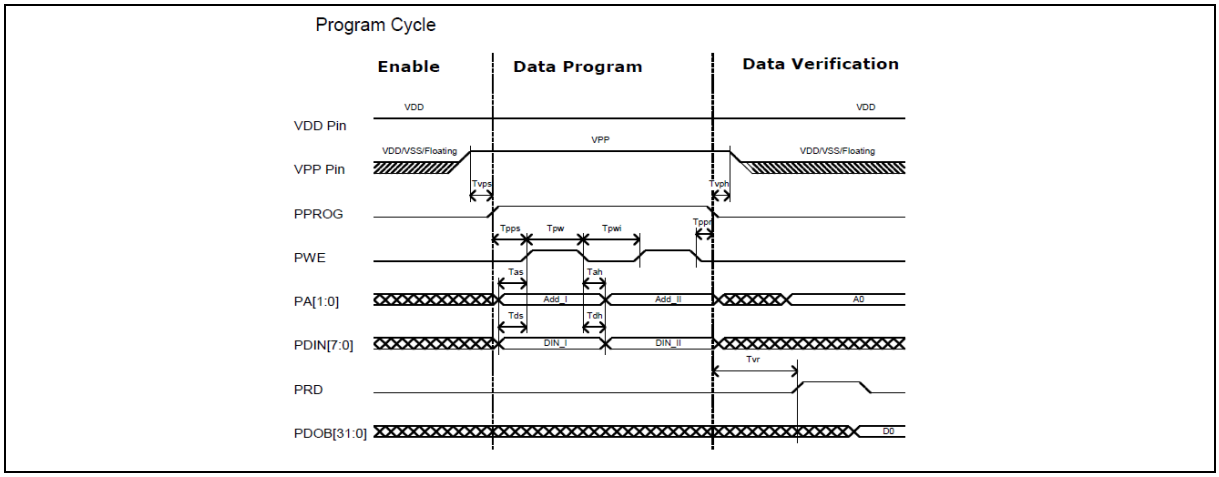


Figure 6.4-12 OTP Program Cycle Timing

Timing (T_J=-40°C to 125°C)
Timing Parameters (C_{LOAD}=1pf)

Parameter	Symbol	Min	Max	Unit
Rising Time	T_r	-	1	ns
Faling Time	T_f	-	1	ns
Read Data Access Time	T_{aa}	-	70	ns
Read Pulse Width Time	T_{prd}	200	50000	ns
Address Setup Time	T_{as}	4	-	ns
Address Hold Time	T_{ah}	9	-	ns
Data Setup Time	T_{ds}	4	-	ns
Data Hold Time	T_{dh}	9	-	ns
Program Mode Setup Time	T_{pps}	2	-	us
Program Mode Recovery Time	T_{ppr}	2	-	us
External VPP Setup Time	T_{vps}	10	-	ns

External VPP Hold Time	T_{vph}	10	-	ns
Program Pulse Width Time	T_{pw}	100	300	us
Program Pulse Interval Time	T_{pwi}	2	-	us
Program Recovery Time	T_{vr}	10	-	us
VDO Setup Time	T_{vds}	0	-	ns
VDO Recovery Time	T_{vdr}	0	-	ns
Control Signal Enable Time	T_{rst}	20	-	ns
PTM Mode Setup Time	T_{ms}	10	-	ns
PTM Mode Hold Time	T_{mh}	10	-	ns

Figure 6.4-13 OTP Timing Specification

6.5 ADC Operating Flow Chart

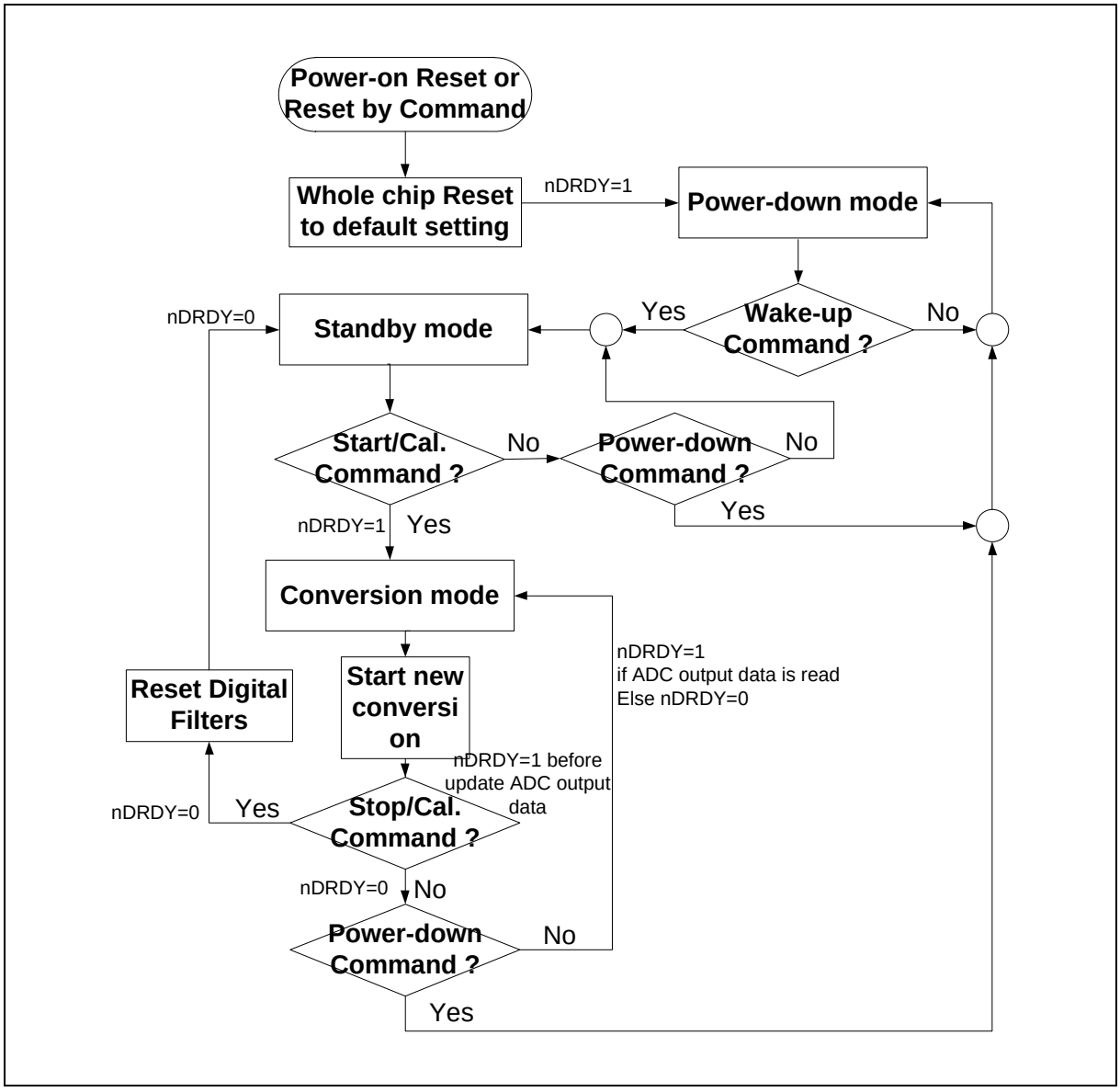


Figure 6.5-1 ADC Operating Flow Chart

Standby mode:

The device powers up in standby mode and automatically enters this mode whenever there is no ongoing conversion. In this mode the device is not active. This allows conversions to start immediately after receiving a START command. When the STOP command is sent, the device enters standby mode.

Conversion mode:

After receiving a START command, the ADC converts indefinitely until stopped by the STOP command. User cannot change any digital filter setting (DF_CTRL) under this mode.

Power-down mode:

Power-down mode is entered by receiving the POWER_DOWN command. In this mode, all analog and digital circuitry is powered down for lowest power consumption regardless of the register settings. All register values retain the current settings during power-down mode. A WAKE_UP command must be

issued in order to exit power-down mode and to enter standby mode.

To release the device from POWER_DOWN, issue the WAKE_UP command to enter standby mode. The device then waits for a START command to go into conversion mode.

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

7.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-VSS[*1]	DC power supply	-0.3	4.0	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	4.0	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply

Table 7.1-1 Voltage Characteristics

7.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into AV_{DD}/V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of AV_{SS}/V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 7.1-2 Current Characteristics

7.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	28	-	°C/Watt
	Thermal resistance junction-case 20-pin TSSOP(4.4x6.5 mm)	-	38	-	°C/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 7.1-3 Thermal Characteristics

7.1.4 EMC Characteristics

7.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits built into chips to avoid any damage that can be caused by typical levels of ESD.

7.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

7.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-4	-	+4	kV
V_{CDM}[*2]	Electrostatic discharge,charge device model	-750	-	+750	V
V_{MM}[*]	Electrostatic discharge,machine model	-300	-	+300	
LU[*3]	Pin current for latch-up[*3] Class II for max. Ta temperature	-100	-	+100	mA
V_{EFT}[*4]	Fast transient voltage burst	-4.4	-	+4.4	kV
V_{SYSESD}	System electrostatic discharge (contact mode)	-2	-	+2	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.
5. Determinded according to IEC 61000-4-6 standard and the performance class is class A.

Table 7.1-4 EMC Characteristics

ST severity level and behavior class

The IEC 61000-4-2 and IEC 61000-4-4 standards do not refer specifically to semiconductor components such as microcontrollers. Usually electromagnetic stress is applied on other parts of the system such as connectors, mains, supplies. The energy level of the F_ESD and FTB test decreases before reaching the microcontroller, governed by the laws of physics. A large amount of statistical data collected by ST on the behavior of MCUs in various application environments has been used to develop a correlation chart between ST F_ESD or FTB test voltage and IEC 61000-4-2/61000-4-4 severity levels (see Figure 7.1-5).

Severity level	ESD (IEC 61000-4-2) Equipment standard (kV)	FTB (IEC 61000-4-4) Equipment standard (kV)	ESD ST internal EMC test (kV)	FTB ST internal EMC test (kV)
1	2	0.5	S0.5	5 0.5
2	4	1	S 1	5 1
3	6	2	S 1.5	5 1.5
4	8	4	52	5 2.5
5(1)	>8	>4	NA	>2.5
Note: The severity level 5 has been introduced on December 14 2015. Older products might indicate level 4 even if level 5 might be passed.				

Table 7.1-5 ST ESD Severity Levels

7.1.5 Package Moisture Sensitivity (MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
20-pin TSSOP(4.4x6.5 mm) [*1]	MSL 3
33-pin QFN(4x4 mm) [*1]	MSL 3
Note: Determined according to IPC/JEDEC J-STD-020	

Table 7.1-6 Package Moisture Sensitivity (MSL)

7.1.6 Soldering Profile

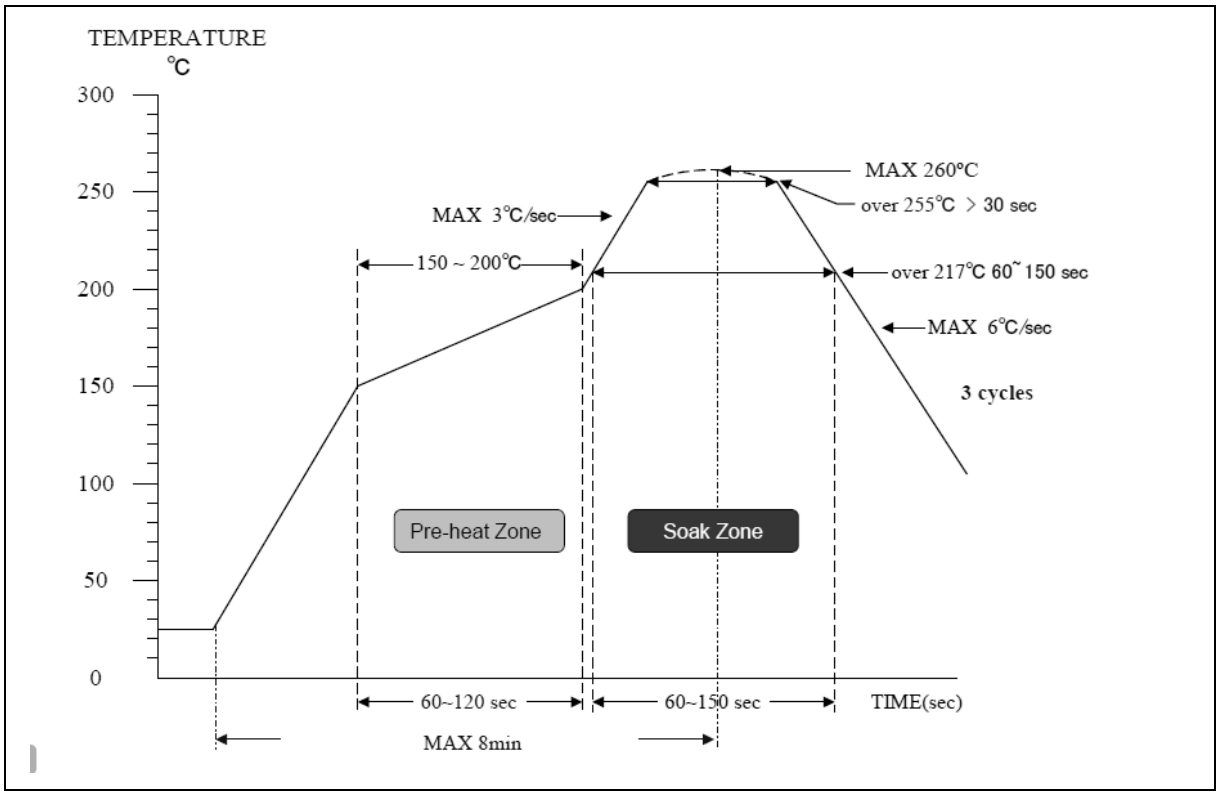


Figure 7.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec ax.
Time 25°C to peak temperature	8 min. max
Note: Determined according to J-STD-020C	

Table 7.1-7 Soldering Profile

7.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.7 ~ 3.6V, T_A = 25°C unless otherwise specified.)

General Operating Conditions						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Voltage (Normal Mode)	AV_{DD}	2.7	3.3	3.6	V	
	V_{DD}	2.7	3.3	3.6	V	
Operating Voltage (Over-driving Mode)	AV_{DD}	3.15	3.3	3.6	V	
	V_{DD}	3.15	3.3	3.6	V	
Temperature	T_A	-40	25	105	°C	
Operating Current (Normal Mode)	IAVDD		900	1100	uA	ADC+PGA only (Exclude HIRC) @3.6V, 105°C , default register setting
			1380	1750		ADC+PGA+HIRC @3.6V, 105°C, default register setting
			1780	2250		ADC+PGA+HIRC+ADC_REFP/ADC_REFN buffer @3.6V, 105°C, default register setting
Operating Current (Over-driving Mode)	$IAVDD_{-OD}$		4.8	5.5	mA	ADC+PGA only (Exclude HIRC) @3.6V, 105°C , over-driving mode register setting (CLK=49.152 MHz, ADC CLK=6.144 MHz, OSR=64, Data Rate=96 KSPS, Bias Current=Maximum)
			5.3	6.2		ADC+PGA+HIRC @3.6V, 105°C, over-driving mode register setting (CLK=49.152 MHz, ADC CLK=6.144 MHz, OSR=64, Data Rate=96 KSPS, Bias Current=Maximum)
			5.7	6.7		ADC+PGA+HIRC+ADC_REFP/ADC_REFN buffer @3.6V, 105°C, over-driving mode register setting (CLK=49.152 MHz, ADC CLK=6.144 MHz, OSR=64, Data Rate=96 KSPS, Bias Current=Maximum)
Operating Current	IDVDD		400	550	uA	ADC + SINC Filter only @3.6V, 105°C, default register setting
			500	600		ADC + SINC Filter +FIR Filter @3.6V, 105°C, default register setting
Operating Current (Over-driving Mode)	$IDVDD_{-OD}$		2.5	3	mA	ADC + SINC Filter only @3.6V, 105°C, default register setting
Power down current	I_{PD}		0.3	1	uA	T_A=25°C, 2.5~3.6V
				30		T_A=85°C, 2.5~3.6V
				50		T_A=105°C, 2.5~3.6V

Table 7.1-8 General Operating Conditions

7.3 Electrical Characteristics

(V_{DD}-V_{SS} = 2.7 ~ 3.6V, T_A = 25°C unless otherwise specified.)

7.3.1 Analog INPUT

(1) Design guarantee

Analog Input						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Analog Differential Input Impedance(1)	RDI		5		GΩ	With PGA
Input Capacitance(1)	CIN		5		pF	
Input Bandwidth(-3dB)	BW			1000	Hz	GAIN=1
PGA Gain Front	Gain	1		64	V/V	
PGA Band Width Buffer Gain	Gain	1		2	V/V	
Digital Filter Gain	Gain	1		8	V/V	
Input Reference Voltage Range (V_{ADC_REFP}-V_{ADC_REFN})	V_{ADC_REF}	1		2.4	V	
Input Reference Positive Voltage Range (V_{ADC_REFP})	V_{ADC_REFP}	V_{ADC_REFN}+1		2.4	V	
Input Reference Negative Voltage Range (V_{ADC_REFN})	V_{ADC_REFN}	0		V_{ADC_REFP}-1	V	
Analog Input Range	V_{ADC_IN}	**0.1**		V_{ADC_REF} *0.9/(PGA Gain)	V	V_{ADC_IN} = V_{AINP} or V_{AINN}
Analog Differential Input Range	$V_{ADC_DIFF_IN}$	-V_{ADC_REF} ***0.5**/(PGA Gain)		V_{ADC_REF} ***0.5**/(PGA Gain)	V	$V_{ADC_DIFF_IN}$ = V_{AINP}-V_{AINN}

Table 7.1-9 Electrical Characteristics

7.3.2 ADC

ADC Performance						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition (V_{ADC_REF}=2.4V if not noted)**
Sampling Frequency	FS			1.024	MHz	Normal mode (CLK=8.192 MHz)
				6.144		Over-driving mode (CLK=49.152 MHz)
Output Data Rate	FD	15.625		16000	SPS	Normal mode (CLK=8.192 MHz)
				96000		Over-driving mode (CLK=49.152 MHz)
Integral Non-linearity Error	INL		±15		ppm of FSR	With Calibration, GAIN=128
Offset Error	OE	-4.3		+0.15	ppm of FSR	With Calibration and 1024 samples
Offset Drift	OE_drift		±0.1		ppm of FSR/°C	With Calibration and 1024 samples
Gain Error	GE				%	
Gain Drift	GE_drift				ppm of FSR/°C	
Common Mode Rejection Ratio	CMRR		110		dB	
Power Supply Rejection Ratio	PSRR		80		dB	
Signal-to-Noise and Distortion Ratio	SINAD	89	91		dB	T_A=25°C
		80	81.5		dB	AV_{DD} = 2.7 ~3.6V; T_A = -40~ 105°C
Signal-to-Noise Ratio	SNR	90	91.5		dB	T_A=25°C
		80	81.5		dB	AV_{DD} = 2.7 ~3.6V; T_A = -40~ 105°C
Total Harmonic Distortion	THD		-90	-87	dB	
Start-up Time	T_{su}			200	uS	

Table 7.1-10 ADC Performace Characteristics

7.3.3 ADC Reference Voltage Input Buffer

ADC Reference Voltage Input Buffer						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Current	I_{OP}		400	500	µA	At T_A = 105°C, AV_{DD}=3.6V
Standby Current	I_{SB}		0.1	1	µA	When disable
Gain	G_{REFI}	0.25	0.5	1	V/V	T_A = -40 to + 105°C
Start-up Time	T_{su}			200	µS	

Table 7.1-11 ADC Reference Characteristics

7.3.4 Temperature Sensor

Internal Temperature Sensor						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Current	I_{OP}		30	60	µA	At T_A = 25°C, AV_{DD}=3.6V
Standby Current	I_{SB}		0.1	1	µA	When disable
Temperature Accuracy	TACC		±1	±2	°C	T_A = 0 to +85°C, 1 point Cal. +/-2° C, ADC CLK=500 kHz@250SPS & 10 conversions average
			±1	±3		T_A = -40 to +105°C, 1 point Cal. +/-3° C, ADC CLK=500 kHz@250SPS & 10 conversions average
Sensor Temperature Drift	ST_D		169.8		µV/°C	
Absolute Temperature Scale 0°K	K_T	-275	-273	-271	°C	(V_{BE1}-V_{BE2})=50.6mV @TT/25°C
Start-up Time	T_{su}			200	µS	

Table 7.1-12 Internal Temperature Characteristics

7.3.5 Internal Reference Voltage Generator

Internal Reference Voltage Generator						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Output Voltage without Loading	V_{REF}	1.188	1.2	1.212	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C, no loading, after trim Output voltage options: 2.4/1.2V
		2.376	2.4	2.424		
Output Voltage with +/-5mA Loading	$V_{REF-LOAD}$	1.188	1.2	1.212	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C, +/-5mA loading, +/-1% after trim Output voltage options: 2.4/1.2V
		2.376	2.4	2.424		
Output Voltage with +/-10mA Loading		1.182	1.2	1.218	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C, +/-10mA loading, +/-1.5% after trim Output voltage options: 2.4/1.2V
		2.364	2.4	2.436		
Band-gap Voltage	V_{BG}	1.188	1.2	1.212	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C, after trim, no load
Capacitor Loading	C_L		4.7		uF	X7R capactior
Operating Current	I_{VBGQ}		160	200	µA	
	I_VREF_Q		200	300	µA	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Standby Current	$I_VREF_{_SB}$		0.1	1	µA	When disable
Output Current	I_{DRV}	-10		10	mA	AV_{DD} =2.7~3.6V, T_A= -40~105°C
V_{REF}	$TRIM_VREF$		4		Bit	
	TC_VREF		100	160	ppm/°C	
VBG	$TRIM_{VBG}$		4		Bit	
	TC_{VBG}		100	160	ppm/°C	
Start-up Time	T_{su}			200	µS	Enable to reach target level+/-1%

Table 7.1-13 Internal V_{REF} Characteristics

7.3.6 HIRC 49.152 MHz

HIRC49.152M						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Voltage	AV_{DD}	2.7	3.3	3.6	V	
	VDD_{18}	1.6	1.8	2.0	V	
Temperature Range	T_j	-40	25	125	°C	
Current Consumption	I_{op}		480	650	µA	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Disable Current	I_{sb}			10	nA	OSCEN=0
Output Frequency	F_{osc}		49.152		MHz	
Frequency Drift	ΔF_{osc}		±0.125	±0.3	%	AV_{DD} =3.3V, 25°C
		-2		+2	%	AV_{DD} =2.7~3.6V, T_A= -40~105°C

Stable Time	T_{stable}			20	µs	To ±5% error of Fosc
Clock Duty	T_{duty}	45	50	55	%	
Trim Bit			5		bit	
Trim Range	F_{trim}	-15		+15	%	3.3V,25°C.Fmax@trim code=0.
Clock Jitter (peak-to-peak)	Jitter(p-p)			±2	%	AV_{DD} =2.7~3.6V, Ta= -40~105°C, FMOD=1.024 MHz, OSR=64 (Output Data Rate=16 KSPS), FIR enable

Table 7.1-14 HIRC 49.152 MHz Characteristics

7.3.7 POR33

POR33						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Voltage	AV_{DD}	1.3	3.3	3.6	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Operating junction temperature	T_j	-40	25	125	°C	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Power rising rate	T_r	10		∞	us/V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Power falling rate	T_f	10		∞	us/V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
POR33 power step down response time	T_{por}		5	10	us	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Release Threshold Voltage	V_{POR}	2.1		2.4	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
	V_{PDR}	2.0		2.3	V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Disable current	I_{DIS}		10	60	nA	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Operating current	I_{OP}		20	30	µA	AV_{DD} =2.7~3.6V, T_A= -40~105°C

Table 7.1-15 POR33 Characteristics

7.3.8 POR18

POR18						
Key Parameter	**Symbol**	**MIN**	**TYP**	**MAX**	**UNIT**	**Test Condition**
Operating Voltage	VDD_{18}	1.62	1.8	1.98	Volt	AV_{DD} =2.7~3.6V, T_A= -40~105°C
	AV_{DD}	1.8	3.3	3.6	Volt	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Operating junction temperature	T_j	-40	25	125	°C	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Power rising rate	T_r	10			us/V	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Release Threshold Voltage	V_{POR18}	1.2	1.4	1.6	Volt	AV_{DD} =2.7~3.6V, T_A= -40~105°C
	V_{PDR18}	1.1	1.3	1.5	Volt	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Disable current	I_{DIS}		1	20	nA	AV_{DD} =2.7~3.6V, T_A= -40~105°C
Operating current	I_{op}		15	20	uA	AV_{DD} =2.7~3.6V, T_A= -40~105°C

Figure 7.1-2 POR18 Characteristics

7.4 Typical Characteristics

7.4.1 24-bit ADC

ENOB with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=1.0, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On (except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	23.0317	22.1651	21.8606	21.1393	20.9585	20.2343	19.6603	18.6619	17.6815
62.5	16384	22.6586	21.6724	21.3830	20.7332	20.4388	19.7246	19.2015	18.1932	17.1667
125	8192	22.2182	21.1822	20.9240	20.2613	19.9841	19.2642	18.6693	17.7177	16.7120
250	4096	21.7628	20.7114	20.4294	19.7604	19.4679	18.7555	18.1930	17.1645	16.1906
500	2048	21.2628	20.2215	19.9364	19.2840	18.9430	18.2521	17.6805	16.6776	15.7025
1000	1024	20.7627	19.6581	19.4309	18.8323	18.4651	17.7768	17.1640	16.2151	15.1776
2000	512	20.2465	19.1939	18.9152	18.2812	17.9628	17.2637	16.6269	15.7109	14.7138
4000	256	19.7511	18.6882	18.3964	17.8087	17.4831	16.7523	16.1791	15.2383	14.2102
8000	128	19.2646	18.1860	17.8819	17.3229	16.9693	16.2542	15.6396	14.7158	13.7326
16000	64	18.6176	17.9587	17.4235	16.7689	16.4639	15.7814	15.1699	14.1778	13.1965

Figure 7.1-3 ENOB (V_{REF} Gain=1.0)

ENOB with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=0.5, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	22.1263	21.1275	20.8680	20.2607	19.9816	19.2711	18.6930	17.6512	16.7557
62.5	16384	21.6737	20.6574	20.4143	19.7198	19.4687	18.7235	18.2086	17.2238	16.1605
125	8192	21.2356	20.2153	19.8910	19.1989	18.9548	18.2592	17.6955	16.6864	15.6942
250	4096	20.7776	19.6854	19.4024	18.7271	18.4567	17.7465	17.2179	16.2010	15.2471
500	2048	20.2736	19.2029	18.8903	18.2126	17.9841	17.2367	16.6618	15.6715	14.6908
1000	1024	19.8100	18.6998	18.4404	17.7326	17.4719	16.7888	16.1654	15.1783	14.1966
2000	512	19.2763	18.2154	17.8884	17.2275	16.9656	16.2388	15.6702	14.7387	13.6857
4000	256	18.7688	17.7329	17.4439	16.7673	16.4983	15.6963	15.1633	14.1802	13.1800
8000	128	18.3280	17.2006	16.9406	16.2014	15.9234	15.2670	14.6721	13.6467	12.7013
16000	64	17.7314	16.7135	16.4233	15.7355	15.5046	14.7780	14.1728	13.2007	12.1841

Figure 7.1-4 ENOB (V_{REF} Gain=0.5)

ENOB with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=0.25, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	21.1658	20.1744	19.8662	19.1542	18.9258	18.2847	17.6214	16.7258	15.7021
62.5	16384	20.6356	19.7217	19.4271	18.6930	18.5124	17.7669	17.1979	16.1794	15.1841
125	8192	20.3022	19.2194	18.9082	18.2762	17.9845	17.2696	16.6780	15.7436	14.6839
250	4096	19.7837	18.7408	18.4071	17.7690	17.4746	16.7256	16.1561	15.2065	14.2002
500	2048	19.3299	18.2026	17.9175	17.1879	16.9714	16.2384	15.6784	14.6843	13.7314
1000	1024	18.7936	17.7319	17.4344	16.7747	16.4969	15.7520	15.1652	14.2139	13.2166
2000	512	18.1237	17.2319	16.8719	16.2238	16.0077	15.2175	14.6478	13.6921	12.6982
4000	256	17.8028	16.6670	16.2839	15.7635	15.4700	14.7754	14.1640	13.2206	12.1986
8000	128	17.3280	15.7212	15.9410	15.2565	14.9934	14.2668	13.6880	12.7237	11.7332
16000	64	16.7845	15.7157	15.3973	14.7392	14.4965	13.8145	13.1537	12.1968	11.2155

Figure 7.1-5 ENOB (V_{REF} Gain=0.25)

ENOB with OSR/Gain at V_{DD}=AV_{DD}=3.15V, V_{REF}=2.4V, V_{REF} Gain=Bypass/1, CLK=49.152 MHz, ADCCLK=6.144 MHz, Bias Current=0xFD&0xFA, Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Reat (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
24000	256	19.3679	18.2963	18.0616	17.5436	16.2377	15.9709	15.5607	14.7954	13.7843
48000	128	18.9197	17.7864	17.5720	17.1125	15.7970	15.5005	15.1057	14.2759	13.2560
96000	64	18.3557	17.3295	17.0471	16.5652	15.3606	15.0423	14.6297	13.7777	12.8209

Figure 7.1-6 ENOB (Over driving mode)

RSM (Noise)uV with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=1.0, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	0.5598	0.5103	0.3151	0.2598	0.1472	0.1216	0.0905	0.0904	0.0892
62.5	16384	0.7250	0.7181	0.4388	0.3442	0.2111	0.1731	0.1244	0.1251	0.1274
125	8192	0.9838	1.0086	0.6032	0.4774	0.2893	0.2382	0.1799	0.1740	0.1747
250	4096	1.3489	1.3979	0.8498	0.6756	0.4137	0.3389	0.2503	0.2553	0.2507

500	2048	1.9076	1.9630	1.1960	0.9399	0.5953	0.4805	0.3570	0.3577	0.3516
1000	1024	2.6980	2.9009	1.6978	1.2855	0.8290	0.6679	0.5107	0.4930	0.5059
2000	512	3.8587	4.0020	2.4274	1.8835	1.1743	0.9532	0.7411	0.6992	0.6978
4000	256	5.4395	5.6821	3.4780	2.6133	1.6375	1.3588	1.0108	0.9702	0.9893
8000	128	7.6210	8.0480	4.9683	3.6595	2.3380	1.9190	1.4691	1.3936	1.3775
16000	64	11.9341	9.4213	6.8265	5.3729	3.3189	2.6632	2.0345	2.0234	1.9973

Figure 7.1-7 RMS (V_{REF} Gain=1.0)

RSM (Noise)uV with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=0.5, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	1.0485	1.0476	0.6270	0.4776	0.2898	0.2371	0.1770	0.1822	0.1694
62.5	16384	1.4348	1.4511	0.8587	0.6949	0.4135	0.3465	0.2476	0.2450	0.2560
125	8192	1.9440	1.9715	1.2342	0.9970	0.5904	0.4781	0.3533	0.3556	0.3536
250	4096	2.6703	2.8466	1.7317	1.3827	0.8339	0.6821	0.4920	0.4978	0.4821
500	2048	3.7869	3.9772	2.4696	1.9753	1.1571	0.9712	0.7234	0.7185	0.7090
1000	1024	5.2218	5.6367	3.3734	2.7549	1.6503	1.3248	1.0204	1.0113	0.9986
2000	512	7.5597	7.8857	4.9458	3.9097	2.3441	1.9397	1.4384	1.3716	1.4230
4000	256	10.7462	11.0172	6.7306	5.3789	3.2408	2.8251	2.0438	2.0200	2.0203
8000	128	14.5872	15.9337	9.5404	7.9623	4.8271	3.8043	2.8728	2.9238	2.8154
16000	64	22.0571	22.3329	13.6544	10.9973	6.4531	5.3393	4.0610	3.9831	4.0292

Figure 7.1-8 RMS (V_{REF} Gain=0.5)

RSM (Noise)uV with OSR/Gain at V_{DD}=AV_{DD}=2.7V, V_{REF}=2.4V,V_{REF} Gain=0.25, CLK=8.192 MHz, ADCCLK=1.024 MHz, Bias Current=default(x1), Chopper On(except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							PGA*PGA Buffer Gain	PGA Gain*PGA Buffer Gain*DF Gain
Data Rate (SPS)	OSR	1	2	4	8	16	32	64	128 (64*2)	256 (64*2*2)
31.25	32768	2.0403	2.0282	1.2556	1.0284	0.6024	0.4697	0.3720	0.3460	0.3517
62.5	16384	2.9465	2.7757	1.7023	1.4158	0.8023	0.6725	0.4989	0.5053	0.5036
125	8192	3.7126	3.9319	2.4393	1.8901	1.1567	0.9494	0.7153	0.6835	0.7124
250	4096	5.3181	5.4784	3.4522	2.6863	1.6471	1.3841	1.0270	0.9918	0.9961
500	2048	7.2840	7.9560	4.8470	4.0186	2.3347	1.9401	1.4302	1.4244	1.3786
1000	1024	10.5635	11.0251	6.7749	5.3513	3.2439	2.7182	2.0411	1.9734	1.9697

2000	512	16.8057	15.5914	10.0051	7.8398	4.5532	3.9371	2.9218	2.8333	2.8213
4000	256	20.9927	23.0643	15.0393	10.7862	6.6099	5.3488	4.0858	3.9286	3.9889
8000	128	29.1742	44.4293	19.0742	15.3278	9.1972	7.6096	5.6827	5.5439	5.5077
16000	64	42.5215	44.5978	27.8052	21.9392	12.9790	10.4118	8.2298	7.9879	7.8852

Figure 7.1-9 RMS (V_{REF} Gain=0.25)

RMS (Noise)uV with OSR/Gain at V_{DD} =AV_{DD} = 3.15V, V_{REF} = 2.4V, V_{REF} Gain=Bypass/1, CLK=49.152 MHz, ADCCLK=6.144 MHz, Bias Current = 0xFD&0xFA, Chopper On (except ADC modulator reference P/N buffer chopper is disable), FIR Off, 25˚C										
		PGA Gain							**PGA*PGA Buffer Gain**	**PGA Gain*PGA Buffer Gain*DF Gain**
Data Reat (SPS)	**OSR**	**1**	**2**	**4**	**8**	**16**	**32**	**64**	**128 (64*2)**	**256 (64*2*2)**
24000	256	7.0943	7.4556	4.3862	3.1404	3.8824	2.3355	1.5517	1.3188	1.3290
48000	128	9.6792	10.6162	6.1584	4.2343	5.2694	3.2358	2.1272	1.8905	1.9166
96000	64	14.3091	14.5717	8.8612	6.1878	7.1305	4.4452	2.9587	2.6701	2.5913

Figure 7.1-10 RMS (Over Driving Mode)

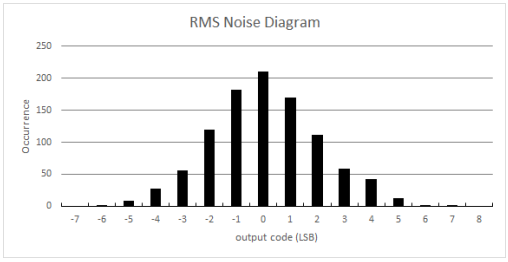


Figure 7.1-11 RMS Noise Histogram
(PGA Gain=1, Buffer Gain=1)

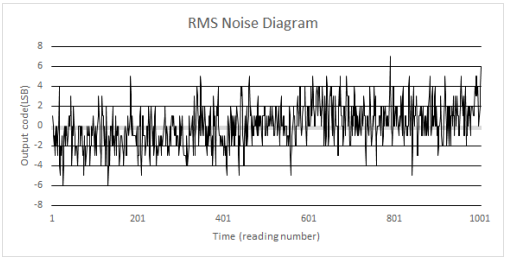


Figure 7.1-12 RMS Output Code
(PGA Gain=1, Buffer Gain=1)

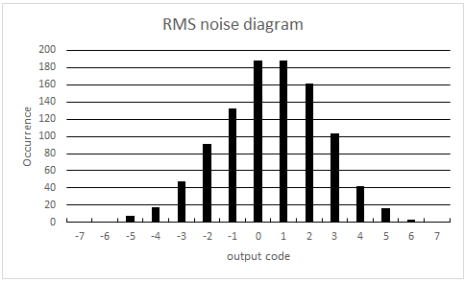


Figure 7.1-13 RMS Noise Histogram
(PGA Gain=16, Buffer Gain=1)

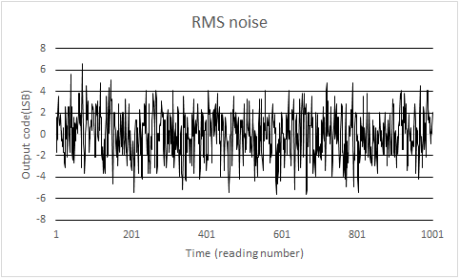


Figure 7.1-14 RMS Output Code
(PGA Gain=16, Buffer Gain=1)

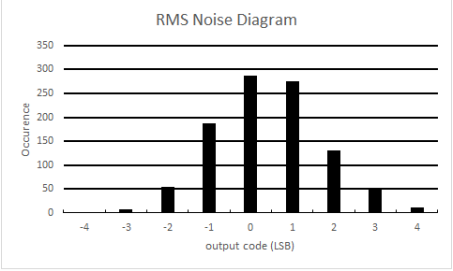


Figure 7.1-15 RMS Noise Histogram
(PGA Gain=64, Buffer Gain=1)

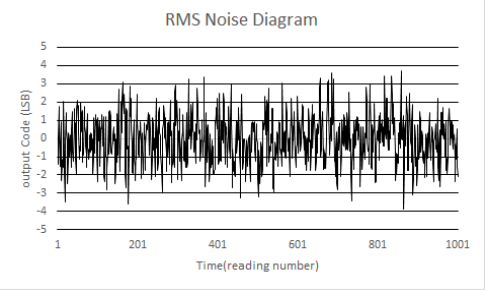


Figure 7.1-16 RMS Output Code
(PGA Gain=64, Buffer Gain=1)

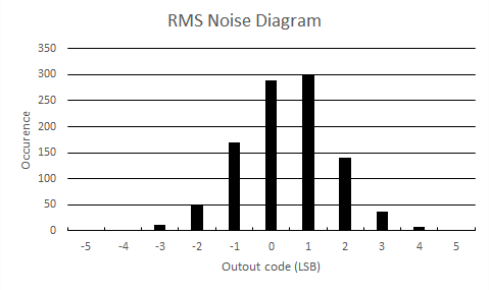


Figure 7.1-17 RMS Noise Histogram
(PGA Gain=64, Buffer Gain=2)

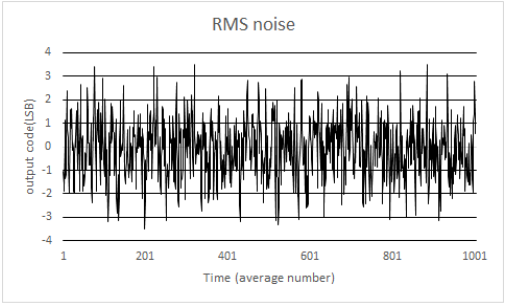


Figure 7.1-18 RMS Output Code
(PGA Gain=64, Buffer Gain=2)

V_{DD} = AV_{DD}=2.7V, V_{REF}= 2.4V, V_{REF} Gain=Bypass/1,CLK = 8.192 MHz, ADCCLK=1.024 MHz, Bias Current = default(x1), Chopper On (except ADC modulator reference P/N buffer chopper is disable), PGA Gain=1, PGA Buffer Gain=1, DF Gain = 1, OSR = 32768, 1000 samples base on 24-bit output (TT, QFN32)

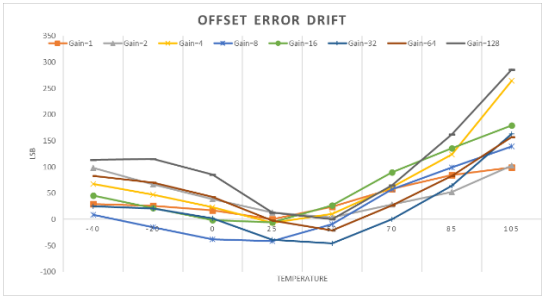


Figure 7.1-19 Offset Error vs Temperature
(PGA Gain=1/2/4/8/16/32/64, Buffer Gain=1/2)

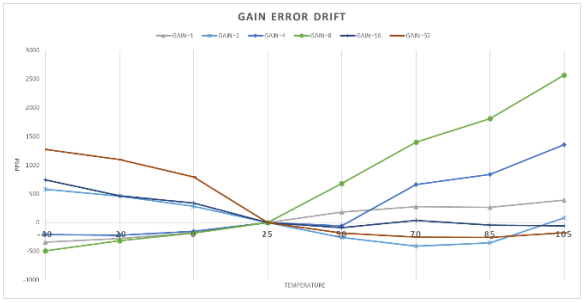


Figure 7.1-20 Gain Error vs Temperature
(PGA Gain=1/2/4/8/16/32, Buffer Gain=1)

V_{DD} = AV_{DD}=3.3V, V_{REF}= 2.4V, V_{REF} Gain=Bypass/1,CLK = 8.192 MHz, ADCCLK=1.024 MHz, Bias Current = default(x1), Chopper On (except ADC modulator reference P/N buffer chopper is disable), PGA Gain=1/2/4/8/16/32/64, PGA Buffer Gain=1/2, DF Gain = 1, OSR = 4096(250SPS), 1000 samples base on 24-bit output (TT, QFN32)

Data Settling Delay vs Data Rate		
DATA RATE (SPS)	**DRDY Periods (Normal mode)**	**DRDY Periods (Low latency mode)**
1.25	5	3
2.5	5	3
5	5	3
10	5	3
20	5	3
40	5	3
80	5	3
160	5	3
320	5	3
640	5	3
1000	5	3
2000	5	3
4000	5	3
8000	5	3
16000	5	3
24000	5	3
48000	5	3
96000	5	3

Table 7.1-16 Data Settling Delay vs Data Rate

Digital Filter Frequency Response for different output data rate

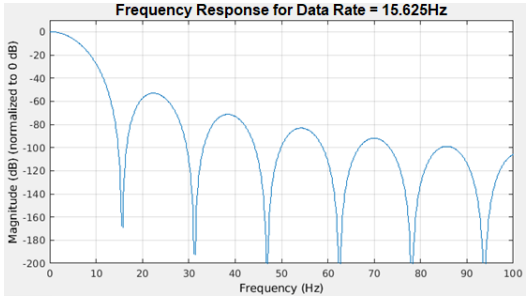


Figure 7.1-19 Frequency Response for Data Rate = 15.625

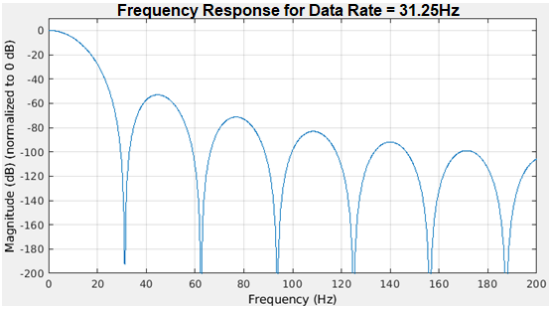


Figure 7.1-20 Frequency Response for Data Rate = 31.25

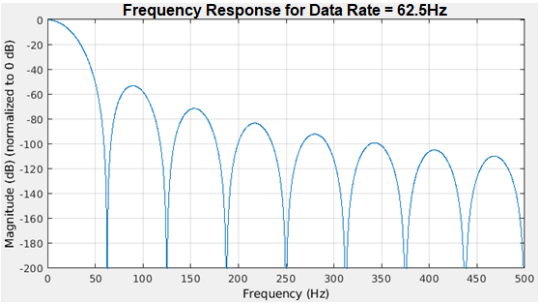


Figure 7.1-21 Frequency Response for Data Rate = 62.5

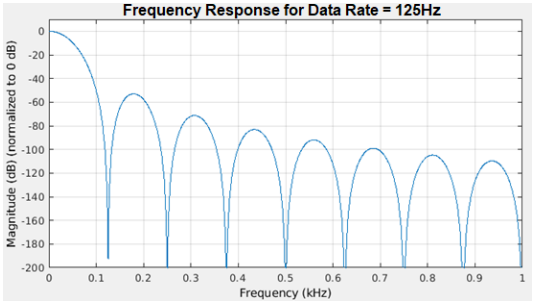


Figure 7.1-22 Frequency Response for Data Rate = 125

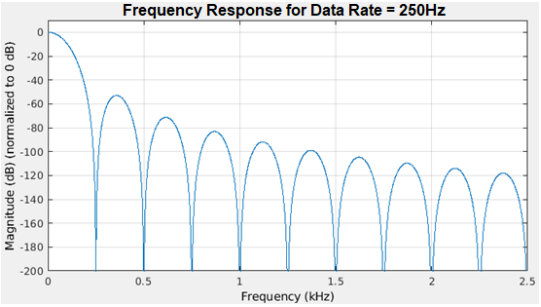


Figure 7.1-23 Frequency Response for Data Rate = 250

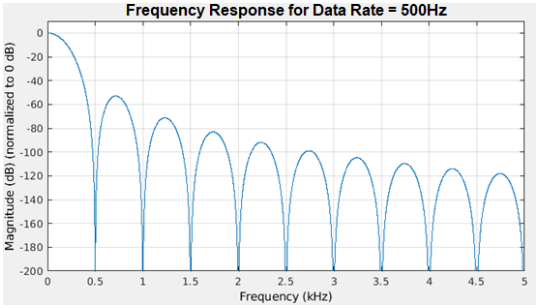


Figure 7.1-24 Frequency Response for Data Rate = 500

7.4.2 Internal Temperature Sensor

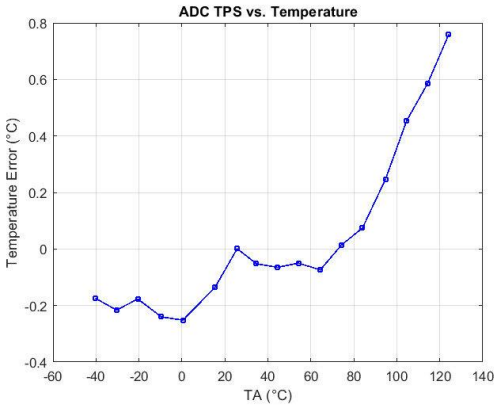


Figure 7.1-25 Temperature Error

7.4.3 Internal Reference Voltage Generator

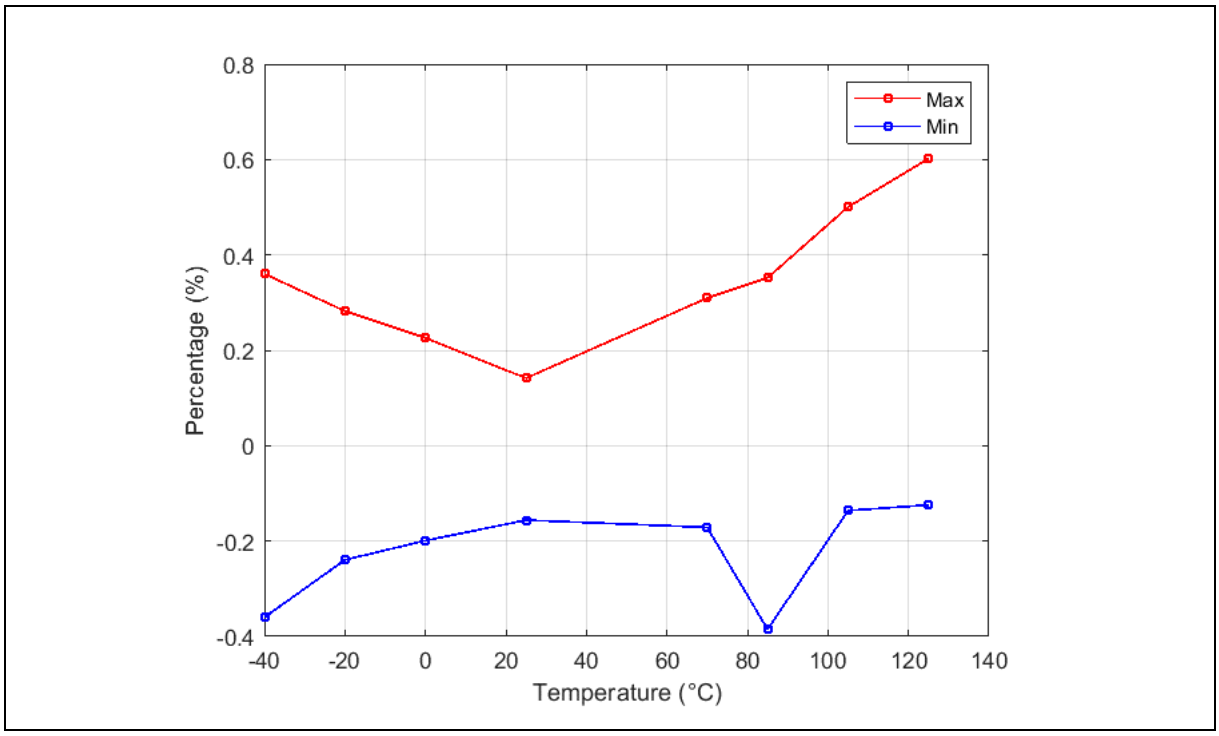


Figure 7.1-26 Internal V_{REF} = 2.4V vs Temperature

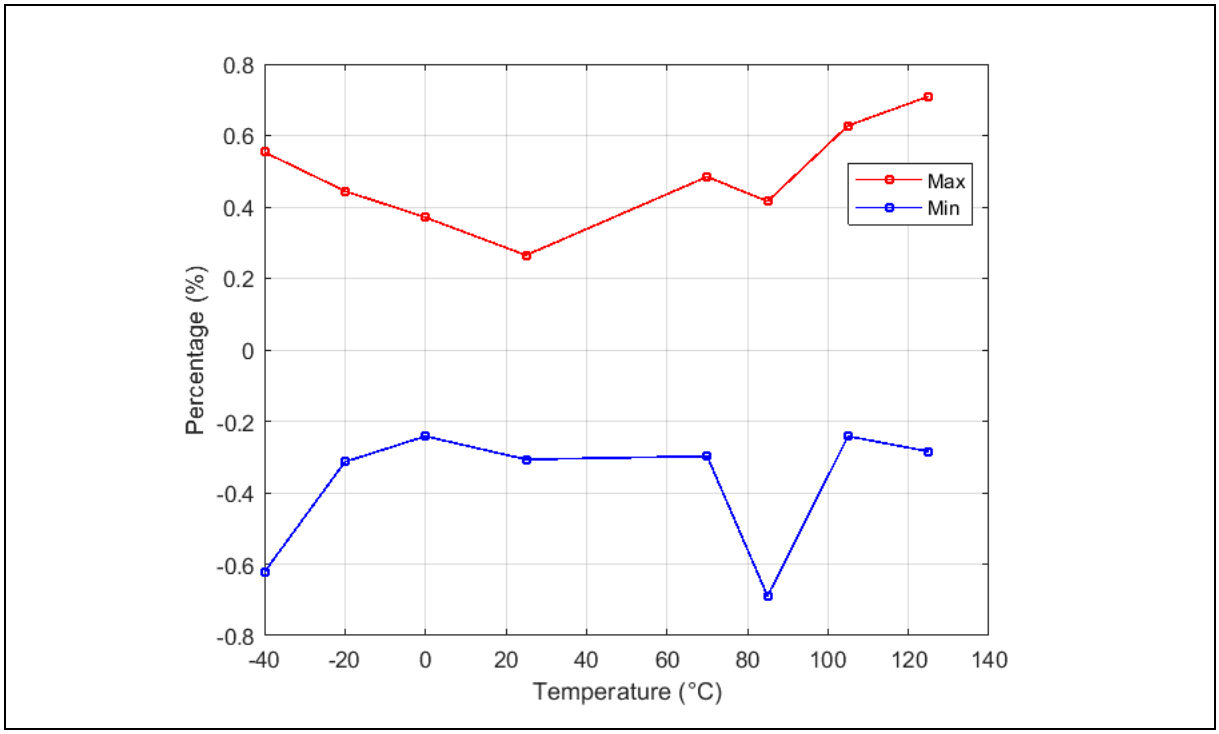


Figure 7.1-27 Internal V_{REF} = 1.2V vs Temperature

7.4.4 Internal 8.192 MHz RC Oscillator

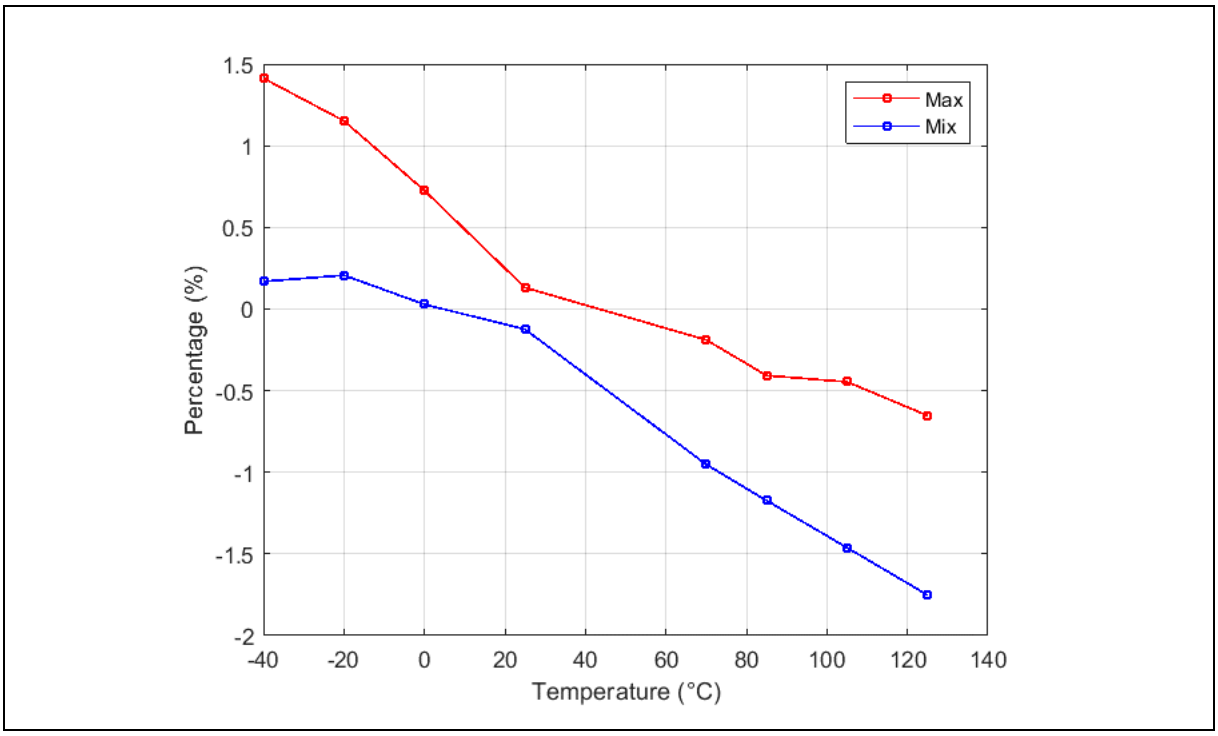


Figure 7.1-28 Internal HIRC = 8.192 MHz vs Temperature

8 APPLICATION CIRCUIT

8.1 NADC24 Series Application Circuit

The NADC24 provides a low-cost, high resolution analog-to-digital function. Because the analog-to-digital function is provided by a ΔΣ architecture, it makes the part more immune to noisy environments, making it ideal for use in sensor measurement and industrial and process control applications.

Figure 8.1-1 is a typical application schematic of NADC24.

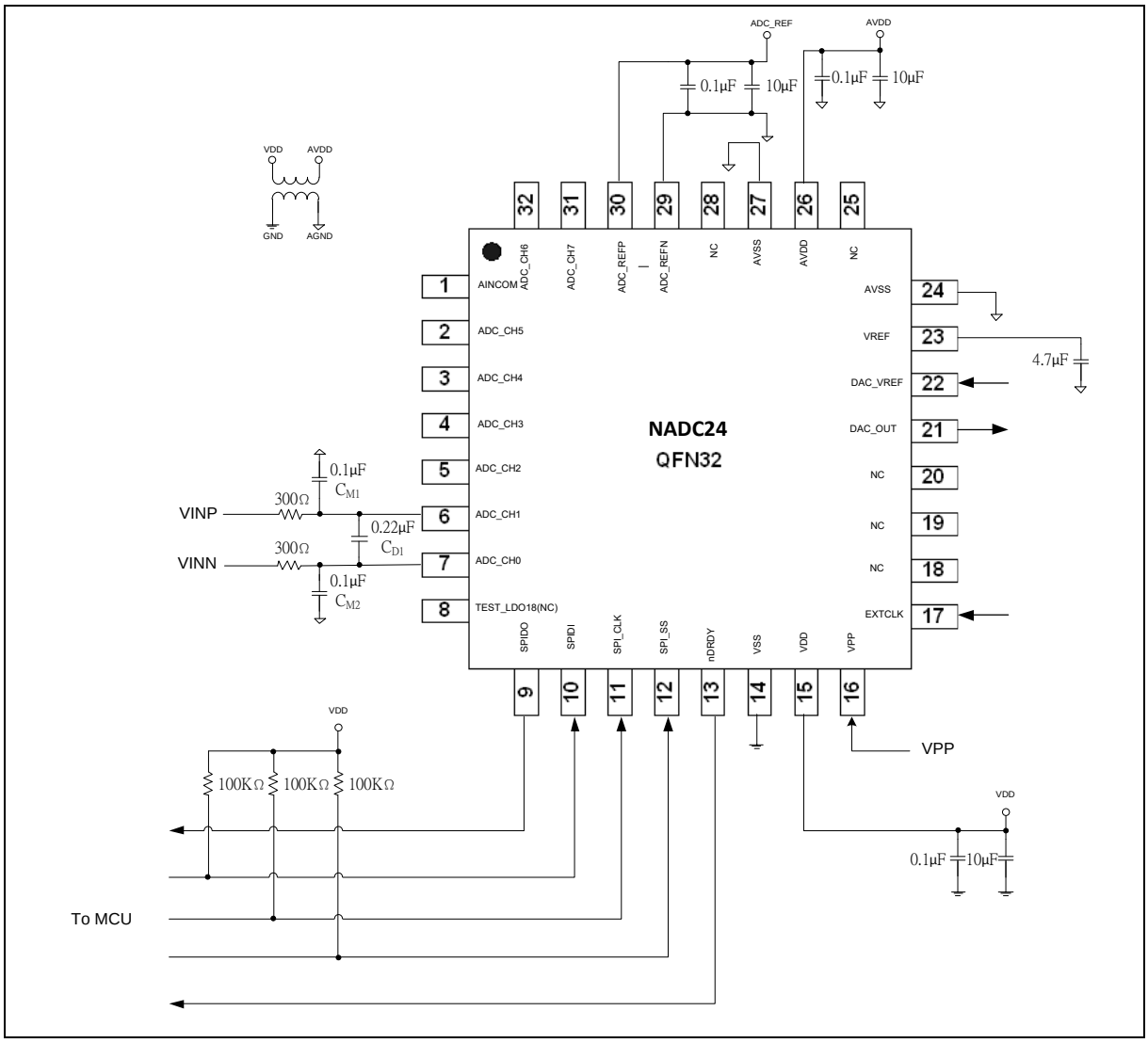


Figure 8.1-1 Application Circuit

9 PCB LAYOUT GUIDE

9.1 System Component Placement

The printed circuit board (PCB) that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board.

The following basic recommendations for layout of the NADC24 help achieve the best possible performance of the ADC. The ground plane can be split into an analog plane (AV_{SS}) and digital plane (V_{SS}), but this (splitting) is not necessary. Place digital signals over the digital plane, and analog signals over the analog plane. As a final step in the layout, the split between the analog and digital grounds must be connected to together at the ADC.

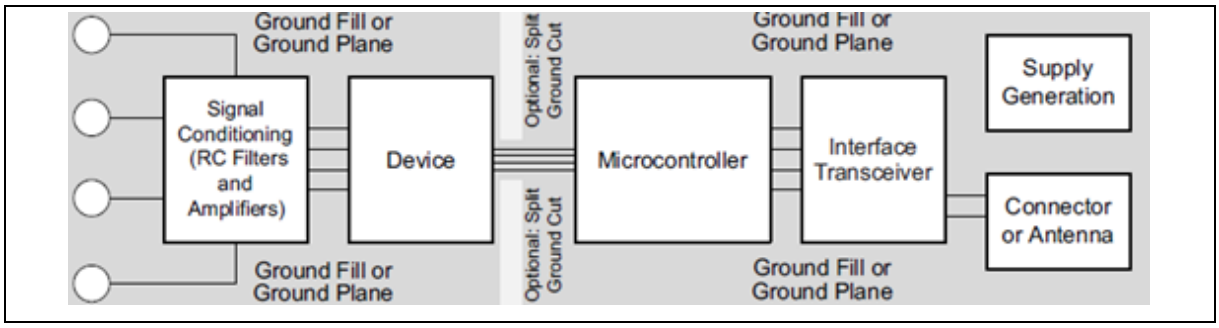


Figure 9.1-1 System Component Placement

Power

The power supply lines to the NADC24 must use as wide a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line.

Good decoupling is important when using high resolution ADCs. Decouple all analog supplies with 10 µF tantalum in parallel with 0.1µF capacitors to AV_{SS}. To achieve the best from these decoupling components, place them as close as possible to the device, ideally right up against the device.

Decouple all logic chips with 0.1µF ceramic capacitors to V_{SS}. In systems in which a common supply voltage is used to drive both the AV_{DD} and V_{DD} of the NADC24, it is recommended that the system AV_{DD} supply be used. For this supply, place the recommended analog supply decoupling capacitors between the AV_{DD} pin of the NADC24 and AV_{SS} and the recommended digital supply decoupling capacitor between the V_{DD} pin of the NADC24 and V_{SS}.

Ground

In systems in which the AV_{SS} and V_{SS} are connected somewhere else in the system (that is, the power supply of the system), they should not be connected again at the NADC24 because a ground loop results. In these situations, it is recommended that ground pins of the NADC24 be tied to the AV_{SS} plane.

Signals

It must keep in mind the flow of currents in the system, ensuring that the paths for all currents are as close as possible to the paths the currents took to reach their destinations. Avoid forcing digital currents to flow through the AV_{SS}.

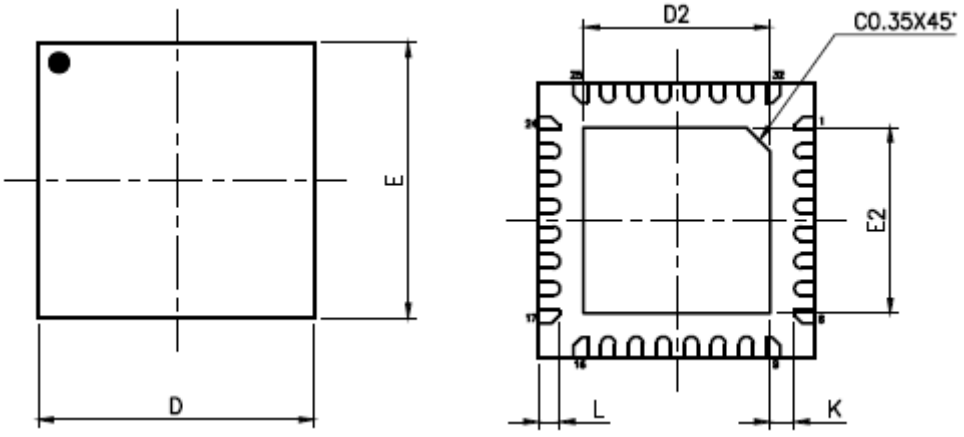
Avoid running digital lines under the device because this couples noise onto the die and allow the analog ground plane to run under the NADC24 to prevent noise coupling.

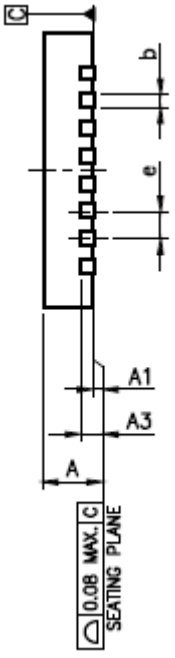
Shield fast switching signals like clocks with digital ground to prevent radiating noise to other sections of the board, and never run clock signals near the analog inputs. Avoid crossover of digital and analog signals.

10 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

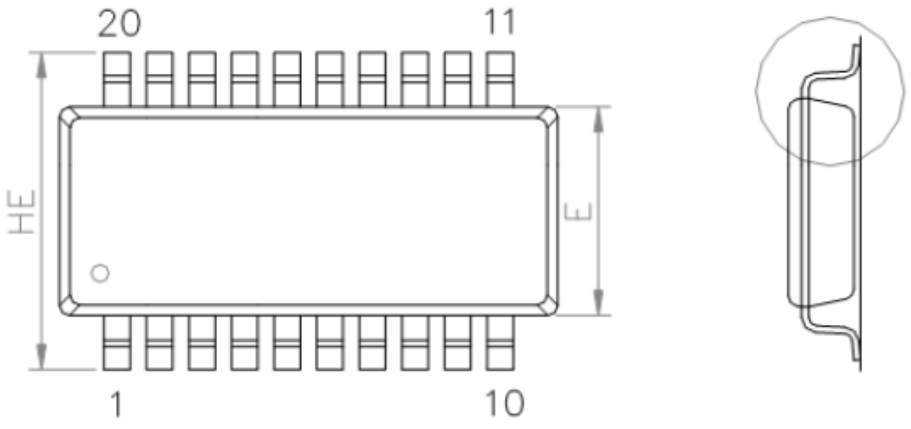
10.1 QFN 32L (4x4x0.8 mm Pitch:0.40 mm)

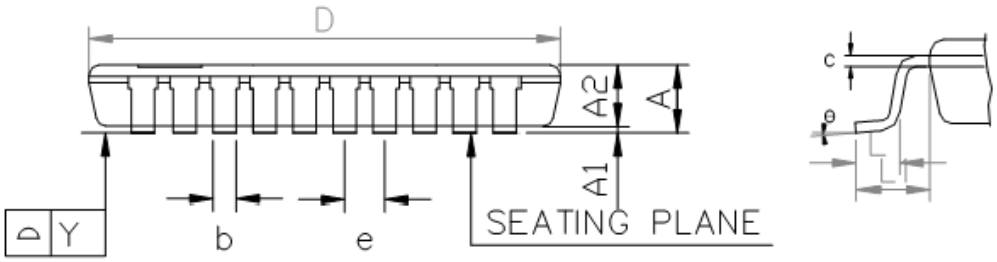




SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
K	0.20	—	—

10.2 TSSOP 20-Pin (4.4x6.5x0.9 mm)





SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

11 REVISION HISTORY

Date	Revision	Description
2023.10.02	1.00	• Initial version.
2024.04.09	1.01	• Revised offset calibration description in section 6.1.6.6.1.6 • Revised timing diagram and added channel change and settling time portion timing diagram in section 6.4.6.1.6 • Revised ADC analog differential input range from +/-V_{ADC_REF}*0.9/(PGA Gain) to +/-V_{ADC_REF}*0.5/(PGA Gain). • Added ADC portion gain error, gain error drift spec. and revised offset error and offset error drift spec. in section6.1.6 7.3.2. • Added offset error drift and gain error drift figures in section 6.1.67.4.1.
2024.04.26	1.02	• Revised Figure 4.3-1. • Removed LDO spec. in section 7.3.6.

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