Operating the NAU8822L Audio CODEC at 96kHz/192kHz Sampling Frequency

This application note describes the procedure to program the register map of the NAU8822L audio codec for applications requiring sampling frequency of 96 kHz/192kHz. The NAU8822L datasheet specifications are described for 48 kHz sampling frequency. Using the procedure described below, the NAU8822L can be made to operate at 96 kHz/ 192 kHz sampling frequency.

The internal ADC and DAC require 256*FS internal clock for sampling, hence it is essential that the external I2S master provides the Master Clock (MCLK), Bit clock (BCLK) along with the sampling clock(FS) of 96 kHz/192kHz to satisfy the requirement of the internal data converters. In applications where there is a fixed MCLK which is not the integral multiple of FS, the internal PLL is to be configured in a way such that its output generates the 256*FS clock for the data converters. The Codec can operate in Master mode or Slave mode. In the Master mode, the NAU8822L requires just the MCLK as the input, and using the internal PLL, it generates synchronized BCLK and FS.

The NAU8822L requires proper setting of OSR (Over Sampling Rate) bit, PLL49MOUT bit, MCLK select bit and ADCB_OVER (ADC Bias current Override) bit in order to operate in the 96kHz / 192kHz sampling mode. The following section shows the bit locations of OSR bit, PLL49MOUT, ADCB_OVER and the expected results in 96 kHz and 192 kHz sampling frequency modes.

Case 1: Sampling Frequency 96kHz. , MCLK =12MHz

The OSR needs to set at 64x for 96kHz sampling frequency.This OSR bit is defined in bit 3 of 0x0A register for DAC and bit 3 of 0x0E for ADC.

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
14	0E	ADC Control	HPFEN	HPFAM	HPF			ADCOS	0	RADCPL	LADCPL

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
10	0A	DAC Control	0	0	SOFTMT	0	0	DACOS	AUTOMT	RDACPL	LDACPL

DACOS/ADCOS 0 64x OSR
1 128x OSR

In addition to the OSR bit, ADCB_OVER bit needs to be set in order to operate in the 96 kHz mode. This is defined at bit5 of R72.

The following table shows the results under this condition.

Parameter	Symbol	Comments/Conditions	Value	Units
ADC				
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	90	dB
Total harmonic distortion	THD+N	Input = -3dB FS input	-80	dB
DAC driving RHP/LHP with 10kΩ / 50pF load				
Signal-to-noise ratio	SNR	A-weighted	94	dB
Total harmonic distortion	THD+N	R_L = 10kΩ; Input = -3dB FS input	-84	dB

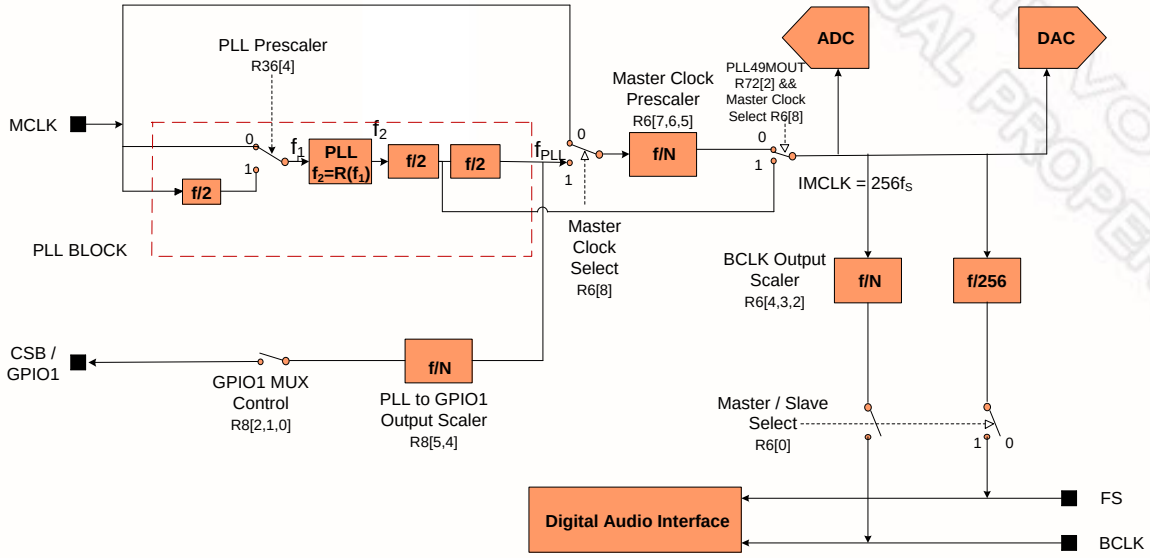
Case 2: Sampling Frequency 192 kHz. , MCLK =12MHz

The PLL49MOUT bit ,Master clock select bit R6[8] and ADCB_OVER R72[5] need to be set in order to operate in this mode. The OSR32x bit is defined in bit 1 of 0x48 register for DAC, bit 0 of 0x48 for ADC and the PLL49MOUT is defined in bit3 of 0x48 register. The suggested OSR for 192kHz sampling frequency is 32x.

DEC	HEX	NAME	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
72	48	192kHzControl	R	R	R	ADCB_OVER	R	R	PLL49MOUT	DAC32xOSR	ADC32xOSR

ADC32xOSR/DAC32xOSR -- 0 32xOSR Disabled
ADC32xOSR/DAC32xOSR -- 1 32xOSR Enabled
PLL49MOUT -- 0 for 48kHz / 96kHz sampling (Default value)
PLL49MOUT -- 1 for 192kHz sampling
ADCB_OVER --- 0 for 48kHz sampling
ADCB_OVER --- 1 for 96kHz/192kHz sampling

The below PLL block diagram shows the effect of PLL49MOUT bit while generating the clocks.



PLL Block Diagram

The following table lists the results under this condition.

Parameter	Symbol	Comments/Conditions	Value	Units
ADC				
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	90	dB
Total harmonic distortion	THD+N	Input = -3dB FS input	-80	dB
DAC driving RHP/LHP with 10kΩ / 50pF load				
Signal-to-noise ratio	SNR	A-weighted	94	dB
Total harmonic distortion	THD+N	R_L = 10kΩ; Input = -3dB FS input	-84	dB

Revision History

VERSION	DATE	PAGE	DESCRIPTION
0.1	March,2013		Initial Version

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