MA35D1 Series Hardware Development Guide

Application Note for 64-bit NuMicro® Family

Document Information

Abstract	This MA35D1 hardware design guide is intended for hardware system designers who require a hardware implementation overview for a MA35D1 based system.
Apply to	NuMicro® MA35D1 series.

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1 Overview

The MA35D1 hardware design guide is intended for hardware system designers who require a hardware implementation overview for a MA35D1 based system. The features include peripheral hardware description of main function, PCB trace notes and reference circuits. This design guide shows how to use the MA35D1 series and describes the minimum hardware resources required to develop a MA35D1 based system.

This design guide can be tailored to any other MA35D1 series with different package using the pins correspondingly given in the MA35D1 Datasheet.

2 MA35D1 Features

Core and System	
Arm® Cortex®-A35	● Dual 64/32-bit Arm® Cortex®-A35 core running up to 1G Hz ● Built-in 32 KB instruction and 32 KB data L1 cache for each core with Memory Management Unit (MMU) ● Built-in 512 KB shared L2 cache with Snoop Control Unit (SCU)-L2 cache protection ● Arm® TrustZone® ● Arm® NEONTM SIMD Engine and FPU ● Arm® Cryptographic Extension ● Armv8 debug logic ● Supports Generic Interrupt Controller (GIC) CPU interface ● Supports 64-bit count input for Generic Timer
Arm® Cortex®-M4	● 32-bit Arm® Cortex®-M4 processor core running up to 180 MHz ● Built-in 16 KB instruction and 16 KB data cache ● Built-in Memory Protection Unit (MPU) ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Hardware IEEE 754 compliant Floating-point Unit (FPU) ● DSP extension with hardware divider and single-cycle 32-bit hardware multiplier ● 24-bit system tick timer ● Programmable and mask able interrupt ● Low Power Sleep mode by WFI and WFE instructions

Arm® CoreLinkTM GIC-400 Generic Interrupt Controller (GIC)	● Up to 170 interrupts - 16 Software Generated Interrupt (SGIs) - 4 external Private Peripheral Interrupts (PPIs) for each processor - 1 internal PPI for each processor - 138 Shared Peripheral Interrupt (SPIs) ● Interrupt Enabled or Disabled ● Interrupt Prioritized ● Interrupt to dual Arm® Cortex®-A35 processor core ● Level-sensitive interrupt ● Security Extensions - Group 0 interrupt as Secure interrupts - Group 1 interrupt as Non-secure interrupts ● Virtualization Extensions
Hardware Semaphore	● Eight hardware semaphores for inter-processor synchronization ● Supports interrupt when semaphore released
Wormhole	● Supports two wormhole controller for inter-processor communication ● Supports interrupt for reset event and power state change event ● Four general event interrupts ● Eight 16-byte unidirectional message channels, four for each processor ● Supports message recall mechanism
Low Voltage Detect (LVD)	● Two-level LVD with low voltage detect interrupt (2.8V/ 2.6V)
Low Voltage Reset (LVR)	● LVR with 2.4V threshold voltage level
Memories	

Boot Loader	● Factory pre-loaded 128 KB mask ROM supporting four booting modes - Boot from USB (as device/ HOST) - Boot from SD/ eMMC - Boot from NAND Flash - Boot from SPI Flash (SPI-NOR/ SPI-NAND)
SDRAM	● Supports DDR2 (Double-Data-Rate 2), DDR3 (Double-Data-Rate 3) and DDR3L (DDR3 Low Voltage) type of SDRAM ● Clock speed up to 533 MHz ● Supports 16-bit data width ● SDRAM burst length of 8 ● Up to 2 memory ranks ● Maximum SDRAM size up to 2 GB (each chip select for 1 GB)
SRAM	● Up to 384 (128 + 256) KB on-chip SRAM ● Supports byte-, half-word- and word-access ● Supports PDMA operation
Peripheral DMA (PDMA)	● Four sets of PDMA with 10 independent and configurable channels for automatic data transfer between memories and peripherals ● Basic and Scatter-Gather transfer modes ● Each channel supporting circular buffer management using Scatter-Gather Transfer mode ● Stride function for rectangle image data movement ● Fixed-priority and Round-robin priorities modes ● Single and burst transfer types ● Byte-, half-word- and word transfer unit with count up to 65536 ● Incremental or fixed source and destination address

Security and Safety	
System Security Memory Configuration Controller (SSMCC)	● Three Arm® CoreLink™ TZC-400 TrustZone® Address Space Controllers for eight AXI channels ● Configurable security attribution of SDRAM memory ● Security violation detection, report and interrupt generation ● Programmable SDRAM region for SubM system ● Write protection of security configuration
System Security Peripheral Configuration Controller (SSPCC)	● Configurable security attribution of SRAM by boundary ● Configurable security attribution of GPIO by pin ● Configurable security attribution of peripherals ● Security violation detection, report and interrupt generation ● Write protection of security configuration ● Debug interface protection mechanism ● Product Lift-cycle Management
Clocks	
External Clock Source	● 24 MHz High-speed external crystal oscillator (HXT) for precise timing operation ● 32.768 kHz Low-speed external crystal oscillator (LXT) for RTC function and low-power operation ● Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	● 32 kHz Low-speed Internal RC oscillator (LIRC) ● 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 5% accuracy at -40 to 85℃ ● Six on-chip PLLs up to 1 GHz on-chip PLL, sourced from HXT, allowing CPU operation up to the maximum CPU frequency

Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain (V_{BAT}) • RTC clock source including Low-speed external crystal oscillator (LXT) • RTC block including 64 bytes backup registers • Able to wake up CPU • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock to be Timer capture source for calibration • Supports 1 pairs dynamic loop tamper pin or 2 individual tamper pin
Timers	
32-bit Timer	Timer • Twelve sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Event counting function to count the event from external pin • Input capture function to capture or reset counter value • External capture pin event for interval measurement • External capture pin event to reset 24-bit up counter • Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag

	to trigger EPWM, EADC and PDMA ● internal capture triggered from internal clock (HIRC, LIRC) or external clock (HXT, LXT) ● Inter-Timer trigger capture mode PWM ● Twelve 16-bit PWM counters with 12-bit clock pre-scale ● Supports 12-bit dead band (dead time) ● Up, down or up-down PWM counter type ● Supports brake function ● Supports mask function and tristate output for each PWM channel
Enhanced PWM (EPWM)	● Eighteen 16-bit counters with 12-bit clock pre-scale for eighteen PWM output channels ● Up to 18 independent input capture channels with 16-bit resolution counter ● Supports dead time with maximum divided 12-bit pre-scale ● Up, down or up-down PWM counter type ● Supports complementary mode for 3 complementary paired PWM output channels ● Synchronous function for phase control ● Counter synchronous start function ● Brake function with auto recovery mechanism ● Mask function and tri-state output for each PWM channel ● Able to trigger EADC to start conversion
Watchdog	● Three Watchdogs, one for TrustZone® Secure (TZS), one for TrustZone® Secure/Non-Secure (TZS/TZNS) and the other for SubM ● 20-bit free running up counter for WDT time-out

	interval ● Supports multiple clock sources from LIRC (default selection), PCLK/4096 or LXT with 9 selectable time-out period ● Able to wake up system from Power-down or Idle mode ● Time-out event to trigger interrupt or reset system ● Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period ● Configured to force WDT enabled on chip power-on or reset
Window Watchdog	● Three Window Watchdogs, one for TrustZone® Secure (TZS), one for TrustZone® Secure/Non-Secure (TZS/TZNS) and the other for SubM ● Clock sourced from LIRC (default selection) or PCLK/4096; the window set by 6-bit counter with 11-bit pre-scale ● Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	● One 12-bit, 4.7 MSPS SAR EADC with up to 8 single-ended input channels or 4 differential input pairs; 10-bit accuracy is guaranteed ● One internal channels for Battery power (V_{BAT}) ● Supports external V_{REF} pin or internal reference voltage ● Analog-to-Digital conversion can be triggered by software enable, external pin, Timer 0~11 overflow pulse trigger, ADINT0 and ADINT1 EOC interrupt pulse trigger, or EPWM trigger ● Configurable EADC sampling time ● Up to 9 sample modules, supporting double data buffers for sample module 0~3 ● Supports PDMA operation

Analog-to-Digital Converter (ADC)	● One 12-bit, 8-ch 500 KSPS SAR ADC with up to 8 single-ended input channels; 10-bit accuracy is guaranteed ● Supports 4-wire or 5-wire touch screen ● Supports external V_{REF} pin
Temperature Sensor	● Built-in temperature sensor with ±5℃ accuracy
Communication Interfaces	
Low-power UART	● 17 sets of UARTs with up to 9.5 MHz baud rate ● Auto-Baud Rate measurement and baud rate compensation function ● Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped ● Separated receive and transmit 32/32-byte FIFOs with receive FIFO programmable level trigger supported ● Auto flow control (nCTS and nRTS) ● Supports IrDA (SIR) function ● Supports RS-485 9-bit mode and direction control ● Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode ● Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction ● Supports wake-up function ● 8-bit receiver FIFO time-out detection function ● Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function ● Supports Single-wire mode ● PDMA operation
Smart Card Interface	● Two sets of ISO-7816-3 compliant with ISO-7816-3

	T=0, T=1 ● Supports full duplex UART function ● 4-byte FIFOs with programmable level trigger ● Programmable guard time selection (11 ETU~266 ETU) ● One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing ● Auto inverse convention function ● Stop clock level and clock stop (clock keep) function ● Transmitter and receiver error retry function ● Supports hardware activation, deactivation and warm reset sequence process ● Supports hardware auto deactivation sequence after card removal
I^2C	● Six sets of I^2C devices with Master/ Slave mode ● Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) ● Supports 10-its mode ● Programmable clocks allowing for versatile rate control ● Supports multiple address recognition (four slave addresses with mask option) ● Supports SMBus and PMBus ● Supports multi-address power-down wake-up function ● PDMA operation
Quad SPI	● Two sets of SPI Quad controllers with Master/ Slave mode, up to 100 MHz ● Supports Dual and Quad I/O Transfer mode ● Supports one data channel half-duplex transfer

	● Supports receive-only mode ● Configurable bit length of a transfer word from 8- to 32-bit ● Provides separate 8-level depth transmit and receive FIFO buffers ● Supports MSB first or LSB first transfer sequence ● Supports the byte reorder function ● Supports Byte or Word Suspend mode ● Supports 3-wired, no slave select signal, bi-direction interface ● PDMA operation
SPI/ I²S	● Four sets of SPI/ I²S controllers with Master/Slave mode ● For SPI PDMA function disable, provides separate 8-level of 32-bit or 16-level of 16-bit transmit and receive FIFO buffers ● For SPI PDMA function enable, provides separate 8-level of 32-bit, 16-level of 16-bit or 32-level of 8-bit transmit and receive FIFO buffers SPI ● Up to 100 MHz in Master mode ● Configurable bit length of a transfer word from 8- to 32-bit ● MSB first or LSB first transfer sequence ● Byte reorder function ● Supports Byte or Word Suspend mode ● Supports one data channel half-duplex transfer ● Supports receive-only mode ● Supports 3-wired, no slave select signal, bi-direction interface I²S ● Supports mono and stereo audio data with 8-, 16-,

	24- and 32-bit audio data sizes ● Supports PCM mode A, PCM mode B, I²S and MSB justified data format ● PDMA operation
I²S	● Two sets of I²S interfaces with Master/Slave mode ● Supports I²S audio sampling frequencies up to 192 kHz ● Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes ● Two 16-level FIFO data buffers, one for transmitting and the other for receiving ● Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format ● Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format ● PCM protocol supporting TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 ● PDMA operation
CAN FD	● Four sets of CAN FD controllers ● Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015 ● Compliant with CAN FD version 1.0 with up to 64 data bytes supported ● Supports CAN Error logging, AUTOSAR and SAE J1938 ● Built-in 2K word (32-bit) Message SRAM for each CAN FD controller ● Supports power-down
Secure Digital Host Controller (SDHC)	● Two sets of Secure Digital Host Controllers ● Supports 1-bit and 4-bit data bus width for SD memory card specification version 3.0 (SDR104 speed limited to maximum allowed I/O speed. SPI

	mode, DDR50 and UHS-II mode not supported) ● Supports 1-bit, 4-bit and 8-bit data bus widths for the eMMC interface (HS200 speed limited to maximum allowed I/O speed and HS400 not supported) ● Supports SD/ SDHC/ SDXC/ SDIO, eMMC card ● Supports SD/ eMMC tuning, CMD19 (SD) or CMD21(eMMC) ● Supports 200 MHz to achieve eMMC HS200 at 1.8V I/O operation
NAND Flash Controller	● Supports SLC and MLC type NAND Flash device ● Supports 2 KB, 4 KB and 8KB page size NAND Flash device ● 8-bit data width ● Supports EDO mode ● Supports ECC8, ECC12 and ECC24 BCH algorithm with ECC code generation, error detection and error correction ● Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and NAND Flash
External Bus Interface (EBI)	● Supports up to three memory banks with individual adjustment of timing parameter ● Each bank supporting dedicated external chip select pin with polarity control and up to 1 MB addressing space ● 8-/16-bit data width ● Supports byte write enable in 16-bit data width mode ● Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) ● Supports Address/Data multiplexed mode

	● Supports address bus and data bus separate mode ● PDMA operation
GPIO	● Supports three I/O modes - Push-Pull output mode - Open-Drain output mode - Input only with high impendence mode ● Selectable TTL/ Schmitt trigger input ● Configured as interrupt source with edge/level trigger setting ● Supports independent pull-up/ pull-down control
Key Pad Interface (KPI)	● Matrix keypad interface with up to 8x8 array ● Programmable de-bounce time ● Low-power wake-up mode ● Programmable three-key reset ● Generate interrupt and update press/release status of all keys once key press or release detected
Control Interfaces	
Quadrature Encoder Interface (QEI)	● Three sets of QEIs with two QEI phase inputs (QEI_A, QEI_B) and one Index input (QEI_INDEX) each ● Supports 2/ 4 times free-counting mode and 2/4 compare-counting mode ● Supports encoder pulse width measurement mode with ECAP
Enhanced Capture (ECAP)	● Three sets of ECAPs ● Input Capture Timer/ Counter ● Supports three input channels with independent capture counter hold register ● 24-bit Input Capture up-counting timer/counter supporting captured events reset and/or reload

	capture counter ● Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports ● Supports compare-match function
Advanced Connectivity	
USB 2.0 High Speed with on-chip transceiver	USB 2.0 High Speed HOST/ Device ● One set of on-chip USB 2.0 high speed dual role transceiver configurable as host, device or ID-dependent ● One set of on-chip USB 2.0 high speed transceiver with host only USB 2.0 High Speed Host Controller ● Compliant with USB Revision 2.0 Specification ● Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0 ● Compatible with OHCI (Open Host Controller Interface) Revision 1.0 ● Supports high-speed (480 Mbps), full-speed (12 Mbps) and low-speed (1.5 Mbps) USB devices ● Integrated with a port routing logic to route full/low speed device to OHCI controller ● Supports an integrated Root Hub ● Built-in DMA USB 2.0 High Speed Device Controller ● Compliant with USB Revision 2.0 Specification ● Supports up to eight bi-directional endpoints, in addition to control endpoint 0 ● Supports Control, Bulk, Interrupt and Isochronous transfers ● Supports Descriptor (Scatter-Gather) DMA operation

	• Supports LPM feature • Supports V_{BUS}/ Resume wake-up from system power-down mode
Gigabit Ethernet MAC (GMAC)	• Two sets of Gigabit Ethernet MAC • Compliant with IEEE Std. 802.3-2008 for Ethernet MAC • Compliant with IEEE Std. 1588-2008 for precision networked clock synchronization • Compliant with IEEE Std. 802.3az-2010 for Energy Efficient Ethernet (EEE) • Compliant with RGMII specification version 2.6 from HP/Marvell • Compliant with RMII specification version 1.2 from RMII consortium • Full-duplex operation - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion - Forwarding of received Pause frames to the user application • Half-duplex operation - CSMA/ CD Protocol support - Flow control using backpressure support - Frame bursting and frame extension in 1000 Mbps half-duplex operation • Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 KB of size • IEEE 802.1Q VLAN tag detection for reception frames • Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1) • Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP

	checksum encapsulated in IPv4 or IPv6 datagrams (Type 2) ● CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control ● Serial management interface (MDC/ MDIO) master mode for PHY device configuration and management ● Supports Magic Packet recognition to wake system up from Power-down mode
CMOS Sensor Interface	● Two sets of CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor ● Resolution up to 3 M pixels ● Supports YUV422 and RGB565 color format for data output by CMOS image sensor ● Supports YUV422, RGB565, RGB555 and Y-only color format with planar and packet data format for data storing to system memory ● Supports image cropping and cropping window up to 4096x2048 ● Supports vertical and horizontal scaling-down with N/M scaling factor ● Supports Negative, Sepia and Posterization color effects
Multi-Media	
TFT LCD Display Interface	● Display Interface - Supports parallel pixel output with 24-bit Data, HSync, VSync, Data enable - Supports DPI 24-bit, 18-bit and 16-bit - Supports i80/ m68 MPU type interface with optional VS_{YNC} or TE signal ● Frame rate up to 1920x1080 at 60 fps ● Input Format - ARGB2101010, A/XRGB8888, A/XRGB1555,

	RGB565, A/XRGB4444 - Index1/2/4/8 - YUV422 packed and semi planar (YUV2, UYVY, NV16) - YUV420 semi-planar (YUY2-P010), NV12 and YUV420 semi-planar 10-bit) ● Output Format - DPI_D16CFG1, DPI_D16CFG2, DPI_D16CFG3 - DPI_D18CFG1, DPI_D18CFG2 - DPI_D24 ● Color Space Conversion BT.2020 and BT.709 ● Supports ARGB888 and Mask cursor formats for hardware cursor ● Supports On Screen Display (OSD)
2D Graphic Engine (GFX)	● BitBLT, Stretch Blit and Filter Blit ● Line drawing, Rectangle fill and clear ● Mono expansion for text rendering ● ROP2, ROP3 and ROP4 ● Alpha blending, including Java 2 Porter-Duff compositing blending rules ● 32 Kx32 K coordinate system ● 90/ 180/ 270 degree rotation ● Transparency by monochrome mask, chroma key, or pattern mask ● Supports 2x2 in 4x4 tile format ● Supports XMajor and YMajor Super Tile 64x64 format ● A8 output with rotation in filter blit and bit blit ● Supports Source and Destination color key full bypass

	● Multi source blending - Full support for Multi source blending with variable block size - Up to 8 sources - Programmable block size ● Supports 90, 180, 270 degree rotation with different block size ● Supports format converting for non-planar YUV to planar YUV ● YUV422 output with alpha blending
Video and Image Decoder	AVC (H.264) / MVC / SVC Decoding ● Input stream format - AVC (H.264) stream including Byte stream and NAL unit stream - MVC stream - SVC stream ● Output picture format - YCbCr 4:2:0 semi-planar raster-scan - YCbCr 4:2:0 semi-planar 8x4 tiled - YCbCr 4:0:0 (monochrome) ● Frame by frame (field by field) and slice by slice decoding scheme ● Picture size from 48x48 to 1920x1080 with step size 16 pixels ● Frame rate up to 1920x1080 at 45 fps JPEG Decoding ● Input picture format - JFIF file format 1.02 - YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4

sampling formats

- Output picture format

  - YCbCr 4:2:0 semi-planar raster scan

- Picture size from 48x48 to 16368x16368 with step size 8 pixels
- Supports JPEG compressed thumbnails

Post Processing

- Input data format

  - YCbCr 4:2:0 semi-planar raster-scan

  - YCbCr 4:2:0 semi-planar 8x4 tiled

  - YCbCr 4:2:0 planar

  - YCbCr 4:0:0 (monochrome)

  - YCbYCr 4:2:2, YCrYCb 4:2:2

  - CbYCrY 4:2:2, CrYCbY 4:2:2

- Output data format

  - YCbCr 4:2:0 semi-planar

  - YCbYCr 4:2:2 raster-scan or 4x4 tiled

  - YCrYCb 4:2:2 raster-scan or 4x4 tiled

  - CbYCrY 4:2:2 raster-scan or 4x4 tiled

  - CrYCbY 4:2:2 raster-scan or 4x4 tiled

  - Fully configurable ARGB channel lengths and locations inside 32-bits, such as ARGB 32-bit (8-8-8-8), RGB 16-bit (5-6-5), ARGB 16-bit (4-4-4-4)

- Input image size from 48x48 to 16368x16368 with step size 8 pixels
- Output image size from 16x16 to 1920x1080 with horizontal step size eight and vertical step size 2
- Down Scaling

  - Arbitrary, non-integer scaling ratio separately for

    both dimensions

	- Unlimited down-scaling ratio ● Up Scaling - Arbitrary, non-integer scaling ratio separately for both dimensions - Maximum output width is 3x the input width (within the maximum output image size limit) - Maximum output height is 3x the input height – 2 pixels (within the maximum output image size limit) ● YCbCr to RGB color conversion - BT.601-5 compliant - BT.709 compliant - User definable conversion coefficient ● Dithering ● Alpha blending ● De-interlacing ● Contrast, brightness and color saturation adjustment for RGB image ● Supports Image cropping and digital zoom ● Picture in picture, output image masking ● Image rotation - Rotation 90, 180 or 270 degrees - Horizontal and vertical flip
Security Sub-System	
Trusted Security Island (TSI)	● An isolated secure hardware unit and operation is not affected by MA35D1 system ● Built-in cryptographic accelerators, Key Store and OTP memory ● Performs all the security operation, including secure

	boot and tamper-pin detection ● Refer to the TSI Application Note document for more detailed information
True Random Number Generator (TRNG)	● Compliant with NIST SP800-90A/B/C and BSI AIS 20/31 ● 128-bit random number generation ● 128-bit or 256-bit of security strength ● Background noise collection to speed reseeding operations ● Internal random seeding operation ● Start-up, continuous and on-demand health tests
Pseudo Random Number Generator (PRNG)	● Supports 128-, 163-, 192-, 224-, 233-, 255-, 256-, 283-, 384-, 409-, 512-, 521- and 571-bits random number generation (283~571-bits only generate for Key Store) ● Able to take the true random number seed from TRNG ● Able to take the true random number from TRNG (only for Key Store)
Advanced Encryption Standard (AES)	● Hardware AES accelerator ● Supports FIPS NIST 197 ● Supports SP800-38A and addendum ● Supports 128-, 192-, and 256-bits key ● Supports both encryption and decryption ● Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes ● Supports CCM mode, GCM mode and GHASH function ● Supports SM4 block cipher algorithm ● Supports key expander ● Supports one technique to improve side-channel

	attack protection ability
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports FIPS NIST 180, 180-2, 180-4 • Supports MD5 • Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and SHA-512/t • Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256 • Supports SM3 Cryptographic Hash Algorithm
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports both prime field GF (p) and binary filed GF (2^m) • Supports NIST P-192, P-224, P-256, P-384, and P-521 • Supports NIST B-163, B-233, B-283, B-409, and B-571 • Supports NIST K-163, K-233, K-283, K-409, and K-571 • Supports Curve25519 • Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves • Supports point multiplication, addition and doubling operations in GF (p) and GF (2^m) • Supports modulus division, multiplication, addition and subtraction operations in GF (p) • Supports three techniques to improve side-channel attack protection ability
Rivest、Shamir and Adleman Cryptography (RSA)	• Hardware RSA accelerator • Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits • Supports CRT decryption with 2048, 3072 and 4096

	bits ● Supports three techniques to improve side-channel attack protection ability
Key Store	● Supports programming interface for key management ● Supports key size required for Cryptography from 128-bits to 4096-bits ● Supports 32 keys for SRAM and 9 keys for OTP at most ● Supports crypto engine access or store key in key store directly ● Supports ECDH operation with ECC and PRNG engine ● Supports to store middle data for RSA CRT and SCAP mode ● Supports revoke operation ● Supports erase key in SRAM and revoke key in OTP while tamper detected ● Supports integrity checking ● Supports data scrambling ● Supports data remanence prevention at SRAM ● Supports silent access for side-channel protection at SRAM
OTP Controller	● Supports 32-bits programming function and reading function ● Supports 8 Kbits Secure OTP memory ● Supports data retention more than 10 years ● Supports fault tolerant mechanism ● Supports read only lock bit ● Supports side-band handshaking signals with KeyStore

3 Block Diagram

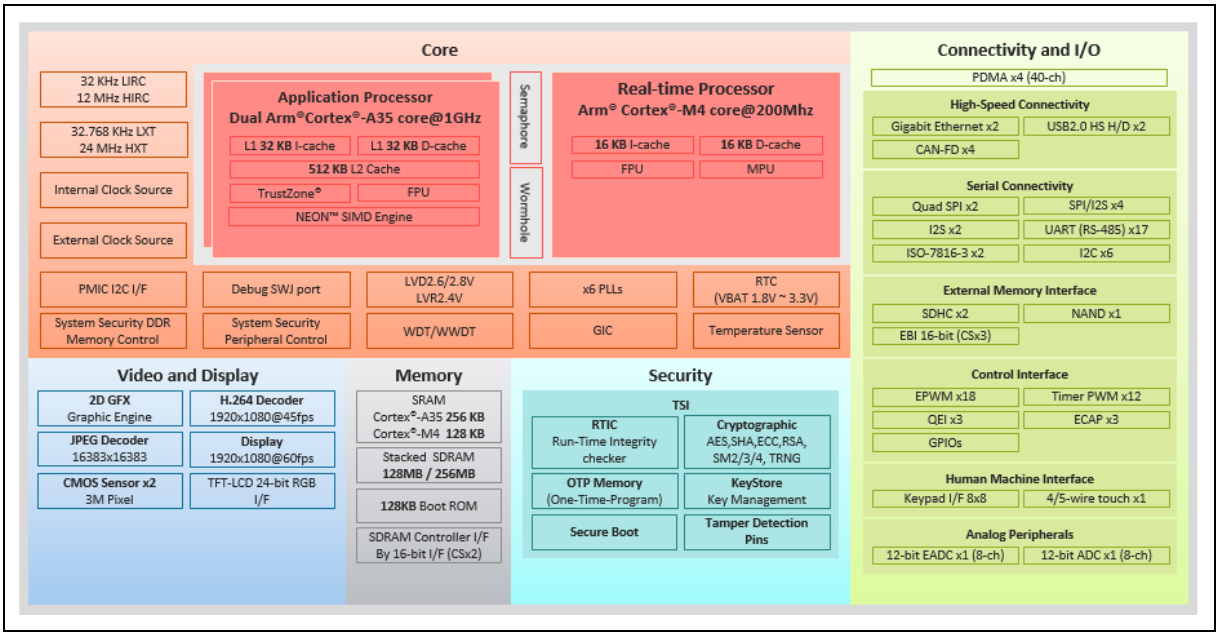


Figure 3-1 NuMicro® MA35D1 Block Diagram

4 Power Supplies

This section describes design considerations related to the MA35D1 series power supply scheme and power operating modes.

4.1 Power Supply Scheme

The MA35D1 series should be supplied by a stabilized power: VDD_CPU, VDD_CORE, MV_{DD}, MVDD_DPHYPLL, VDDIO0~10, AV_{DD}, AVDD_EADC0, AVDD_ADC0, V_{BAT}, VDD_OPT, VDD_HSUSB0~1, AVDDH_PLL1~2, AVDDL_PLL0~2, AVDDL_ROSC and VDD_PLL1.

Some points need to be considered when using these power rails:

- VDD_CPU pin must be powered by 1.2V±10% and with external decoupling capacitors (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each VDD_CPU pin is recommended).
- VDD_CORE pin must be powered by 1.2V±10% and with external decoupling capacitors (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each VDD_CORE pin is recommended).
- MV_{DD} pin must be powered by 1.35V±0.1V or 1.8V±0.1V (depending on DDR3L or DDR2) and with external decoupling capacitors (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each MV_{DD} pin is recommended).
- MVDD_DPHYPLL is DRAM PHY power pin which should be supplied by 2.5V±10% and with external decoupling capacitors (place one 0.1uF capacitor and one buck 10uF capacitor is recommended).
- VDDIO0, 1, 6 and 10 pin must be powered by 3.3V±10% and with external decoupling capacitors (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each VDDIO0,1, 6 and 10 pin is recommended).
- VDDIO2, 3, 4, 5, 7, 8 and 9 pin must be powered by 1.8V or 3.3V and with external decoupling capacitors (place one 0.1uF with MLCC and one buck 10uF with Tantalum capacitor for each VDDIO2, 3, 4, 5, 7, 8 and 9 pin is recommended).
- AV_{DD} is analog power pin which should be powered by 3.3V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor for each AV_{DD} pin is recommended).
- AVDD_EADC0 is enhance ADC power pin which should be supplied by 3.3V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).
- AVDD_ADC0 is ADC power pin which should be supplied by 3.3V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).
- V_{BAT} is an independent power domain which can be powered by 3.3V and place with a

0.1uF decoupling capacitor.

- VDD_OTP is OTP power pin which should be supplied by 2.5V±10% and with external decoupling capacitors (place one 0.1uF capacitor and one buck 10uF capacitor is recommended).
- VDD_HSUSB0~1 is USB port 0 and 1 PHY power pin which should be supplied by 3.3V±10% and with external decoupling capacitors (place one 0.1uF capacitor and one buck 10uF capacitor is recommended).
- AVDDH_PLL1~2 is phase lock loop analog high power pin which should be supplied by 3.3V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).
- AVDDL_PLL0~2 is phase lock loop analog low power pin which should be supplied by 1.2V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).
- VDD_PLL1 is phase lock loop digital power pin which should be supplied by 1.2V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).
- AVDDL_ROSC is low analog power supply for internal 12 MHz high speed RC Oscillator power pin which should be supplied by 1.2V±10% and with external decoupling capacitors (place one 0.1uF capacitor and a buck 10uF capacitor is recommended).

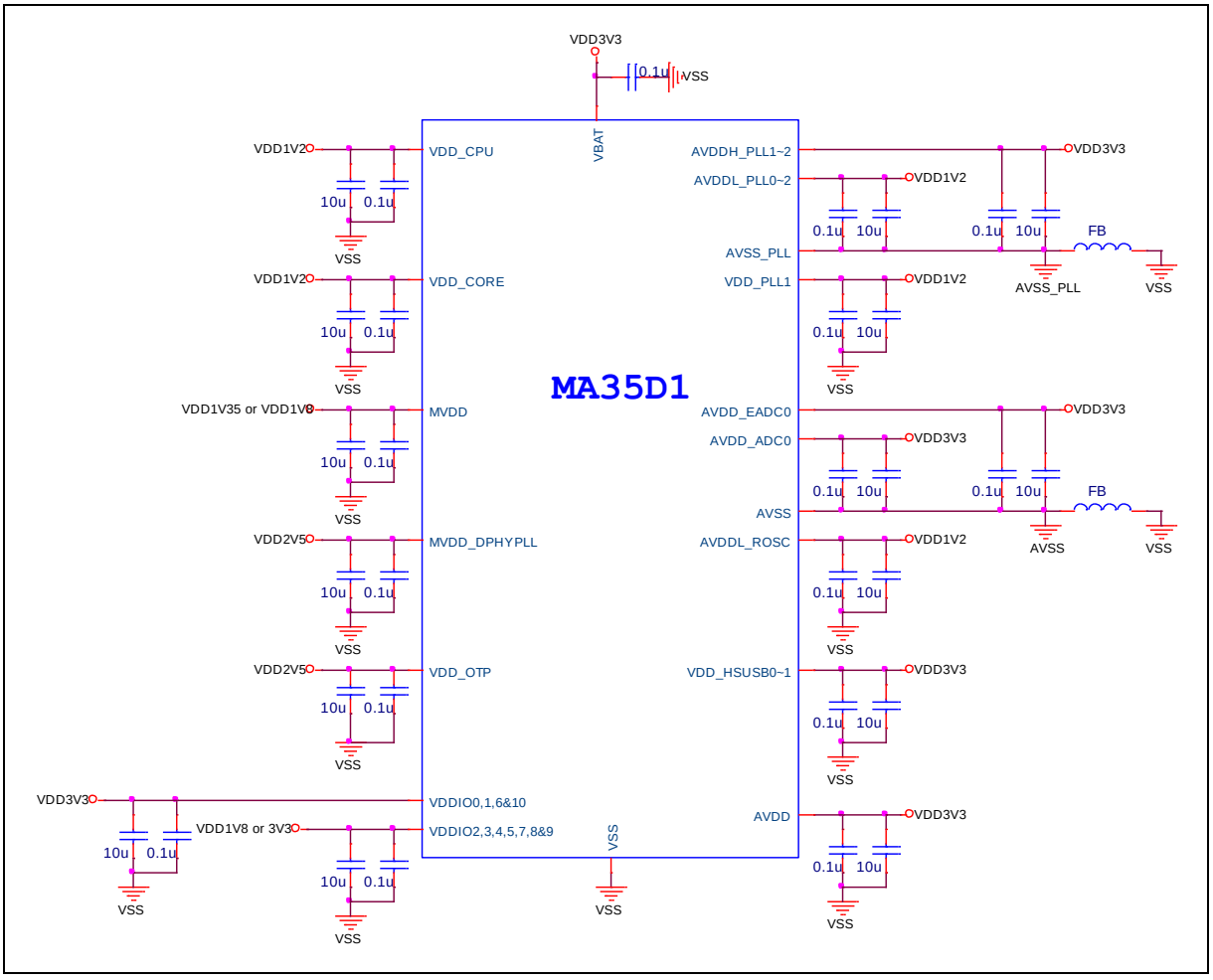


Figure 4-1 Power Supply Scheme of MA35D1 Series

4.2 V_{BAT}

The MA35D1 series has a built-in Real Time Clock (RTC) that is operated by the independent power supply while the system power is off. The RTC uses a 32.768 kHz external crystal.

This section will describe design considerations related to the V_{BAT}.

4.2.1 RTC Power Backup and Power Saving

For some applications requiring operation with either an external power supply or a battery backup, it is recommending to implement with a simple diode OR circuitry as Figure 4-2. The diode D1 prevents current from flowing into the CR2032 (3V) battery from LDO when the external power is supplied.

Low forward voltage Schottky diodes are used to minimize the voltage dropout from the diode and ensure that the LDO output will be a little higher than CR2032 (3V). This solution can save CR2032 BAT power life time and provided proper powered to V_{BAT}.

When external power is removed and the voltage is dropping lower than V_{BAT}, the CR2032 (3V) battery will start supplying power to MA35D1.

To avoid V_{BAT} power dropping causes RTC data loss by different power supply switching through diodes, at least place a 100nF capacitance to V_{BAT} with C1.

Figure 4-2 shows the RTC backup power block diagram for design reference.

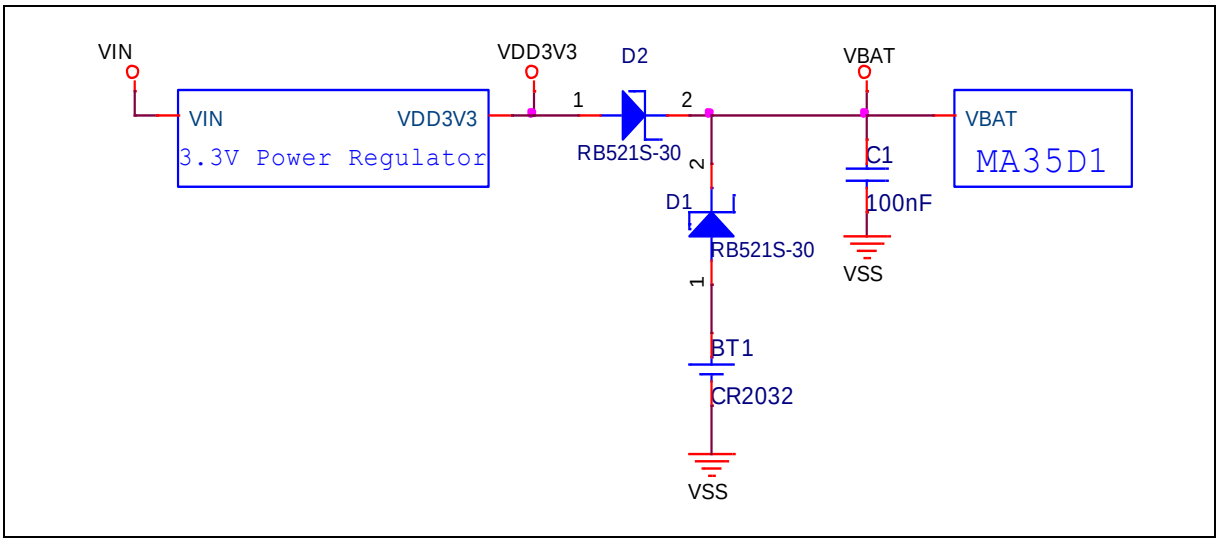


Figure 4-2 RTC Power Backup Block

5 RESET

Hardware Reset conditions can be issued by one of the listed events. These reset event flags can be read by RSTSTS register.

- Power-on Reset (POR)
- Low level on the nRESET Pin (nRST)
- Watchdog time-out reset (WDT)
- Low voltage reset (LVR)

5.1 POR

The MA35D1 integrated POR12 circuitry for core power, POR25 circuitry for OTP power and POR33 circuitry for I/O power to guarantee low level logic output state during the first power up phase.

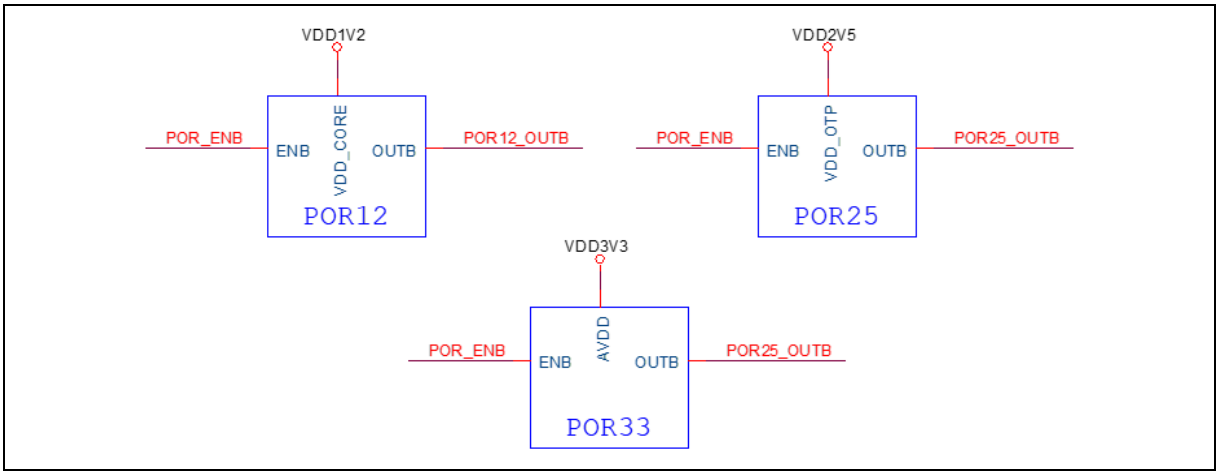


Figure 5-1 POR12/ POR25/ POR33 Inner Block

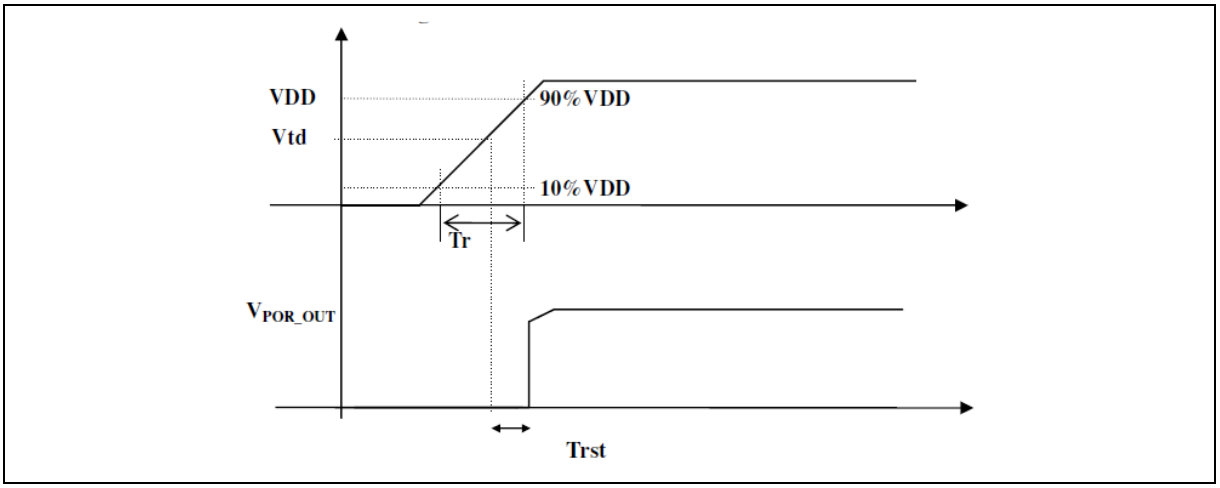


Figure 5-2 Power-on Reset at POR12

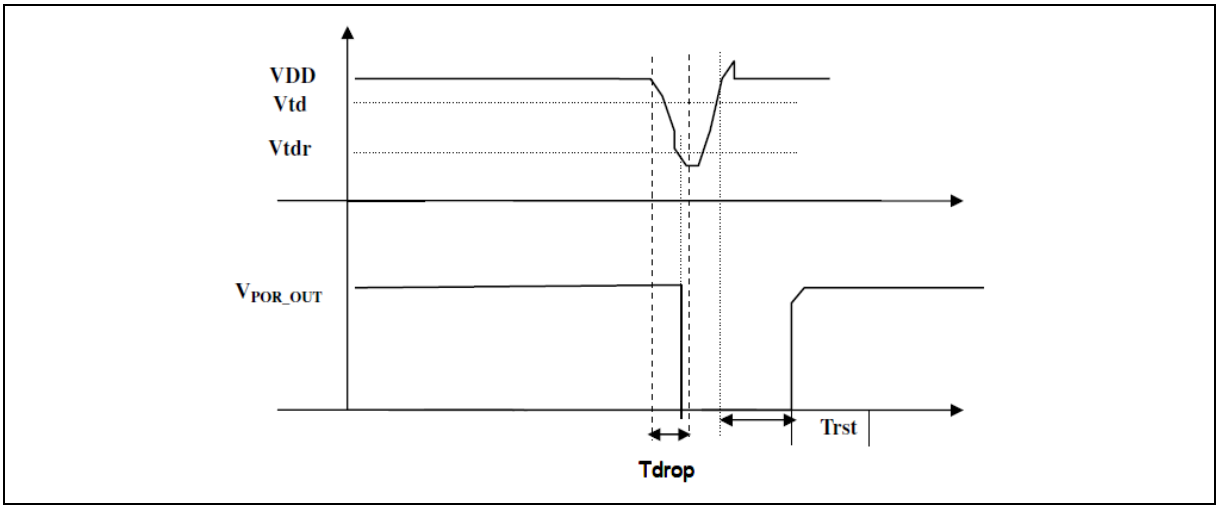


Figure 5-3 Power-drop Reset at POR12

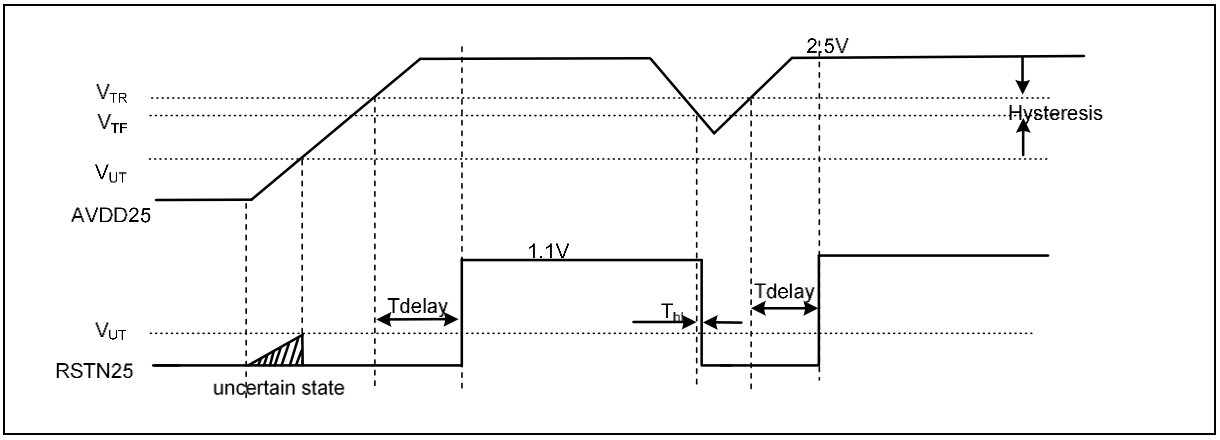


Figure 5-4 Power-on Reset at POR25

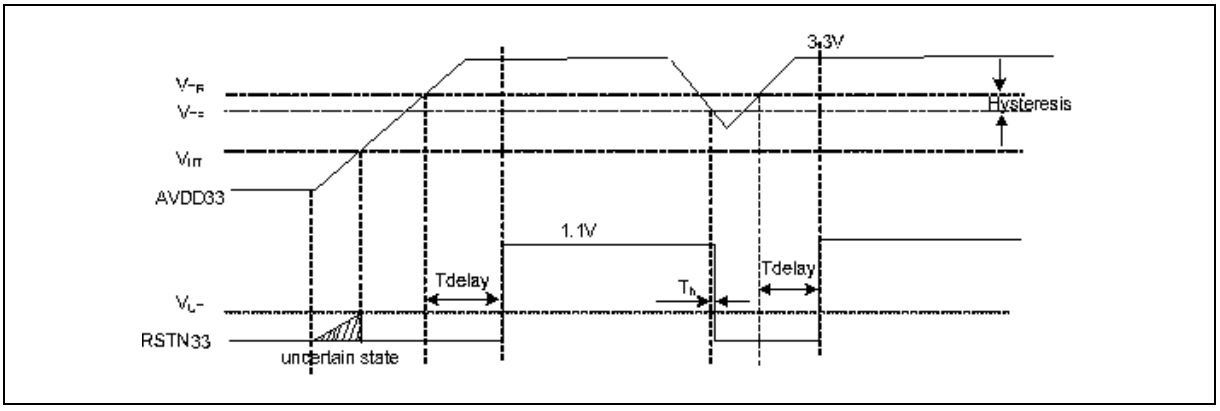


Figure 5-5 Power-on Reset at POR33

6 Power Sequence and nRESET

6.1 Power-on Sequence

T_{VDD1V2} >T_{MVDD} & T_{VDD2V5} & T_{VDD3V3}, the time of delay gap between ≦ 2 ms is preferred.

The nRESET pin becomes high when all power is stable for more than 10 ms.

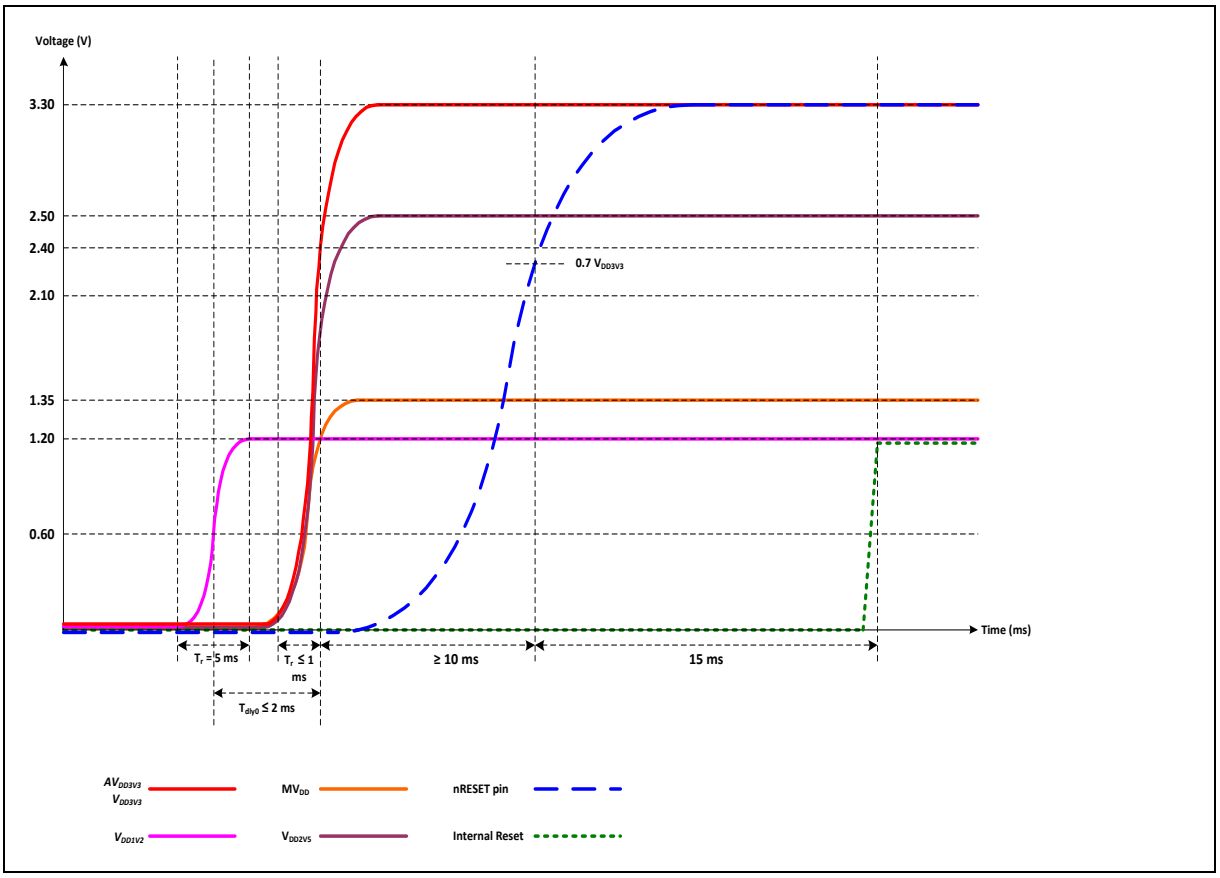


Figure 6-1 RESET vs Power-on Sequence

6.2 nRESET

nRESET is MA35D1 nRESET pin, generated from Figure 6-2 circuitry.

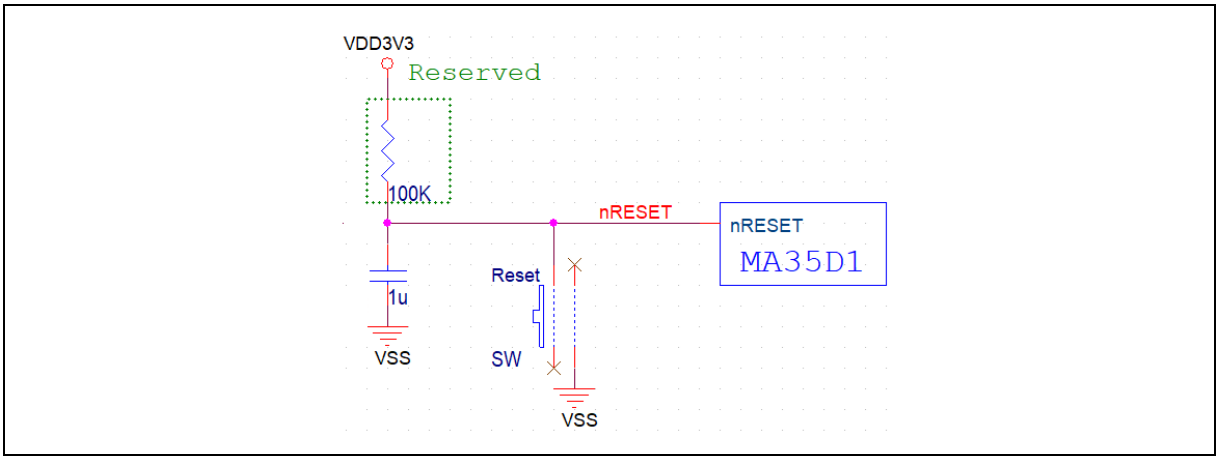


Figure 6-2 nRESET External Circuitry

Note: Guaranteed by characterization and design results, not tested in production.

6.3 WDT

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24~220) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK=32.768 kHz
- System kept in reset state for a period of (1/WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports WDT time-out wake-up function only
- WDT0 can reset both real time Cortex®-A35 and real time Cortex®-M4 sub-systems
- WDT1 can reset real time Cortex®-A35 sub-system when WDT1RSTAEN (SYS_MISCRFCR[16]) is set
- WDT1 can reset real time Cortex®-M4 sub-system when WDT1RSTMEN (SYS_MISCRFCR[18]) is set
- WDT2 can reset Cortex®-M4 sub-system
- WDT2 can reset Cortex®-A35 sub-system when WDT2RSTAEN (SYS_MISCRFCR[17]) is set

6.4 LVDR/ LVDR_V_{BAT}

The Low Voltage Reset (LVR) and the Low Voltage Detector (LVD) circuit prevent the contingency of internal operation failure caused by unstable supply voltage. It monitors the 3.3V or V_{BAT} (3.3V) voltage levels. The block diagram is shown as Figure 6-3.

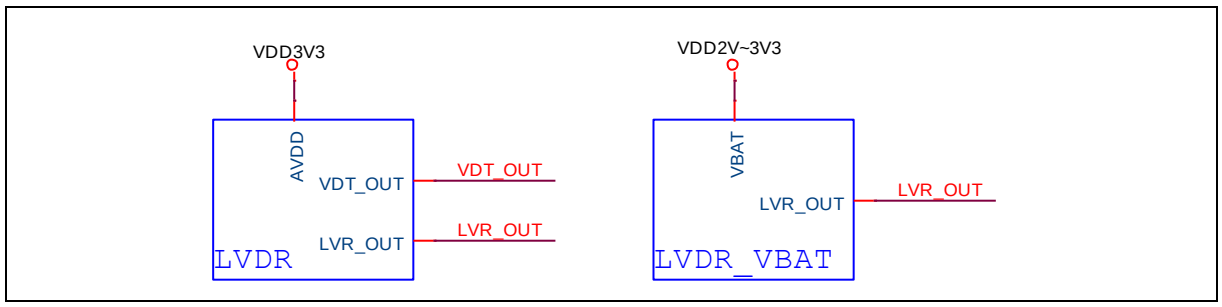


Figure 6-3 LVDR/ LVDR_V_{BAT} Block

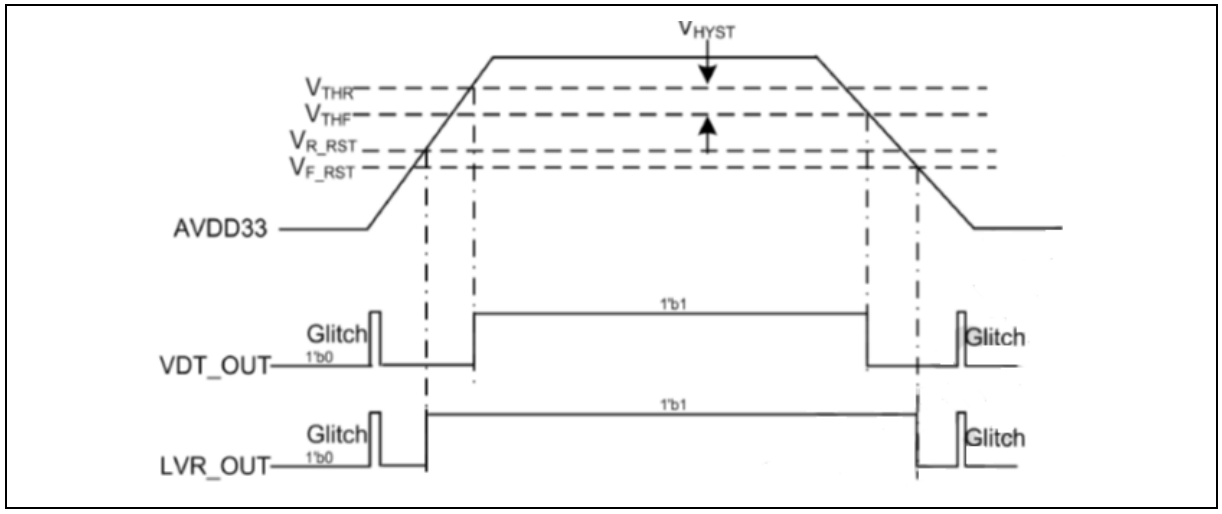


Figure 6-4 LVR and LVD Timing Waveform

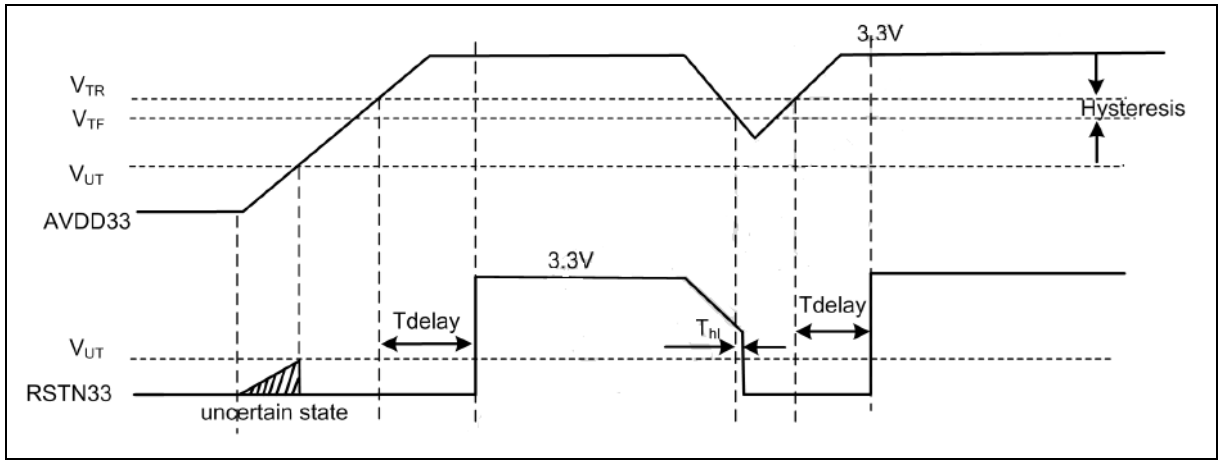


Figure 6-5 LVDR_V_{BAT} Timing Waveform

Glitches on AVDD33 will affect RSTN33 in two ways; one is RSTN33 that will not fall down to '0' since the glitch duration is short. If the glitch lasts for a long time, RSTN33 first drops to '0' and then rises to '1' after Tdelay time, as Figure 6-7.

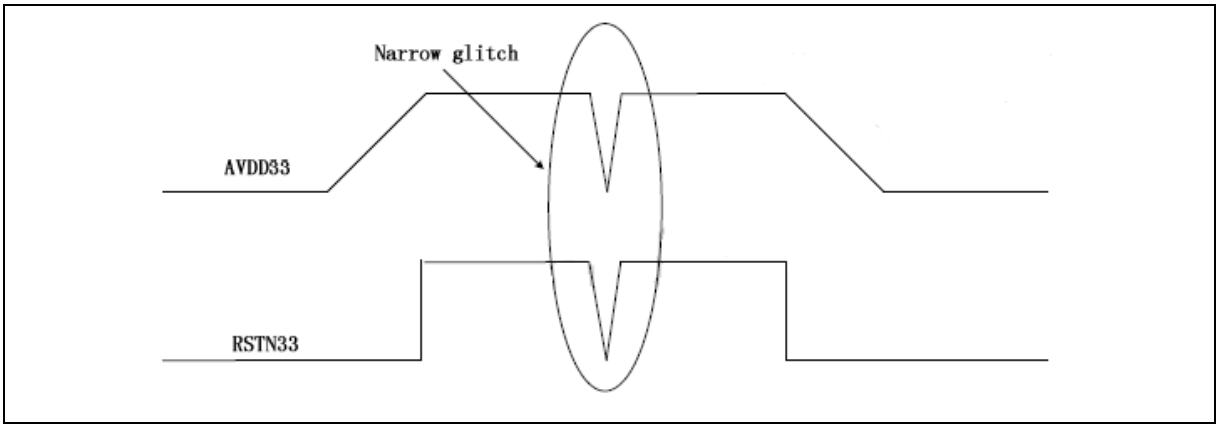


Figure 6-6 Narrow Glitch on AVDD33

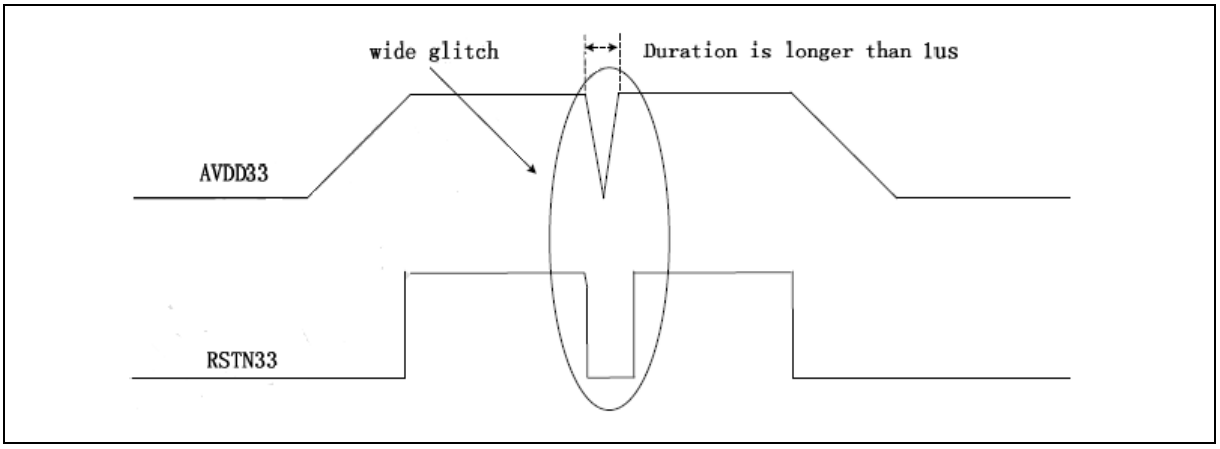


Figure 6-7 Wide Glitch on AVDD33

7 Power on Setting

The power-on setting is used to configure the chip to enter the specified state when the chip is power-up or reset.

Since each pin of power-on setting has an internal pulled-down resistor when in reset period. If the application needs to set the configuration to “1”, the proper pull-up must be added resisters for corresponding configuration pins as Figure 7-1.

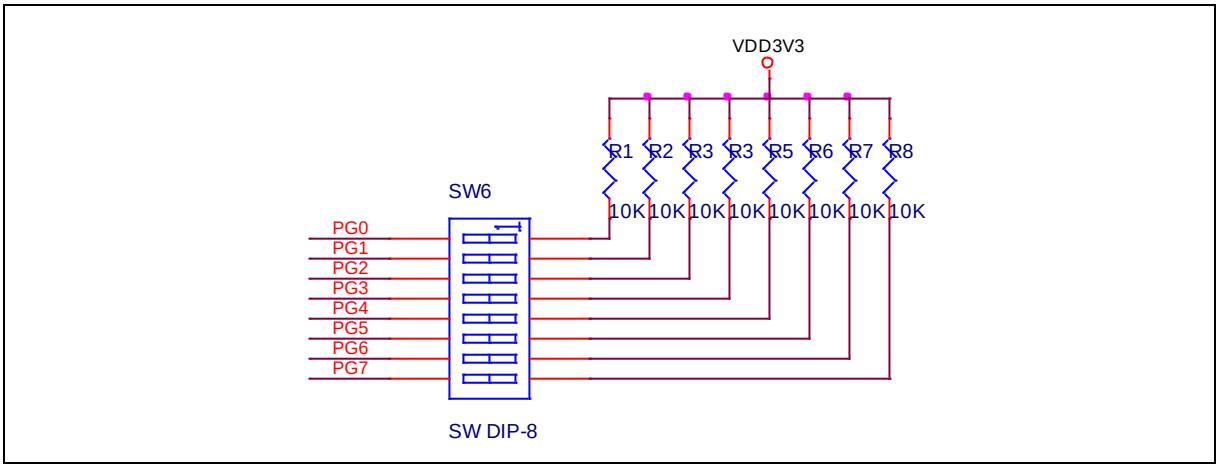


Figure 7-1 Power-on Setting Switch

Note:

0=Open-Internal pulled-down

1=ON-External pulled-up

PG[7:0]=SYS_PWRONPIN[7:0]

Power-on Setting Pin	Description	Power-on Setting Register Bit
PG0	**Secure Boot Disable Bit** 0=Secure Boot Enabled (Default) 1=Secure Boot Disabled	SYS_PWRONPIN[0]

Table 7-1 Power-on Setting, PG0[0] for Secure Boot Enable/Disable Selection

Power-on Setting Pin	Description	Power-on Setting Register Bit
PG1	**Boot Source Interface I/O Voltage** 0=Boot source interface I/O voltage is 3.3V (Default) 1= Boot source interface I/O voltage is 1.8V	SYS_PWRONPIN[1]

Table 7-2 Power-on Setting, PG1[1] for Boot Source Interface I/O Voltage Selection

Power-on Setting Pin	Description	Power-on Setting Register Bit
PG[3:2]	**Boot Source Selection** 00=Boot from SPI Flash (Default) 01=Boot from SD/ eMMC 10=Boot from NAND Flash 11=Boot from USB	SYS_PWRONPIN[3:2]

Table 7-3 Power-on Setting, PG[3:2] for Boot Source Selection

Power-on Setting Pin	Description	Power-on Setting Register Bit
PG[5:4]	**If PG[3:2]=10, Boot from NAND Flash** **NAND Flash Page Size Selection** 00=Ignore (Default) 01=NAND Flash page size is 2 KB 10=NAND Flash page size is 4 KB 11=NAND Flash page size is 8 KB **If PG[3:2]=11, Boot from USB** 00=USB Device port0 boot (Default) 01=USB HOST port0 boot 10=USB Device port0 boot 11=USB HOST port 1 boot	SYS_PWRONPIN[5:4]

Table 7-4 Power-on Setting, PG[5:4] for NAND Type or USB Role and Port Selection

Power-on Setting Pin	Description	Power-on Setting Register Bit
PG[7:6]	**If PG[3:2]=01, boot from SD/ eMMC** **PG6:** 0=SD0/ eMMC0 boot (Default) 1=SD1/ eMMC1 boot **PG7:** 0=eMMC 4-bit boot (Default) 1=eMMC 8-bit boot **If PG[3:2]=10, boot from NAND Flash** 00=Ignore (Default) 01=ECC is BCH T12 10=ECC is BCH T24 11=No ECC **If PG[3:2]=00, boot from SPI Flash** **PG7:** 0=SPI-NAND Flash with 1-bit mode boot (Default) 1=SPI-NOR Flash with 1-bit mode boot **If PG[3:2]=11, Boot from USB** **PG6:** 0=Over-current low active detect. (Default) 1= Over-current high active detect.	SYS_PWRONPIN[7:6]

Table 7-5 Power-on Setting, PG[7:6] for MISC. Type Selection

Power-on Setting Pin	Description	Power-on Setting Register Bit
HSUSB0_ID	**USB Port0 ID Pin Status** 0=USB Port0 act as a USB HOST 1=USB Port0 act as a USB device (Default)	-

Table 7-6 Power-on Setting, HSUSB0_ID for USB Port0 HOST/Device Selection

Note: HSUSB0_ID pin has an internal pull-up with 50 kΩ around.

8 Clock

The clock controller generates all clocks for CPU, system bus, AHB masters and all APB IP functionalities. The MA35D1 includes six PLL modules. Each functionality clock source comes from the PLL or from the external crystal input directly.

For each clock there is a bit on the CLK_SYSCLKx register to control the clock ON or OFF individually, and the divider setting is in the CLK_CLKDIVx register. The register can also be used to control the clock enable or disable for power control.

This section describes that design considerations with CLK oscillation installation.

8.1 External Crystal Sources

There are two external clock sources for the MA35D1 series:

- HXT, external 24 MHz high speed crystal input for PLL precise timing operation
- LXT, external 32.768 kHz low speed crystal input for RTC function and low speed clock source

The oscillators of 24 MHZ CLK and RTC_32K are connected with a quartz X'tal and two capacitors externally.

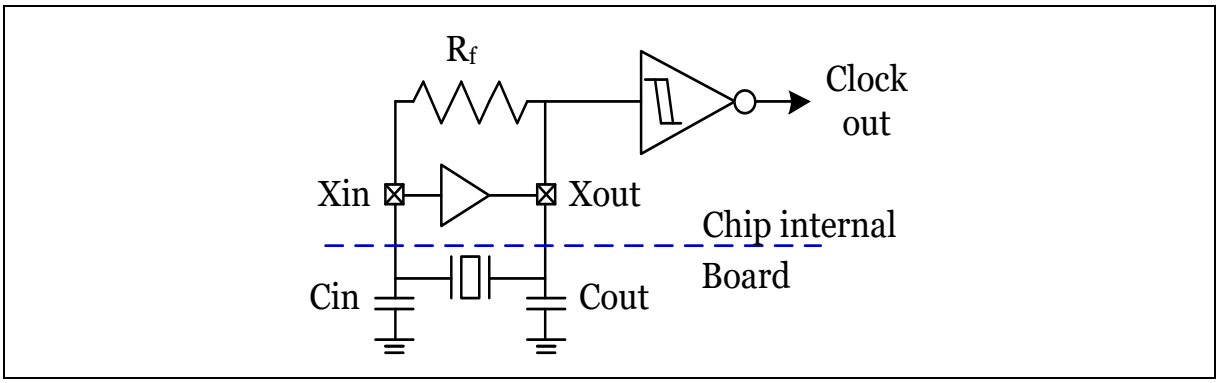


Figure 8-1 Crystal Oscillator Circuit

- Cin, Cout: External capacitors
- Rf: feedback resistor
- X'tal: External X'tal

The external crystal oscillator and two capacitors are connected to the pad "Xin" and pad "Xout". The capacitance value of the two capacitors may be adjustment by different crystal oscillator characteristic.

8.2 HXT, High Speed XTAL 24 MHz

C1 and C2 should use high-quality ceramic capacitors, usually C1 with C2 have same value by symmetry. Here, C1/C2 using 20 pF is recommended for resonating with low equivalent series resistance (ESR) (≦25 Ω) 24 MHz crystal and the crystal's CL is 12 pF around.

Typically, PCB layout and MA35D1 package capacitances should be calculated, the capacitance can be estimated as 2pF around if PCB is 4-layers with FR4 material. For layout, make sure that crystal, C1/C2 and related components are placed together to be close to MA35D1 XT1_IN pin and XT1_OUT pin to get that optimum performance and stability.

For details of C1/C2 value calculation, please refer to the application note “MA35D1 XTAL CL design note”.

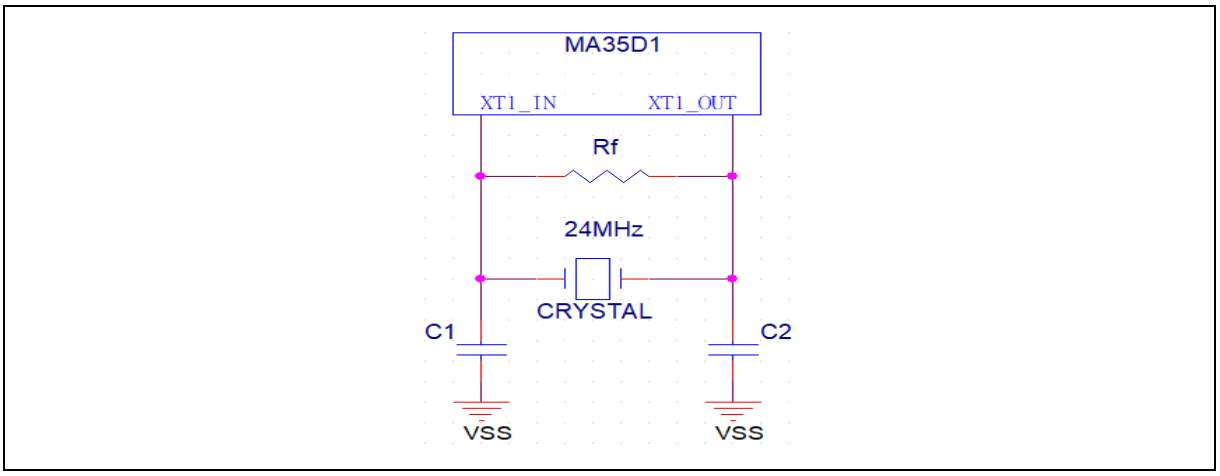


Figure 8-2 24 MHz Crystal Oscillator Circuit

Crystal	ESR (Ω)	C1, C2 (pF)	Condition
24 MHz	≦25	20	Assume that: XTAL CL=12pF PCB layout CL=4pF

Table 8-1 24 MHz C1/C2 Reference Value

8.3 LXT, Low Speed XTAL 32.768 kHz

About RTC 32.768 kHz oscillation circuit that C1 and C2 are recommended to use high-quality ceramic capacitors. Usually C1 and C2 have the same value by symmetry. Using 15 pF is recommended for resonating with 32.768 kHz crystal.

For getting the 32.768 kHz accurately, typical engineer can operate the timer counter machine to calibrate C1/C2 value or alternatively use software method that adjusts the MA35D1 RTC frequency compensation register to be close to 32.768 kHz.

For PCB layout XTAL, C1/C2 and related components must be placed together to be close to MA35D1 to X32_IN pin and X32_out pin ASAP to get optimum accuracy and stability.

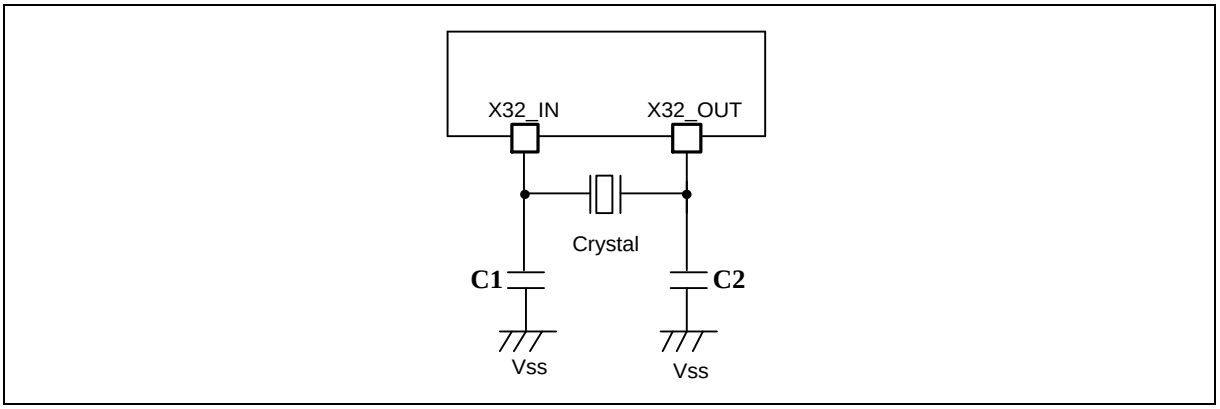


Figure 8-3 32.768 kHz Crystal Oscillator Circuit

Board Parameter	Symbol	Value
X32_IN, X32_OUT Capacitance	C1, C2	20 pf

Table 8-2 32.768 kHz C1 and C2 Recommend Value

9 External Bus Interface (EBI)

The EBI supports 8-/16-bit data width have three chip selects that can connect three external devices with different timing setting requirements.

The EBI supports dedicated external chip select pin with polarity control for each bank, and also supports accessible space up to 1 Mbytes for each bank. Actually external addressable space is dependent on package pin out.

EBI bus can support LCD interface i80 mode with PDMA, and support variable external bus base clock (MCLK) based on HCLK.

9.1 EBI Block Diagram

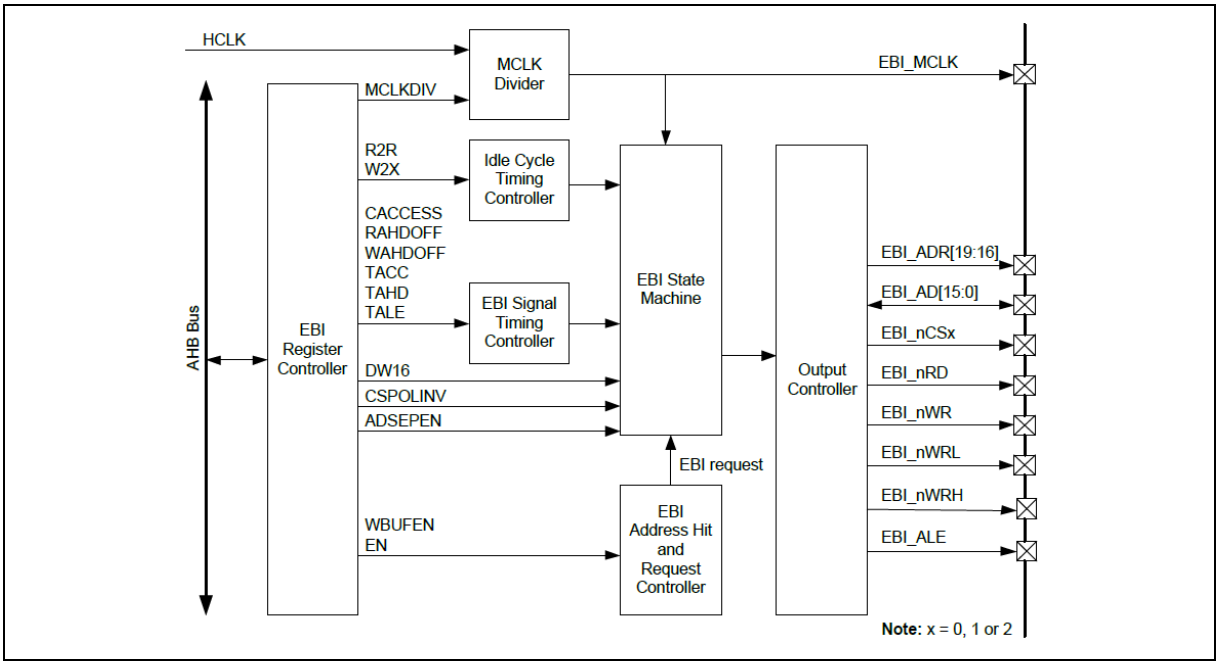


Figure 9-1 EBI Block Diagram

9.2 EBI Pin Configuration

Group	Pin Name	GPIO	MFP
	EBI_AD0	PL.12	MFP8
		PA.0	MFP7
		PG.11	MFP10
		PK.9	MFP8
	EBI_AD1	PL.13	MFP8
		PA.1	MFP7
		PG.12	MFP10

		PK.10	MFP8
	EBI_AD2	PL.14	MFP8
		PA.2	MFP7
		PG.13	MFP10
		PK.11	MFP8
	EBI_AD3	PL.15	MFP8
		PA.3	MFP7
		PG.14	MFP10
		PM.0	MFP8
	EBI_AD4	PA.4	MFP7
		PD.12	MFP8
		PG.15	MFP10
		PM.1	MFP8
	EBI_AD5	PA.5	MFP7
		PD.13	MFP8
		PL.6	MFP8
		PD.6	MFP9
		PM.2	MFP8
	EBI_AD6	PA.6	MFP7
		PD.14	MFP8
		PL.7	MFP8
		PD.7	MFP9
		PM.3	MFP8
	EBI_AD7	PA.7	MFP7
		PD.15	MFP8
		PL.8	MFP8
		PD.8	MFP9
		PM.4	MFP8
		PJ.0	MFP12
		PG.8	MFP12
	EBI_AD8	PA.8	MFP7
		PM.12	MFP8
		PL.9	MFP8

		PD.9	MFP9
		PM.5	MFP8
		PJ.1	MFP12
		PG.9	MFP12
	EBI_AD9	PA.9	MFP7
		PM.13	MFP8
		PL.10	MFP8
		PD.10	MFP9
		PM.6	MFP8
		PJ.2	MFP12
		PG.10	MFP12
	EBI_AD10	PA.10	MFP7
		PM.14	MFP8
		PL.11	MFP8
		PD.11	MFP9
		PM.7	MFP8
		PJ.3	MFP12
		PK.4	MFP12
	EBI_AD11	PL.12	MFP13
		PA.11	MFP7
		PM.15	MFP8
		PL.0	MFP8
		PM.8	MFP8
		PJ.0	MFP9
		PI.8	MFP12
	EBI_AD12	PL.13	MFP13
		PA.12	MFP7
		PL.1	MFP8
		PM.9	MFP8
		PJ.1	MFP9
		PI.9	MFP12
	EBI_AD13	PL.14	MFP13
		PA.13	MFP7

		PL.2	MFP8
		PM.10	MFP8
		PJ.2	MFP9
		PI.10	MFP12
		PB.9	MFP10
	EBI_AD14	PL.15	MFP13
		PA.14	MFP7
		PL.3	MFP8
		PM.11	MFP8
		PJ.3	MFP9
		PI.11	MFP12
		PB.10	MFP10
	EBI_AD15	PG.0	MFP7
		PK.8	MFP8
	EBI_ADR0	PA.0	MFP9
		PI.0	MFP8
		PK.9	MFP10
	EBI_ADR1	PA.1	MFP9
		PI.1	MFP8
		PK.10	MFP10
	EBI_ADR2	PA.2	MFP9
		PI.2	MFP8
		PK.11	MFP10
	EBI_ADR3	PA.3	MFP9
		PI.3	MFP8
		PM.0	MFP10
	EBI_ADR4	PA.4	MFP9
		PI.4	MFP8
		PM.1	MFP10
	EBI_ADR5	PA.5	MFP9
		PI.5	MFP8
		PM.2	MFP10
	EBI_ADR6	PA.6	MFP9

		PI.6	MFP8
		PM.3	MFP10
	EBI_ADR7	PA.7	MFP9
		PI.7	MFP8
		PM.4	MFP10
	EBI_ADR8	PA.8	MFP9
		PK.0	MFP8
		PM.5	MFP10
	EBI_ADR9	PA.9	MFP9
		PK.1	MFP8
		PM.6	MFP10
	EBI_ADR10	PA.10	MFP9
		PK.2	MFP8
		PM.7	MFP10
	EBI_ADR11	PA.11	MFP9
		PK.3	MFP8
		PM.8	MFP10
	EBI_ADR12	PA.12	MFP9
		PJ.12	MFP8
		PM.9	MFP10
	EBI_ADR13	PA.13	MFP9
		PJ.13	MFP8
		PM.10	MFP10
	EBI_ADR14	PA.14	MFP9
		PJ.14	MFP8
		PM.11	MFP10
	EBI_ADR15	PG.0	MFP15
		PJ.15	MFP8
		PK.8	MFP10
		PB.10	MFP9
	EBI_ADR16	PG.2	MFP7
		PJ.0	MFP10
		PB.12	MFP9

	EBI_ADR17	PG.3	MFP7
		PJ.1	MFP10
		PB.13	MFP9
	EBI_ADR18	PB.14	MFP9
		PG.4	MFP7
		PJ.2	MFP10
	EBI_ADR19	PB.15	MFP9
		PG.5	MFP7
		PJ.3	MFP10
	EBI_ALE	PD.15	MFP7
		PA.15	MFP7
		PG.5	MFP8
		PG.14	MFP7
		PB.9	MFP9
		PB.11	MFP10
	EBI_MCLK	PD.14	MFP7
		PG.3	MFP9
		PG.13	MFP7
		PK.8	MFP9
		PB.10	MFP6
	EBI_nCS0	PG.1	MFP7
		PG.4	MFP8
		PG.15	MFP7
		PJ.0	MFP11
		PG.8	MFP13
		PB.8	MFP9
	EBI_nCS1	PD.12	MFP7
		PG.3	MFP8
		PG.11	MFP8
		PJ.1	MFP11
		PG.9	MFP13
	EBI_nCS2	PD.13	MFP7
		PG.2	MFP8

		PB.11	MFP9
	EBI_nRD	PG.6	MFP7
		PL.4	MFP8
	EBI_nWR	PG.7	MFP7
		PL.5	MFP8
	EBI_nWRH	PG.11	MFP7
		PL.10	MFP11
		PJ.2	MFP11
		PG.10	MFP13
	EBI_nWRL	PG.12	MFP7
		PL.11	MFP11
		PJ.3	MFP11
		PK.4	MFP13

Table 9-1 EBI Pin List

9.3 EBI Connectivity

The pin configuration table is to connect the EBI bus to connector for external devices connectivity, such as SRAM, LCD.

The EBI supports the device whose address bus and data bus are multiplexed. For the external device with separated address and data bus, the connection to device needs additional latch device to latch the address. In this case, the pin EBI_ALE is connected to the latch device to latch the address value. Pin EBI_AD is the input of the latch device, and the output of the latch device is connected to the address of external device.

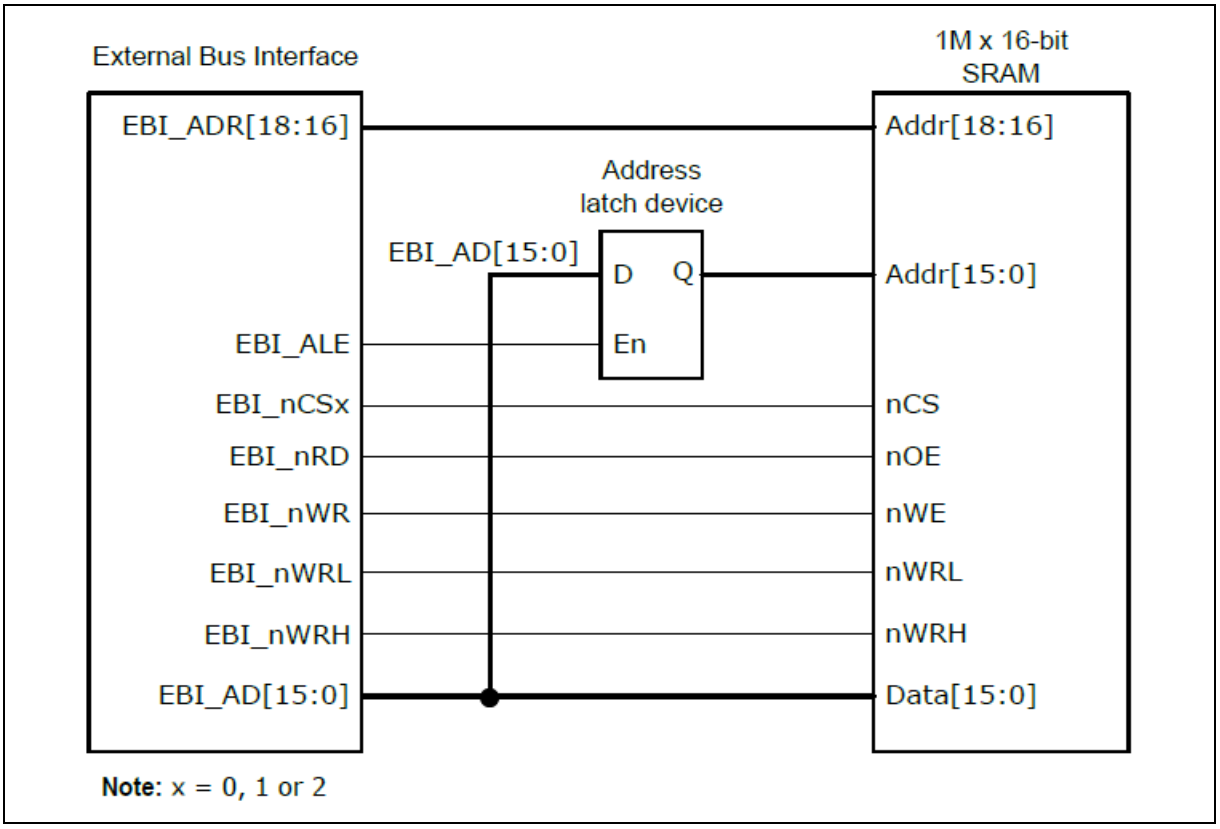


Figure 9-2 Connection of 16-bit EBI Data Width with 16-bit Device

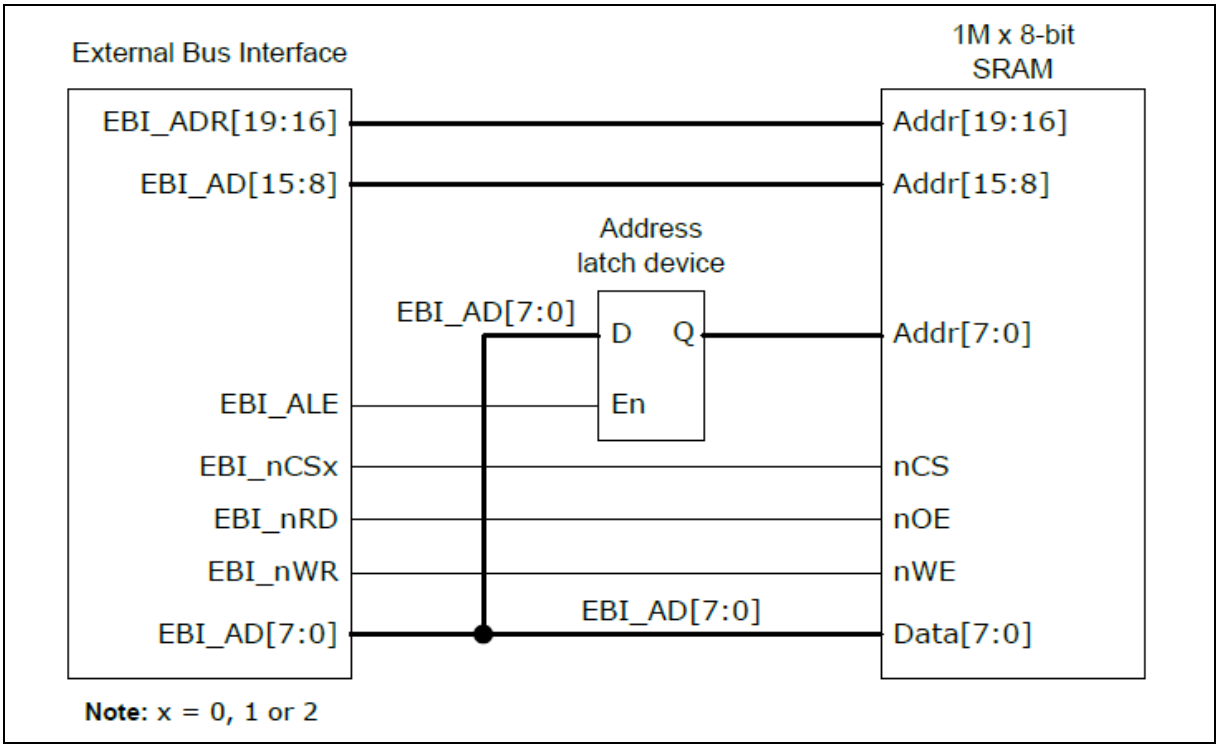


Figure 9-3 Connection of 8-bit EBI Data Width with 8-bit Device

10 SAR_ADC

The MA35D1 series contains two 12-bit Successive Approximation Register analog-to-digital converters (SAR A/D converter).

- ADC (Analog-to-Digital Converter)

  8 input channels. The A/D converter supports two operation modes: 4-wire or 5-wire mode. The ADC is especially suitable to act as touch screen controller.

- EADC (Enhanced Analog-to-Digital Converter)

  8 external input channels and 1 internal channel and 4 pair differential analog input channels. The ADC converter can be started by
  software trigger, EPWM0/1/2 triggers, Timer0~11 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

10.1 ADC Features

- Resolution: 12-bit resolution
- DNL: ±1.5 LSB, INL: ±3 LSB
- Maximum ADC clock frequency is 16 MHz
- Up to 727.2 KSPS conversion rate when ADC clock frequency is 16 MHz in high speed mode
- Up to 145.4 KSPS conversion rate when ADC clock frequency is 3.2 MHz in low speed mode
- Analog Input Range: V_{REF} to AGND, can be rail-to-rail
- Analog Supply: 2.7~3.6V
- 8 Single-Ended analog inputs
- Compatible with 4-wire or 5-wire Touch Screen Interface
- Low Power Consumption: 600uA (727.2 KSPS)/300uA (145.4 KSPS)

The ADC output coding is offset in binary, 1LSB=V_{REF}/4096. The transfer characteristic is shown in Figure 10-1.

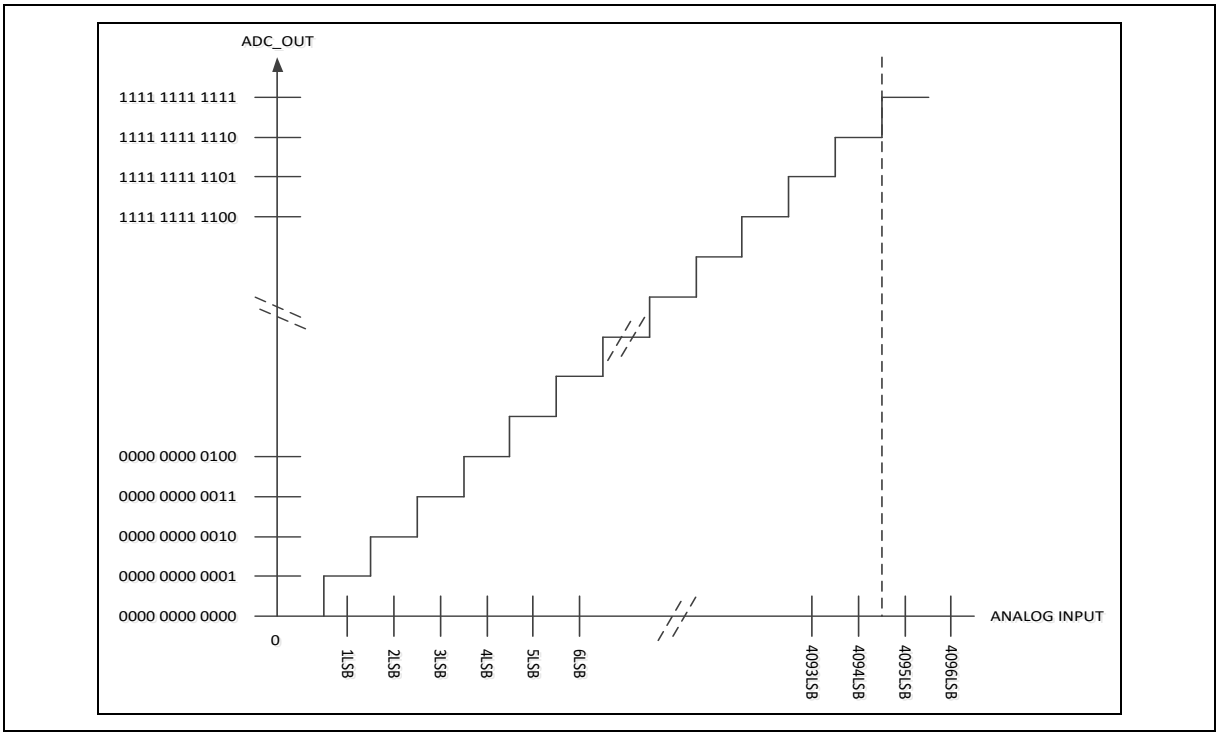


Figure 10-1 ADC Transfer Function

Group	Pin Name	GPIO	MFP
ADC	ADC_CH0	PB.8	MFP8
	ADC_CH1	PB.9	MFP8
	ADC_CH2	PB.10	MFP8
	ADC_CH3	PB.11	MFP8
	ADC_CH4	PB.12	MFP8
	ADC_CH5	PB.13	MFP8
	ADC_CH6	PB.14	MFP8
	ADC_CH7	PB.15	MFP8

Table 10-1 ADC Interfaces Pin List

10.1.1 ADC Selection of Input Signal

CHSEL[2:0]	Select ADC Analog Input Signal	Description
000	ADC_CH0	Positive ADC reference voltage input or Normal ADC analog input
001	ADC_CH1	Normal ADC analog input
010	ADC_CH2	Normal ADC analog input

011	ADC_CH3	Used for 4-wire touch screen detection(V_{SESE}) or Normal ADC analog input
100	ADC_CH4	If used in touch screen, it should connect to the negative end of Y axis(YM). If used in 4-wire touch screen, it should connect to the lower-left electrode or Normal ADC analog input
101	ADC_CH5	If used in touch screen, it should connect to the positive end of Y axis(YP). If used in 4-wire touch screen, it should connect to the upper-right electrode or Normal ADC analog input
110	ADC_CH6	If used in touch screen, it should connect to the negative end of X axis(XM). If used in 4-wire touch screen, it should connect to the lower-right electrode or Normal ADC analog input
111	ADC_CH7	If used in touch screen, it should connect to the positive end of X axis(XP). If used in 4-wire touch screen, it should connect to the upper-left electrode or Normal ADC analog input

Table 10-2 ADC Chanel Selection

10.1.2 Selection of Reference Voltage

REFSEL[1:0]	ADC Analog Reference Pair Selection Signals
00	AV_{SS} to V_{REF} input(ADC0_CH0)
01	YM to YP
10	XM to XP
11	AV_{SS} to AVDD_ADC0

Table 10-3 ADC Reference Voltage Select

Note: Reference voltage can be selected according to the application. When REFSEL is set to 00, reference voltage of ADC is switched to V_{REF} pin. When REFSEL is set to 11, reference voltage of ADC is switched to AVDD_ADC0. For 4-wire/5-wire touch Screen Y axis conversion, REFSEL can be set to 01. For 4-wire/5-wire touch Screen X axis conversion, REFSEL can be set to 10.

10.2 EADC Features

- Analog input voltage range: 0~V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution
- Up to 8 single-end analog external input channels and 4 pair differential analog input channels
- Up to 1 internal channel for Battery power (V_{BAT})
- Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum ADC clock frequency of 80 MHz
- Up to 4.7 MSPS conversion rate when ADC clock frequency is 80 MHz in high speed mode
- Up to 941.1 KSPS conversion rate when ADC clock frequency is 16 MHz in low speed mode
- Configurable ADC internal sampling time
- Supports calibration function
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 9 sample modules:
  - Each of sample modules which is configurable for ADC converter channel EADC_CH0~7 and trigger source
  - Sample module eight is fixed for ADC channel 8 input source as battery power (V_{BAT})
  - Double buffer for sample control logic module0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 9 data registers with valid and overrun indicators
- An ADC conversion can be started by:
  - Write 1 to SWTRG (EADC_SWTRG[n], n=0~8)
  - External pin EADC0_ST

- Timer0~11 overflow pulse triggers
- ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
- EPWM triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

Group	Pin Name	GPIO	MFP
EADC	EADC_CH0		
	EADC_CH4		
	EADC_CH1		
	EADC_CH5		
	EADC_CH2		
	EADC_CH6		
	EADC_CH3		
	EADC_CH7		
	EADC_ST	PF.14	MFP2
		PG.0, PJ.15, PK.1	MFP6
		PK.8	MFP7
		PK.5, PN.15	MFP9
		PD.7	MFP11

Table 10-4 EADC Interfaces Pin List

10.2.1 EADC Selection in the Single-end Input Mode

CHSEL[3:0]	Select EADC Analog Input Signal(VIN)
0000	EADC_CH0
0001	EADC_CH1
0010	EADC_CH2
0011	EADC_CH3
0100	EADC_CH4
0101	EADC_CH5
0110	EADC_CH6
0111	EADC_CH7
1000	$V_{BAT}/4$

Table 10-5 EADC Single-end Mode Channel Selection

- For single-end input mode, the ADC output code:
  - ADC[11:0]=V_{IN}/(V_{REF}-0)*4096

10.2.2 EADC Selection in the Differential Input Mode

Differential Analog Input Paired Channel	ADC Analog Input	
	Vplus	Vminus
0	EADC_CH0	EADC_CH4
1	EADC_CH1	EADC_CH5
2	EADC_CH2	EADC_CH6
3	EADC_CH3	EADC_CH7

Table 10-6 EADC Differential Mode Channel Selection

- For differential input mode, the ADC output code:
  - ADC[11:0]= (Vplus-Vminus)/[2*(V_{REF}-0)]*4096_2048

10.2.3 EADC Internal Channel for V_{BAT} Measurement

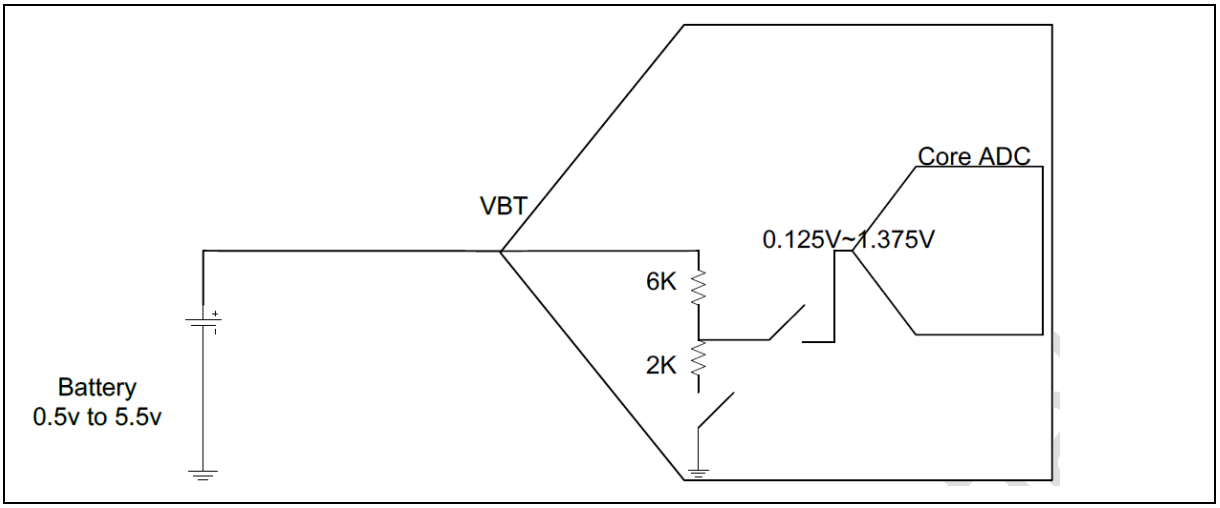


Figure 10-2 V_{BAT} Battery Measurement, Inner Function Block Diagram

11 USB

The MA35D1 USB0 supports USB 2.0 High Speed Dual Role (Host/Device). The USB1 is dedicated support USB 2.0 High Speed Host Controller.

The following guidelines will provide PCB design considerations for system designer reference.

11.1 USB Termination

For getting a good USB signals quality and USB Eye-Diagram to meet USB compliant test electrical characteristic that USB bus must be request that 90 Ω impedance for PCB layout.

Normally, the USB terminator resistors and terminator capacitors should be close and placed to USB termination, i.e. the purpose is for USB eye diagram and USB signal quality matching impedance 90 Ω correction.

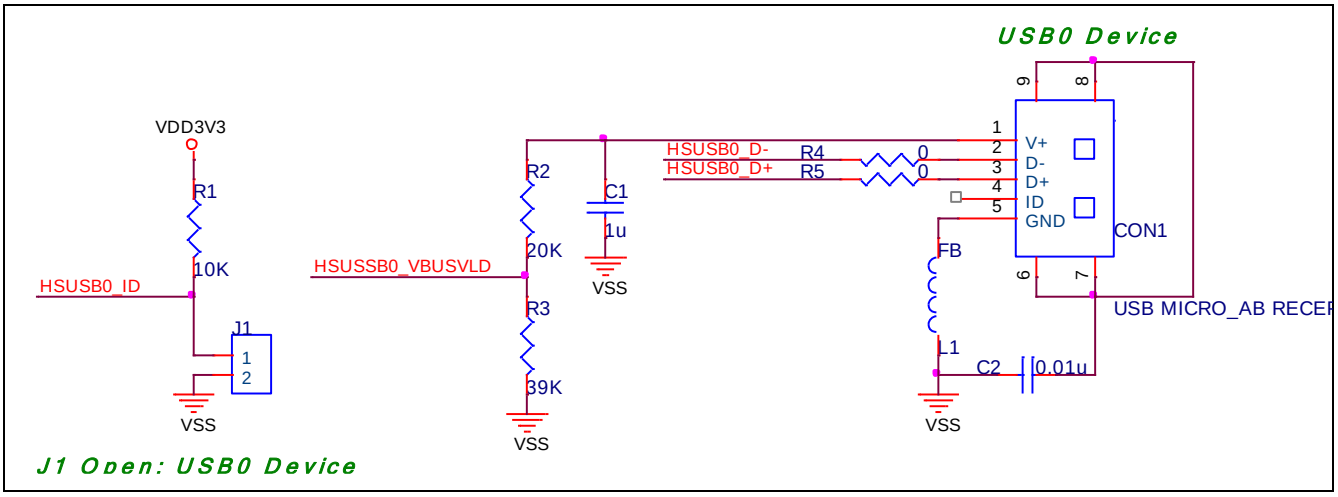


Figure 11-1 Example for USB0 Device Termination Connection

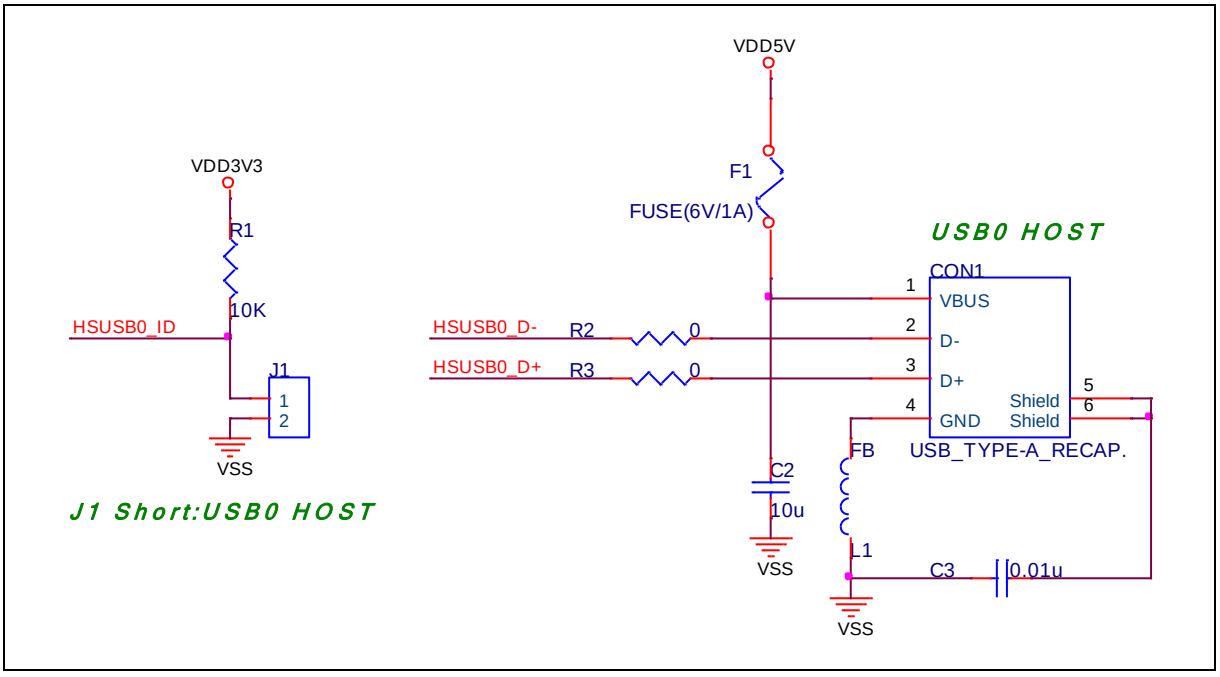


Figure 11-2 Example for USB0 HOST Termination Connection

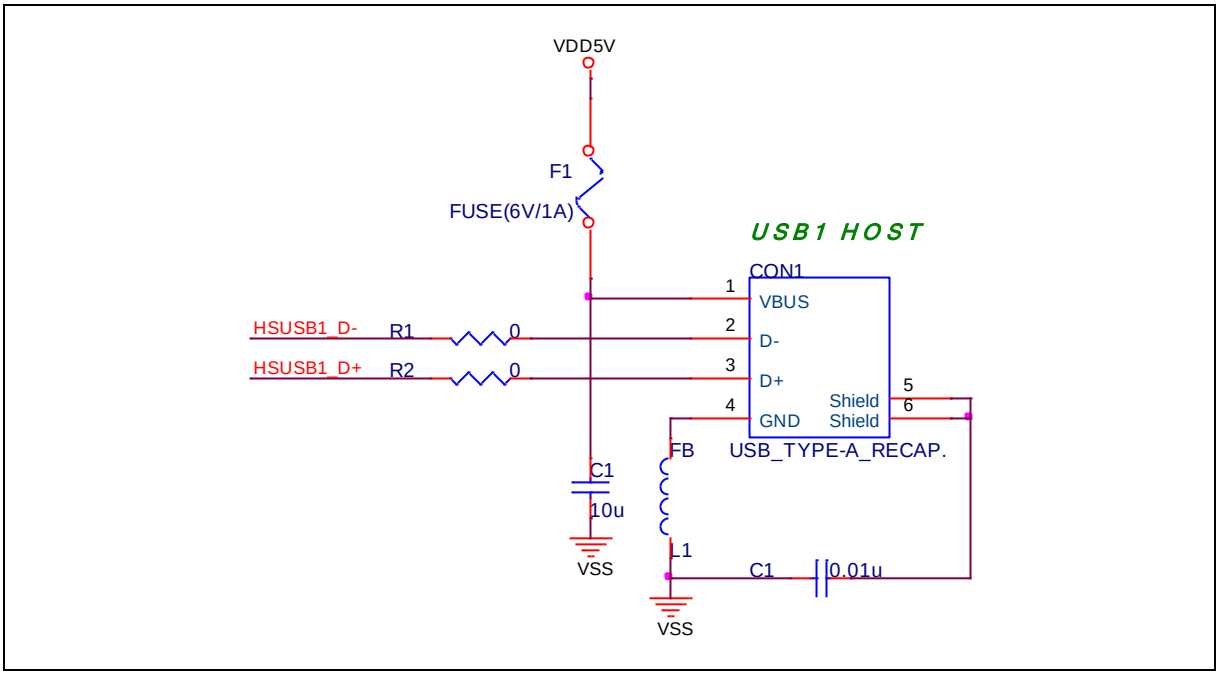


Figure 11-3 Example for USB1 HOST Termination Connection

11.2 USB Power

The PCB design also needs to consider USB power and ground as Figure 11-4, VDD_HSUSBx and V_{SS}, which are isolated with ferrite bead or 0 Ω resistor for reducing possible power noise from system.

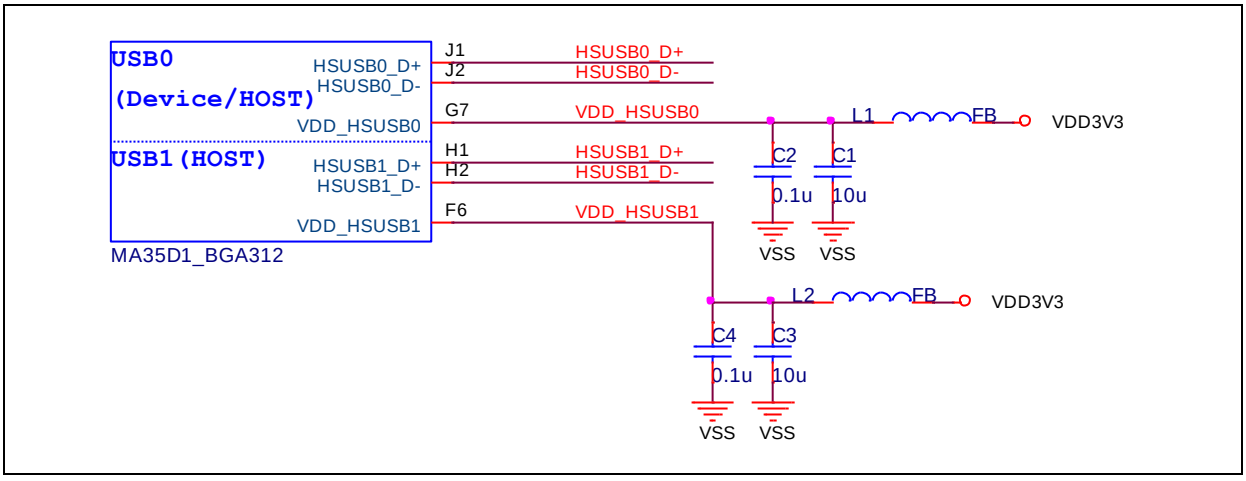


Figure 11-4 Example of USB Power Connection

11.3 PCB Layout Considerations

Traces the DP/DM to the connector, the signal swing during high-speed operation on the DP/DM line is relatively a small waveform about 400 mV. So, if there is any differential noise picked up will affect transceiver signal on the pair traces. When the DP/DM traces are not shield, the traces behave like an antenna to pick up noise by the surrounding components.

To lower the interference effect, use the following general routing and placement guidelines when laying out a new design. These guidelines will help to minimize signal quality and EMI problems.

The high speed USB validation efforts focus on a four-layer PCB where the first layer is a signal layer, the second layer is power, the third layer is ground and the fourth is a signal layer. This results in placing most of the routing on the fourth layer closest to the ground layer, and allowing a higher component density on the first layer.

11.3.1 Layout Guidelines

- DP/DM traces should be length matched and as close as possible to the connector.
- Route DP/DM traces should be close together for noise rejection on the differential signals, parallel to each other and the length difference within 200 mil.
- If the common chock is necessary, it should be as close as to the connector.
- No extra components at DP/DM pair traces to maintain signal integrity.
- No de-coupled caps on the DP/DM.
- The characteristic of matching impedance 90 Ω on the DP/DM is necessary.
- Stubs on high speed USB signals should be avoided, as stubs will cause signal reflections and affect signal quality. If a stub is unavoidable in the design, no stub should be greater than 200 mils.

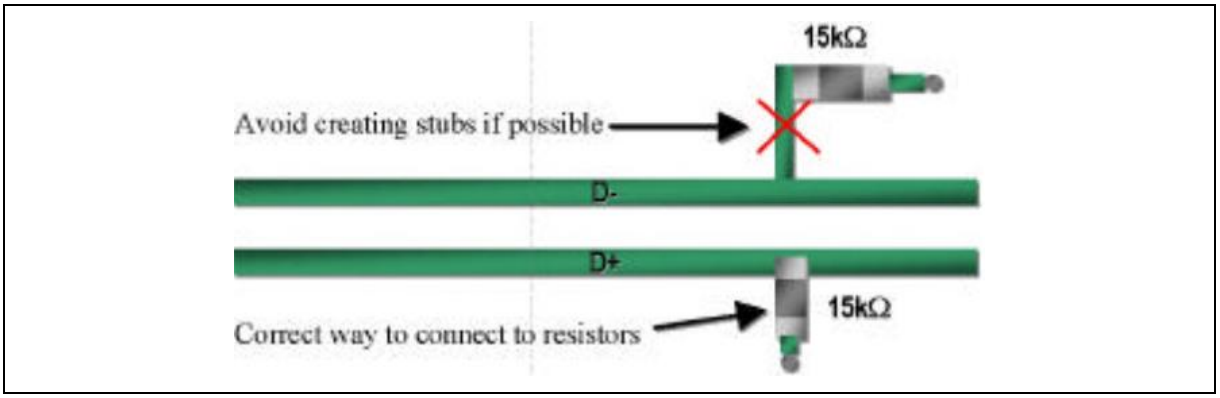


Figure 11-5 BUS Stubs Should Be Avoided

- Route all traces over continuous planes (V_{CC} or GND), with no interruptions. Avoid crossing over anti-etch if at all possible. Crossing over anti-etch (plane splits) increases inductance and radiation levels by forcing a greater loop area. Likewise, avoid changing layers with high-speed traces as much as practical. It is preferable to change layers to avoid crossing a plane split.
- Use the following guidelines for the V_{CC} OR GND plane.
- Traces should not cross anti-etch, for it greatly increases the return path for those signal traces. This applies to High Speed USB signals, high-speed clock and signal traces as well as slower signal traces, which might be coupling to them. USB signaling is not purely differential in all speeds (i.e. the FS Single Ended Zero is common mode)
- Avoid routing of USB signals within 25 mils of any anti-etch to avoid coupling to the next split or radiating from the edge of the PCB.
- Separate signal traces into similar categories and route similar signal traces together (such as routing differential pairs together).
- Keep high-speed USB signals clear of the core logic set. High current transients are produced during internal state transitions and can be very difficult to filter out.
- Follow the 20*h thumb rule by keeping traces at least 20*(height above the plane) away from the edge of the plane (V_{CC} or GND, depending on the plane the trace is over). For the suggested stack up the height above the plane are 4.5 mils. This calculates to a 90 mil spacing requirement from the edge of the plane. This helps prevent the coupling of the signal onto adjacent wires and also helps prevent free radiation of the signal from the edge of the PCB.

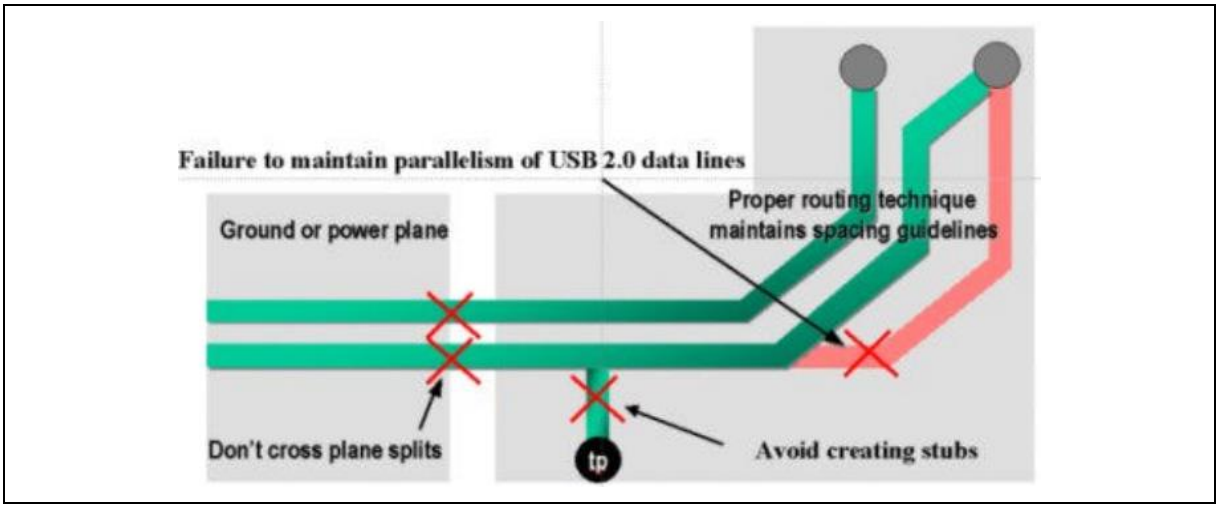


Figure 11-6 Maintain Parallelism USB BUS

11.3.2 Through Hole Consideration for D+ and D-

For the two-layer or multi-layer of PCB, when the signals of D+ and D- need to be through another layer, in which the resistively of through hole should be concerned. To lower the resistively issue for the sensitivity case, the two-via or multi-via should be adapted, as Figure 11-7.

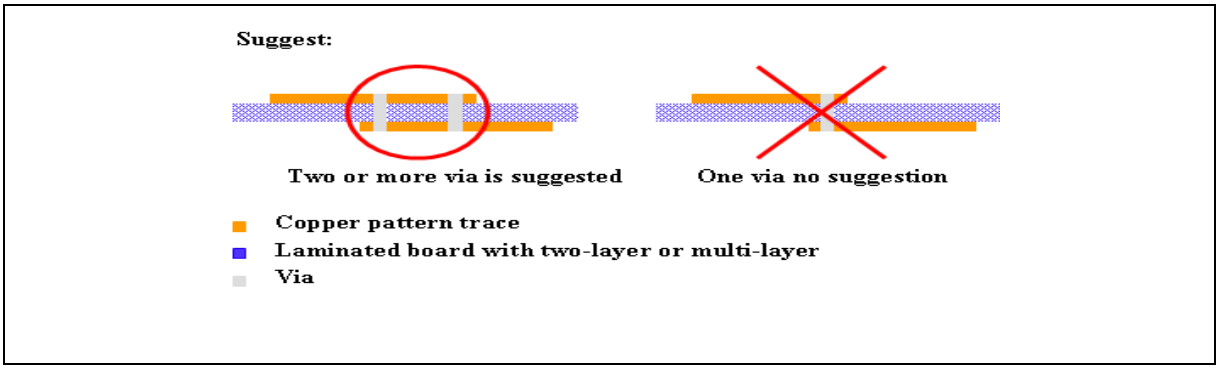


Figure 11-7 Through Hole for D+ and D-

11.3.3 USB High Speed Trace Spacing

Figure 11-8 provides an illustration of the recommended trace spacing for multi-layer PCB.

- Maintain parallelism between USB differential signals with the trace spacing needed to achieve 90 Ω differential impedance. Deviations will normally occur due to package breakout and routing to connector pins. Just ensure the amount and length of the deviation is kept to the minimum possible.
- Use an impedance calculator to determine the trace width and spacing required for the specific board stack up being used. For the board stack up parameters referred to in Layer Stacking, 7.5 mil traces with 7.5 mil spacing results in approximately 90 Ω differential trace impedance.

- Minimize the length of high-speed clock and periodic signal traces that run parallel to high speed USB signal lines, to minimize crosstalk. Based on EMI testing experience, the minimum suggested spacing to clock signals is 50 mils.
- Based on simulation data, use 20 mil minimum spacing between high-speed USB signal pairs and other signal traces for optimal signal quality. This helps to prevent crosstalk.

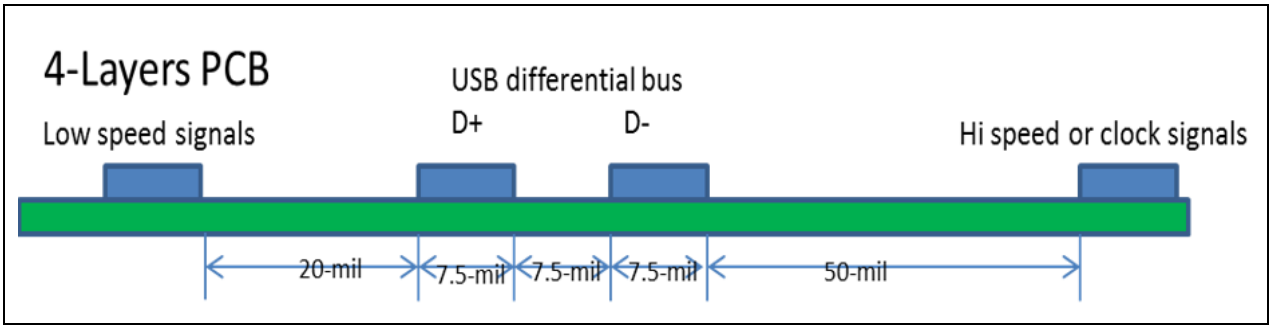


Figure 11-8 Multi-layer PCB USB Bus Trace Space Recommendation

11.3.4 High Speed USB Trace Length

Main board's USB signal pairs total trace length should be less than or equal to 18 inches.

11.3.5 PCB Stacking for USB

Figure 11-9 is an example of PCB layout stack-up for USB 4-Layer Stack-Up:

- Layer-1 Signal (top)
- Layer-2 V_{CC}
- Layer-3 GND
- Layer-4 Signal (bottom)

In this case, high speed USB validation PCB uses 7.5 mil traces with 7.5 mil spacing between differential pairs to obtain 90 Ω differential impedance. The PCB specific board stack up used is as Figure 11-9.

- 1 oz. copper
- Prepreg at 4.5 mils
- Core at 53 mils
- PCB thickness at 63 mils (1.6 mm)
- FR4 material

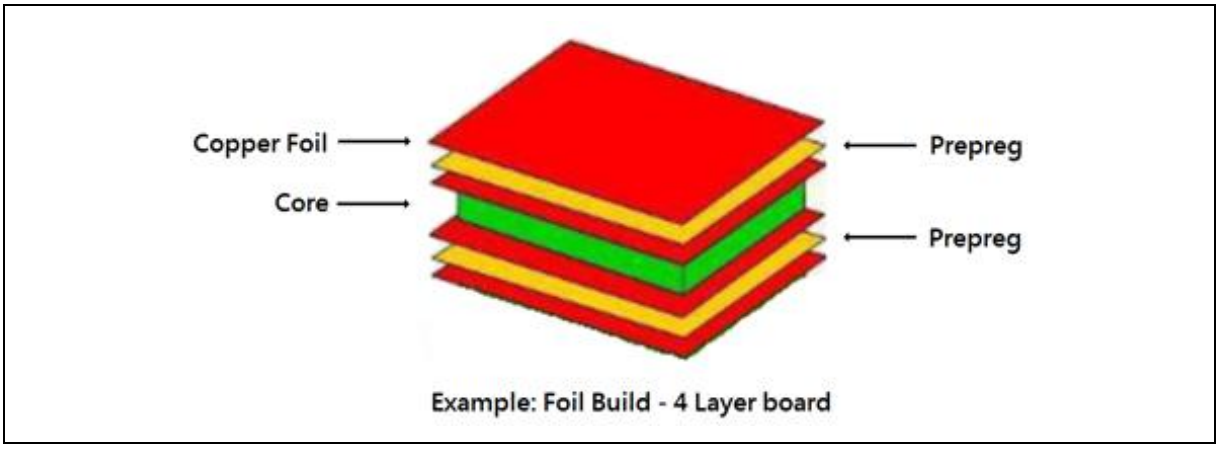


Figure 11-9 4-layer PCB Structures

11.3.6 USB EMI/ESD Considerations

The following guidelines apply to the selection and placement of common mode chokes and ESD protection devices.

11.3.7 EMI - Common Mode Chokes

Testing has shown that common mode chokes can provide required noise attenuation. A design may include a common mode choke footprint to provide a stuffing option in the event the choke is needed to pass EMI testing. Figure 11-10 shows the schematic of a typical common mode choke and ESD suppression components. The choke should be placed as close as possible to the USB connector signal pins.

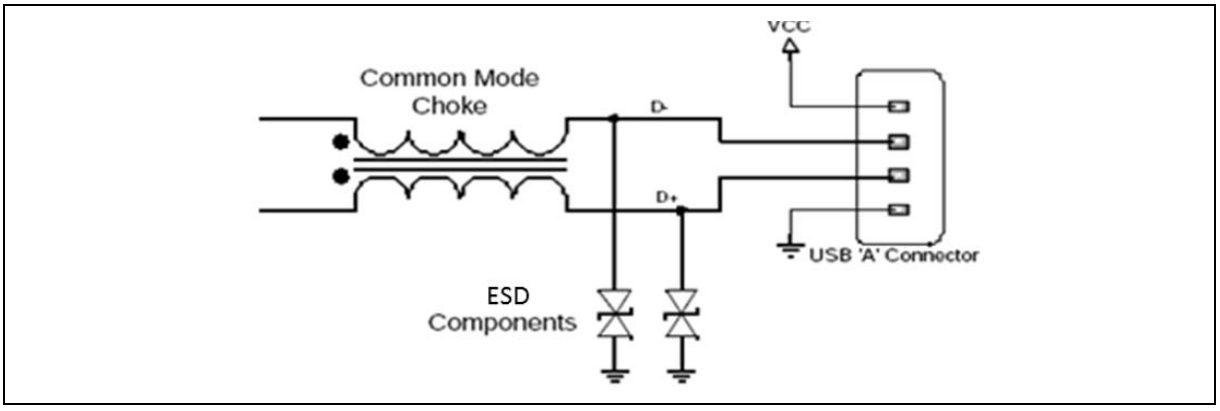


Figure 11-10 Common Mode Choke

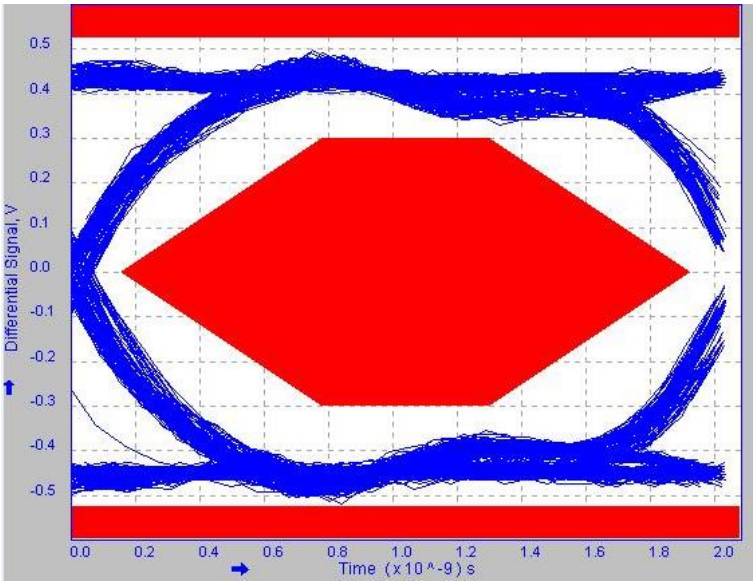


Figure 11-11 USB Port0 High Speed Device

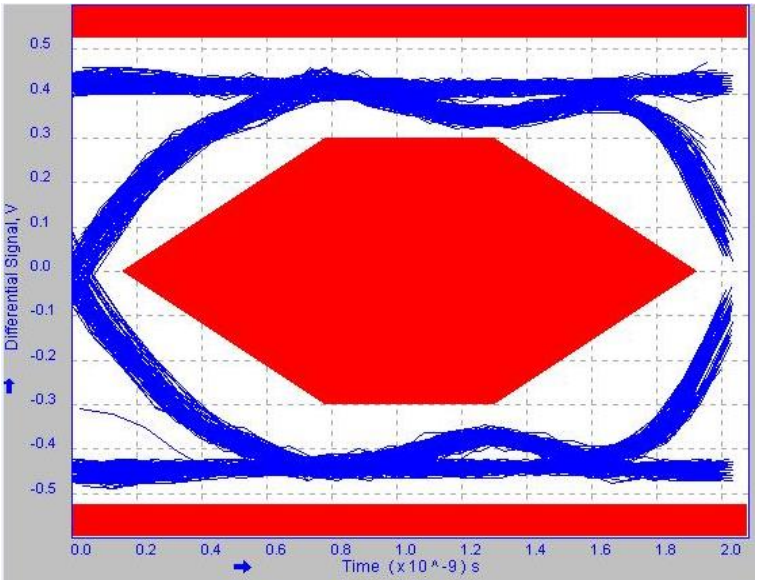


Figure 11-12 USB Port0 High Speed Device

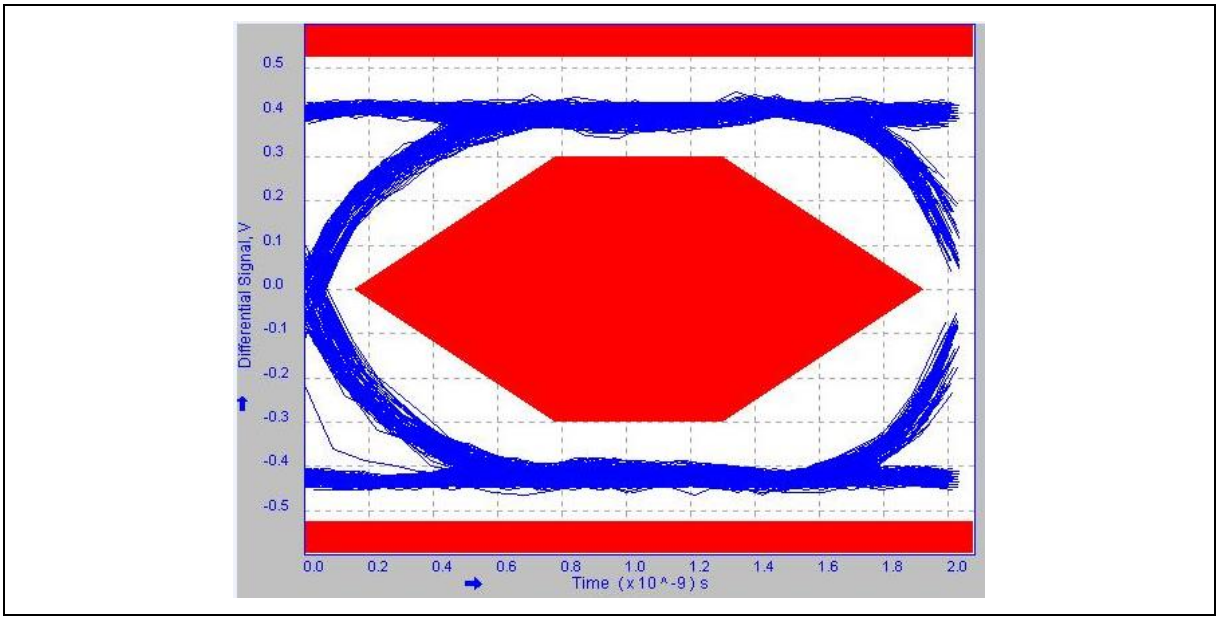


Figure 11-13 USB Port1 High Speed Device

The eye diagram above shows USB signal quality, as the common mode impedance increases, this distortion will increase, so you should test the effects of the common mode choke on full speed and high-speed signal quality.

Finding a common mode choke that meets the designer's needs is a two-step process.

- A part must be chosen with the impedance value that provides the required noise attenuation. This is a function of the electrical and mechanical characteristics of the part chosen, and the frequency and strength of the noise present on the USB traces that the designer is trying to suppress.
- Once the designer has a part that gives passing EMI results, the second step is to test the effect this part has on signal quality. Higher impedance common mode chokes generally have a greater damaging effect on signal quality, so be careful about increasing the impedance without doing thorough testing. Thorough testing means that the signal quality must be checked for Low speed, Full speed and High speed USB operation.

11.3.8 USB ESD Solution

Low-speed and full-speed USB provide ESD suppression using in-line ferrites and capacitors that formed a low pass filter. This technique does not work for high speed USB due to the much higher signal rate of HS data. Thus, for high speed USB solution designer should select proper low-capacitance ESD protection devices to resolve.

As with the common mode choke solution, it is suggested to include the footprints for this device, or some other proven solution, as a stuffing option in case it is needed to pass ESD testing.

ESD protection and common mode chokes are only needed if the design does not pass EMI or ESD testing. Footprints for common mode chokes and/or ESD suppression components should be included in the event that a problem occurs.

12 Ethernet

The MA35D1 provides two Ethernet MAC Controllers (EMAC) for Network application.

The MA35D1 supports both half and full duplex for 10 Mbps, 100 Mbps or 1000 Mbps operation; the EMAC supports RMII (Reduced Media Independent Interface) and RGMII (Reduced Gigabit Media Independent Interface) interface to connect with external Ethernet PHY.

Group	Pin Name	GPIO	MFP	Type	Description
RGMII0	RGMII0_MDC	PE.0	MFP8	O	RGMII0 PHY Management Clock output pin
	RGMII0_MDIO	PE.1	MFP8	I/O	RGMII0 PHY Management Data pin
	RGMII0_PPS	PL.12	MFP14	O	RGMII0 Pulse Per Second output pin
		PA.15	MFP14	O	
		PF.14	MFP8	O	
	RGMII0_RXCLK	PE.5	MFP8	I	RGMII0 Mode RX Clock input pin
	RGMII0_RXCTL	PE.6	MFP8	I	RGMII0 Receive Control input pin
	RGMII0_RXD0	PE.7	MFP8	I	RGMII0 Receive Data bus bit 0
	RGMII0_RXD1	PE.8	MFP8	I	RGMII0 Receive Data bus bit 1
	RGMII0_RXD2	PE.9	MFP8	I	RGMII0 Receive Data bus bit 2
	RGMII0_RXD3	PE.10	MFP8	I	RGMII0 Receive Data bus bit 3
		PF.0	MFP6	I	
	RGMII0_TXCLK	PE.11	MFP8	O	RGMII0 Mode TX Clock output pin
		PF.1	MFP6	O	
	RGMII0_TXCTL	PE.2	MFP8	O	RGMII0 Transmit Control output pin
	RGMII0_TXD0	PE.3	MFP8	O	RGMII0 Transmit Data bus bit 0
	RGMII0_TXD1	PE.4	MFP8	O	RGMII0 Transmit Data bus bit 1
	RGMII0_TXD2	PE.12	MFP8	O	RGMII0 Transmit Data bus bit 2
		PF.2	MFP6	O	
	RGMII0_TXD3	PE.13	MFP8	O	RGMII0 Transmit Data bus bit 3
		PF.3	MFP6	O	
RGMII1	RGMII1_MDC	PF.0	MFP8	O	RGMII1 PHY Management Clock output pin
	RGMII1_MDIO	PF.1	MFP8	I/O	RGMII1 PHY Management Data pin
	RGMII1_PPS	PL.13	MFP14	O	RGMII1 Pulse Per Second output pin
		PG.1	MFP14	O	

		PF.14	MFP3	O	
	RGMII1_RXCLK	PF.5	MFP8	I	RGMII1 Mode RX Clock input pin
	RGMII1_RXCTL	PF.6	MFP8	I	RGMII1 Receive Control input pin
	RGMII1_RXD0	PF.7	MFP8	I	RGMII1 Receive Data bus bit 0
	RGMII1_RXD1	PF.8	MFP8	I	RGMII1 Receive Data bus bit 1
	RGMII1_RXD2	PF.9	MFP8	I	RGMII1 Receive Data bus bit 2
	RGMII1_RXD3	PF.10	MFP8	I	RGMII1 Receive Data bus bit 3
	RGMII1_TXCLK	PF.11	MFP8	O	RGMII1 Mode TX Clock output pin
	RGMII1_TXCTL	PF.2	MFP8	O	RGMII1 Transmit Control output pin
	RGMII1_TXD0	PF.3	MFP8	O	RGMII1 Transmit Data bus bit 0
	RGMII1_TXD1	PF.4	MFP8	O	RGMII1 Transmit Data bus bit 1
	RGMII1_TXD2	PF.12	MFP8	O	RGMII1 Transmit Data bus bit 2
	RGMII1_TXD3	PF.13	MFP8	O	RGMII1 Transmit Data bus bit 3
RMII0	RMII0_CRSDV	PE.6	MFP9	I	RMII0 Carrier Sense/Receive Data input pin
	RMII0_MDC	PE.0	MFP9	O	RMII0 PHY Management Clock output pin
	RMII0_MDIO	PE.1	MFP9	I/O	RMII0 PHY Management Data pin
	RMII0_PPS	PL.12	MFP15	O	RMII0 Pulse Per Second output pin
		PA.15	MFP15	O	
		PF.14	MFP9	O	
	RMII0_REFCLK	PE.5	MFP9	I	RMII0 Reference Clock input pin
	RMII0_RXD0	PE.7	MFP9	I	RMII0 Receive Data bus bit 0
	RMII0_RXD1	PE.8	MFP9	I	RMII0 Receive Data bus bit 1
	RMII0_RXERR	PE.9	MFP9	I	RMII0 Receive Data Error input pin
	RMII0_TXD0	PE.3	MFP9	O	RMII0 Transmit Data bus bit 0
	RMII0_TXD1	PE.4	MFP9	O	RMII0 Transmit Data bus bit 1
	RMII0_TXEN	PE.2	MFP9	O	RMII0 Transmit Enable output pin
RMII1	RMII1_CRSDV	PF.6	MFP9	I	RMII1 Carrier Sense/Receive Data input pin
	RMII1_MDC	PF.0	MFP9	O	RMII1 PHY Management Clock output pin
	RMII1_MDIO	PF.1	MFP9	I/O	RMII1 PHY Management Data pin
	RMII1_PPS	PL.13	MFP15	O	RMII1 Pulse Per Second output pin
		PG.1	MFP15	O	
		PF.14	MFP4	O	
	RMII1_REFCLK	PF.5	MFP9	I	RMII1 Reference Clock input pin

	RMII1_RXD0	PF.7	MFP9	I	RMII1 Receive Data bus bit 0
	RMII1_RXD1	PF.8	MFP9	I	RMII1 Receive Data bus bit 1
	RMII1_RXERR	PF.9	MFP9	I	RMII1 Receive Data Error input pin
	RMII1_TXD0	PF.3	MFP9	O	RMII1 Transmit Data bus bit 0
	RMII1_TXD1	PF.4	MFP9	O	RMII1 Transmit Data bus bit 1
	RMII1_TXEN	PF.2	MFP9	O	RMII1 Transmit Enable output pin

Table 12-1 RGMII0/1 and RMII0/1 Interfaces Pin List

The following recommendation will help users to gain maximum performance.

- Make a stable and low-noise environment for Ether Net PHY working
- Make a better circuit for Ethernet PHY by simplifying signal trace
- Reduce EMI and EMC
- Make better ESD protecting

12.1 RGMII PHY Layout Guideline (Refer to Realtek RTL8211F(D)I Design Guide)

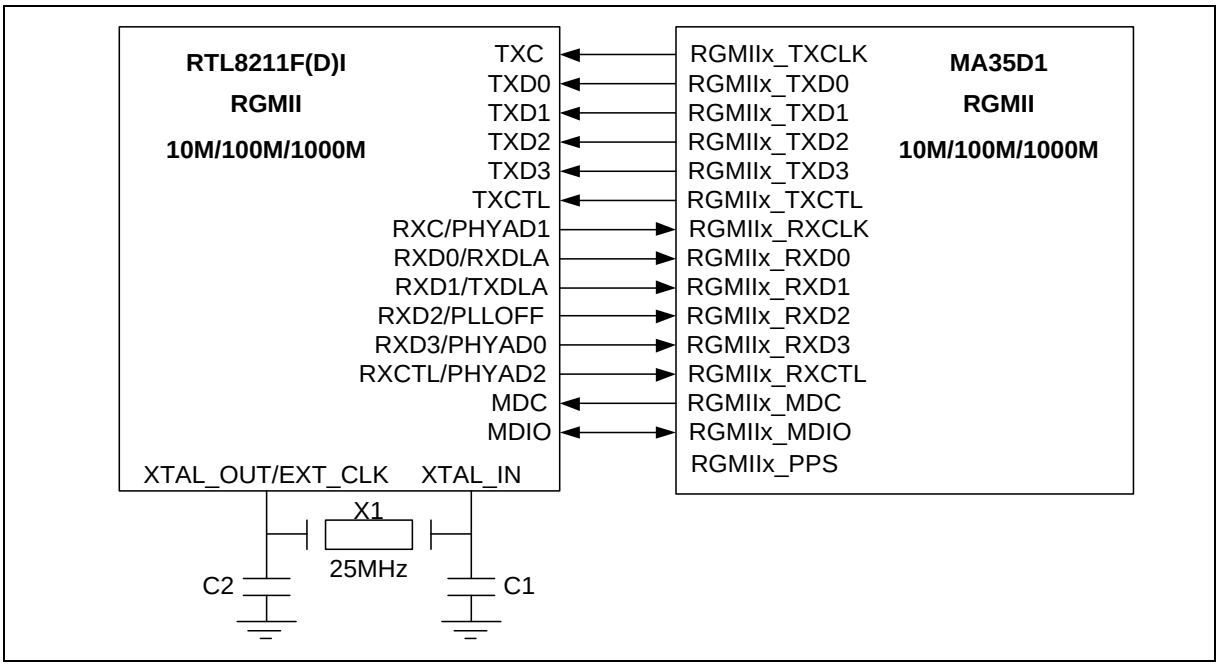


Figure 12-1 RGMII Interface Connection

12.1.1 Placement

- The PHY must be placed as close as possible to the MA35D1 (less than 15 cm)
- The 10/100/1000M magnetics shout be placed as close as possible to the RJ-45

connector. The MDI traces must be less than 12 cm.

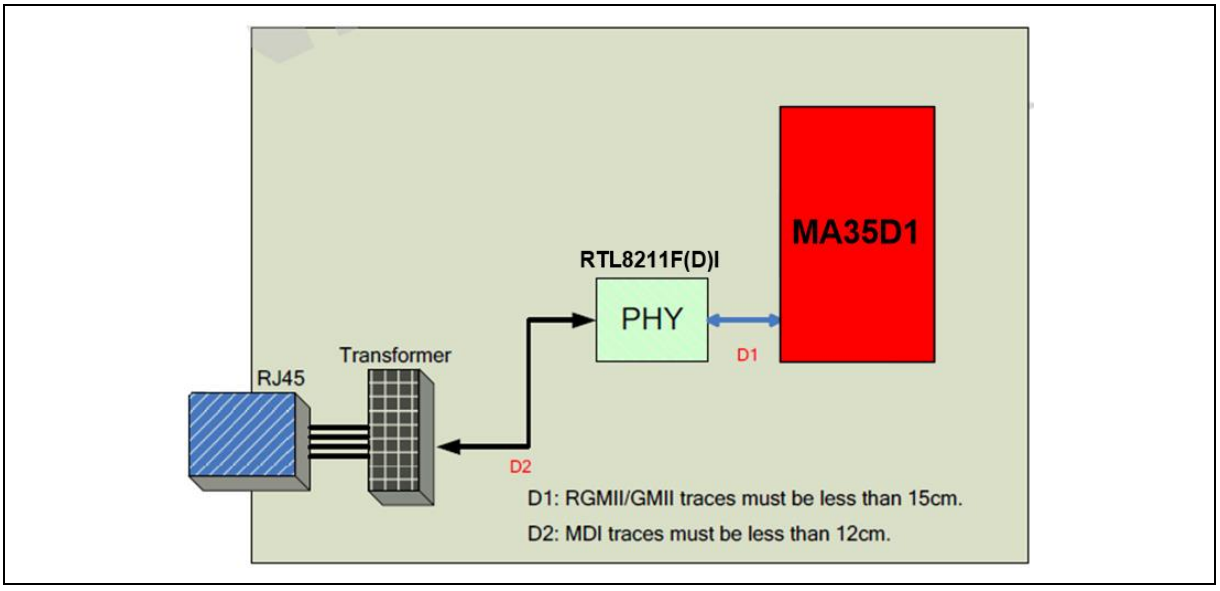


Figure 12-2 RGMII and MDI Placement

- The Crystal should be placed at least three times its own width from I/O ports, important or high frequency signal traces (Tx, Rx, and power), and magnetics.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.
- Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0 Ω resistors. Decoupling capacitors must be placed close to the power pins, such that the distance from the chip power pin to the capacitor is less than 200 mils.

12.1.2 Signal and Trace Routing

- RXC/TXC clock signal traces should be kept as short and wide as possible.
- Route the receive reference clock traces adjacent to an unbroken ground or power plane Minimize via and layer changes.
- Ninety-degree trace turns must be avoided. It is suggested that the traces turn at 45° angles. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

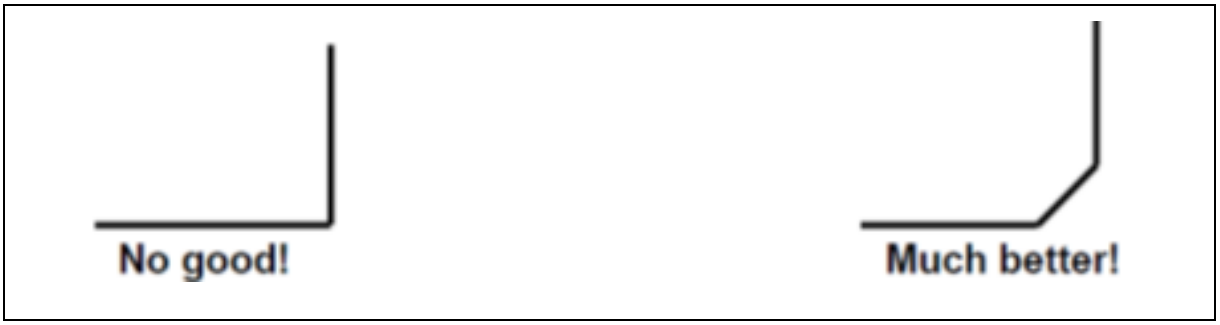


Figure 12-3 PCB Layout Trace Signal Trace Angles

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high-speed signal traces must be as short as possible (less than 15 cm). It is better to have a ground plane under these traces. Using a GND plane to surround them is necessary.
- RXC and TXC are high-speed (125 MHz) signals, keep a 20 mils space between clock and data signals.
- Match each RGMII Tx (TXCLK/TXCTL/TXD) and Rx (RXCLK/RXCTL/RXD) group trace length to within 100 mils.
- Route the RGMII traces at 50 Ω impedance, and route through an inner layer to reduce radiation.
- Keep all RGMII trace as short as possible (less than 15 cm).
- All RGMII traces must be referenced to an unbroken ground plane.
- Route the RGMII trace away from I/O traces to avoid crosstalk (>20 mils).

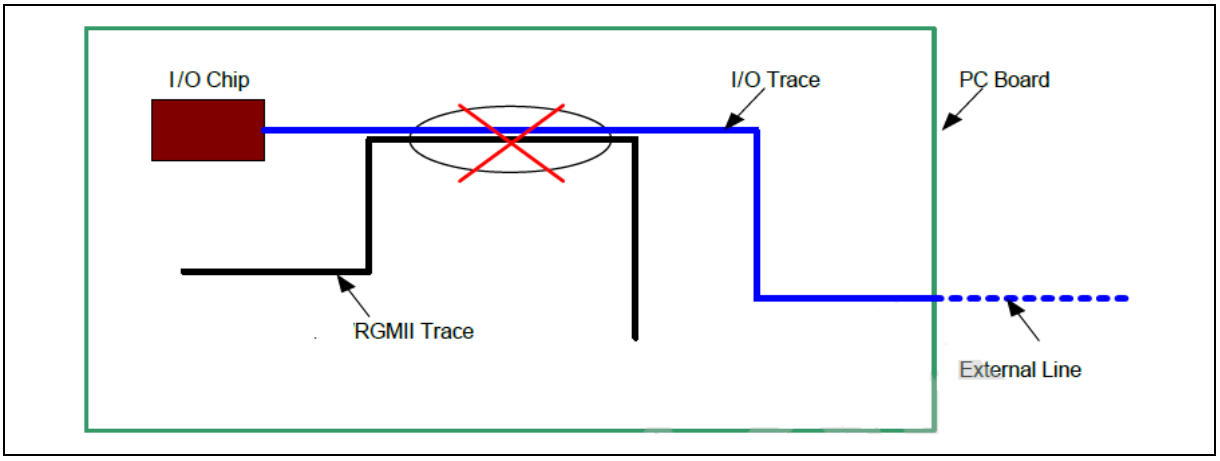


Figure 12-4 RGMII Trace and I/O Trace

- Traces routed from PHY to 10/100/1000M magnetics, and to the RJ-45 connector, should be as short as possible. The 12 cm maximum length between the PHY and magnetics is achievable only when there is no interference.

It is also very important to keep all four differential pair signal traces (MDIP0/MDIN0, MDIP1/MDIN1, etc.) at matching lengths (within 800 mil). MDI impedance is 100 Ω in differential mode.

The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is 8mil, then D1 can be 8 mil wide.

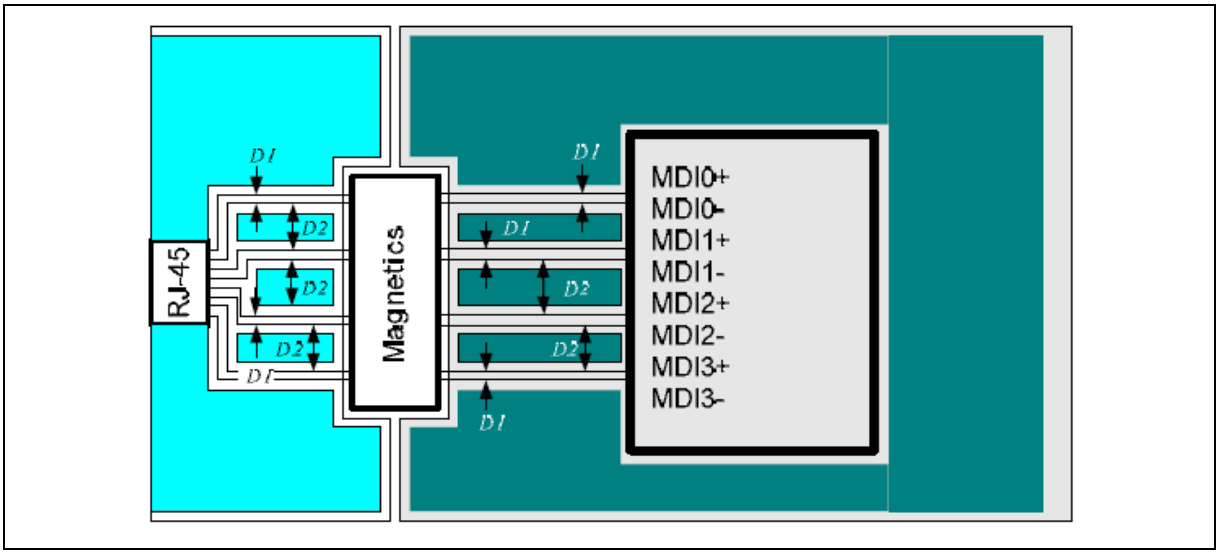


Figure 12-5 MDI Signals

- It is suggested that there should be more than 30 mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2). In addition, Ground Plane shielding can be used to separate all four signal pairs.
- A good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, it is suggested that not using via on the four differential pairs.
- Signal crossing a plane split may cause unpredictable return path currents and would likely result in signal quality failure, as well as induce EMI problems.

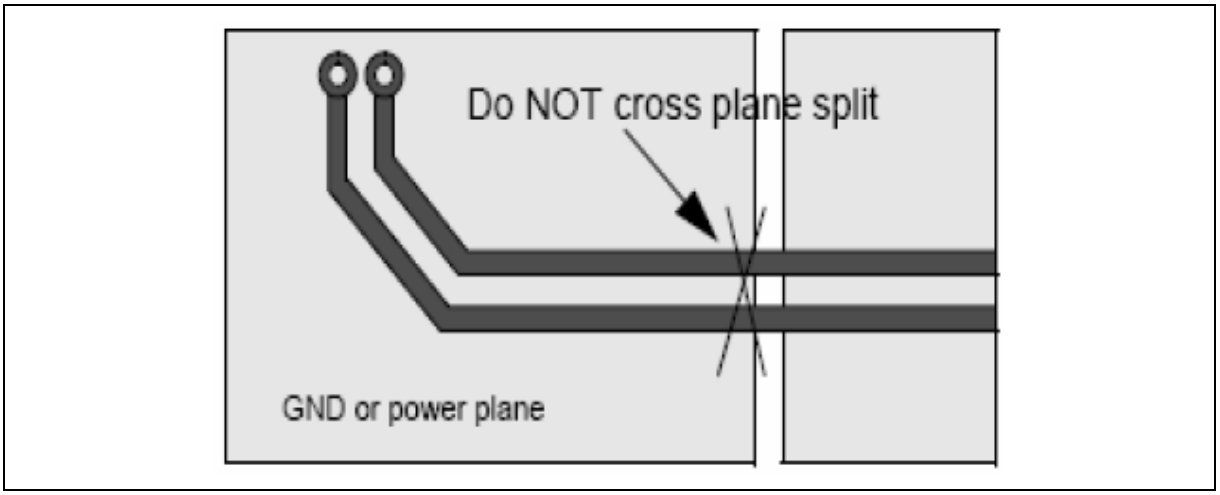


Figure 12-6 Signal Trace

- The power supply into the PHY digital power pins can be improved with de-coupling capacitors. The power signal traces should be as short and wide as possible. The vias of the de-coupling capacitor should be large enough in diameter. All analog power pins on the PHY need to be de-coupled with a capacitor. The de-coupling capacitors must be placed close to the PHY (<200 mils), and the traces should be kept short.
- Place R1/C1 close to the PHY (must be less than 500 mils)

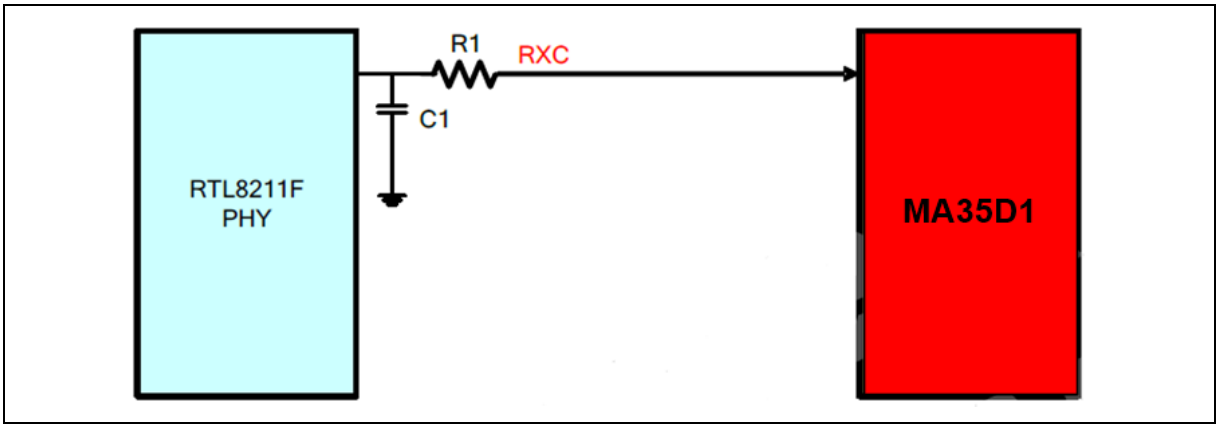


Figure 12-7 R1/C1 Placement

12.1.3 PCB Stack-up

- PCB stack-up is a major factor affecting the EMC performance of a product. A good stack-up effectively reduces radiation from the loops on the PCB, as well as from the cables connected to the board. Conversely, a poor stack-up may increase the radiation from both of these items considerably.
- RGMII signals are routed on layer 4 and reference layer 3 (GND plane).

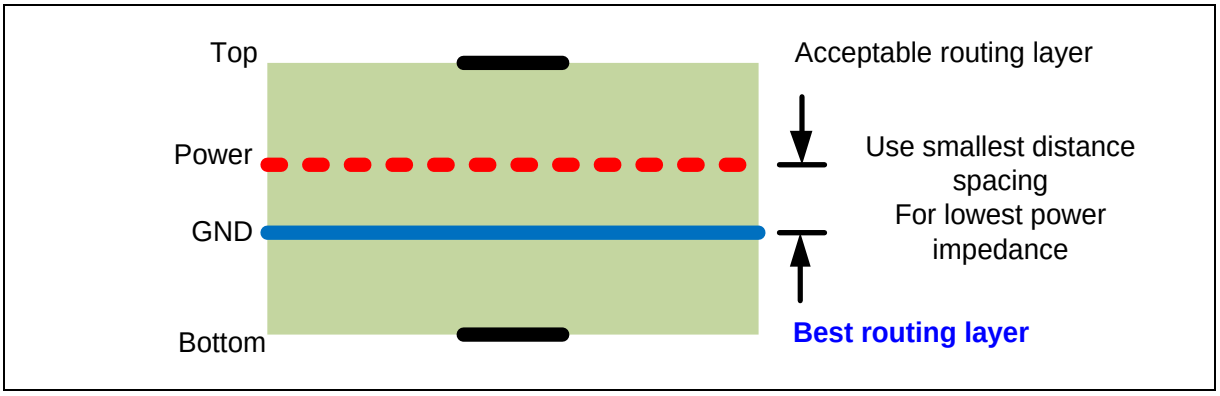


Figure 12-8 Four-layer Stack-up

- RGMII signals are routed on layer 4 (IN2) and reference layer 5 (GND plane).

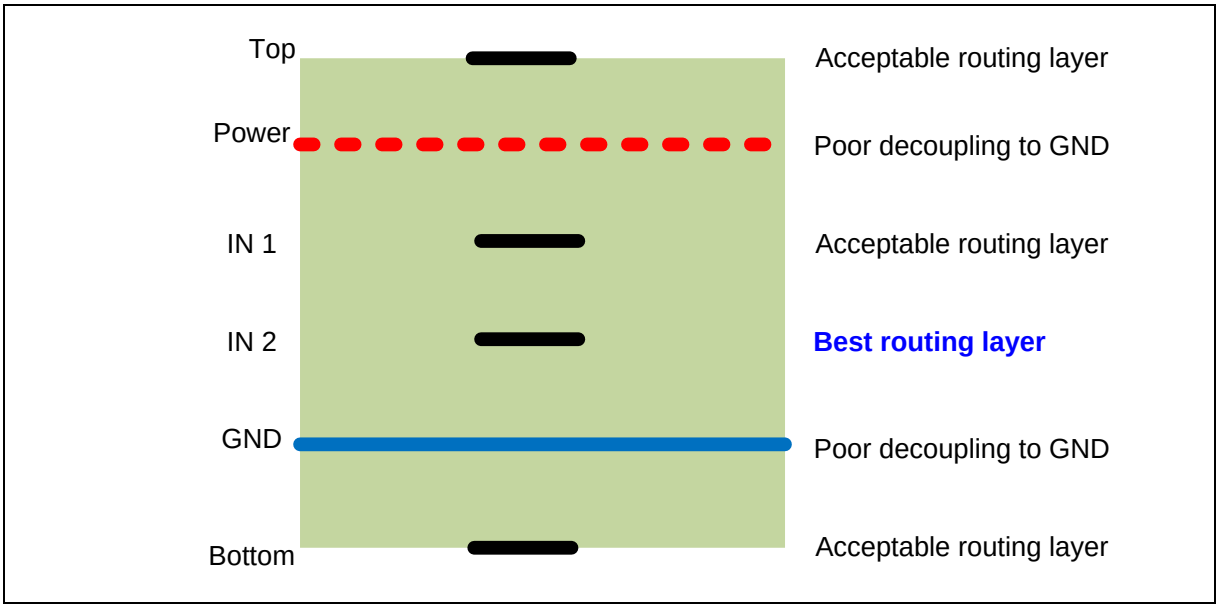


Figure 12-9 Six-layer Stack-up (A)

- RGMII signals are routed on layer 3 (IN1) and reference layer 2 (GND plane).

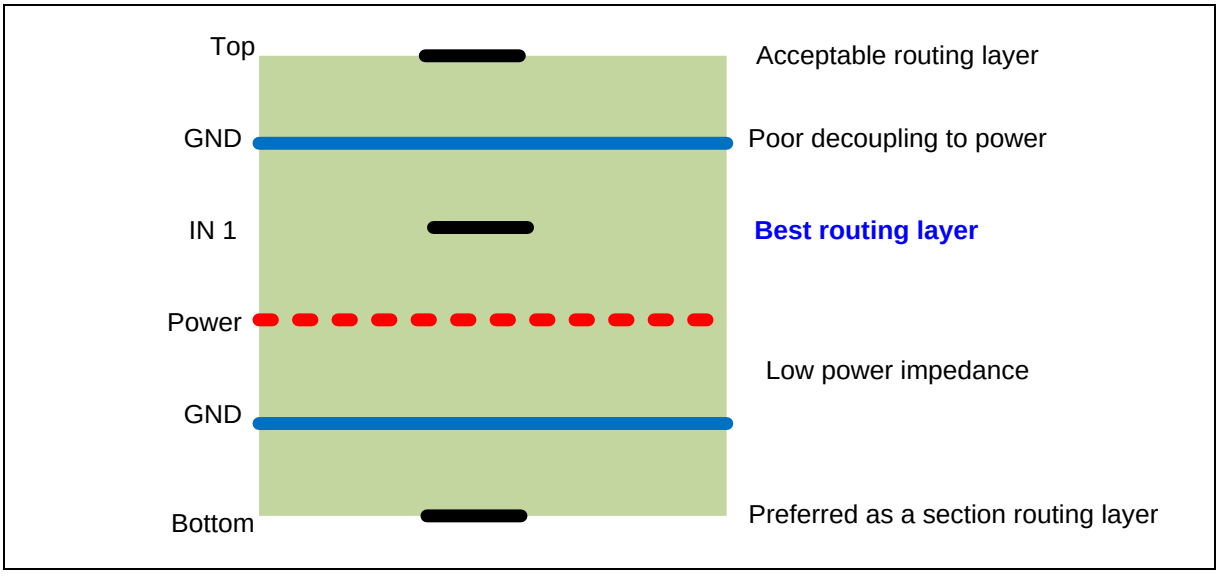


Figure 12-10 Six-layer Stack-up (B)

12.1.4 Ground Plane Layout

- The void area is to keep transformer-induced noise away from the power and system ground planes.

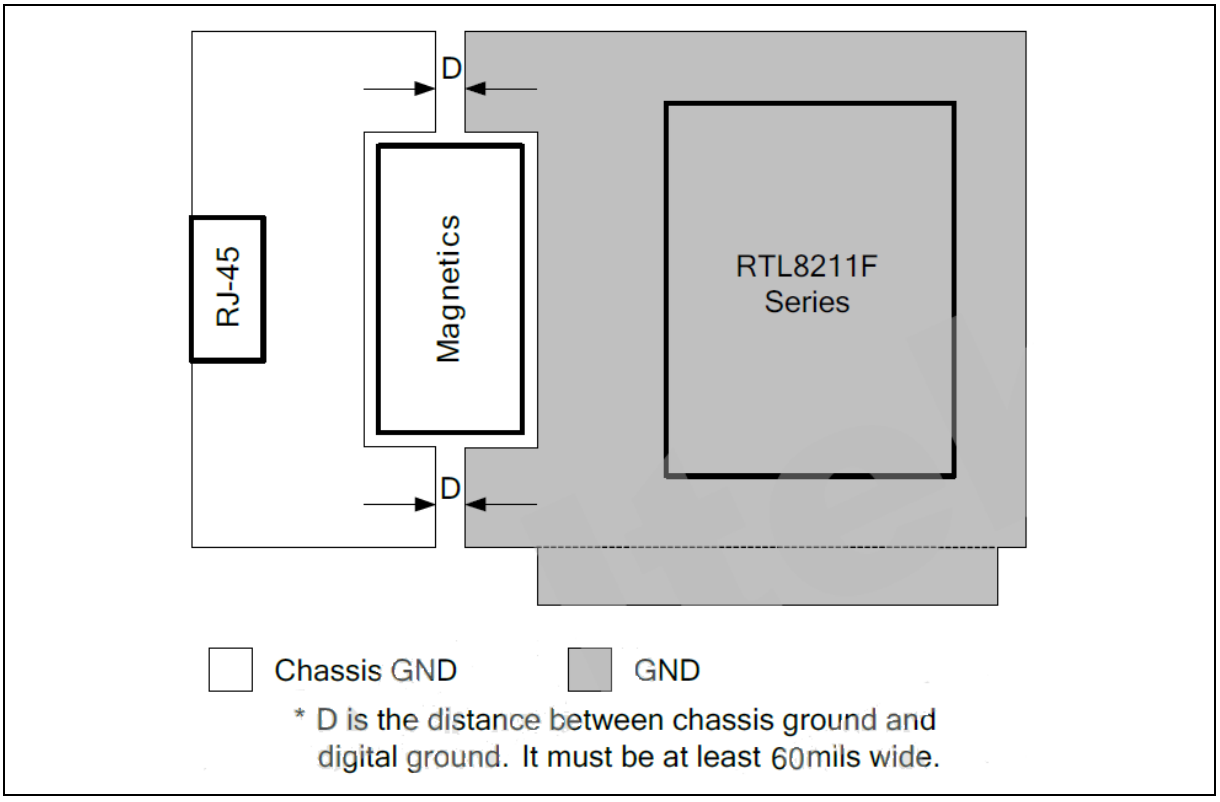


Figure 12-11 Ground Plane Separation

- The Chassis Ground as Figure 12-11 is known as an ‘Isolated Ground’. It connects

directly to the RJ-45 connector. In addition, a 2 kV high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

- It is important to keep the gap between Chassis GND and System GND wider than 60 mils for better isolation.
- Keep all RGMII trace as short as possible (less than 15 cm).
- All RGMII traces must be referenced to an unbroken ground plane.

12.2 RMII PHY Layout Guideline (Refer to Realtek RTL8201FI Design Guide)

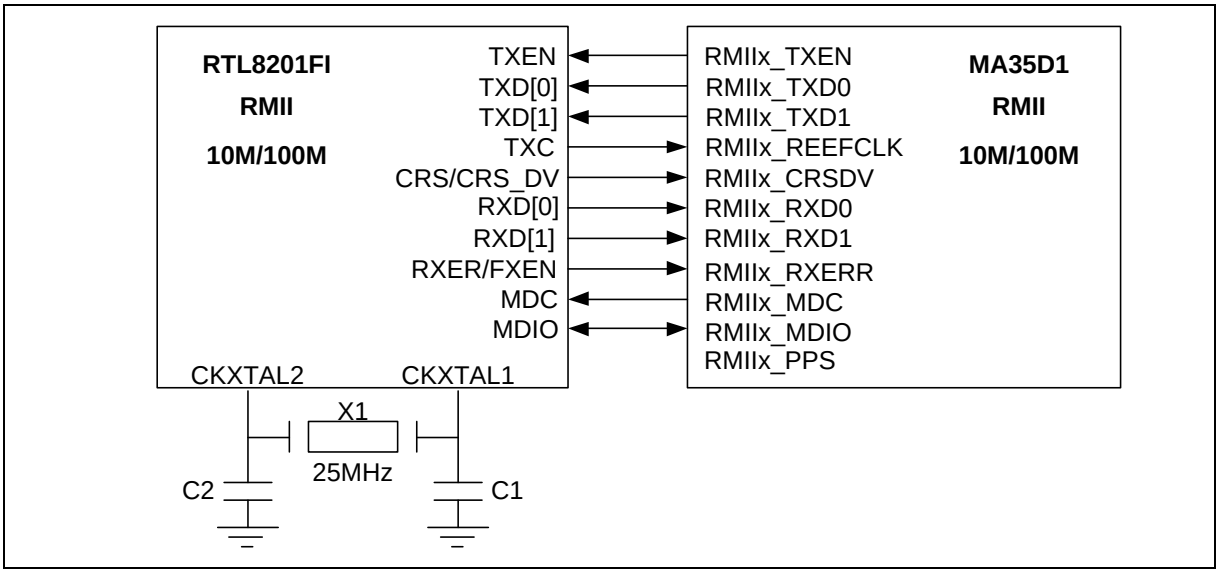


Figure 12-12 RMII Interface Connection

12.2.1 Placement

- For The PHY must be placed as close as possible to the MA35D1 (less than 8 inches).
- The 10/100 magnetics shout be placed as close as possible to the RJ-45 connector. The MDI traces must be less than 12 cm.
- The distance between the RJ-45 and magnetics (L3) should be as short as possible.

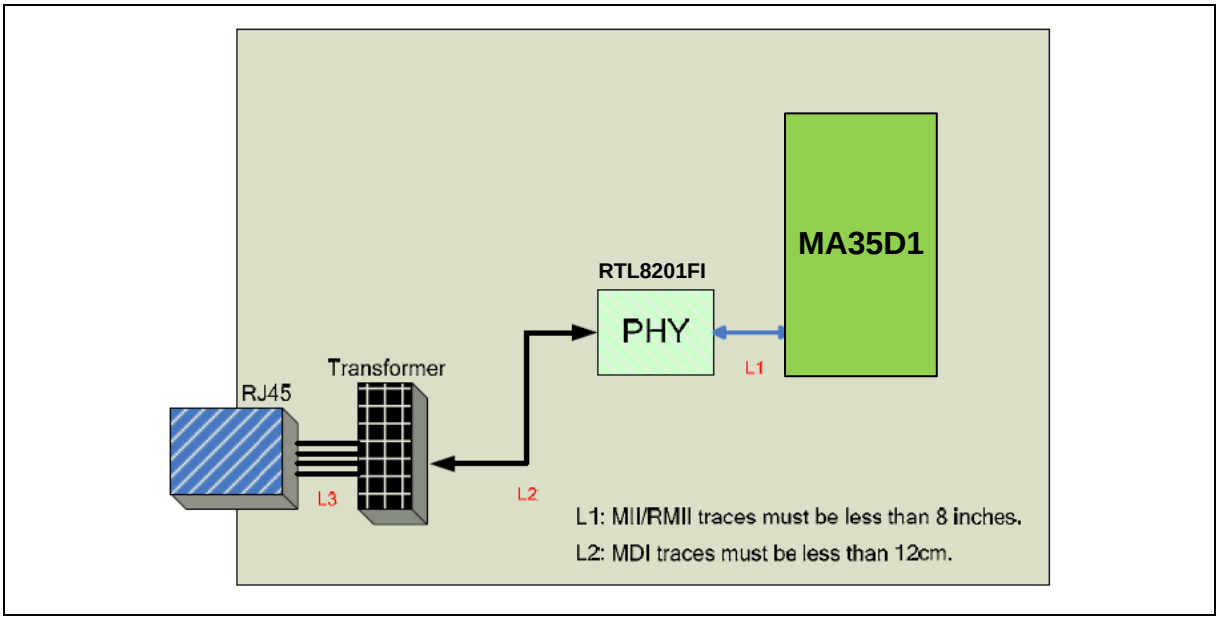


Figure 12-13 RMII and MDI Placement

- The Crystal should be placed far away from I/O ports, important or high frequency signal traces (Tx, Rx, and power), magnetics or board edges.
- The outer shield of the Crystal requires good grounding to avoid induction of EMC/EMI. The retaining straps of the OSC, if any, need good grounding as well.
- Every PCB design has its unique noise coupling behavior. Ferrite beads are used to suppress power noise. System designers are suggested to provide the option to replace the ferrite beads with 0 Ω resistors. Decoupling capacitors must be placed close to the power pins, such that the distance from the chip power pin to the capacitor is less than 200 mils.

12.2.2 Signal and Trace Routing

- The signal trace length difference between TX+ and TX- (RX+ and RX-) should be kept within 2 cm.
- Avoid digital signal (such as RMII or Clock signals) interference with analog signals (TX±, RX±, Rset trace) and Power trace. If it is necessary to cross digital signals with Analog/Power, the cross should be made at a 90° angle.

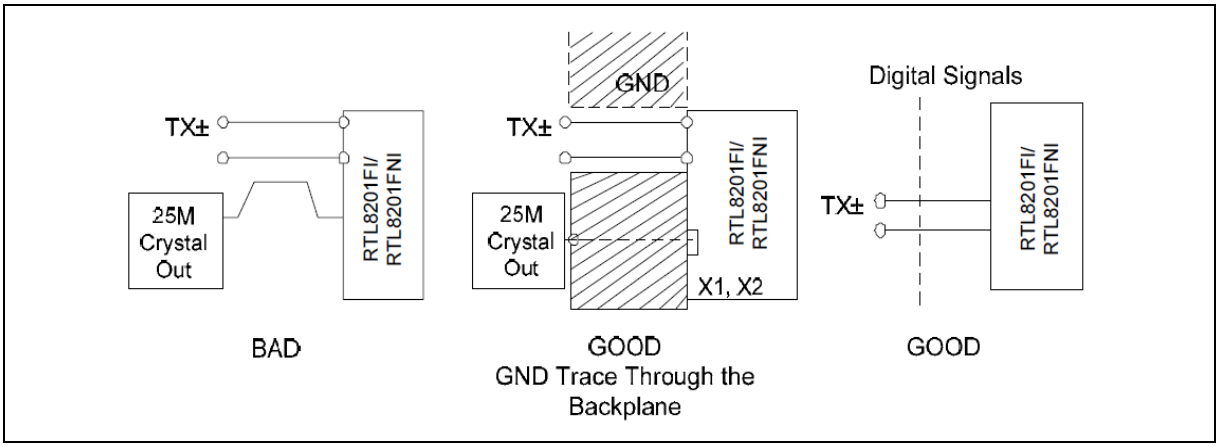


Figure 12-14 Digital Signals Avoidance and Crossing

- TXC are high-speed (50 MHz) signals; keep a 20 mils spacing between clock and data signal.
- Ninety-degree trace turns must be avoided. It is suggested that the traces turn at 45° angles. Sharp edges may add unexpected parasitic effects into the circuitry. Reducing the trace length will reduce trace inductance during quick energy bursts.

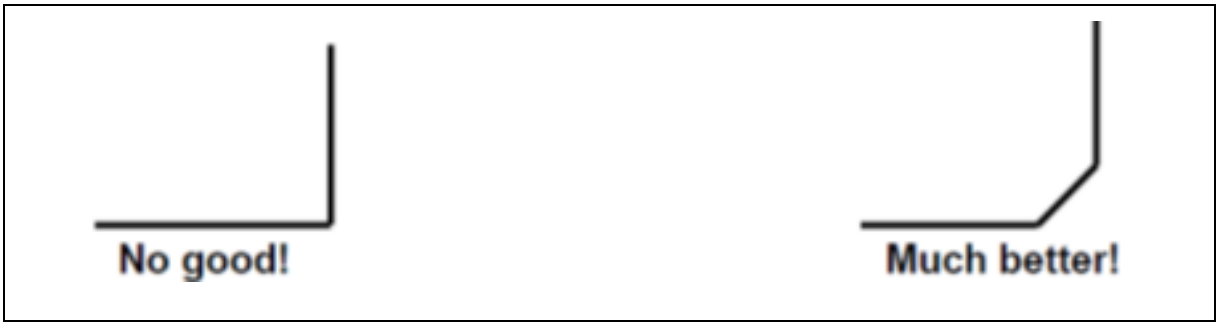


Figure 12-15 PCB Layout Trace Signal Trace Angles

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces. If possible, use a GND plane to surround them.
- Traces routed from PHY to 10/100M magnetics, and to the RJ-45 connector, should be as short as possible. The 12 cm maximum length between the PHY and magnetics is achievable only when there is no interference.

It is also very important to keep all four differential pair signal traces (MDI0±, MDI1±, etc.) at matching lengths (within 25 mil). MDI impedance is 50 Ω common mode, 100 Ω differential mode.

The two traces of each pair should be placed close to each other (D1) since they are differential pair signals to each other and provide a strong cancelling effect on noise. D1 can be the width of each of the two differential traces. E.g., if the width of the trace is 8 mil, then D1 can be 8 mil wide.

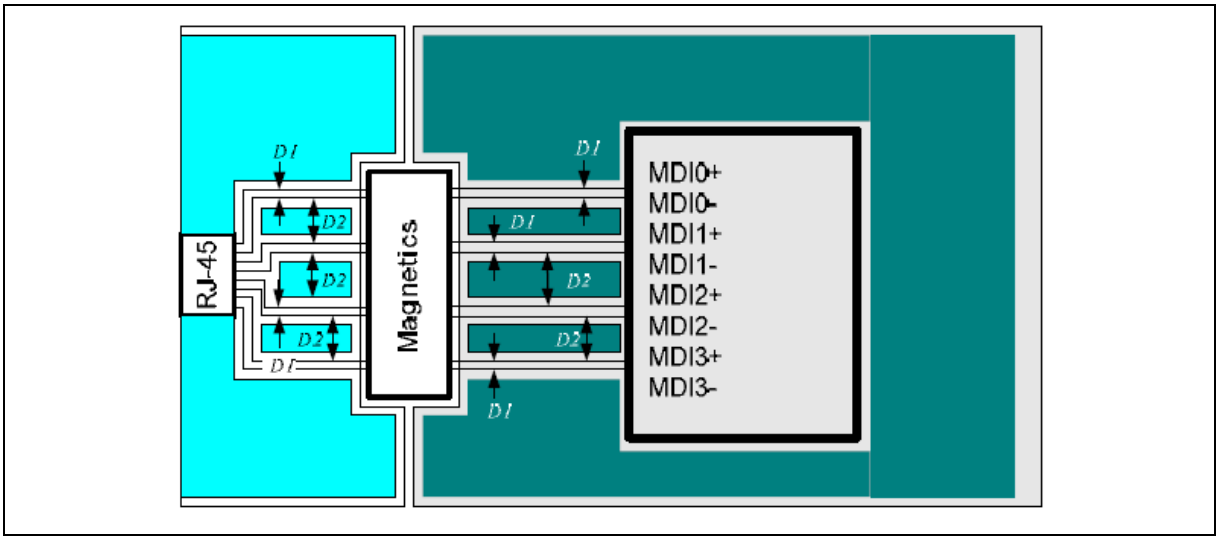


Figure 12-16 MDI Signals

- It is suggested that there should be more than 50 mil spacing between different differential pairs to minimize crosstalk coupled from other pairs (D2). In addition, Ground Plane shielding can be used to separate all four signal pairs.
- A good layout should avoid the following situations:
  - Intersection of any two pairs of signal traces
  - Intersection of the two signal traces of the same differential pair
- To minimize impedance mismatch, it is suggested that not using via on the differential pairs.
- Signal crossing a plane split may cause unpredictable return path currents and would likely result in signal quality failure, as well as induce EMI problems.

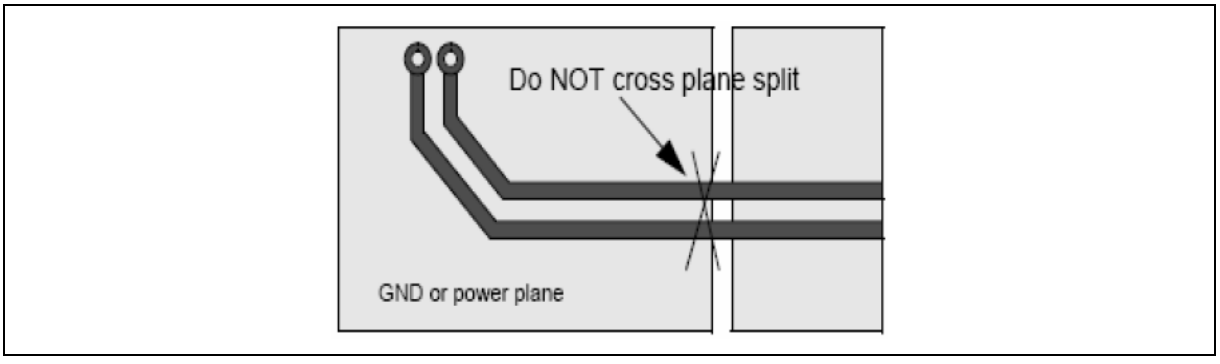


Figure 12-17 Signal Trace

- RMII traces (REF_CLK) between the PHY and the MA35D1 should be surrounded by GND trace.

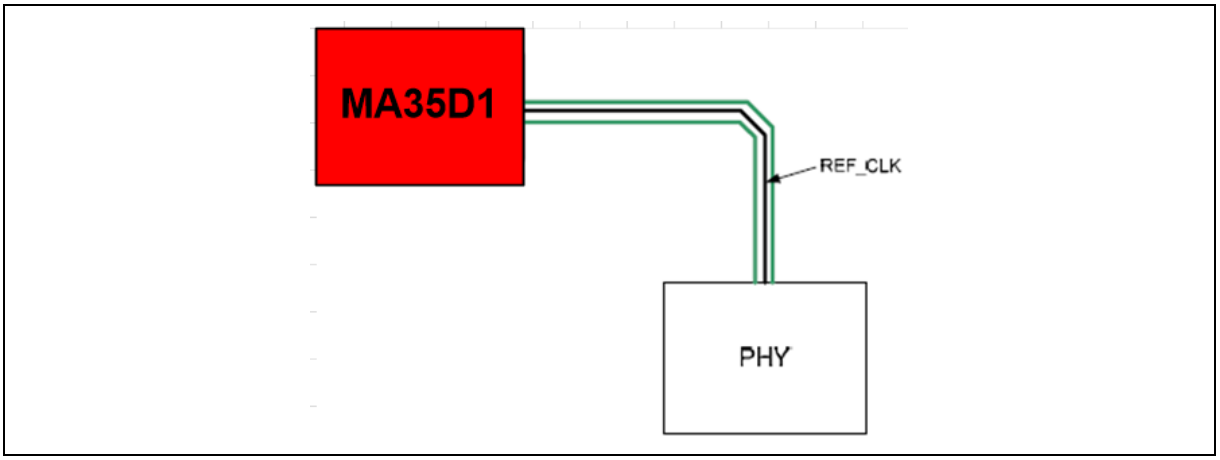


Figure 12-18 RMII Mode Clock (REF_CLK)

- Place the RC filter component close to the source of the reference clock in RMII mode. When the reference clock is output, i.e., from PHY to MA35D1 (MAC).

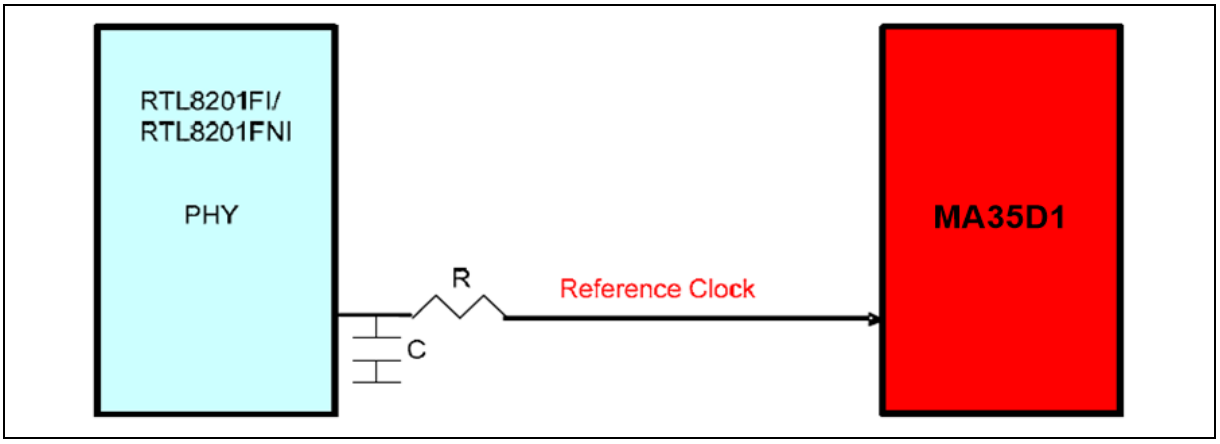


Figure 12-19 R/C Placement

12.2.3 PCB Stack-up

- It is suggested that using at least a 4-layer PCB. The digital power plane should be separate from analog areas, which are extremely sensitive to noise.
- RGMII signals are routed on layer 4 and reference layer 3 (GND plane).

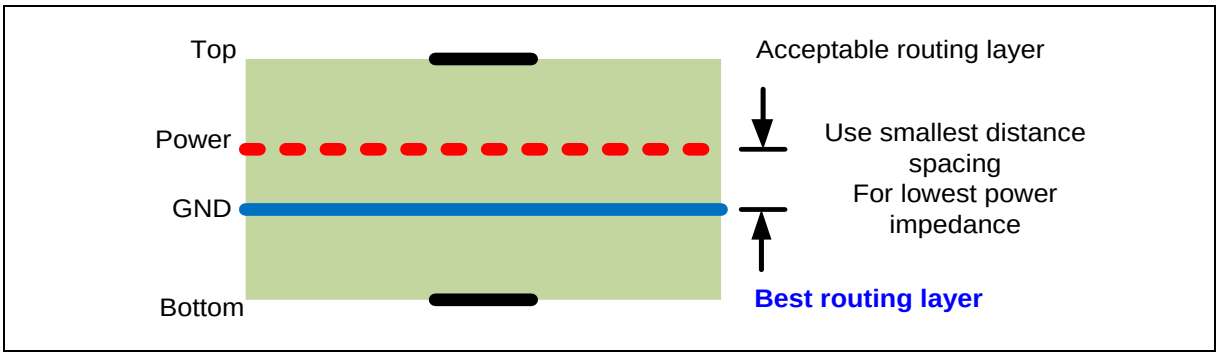


Figure 12-20 Four-layer Stack-up

- Any analog circuit on the same plane as the digital power will experience an energy fluctuation due to the fast switching time if digital components. This could improperly bias transistors, and cause the circuits to malfunction. A low-pass filter combination of a ferrite bead and capacitors should be used to provide a clean, filtered power plane for analog consideration. Keep power traces to the PHY as short and wide as possible and make good use of via. Keep the digital power plane as a whole, and leave some space for the analog power plane.

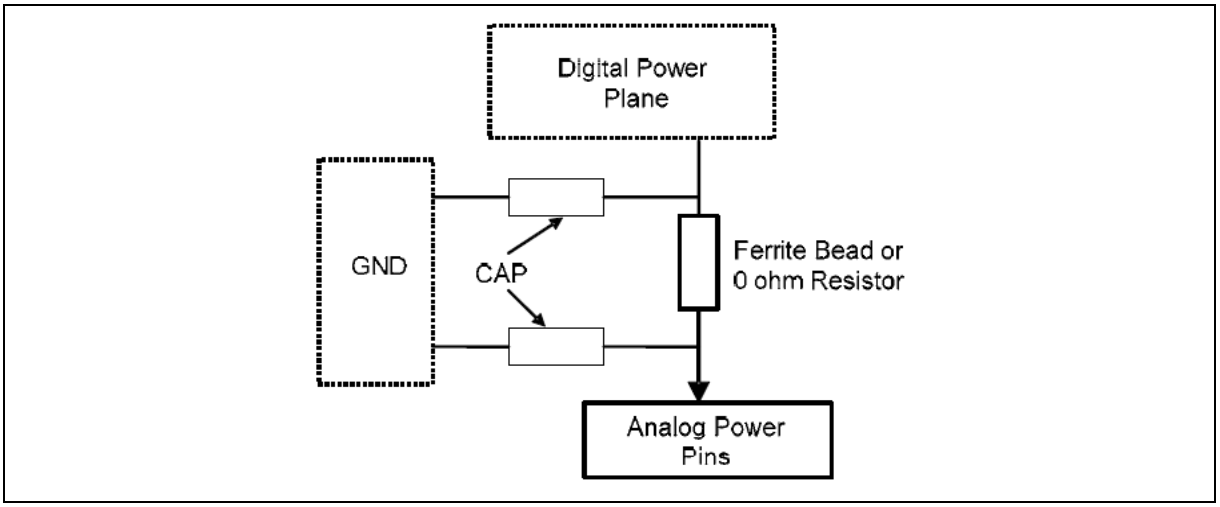


Figure 12-21 Power Plane

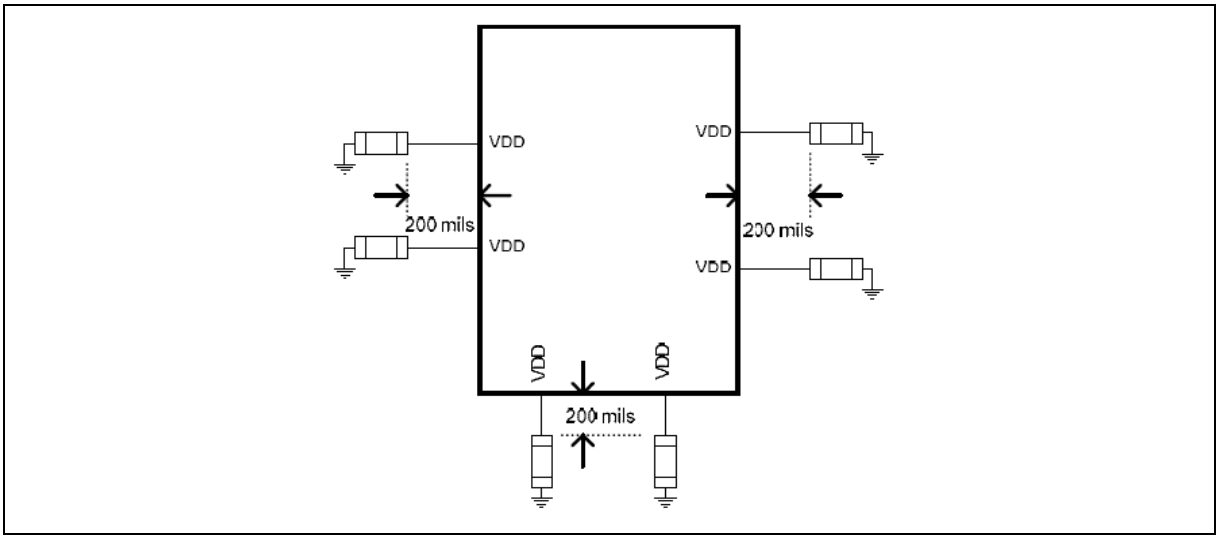


Figure 12-22 Decoupled Capacitor Example

12.2.4 Ground Plane Layout

- Isolated separation between Analog and Digital Ground domains is not recommended, as bad ground plane partitioning could cause serious EMI emissions and degrade analog performance due to bouncing noise.

- The trace length and the ratio of trace width to trace height above the ground planes should be carefully considered. Clock and other high-speed signal traces should be as short and wide as possible (compared to normal digital traces). It is better to have a ground plane under these traces.

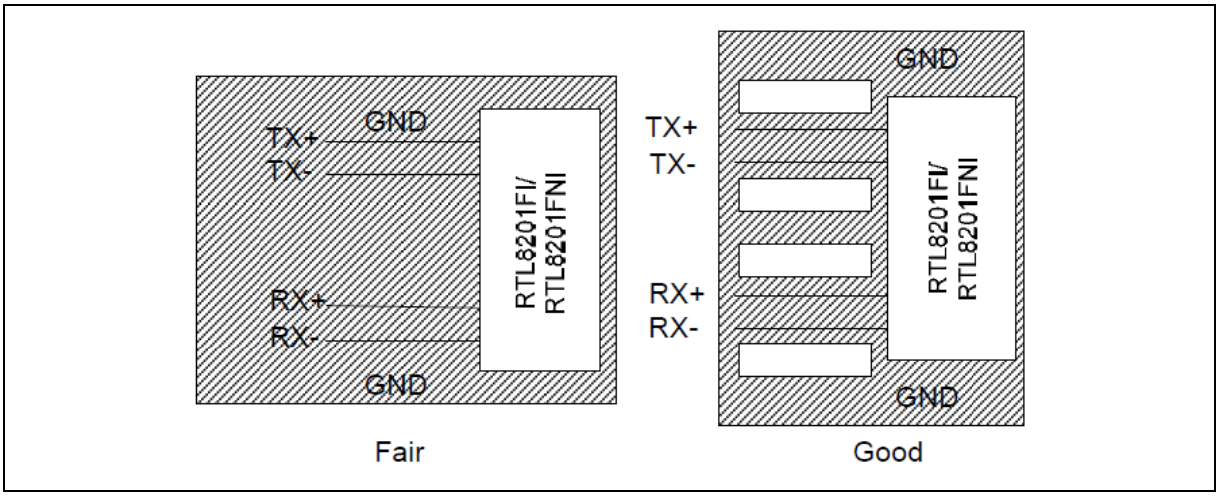


Figure 12-23 Ground Plane Under Traces

- The void area is to keep transformer-induced noise away from the power and system ground planes.

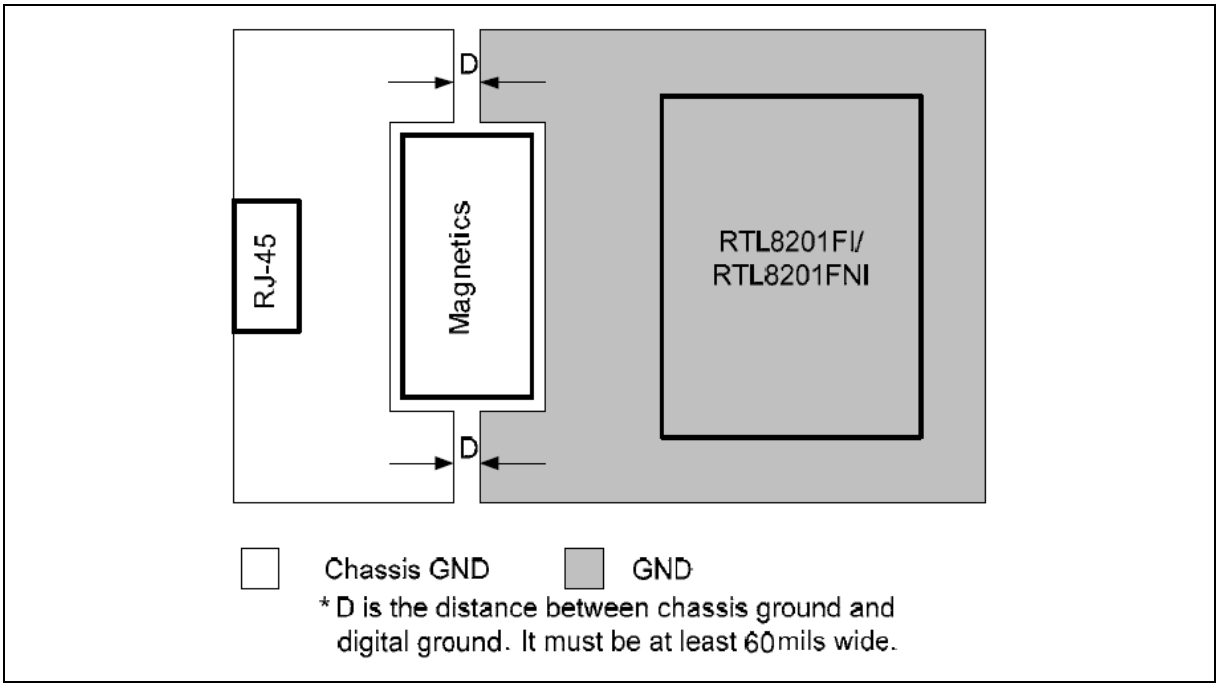


Figure 12-24 Ground Plane Separation

- The Chassis Ground as Figure 12-24 is known as an ‘Isolated Ground’. It connects directly to the RJ-45 connector. In addition, a 2 kV high voltage capability capacitor is needed to connect to this chassis ground for ESD protection.

- It is important to keep the gap between Chassis GND and System GND wider than 60 mils for better isolation.

13 Capture Sensor Interface

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO output them into frame buffer.

The MA35D1 series has two sets of CMOS capture sensor interfaces supporting CCIR601 and CCIR656 type sensor and resolution up to 3M pixels. It can support YUV422 and RGB565 color format for data output by CMOS image sensor.

13.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
VCAP0	VCAP0_DATA0	PM.2	MFP6	I	Video Image/Camera capture 0 data input bus bit 0
	VCAP0_DATA1	PM.3	MFP6	I	Video Image/Camera capture 0 data input bus bit 1
	VCAP0_DATA2	PM.4	MFP6	I	Video Image/Camera capture 0 data input bus bit 2
	VCAP0_DATA3	PM.5	MFP6	I	Video Image/Camera capture 0 data input bus bit 3
	VCAP0_DATA4	PM.6	MFP6	I	Video Image/Camera capture 0 data input bus bit 4
	VCAP0_DATA5	PM.7	MFP6	I	Video Image/Camera capture 0 data input bus bit 5
	VCAP0_DATA6	PM.8	MFP6	I	Video Image/Camera capture 0 data input bus bit 6
	VCAP0_DATA7	PM.9	MFP6	I	Video Image/Camera capture 0 data input bus bit 7
	VCAP0_DATA8	PM.10	MFP6	I	Video Image/Camera capture 0 data input bus bit 8
	VCAP0_DATA9	PM.11	MFP6	I	Video Image/Camera capture 0 data input bus bit 9
	VCAP0_HSYNC	PK.11	MFP6	I	Video Image/Camera capture 0 interface HSYNC input pin
	VCAP0_PIXCLK	PK.10	MFP6	I	Video Image/Camera capture 0 interface pixel clock input pin
	VCAP0_SCLK	PK.9	MFP6	O	Video Image/Camera capture 0 interface sensor clock output pin
	VCAP0_SFIELD	PM.1	MFP6	I	Video Image/Camera capture 0 interface SFIELD input pin

	VCAP0_VSYNC	PM.0	MFP6	I	Video Image/Camera capture 0 interface VSYNC input pin
VCAP1	VCAP1_DATA0	PN.0	MFP6	I	Video Image/Camera capture 1 data input bus bit 0
		PE.0	MFP7	I	
	VCAP1_DATA1	PN.1	MFP6	I	Video Image/Camera capture 1 data input bus bit 1
		PE.1	MFP7	I	
	VCAP1_DATA2	PN.2	MFP6	I	Video Image/Camera capture 1 data input bus bit 2
		PE.2	MFP7	I	
	VCAP1_DATA3	PN.3	MFP6	I	Video Image/Camera capture 1 data input bus bit 3
		PE.3	MFP7	I	
	VCAP1_DATA4	PN.4	MFP6	I	Video Image/Camera capture 1 data input bus bit 4
		PE.4	MFP7	I	
	VCAP1_DATA5	PN.5	MFP6	I	Video Image/Camera capture 1 data input bus bit 5
		PE.5	MFP7	I	
	VCAP1_DATA6	PN.6	MFP6	I	Video Image/Camera capture 1 data input bus bit 6
		PE.6	MFP7	I	
	VCAP1_DATA7	PN.7	MFP6	I	Video Image/Camera capture 1 data input bus bit 7
		PE.7	MFP7	I	
	VCAP1_DATA8	PN.8	MFP6	I	Video Image/Camera capture 1 data input bus bit 8
		PE.12	MFP7	I	
	VCAP1_DATA9	PN.9	MFP6	I	Video Image/Camera capture 1 data input bus bit 9
		PE.13	MFP7	I	
	VCAP1_HSYNC	PN.12	MFP6	I	Video Image/Camera capture 1 interface HSYNC input pin
		PE.10	MFP7	I	
		PB.9	MFP7	I	
	VCAP1_PIXCLK	PN.11	MFP6	I	Video Image/Camera capture 1 interface pixel clock input pin
		PE.9	MFP7	I	
	VCAP1_SCLK	PN.10	MFP6	O	Video Image/Camera capture 1 interface sensor clock output pin
		PE.8	MFP7	O	
	VCAP1_SFIELD	PN.14	MFP6	I	Video Image/Camera capture 1 interface SFIELD input pin
		PF.14	MFP7	I	
		PB.11	MFP7	I	
	VCAP1_VSYNC	PN.13	MFP6	I	

		PE.11	MFP7	I	Video Image/Camera capture 1 interface VSYNC input pin
		PB.10	MFP7	I	

Table 13-1 Video Capture0/1 Interface Pin List

13.2 Reference Connection

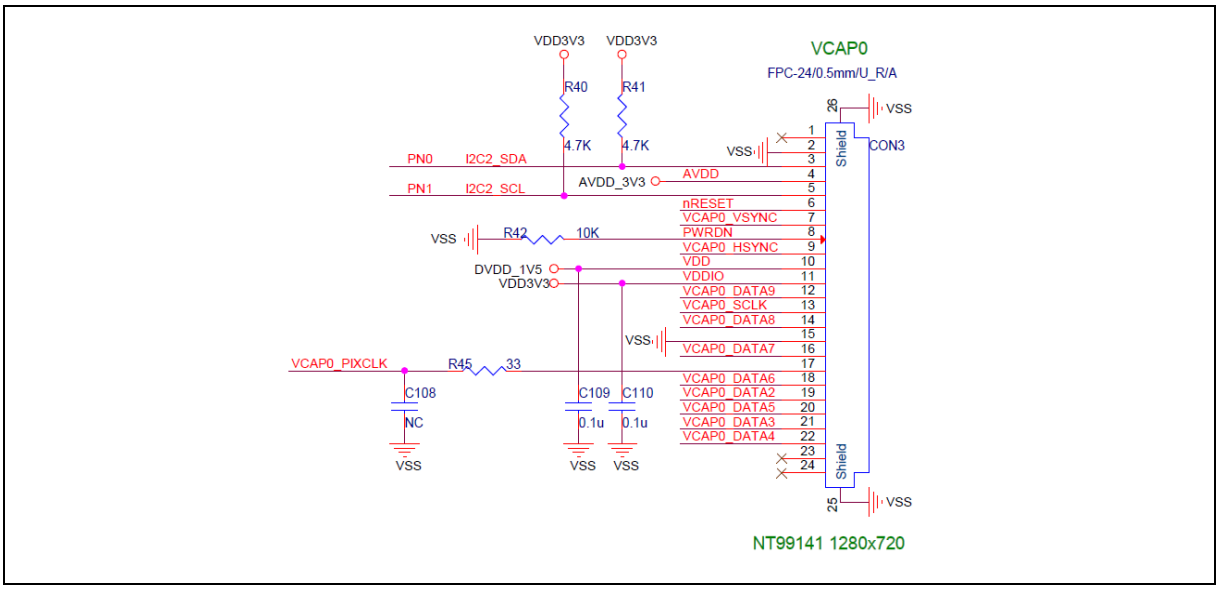


Figure 13-1 CMOS Sensor Interface Connection

13.3 PCB Design Considerations

- Routing sequences: PIXCLK ➔ SCLK ➔ Data ➔ HSYNC ➔ VSYNC ➔ Others
- Connect GND and route ground plane as large as possible.
- Minimum gap between PIXCLK and SCLK trace is double of trace width (W*2).

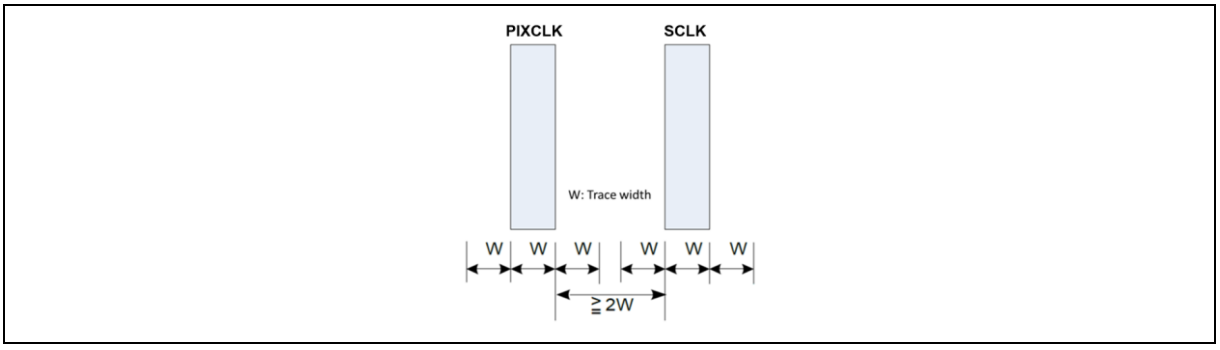


Figure 13-2 PIXCLK and SCK Trace

- Route ground trace adjacent to PIXCLK/SCLK traces to reduce crosstalk between other traces, or route power or low frequency signal adjacent to PIXCLK/SCLK traces.
- Priority: GND->Power->Low frequency signals

Note: low frequency signal: I^2C/ PWRDN/ nRESETN/ VS_{YNC} etc.

- Place Decoupling Caps as close to CMOS sensor power pins as possible, connect Cap first and then connect power pins, Decoupling Caps is recommending to get better image quality. In placement or routing issue, you may use less Cap by Cap sharing (with adjacent power pin), the Cap sharing need use larger Cap.
- When using external LDO V_{DD}, decoupling Cap for V_{DD} is required.
- Do not route PIXCLK and SCLK under Sensor, route trace outside Sensor is recommend.
- Do not route VS_{YNC}/HS_{YNC}/SCLK/PIXCLK traces adjacently, if possible, shield by GND trace would be better.
- In all signal trace, use Via less than three to get good signal quality.
- Route CMOS sensor AV_{DD} trace directly to AV_{DD} plane to get good image quality.

14 Quad Serial Peripheral Interface (QSPI)

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The MA35D1 series contains two sets QSPI (QSPI0/QSPI1) controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports Dual and Quad I/O Transfer mode and the controller supports PDMA function to access the data buffer.

QSPI0/QSPI1 can support SPI-NOR and SPI-NAND types Flash.

QSPI0 supports SPI Flash booting.

14.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
QSPI0	QSPI0_CLK	PD.1	MFP5	I/O	Quad SPI0 serial clock pin
	QSPI0_MISO0	PD.3	MFP5	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin
	QSPI0_MISO1	PD.5	MFP5	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin
	QSPI0_MOSI0	PD.2	MFP5	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin
	QSPI0_MOSI1	PD.4	MFP5	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin
	QSPI0_SS0	PD.0	MFP5	I/O	Quad SPI0 slave select 0 pin
QSPI1	QSPI1_CLK	PD.9	MFP5	I/O	Quad SPI1 serial clock pin
		PL.3	MFP6	I/O	
	QSPI1_MISO0	PD.11	MFP5	I/O	Quad SPI1 MISO0 (Master In, Slave Out) pin
		PL.5	MFP6	I/O	
	QSPI1_MISO1	PL.7	MFP6	I/O	Quad SPI1 MISO1 (Master In, Slave Out) pin
		PD.7	MFP5	I/O	
		PL.1	MFP6	I/O	
	QSPI1_MOSI0	PD.10	MFP5	I/O	Quad SPI1 MOSI0 (Master Out, Slave In) pin
		PL.4	MFP6	I/O	
	QSPI1_MOSI1	PL.6	MFP6	I/O	Quad SPI1 MOSI1 (Master Out, Slave In) pin
		PD.6	MFP5	I/O	
		PL.0	MFP6	I/O	
	QSPI1_SS0	PD.8	MFP5	I/O	Quad SPI1 slave select 0 pin
	QSPI1_SS1	PL.2	MFP6	I/O	Quad SPI1 slave select 1 pin

Table 14-1 QSPI0/QSPI1 Interface Pin List

14.2 QSPI Reference Connection

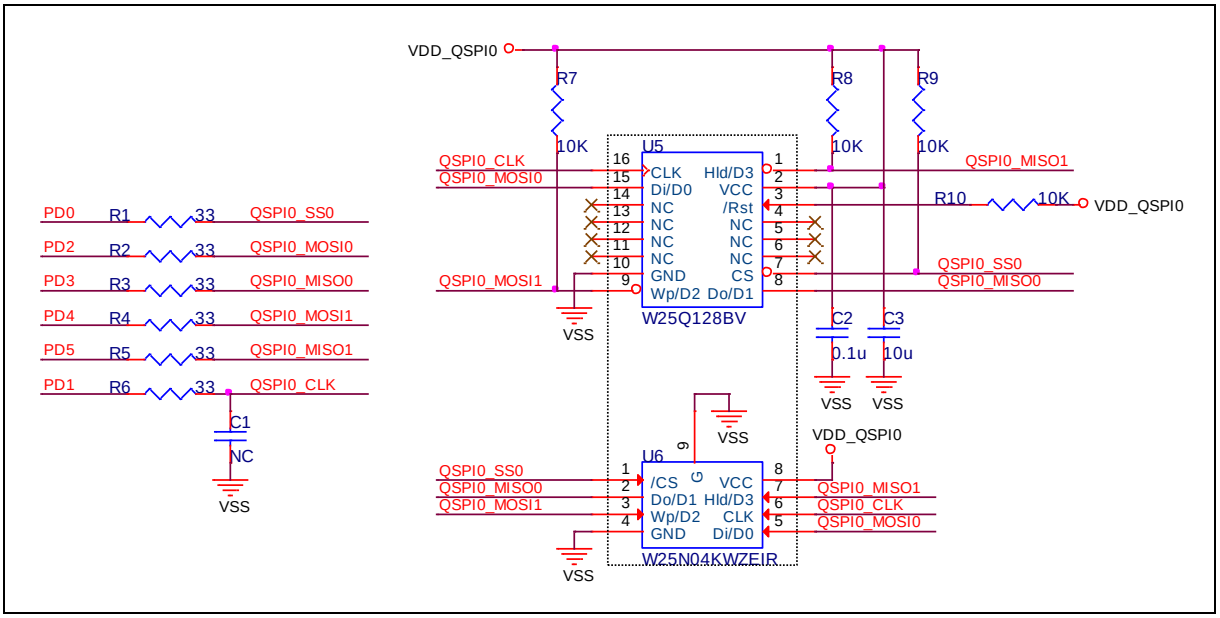


Figure 14-1 Reference Circuit for QSPI0 Booting with SPI Flash

14.3 PCB Layout Considerations for QSPI Flash

QSPI0 supports (up to 100 MHz) high speed SPI Flash memory device for booting.

This session provides the recommendations for PCB layout.

14.3.1 Power Supply Decoupling

The SPI Flash has one power supply pin (V_{CC}) and one ground pin (GND). One ceramic capacitor with 0.1μF at least is recommended for power supply decoupling. This capacitor should be placed as close as possible to the power supply pin of the package.

14.3.2 Clock Signal Routing

In high speed synchronous data transfer, good signal integrity in a PCB design is of importance, especially for the clock signal. When routing the clock signal, special cares should be taken. The following practices are recommended.

- Run the clock signal at least 3x of the trace width away from all other signal traces. This helps to keep clock signal clean from noise. See Figure 14-2.
- Use as less via(s) as possible for the whole path of clock signal. Via will cause impedance change and signal reflection.
- Run the clock trace as straight as possible and avoid using serpentine routing. See Figure 14-3.
- Keep a continuous ground in the next layer as reference plane.
- Route the clock trace with controlled impedance.

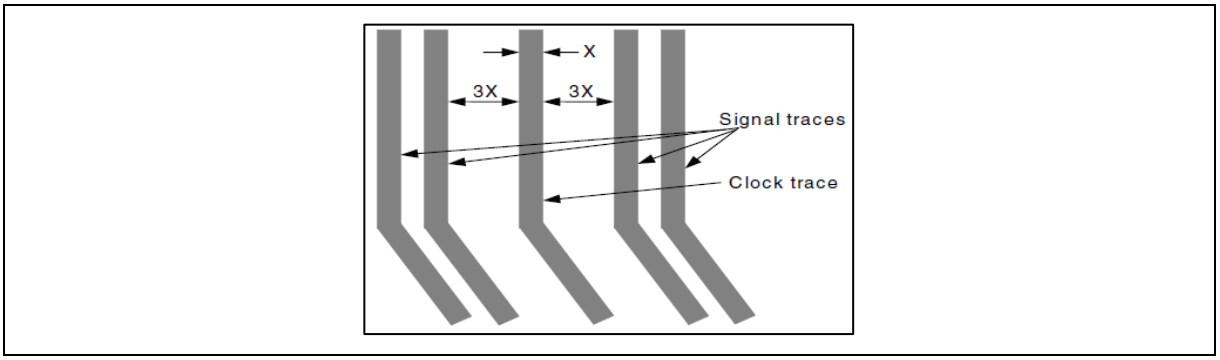


Figure 14-2 Separate SPI Clock from Other Signals

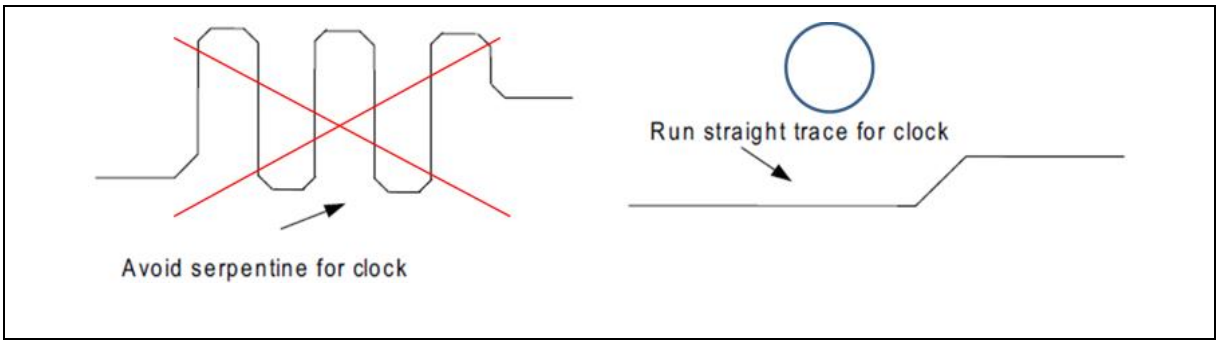


Figure 14-3 Run Straight Trace for Clock

14.3.3 Data Signal Routing

QSPI Flash has a 4-bit data bus, IO0-IO3. In order to keep the correct timing for the data transfer, in the PCB routing, the data traces should match the time delay with the clock trace from the host controller to the Flash. The data signals should be routed with the traces of controlled impedance to reduce the signal reflection. It should be avoided to route the traces with 90 angle corner. The recommendation is to cut the corner and smooth the trace when trace route needs to change direction.

Figure 14-4 shows the example of trace routing at the corner. To further improve the signal integrity, it should be considered to avoid using multiple signal layers for data signal routing. All signal traces should have a continuous reference plane.

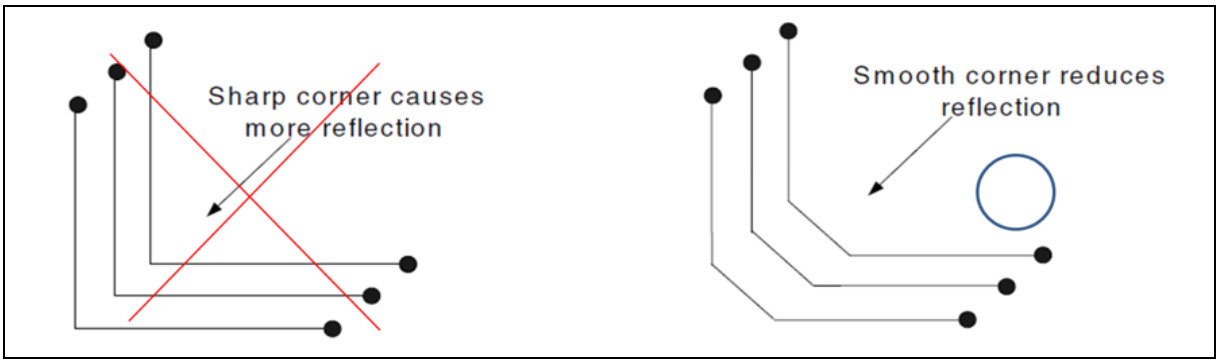


Figure 14-4 Signal Routing at the Corner

14.3.4 Recommendations

Checklist for PCB design recommendations:

- Put the decoupling capacitor as close as possible to the power pin. A value of around 0.1μF ceramic capacitor with 0603/0402 package is a good choice.
- Clock should be routed straight and with less via if possible. Separation of clock and other signals is important to make the clock clean.
- All signal traces should go with a solid reference plane (either GND or V_{CC}).
- All signals should be routed with controlled impedance. Typically, the PCB is recommended to be built using 50-75 Ω trace impedance with ±5% tolerance.
- Data bus should be routed with matching length to the reference of the clock. The matching length, typically, is recommended within ±150 mils.
- The QSPI must be placed as close as possible to the MA35D1 (less than 10 cm)

15 Controller Area Network Flexible Data-Rate (CAN FD)

The Controller Area Network Flexible Data-rate (CAN FD) is a serial communications protocol that efficiently supports distributed real-time control with a very high level of security. Its domain of application ranges from high speed networks to low cost multiple wiring.

The MA35D1 series has four sets of CAN FD controllers. Each supports 32 Message Objects; each Message Object has its own identifier mask.

The CAN FD controller performs communication according to the ISO 11898-1:2015 and needs to be connected to additional transceiver hardware for the CAN bus physical layer.

15.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
CAN FD0	CAN0_RXD	PG.2	MFP3	I	CAN FD0 bus receiver input
		PI.2	MFP3	I	
		PL.6	MFP3	I	
		PM.6	MFP3	I	
		PJ.10	MFP3	I	
		PK.6	MFP3	I	
		PC.2	MFP3	I	
		PN.2	MFP3	I	
		PB.10	MFP3	I	
	CAN0_TXD	PG.3	MFP3	O	CAN FD0 bus transmitter output
		PI.3	MFP3	O	
		PL.7	MFP3	O	
		PM.7	MFP3	O	
		PJ.11	MFP3	O	
		PK.7	MFP3	O	
		PC.3	MFP3	O	
		PN.3	MFP3	O	
		PB.11	MFP3	O	

CAN FD1	CAN1_RXD	PB.14	MFP3	I	CAN FD1 bus receiver input
		PL.14	MFP4	I	
		PG.6	MFP3	I	
		PI.6	MFP3	I	
		PK.10	MFP3	I	
		PJ.2	MFP3	I	
		PC.6	MFP3	I	
		PN.6	MFP3	I	
	CAN1_TXD	PB.15	MFP3	O	CAN FD1 bus transmitter output
		PL.15	MFP4	O	
		PG.7	MFP3	O	
		PI.7	MFP3	O	
		PK.11	MFP3	O	
		PJ.3	MFP3	O	
		PC.7	MFP3	O	
		PN.7	MFP3	O	
CAN FD2	CAN2_RXD	PA.15	MFP5	I	CAN FD2 bus receiver input
		PM.14	MFP4	I	
		PK.2	MFP3	I	
		PM.10	MFP3	I	
		PC.10	MFP3	I	
		PN.10	MFP3	I	
		PF.4	MFP13	I	
		PB.12	MFP5	I	
	CAN2_TXD	PG.1	MFP5	O	CAN FD2 bus transmitter output
		PM.15	MFP4	O	

		PK.3	MFP3	O	
		PM.11	MFP3	O	
		PC.11	MFP3	O	
		PN.11	MFP3	O	
		PF.5	MFP13	O	
		PB.13	MFP5	O	
CAN FD3	CAN3_RXD	PD.14	MFP3	I	CAN FD3 bus receiver input
		PA.14	MFP3	I	
		PJ.14	MFP3	I	
		PL.10	MFP3	I	
		PL.2	MFP3	I	
		PM.2	MFP3	I	
		PJ.6	MFP3	I	
		PG.8	MFP3	I	
		PN.14	MFP3	I	
		PK.14	MFP3	I	
	CAN3_TXD	PD.15	MFP3	O	CAN FD3 bus transmitter output
		PG.0	MFP3	O	
		PJ.15	MFP3	O	
		PL.11	MFP3	O	
		PL.3	MFP3	O	
		PM.3	MFP3	O	
		PJ.7	MFP3	O	
		PG.9	MFP3	O	
		PN.15	MFP3	O	
		PK.15	MFP3	O	

Table 15-1 CAN FD Interface Pin List

15.2 Reference Connection

Termination is typically a 120 Ω resistor at each end of the bus. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination uses two 60 Ω resistors with a capacitor in the middle of these resistors to ground. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common mode voltages at the start and end of message transmissions.

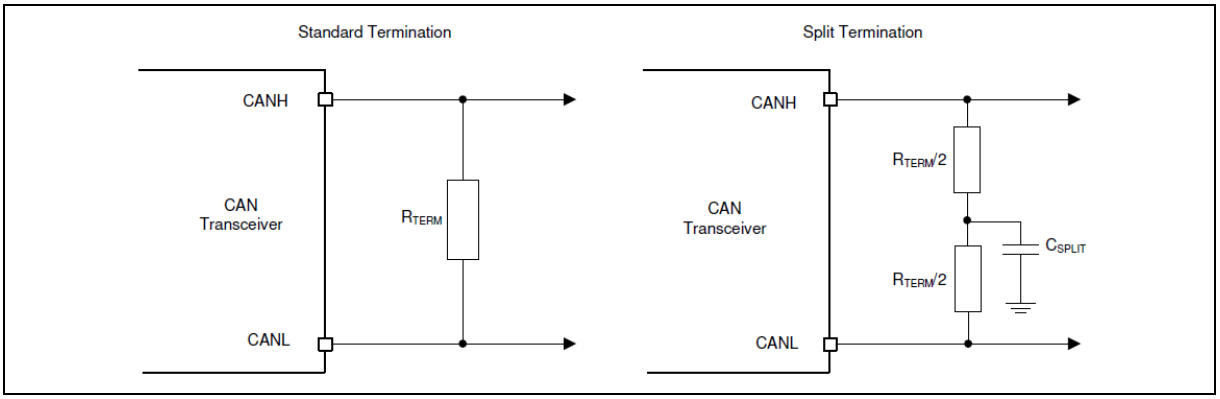


Figure 15-1 CAN BUS Typical Application

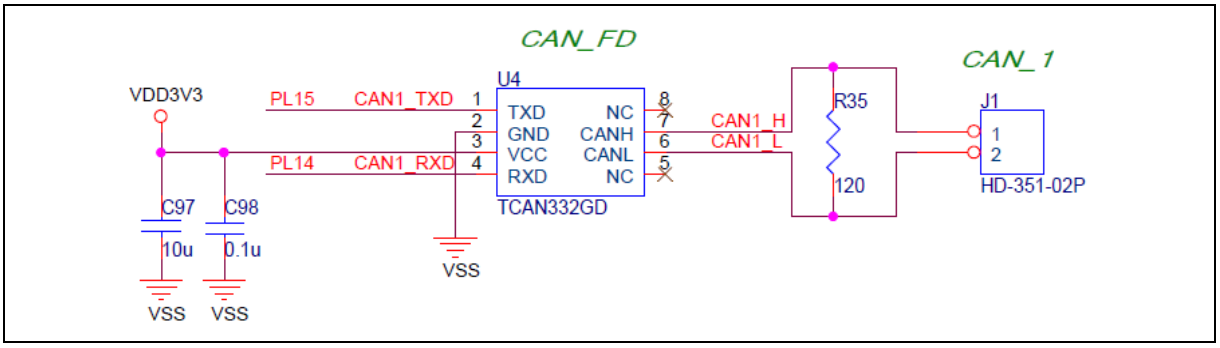


Figure 15-2 Reference Circuit for CAN BUS Transceiver Connection

15.3 Layout Recommendation for CAN FD BUS

The following points should be considered to achieve best performance:

- TxD and RxD connections to MA35D1 should be as short as possible, from MA35D1 port to transceiver TxD pin of than 30 ns.
- Place one individual 100nF capacitor close to transceiver power pin for local decoupling, it is recommended to use ceramic capacitors.
- Avoid routing CANH and CANL in parallel to fast-switching lines to reduce noise injection to the bus.
- CANH and CANL tracks should have the same length.

- Avoid routing transceiver V_{CC}/GND supply and microcontroller V_{CC}/GND supply in series to reduce coupled noise to the transceiver.
- In case an external ESD protection circuit is used, make sure the total capacitance is lower than 50pF. Use equal ESD protection for CANH and CANL to improve signal symmetry.
- For EMI improvement a CMC (common mode choke with 100uH impedance) is probably used, which has to be placed as close as possible to the transceiver bus pin CANH and CANL.
- For CAN FD application it is recommended to use a Common Mode Choke and a Split termination with a capacitance of 4.7nF to achieve excellent EME performance in automotive applications.

16 FMI NAND Interfaces

The MA35D1 Flash Memory Interface (FMI) controller has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for NFI to exchange data between system memory (e.g. SDRAM) and shared buffer (128 bytes), and the NAND Flash unit controls the interface of NAND Flash. The interface controller can support NAND-type Flash and the NFI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

16.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
NAND	NAND_ALE	PA.12	MFP6	O	NAND Flash address latch enable output pin
	NAND_CLE	PA.11	MFP6	O	NAND Flash command latch enable output pin
	NAND_DATA0	PA.0	MFP6	I/O	NAND Flash date bus bit 0
	NAND_DATA1	PA.1	MFP6	I/O	NAND Flash date bus bit 1
	NAND_DATA2	PA.2	MFP6	I/O	NAND Flash date bus bit 2
	NAND_DATA3	PA.3	MFP6	I/O	NAND Flash date bus bit 3
	NAND_DATA4	PA.4	MFP6	I/O	NAND Flash date bus bit 4
	NAND_DATA5	PA.5	MFP6	I/O	NAND Flash date bus bit 5
	NAND_DATA6	PA.6	MFP6	I/O	NAND Flash date bus bit 6
	NAND_DATA7	PA.7	MFP6	I/O	NAND Flash date bus bit 7
	NAND_RDY	PA.8	MFP6	I	NAND Flash ready/busy input pin
	NAND_nCS	PA.13	MFP6	O	NAND Flash chip select pin
	NAND_nRE	PA.9	MFP6	O	NAND Flash read enable output pin
	NAND_nWE	PA.10	MFP6	O	NAND Flash write enable output pin
	NAND_nWP	PA.14	MFP6	I	NAND Flash write protect input pin

Table 16-1 NAND Interface Pin List

16.2 FMI Reference Connection

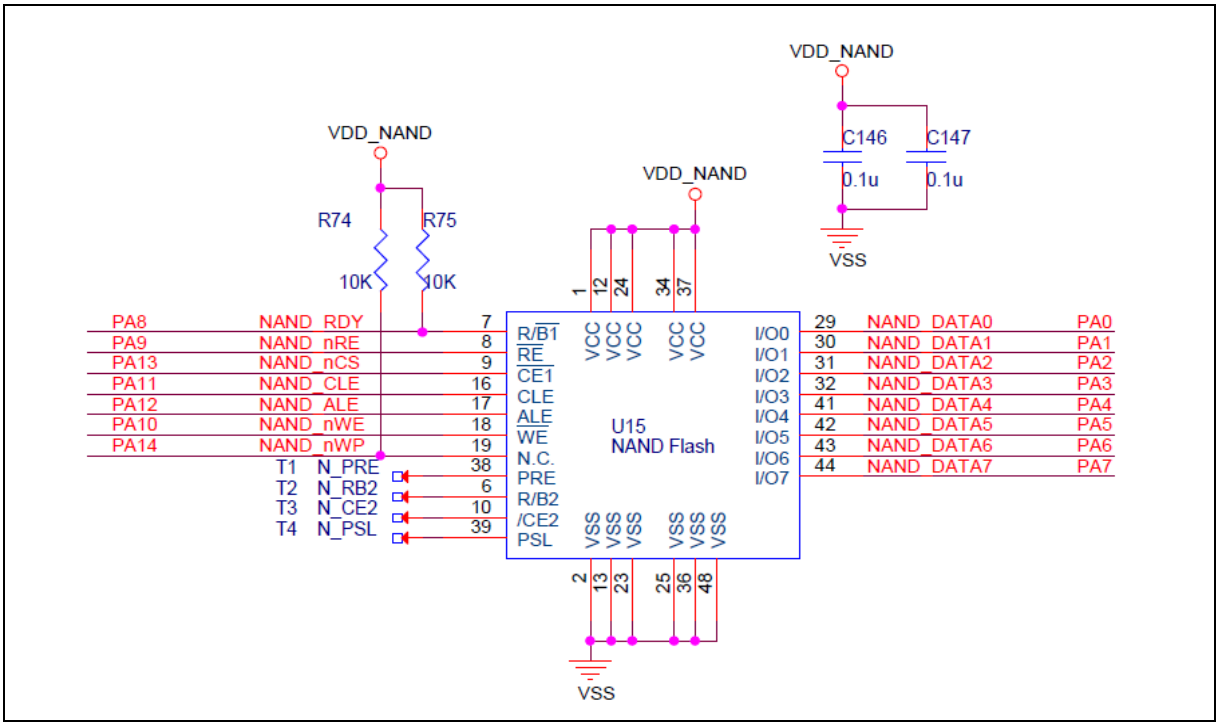


Figure 16-1 Reference Circuit for NAND Flash Connectivity

16.3 General PCB Signal Routing Guidelines

The following general guidelines must be considered before and throughout the PCB layout design effort:

- Use the V_{SS} plane as a primary reference or return path for all signals. Power should only be considered as secondary reference option where a solid continuous ground reference is also present.
- Avoid multiple via on reference planes to eliminate or minimize return current discontinuity.
- Try to avoid routing signal traces at the edge of the reference plane.
- Route the identified longest signal trace first before routing and adjusting the length of other signal traces.
- Route the same signal groups on the same signal layer and follow the routing from pin to pin as a group (that is, route them together).
- Isolate the ground return path of analog signals from digital signals; i.e. separate digital and analog grounds.

17 SD/ eMMC Interfaces

The Secure Digital Host Controller (SD Host) has DMA engine, host controller registers, FIFO controller and SD/UHS-I/eMMC unit. The DMA engine provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer, and DMA options such as SDMA (Single operation DMA), ADMA2 (Advanced DMA) and ADMA3 as specified in the SD host controller standard. The SD host controller can support SD or eMMC specification and cooperate with the DMA engine to provide a fast data transfer between system memory and cards.

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports data transfer type such as CPU, SDMA and ADMA2 for SD, eMMC mode.
- Supports 1-bit and 4-bit data bus widths for the SD memory card specification version 3.0. (SDR104 speed limited to maximum allowed I/O speed. SPI mode, DDR50 and UHS-II mode not supported).
- Supports 1-bits, 4-bits and 8-bits data bus widths for the eMMC interface. (HS200 speed limited to maximum allowed I/O speed and HS400 is not supported).
- Supports 1-bit, 4-bit and 8-bit data bus widths for the eMMC interface.
- Supports SD/SDHC/SDXC/SDIO, eMMC card.
- Supports gating of controller base clock if host controller is inactive.
- Supports two set of SD host controllers, only one can support UHS-I mode.
- Supports SD/eMMC tuning, CMD19(SD) or CMD21(eMMC).
- Supports 50 MHz to achieve SD 25 Mbyte/s for 4-bit mode.
- Supports 200 MHz to achieve eMMC HS200 at 1.8V I/O operation.

17.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
SD0	SD0_CLK/eMMC0_CLK	PC.1	MFP6	O	SD/SDIO0 clock output pin eMMC0 clock output pin
	SD0_CMD/eMMC0_CMD	PC.0	MFP6	I/O	SD/SDIO0 command/response pin eMMC0 command/response pin
	SD0_DAT0/eMMC0_DAT0	PC.2	MFP6	I/O	SD/SDIO0 data line bit 0 eMMC0 data line bit 0

	SD0_DAT1/eMMC0_DAT1	PC.3	MFP6	I/O	SD/SDIO0 data line bit 1 eMMC0 data line bit 1
	SD0_DAT2/eMMC0_DAT2	PC.4	MFP6	I/O	SD/SDIO0 data line bit 2 eMMC0 data line bit 2
	SD0_DAT3/eMMC0_DAT3	PC.5	MFP6	I/O	SD/SDIO0 data line bit 3 eMMC0 data line bit 3
	SD0_nCD	PC.6	MFP6	I	SD/SDIO0 card detect input pin
	SD0_WP	PC.7	MFP6	I	SD/SDIO0 write protect input
SD1	SD1_CLK/eMMC1_CLK	PJ.7	MFP6	O	SD/SDIO1 clock output pin eMMC1 clock output pin
	SD1_CMD/eMMC1_CMD	PJ.6	MFP6	I/O	SD/SDIO1 command/response pin eMMC1 command/response pin
	SD1_DAT0/eMMC1_DAT0	PJ.8	MFP6	I/O	SD/SDIO1 data line bit 0 eMMC1 data line bit 0
	SD1_DAT1/eMMC1_DAT1	PJ.9	MFP6	I/O	SD/SDIO1 data line bit 1 eMMC1 data line bit 1
	SD1_DAT2/eMMC1_DAT2	PJ.10	MFP6	I/O	SD/SDIO1 data line bit 2 eMMC1 data line bit 2
	SD1_DAT3/eMMC1_DAT3	PJ.11	MFP6	I/O	SD/SDIO1 data line bit 3 eMMC1 data line bit 3
	SD1_WP	PJ.4	MFP6	I	SD/SDIO1 write protect input
	SD1_nCD	PJ.5	MFP6	I	SD/SDIO1 card detect input pin
eMMC1	eMMC1_DAT4	PJ.0	MFP6	I/O	eMMC1 data line bit 4
	eMMC1_DAT5	PJ.1	MFP6	I/O	eMMC1 data line bit 5
	eMMC1_DAT6	PJ.2	MFP6	I/O	eMMC1 data line bit 6
	eMMC1_DAT7	PJ.3	MFP6	I/O	eMMC1 data line bit 7

Table 17-1 NAND Interface Pin List

17.2 SD/ eMMC Reference Connection

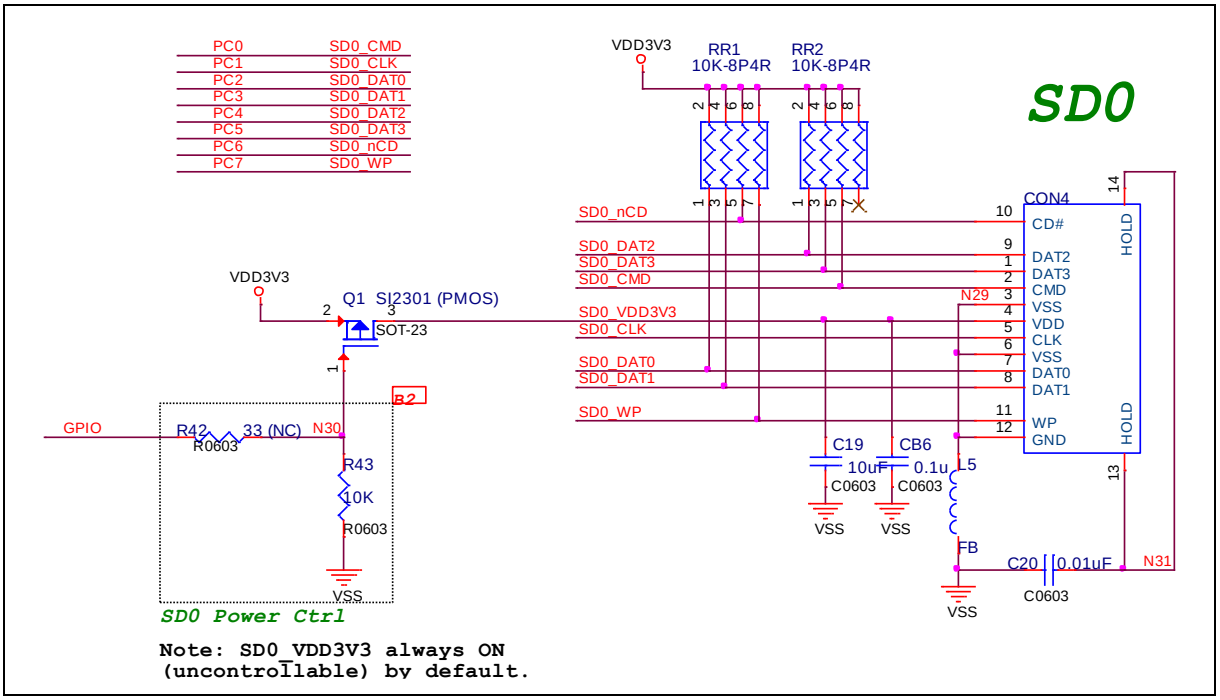


Figure 17-1 Reference Circuit for SD0 Connectivity with PC Port

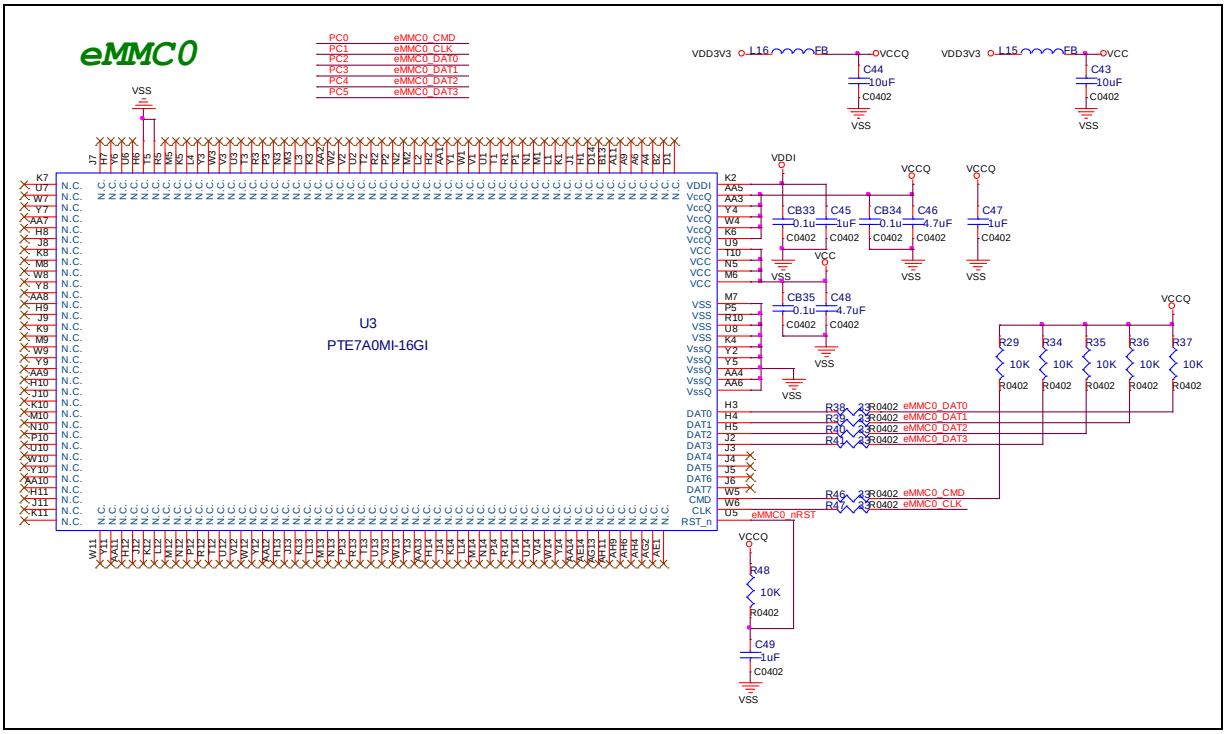


Figure 17-2 Reference Circuit for eMMC0 Connectivity with PC Port

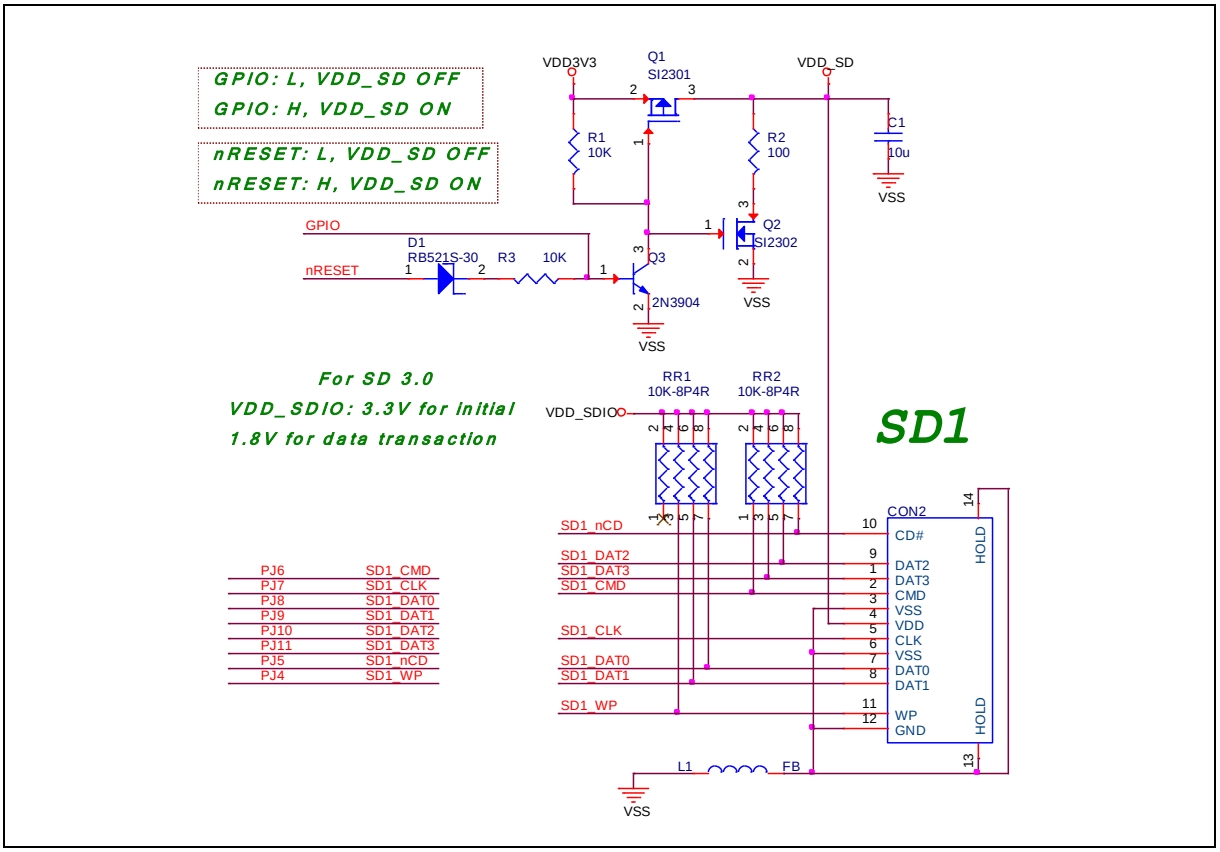


Figure 17-3 Reference Circuit for SD1 Connectivity with PJ Port

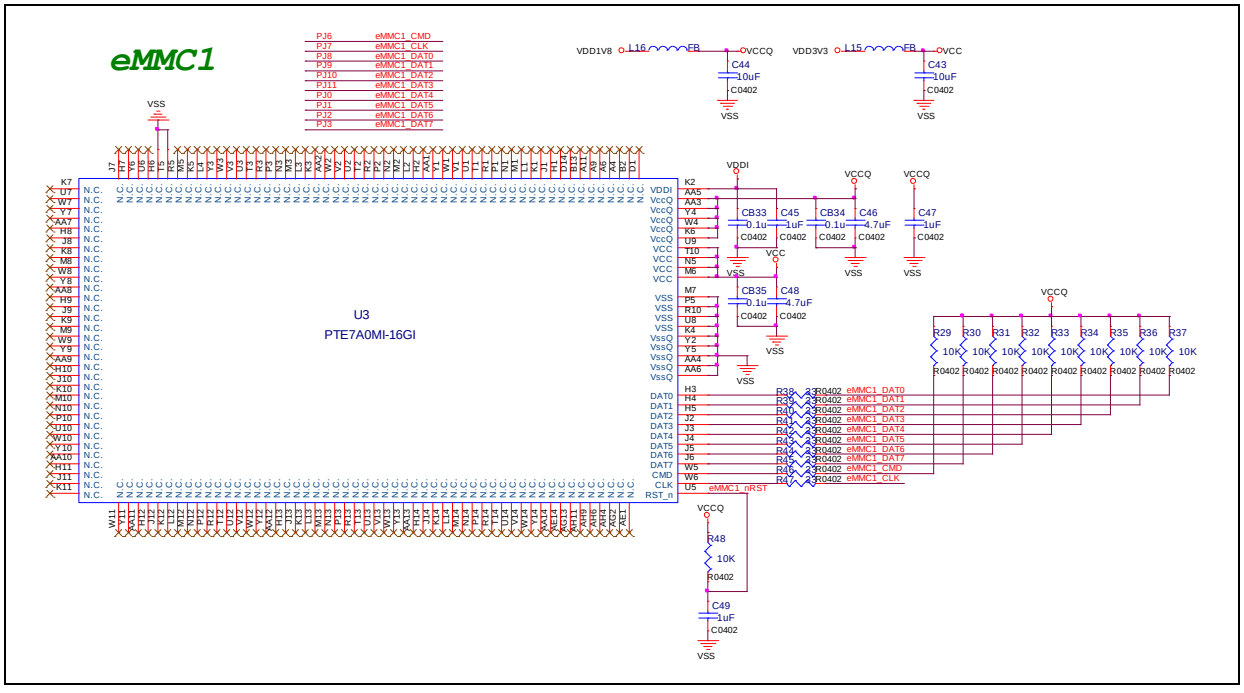


Figure 17-4 Reference Circuit for eMMC1 Connectivity with PJ Port

17.3 General PCB Signal Routing Guidelines

The following general guidelines must be considered before and throughout the PCB layout design effort:

- Use the V_{SS} plane as a primary reference or return path for all signals. Power should only be considered as secondary reference option where a solid continuous ground reference is also present.
- Avoid multiple via on reference planes to eliminate or minimize return current discontinuity.
- Try to avoid routing signal traces at the edge of the reference plane.
- Route the identified longest signal trace first before routing and adjusting the length of other signal traces.
- Route the same signal groups on the same signal layer and follow the routing from pin to pin as a group (that is, route them together).
- Isolate the ground return path of analog signals from digital signals; i.e. separate digital and analog grounds.
- For SD connectivity, if SD_CLK has serials a resistor for signal quality recovery that it should be placed to MA35D1 side ASAP.
- About ESD protection parts for SD, the ESD parts location must close to SD connector side ASAP and also need to use low capacitance CL value to avoid that side-effect wh
- All signals and clock should be routed with controlled impedance. Typically, the PCB is recommended to be built using 50 Ω trace impedance with ± 5% tolerance.
- SD data bus should be routed with matching length to the reference of the clock. The matching length, typically, When CLK=50MHz max skew between data signal <100ps ≒15 mm, When CLK=200MHz max skew between data signal <20ps≒3 mm
- eMMC signal trace length skew constraints

  ABS(CLK – DATA0~7)≦250 mil

  ABS(CLK – CMD)≦250 mil
- eMMC total signal trace length < 2000 mil
- Suggested to use the GND shiedlding to reduce crosstalk effect for eMMC signals.

18 I²C, SPI and I²S Interfaces

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The MA35D1 series provides six sets of I²C devices with Master/Slave mode, which supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps), which can support SMBus and PMBus and with PDMA operation.

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Except for two QSPI controllers, the MA35D1 series also has up to four sets of SPI controllers to support Master or Slave mode operation, Master mode up to 100 MHz and Slave mode up to 100 MHz. Each SPI controller can support the PDMA function to access the data buffer.

The I²S controller consists of I²S and PCM protocols to interface with external audio CODEC. The I²S and PCM interface supports 8-, 16-, 18-, 20- and 24-bit left/right precision in record and playback. The MA35D1 series has two sets of I²S controllers using DMA to playback and record data with interrupt, which supports I²S interface record and playback with mater and slave mode, and also supports PCM interface record and playback with master mode only.

18.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
I²C0	I2C0_SCL	PD.7	MFP6	I/O	I²C 0 clock pin
		PM.9	MFP4	I/O	
		PC.9	MFP4	I/O	
		PN.9	MFP4	I/O	
	I2C 0_SDA	PD.6	MFP6	I/O	I²C 0 data input/output pin
		PM.8	MFP4	I/O	
		PC.8	MFP4	I/O	
		PN.8	MFP4	I/O	
I²C 1	I2C1_SCL	PN.5	MFP4	I/O	I²C 1 clock pin
		PB.11	MFP12	I/O	
	I2C1_SDA	PN.4	MFP4	I/O	I²C 1 data input/output pin
		PB.10	MFP12	I/O	
I²C 2	I2C 2_SCL	PL.13	MFP10	I/O	I²C 2 clock pin
		PM.13	MFP5	I/O	

		PI.1	MFP4	I/O	
		PJ.1	MFP4	I/O	
		PD.5	MFP4	I/O	
		PN.1	MFP4	I/O	
		PB.9	MFP4	I/O	
	I2C2_SDA	PL.12	MFP10	I/O	I²C2 data input/output pin
		PM.12	MFP5	I/O	
		PI.0	MFP4	I/O	
		PJ.0	MFP4	I/O	
		PD.4	MFP4	I/O	
		PN.0	MFP4	I/O	
		PB.8	MFP4	I/O	
I²C 3	I2C3_SCL	PM.15	MFP6	I/O	I²C3 clock pin
		PI.5	MFP4	I/O	
		PL.1	MFP4	I/O	
		PK.9	MFP4	I/O	
		PJ.5	MFP4	I/O	
		PG.9	MFP7	I/O	
		PB.13	MFP4	I/O	
	I2C3_SDA	PM.14	MFP6	I/O	I²C3 data input/output pin
		PI.4	MFP4	I/O	
		PL.0	MFP4	I/O	
		PK.8	MFP4	I/O	
		PJ.4	MFP4	I/O	
		PG.8	MFP7	I/O	
		PB.12	MFP4	I/O	

I²C 4	I2C4_SCL	PB.15	MFP5	I/O	I²C4 clock pin
		PD.13	MFP4	I/O	
		PG.1	MFP4	I/O	
		PK.1	MFP4	I/O	
		PL.5	MFP4	I/O	
		PM.1	MFP4	I/O	
		PJ.9	MFP4	I/O	
		PK.5	MFP4	I/O	
		PC.1	MFP4	I/O	
		PK.13	MFP4	I/O	
		PF.7	MFP10	I/O	
	I2C4_SDA	PB.14	MFP5	I/O	I²C4 data input/output pin
		PD.12	MFP4	I/O	
		PA.15	MFP4	I/O	
		PK.0	MFP4	I/O	
		PL.4	MFP4	I/O	
		PM.0	MFP4	I/O	
		PJ.8	MFP4	I/O	
		PC.0	MFP4	I/O	
		PK.12	MFP4	I/O	
		PF.6	MFP10	I/O	
I²C 5	I2C5_SCL	PJ.13	MFP4	I/O	I²C5 clock pin
		PL.9	MFP4	I/O	
		PM.5	MFP4	I/O	
		PC.5	MFP4	I/O	
		PN.13	MFP4	I/O	

		PK.15	MFP10	I/O	
		PF.9	MFP4	I/O	
	I2C5_SDA	PJ.12	MFP4	I/O	I²C5 data input/output pin
		PL.8	MFP4	I/O	
		PM.4	MFP4	I/O	
		PC.4	MFP4	I/O	
		PN.12	MFP4	I/O	
		PK.14	MFP10	I/O	
		PF.8	MFP4	I/O	

Table 18-1 I²C0/1/2/3/4/5 Interfaces Pin List

Group	Pin Name	GPIO	MFP	Type	Description
SPI0	SPI0_CLK	PL.13	MFP5	I/O	SPI0 serial clock pin
		PB.9	MFP5	I/O	
	SPI0_I2SMCLK	PG.3	MFP5	I/O	SPI0 I²S master clock output pin
		PF.14	MFP5	I/O	
		PB.8	MFP6	I/O	
	SPI0_MISO	PL.15	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin
		PB.11	MFP5	I/O	
	SPI0_MOSI	PL.14	MFP5	I/O	SPI0 MOSI (Master Out, Slave In) pin
		PB.10	MFP5	I/O	
	SPI0_SS0	PL.12	MFP5	I/O	SPI0 slave select 0 pin
		PG.0	MFP5	I/O	
		PF.8	MFP5	I/O	
	SPI0_SS1	PG.2	MFP5	I/O	SPI0 slave select 1 pin
		PF.9	MFP5	I/O	
		PB.8	MFP5	I/O	

SPI1	SPI1_CLK	PC.9	MFP5	I/O	SPI1 serial clock pin
		PK.13	MFP6	I/O	
		PE.11	MFP5	I/O	
		PF.5	MFP5	I/O	
		PF.11	MFP6	I/O	
	SPI1_I2SMCLK	PN.9	MFP5	I/O	SPI1 I^2S master clock output pin
		PN.14	MFP7	I/O	
		PN.15	MFP7	I/O	
		PF.14	MFP6	I/O	
	SPI1_MISO	PC.11	MFP5	I/O	SPI1 MISO (Master In, Slave Out) pin
		PK.15	MFP6	I/O	
		PE.13	MFP5	I/O	
		PF.7	MFP5	I/O	
		PF.13	MFP6	I/O	
	SPI1_MOSI	PC.10	MFP5	I/O	SPI1 MOSI (Master Out, Slave In) pin
		PK.14	MFP6	I/O	
		PE.12	MFP5	I/O	
		PF.6	MFP5	I/O	
		PF.12	MFP6	I/O	
	SPI1_SS0	PC.8	MFP5	I/O	SPI1 slave select 0 pin
		PK.12	MFP6	I/O	
		PE.10	MFP5	I/O	
		PF.4	MFP5	I/O	
		PF.10	MFP6	I/O	
	SPI1_SS1	PN.14	MFP5	I/O	SPI1 slave select 1 pin
		PN.15	MFP6	I/O	

		PF.14	MFP13	I/O	
SPI2	SPI2_CLK	PL.3	MFP5	I/O	SPI2 serial clock pin
		PJ.1	MFP5	I/O	
		PG.9	MFP5	I/O	
		PK.5	MFP5	I/O	
	SPI2_I2SMCLK	PM.10	MFP7	I/O	SPI2 I²S master clock output pin
		PN.8	MFP5	I/O	
	SPI2_MISO	PL.1	MFP5	I/O	SPI2 MISO (Master In, Slave Out) pin
		PJ.3	MFP5	I/O	
		PK.4	MFP5	I/O	
		PK.7	MFP5	I/O	
	SPI2_MOSI	PL.0	MFP5	I/O	SPI2 MOSI (Master Out, Slave In) pin
		PJ.2	MFP5	I/O	
		PG.10	MFP5	I/O	
		PK.6	MFP5	I/O	
	SPI2_SS0	PL.2	MFP5	I/O	SPI2 slave select 0 pin
		PJ.0	MFP5	I/O	
		PG.8	MFP5	I/O	
	SPI2_SS1	PI.4	MFP5	I/O	SPI2 slave select 1 pin
		PM.11	MFP7	I/O	
SPI3	SPI3_CLK	PG.5	MFP5	I/O	SPI3 serial clock pin
		PI.1	MFP5	I/O	
		PJ.15	MFP5	I/O	
		PL.9	MFP5	I/O	
		PK.8	MFP5	I/O	
	SPI3_I2SMCLK	PK.2	MFP5	I/O	SPI3 I²S master clock output pin

		PM.1	MFP5	I/O	
	SPI3_MISO	PG.7	MFP5	I/O	SPI3 MISO (Master In, Slave Out) pin
		PI.3	MFP5	I/O	
		PJ.14	MFP5	I/O	
		PL.11	MFP5	I/O	
		PL.5	MFP5	I/O	
	SPI3_MOSI	PG.6	MFP5	I/O	SPI3 MOSI (Master Out, Slave In) pin
		PI.2	MFP5	I/O	
		PJ.13	MFP5	I/O	
		PL.10	MFP5	I/O	
		PL.4	MFP5	I/O	
	SPI3_SS0	PG.4	MFP5	I/O	SPI3 slave select 0 pin
		PI.0	MFP5	I/O	
		PJ.12	MFP5	I/O	
		PL.8	MFP5	I/O	
		PM.10	MFP5	I/O	
	SPI3_SS1	PK.3	MFP5	I/O	SPI3 slave select 1 pin
		PD.6	MFP10	I/O	
		PM.11	MFP5	I/O	

Table 18-2 SPI0/1/2/3 Interfaces Pin List

Group	Pin Name	GPIO	MFP	Tye	Description
I^2S0	I2S0_BCLK	PG.13	MFP5	O	I2S0 bit clock output pin
		PL.1	MFP7	O	
		PJ.1	MFP7	O	
		PK.13	MFP5	O	
		PF.5	MFP4	O	

		PF.11	MFP5	O	
	I2S0_DI	PG.14	MFP5	I	I2S0 data input pin
		PL.2	MFP7	I	
		PJ.2	MFP7	I	
		PK.14	MFP5	I	
		PF.6	MFP4	I	
		PF.12	MFP5	I	
	I2S0_DO	PG.15	MFP5	O	I2S0 data output pin
		PL.3	MFP7	O	
		PJ.3	MFP7	O	
		PK.15	MFP5	O	
		PF.7	MFP4	O	
		PF.13	MFP5	O	
	I2S0_LRCK	PG.12	MFP5	O	I2S0 left right channel clock output pin
		PL.0	MFP7	O	
		PJ.0	MFP7	O	
		PK.12	MFP5	O	
		PF.4	MFP4	O	
		PF.10	MFP5	O	
	I2S0_MCLK	PG.11	MFP5	O	I2S0 master clock output pin
		PD.6	MFP7	O	
		PL.4	MFP7	O	
		PN.15	MFP5	O	
		PF.14	MFP15	O	
		PB.9	MFP6	O	
I^2S1	I2S1_BCLK	PL.13	MFP6	O	I2S1 bit clock output pin

		PD.13	MFP12	O	
		PG.6	MFP9	O	
		PI.5	MFP6	O	
		PL.9	MFP7	O	
		PD.9	MFP7	O	
		PK.6	MFP7	O	
		PB.13	MFP6	O	
	I2S1_DI	PB.14	MFP6	I	I2S1 data input pin
		PL.14	MFP6	I	
		PD.14	MFP12	I	
		PG.5	MFP9	I	
		PI.6	MFP6	I	
		PL.10	MFP7	I	
		PD.10	MFP7	I	
		PK.5	MFP7	I	
	I2S1_DO	PB.15	MFP6	O	I2S1 data output pin
		PL.15	MFP6	O	
		PD.15	MFP12	O	
		PG.4	MFP9	O	
		PI.7	MFP6	O	
		PL.11	MFP7	O	
		PD.11	MFP7	O	
	I2S1_LRCK	PL.12	MFP6	O	I2S1 left right channel clock output pin
		PD.12	MFP12	O	
		PG.7	MFP9	O	
		PI.4	MFP6	O	

		PL.8	MFP7	O	
		PD.8	MFP7	O	
		PK.7	MFP7	O	
		PB.12	MFP6	O	
	I2S1_MCLK	PG.0	MFP9	O	I2S1 master clock output pin
		PG.3	MFP12	O	
		PM.12	MFP9	O	
		PK.0	MFP6	O	
		PD.7	MFP7	O	
		PL.5	MFP7	O	
		PB.9	MFP12	O	
		PB.11	MFP6	O	

Table 18-3 I²S0/1 Interface Pin List

18.2 Reference Connection

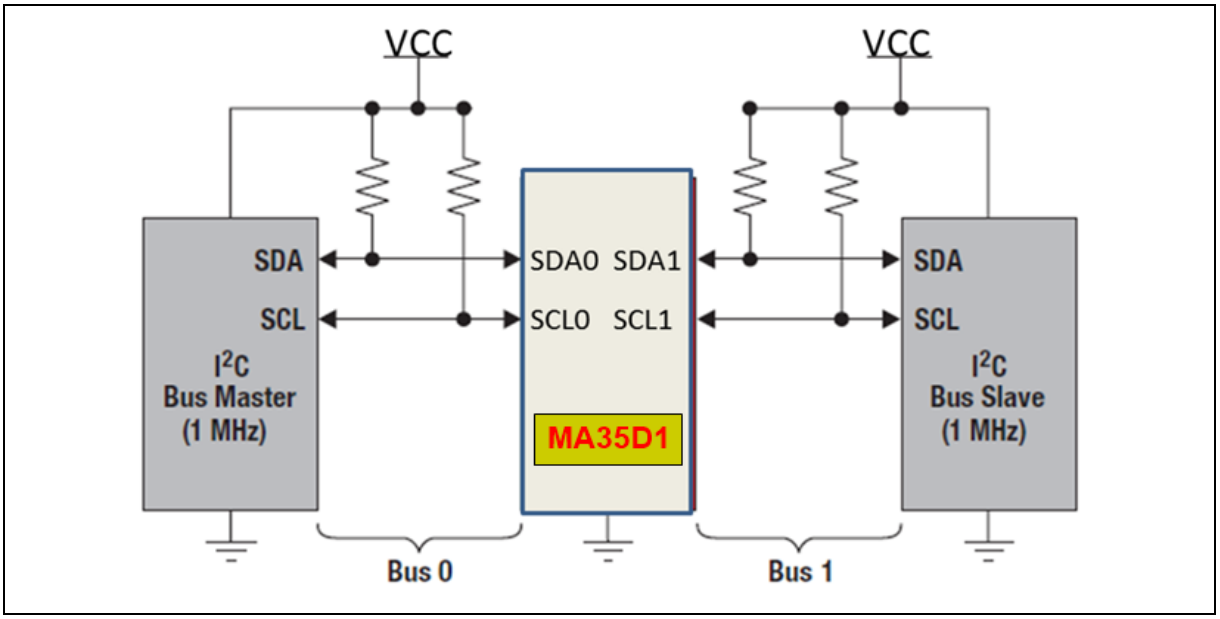


Figure 18-1 I²C Application Block Diagram

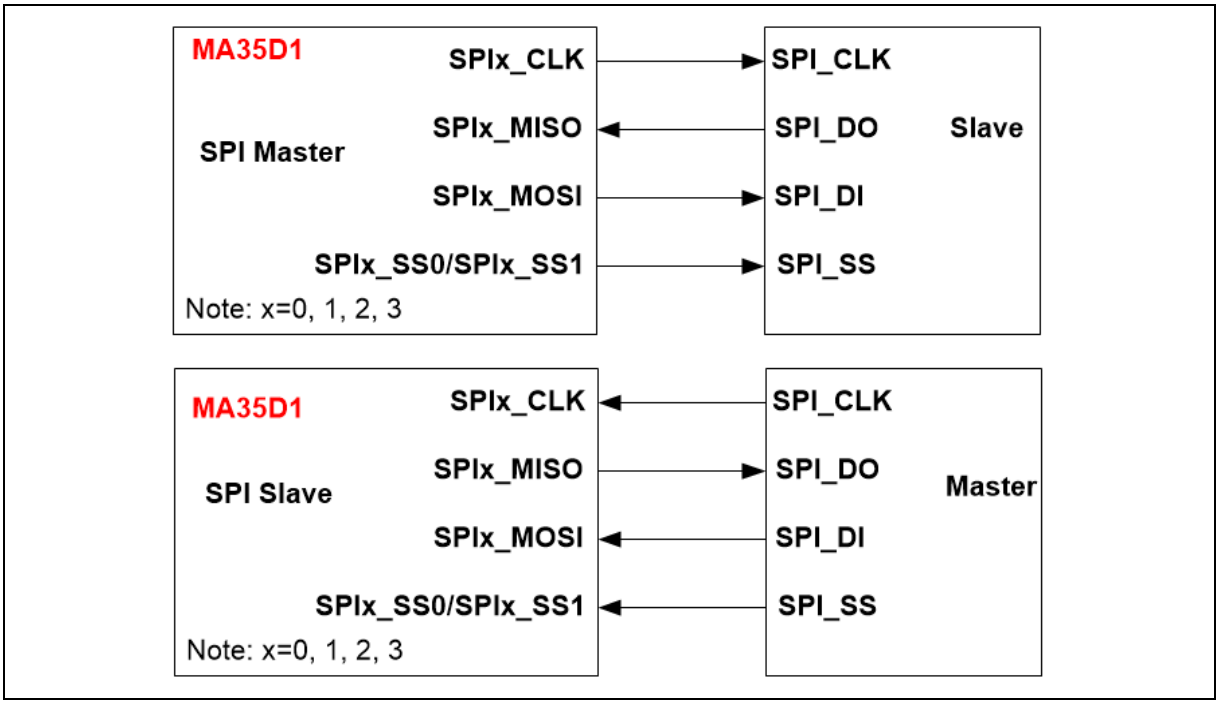


Figure 18-2 SPI0/1/2/3 Application Block Diagram

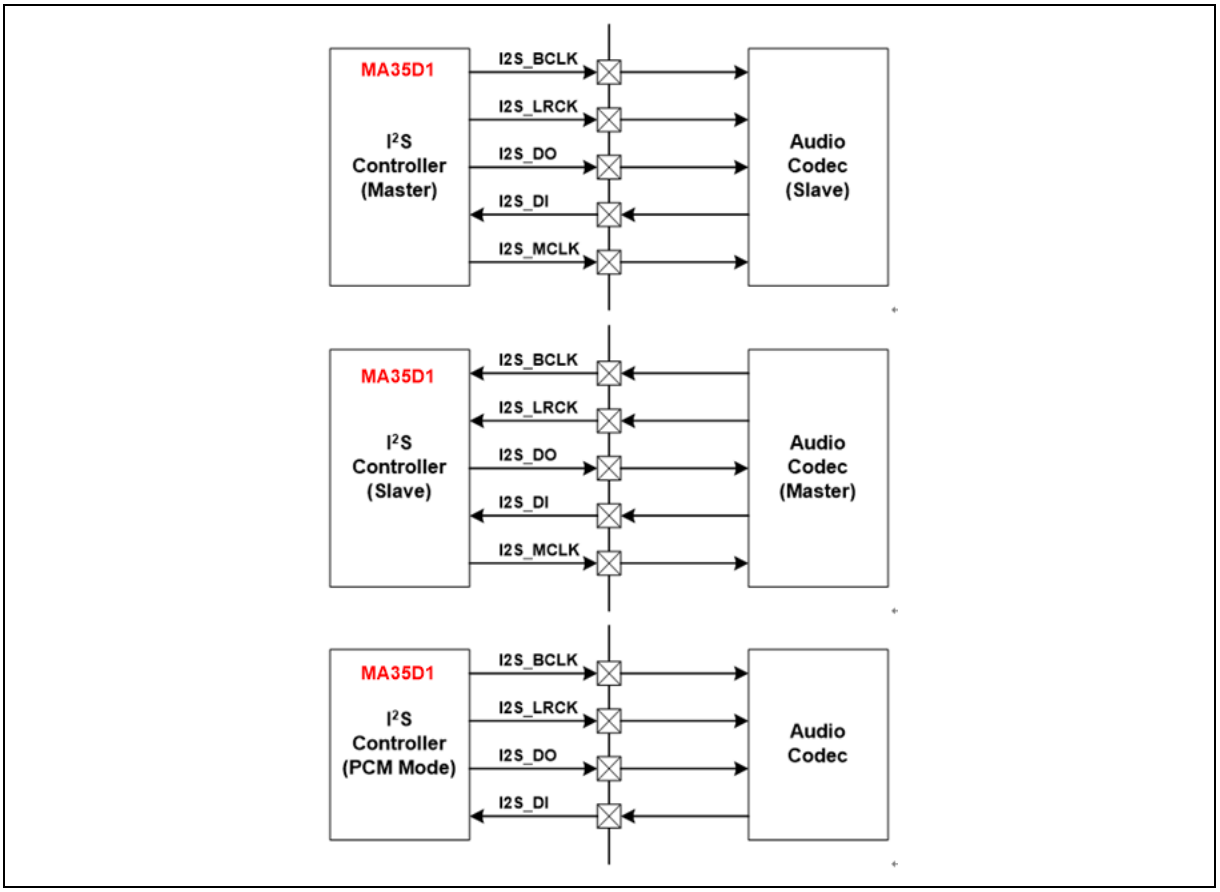


Figure 18-3 I²S Application Block Diagram

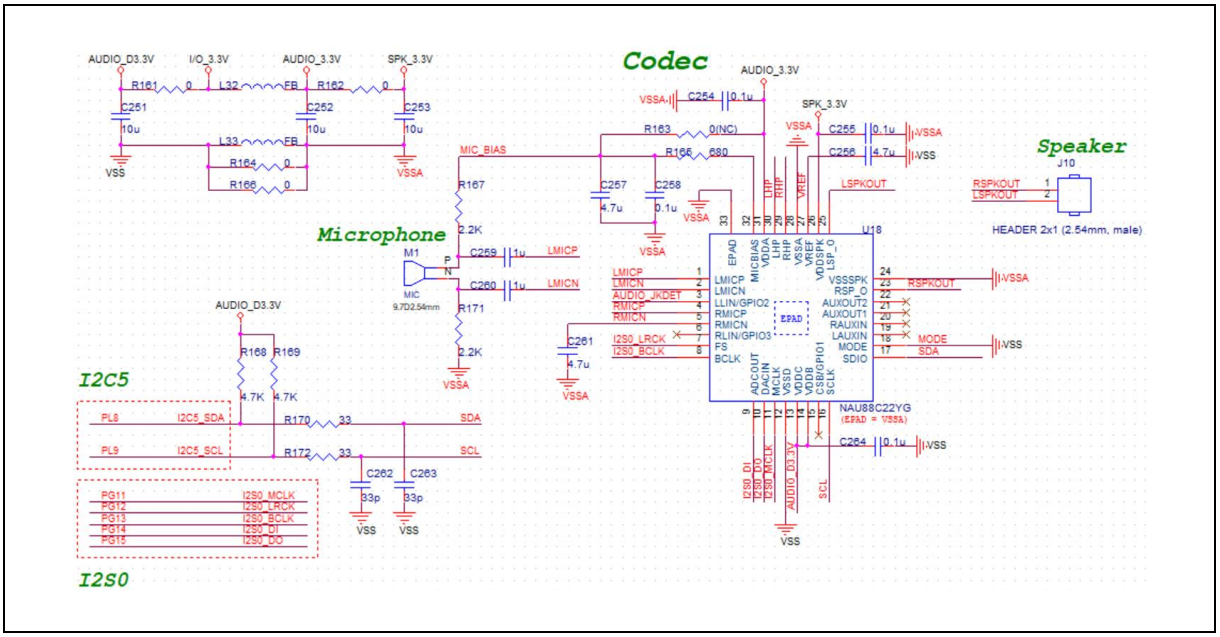


Figure 18-4 I²C and I²S Connectivity with External Audio Codec

18.3 PCB Layout Considerations

18.3.1 I²C

The I²C bus is a world standard over thousands different chips manufactured. Additionally, the I²C bus is used in various control architectures such as System Management Bus (SMBus), Power Management Bus (PMBus). Serial, 8-bit, bi-directional data transfers can be made at up to 100 Kbit/s in Standard-mode, up to 400 Kbit/s in Fast-mode, or up to 1 Mbit/s in Fast-mode Plus, also up to 3.4 Mbit/s in High-speed mode.

PCB design should have spike rejection filter on the bus data line to preserve data integrity. The number of ICs that can be connected to the same bus is limited only by the maximum bus capacitance. More capacitance may be allowed under some conditions. As Figure 18-1, the reserved the serial resistor and capacitor of termination for I²C bus signals integrity preservation.

18.3.2 SPI

The Serial Peripheral Interface (SPI) bus is a full duplex synchronous serial communication interface specification used for short distance communication. SPI devices communicate in full duplex mode using Master-Slave architecture with a single master. The master device originates the frame for reading and writing. Multiple slave devices are supported through selection, with individual slaves selected by CS lines.

The MA35D1 series may be configurable as a SPI master or slave depending on the application, with two SPI devices that can be used. The SPI interface could be an external serial flash or application processor that needs to be configurable to different memory maps.

Same as QSPI0, SPI CLK speed also supports up to 100 MHz, about the PCB layout consideration can be follow up.

18.3.3 I²S

The MA35D1 evaluation board provides I²S interface and is connected with an external audio codec NAU88C22 shown as Figure 18-4. The driver of the I²S device is available for now.

I²S is a digital audio interface can connect to master/slave device directly without concerns. For device quality and performance, such as NAU88C22 audio codec, please refer to the NAU88C22 design guidelines.

19 UART and Smart Card Interface (ISO/IEC 7816-3)

The MA35D1 series provides seventeen channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. The MA35D1 series provides up to two ISO-7816-3 ports. It has separated receive/transmit 4-byte entry FIFO for data payloads can support UART mode with full duplex, asynchronous communications.

19.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
UART0	UART0_RXD	PE.15	MFP1	I	UART0 data receiver input pin
	UART0_TXD	PE.14	MFP1	O	UART0 data transmitter output pin
UART1	UART1_RXD	PA.2	MFP2	I	UART1 data receiver input pin
		PJ.12	MFP3	I	
		PD.6	MFP2	I	
		PL.4	MFP3	I	
		PK.14	MFP2	I	
		PF.0	MFP3	I	
		PB.8	MFP3	I	
	UART1_TXD	PA.3	MFP2	O	UART1 data transmitter output pin
		PJ.13	MFP3	O	
		PD.7	MFP2	O	
		PL.5	MFP3	O	
		PK.15	MFP2	O	
		PF.1	MFP3	O	

		PB.9	MFP3	O	
	UART1_nCTS	PA.0	MFP2	I	UART1 clear to Send input pin
		PD.4	MFP2	I	
		PK.12	MFP2	I	
	UART1_nRTS	PA.1	MFP2	O	UART1 request to Send output pin
		PD.5	MFP2	O	
		PK.13	MFP2	O	
UART2	UART2_RXD	PA.4	MFP3	I	UART2 data receiver input pin
		PJ.14	MFP2	I	
		PL.6	MFP2	I	
		PD.4	MFP3	I	
		PF.2	MFP2	I	
		PB.10	MFP2	I	
	UART2_TXD	PA.5	MFP3	O	UART2 data transmitter output pin
		PJ.15	MFP2	O	
		PL.7	MFP2	O	
		PD.5	MFP3	O	
		PF.3	MFP2	O	
		PB.11	MFP2	O	
	UART2_nCTS	PJ.12	MFP2	I	UART2 clear to Send input pin
		PL.4	MFP2	I	
		PF.0	MFP2	I	
		PB.8	MFP2	I	
	UART2_nRTS	PJ.13	MFP2	O	UART2 request to Send output pin
		PL.5	MFP2	O	
		PF.1	MFP2	O	

		PB.9	MFP2	O	
UART3	UART3_RXD	PA.6	MFP2	I	UART3 data receiver input pin
		PI.8	MFP3	I	
		PD.2	MFP2	I	
		PE.4	MFP3	I	
		PB.12	MFP3	I	
	UART3_TXD	PA.7	MFP2	O	UART3 data transmitter output pin
		PI.9	MFP3	O	
		PD.3	MFP2	O	
		PE.5	MFP3	O	
		PB.13	MFP3	O	
	UART3_nCTS	PA.4	MFP2	I	UART3 clear to Send input pin
		PD.0	MFP2	I	
	UART3_nRTS	PA.5	MFP2	O	UART3 request to Send output pin
		PD.1	MFP2	O	
UART4	UART4_RXD	PB.14	MFP2	I	UART4 data receiver input pin
		PA.8	MFP3	I	
		PI.10	MFP2	I	
		PD.0	MFP3	I	
		PE.6	MFP2	I	
	UART4_TXD	PB.15	MFP2	O	UART4 data transmitter output pin
		PA.9	MFP3	O	
		PI.11	MFP2	O	
		PD.1	MFP3	O	
		PE.7	MFP2	O	
	UART4_nCTS	PI.8	MFP2	I	UART4 clear to Send input pin

		PE.4	MFP2	I	
		PB.12	MFP2	I	
	UART4_nRTS	PI.9	MFP2	O	UART4 request to Send output pin
		PE.5	MFP2	O	
		PB.13	MFP2	O	
UART5	UART5_RXD	PA.10	MFP2	I	UART5 data receiver input pin
		PG.6	MFP2	I	
		PI.12	MFP3	I	
	UART5_TXD	PA.11	MFP2	O	UART5 data transmitter output pin
		PG.7	MFP2	O	
		PI.13	MFP3	O	
	UART5_nCTS	PA.8	MFP2	I	UART5 clear to Send input pin
		PG.4	MFP2	I	
	UART5_nRTS	PA.9	MFP2	O	UART5 request to Send output pin
		PG.5	MFP2	O	
UART6	UART6_RXD	PA.15	MFP3	I	UART6 data receiver input pin
		PG.4	MFP3	I	
		PI.14	MFP2	I	
		PN.14	MFP2	I	
	UART6_TXD	PG.1	MFP3	O	UART6 data transmitter output pin
		PG.5	MFP3	O	
		PI.15	MFP2	O	
		PN.15	MFP2	O	
	UART6_nCTS	PI.12	MFP2	I	UART6 clear to Send input pin
		PN.12	MFP2	I	
	UART6_nRTS	PI.13	MFP2	O	UART6 request to Send output pin

		PN.13	MFP2	O	
UART7	UART7_RXD	PL.14	MFP2	I	UART7 data receiver input pin
		PA.14	MFP2	I	
		PJ.0	MFP3	I	
		PH.0	MFP3	I	
	UART7_TXD	PL.15	MFP2	O	UART7 data transmitter output pin
		PG.0	MFP2	O	
		PJ.1	MFP3	O	
		PH.1	MFP3	O	
	UART7_nCTS	PL.12	MFP2	I	UART7 clear to Send input pin
		PA.12	MFP2	I	
	UART7_nRTS	PL.13	MFP2	O	UART7 request to Send output pin
		PA.13	MFP2	O	
UART8	UART8_RXD	PA.12	MFP3	I	UART8 data receiver input pin
		PJ.2	MFP2	I	
		PH.2	MFP2	I	
		PE.0	MFP3	I	
	UART8_TXD	PA.13	MFP3	O	UART8 data transmitter output pin
		PJ.3	MFP2	O	
		PH.3	MFP2	O	
		PE.1	MFP3	O	
	UART8_nCTS	PJ.0	MFP2	I	UART8 clear to Send input pin
		PH.0	MFP2	I	
	UART8_nRTS	PJ.1	MFP2	O	UART8 request to Send output pin
		PH.1	MFP2	O	
UART9	UART9_RXD	PG.2	MFP2	I	UART9 data receiver input pin

		PH.4	MFP3	I	
		PC.8	MFP3	I	
		PE.2	MFP2	I	
	UART9_TXD	PG.3	MFP2	O	UART9 data transmitter output pin
		PH.5	MFP3	O	
		PC.9	MFP3	O	
		PE.3	MFP2	O	
	UART9_nCTS	PA.15	MFP2	I	UART9 clear to Send input pin
		PE.0	MFP2	I	
	UART9_nRTS	PG.1	MFP2	O	UART9 request to Send output pin
		PE.1	MFP2	O	
UART10	UART10_RXD	PD.12	MFP3	I	UART10 data receiver input pin
		PM.14	MFP2	I	
		PL.0	MFP3	I	
		PH.6	MFP2	I	
		PC.10	MFP2	I	
		PF.4	MFP3	I	
	UART10_TXD	PD.13	MFP3	O	UART10 data transmitter output pin
		PM.15	MFP2	O	
		PL.1	MFP3	O	
		PH.7	MFP2	O	
		PC.11	MFP2	O	
		PF.5	MFP3	O	
	UART10_nCTS	PM.12	MFP2	I	UART10 clear to Send input pin
		PH.4	MFP2	I	
		PC.8	MFP2	I	

	UART10_nRTS	PM.13	MFP2	O	UART10 request to Send output pin
		PH.5	MFP2	O	
		PC.9	MFP2	O	
UART11	UART11_RXD	PD.13	MFP2	I	UART11 data receiver input pin
		PM.12	MFP4	I	
		PI.0	MFP3	I	
		PL.2	MFP2	I	
		PC.12	MFP3	I	
		PF.6	MFP2	I	
	UART11_TXD	PD.12	MFP2	O	UART11 data transmitter output pin
		PM.13	MFP4	O	
		PI.1	MFP3	O	
		PL.3	MFP2	O	
		PC.13	MFP3	O	
		PF.7	MFP2	O	
	UART11_nCTS	PD.14	MFP2	I	UART11 clear to Send input pin
		PL.0	MFP2	I	
		PF.4	MFP2	I	
	UART11_nRTS	PD.15	MFP2	O	UART11 request to Send output pin
		PL.1	MFP2	O	
		PF.5	MFP2	O	
UART12	UART12_RXD	PI.2	MFP2	I	UART12 data receiver input pin
		PG.8	MFP2	I	
		PK.6	MFP2	I	
		PC.14	MFP2	I	
		PN.12	MFP3	I	

		PE.8	MFP3	I	
	UART12_TXD	PI.3	MFP2	O	UART12 data transmitter output pin
		PG.9	MFP2	O	
		PK.7	MFP2	O	
		PC.15	MFP2	O	
		PN.13	MFP3	O	
		PE.9	MFP3	O	
	UART12_nCTS	PI.0	MFP2	I	UART12 clear to Send input pin
		PK.4	MFP2	I	
		PC.12	MFP2	I	
	UART12_nRTS	PI.1	MFP2	O	UART12 request to Send output pin
		PG.10	MFP2	O	
		PK.5	MFP2	O	
		PC.13	MFP2	O	
UART13	UART13_RXD	PI.4	MFP3	I	UART13 data receiver input pin
		PL.8	MFP3	I	
		PK.4	MFP3	I	
		PH.12	MFP3	I	
		PK.12	MFP3	I	
		PF.8	MFP2	I	
	UART13_TXD	PI.5	MFP3	O	UART13 data transmitter output pin
		PL.9	MFP3	O	
		PG.10	MFP3	O	
		PK.5	MFP3	O	
		PH.13	MFP3	O	
		PK.13	MFP3	O	

		PF.9	MFP2	O	
	UART13_nCTS	PE.8	MFP2	I	UART13 clear to Send input pin
		PF.10	MFP2	I	
	UART13_nRTS	PE.9	MFP2	O	UART13 request to Send output pin
		PF.11	MFP2	O	
UART14	UART14_RXD	PL.12	MFP4	I	UART14 data receiver input pin
		PI.6	MFP2	I	
		PL.10	MFP2	I	
		PH.14	MFP2	I	
		PE.10	MFP3	I	
	UART14_TXD	PL.13	MFP4	O	UART14 data transmitter output pin
		PI.7	MFP2	O	
		PL.11	MFP2	O	
		PH.15	MFP2	O	
		PE.11	MFP3	O	
	UART14_nCTS	PI.4	MFP2	I	UART14 clear to Send input pin
		PL.8	MFP2	I	
		PH.12	MFP2	I	
	UART14_nRTS	PI.5	MFP2	O	UART14 request to Send output pin
		PL.9	MFP2	O	
		PH.13	MFP2	O	
UART15	UART15_RXD	PK.0	MFP3	I	UART15 data receiver input pin
		PD.8	MFP3	I	
		PE.12	MFP2	I	
	UART15_TXD	PK.1	MFP3	O	UART15 data transmitter output pin
		PD.9	MFP3	O	

		PE.13	MFP2	O	
	UART15_nCTS	PE.10	MFP2	I	UART15 clear to Send input pin
	UART15_nRTS	PE.11	MFP2	O	UART15 request to Send output pin
UART16	UART16_RXD	PA.0	MFP3	I	UART16 data receiver input pin
		PK.2	MFP2	I	
		PD.10	MFP2	I	
	UART16_TXD	PA.1	MFP3	O	UART16 data transmitter output pin
		PK.3	MFP2	O	
		PD.11	MFP2	O	
	UART16_nCTS	PK.0	MFP2	I	UART16 clear to Send input pin
		PD.8	MFP2	I	
	UART16_nRTS	PK.1	MFP2	O	UART16 request to Send output pin
		PD.9	MFP2	O	

Table 19-1 UART[0..16] Interfaces Pin List

Group	Pin Name	GPIO	MFP	Type	Description
SC0	SC0_CLK	PI.1	MFP7	O	Smart Card 0 clock pin
		PL.8	MFP9	O	
		PJ.0	MFP8	O	
		PK.12	MFP8	O	
		PF.6	MFP13	O	
		PF.10	MFP9	O	
	SC0_DAT	PI.2	MFP7	I/O	Smart Card 0 data pin
		PL.9	MFP9	I/O	
		PJ.1	MFP8	I/O	
		PK.5	MFP8	I/O	
		PK.13	MFP8	I/O	

		PF.7	MFP13	I/O	
		PF.11	MFP9	I/O	
	SC0_PWR	PK.2	MFP7	O	Smart Card 0 power pin
		PL.11	MFP9	O	
		PJ.3	MFP8	O	
		PK.7	MFP8	O	
		PK.15	MFP8	O	
		PF.9	MFP13	O	
		PF.13	MFP9	O	
	SC0_RST	PI.3	MFP7	O	Smart Card 0 reset pin
		PL.10	MFP9	O	
		PJ.2	MFP8	O	
		PK.6	MFP8	O	
		PK.14	MFP8	O	
		PF.8	MFP13	O	
		PF.12	MFP9	O	
	SC0_nCD	PI.0	MFP7	I	Smart Card 0 card detect pin
		PL.5	MFP9	I	
		PN.15	MFP8	I	
		PB.9	MFP13	I	
SC1	SC1_CLK	PL.12	MFP7	O	Smart Card 1 clock pin
		PG.4	MFP10	O	
		PJ.12	MFP7	O	
		PD.8	MFP10	O	
		PL.0	MFP9	O	
	SC1_DAT	PL.13	MFP7	I/O	Smart Card 1 data pin

		PG.5	MFP10	I/O	
		PJ.13	MFP7	I/O	
		PD.9	MFP10	I/O	
		PL.1	MFP9	I/O	
	SC1_PWR	PL.15	MFP7	O	Smart Card 1 power pin
		PG.7	MFP10	O	
		PJ.15	MFP7	O	
		PD.11	MFP10	O	
		PL.3	MFP9	O	
	SC1_RST	PL.14	MFP7	O	Smart Card 1 reset pin
		PG.6	MFP10	O	
		PJ.14	MFP7	O	
		PD.10	MFP10	O	
		PL.2	MFP9	O	
	SC1_nCD	PM.12	MFP7	I	Smart Card 1 card detect pin
		PK.3	MFP7	I	
		PD.7	MFP10	I	
		PL.4	MFP9	I	

Table 19-2 SMART Card0/1 Interfaces Pin List

19.2 Reference Connection

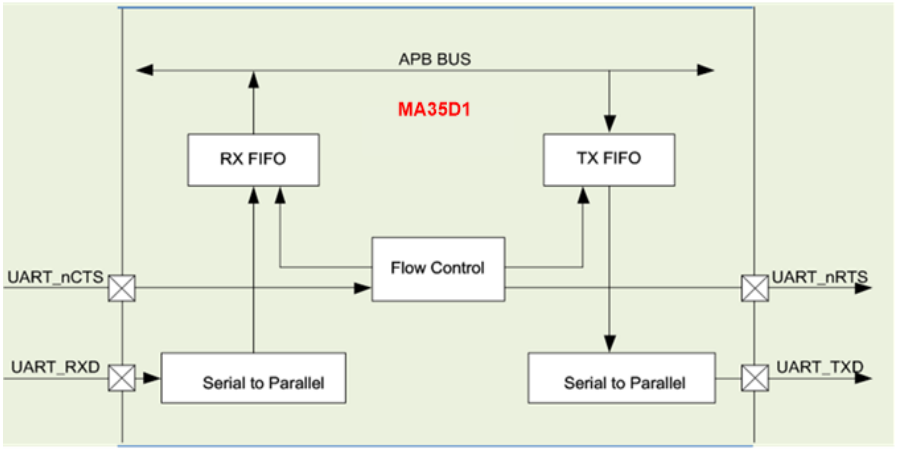


Figure 19-1 UART with Control Flow Block Diagram

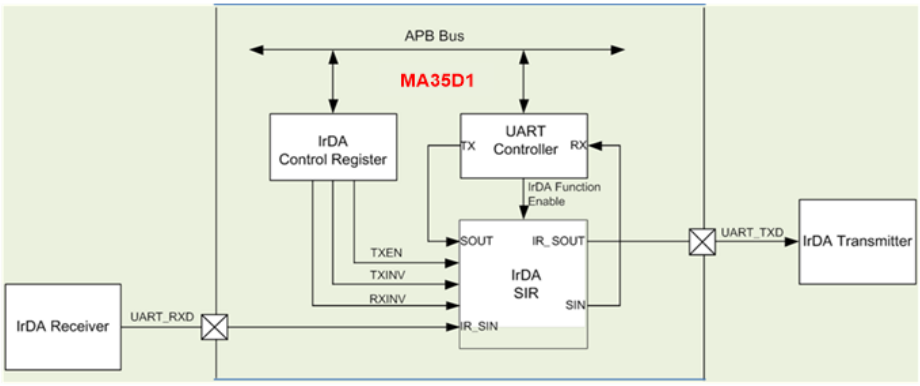


Figure 19-2 IrDA Control Block Diagram

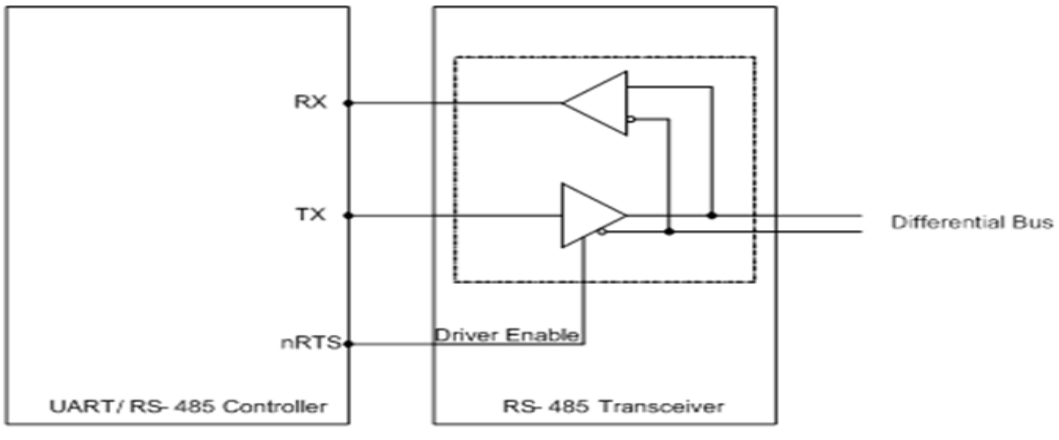


Figure 19-3 RS485 Mode Block Diagram

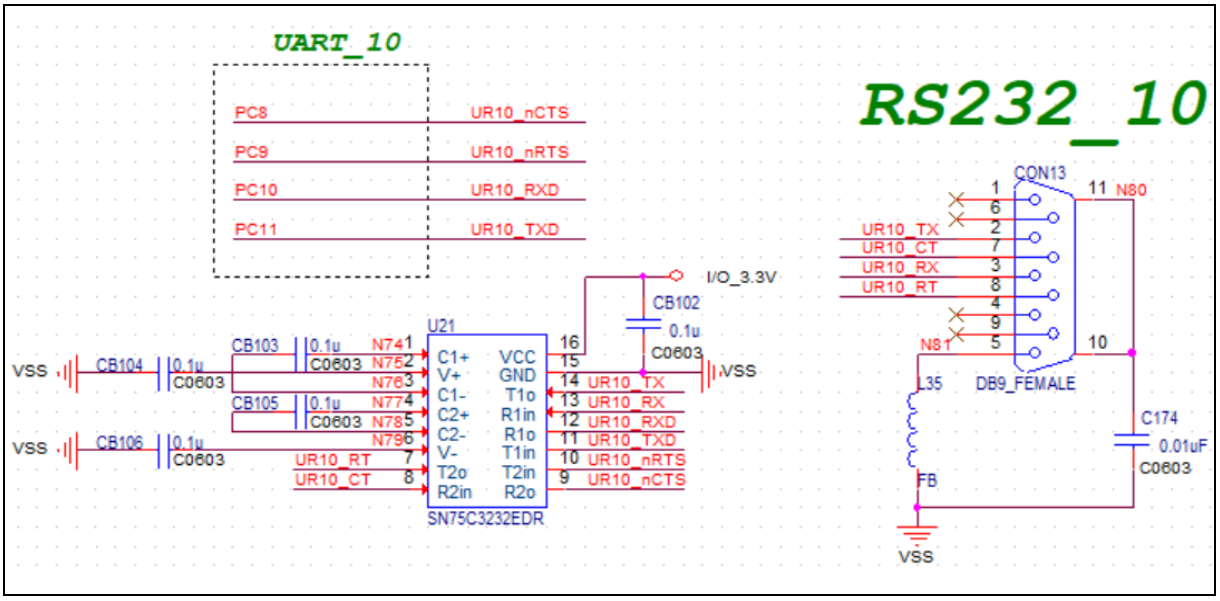


Figure 19-4 RS232 Connectivity with UART10

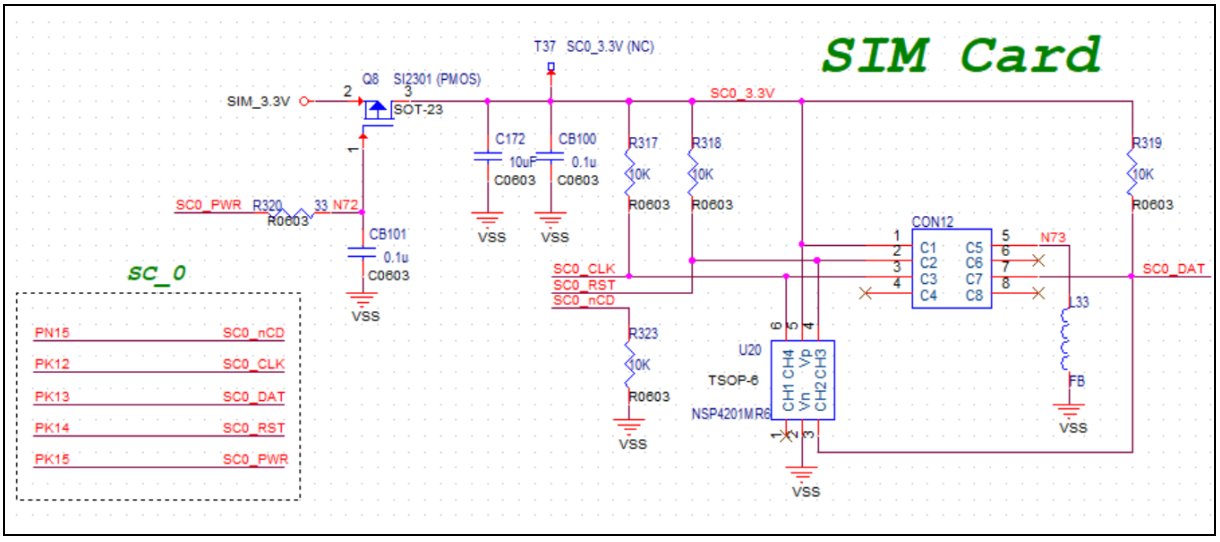


Figure 19-5 SMART Card Connectivity with SC1

20 LCD Display

The MA35D1 display provides an LCD Display controller with the resolution up to 1920x1080 at 60 FPS, parallel pixel output with 24-bit data, support i80/m68 with 8-,9-,16-,18-bit system interface. The controller includes support for parallel pixel output and is easily adapted to external serialization logic, for example HDMI, MIPI and LVDS transmitter.

20.1 Pin Configuration

Group	Pin Name	GPIO	MFP	Type	Description
LCM	LCM_CLK	PG.10	MFP6	O	TFT LCD Module Pixel Clock output pin in Sync-type mode
	LCM_DATA0/LCM_MPU_D0	PI.8	MFP6	I/O	TFT LCD Module Pixel Data output bit 0 in Sync-type mode TFT LCD Module Command/Data input/output bit 0 in MPU-type mode
	LCM_DATA1/LCM_MPU_D1	PI.9	MFP6	I/O	TFT LCD Module Pixel Data output bit 1 in Sync-type mode TFT LCD Module Command/Data input/output bit 1 in MPU-type mode
	LCM_DATA10/LCM_MPU_D10	PH.2	MFP6	I/O	TFT LCD Module Pixel Data output bit 10 in Sync-type mode TFT LCD Module Command/Data input/output bit 10 in MPU-type mode
	LCM_DATA11/LCM_MPU_D11	PH.3	MFP6	I/O	TFT LCD Module Pixel Data output bit 11 in Sync-type mode TFT LCD Module Command/Data input/output bit 11 in MPU-type mode
	LCM_DATA12/LCM_MPU_D12	PH.4	MFP6	I/O	TFT LCD Module Pixel Data output bit 12 in Sync-type mode TFT LCD Module Command/Data input/output bit 12 in MPU-type mode

	LCM_DATA13/LCM_MPU_D13	PH.5	MFP6	I/O	TFT LCD Module Pixel Data output bit 13 in Sync-type mode TFT LCD Module Command/Data input/output bit 13 in MPU-type mode
	LCM_DATA14/LCM_MPU_D14	PH.6	MFP6	I/O	TFT LCD Module Pixel Data output bit 14 in Sync-type mode TFT LCD Module Command/Data input/output bit 14 in MPU-type mode
	LCM_DATA15/LCM_MPU_D15	PH.7	MFP6	I/O	TFT LCD Module Pixel Data output bit 15 in Sync-type mode TFT LCD Module Command/Data input/output bit 15 in MPU-type mode
	LCM_DATA16/LCM_MPU_D16	PC.12	MFP6	I/O	TFT LCD Module Pixel Data output bit 16 in Sync-type mode TFT LCD Module Command/Data input/output bit 16 in MPU-type mode
	LCM_DATA17/LCM_MPU_D17	PC.13	MFP6	I/O	TFT LCD Module Pixel Data output bit 17 in Sync-type mode TFT LCD Module Command/Data input/output bit 17 in MPU-type mode
	LCM_DATA18	PC.14	MFP6	I/O	TFT LCD Module Pixel Data output bit 18 in Sync-type mode
	LCM_DATA19	PC.15	MFP6	I/O	TFT LCD Module Pixel Data output bit 19 in Sync-type mode
	LCM_DATA2/LCM_MPU_D2	PI.10	MFP6	I/O	TFT LCD Module Pixel Data output bit 2 in Sync-type mode TFT LCD Module Command/Data input/output bit 2 in MPU-type mode
	LCM_DATA20	PH.12	MFP6	I/O	TFT LCD Module Pixel Data output bit 20 in Sync-type mode

	LCM_DATA21	PH.13	MFP6	I/O	TFT LCD Module Pixel Data output bit 21 in Sync-type mode
	LCM_DATA22	PH.14	MFP6	I/O	TFT LCD Module Pixel Data output bit 22 in Sync-type mode
	LCM_DATA23	PH.15	MFP6	I/O	TFT LCD Module Pixel Data output bit 23 in Sync-type mode
	LCM_DATA3/LCM_MPU_D3	PI.11	MFP6	I/O	TFT LCD Module Pixel Data output bit 3 in Sync-type mode TFT LCD Module Command/Data input/output bit 3 in MPU-type mode
	LCM_DATA4/LCM_MPU_D4	PI.12	MFP6	I/O	TFT LCD Module Pixel Data output bit 4 in Sync-type mode TFT LCD Module Command/Data input/output bit 4 in MPU-type mode
	LCM_DATA5/LCM_MPU_D5	PI.13	MFP6	I/O	TFT LCD Module Pixel Data output bit 5 in Sync-type mode TFT LCD Module Command/Data input/output bit 5 in MPU-type mode
	LCM_DATA6/LCM_MPU_D6	PI.14	MFP6	I/O	TFT LCD Module Pixel Data output bit 6 in Sync-type mode TFT LCD Module Command/Data input/output bit 6 in MPU-type mode
	LCM_DATA7/LCM_MPU_D7	PI.15	MFP6	I/O	TFT LCD Module Pixel Data output bit 7 in Sync-type mode TFT LCD Module Command/Data input/output bit 7 in MPU-type mode
	LCM_DATA8/LCM_MPU_D8	PH.0	MFP6	I/O	TFT LCD Module Pixel Data output bit 8 in Sync-type mode TFT LCD Module Command/Data input/output bit 8 in MPU-type mode

	LCM_DATA9/LCM_MPU_D9	PH.1	MFP6	I/O	TFT LCD Module Pixel Data output bit 9 in Sync-type mode TFT LCD Module Command/Data input/output bit 9 in MPU-type mode
	LCM_DEN/LCM_MPU_RS	PK.4	MFP6	O	TFT LCD Module Data Enable/Display Control Signal output pin in Sync-type mode TFT LCD Module Register Select (RS) output pin in MPU-type mode
	LCM_HSYNC/LCM_MPU_WR/R/W	PG.9	MFP6	O	TFT LCD Module Horizontal/Line sync. output in Sync-type mode TFT LCD Module Write(WR)/ ReadWrite(R/W) output pin in MPU-type 80/68 mode
	LCM_MPU_TE	PC.15	MFP7	I	TFT LCD Module TE input pin in MPU-type mode
	LCM_MPU_VSYNC	PC.15	MFP8	O	TFT LCD Module VSYNC output pin in MPU-type mode
	LCM_VSYNC/LCM_MPU_RD/EN	PG.8	MFP6	O	TFT LCD Module Vertical/Frame sync. output pin in Sync-type mode TFT LCD Module Read(RD)/Enable(EN) output pin in MPU-type 80/68 mode

Table 20-1 LCD Display Interfaces Pin List

20.2 Reference Connection

Pin Name	LCM_DATA[0:23]	LCM_HSYNC	LCM_VSYNC	LCM_DEN	LCM_CLK	LCM_MPU_VSYNC	LCM_MPU_CS
GPIO	PI.[8:15], PH.[0:7], PC.[12:15], PH.[12:15]	PG.9	PG.8	PK.4	PG.10	PC.15	PC.14
Sync. Mode	DATA[0:23]	HSYNC	VSYNC	DE	CLK_O	x	x
MPU80	DATA[0:17]	WR	RD	RS	x	x	CS
MPU80+VSYNC	DATA[0:17]	WR	RD	RS	x	VSYNC_O	CS
MPU80+TE	DATA[0:17]	WR	RD	RS	x	TE_I	CS
MPU86	DATA[0:17]	R/W	EN	RS	x	x	CS

MPU68+VS$_{YNC}$	DATA[0:17]	R/W	EN	RS	x	VS$_{YNC}$_O	CS
MPU68+TE	DATA[0:17]	R/W	EN	RS	x	TE_I	CS

Table 20-2 Sync/MPU Interface

Formats	D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DPI 24-bit	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
DPI 18-bit 1	x	x	x	x	x	x	R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
DPI 18-bit 2	x	x	R5	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	B5	B4	B3	B2	B1	B0
DPI 16-bit 1	x	x	x	x	x	x	x	x	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B4	B3	B2	B1	B0
DPI 16-bit 2	x	x	x	R4	R3	R2	R1	R0	x	x	G5	G4	G3	G2	G1	G0	x	x	x	B4	B3	B2	B1	B0
DPI 16-bit 3	x	x	R4	R3	R2	R1	R0	x	x	x	G5	G4	G3	G2	G1	G0	x	x	B4	B3	B2	B1	B0	x

Table 20-3 Data Input Formats

20.3 PCB Layout Considerations

20.3.1 Connect Parallel RGB LCD

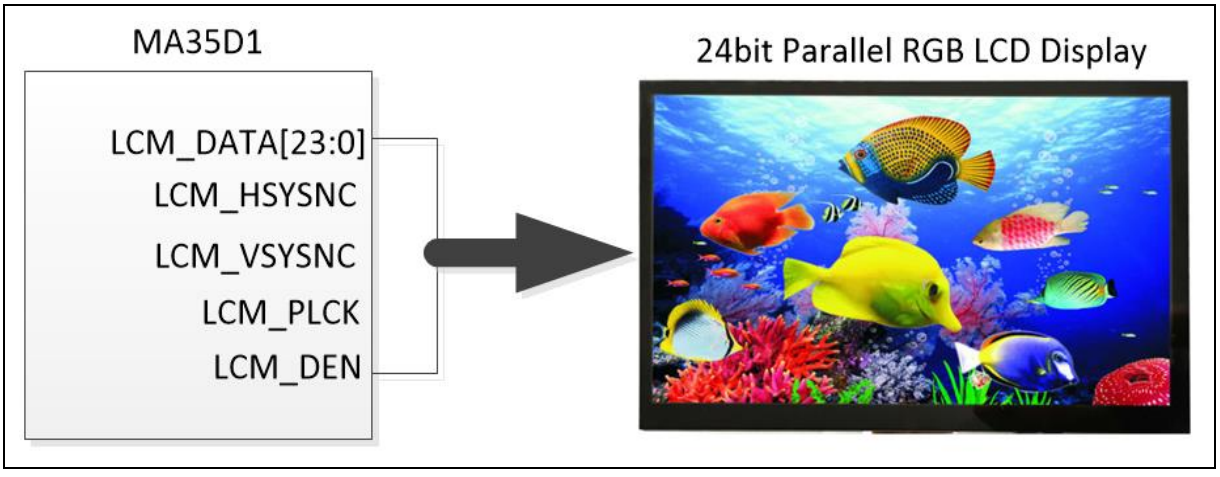


Figure 20-1 Connect Parallel RGB LCD

PCB layout recommendation for parallel RGB LCD

- The layout requirements depend on the pixel clock and therefore on the required display resolution.
- Use a trace impedance of 50 Ω.

- Max skew between data signals <100ps≒15 mm, but the requirement may be relaxed for lower resolutions.
- Max trace length <100 mm, long distances only recommended for low resolution displays.
- It is common to have EMC problems with parallel RGB interface due to the flat flex cables, so they should be kept as short as possible.
- Series resistors on the bus lines are recommended to reduce slew rate and control EMC emissions.
- The requirements can be greatly relaxed if lower resolutions such as VGA 640x480 are used. The maximum length restrictions are defined due to electromagnetic radiation problems associated with the parallel interface.
- From the timing perspective, the trace length of the interface is not limited.

20.3.2 Connect LVDS Transmitter to LVDS LCD

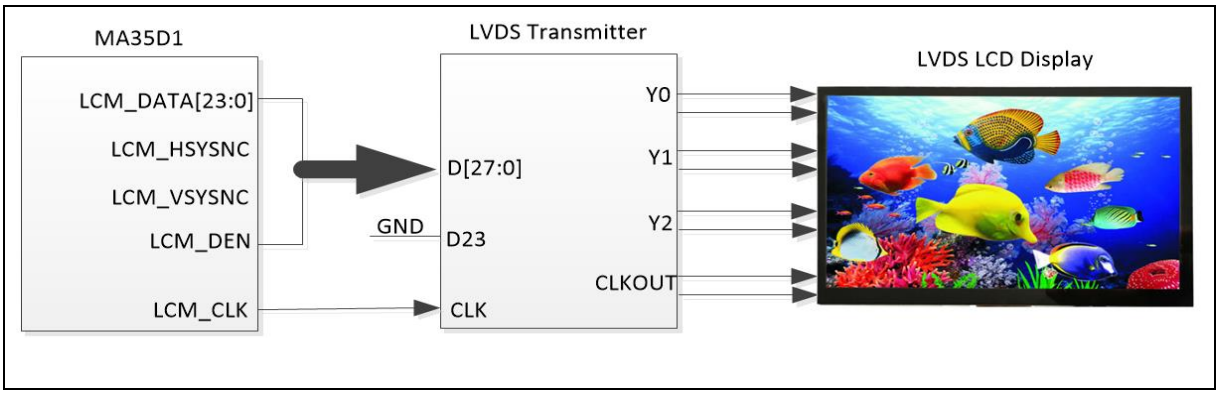


Figure 20-2 Connect LVDS LCD

PCB layout recommendation for LVDS LCD

- The distance between two adjacent LVDS pairs should be greater than or equal to twice the distance between the two individual conductors of a single LVDS pair.
- Maintain equal length on signal traces within a differential pair, Max intra-pair skew <1ps≒150 um.
- Avoid serpentine one side of the differential pair to match skew.
- Max trace length on carrier board and display cable <500 mm,
- Trace impedance 100 Ω for differential signal, 50 Ω for single ended signal.
- Max trace length skew between clock and data pairs <3.5ps≒500 um, depending on LVDS frequency since clock is not embedded, can be relaxed for lower resolutions.
- Do not route high-speed LVDS traces near the edge of the PCB.

20.3.3 Connect MIPI Transmitter to MIPI LCD

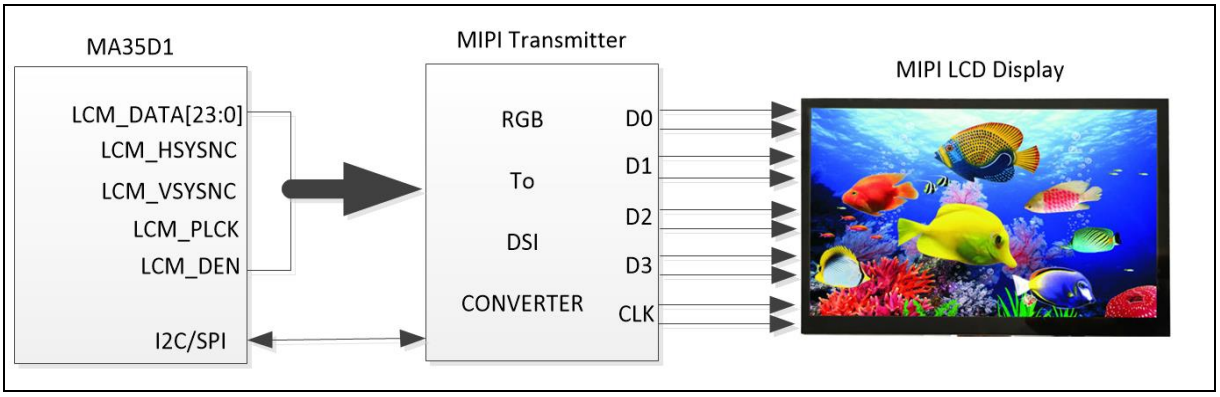


Figure 20-3 Connect MIPI LCD

- PCB layout recommendation for MIPI LCD
- Keep away from other high-speed signals.
- Keep lengths to within 5 mils of each other.
- Trace impedance 100 Ω for differential signal, 50 Ω for single ended signal.
- Maintain equal length on signal traces within a differential pair, Max intra-pair skew <1ps≒150 um.
- Max trace length skew between clock and data lanes <10ps≒1.5 mm.
- Each pair should be separated at least by three times the signal trace width.
- Route all differential pairs on the same layer.
- The number of VIAS should be kept to a minimum. Keeping the VIAS count to two or less is recommended.
- The maximum trace length over FR4 between the MA35D1 and the MIPI Transmitter is 25–30 cm.
- The maximum trace length over FR4 between MIPI Transmitter and the LCD Display is 4 inches for data rates ≤ HBR (2.7 Gbps) and 2 inches for HBR2 (5.4 Gbps).

20.3.4 Connect HDMI Transmitter to HDMI LCD

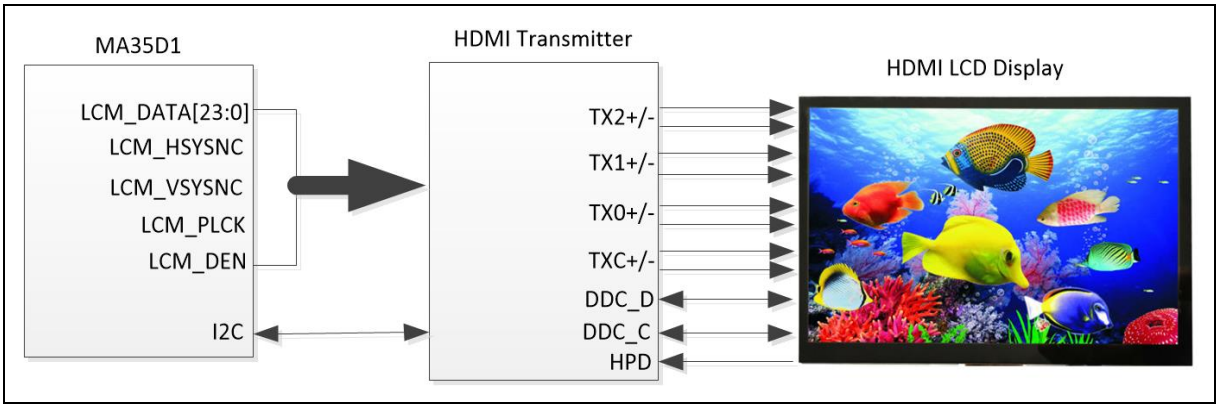


Figure 20-4 Connect HDMI LCD

PCB layout recommendation for HDMI LCD

- Keep away from other high-speed signals.
- Trace impedance 100 Ω for differential signal, 50 Ω for single ended signal.
- Maintain equal length on signal traces within a differential pair, Max intra-pair skew <5ps≒750 um.
- Max trace length skew between clock and data lanes <150ps≒22 mm.
- Max trace length on carrier board and <250 mm.
- Minimum pair to pair spacing >500 um.
- Signal within a pair shall not have any 90° corners shall be chamfered.
- Route all differential pairs on the same layer.

21 External DDR3/DDR3L

This application note gives guidance on how to implement a DDR3 and DDR3L memory interface on the MA35D1 BGA364 package chip. It provides interface schematics and layout implementation rules.

The MA35D1 memory interface can address DDR3 and DDR3L with a data rate speed at 1066 Mbps, MV_{DD} voltage at 1.5V for DDR3 and 1.35V for DDR3L. More information on DDR3 SDRAM can be found on JEDEC DDR3 SDRAM Standard JESD79-3F.

There are challenges in designing a DDR interface due to continuous board-size reductions, which can impose performance limitations on the interface.

In addition, because the DDR connections on both the MA35D1 and memory device interface are fixed, there is very limited flexibility possible in terms of physical layout.

Basic design rules regarding trace isolation, length equalization, power distribution and decoupling and impedance matching, must be respected to ensure correct signal and power integrity.

This document lists the rules that must be applied to implement a DDR3/DDR3L memory interface in 8-layer PCBs.

21.1 DDR3/DDR3L Schematic Implementation

A DDR implementation should be comprised of the following elements.

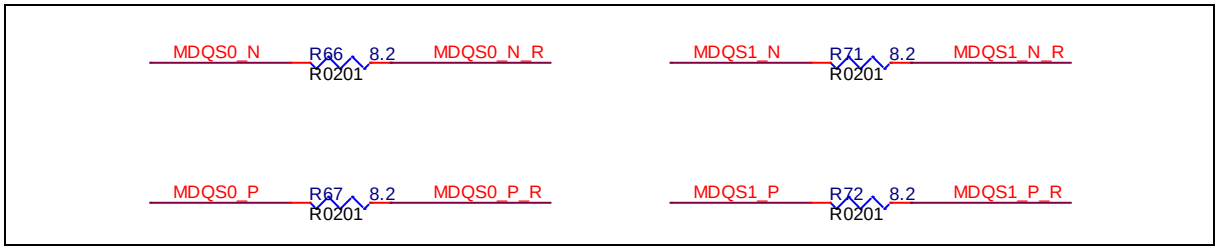
21.1.1 Two DDR3/DDR3L Chips Topology

This topology can be used when there are two DDR chips. It is comprised of:

- A/C bus includes address, command, control and clock signals.
  - A/C bus with on-board termination 56 Ω at VTT (MVDD/2), if required.
  - 33 Ω serial resistors are recommended for every A/C of the DDR chip, to reduce reflection, if required.
  - A differential clock: implement a differential termination of the MCK_N/MCK_P signals using one resistor 100 Ω.
- Data bus includes:
  - 16 data signal bits (MD[15..0])
  - 2 data mask signals (MDMask[1..0])
  - 2 pair differential clocks (MDQS[1..0]_N/MDQS[1..0]_P)
- Series resistance on MDQS0_N/ MDQS0_P and MDQS1_N/ MDQS1_P
  - In some layout case, the glitch amplitude of MDQSx_N/ MDQSx_P may become large and cause a false read. In this case, the implementation of series

resistance on the MDQSx_N/ MDQSx_P should be considered. Place near the ball of MA35, these can be used to significantly reduce the amplitude of glitch.

A typical value for these resistors would be 8.2Ω.



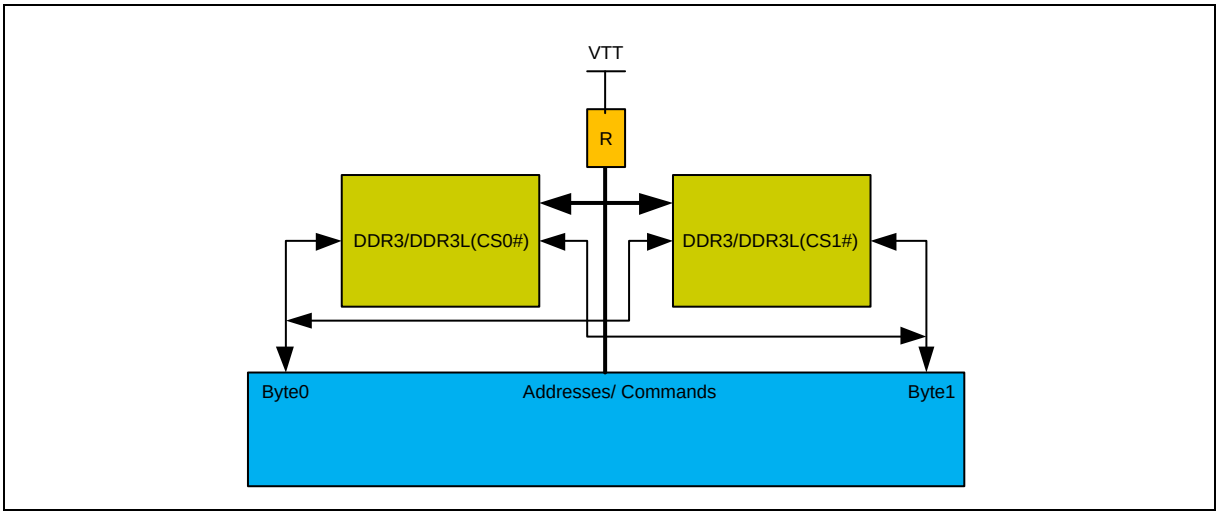


Figure 21-1 Two 16-bit DDR3/3L Connection with Termination

21.1.2 One DDR3/DDR3L Chips Topology

This topology can be used when there is a single DDR chip interface. It is comprised of:

- A/C bus includes address, command, control and clock signals.
  - A/C bus with on-board termination 56 Ω at VTT (MVDD/2), if required.
  - 33 Ω serial resistors are recommended for every A/C of the DDR chip, to reduce reflection, if required.
  - A differential clock: implement a differential termination of the MCK_N/MCK_P signals using one resistor 100 Ω.
- Data bus includes:
  - 16 data signal bits (MD[15..0])
  - 2 data mask signals (MDMask[1..0])
  - 2 pair differential clocks (MDQS[1..0]_N/MDQS[1..0]_P)

- Series resistance on MDQS0_N/ MDQS0_P and MDQS1_N/ MDQS1_P
  - In some layout case, the glitch amplitude of MDQSx_N/ MDQSx_P may become large and cause a false read. In this case, the implementation of series resistance on the MDQSx_N/ MDQSx_P should be considered. Place near the ball of MA35, these can be used to significantly reduce the amplitude of glitch.

    A typical value for these resistors would be 8.2Ω.

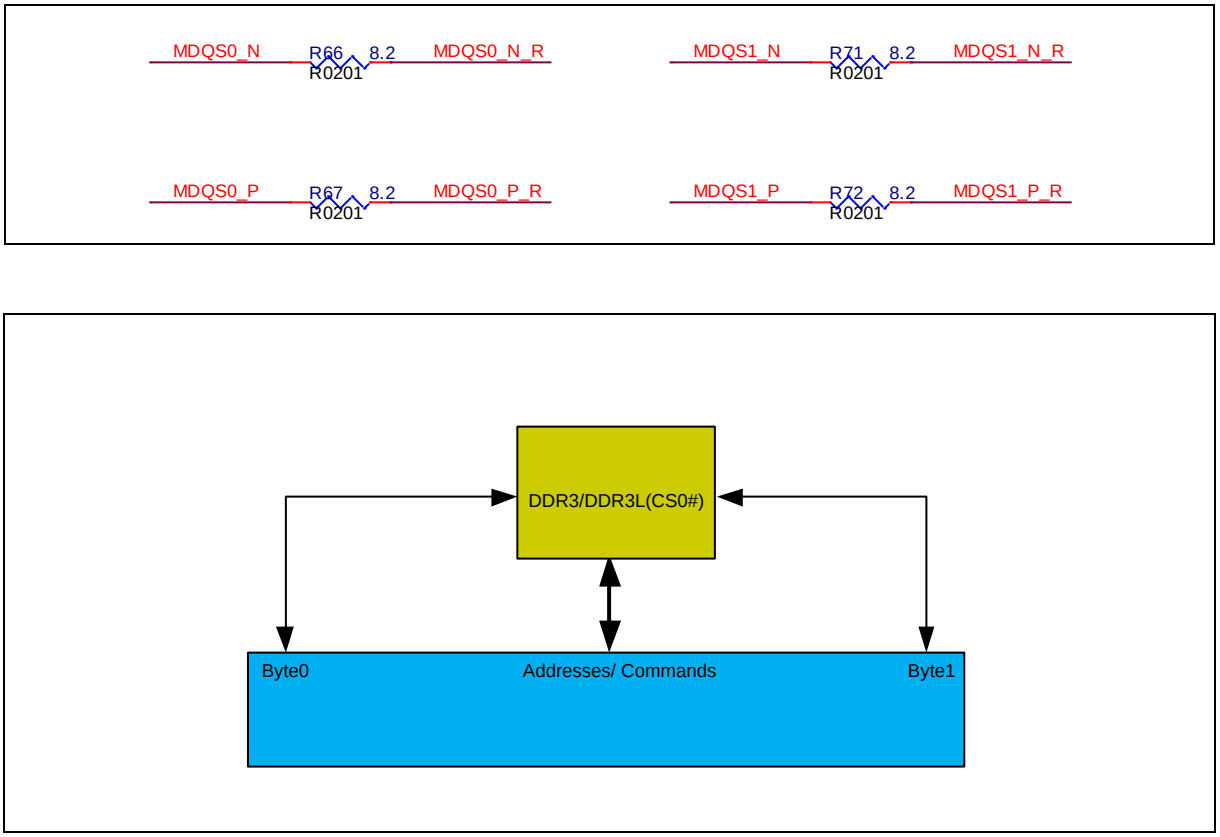


Figure 21-2 16-bit DDR3/3L Connection

21.1.3 Control Signals

In addition, the following signals should be included in the schematic:

- DDR_RESETN:
  - DDR_RESETN is an asynchronous low speed reset signal from DDR controller to DDR devices. The signal is driven low during the power-on or when a reset is required. Otherwise, the signal should be driven high by default.
- ZQ:

- This signal requires, for DDR impedance calibration, that resistors are placed between the signal balls and ground as follows:
  - A 240 Ω (±1%) resistor must be placed between the ZQ ball on each DDR chip and the GND plane.
  - A 240 Ω (±1%) resistor must also be placed between the MZQ_DDRPHY ball of MA35D1 and the GND plane.

- MCKE:
  - MCKE enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM.
  - A 10 kΩ pull-down resistor is required.

21.1.4 Power Supply and Reference Voltages

The following power supply and reference voltage components must be provided:

- V_{REF} reference voltage (equal to $MV_{DD}/2$) is the reference voltage required by MA35D1 and DDR3/3L devices, in order to properly sample Address/Command, Control and data signals.
- Its noise level must remain very low, as described in the JEDEC standard.
- Independent V_{REF} generators ($MV_{REF}CA$, $MV_{REF}DQ$) for each device. Each V_{REF} generator is based on a 2 kΩ (±1%) resistance bridge from MV_{DD} plus a local 100nF decoupling capacitor. The reference voltage, V_{REF}, should be generated as close as possible to its corresponding ball.
- MV_{DD} power plane this is the DDR interface power supply, equal to 1.5V (1.425V-1.575V) for DDR3 or 1.35V (1.283V-1.45V) for DDR3L. This plane requires mandatory decoupling capacitors relative to the GND plane with bulk capacitors and HF (high frequency) capacitors close to each of the power supply pins for DDR and MA35D1.

21.2 PCB Design Considerations

The basic PCB design considerations to take into account are detailed in the following sections.

21.2.1 Trace Isolation Distance

A minimum isolation distance must be provided around every trace, to reduce crosstalk, glitches and jitter caused by neighboring traces.

H definition

H is the distance to its reference plane (L1 to L2, L3 to L2, L6 to L7 and L8 to L7), so H of L1/L8 signals is 3.5mil, L3/L6 signal is 5mil. Figure 21-3 shows this example.

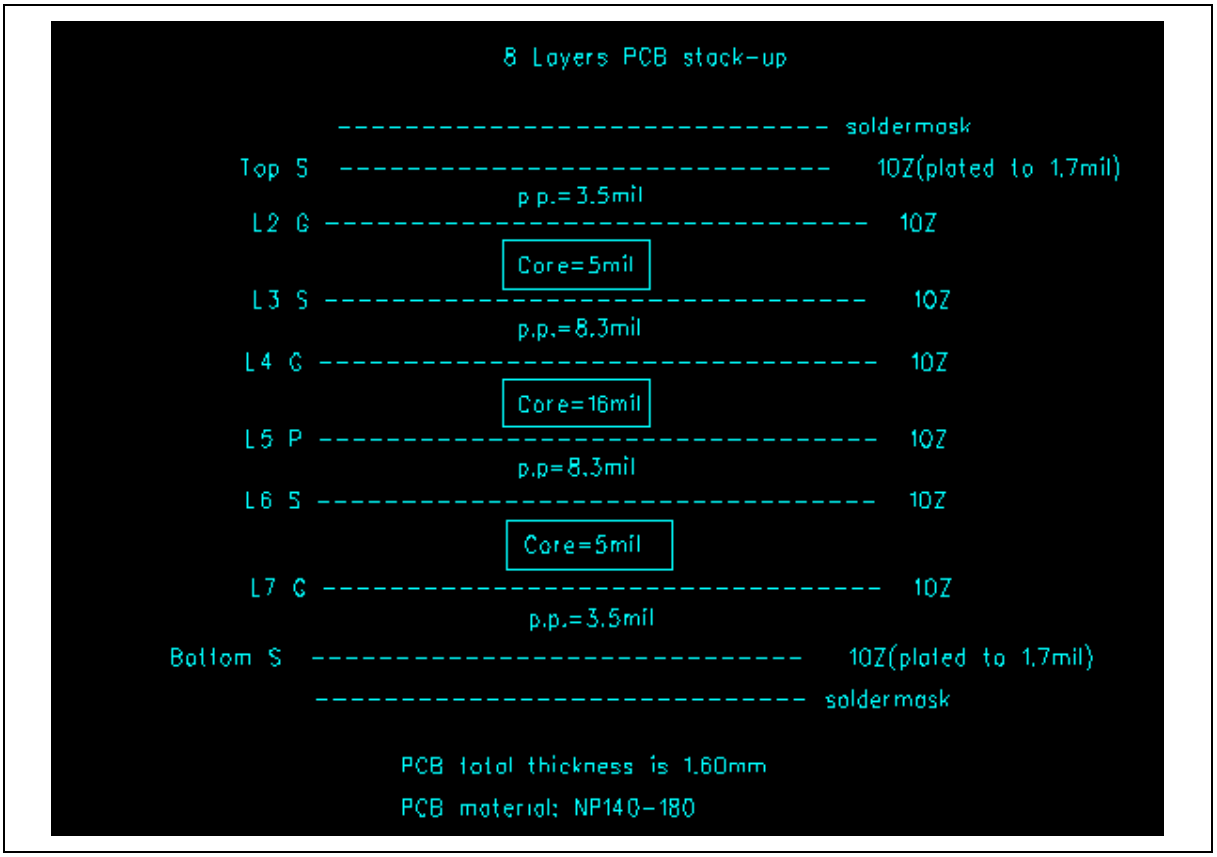


Figure 21-3 H Distance

2H-3H isolation rule

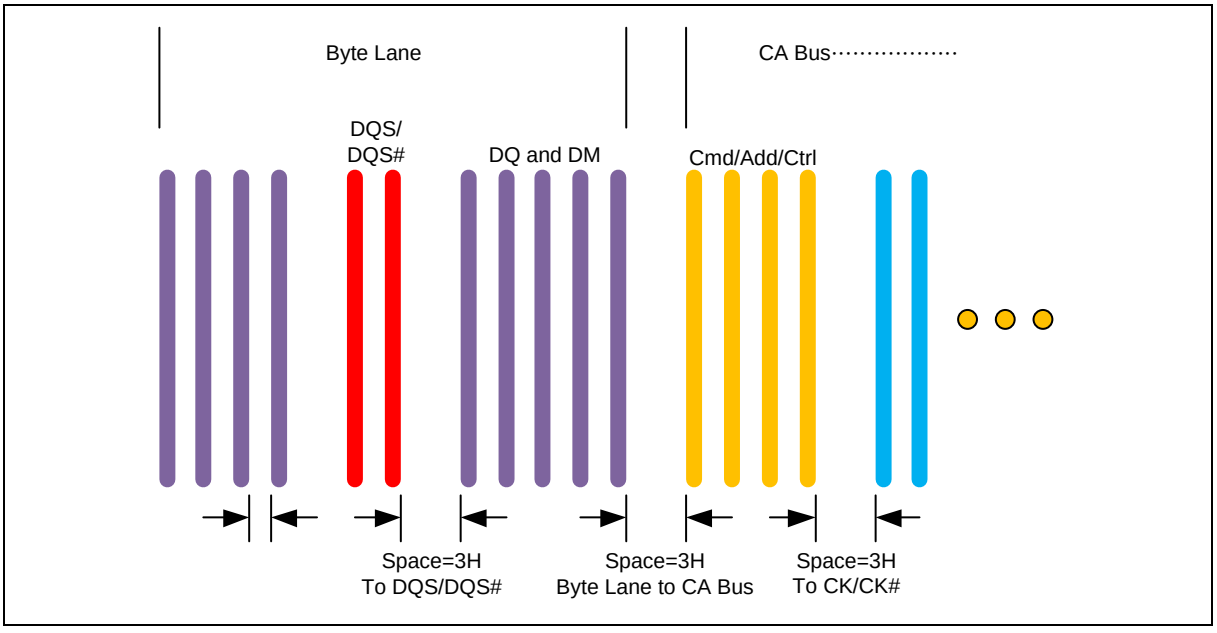


Figure 21-4 Spacing between Different Signal Groups (Relative to height from reference plane)

- Recommendation for trace spacing is:
  - 2 times the distance to the reference plane, for signals within the same group (2H)
  - 3 times the distance to the reference plane, for signals of different groups (3H)
  - The signal spacing between DQ and DQS within a byte should also be >=3H
  - The signal spacing between CA and CK should also be >=3H

21.2.2 Length Equalization

Signals of the same group must have matched setup and hold timings when they arrive at their destination. Due to this, trace length equalization may be required, so that these timing constraints are met.

The whole signal path must be considered (from MA35D1 to memory chip), taking into account the package and PCB lengths.

21.2.3 Impedance

Board impedance must be controlled to guarantee proper transmission line setup, in accordance with trace geometry (width and spacing) and the stack-up of the board.

For DDR3/3L interfaces, Nuvoton recommends the following impedances:

- For single-ended signals: 50 Ω ± 10%.
- For differential signals: differential 100 Ω ± 10%

21.2.4 Layer Allocation for 8-layer Boards

Layers must be allocated and implemented as detailed below, without exception:

- Top layer:
  - This layer is dedicated to those traces with the highest sensitivity.
  - The traces are referenced to the unified, internal ground (GND) plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2,4,7 (GND internal layer):
  - This is the unified internal ground plane.
  - It must be connected by a matrix of via to the top and bottom GND areas.
- Layer 5 (MV_{DD} for DDR3/3L internal layer):
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Layer 3

- This is a second signal layer used for traces.

- Layer 6
  - This is a third signal layer used for traces.
- Bottom layer:
  - This is a fourth signal layer used for traces.

21.2.5 MV_{DD} Power Plane Specification

In normal practice, A/C bus signals are laid out on the L6, L8 layer of the 8-layer PCB.

The L5 layer must be a unified MV_{DD} power plane, which fully overlaps the memory L6 layer signals, to avoid any impedance breaks due to traces referenced to multiple power planes.

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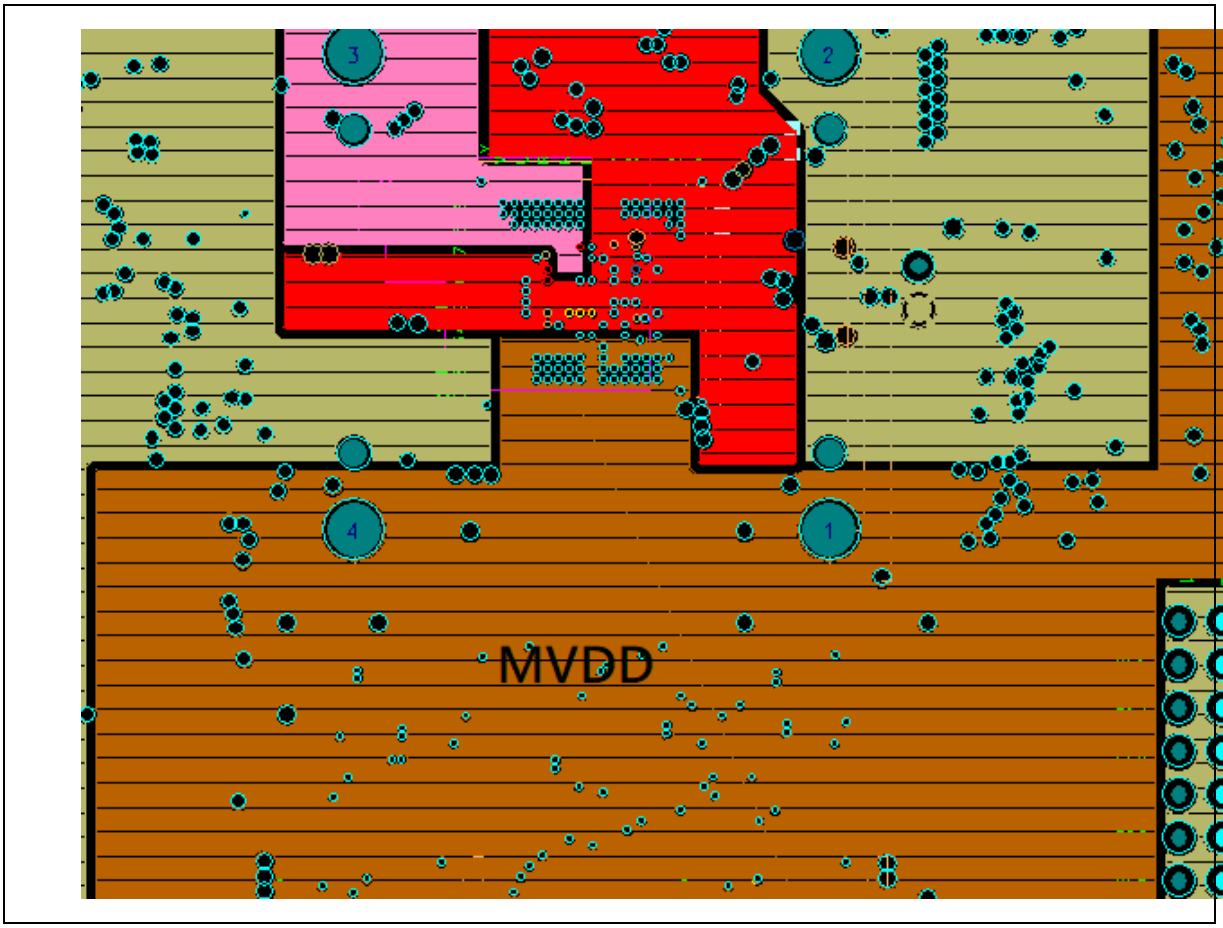

Figure 21-5 Layer L5 MV_{DD} Power Plane

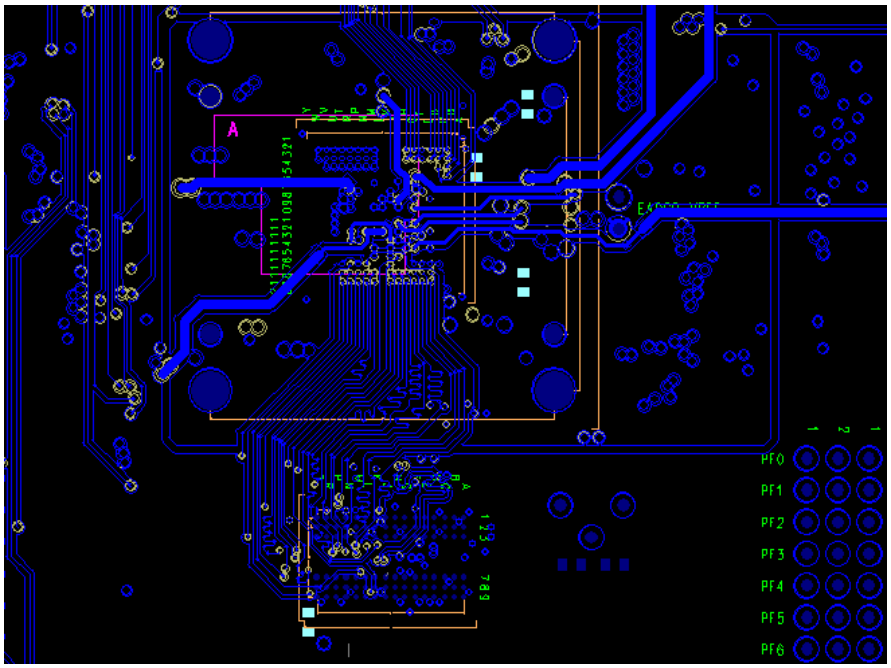

Figure 21-6 Layer L6 Signal Plane

21.2.6 Types of Decoupling Capacitors

Power integrity is essential for avoiding voltage drops and by consequence, eye closure and erroneous data transmission.

Core and sensitive power supplies (like MV_{DD}) must be laid out using internal power planes, and using maximum width, to minimize distribution impedance.

In addition to this, decoupling capacitors are required. There are two types:

- Bulk capacitors:
  - These capacitors provide an on-board energy tank for low-frequency, high-current needs. Capacitance values can range from 10µF to 100µF. You should refer to Nuvoton reference design to choose a capacitor value appropriate for your power supply. Bulk capacitors do not need to be placed very close to their destination.
- HF capacitors:
  - HF (high frequency) capacitors provide a local energy tank for high-frequency current bursts. HF capacitors must be placed as close as possible to the destination (power pins or balls). It is better practice to implement fewer capacitors, but placed in optimum position, to reduce connection inductance.

21.2.7 Minimizing Connection Inductance with HF Capacitors of Decoupling Capacitors

Decoupling capacitor placement must ensure minimum connection inductance.

The closer the capacitor is to its destination, the more efficient it is. This is particularly true for HF capacitors.

Another factor is whether the capacitor is place on the top or bottom layer.

Putting capacitors on the top layer can provide far better decoupling efficiency than placement on the bottom layer.

However, the choice of where capacitors are located can be constrained by BGA fan-out.

For this reason, look at best practices for capacitor placement to minimize connection inductance and improve decoupling efficiency, for both top and bottom layers.

21.2.8 Placing Capacitors on the Top Layer

Capacitors placed on the top layer of PCBs cannot be very close to BGA balls, due to package constraints.

However, if a capacitor is connected by a direct top-layer power trace to the BGA ball, its connection inductance remains smaller than if the capacitor is located much closer, but on the bottom layer, due to the GND layer position in the stack-up (the GND is the return current layer).

The amount of connection inductance that results is directly linked to the area of the current loop.

Therefore, top layer placement offers:

- When possible, try to place an HF capacitor on the top layer, with a top-layer direct power connection. The layer 2 (GND) provides a close return path, which results in a small current loop area and optimal decoupling efficiency.

21.2.9 Placing Capacitors on the Bottom Layer

When top-layer decoupling is not possible, placement of capacitors must be on the bottom layer.

While the connection inductance is higher than for top-layer capacitor placement, due to the bigger current loop area, bottom layer placement remains most of the time the only decoupling option for main BGA. Some basic implementation rules are allowed for an optimization of this placement. For best results, place the capacitor right below the BGA balls.

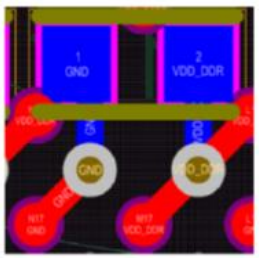

Figure 21-7 HF Capacitor on Bottom Layer

Place the HF capacitors on the bottom layer and connect to the BGA through the via, as Figure 21-7.

21.3 DDR3 PCB Layout Guide

There are 6 DDR3/DDR3L signal groups.

Group	Signal Name	Description
Clock	CK,CK#	Differential clock input to DRAM.
Data	DQ	DQ: Data input/output.
	DQS/DQS#	DQS,DQS#:DataStrobe.Differential.ForDRAM,theyareinputwhenwrite, andoutputwhenread.
	DM	DM: Data Mask: Input. DM is an input mask signal for write data.
Address/ Command	Address	A0 – An: Address inputs.
	Bank Address	BA0 –BA2: Bank address inputs.
	RAS# CAS# WE#	RAS#, CAS#, WE#: Command inputs. The RAS#, CAS#, WE# and CS# define the command being entered.
Control	CKE	CKE: Clock enable. Input.
	CS#	CS#: Chip select. Input.
	ODT	ODT:On Die Termination Enable. Input. When sampled HIGH, internal resistor termination is enabled. This ODT pin function can be ignored via Mode Register.
	RESET#	RESET#: Reset. Input.
Reference voltage	VREF_CA	VREF_CA: Reference voltage for control, command and address inputs
	VREF_DQ	VREF_DQ: Reference voltage for data group.
Power/ Ground	VDDQ/VSSQ	V_{DDQ}/V_{SSQ}: Power supply/ Ground for output drivers
	VDD/VSS	V_{DD}/V_{SS}: Power supply/ Ground for input buffers and chip internal circuits.

21.3.1 General Layout Rules

Equal trace length rule:

- Outer trace (Microstrip) and inner trace (Stripline) have different propagation delay.
- In general, 1.1 inch Microstrip has same delay as 1.0 inch Stripline.

Equal number of via

Equal trace width

At same layer location

21.3.2 Data Group Layout Rules

Bi-directional, speed = x2 clock rate. Most critical group.

Byte lane match. Each byte includes:

- Byte0=MD[7:0], MDMask0, MDQS0_P and MDQS0_N
- Byte1=MD[15:8], MDMask1, MDQS1_P and MDQS1_N

All signals in each byte must match in:

- Length
- Number of via
- Substrate layer location

Via compensation is required if the via count varies within the byte lane. Via equivalent length = 2.5 mm microstrip.

Inter-byte length matching as best as possible.

Enough edge-to-edge trace separation to reduce crosstalk. MDMaskn can be used to separate MD and MDQSn_P/MDQSn_N because MDMaskn is static during READ.

Trace impedance Z0 as close as possible to single end 50ohm, reference to ground plane is recommended.

Inner layer layout preferred to reduce EMI

Length equalization rules:

- Length difference of MD[15:0], MDMask[1:0] to MDQS[1:0]_P/MDQS[1:0]_N is within 60 mils

Recommended layer location: layer1, 3

21.3.3 Clock Group Layout Rules

MCK_P, MCK_N: differential pair.

- The MCK_P/MCK_N signals are terminated differentially, by one 100 Ω resistor.

MCK_P, MCK_N must match in:

- Length
- Number of via
- Substrate layer location

Enable "differential nets" routing in layout tool.

Trace impedance Z0 as close as possible to differential 100ohm, reference to ground plane.

21.3.4 Address/Command Group Layout Rules

Input only, speed = x1 clock rate.

All signals in each byte must match in:

- Length
- Number of via
- Substrate layer location

Length matching to Clock group

Enough edge-to-edge trace separation to reduce crosstalk.

Trace impedance Z0 as close as possible to single end 50ohm, reference to ground plane is recommended.

There are following signals are included in this group:

- MA[15:0], MBA[2:0], MRASn, MCASn, MWEn

21.3.5 Control Group Layout Rules

Input only, low speed signal

All signals in this group must match in:

- Length
- Number of via
- Substrate layer location

Length matching to Clock group

Enough edge-to-edge trace separation to reduce crosstalk.

Trace impedance Z0 as close as possible to single end 50ohm, reference to ground plane is recommended.

There are following signals are included in this group:

- MCS[1:0]n, MCKE[1:0], MODT[1:0], MRESETn

Length equalization rules:

- Length difference of MA[15:0], MBA[2:0], MRASn, MCASn, MWEn, MCS[1:0]n, MCKE[1:0], MODT[1:0] to CLK_P, CLK_N is within 140 mils

- CLK_P/CLK_N maximum length is 4.72 inch (12 cm)

Recommended layer location: layer6, 8

21.3.6 Length Difference Between Groups

Length of MDQS[1:0]_P/MDQS[1:0]_N must be from 0 to 520 mils shorter than CLK_P/CLK_N. CLK_P/CLK_N must be the longest traces.

21.3.7 Skew Control

How tightly skew needs to be controlled on the PCB, depends on the maximum operating frequency. Table 21.1 lists skew recommendations for double data rate and single data rate domains for various operating frequencies. Recommended PCB skew for CK to DQS timing for different bit stripline cases. Assumptions are 151 ps./inch for top layer microstrip and 179 ps./inch for stripline.

These values are selected in order to minimize the impact on the timing budget.

For example, at 1066Mbps operating frequency, we select @1600Mbps column

- Length difference of MD[15:0], MDMask[1:0] to MDQS[1:0]_P/MDQS[1:0]_N is within 60 mils
- Length difference of MA[15:0], MBA[2:0], MRASn, MCASn, MWEn, MCS[1:0]n, MCKE[1:0], MODT[1:0] to CLK_P, CLK_N is within 140 mils
- Length of MDQS[1:0]_P/MDQS[1:0]_N must be from 0 to 520 mils shorter than CLK_P/CLK_N. CLK_P/CLK_N must be the longest traces.

Skew Control Recommendations for DDR Interfaces.					
	Bit Rate	@ 800 Mbps	@ 1600 Mbps	@ 2133 Mbps	@ 2400 Mbps
DQ to DQS Domain	Skew in ps.	25	10	10	10
	Skew in Inches of Microstrip	0.17	0.07	0.07	0.07
	Skew in Inches of Stripline	0.14	0.06	0.06	0.06
Addr/Cmd to CK/CK# Domain	Skew in ps.	50	25	20	15
	Skew in Inches of Microstrip	0.33	0.17	0.14	0.11
	Skew in Inches of Stripline	0.28	0.14	0.11	0.08
DQS to CK	Skew in ps.	188	94	80	71
	Skew in Inches of Microstrip	1.25	0.63	0.54	0.48
	Skew in Inches of Stripline	1.04	0.52	0.44	0.39

Table 21.1 Recommended Skew Budgets

21.3.8 Reference Voltage

Resistor divider: This signal should be laid out so that the trace from the ball to the reference resistor is as short as possible. Ensure good isolation from any noisy aggressor signals.

VREFCA: Minimum 1 of 0.1uF decoupling capacitor to VDD per DRAM. Should be placed as close as possible to the DRAM ball.

VREFDQ: Minimum 1 of 0.1uF decoupling capacitor to VSSQ per DRAM. Should be placed as close as possible to the DRAM ball.

The following signals are included in this group:

- V_{REF}_CA, V_{REF}_DQ

21.3.9 $MV_{DD}/V_{DD}/V_{DDQ}$ Power Plane

Decoupling capacitor placement:

V_{DD}/V_{DDQ}: Minimum 3 of 0.1uF decoupling capacitors to GND per DRAM; should be placed as close as possible to the DRAM ball.

Dedicated layer for power, ground plane, no split or slot.

- It should be a unified power plane at layer 5, ground plane at layer 4.
- This power plane must overlap every DDR3/3L trace on the bottom layer, to avoid impedance discontinuities.
- The MV_{DD} power plane's connection to the MV_{DD} power supply, to the MA35D1 and to each memory device must be done by multiple via.
- Standard decoupling rules must be applied:
  - Bulk capacitors must be placed between the voltage regulator and the MA35D1 and memory devices.
  - HF decoupling capacitors must be placed as close as possible to each of the power pins. The low-connection-induction recommendations are outlined in section 21.2.7

22 ESD Protection Circuit Example for GPIO

IEC 61000-4-2 ESD Pulse Waveform

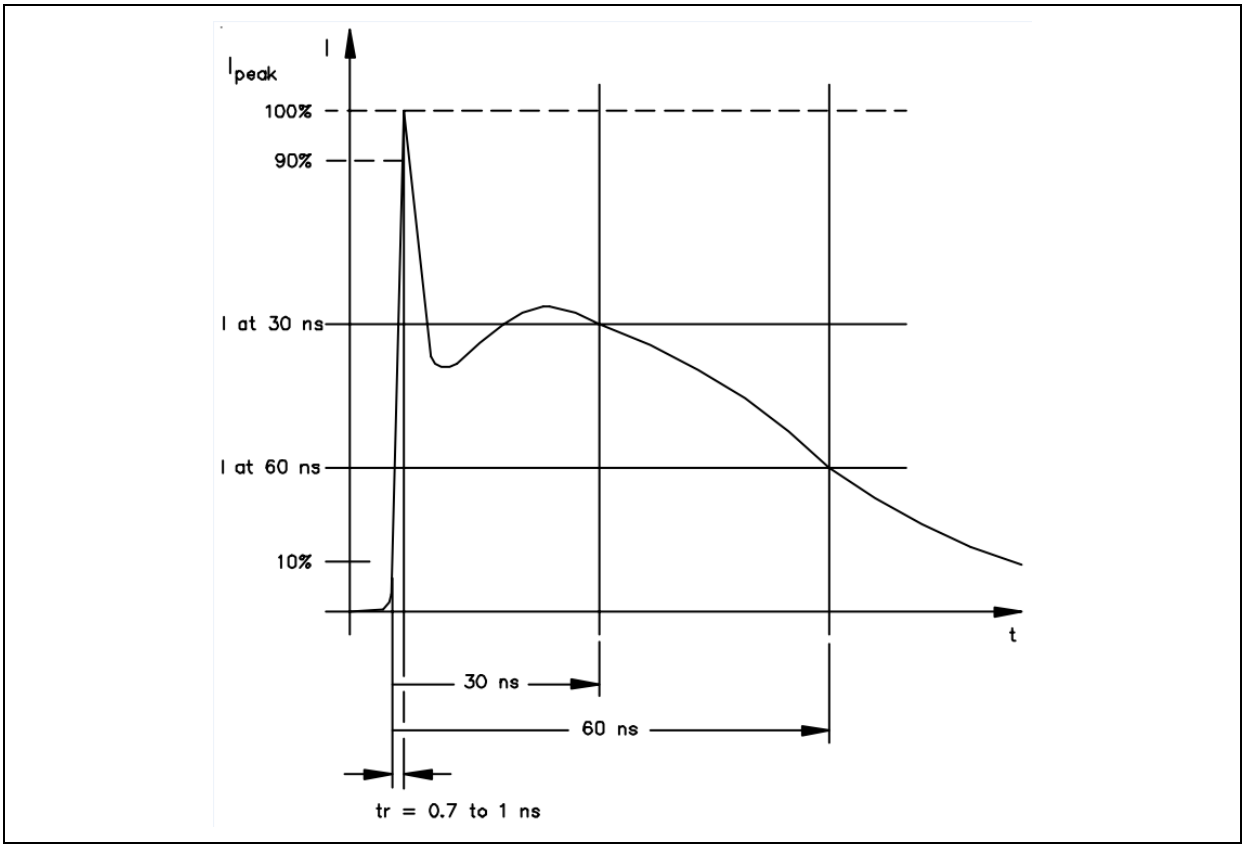

Figure 10-1 IEC 61000-4-2 ESD Pulse Waveform

- Protection Circuit

A general I/O connector of a piece of electrical equipment can be protected with the example circuit composed with external passive components shown in below.

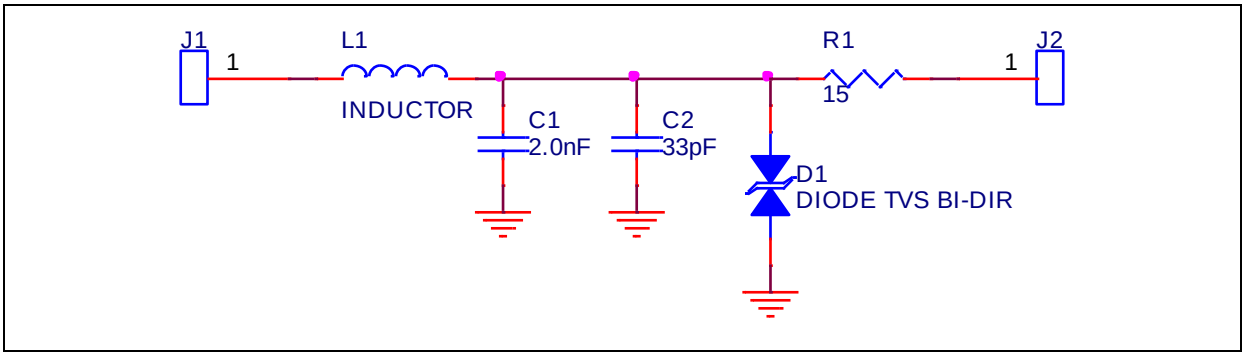

Figure 10-2 ESD Protection Circuit Example for GPIO

The ESD protection circuit composed from these above components can block ESD currents and clamp ESD induced high voltages. The exceeded ESD currents can be suppressed and shunted to minimize the effects of the ESD pulses in the system.

- Circuit Description
  - J1: connection point where the ESD shock occurs (high-voltage IEC 61000-4-2 Test Pulse)
  - J2: ESD-protected connection point (suppressed test signal)
  - L1: series filtering inductor
  - C1, C2: parallel filtering capacitors
  - D1: TVS diode
  - R: series resistor
- The ESD shock is supposed to occur at the “J1” point.

  The “L-C” low-pass filtering section suppresses the fast ESD shock signal; the “L1” inductor can block the large currents, while the “C1” and “C2” capacitors can limit the high voltage induced by the transient fast current spike.
  The “D1” TVS diode can be effectively used for suppressing the fast ramped-up ESD signals.
- Select Component

  The optimum values for the components depend on the level of the ESD signal, board layout. C1 is nanoFarad grade, for example, 2nF. C2 is picoFarad grade, for example, 33pF. R1 is several tens of ohms grade, for example, 15ohm.
  It is possible to select the filtering element values in a way where the largest suppression can be achieved at the GHz region, since the ramp-up time of the fast ESD signal is around 1 ns, as shown in Figure IEC 61000-4-2 ESD Pulse Waveform.
  The TVS diode used in the example protection circuit (“D1”) is: AZ1613-01L.
- Recommended layout

  It is highly recommended to place the protection circuit as close as possible to the connection point on the board where the ESD shock event can occur. This placing approach can minimize the possibility of causing further couplings of the ESD currents and voltages to the other blocks on the module.

23 Reference Schematics

This section shows the NuMaker-HMI-MA35D1-S2 board reference design circuit.

23.1 System Block

Figure 23-1 shows the System Block Circuit.

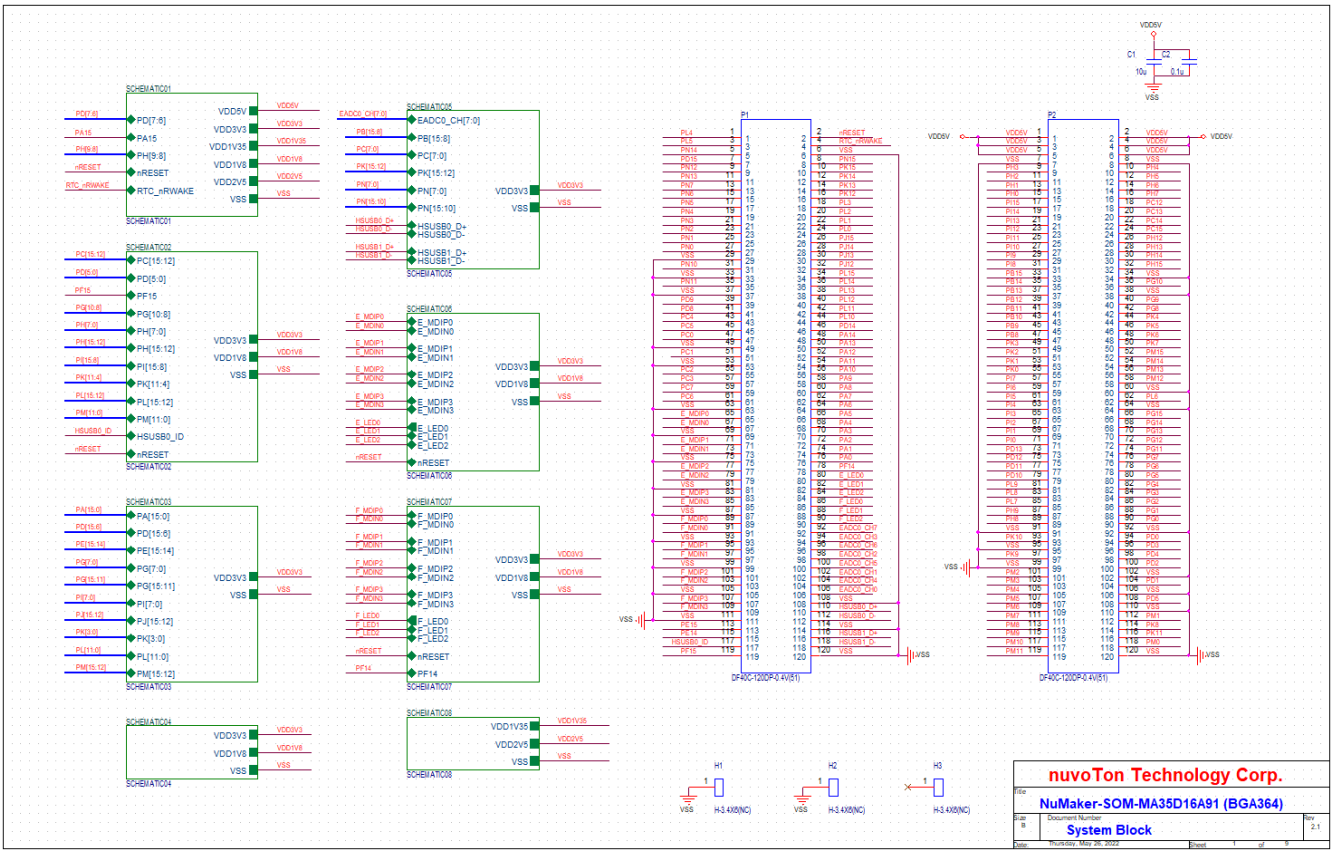

Figure 23-1 System Block Circuit

23.2 PMIC_DA9062

Figure 23-2 shows the PMIC_DA9062 circuit.

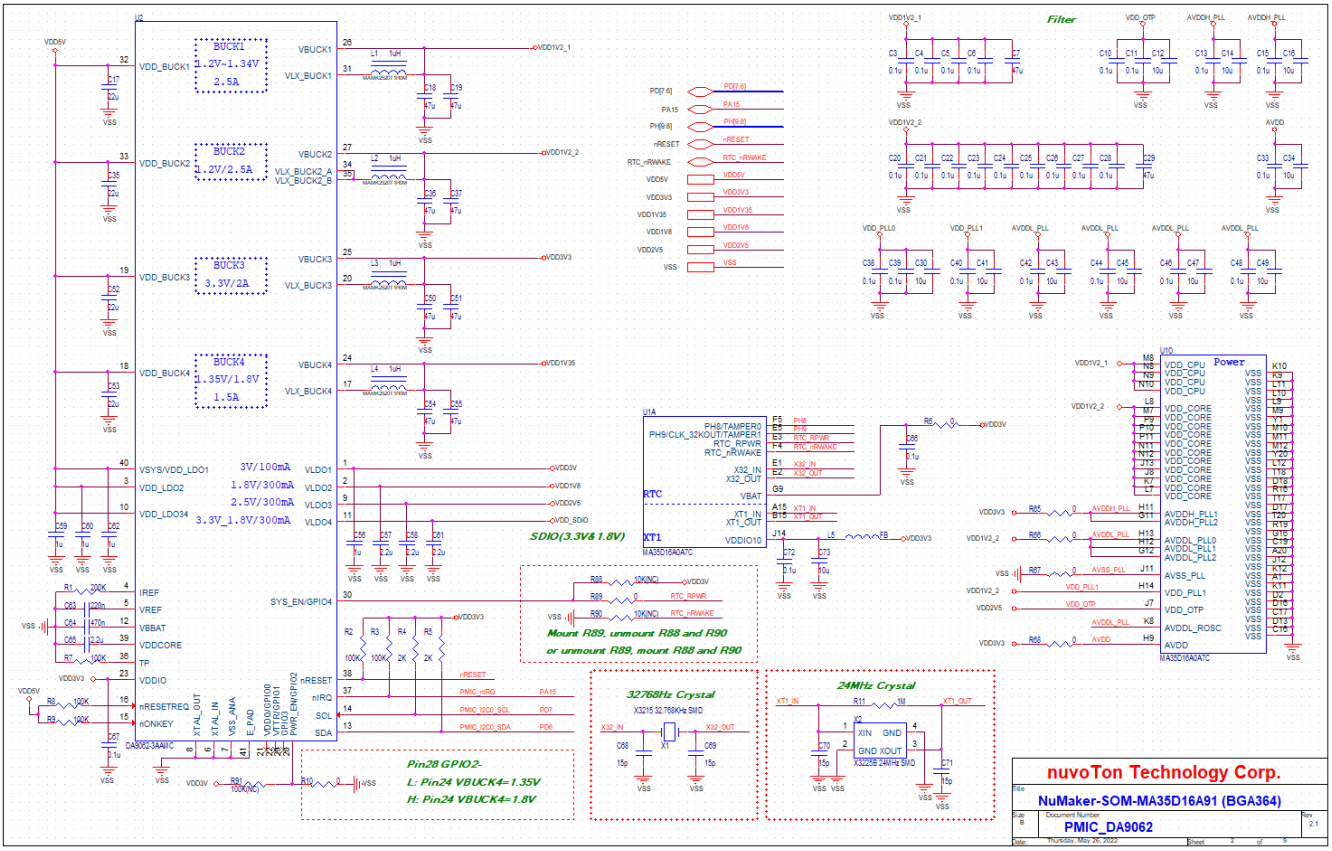

Figure 23-2 PMIC_DA9062 Circuit

23.3 VDDIO0/2/4/5

Figure 23-3 shows the VDDIO0/2/4/5 circuit.

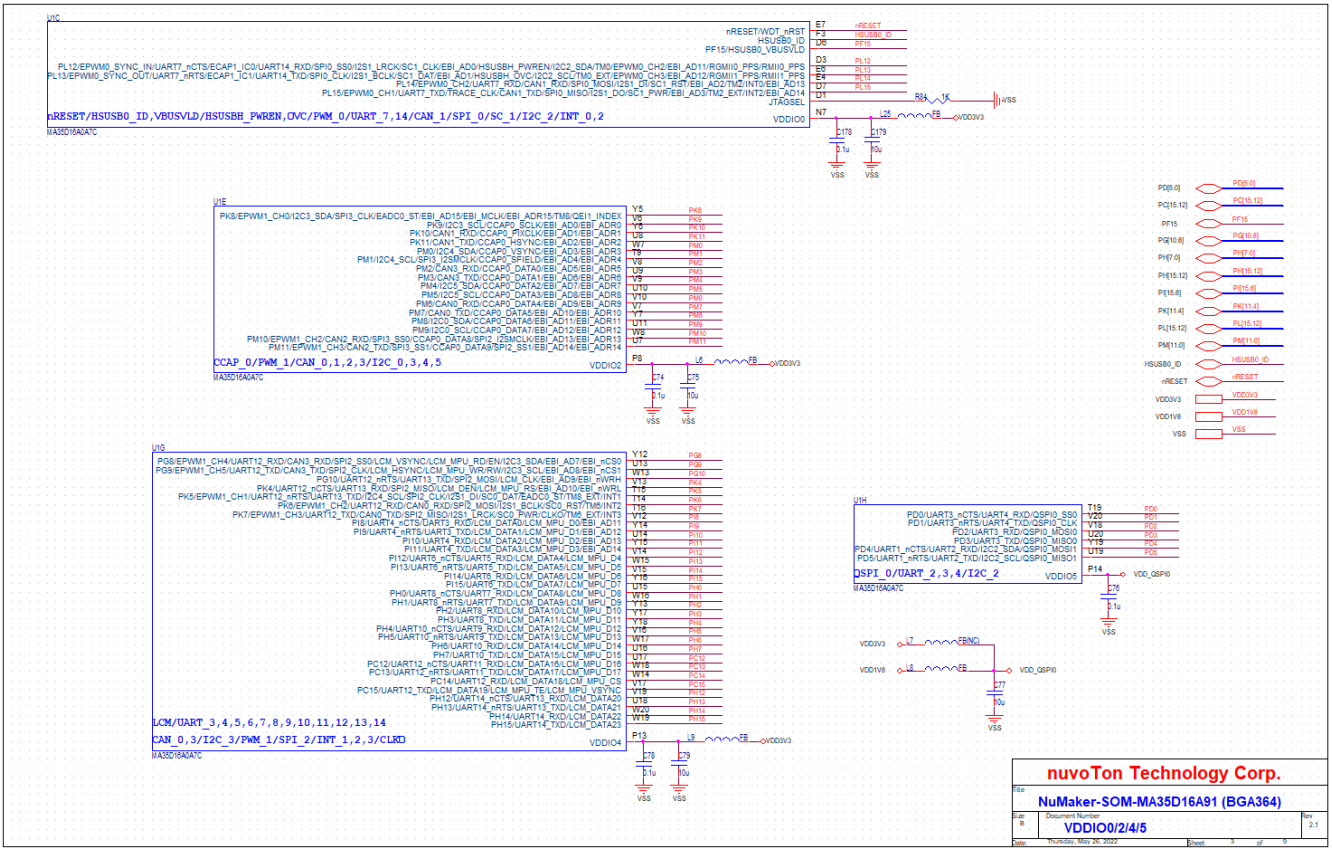

Figure 23-3 VDDIO0/2/4/5 Circuit

23.4 VDDIO1

Figure 23-4 shows the VDDIO1 circuit.

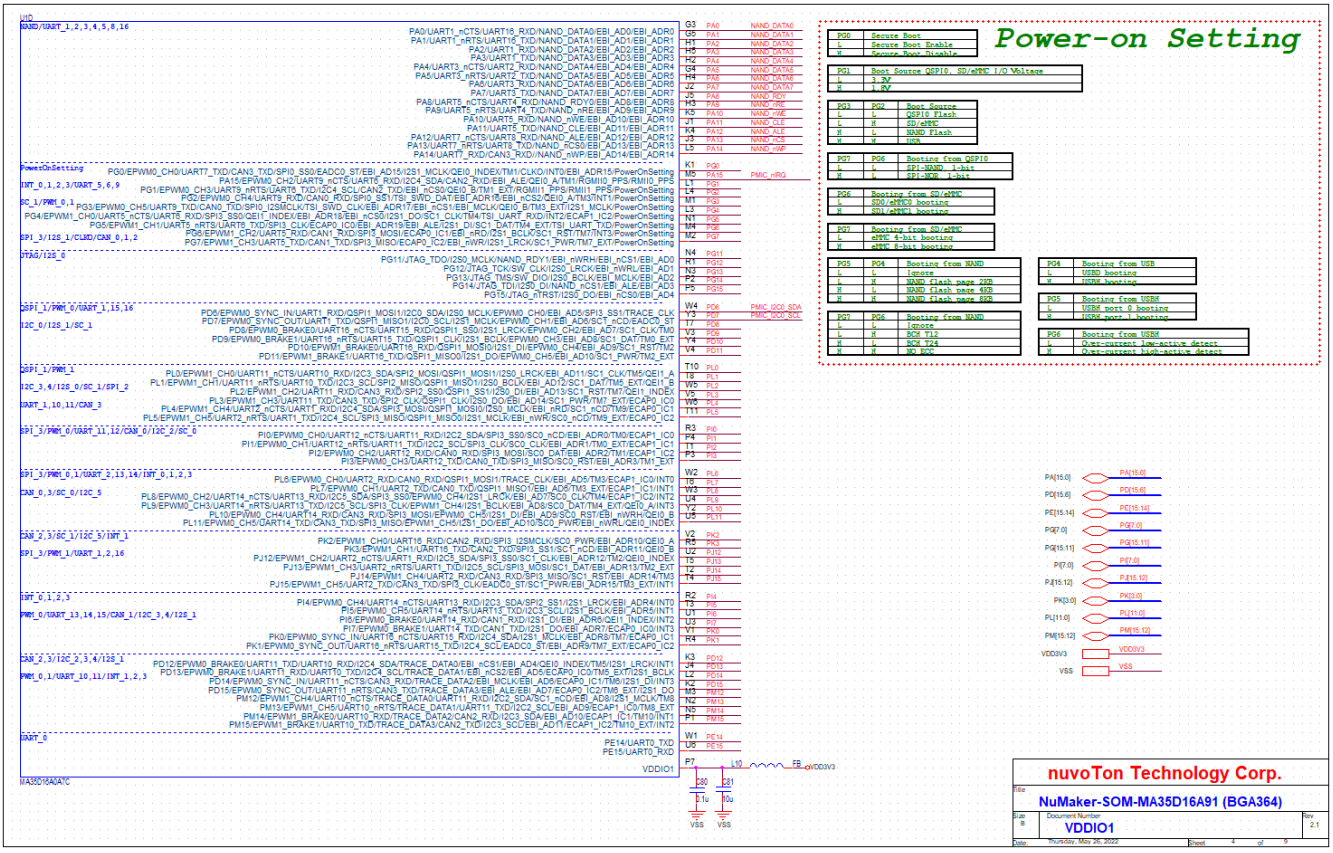

Figure 23-4 VDDIO1 Circuit

23.5 eMMC1 (VDDIO3)

Figure 23-5 shows the eMMC1 (VDDIO3) circuit.

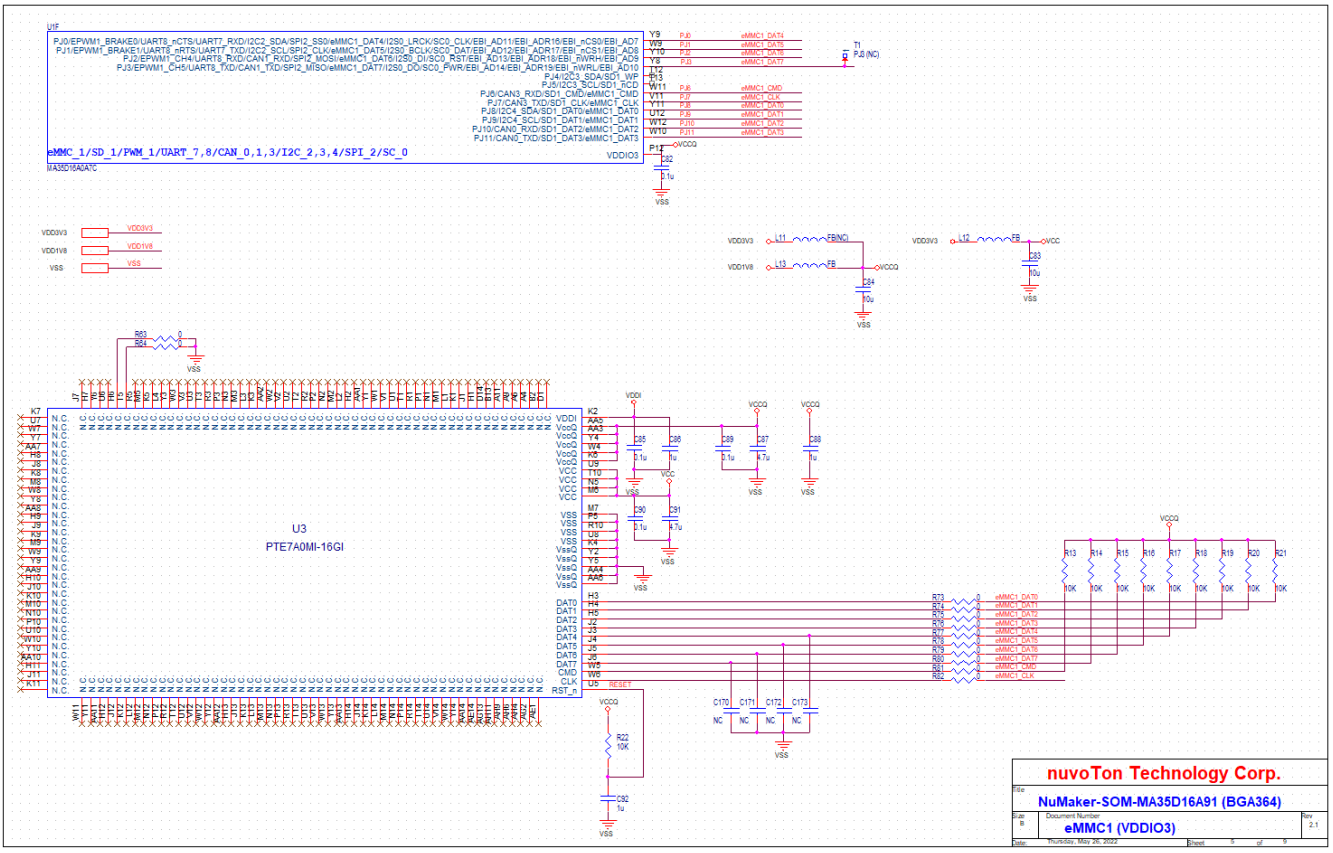

Figure 23-5 eMMC1 (VDDIO3) Circuit

23.6 VDDIO6/7/ADC/USB

Figure 23-6 shows the VDDIO6/7/ADC/USB circuit.

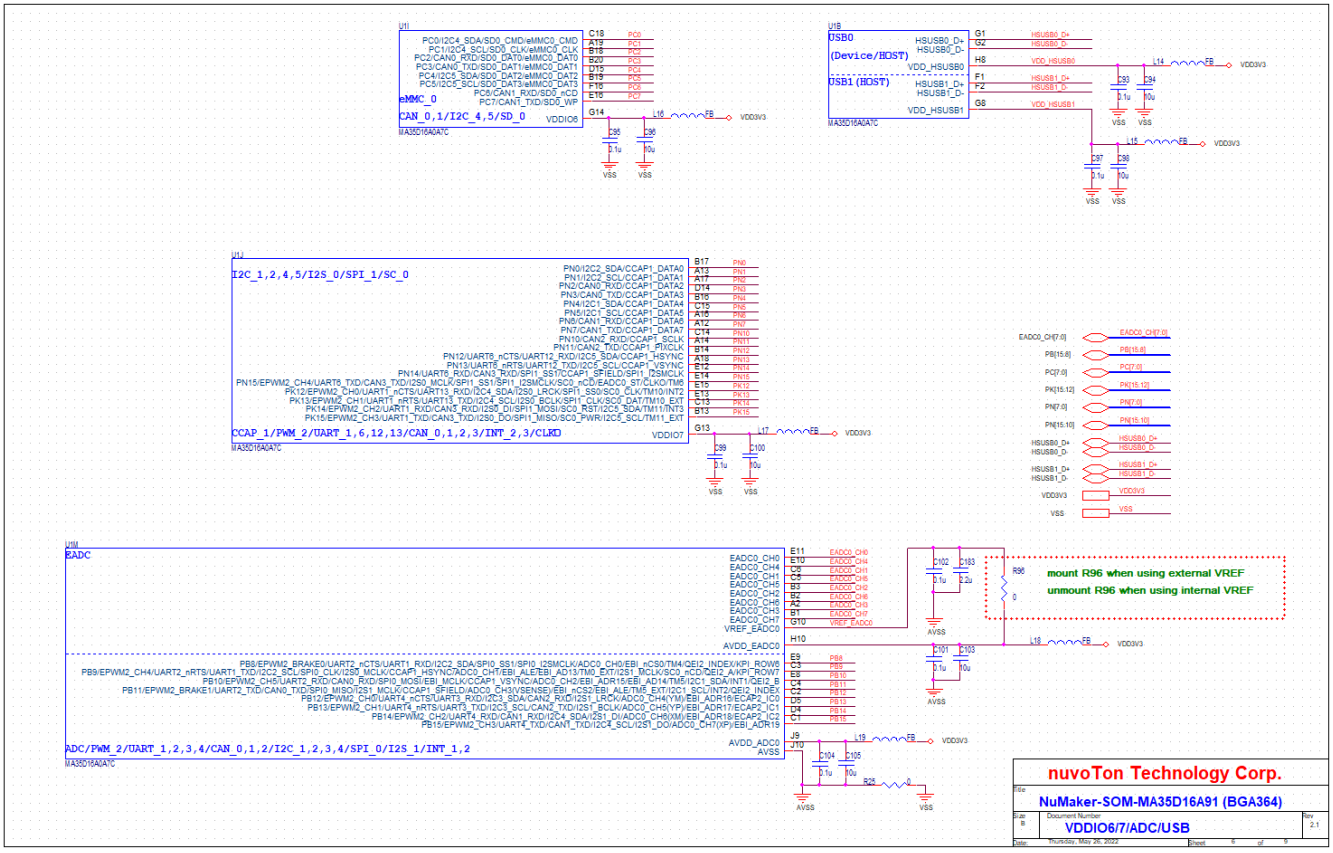

Figure 23-6 VDDIO6/7/ADC/USB Circuit

23.7 RGMII0_RTL8211F(D)I (VDDIO8)

Figure 23-7 shows the RGMII0_RTL8211F(D)I (VDDIO8) circuit.

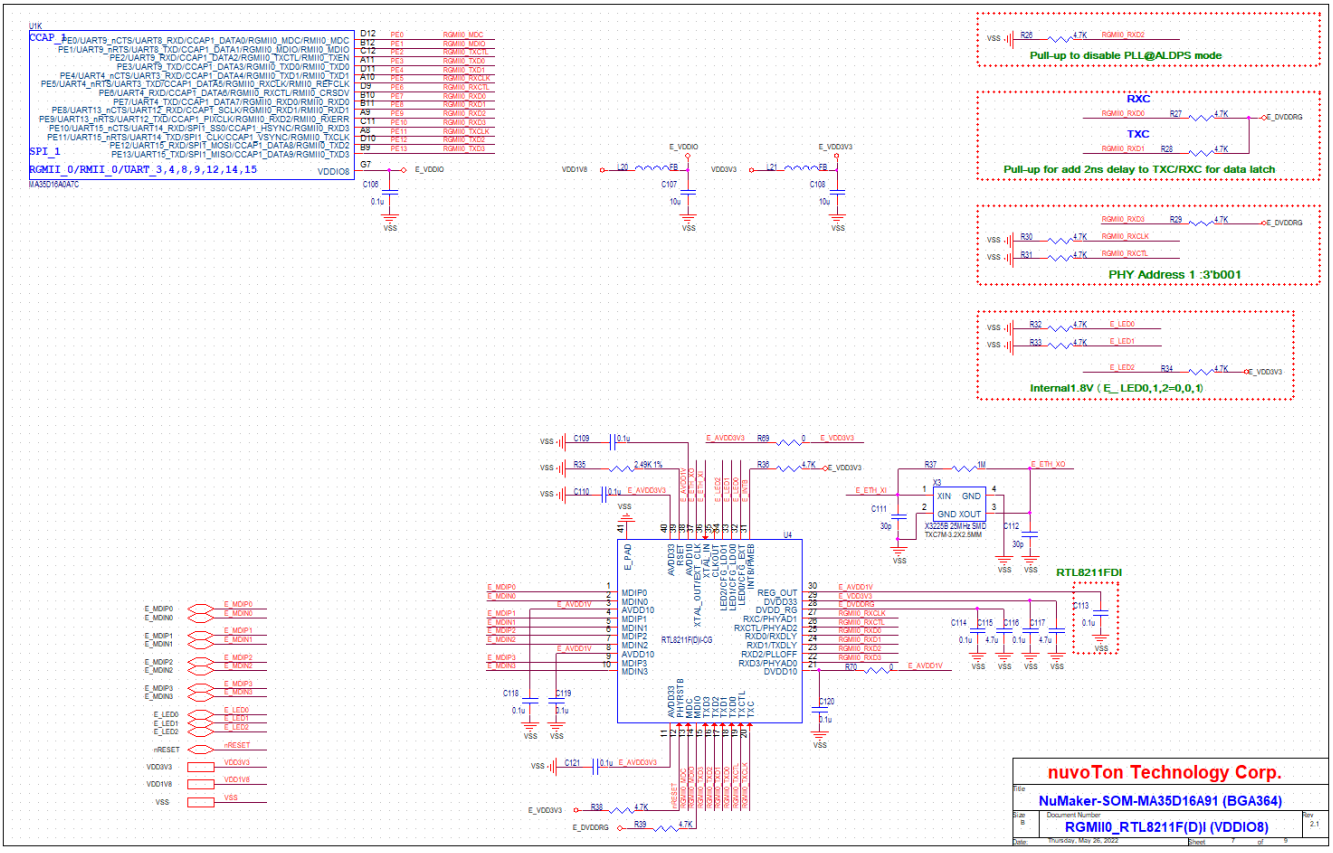

Figure 23-7 RGMII0_RTL8211F(D)I (VDDIO8) Circuit

23.8 RGMII1_RTL8211F(D)I (VDDIO9)

Figure 23-8 shows the RGMII1_RTL8211F(D)I (VDDIO9) circuit.

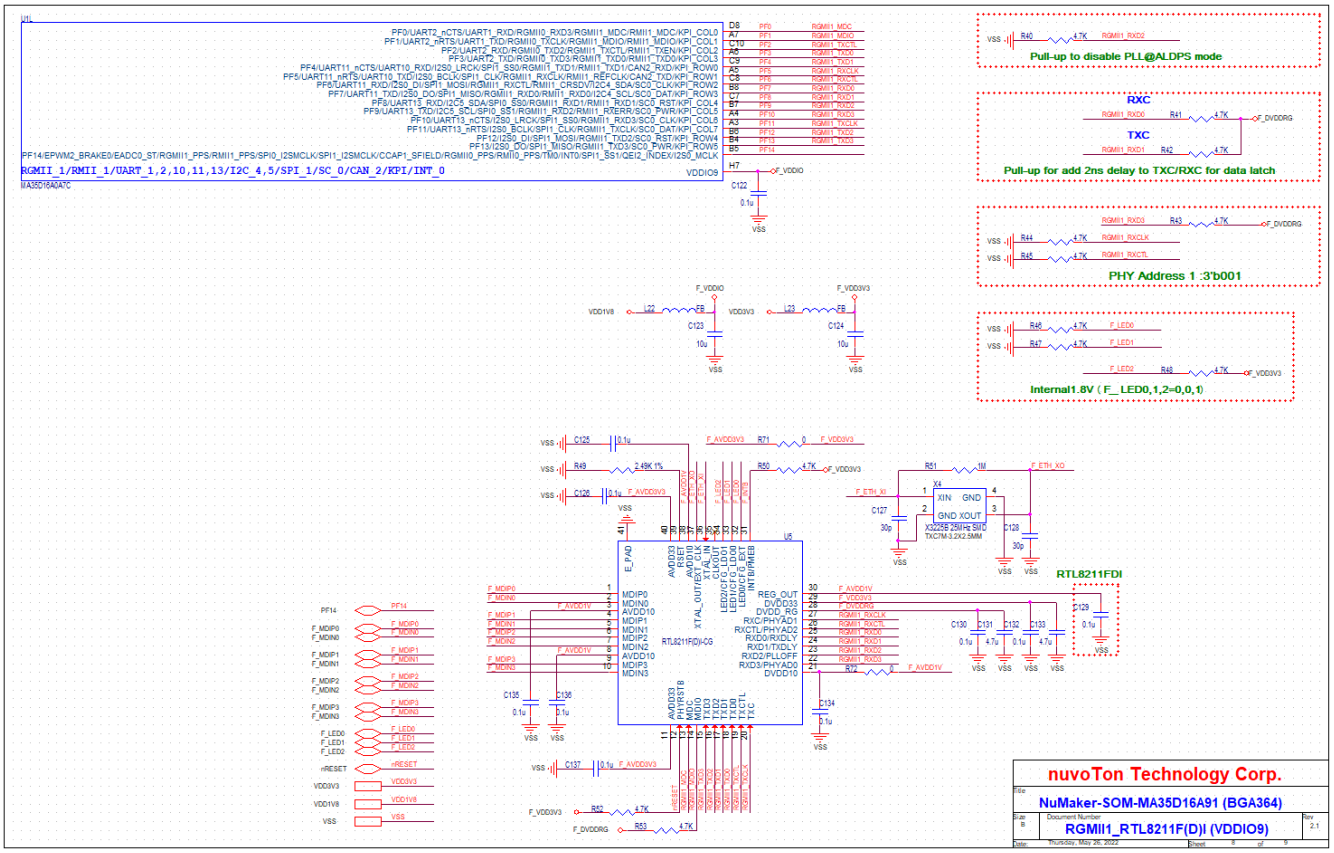

Figure 23-8 RGMII1_RTL8211F(D)I (VDDIO9) Circuit

23.9 DDR3L

Figure 23-9 shows the DDR3L circuit.

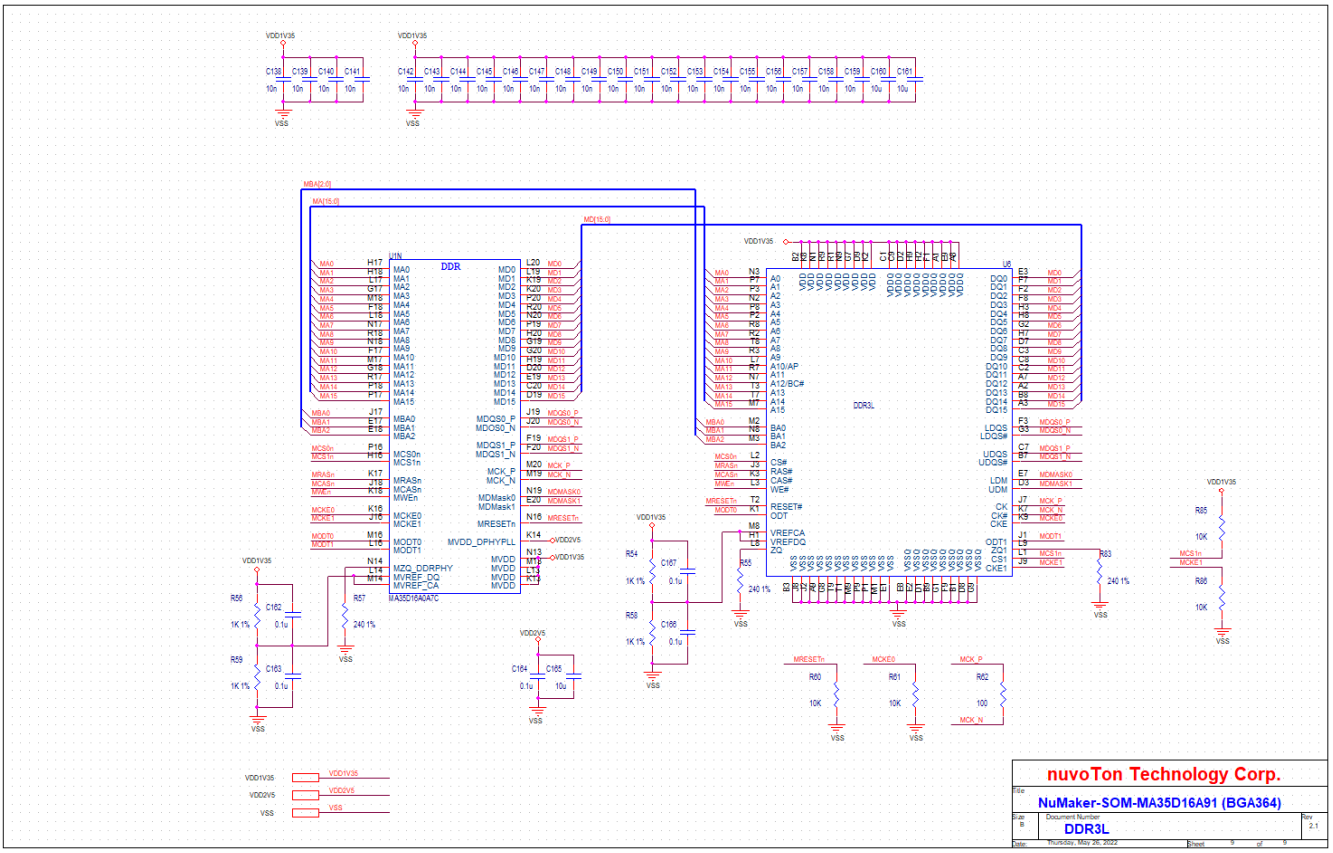

Figure 23-9 DDR3L Circuit

23.10 Power

Figure 23-10 shows the Power circuit.

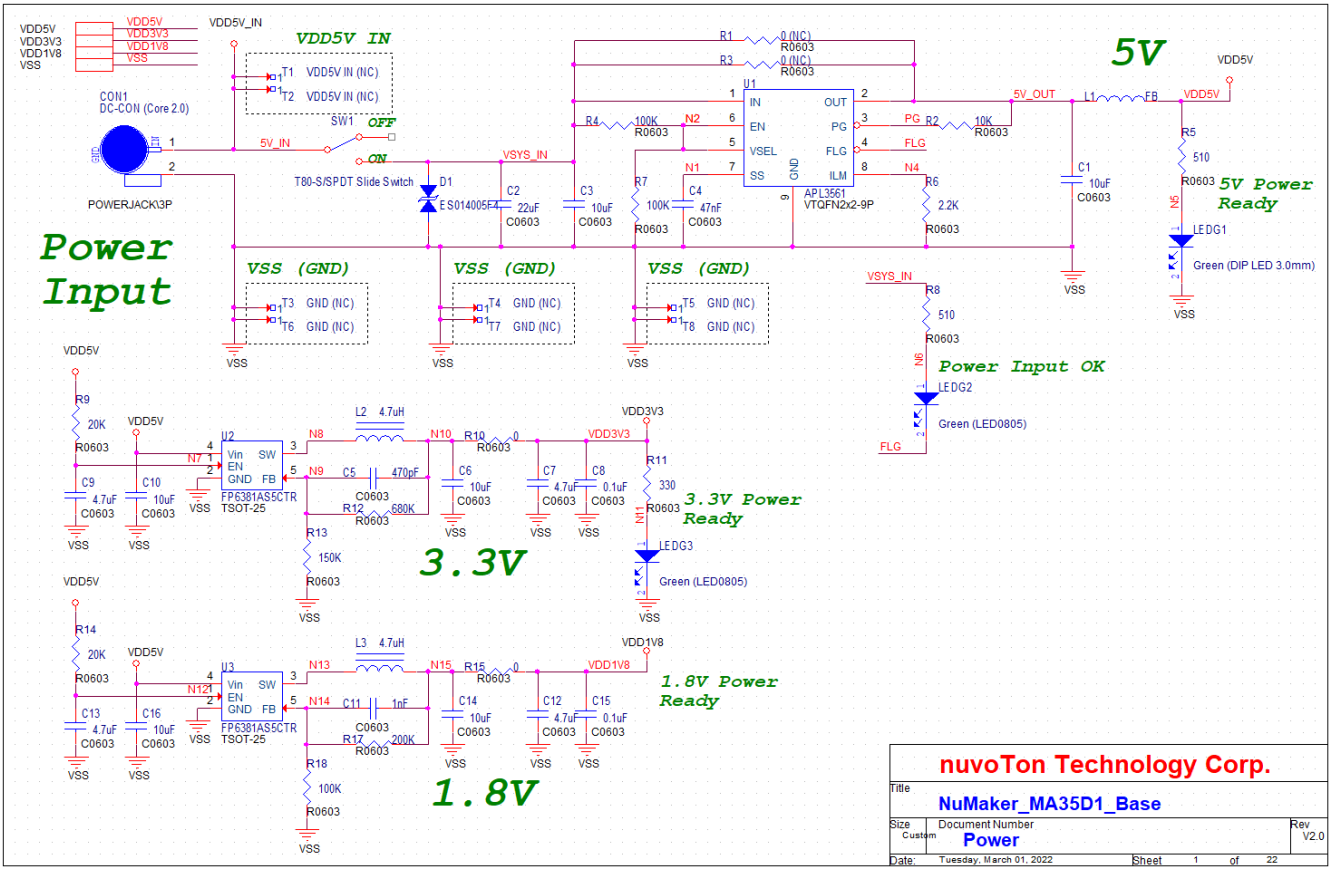

Figure 23-10 Power Circuit

23.11 SOM Connectors

Figure 23-11shows the SOM Connector circuit.

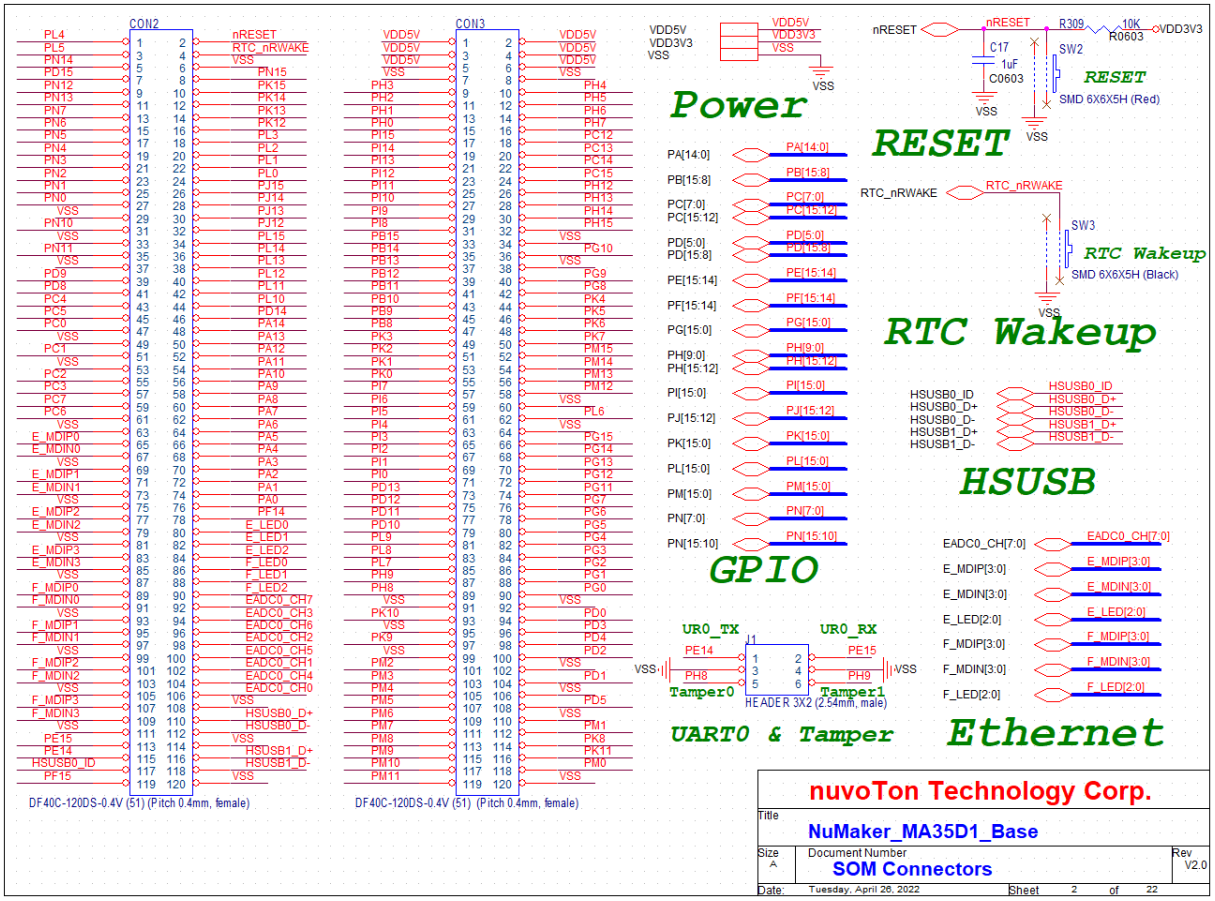

Figure 23-11 SOM Connectors Circuit

23.12 Power-on Setting and NAND Flash

Figure 23-12 shows the Power-on setting and NAND Flash circuit.

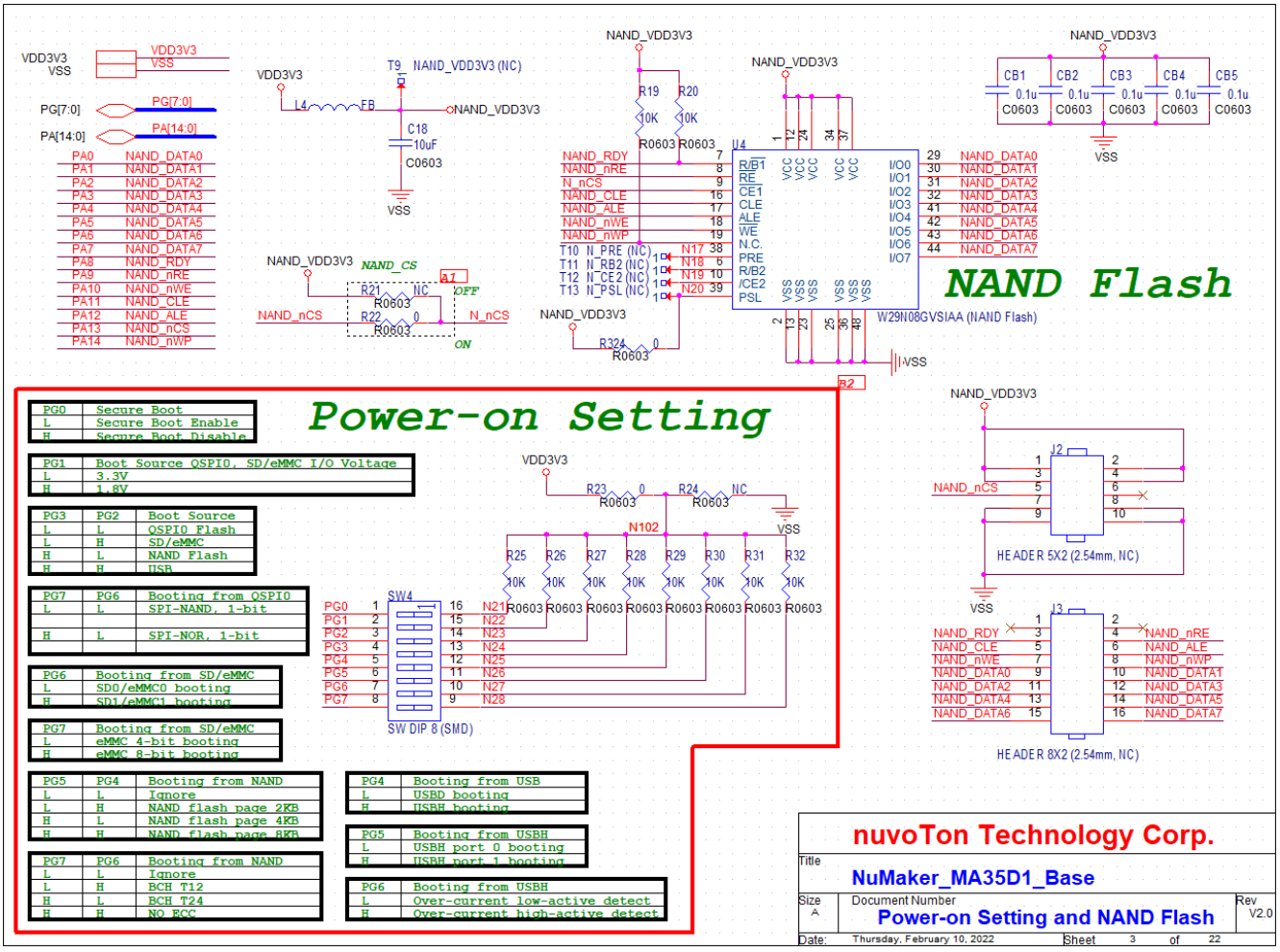

Figure 23-12 Power-on Setting and NAND Flash Circuit

23.13 SD0

Figure 23-13 shows the SD0 circuit.

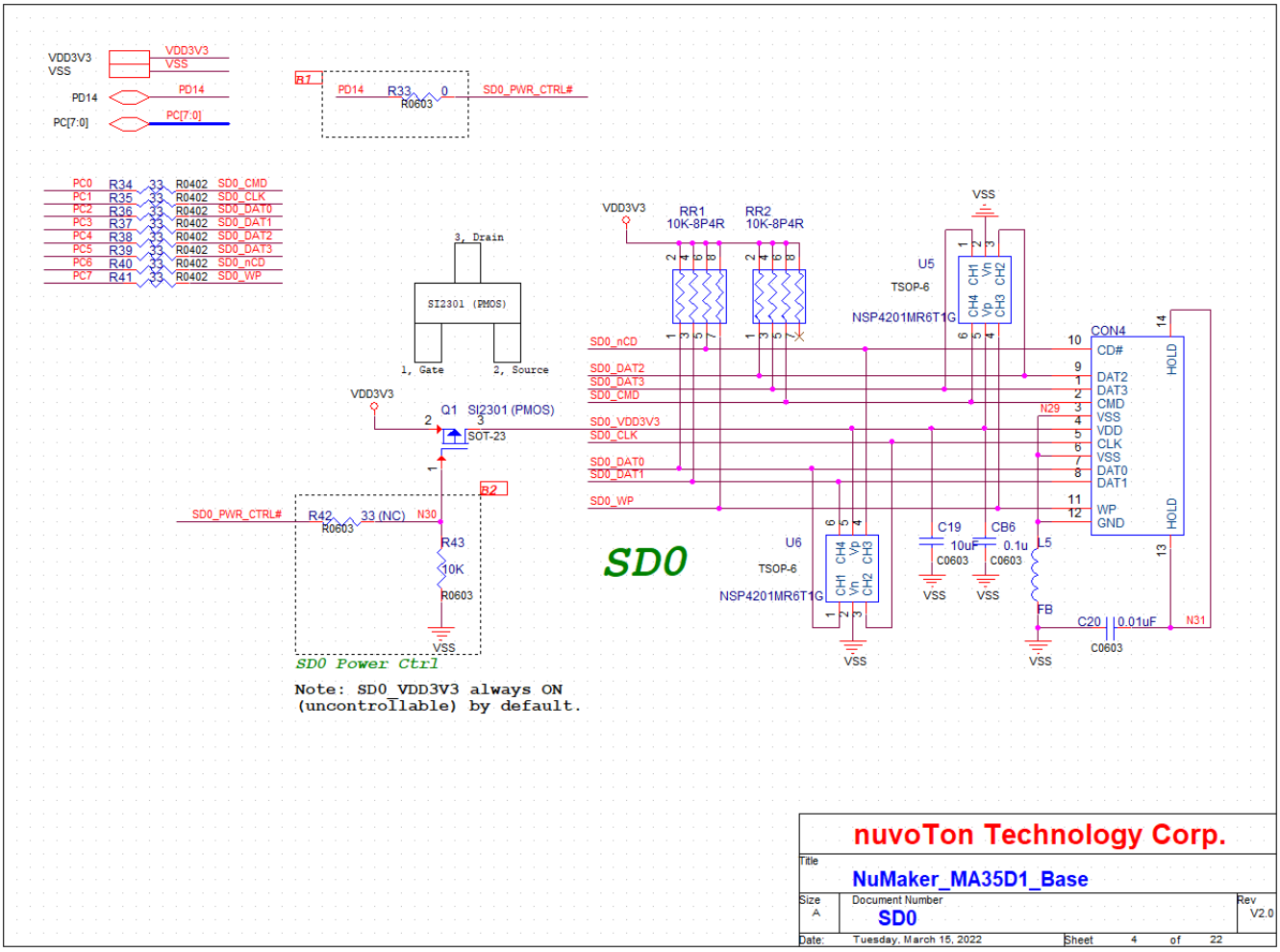

Figure 23-13 SD0 Circuit

23.14 QSPI0

Figure 23-14 shows the QSPI0 circuit.

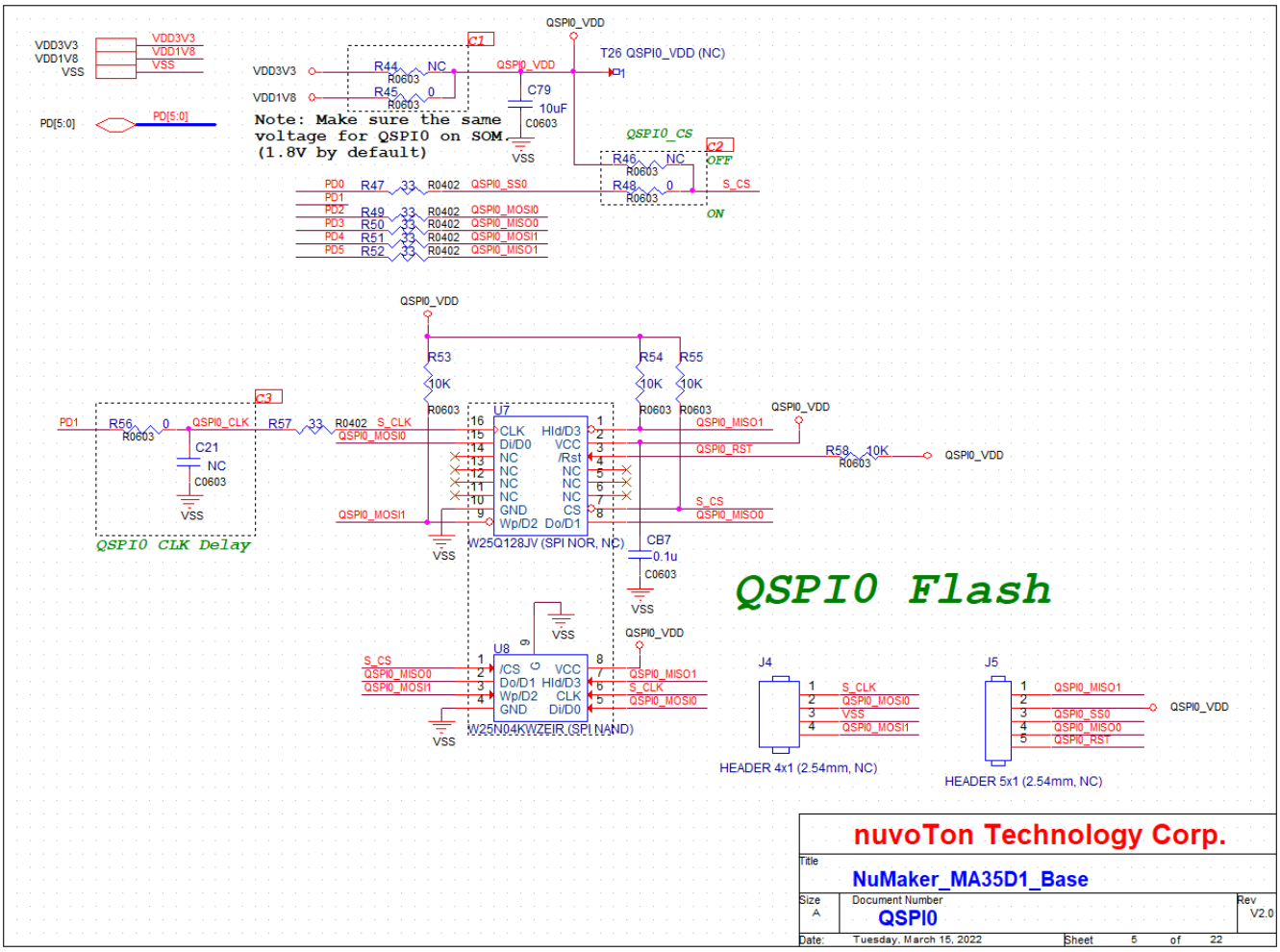

Figure 23-14 QSPI0 Circuit

23.15 EADC0

Figure 23-15 shows the EADC0 circuit.

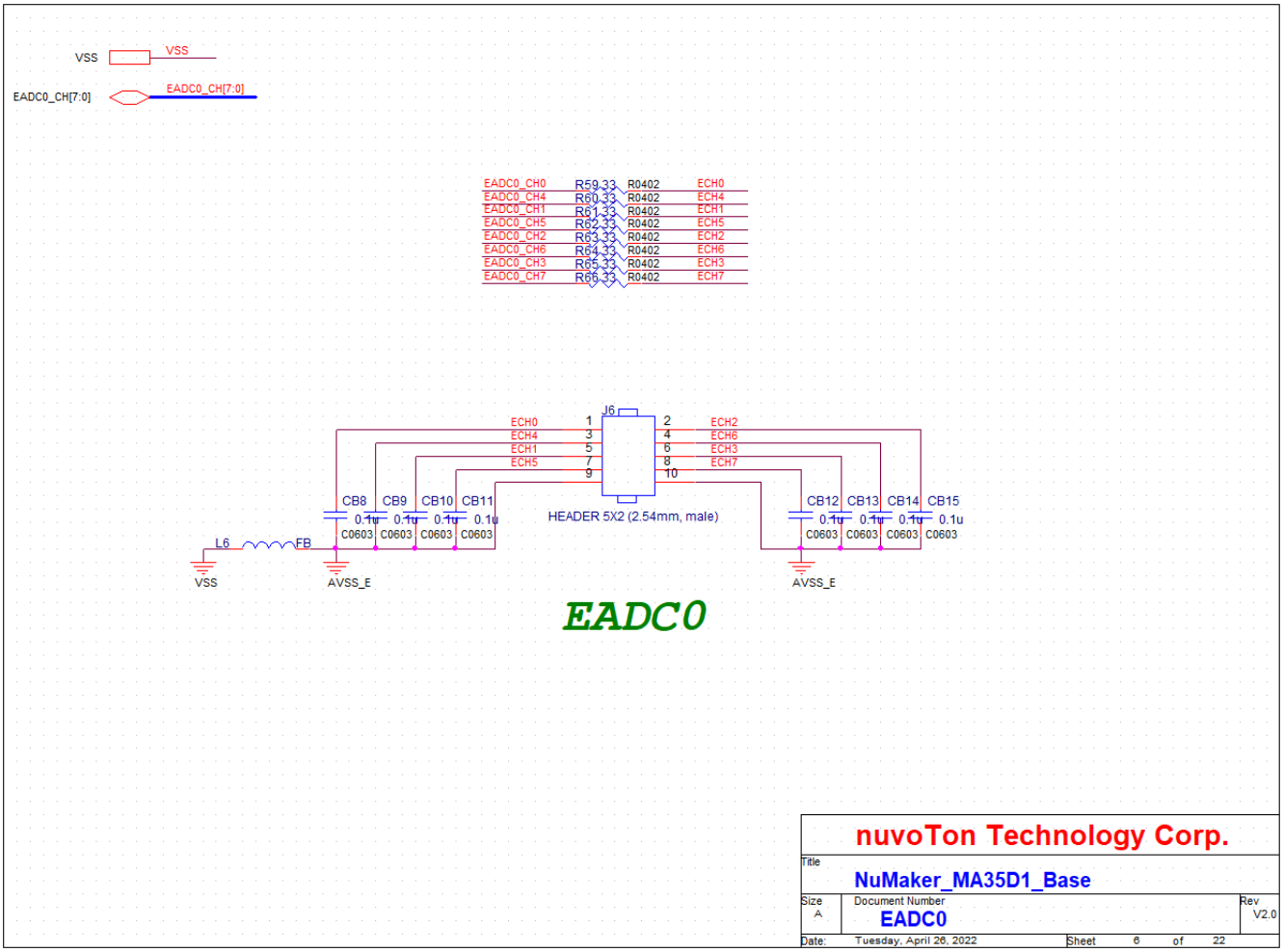

Figure 23-15 EADC0 Circuit

23.16 Ethernet 0 (PE)

Figure 23-16 shows the Ethernet 0 (PE) circuit.

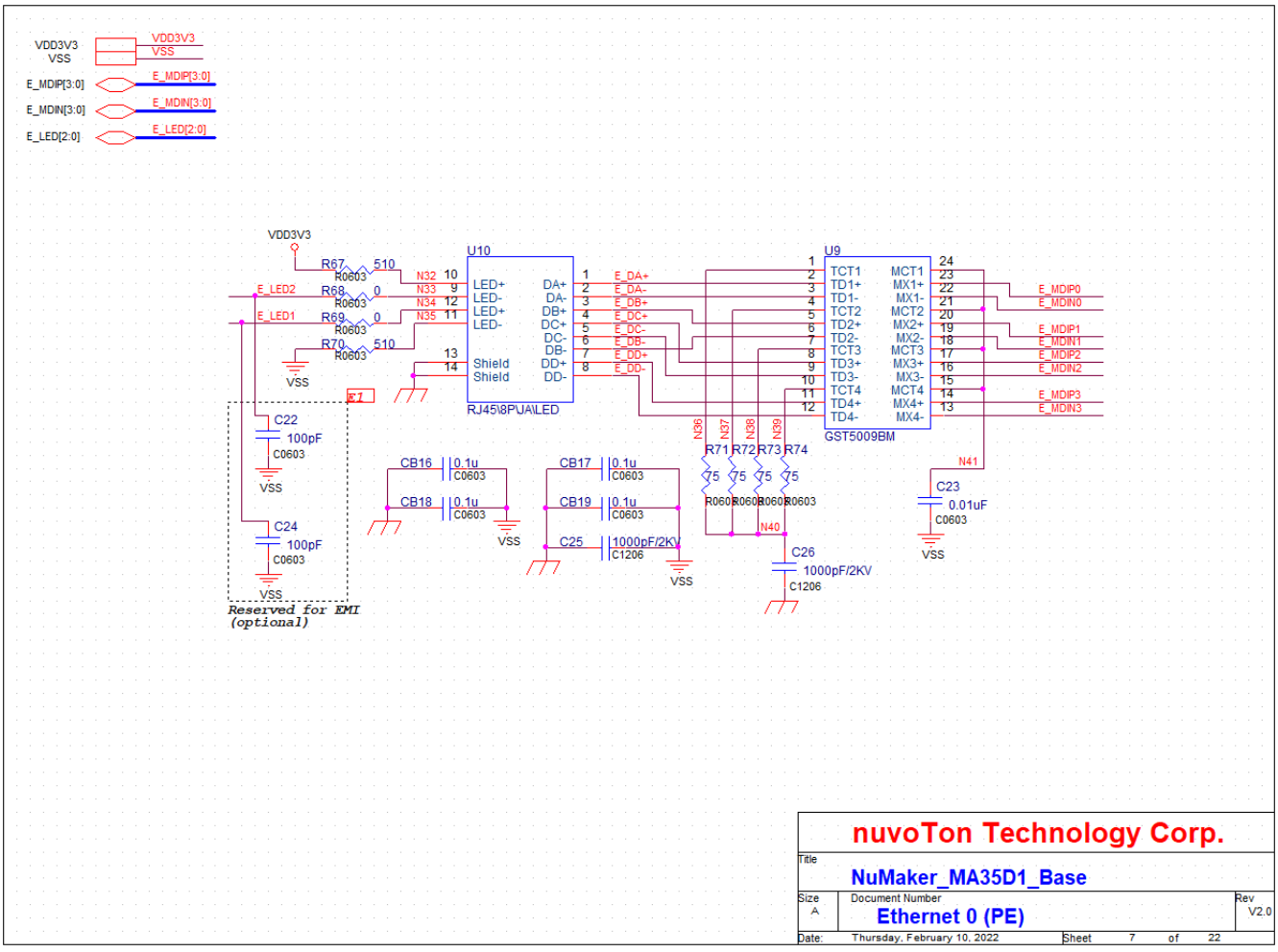

Figure 23-16 Ethernet 0 (PE) Circuit

23.17 Ethernet 1 (PF)

Figure 23-17 shows the Ethernet 1 (PF) circuit.

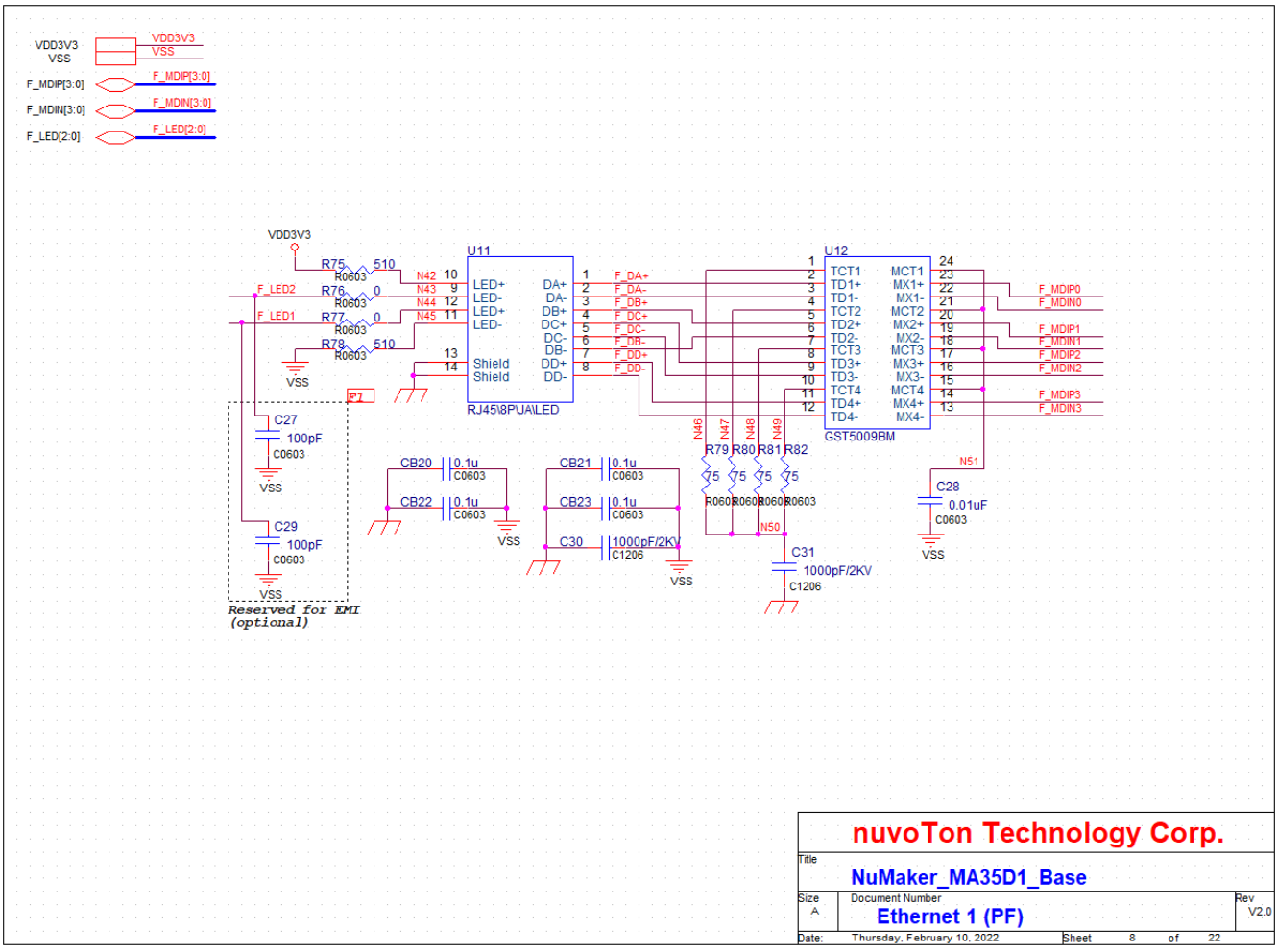

Figure 23-17 Ethernet 1 (PF) Circuit

23.18 HSUSB 0/1

Figure 23-18 shows the HSUSB 0/1 circuit.

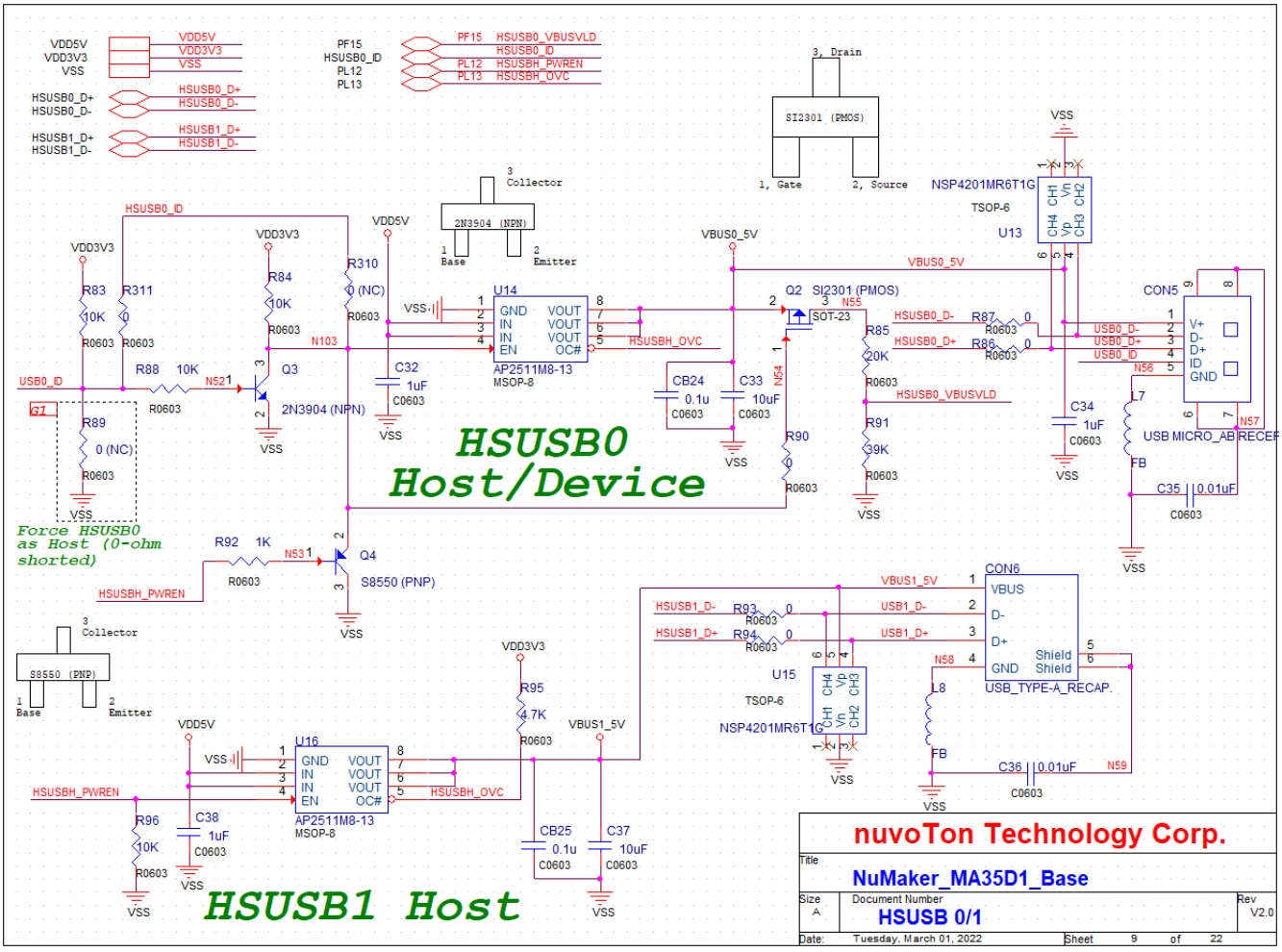

Figure 23-18 HSUSB 0/1 Circuit

23.19 CCAP 0/1 Connectors

Figure 23-19 shows the CCAP 0/1 Connectors circuit.

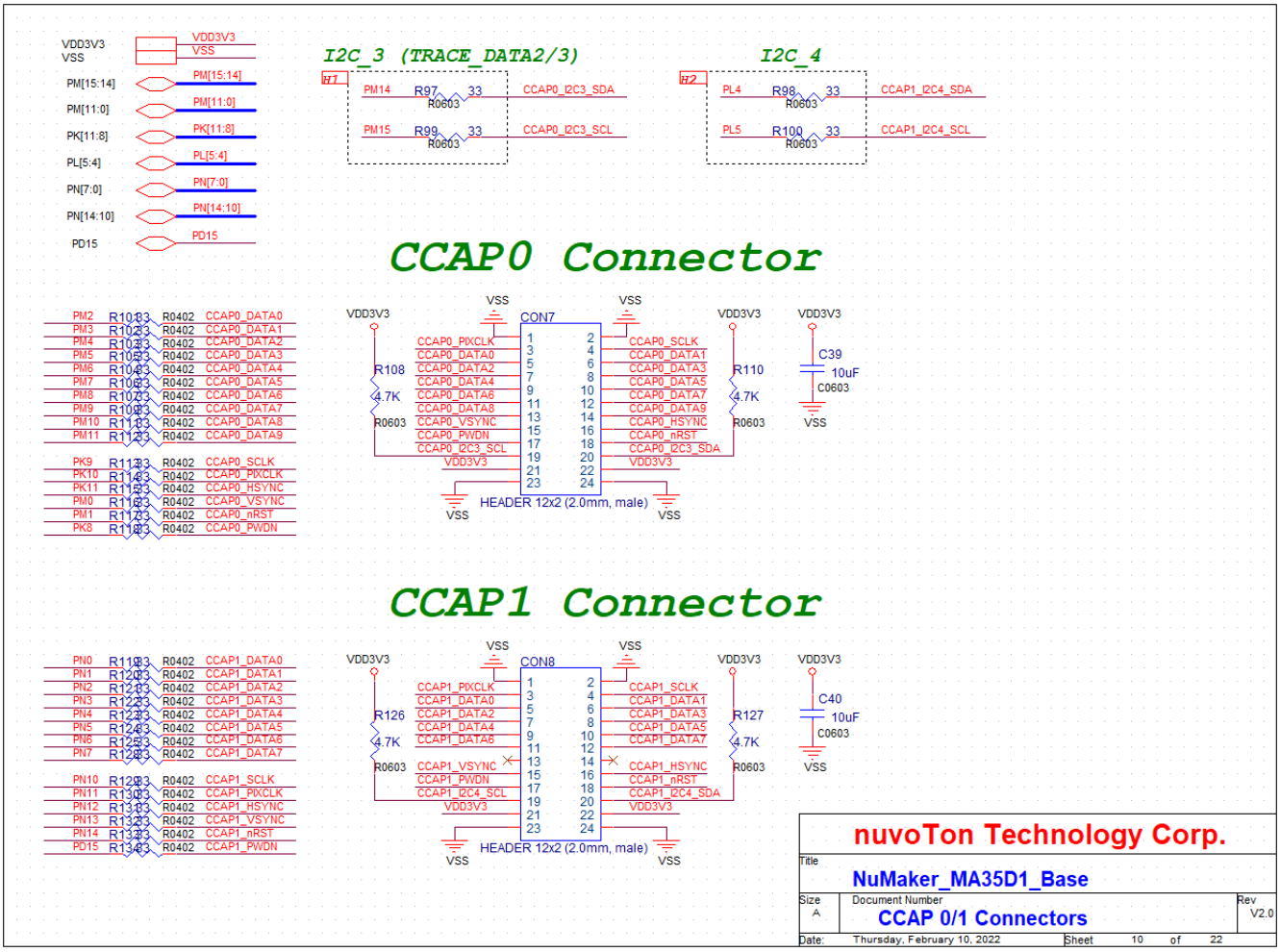

Figure 23-19 CCAP 0/1 Connectors Circuit

23.20 LCM Connector

Figure 23-20 shows the LCM Connector circuit.

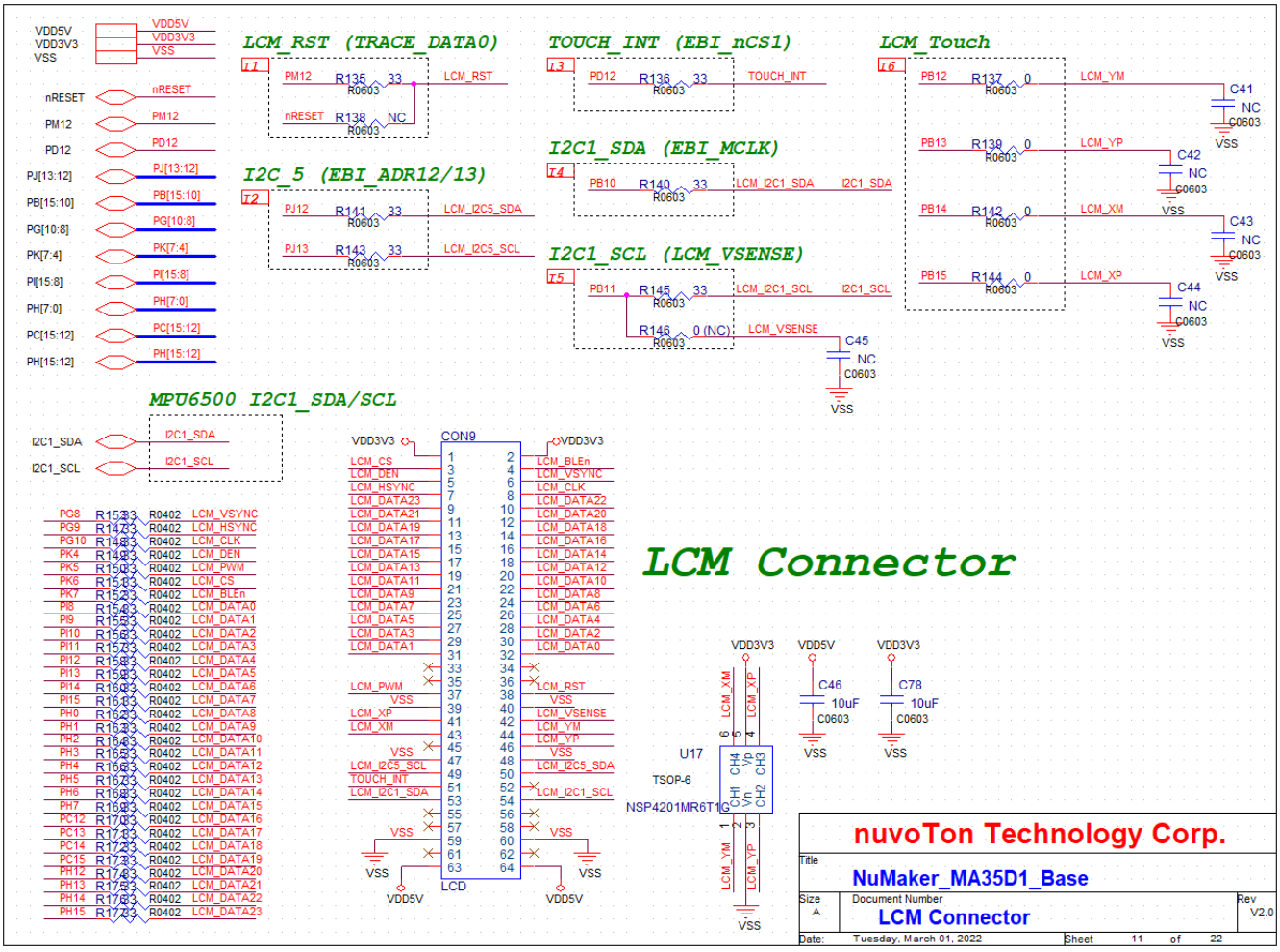

Figure 23-20 LCM Connector Circuit

23.21 EBI Connector

Figure 23-21 shows the EBI Connector circuit.

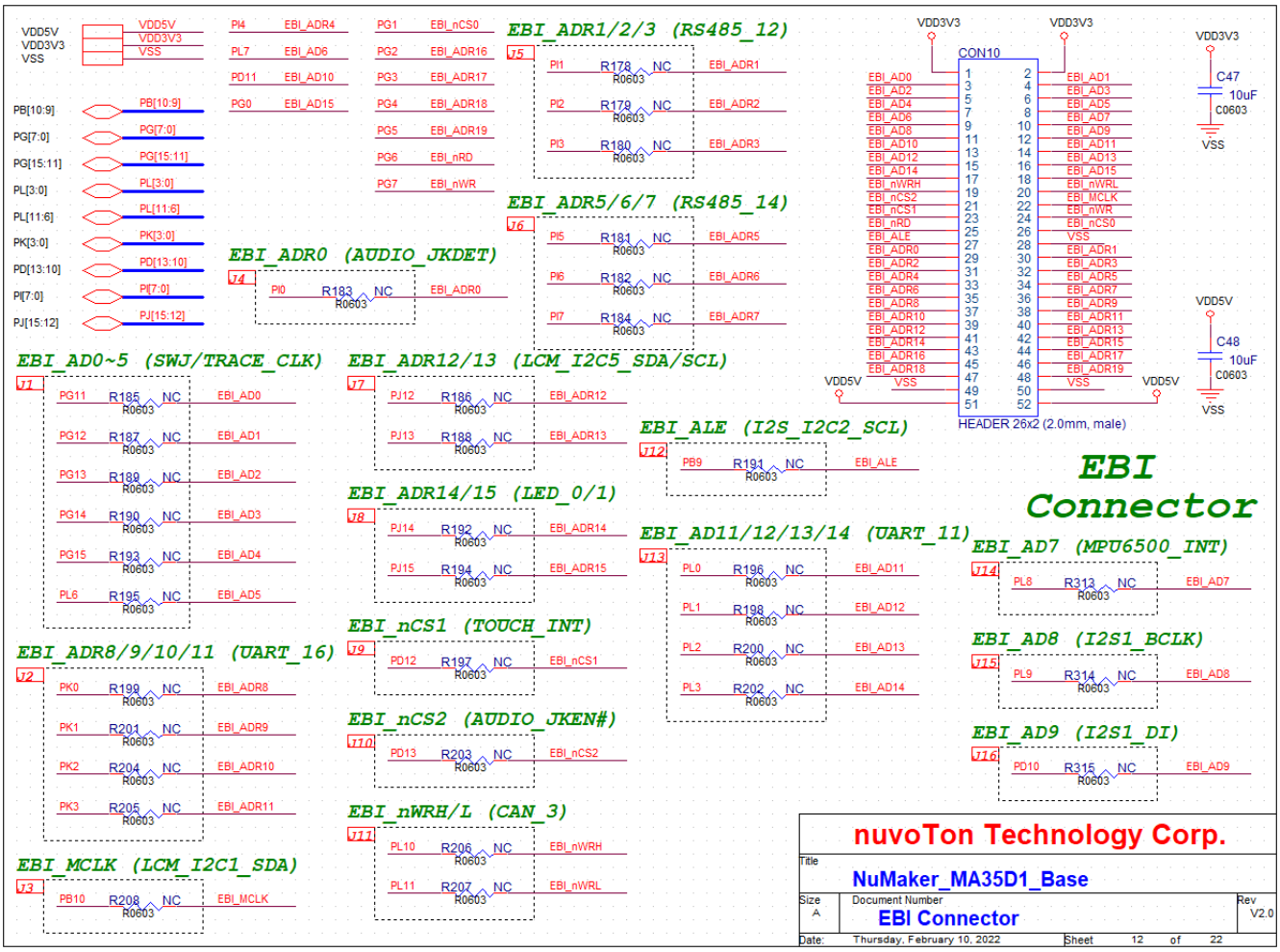

Figure 23-21 EBI Connector Circuit

23.22 NAU88C22 Audio Codec

Figure 23-22 shows the NAU88C22 Audio Codec circuit.

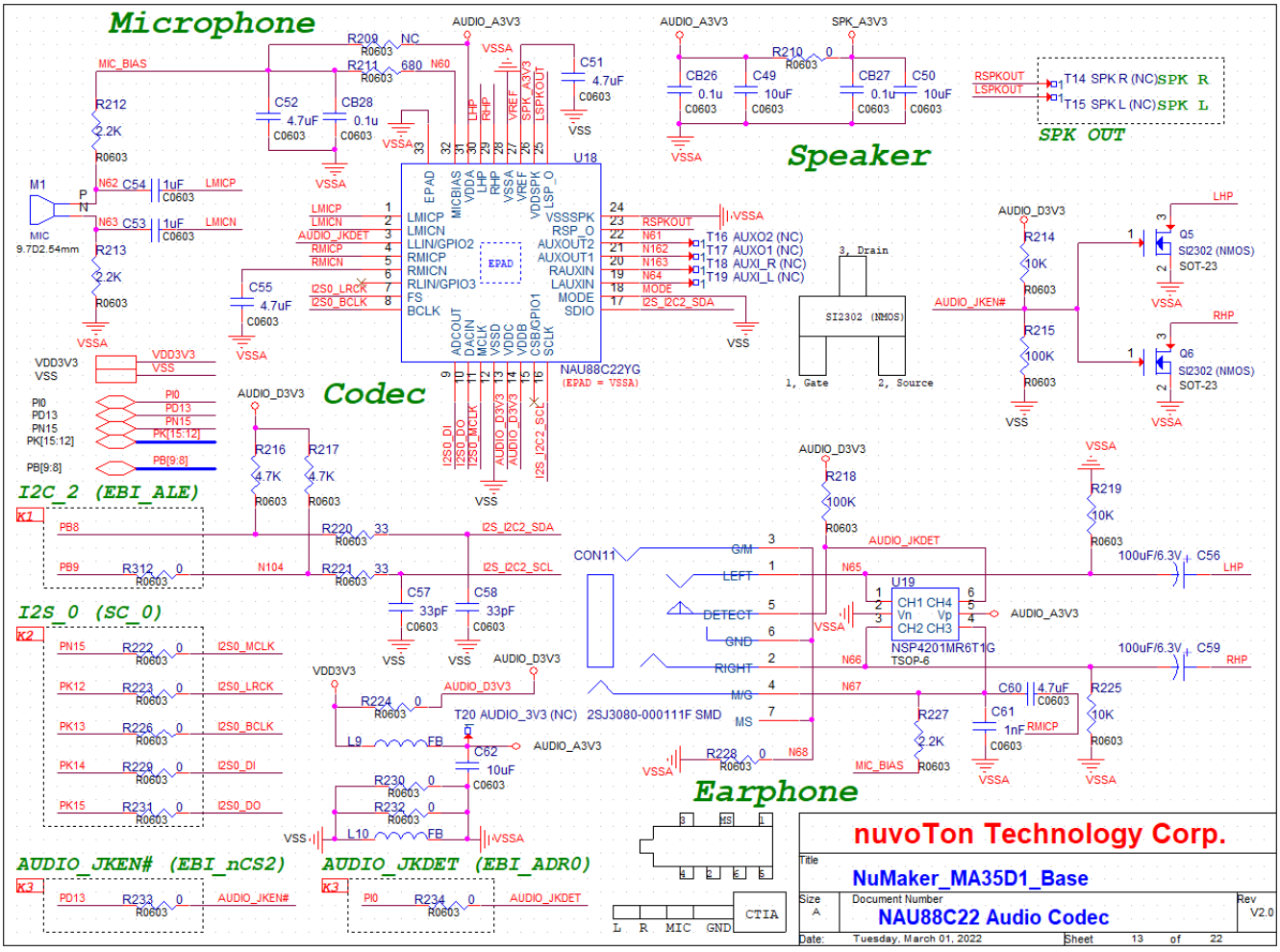

Figure 23-22 NAU88C22 Audio Codec Circuit

23.23 SIM Card

Figure 23-23 shows the SIM card circuit.

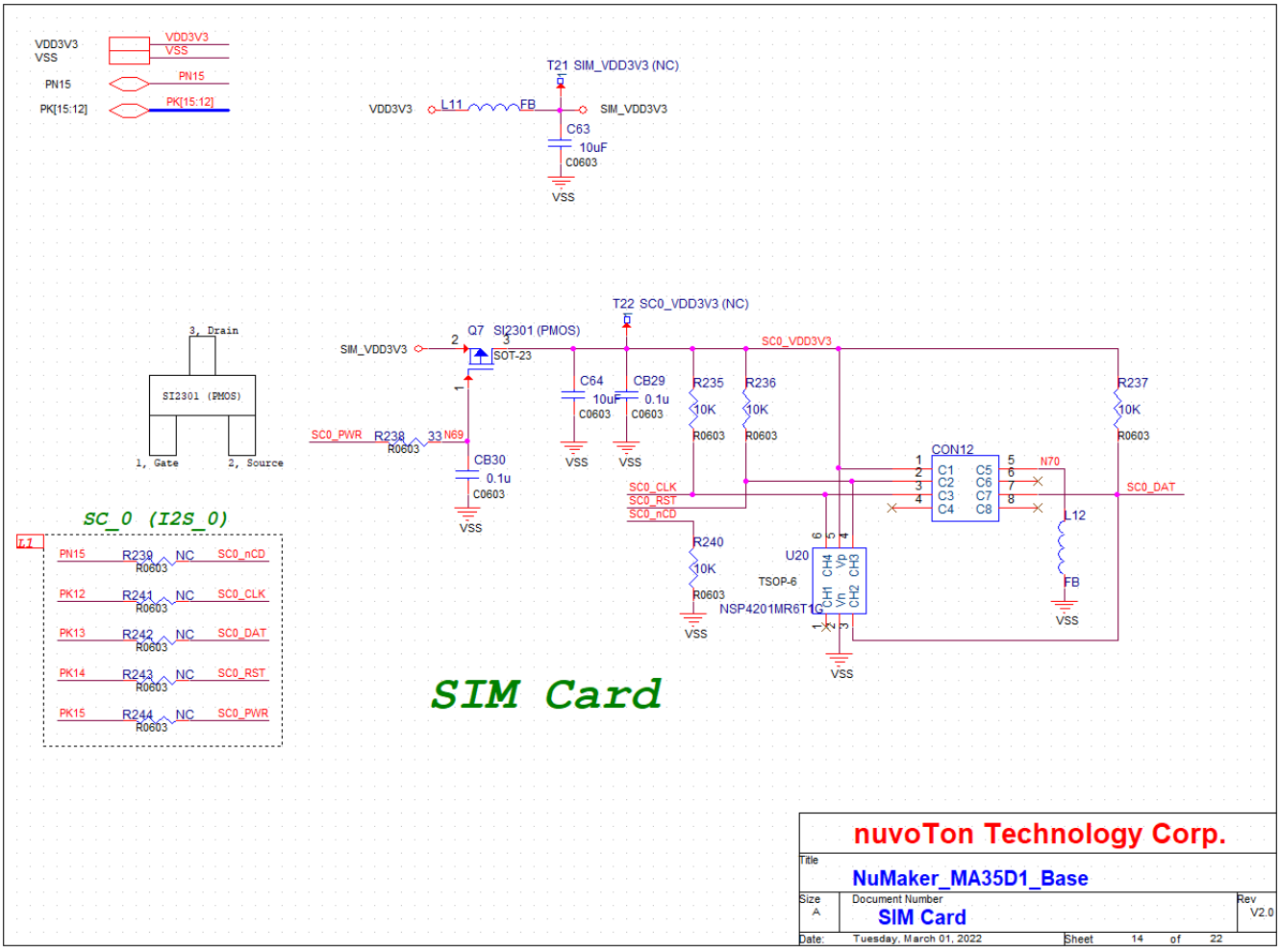

Figure 23-23 SIM Card Circuit

23.24 RS232

Figure 23-24 shows the RS232 circuit.

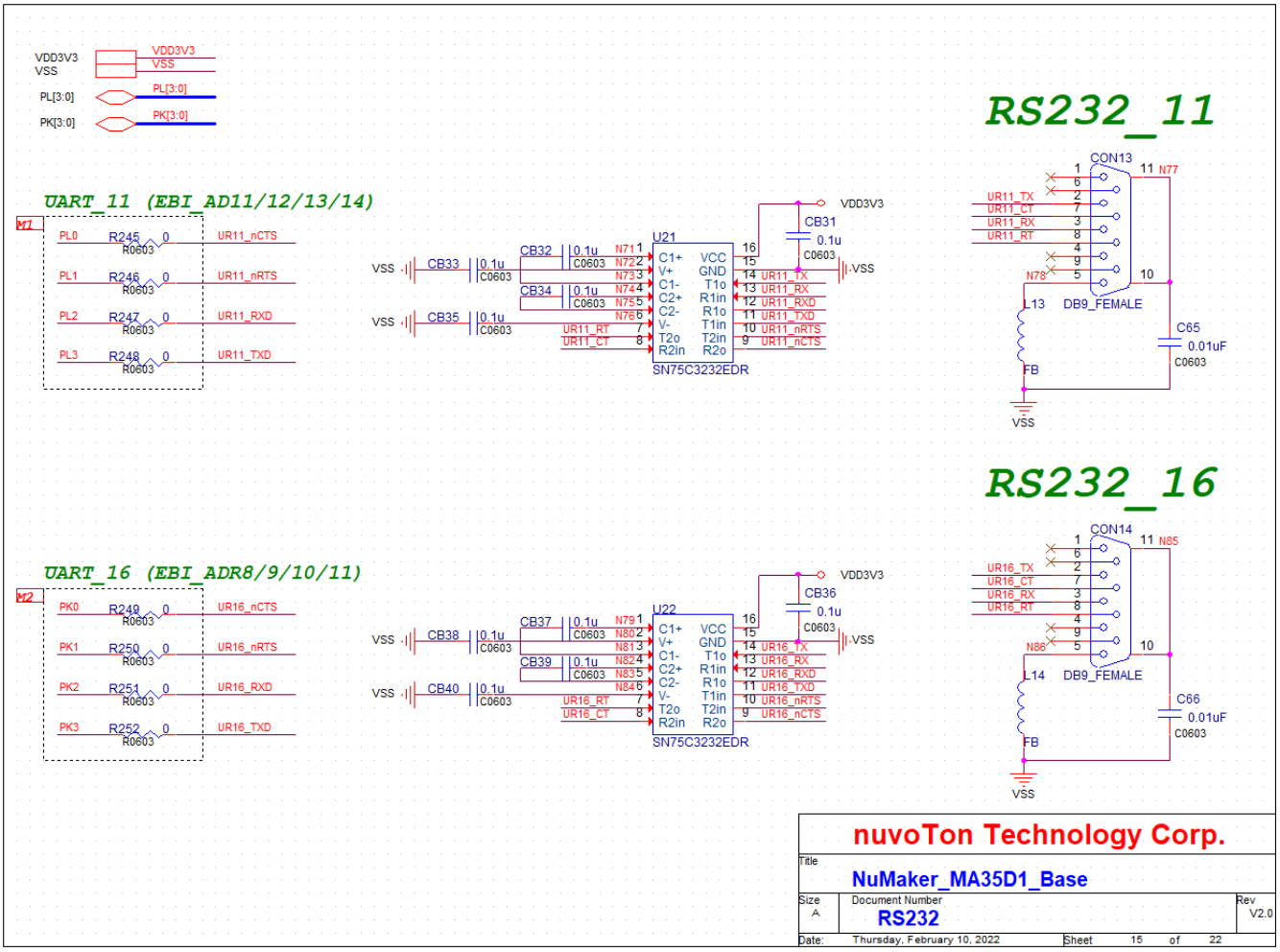

Figure 23-24 RS232 Circuit

23.25 RS485

Figure 23-25 shows the RS485 circuit.

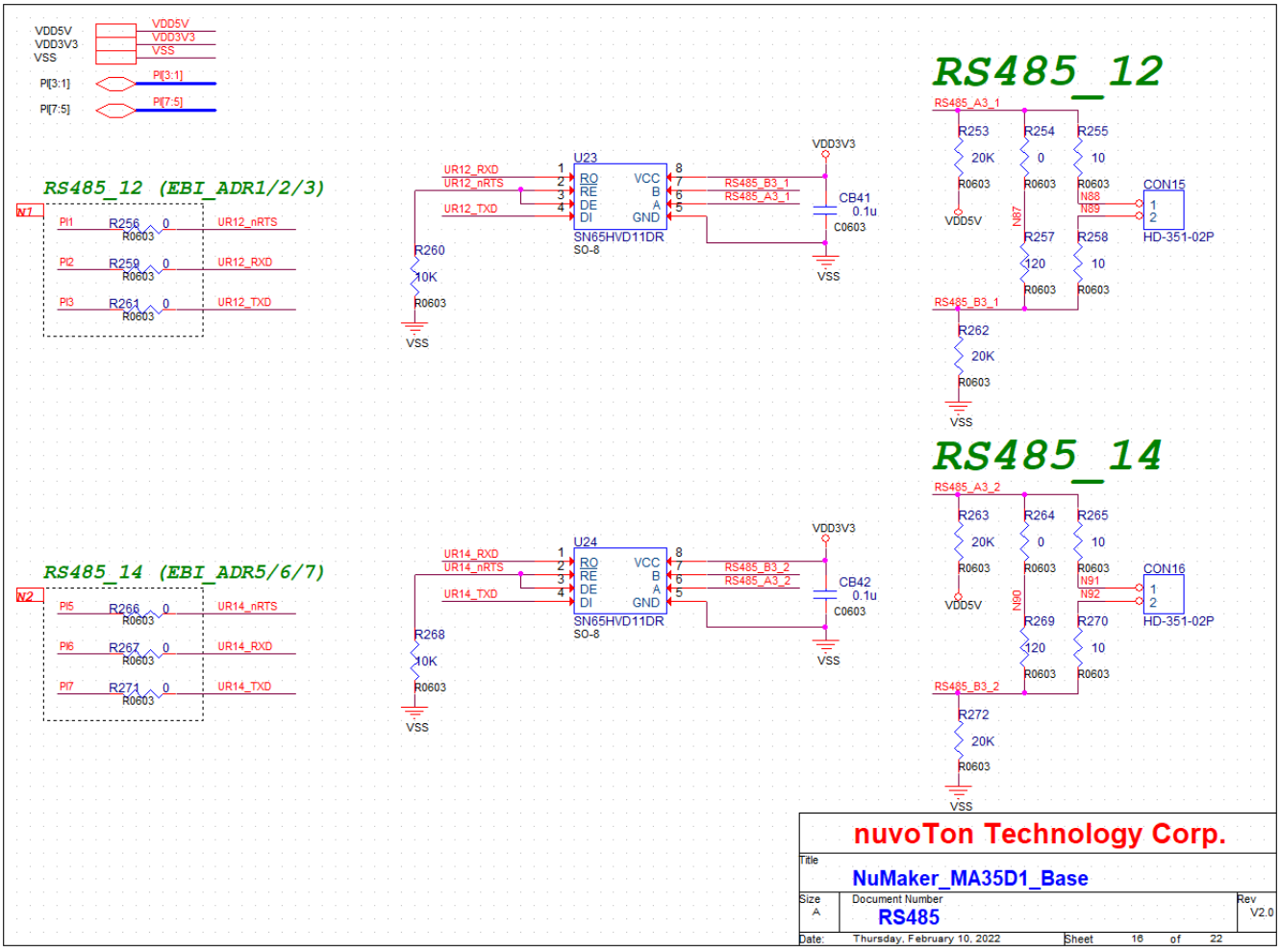

Figure 23-25 RS485 Circuit

23.26 CAN FD

Figure 23-26 shows the CAN FD circuit.

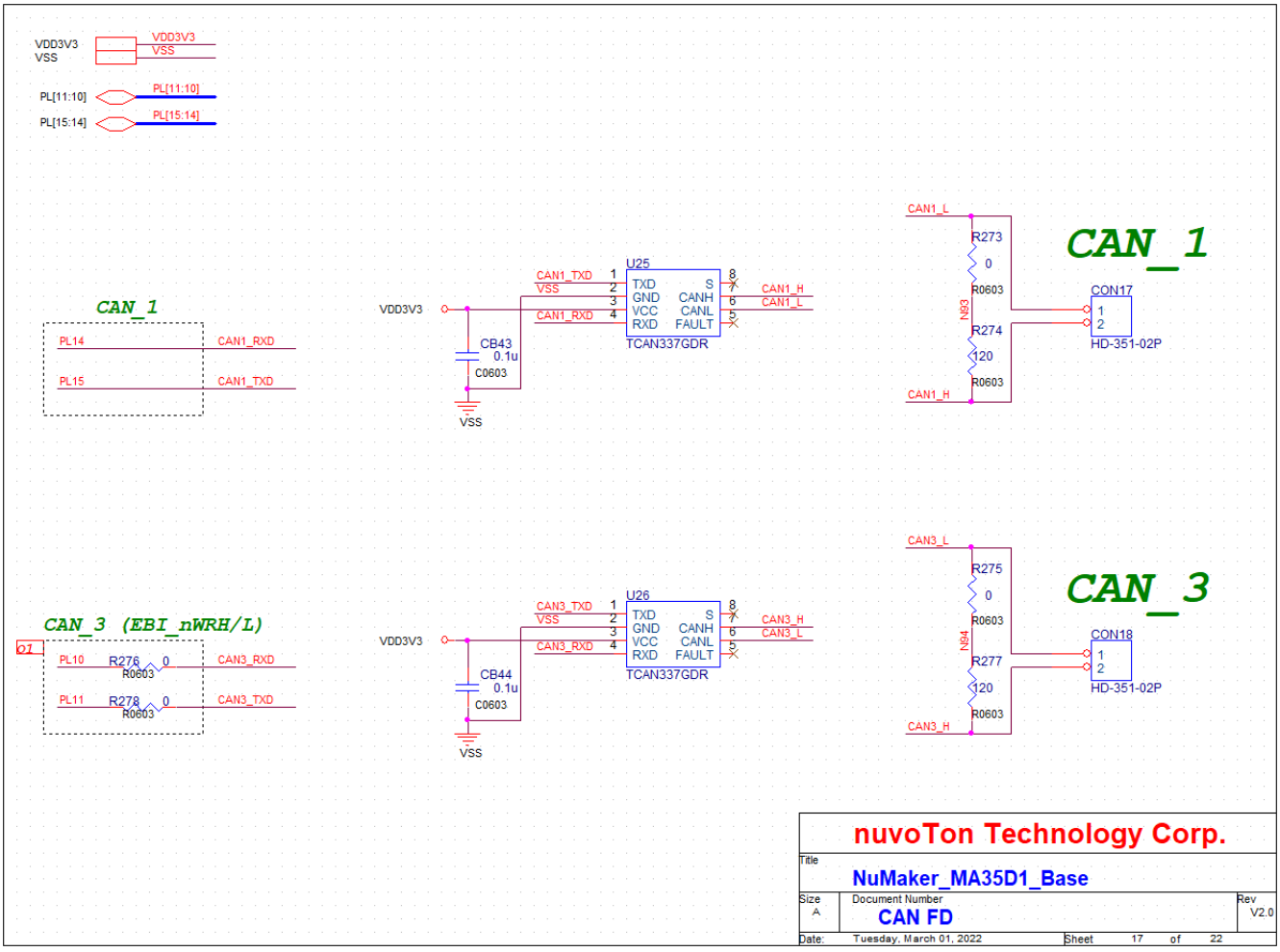

Figure 23-26 CAN FD Circuit

23.27 LED, Buzzer, Buttons

Figure 23-27 shows the LED, Buzzer, Buttons circuit.

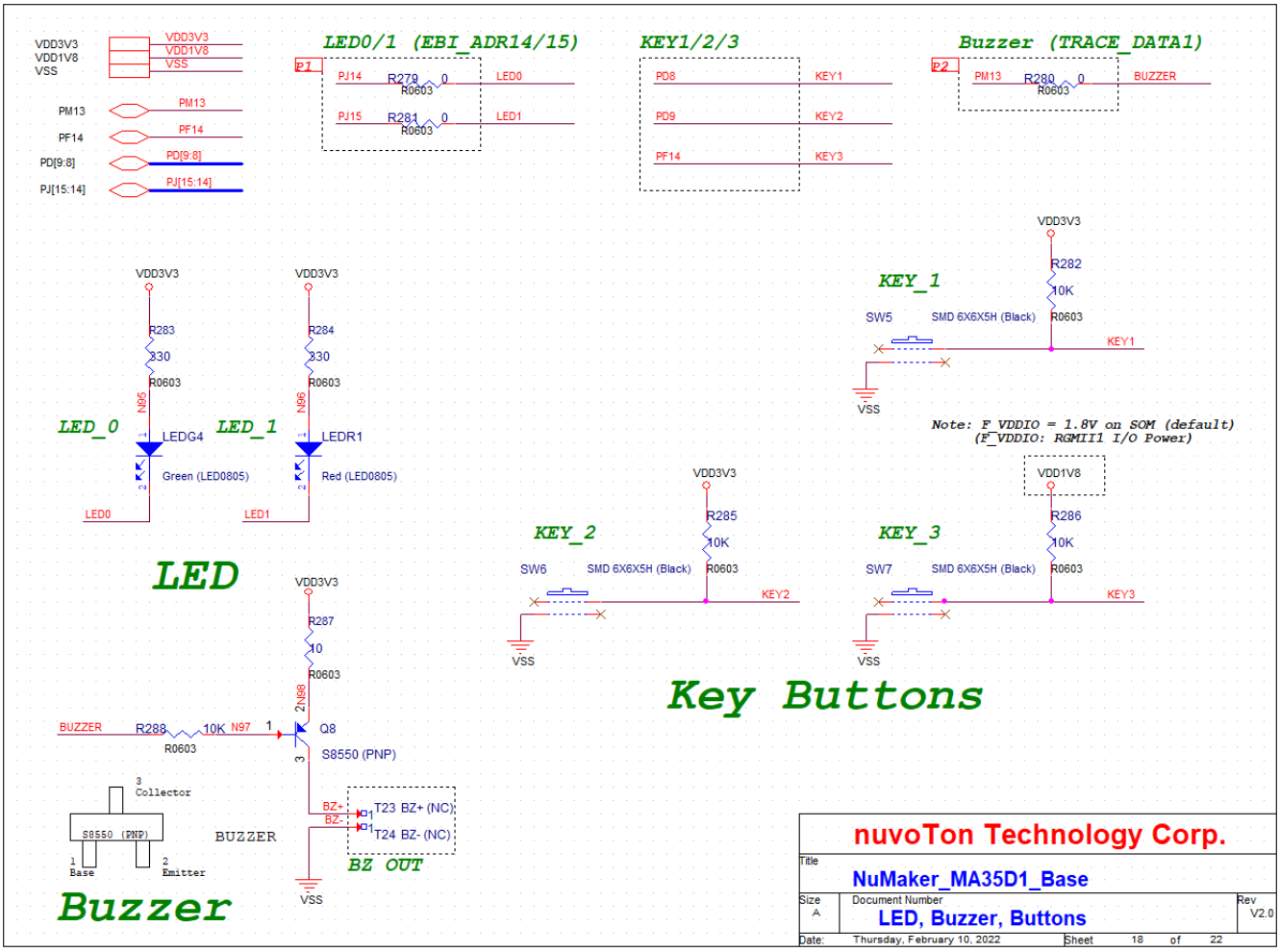

Figure 23-27 LED, Buzzer, Buttons Circuit

23.28 SWJ, SWD and ETM Connectors

Figure 23-28 shows the SWJ, SWD and ETM connectors circuit.

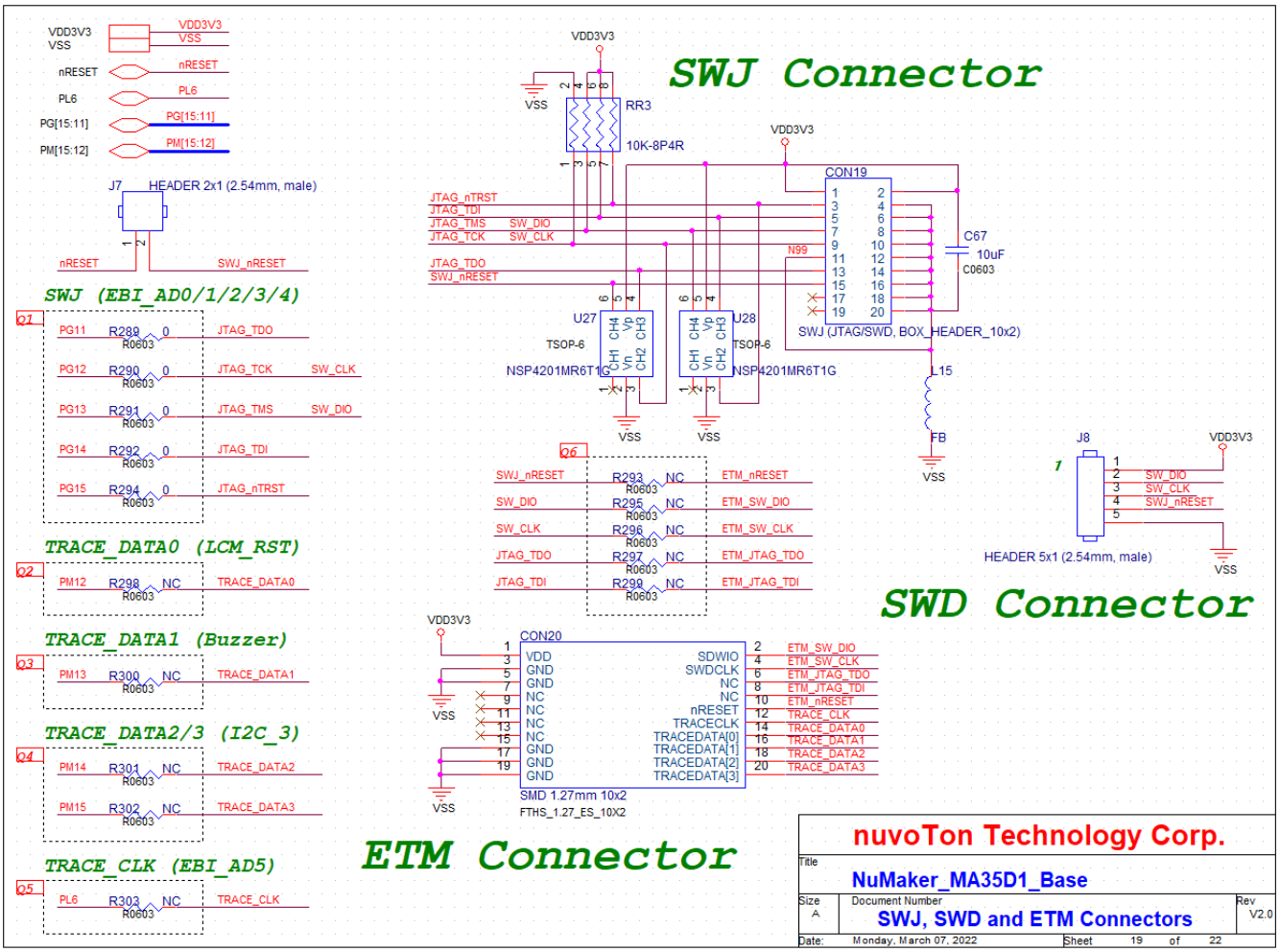

Figure 23-28 SWJ, SWD and ETM Connectors Circuit

23.29 NUC123 VCOM

Figure 23-29 shows the NUC123 VCOM circuit.

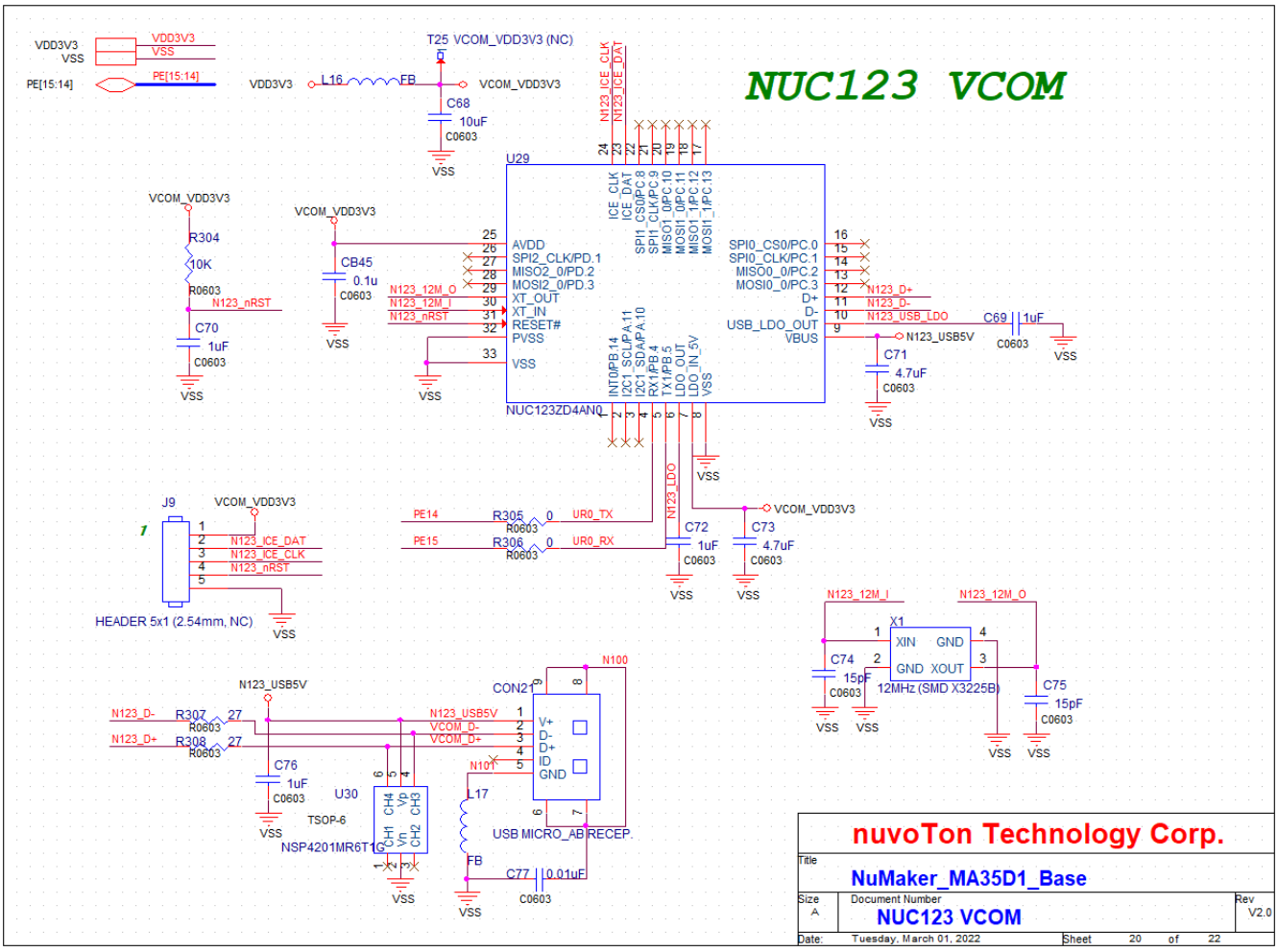

Figure 23-29 NUC123 VCOM Circuit

23.30 MEMS Digital MIC (MP34DT01-M)

Figure 23-30 shows the MEMS Digital MIC (MP34DT01-M) circuit.

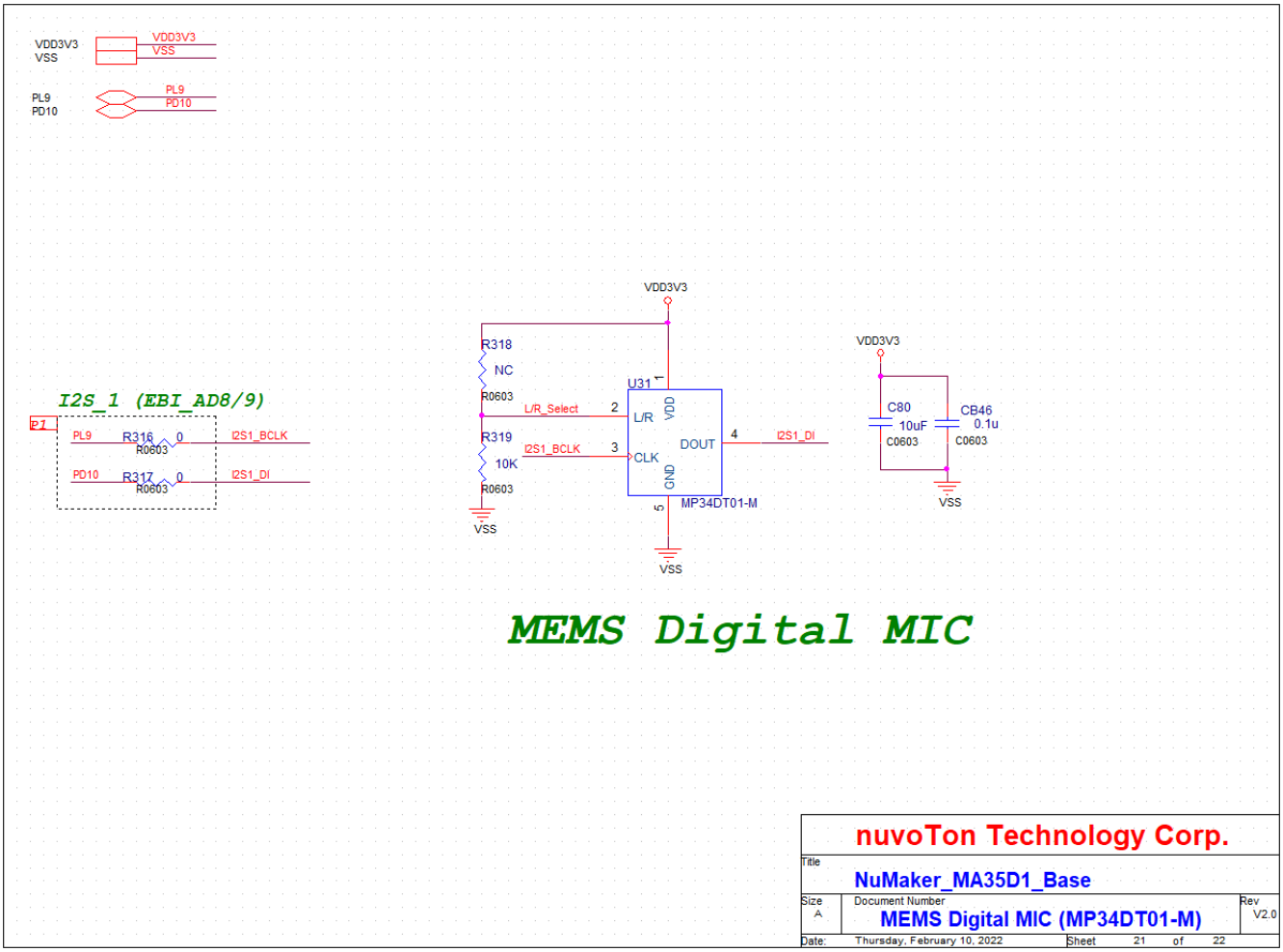

Figure 23-30 MEMS Digital MIC (MP34DT01-M) Circuit

23.31 MEMS G-Sensor (MPU6500)

Figure 23-31 shows the MEMS G-Sensor (MPU6500) circuit.

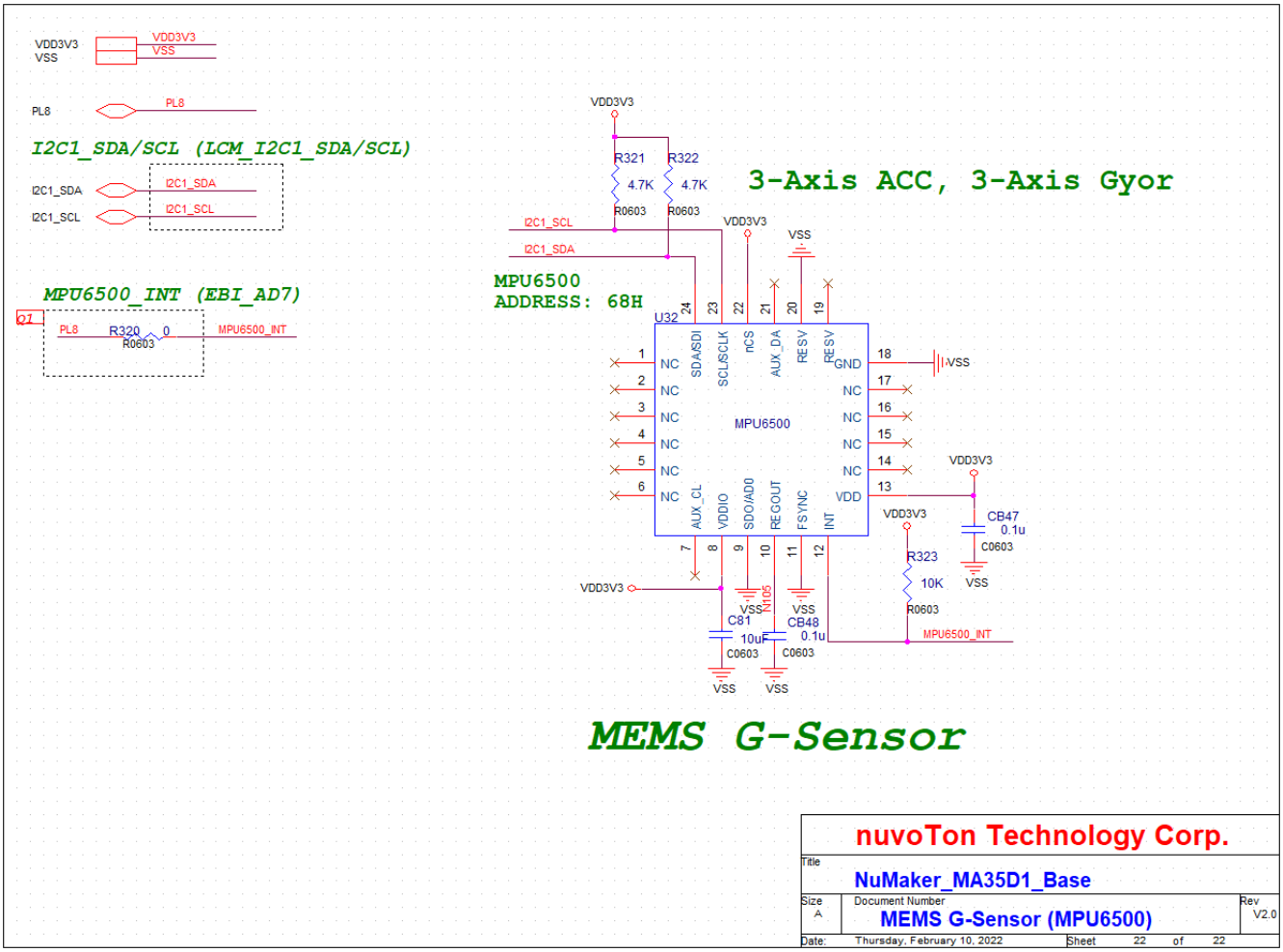

Figure 23-31 MEMS G-Sensor (MPU6500) Circuit

23.32 LCD

Figure 23-32 shows the LCD circuit.

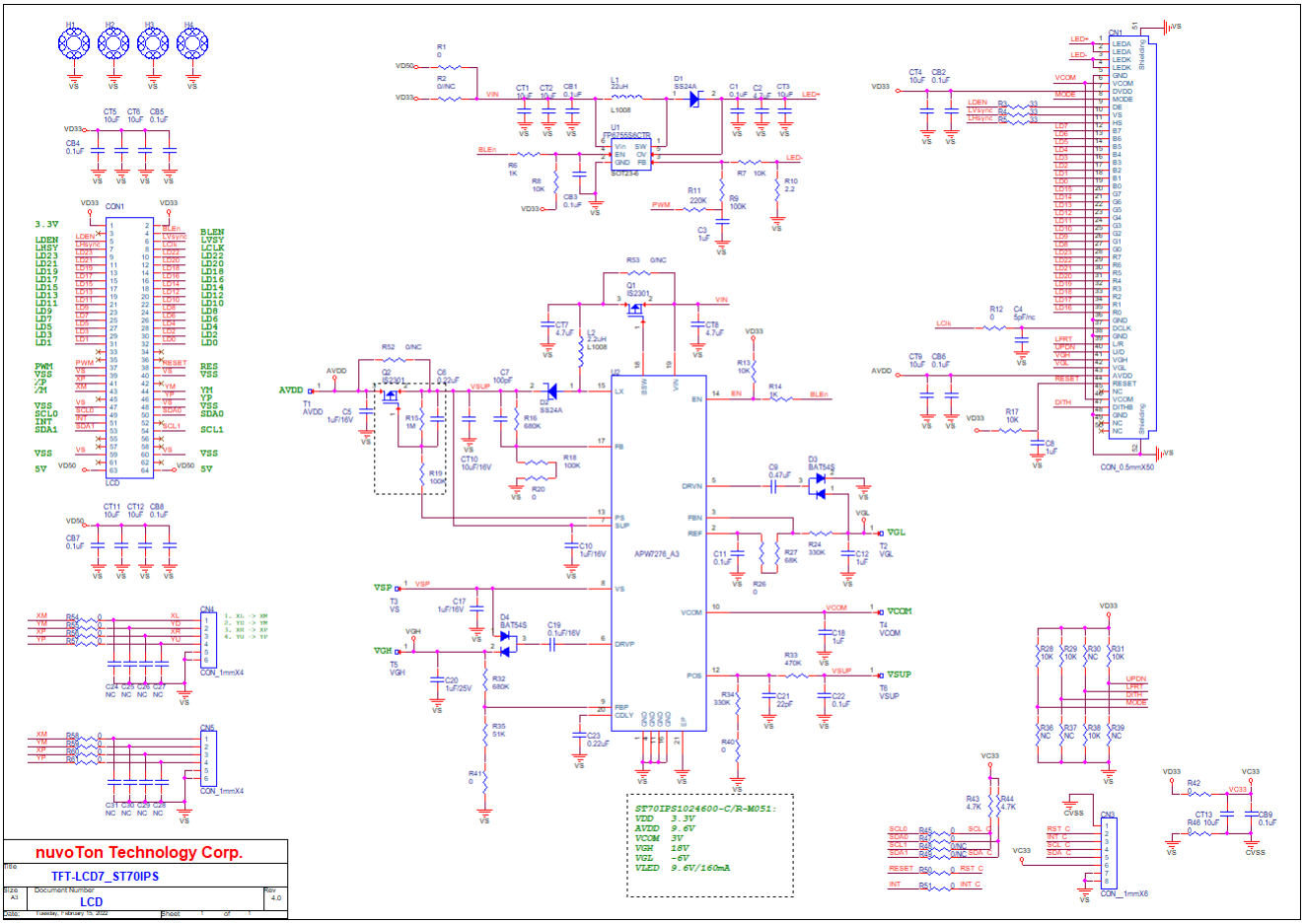

Figure 23-32 LCD Circuit

Revision History

Date	Revision	Description
2022.11.7	1.00	Initial version.
2023.3.31	1.01	Char.21 External DDR3/DDR3L Add: Series resistance on MDQS0_N/ MDQS0_P and MDQS1_N/ MDQS1_P

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.