NuMicro® Family

Arm® Cortex®-A35-based Microprocessor

MA35 Series
High Speed IP Calibration
User Manual

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MA35 SERIES HIGH SPEED IP CALIBRATION USER MANUAL

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1   OVERVIEW

IPTest_MA35_UI is a high-speed IP calibration tool for the MA35 series microprocessor, including MA35D1, MA35H0, and MA35D0. It communicates with MA35 through USB interface, allowing user to issue commands from a computer to test DDR parameters setting and SDH/ SPI high speed I/O drive strength.

2 INSTALLATION

IPTest_MA35_UI is released in executable form. The executable file can be executed directly without installation.

2.1 Install USB Driver

The USB VCOM driver must be installed on the computer to use the IPTest_MA35_UI tool. To install the USB VCOM driver, please follow the steps below:

Step 1: After connecting the computer and the MA35 through USB cable, after turning on the power of the MA35 series microprocessor, Windows will find a new USB device, and select the executable file *WinUSB4NuVCOM.exe* on the computer to start installing the driver. (Figure 2-1)
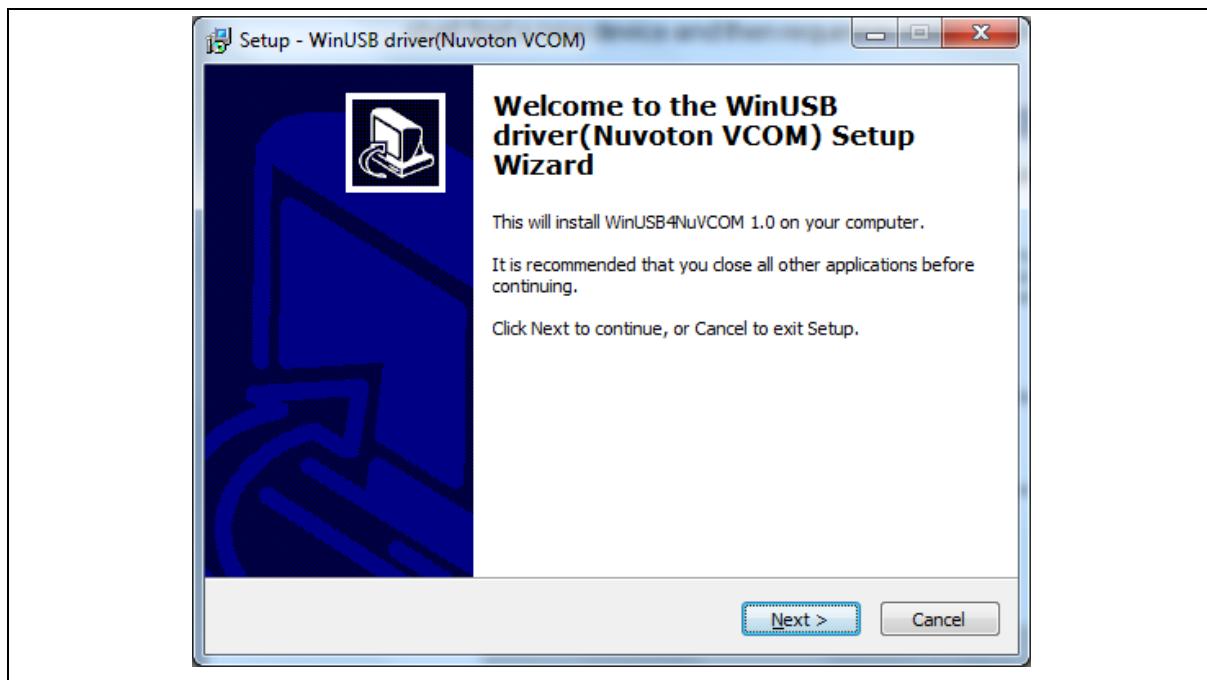

Figure 2-1 WinUSB4NuVCOM Driver Setup (1)

Step 2: Click "**Next**". This screen tells you that the WinUSB4NuVCOM 1.0 driver is about to be installed (Figure 2-2).
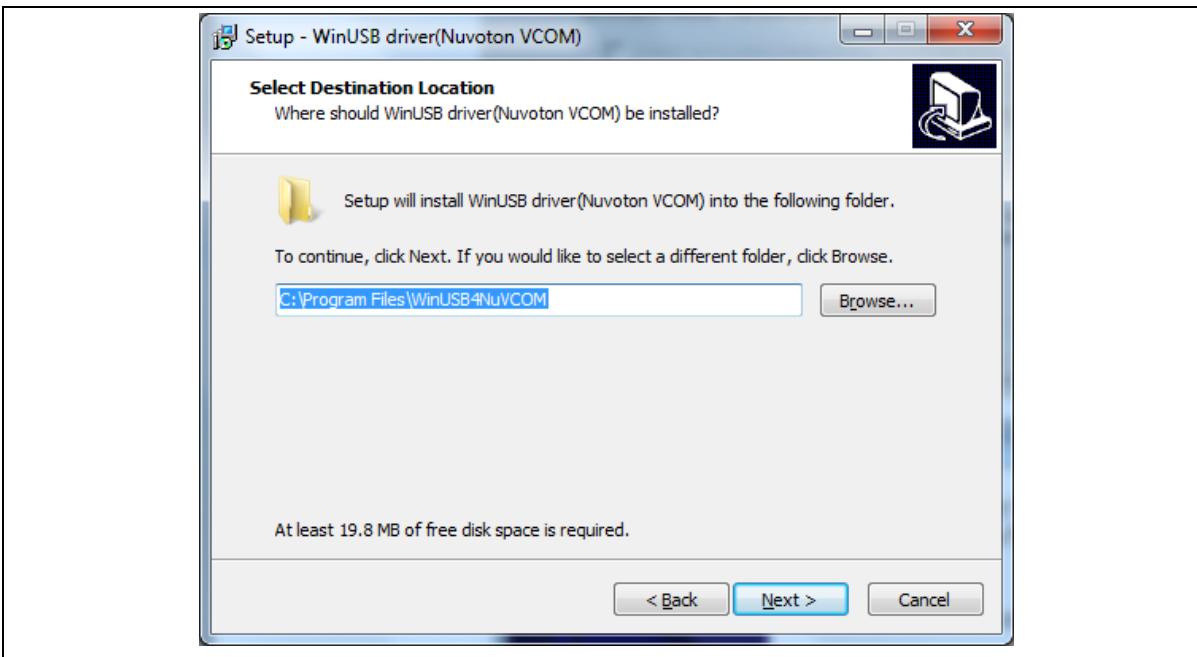
Figure 2-2 WinUSB4NuVCOM Driver Setup (2)

Step 3: Select the path the user wants to install or use the default path and click "**Next**" after confirming (Figure 2-3).
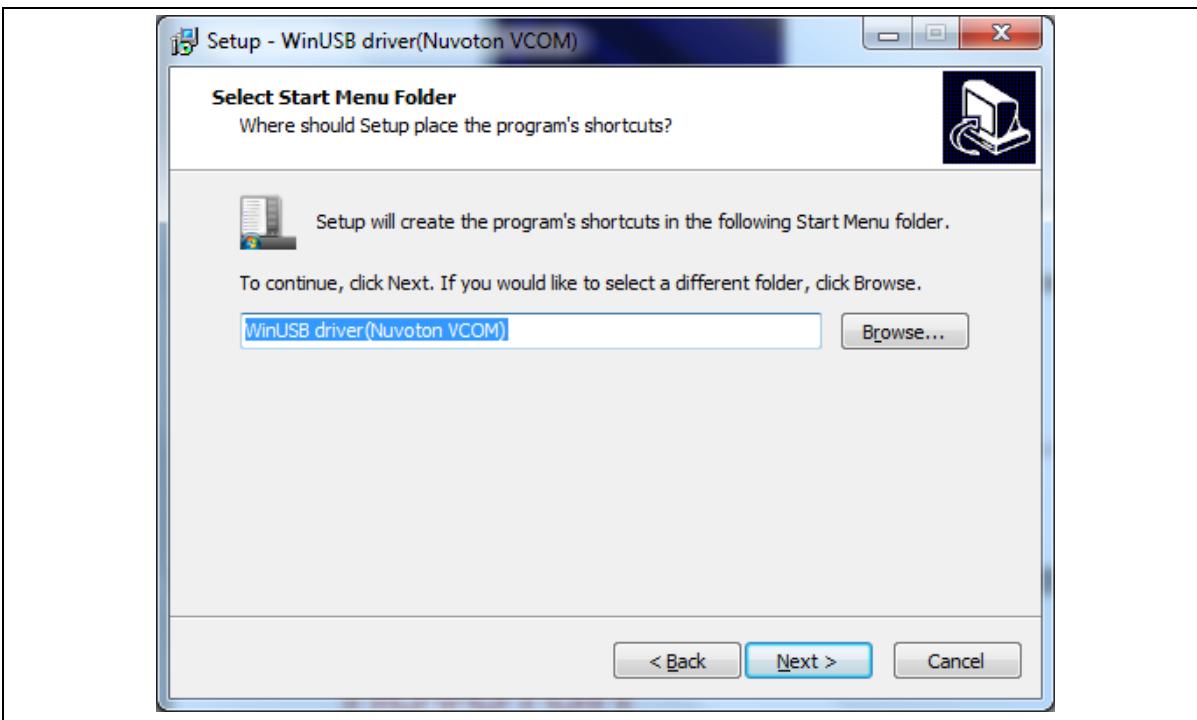

Figure 2-3 WinUSB4NuVCOM Driver Setup (3)

Step 4: Click "**Next**" (Figure 2-4).
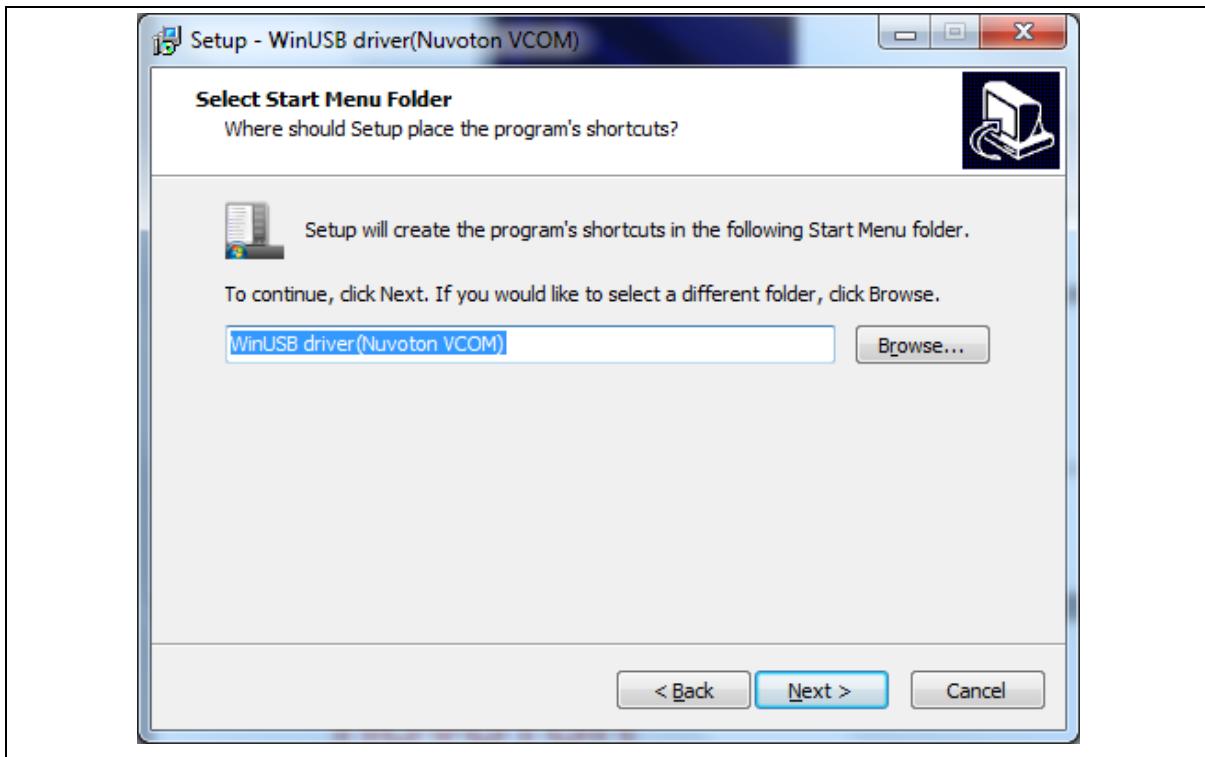
Figure 2-4 WinUSB4NuVCOM Driver Setup (4)

Step 5: Click "**Install**" (Figure 2-5).
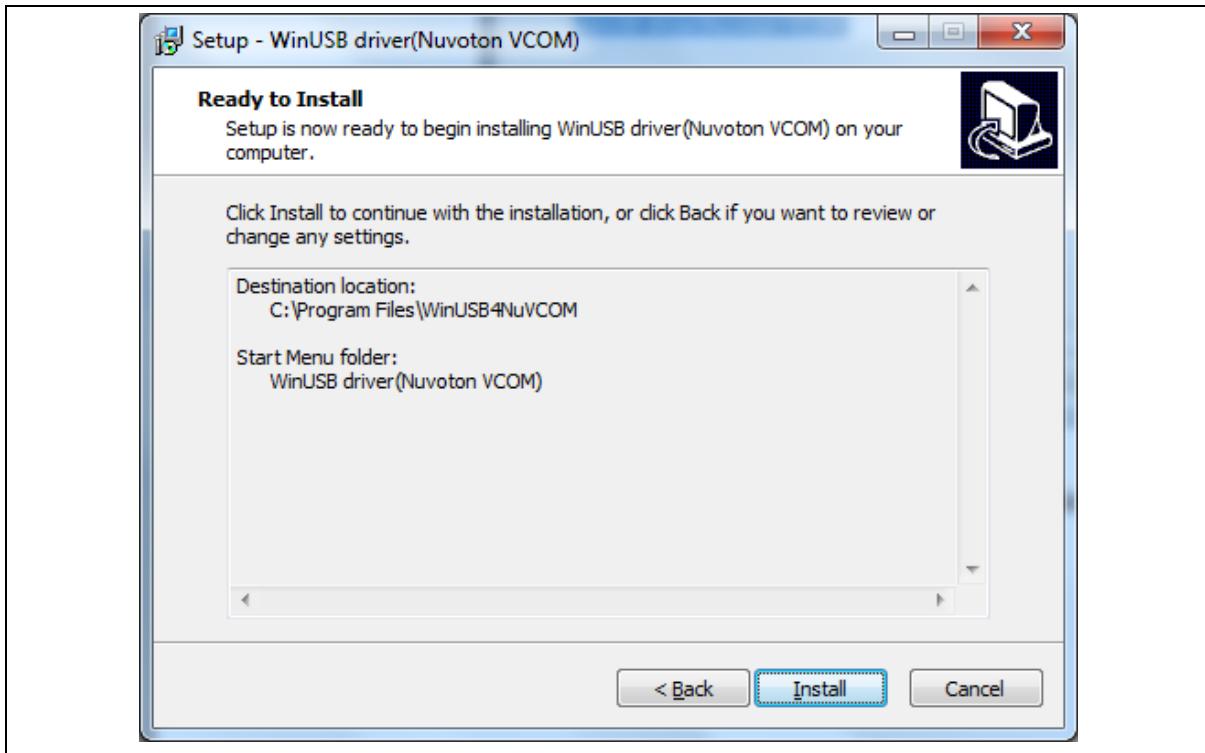
Figure 2-5 WinUSB4NuVCOM Driver Setup (5)

Step 6: Click "**Finish**" to complete the installation of the USB VCOM driver (Figure 2-6).
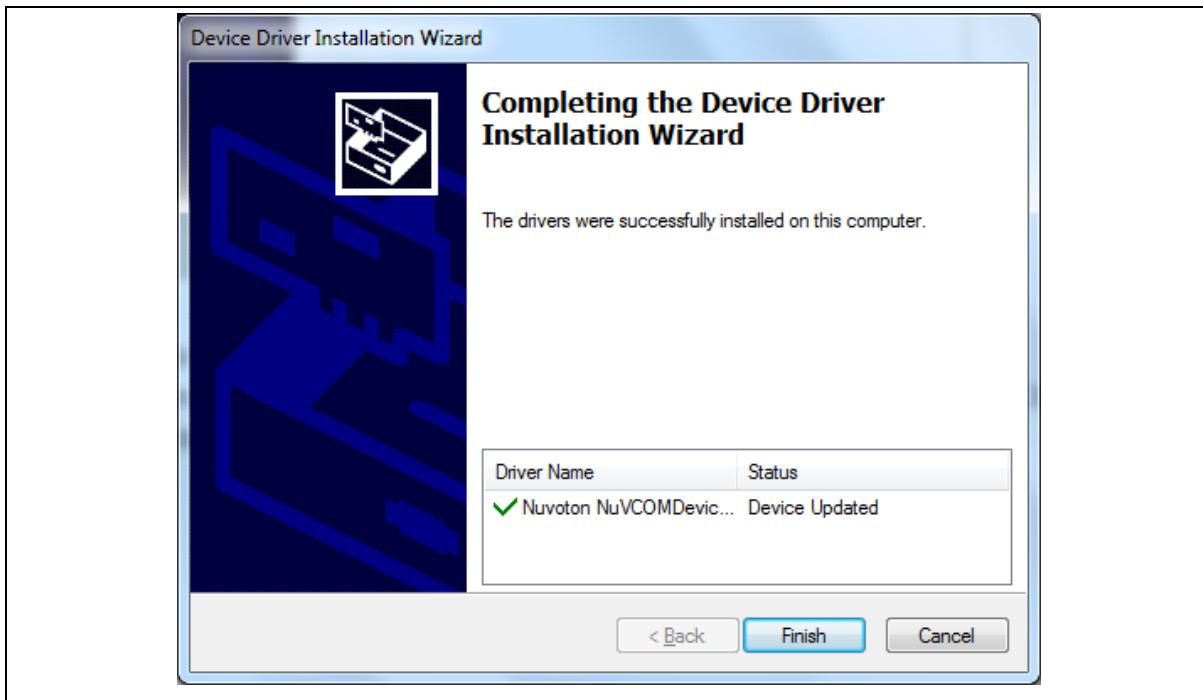
Figure 2-6 WinUSB4NuVCOM Driver Setup (6)

After the installation of the USB VCOM driver is successfully completed, the user can confirm that the Windows operating system should detect the new device and automatically load its corresponding USB settings. Users can see "WinUSB driver (Nuvoton VCOM)" in Device Manager, which means the driver is installed successfully as shown in Figure 2-7.
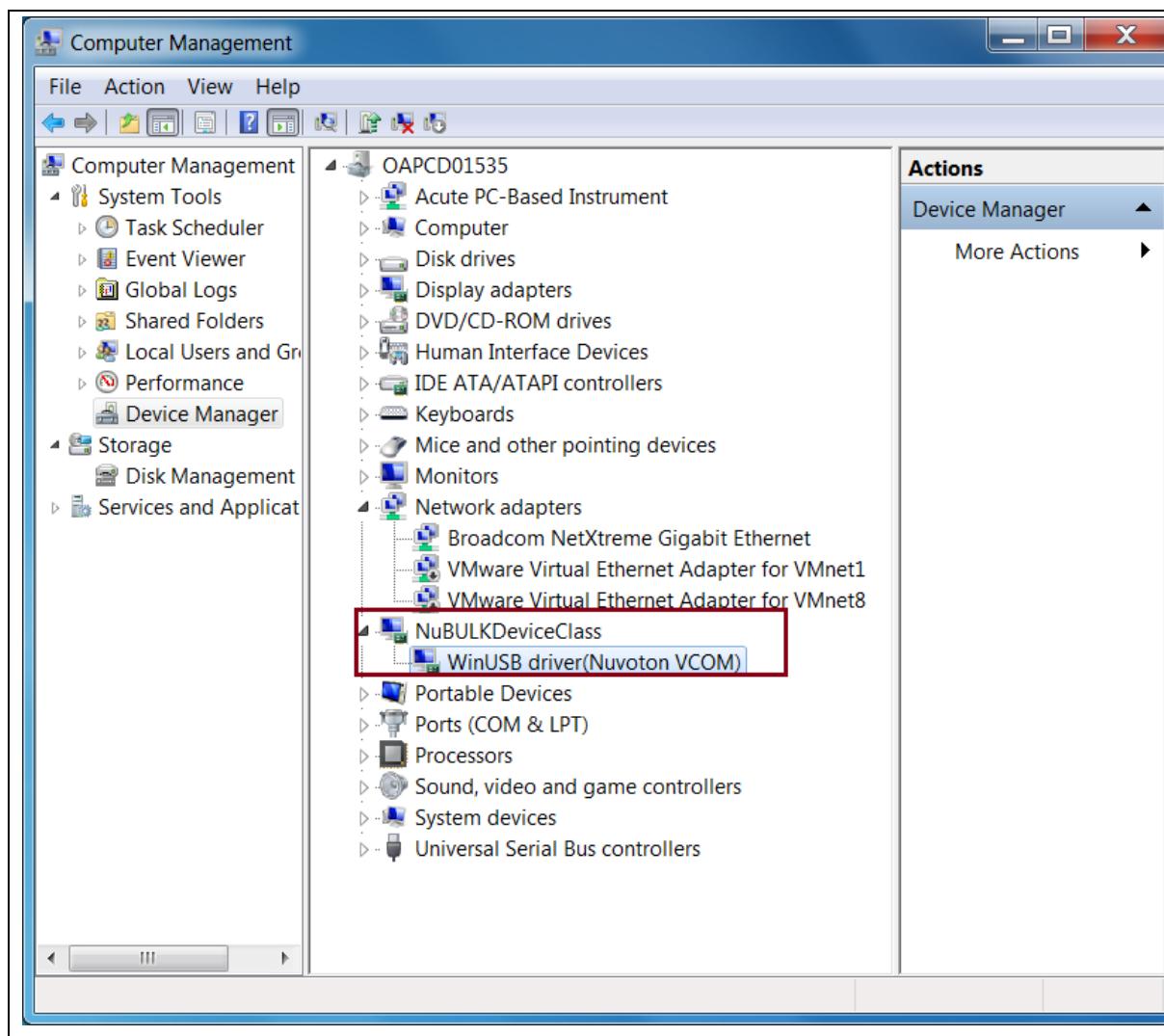
Figure 2-7 IPTest_MA35 VCOM Device

3 HARDWARE CONFIGURATION

3.1 Hardware Connection

The MA35 IBR is communicated with IPTest_MA35_UI through USB port 0. A USB cable should connect between MA35 series microprocessor and computer for the IPTest_MA35_UI tool to control MA35. The UART cable connects between the computer and MA35. UART0 is used to show debug messages printed by IPTest_MA35_UI firmware and is not used for data transfer between MA35 and computer. As an example, Figure 3-1 shows the USB device and UART interface on NuMaker-HMI-MA35D1 board.
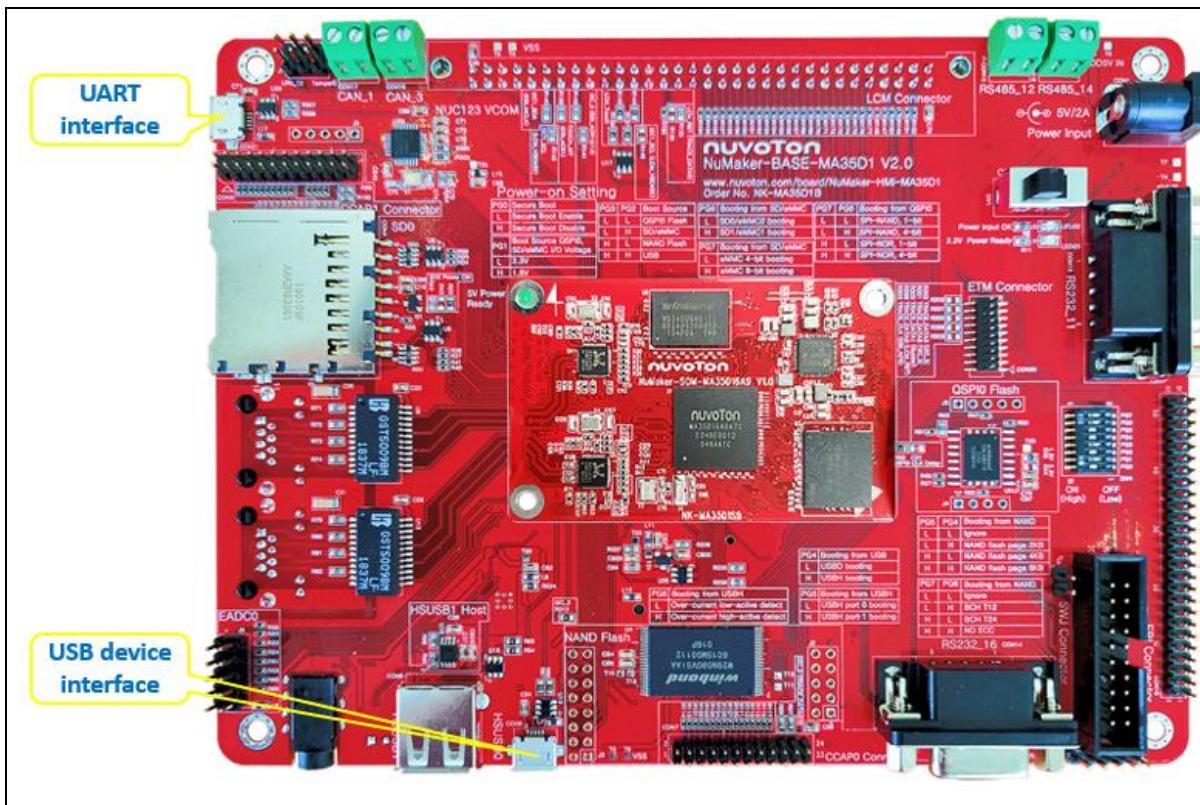
Figure 3-1 Board Connection

4 DDR CALIBRATION

4.1 DDR Parameters Setting

Nuvoton provides an Excel file – ddrmctl2_PAIS_Tool_v3.11.xlsm – to fill in the DDR parameters and then generate files for use by IpTest_MA35_UI and TFA. The Excel file has "How to use" tab for ease of use.

How to use	Revision History	Chip system parameters	DRAM timing parameters	Whole DDR settings

Figure 4-1 DDR Parameters Setting – 1

4.2 Chip System Parameters

Set DRAM type, size and data rate in this tab.

| Descriptions	User fills values	Units	Related items
Base Address of DDR memory controller	0x404d0000	Byte	
Base Address of DDR3/2 PHY	0x404c0000	Byte	
Frequency of APB interface clock of DDR memory controller and DDR3/2 PHY	90	MHz	tPCLK(ns) = 1000/(Frequency of APB interface clock of DDR memory controller and DDR3/2 PHY)
DDR DRAM types	DDR3		
DDR Data Rate	1066	MBPS	tCK(ns) = 2000/DDR Data Rate(MBPS)
DRAM size per device	256	MByte	Total DRAM size = (DRAM size (MBytes) per device) x (Number of ranks)
Number of ranks that system chip connects to used DRAM	1	Rank	
Bit number of bank address for used DRAM	3	Bit	
Bit number of row address for used DRAM	14	Bit	
Bit number of column address for used DRAM	10	Bit	
Output driver impedance for used DDR2	-	ohm	valid values : DDR2 : Normal(100%), Weak(60%)
ODT(On Die Termination) for used DDR2	-	ohm	valid values : DDR2 : Disable, 75, 150, and 50
Output driver impedance for DDR2 PHY	-	ohm	valid values : DDR2 : 40
ODT(On Die Termination) for DDR2 PHY	-	ohm	valid values : DDR2 : 150, 75, and 50
Output driver impedance for used DDR3	34	ohm	RZQ = 240 (ohm) +/- 1%, valid values : DDR3 : RZQ/6 and RZQ/7
ODT(On Die Termination) for used DDR3	60	ohm	RZQ = 240 (ohm) +/- 1%, valid values : DDR3 : Disable, RZQ/4, RZQ/2, RZQ/6, RZQ/12, and RZQ/8
Output driver impedance for DDR3 PHY	34	ohm	RZQ = 240 (ohm) +/- 1%, valid values : DDR3 : 40 and 34
ODT(On Die Termination) for DDR PHY	60	ohm	RZQ = 240 (ohm) +/- 1%, valid values : DDR3 : 120, 60, and 40
Write leveling training function (only for DDR3 DRAM)	Disable		Write leveling training function (only for DDR3 DRAM): Enable, Disable

Figure 4-2 DDR Parameters Setting – 2

4.3 DRAM Timing Parameters

Set DRAM Timing in this tab.

DRAM timing parameter	Descriptions	DRAM type for this item	User fills values from DRAM data sheet — tCK (clock period of DRAM input clock)	ns	Final used DRAM parameter value — Units : tCK (clock period of DRAM input clock)	Reset
			Command and Address Timing			
CL	CAS Latency	DDR2/DDR3	8		8	
CWL	CAS Write Latency	DDR3 ONLY	6	-	6	
tRCD	ACT to internal read or write delay time	DDR2/DDR3	-	13.5	7	
tRP	PRE command period	DDR2/DDR3	-	13.5	7	
tRC	ACT to ACT or REF command period	DDR2/DDR3	-	49.5	26	
tRAS_max	Maximum period of ACT to PRE command	DDR2/DDR3	-	17550	9354	
tRAS_min	Minimum period of ACT to PRE command	DDR2/DDR3	-	36	19	
tDLLK	DLL locking time	DDR3 ONLY	512		512	
tRTP	Internal READ Command to PRECHARGE Command delay	DDR2/DDR3	4	7.5	4	
tWTR	Delay from start of internal write transaction to internal read command	DDR2/DDR3	4	7.5	4	
tWR	WRITE recovery time	DDR2/DDR3	-	15	8	
tMRD	Mode Register Set command cycle time	DDR2/DDR3	4	-	4	
tMOD	Mode Register Set command update delay	DDR3 ONLY	12	15	12	
tCCD	CAS# to CAS# command delay	DDR2/DDR3	4	-	4	
tRRD	ACTIVE to ACTIVE command period for 2KB page	DDR2/DDR3	4	7.5	4	
tFAW	Four activate window for 2KB page size	DDR2/DDR3	-	45	24	
			Calibration Timing (ONLY for DDR3)			
tZQinit	Power-up and RESET calibration time	DDR3 ONLY	512	640	512	
tZQoper	Normal operation Full calibration time	DDR3 ONLY	256	320	256	
tZQCS	Normal operation Short calibration time	DDR3 ONLY	64	80	64	
			Self Refresh Timing			
tXS	Exit Self Refresh to commands not requiring a locked DLL	DDR3 ONLY	5	170	91	
tXSDLL	Exit Self Refresh to commands requiring a locked DLL	DDR3 ONLY	512	-	512	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE)	DDR3 ONLY	5	10	5	
tCKSRX	Valid Clock Requirement after Self Refresh Exit (SRX)	DDR3 ONLY	5	10	5	
tXSNR	Exit Self Refresh to a non-Read command	DDR2 ONLY	-	-	#VALUE!	
tXSRD	Exit Self Refresh to a Read command	DDR2 ONLY	-		-	
			Refresh Timing			
tRFC	REF command to ACT or REF command time	DDR2/DDR3	-	160	85	
tREFI	Average periodic refresh interval	DDR2/DDR3	-	1950	1039	
			Power Down Timing			
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge	DDR2/DDR3	3	6	3	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a	DDR2/DDR3	10	24	13	
tCKE	CKE minimum pulse width	DDR2/DDR3	3	5.625	3	
tXARD	Exit active power down to Read command	DDR2 ONLY	-	-	-	
tXARDS	Exit active power down to Read command (slow exit, lower power)	DDR2 ONLY	-		-	
			Write Leveling Timing (ONLY for DDR3)			
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	DDR3 ONLY	40		40	
tWLO	Write leveling output delay	DDR3 ONLY	9		5	

Figure 4-3 DDR Parameters Setting – 3

4.4 Whole DDR Settings

Set all DDR control registers in this tab. Click "**Cal & Gan**" to generate the DDR initial file – ddr_init.txt.

Register name	Register Address Offset	Field register name	Calculation Equation (DEC)/Method	Setting value of Field registers(HEX)	Setting value of registers(HEX)	
			Register settings of DDR memory controller (UMCTL2) (Base Address = 0x404d0000)			Cal & Gen
DBG1[31:0]	0x304	Reserved[31:2]	0	0x0	0x00000001	
		dis_hif[1]	0	0x0		
		dis_dq[0]	1	0x1		
PWRCTL[31:0]	0x30	Reserved[31:8]	0	0x0	0x00000001	Reset
		dis_cam_drain_selfref[7]	0	0x0		
		Reserved[6]	0	0x0		
		selfref_sw[5]	0	0x0		
		Reserved[4]	0	0x0		
		en_dfi_dram_clk_disable[3]	0	0x0		
		Reserved[2]	0	0x0		
		powerdown_en[1]	0	0x0		
		selfref_en[0]	1	0x1		
MSTR[31:0]	0x0	Reserved[31:26]	0	0x0	0x01040001	
		active_ranks[25:24]	1	0x1		
		Reserved[23:20]	0	0x0		
		burst_rdwr[19:16]	4	0x4		
		dll_off_mode[15]	0	0x0		
		Reserved[14]	0	0x0		
		data_bus_width[13:12]	0	0x0		
		Reserved[11]	0	0x0		
		en_2t_timing_mode[10]	0	0x0		
		burstchop[9]	0	0x0		
		Reserved[8:1]	0	0x0		
		ddr3[0]	1	0x1		

Figure 4-4 DDR Parameters Setting – 4

4.5   DDR Calibration Tool

Open the IpTest_MA35_UI.exe. Click "**Load DDR firmware**" to do DDR calibration.
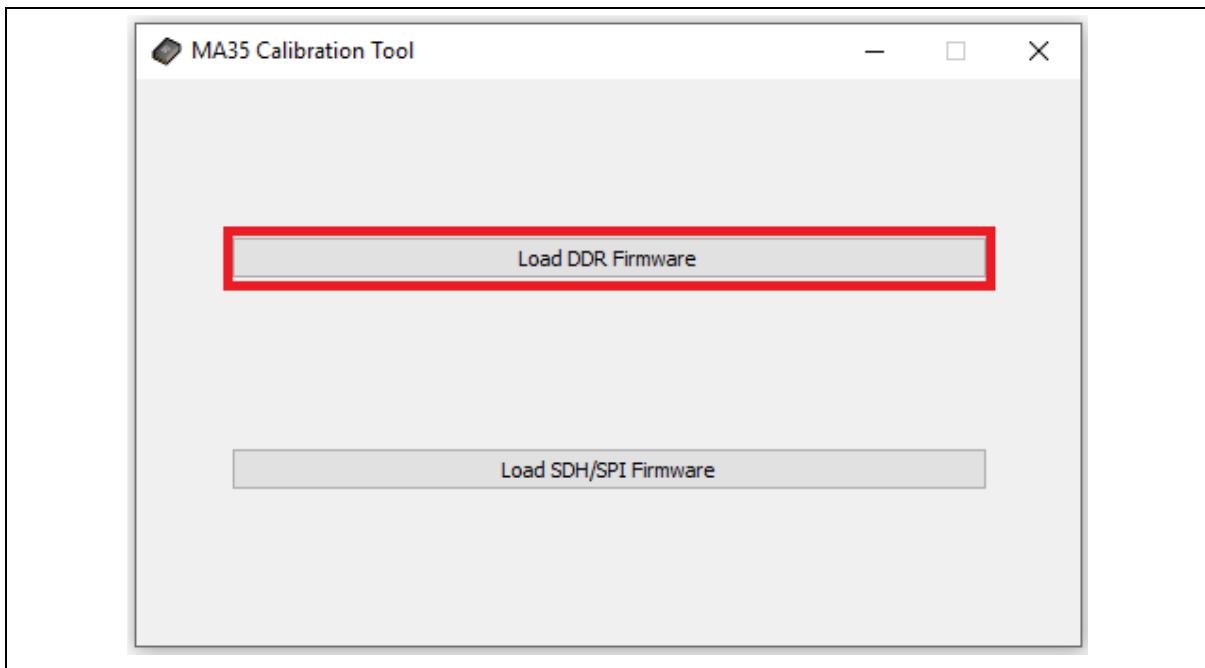
Figure 4-5 DDR Calibration – 1

- Step 1: Browse the ddr_init.txt.
- Step 2: Click "**Start Convert**".
- Step 3: Click "**Start Attach**".
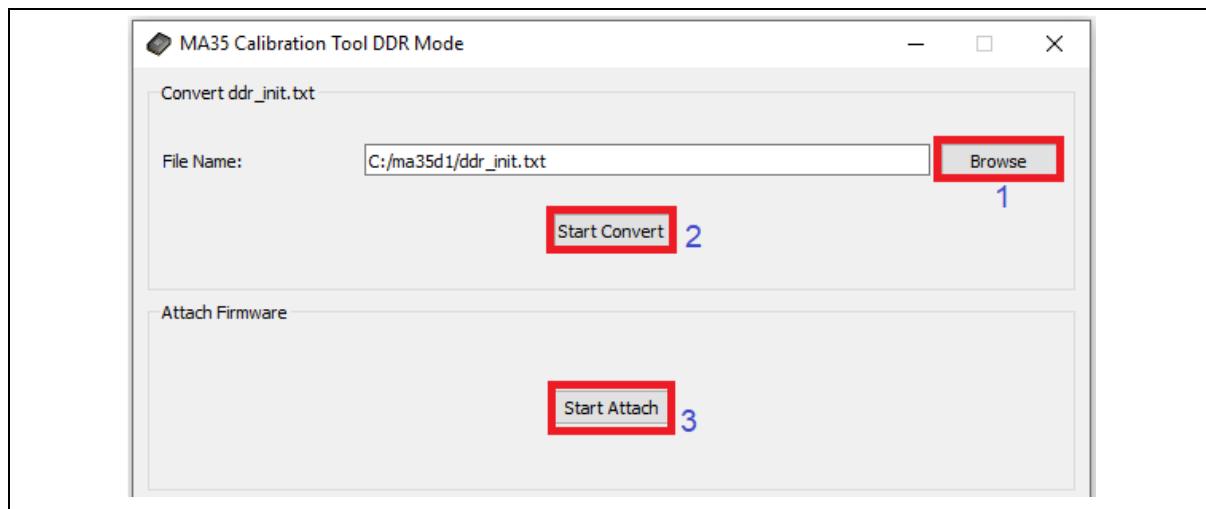
Figure 4-6 DDR Calibration – 2

- Step 1: Browse the ddr.bin.
- Step 2: Set test length, 0x10000 for example.
- Step 3: Set test data rate. Default is 1066 mbps.
- Step 4: Click "**Start Calibration**".
- Step 5: The test result is shown in output window.

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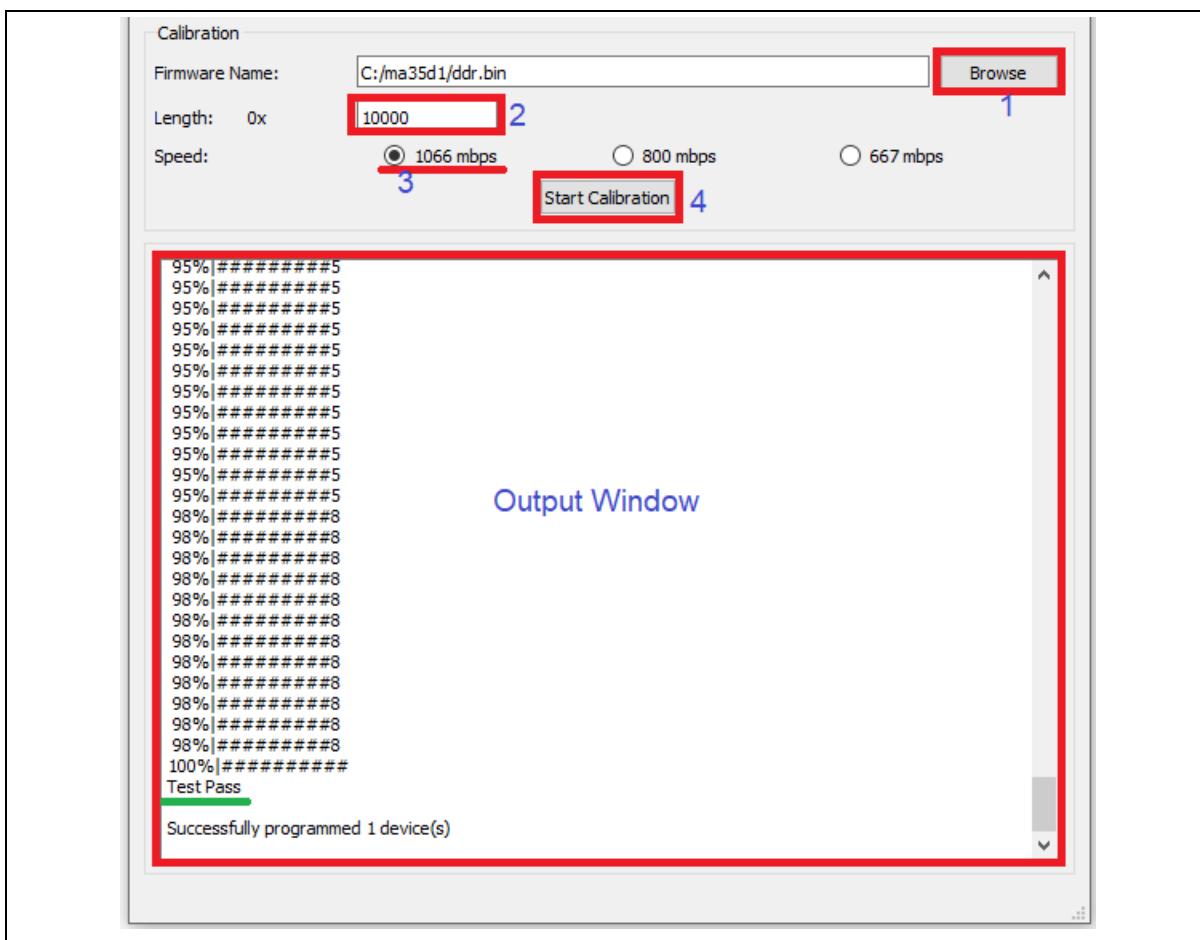
Figure 4-7 DDR Calibration – 3

5 SDH/SPI I/O DRIVE STRENGTH

This test program should be loaded and run in DDR. Before loading firmware, please do DDR initialization. Here is the attached command format where DDR_INIT is the DDR initialize code match the MA35 series microprocessor part.

The DDR type of MA35 series MCP package supports MA35D03F767C, MA35D03F867C, MA35D16A887C, MA35D16F787C, MA35D16F887C, MA35D16F987C, MA35D16H887C, and MA35H04F767C. Please select the DDR firmware corresponding to the MA35 chip on target board.
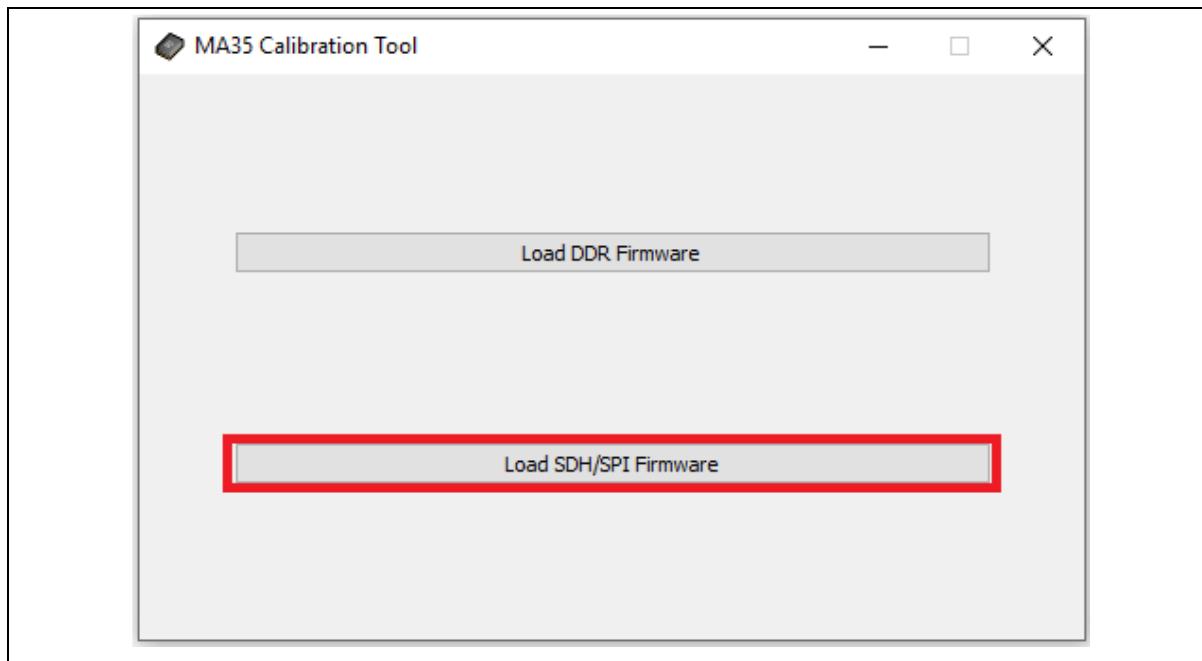

Figure 5-1 High Speed IP Calibration – 1

- Step 1: Browse the suitable DDR initial file.
- Step 2: Click "**Start Attach**".
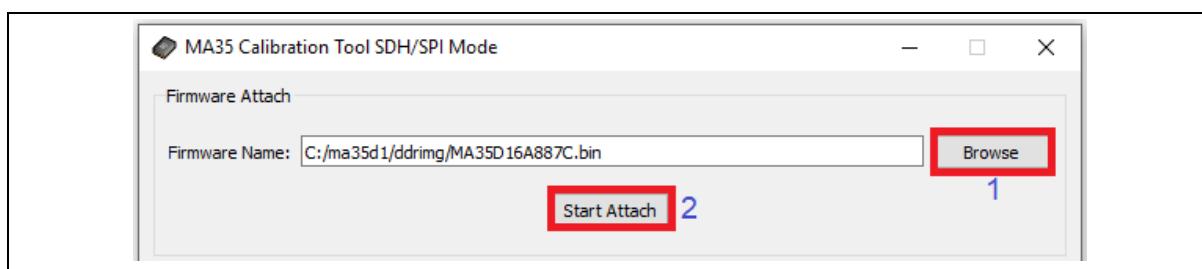
Figure 5-2 High Speed IP Calibration – 2

5.1 SPI

Use this program to test I/O drive strength.

- Step 1: Click "**SPI**".
- Step 2: Click "**Start Calibration**".
- Step 3: The test result is shown in output window.

The test result is: Row is MRxPhase (SPIx_Internal[16:12]). Column is GPIO drive strength (PD_DSL). 'o' means pass, and 'x' means fail. In Figure 5-3, the suitable value is MRxPhase = 0x3, and I/O drive strength = 0x4. The value of PD_DSL register = 0x0044444.
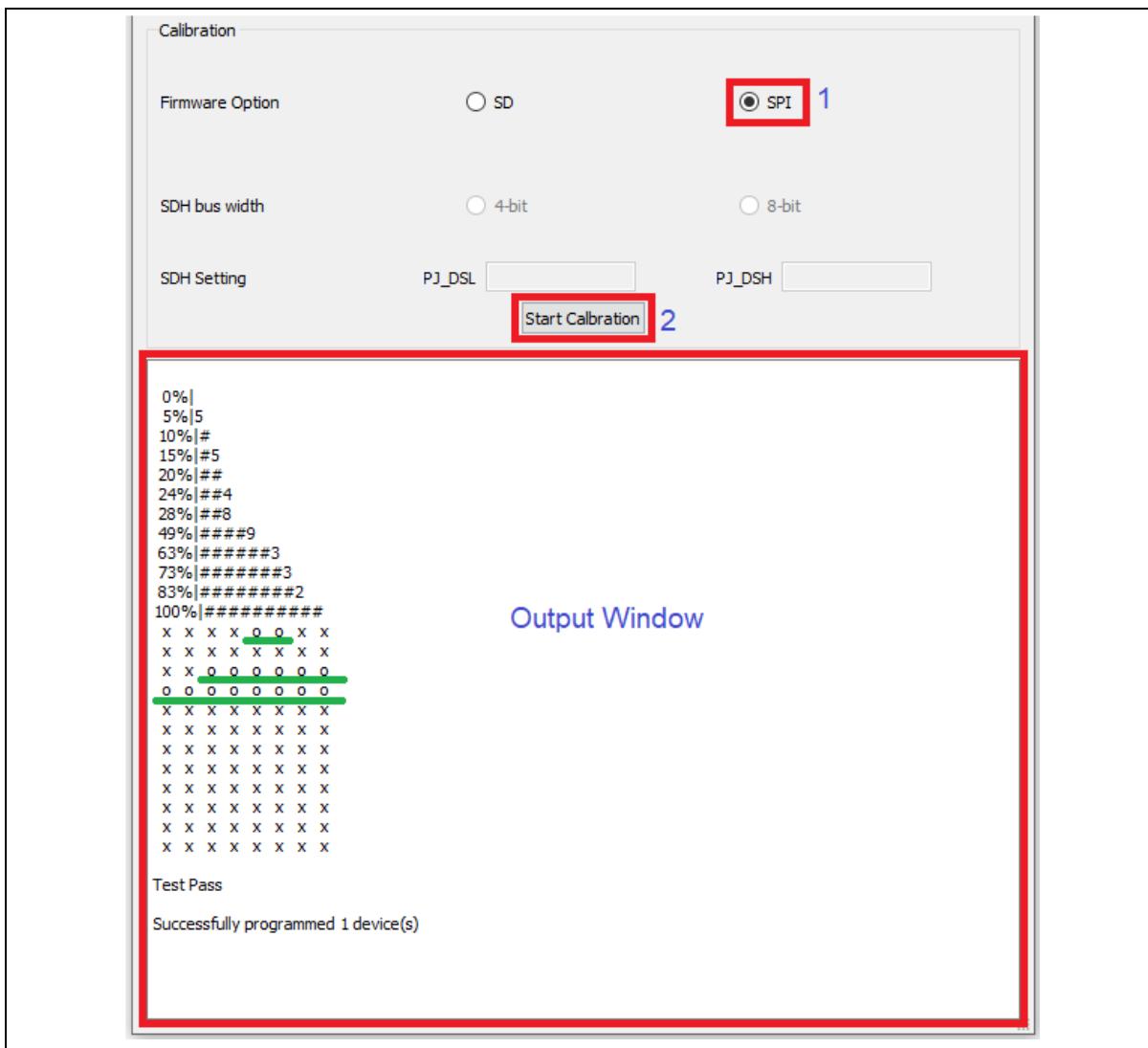

Figure 5-3 SPI Calibration

The above output window shows the suitable value is MRxPhase = 0x3, and I/O drive strength = 0x4.

Apply the two settings to Linux device tree. First, modify the value of "mrxphase" in qspi0 from default value 0 to 3. Then, modify QSPI pinctrl settings in device tree to change GPIO driving strength. Since I/O drive strength should be 4 per calibration result, set QSPI0 PD0~5 GPIO driving strength to 4.

```
    qspi0
    {
        pinctrl_qspi0: qspi0grp{
            nuvoton,pins =
                    <SYS_GPD_MFPL_PD0MFP_QSPI0_SS0        &pcfg_spi_drive4_1_8V>,
                    <SYS_GPD_MFPL_PD1MFP_QSPI0_CLK        &pcfg_spi_drive4_1_8V>,
```

```
                    <SYS_GPD_MFPL_PD2MFP_QSPI0_MOSI0      &pcfg_spi_drive4_1_8V>,
                    <SYS_GPD_MFPL_PD3MFP_QSPI0_MISO0      &pcfg_spi_drive4_1_8V>,
                    <SYS_GPD_MFPL_PD4MFP_QSPI0_MOSI1      &pcfg_spi_drive4_1_8V>,
                    <SYS_GPD_MFPL_PD4MFP_QSPI0_MOSI1      &pcfg_spi_drive4_1_8V>,
          };
        };
```

5.2   SDH

MA35 series microprocessor only has one SD high speed port – SDH1. Use this program to test I/O drive strength. Default bus width is 4-bit.

- Step 1: Click "**SD**".

- Step 2: Click bus width. Default is 4-bit.

- Step 3: Set I/O drive strength.

- Step 4: Click "**Start Calibration**".

- Step 5: The test result is shown in output window.

The test result is: Row is CMD I/O drive strength (PJ_DSL[26:24]). Column is DATA I/O drive strength (PJ_DSL and PJ_DSH). 'o' means pass, and 'x' means fail. In Figure 5-4, the suitalble I/O drive strength for CLK is 0x1 ~ 0x5. The suitable I/O drive strength of CMD and DATA is 0x0 ~ 0x7. Select the middle value: PJ_DSL is 0x33003333, PJ_DSH is 0x00003333.

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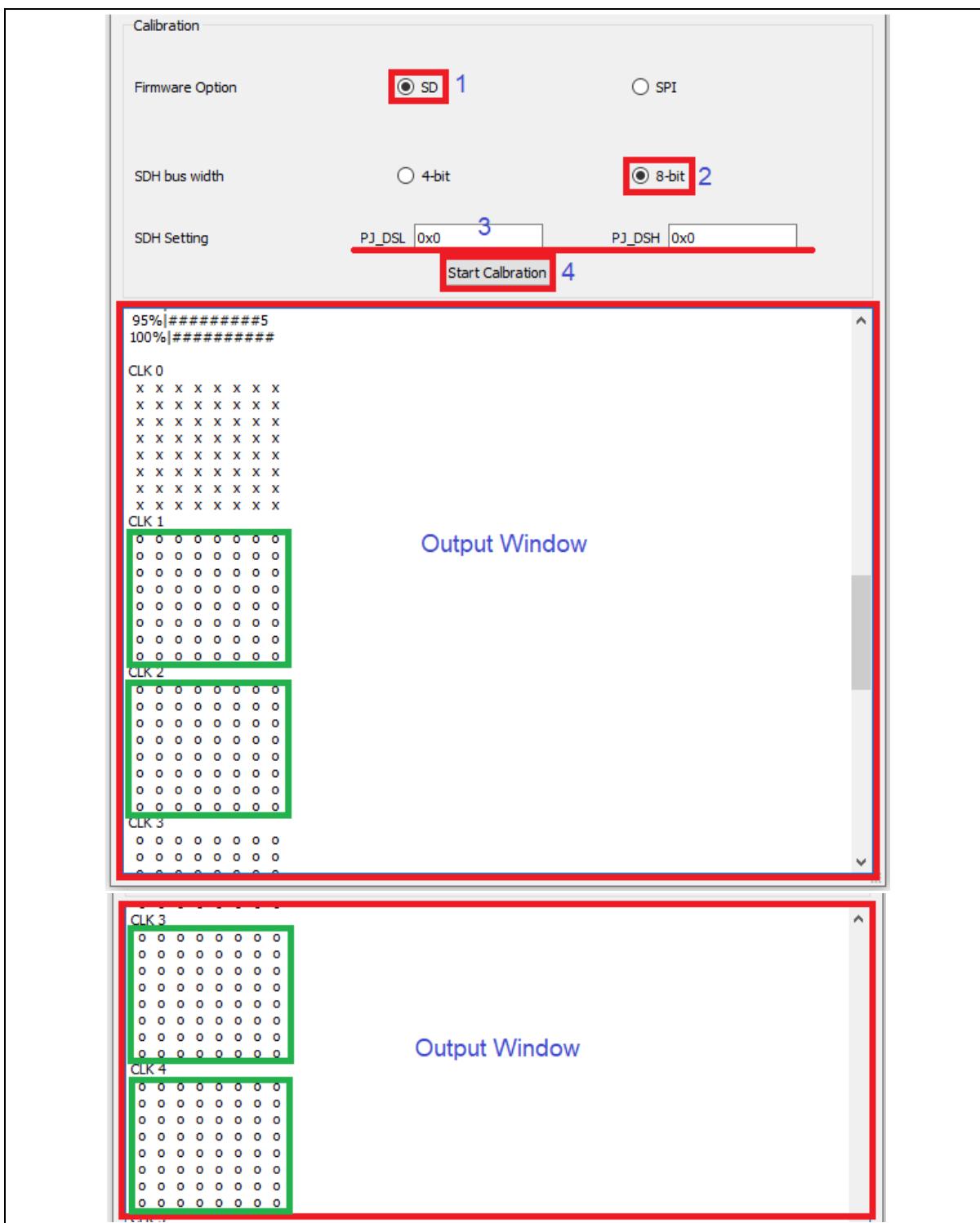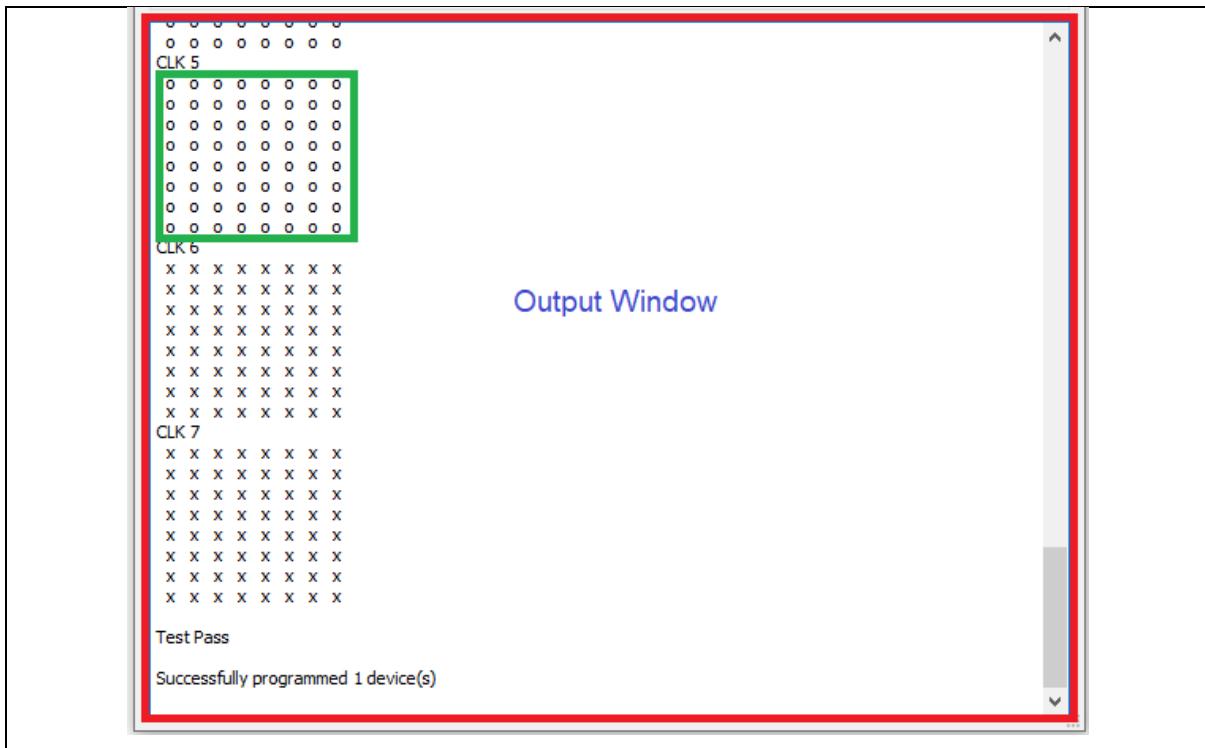
Figure 5-4 SDH Calibration

After setting the drive strength of PJ0 to 3 and configuring SYS_GPJ_MFPL_PJ0MFP_eMMC1_DAT4 to pcfg_sdhci_drive3_1_8V, the following entries should be added to the table:

```
sdhci1 {
    pinctrl_sdhci1_1_8V: sdhci1_1_8Vgrp {
    nuvoton,pins =
            <SYS_GPJ_MFPL_PJ0MFP_eMMC1_DAT4  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPL_PJ1MFP_eMMC1_DAT5  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPL_PJ2MFP_eMMC1_DAT6  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPL_PJ3MFP_eMMC1_DAT7  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPL_PJ6MFP_eMMC1_CMD   &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPL_PJ7MFP_eMMC1_CLK   &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPH_PJ8MFP_eMMC1_DAT0  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPH_PJ9MFP_eMMC1_DAT1  &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPH_PJ10MFP_eMMC1_DAT2 &pcfg_sdhci_drive3_1_8V>,
            <SYS_GPJ_MFPH_PJ11MFP_eMMC1_DAT3 &pcfg_sdhci_drive3_1_8V>;
    };
};
```

6 REVISION HISTORY

Date	Revision	Description
2023.12.18	1.01	Add support for MA35D0 and MA35H0. Rename this document from MA35D1 to MA35 Series. Update description of load DDR firmware.
2023.04.06	1.00	Preliminary issued.

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