ARM® Cortex®-M
32-bit Microcontroller

NuTool - ClockConfigure
User Manual

For additional information or questions, please contact: Nuvoton Technology Corporation.

www.nuvoton.com

Table of Contents

List of Figures

1 Introduction

The **NuTool - ClockConfigure** is used to configure system and peripheral clocks of Nuvoton NuMicro® Family. Its features are listed below:

- **Configuring by the ClockTree**: All the supported modules are collected and listed in the ClockTree. The user can manipulate the tree to configure system and peripheral clocks easily.
- **Configuring by module diagram**: Configuring clocks by module diagram is allowed. The user can complete his operation more intuitively and efficiently.
- **Configuring by editing the register value directly**: The user can utilize this feature to inspect the accuracy of the register value.
- **Generation of code**: After doing the above actions, the user can generate code. The generated code can be included into the developing projects. It also comprises all the configuration information.

Through the application, the user can configure system and peripheral clocks of the NuMicro® Family correctly and handily.

2 Starting to Use the NuTool - ClockConfigure

2.1 System Requirements

The following table lists system requirements for the user to run **NuTool - ClockConfigure**.

	Minimum Requirements	Recommended Specifications
Operating System	Windows®7 with latest service pack	Windows®10 with latest service pack
Internet Explorer	Internet Explorer 9	Internet Explorer 11
Input	Keyboard and mouse required	

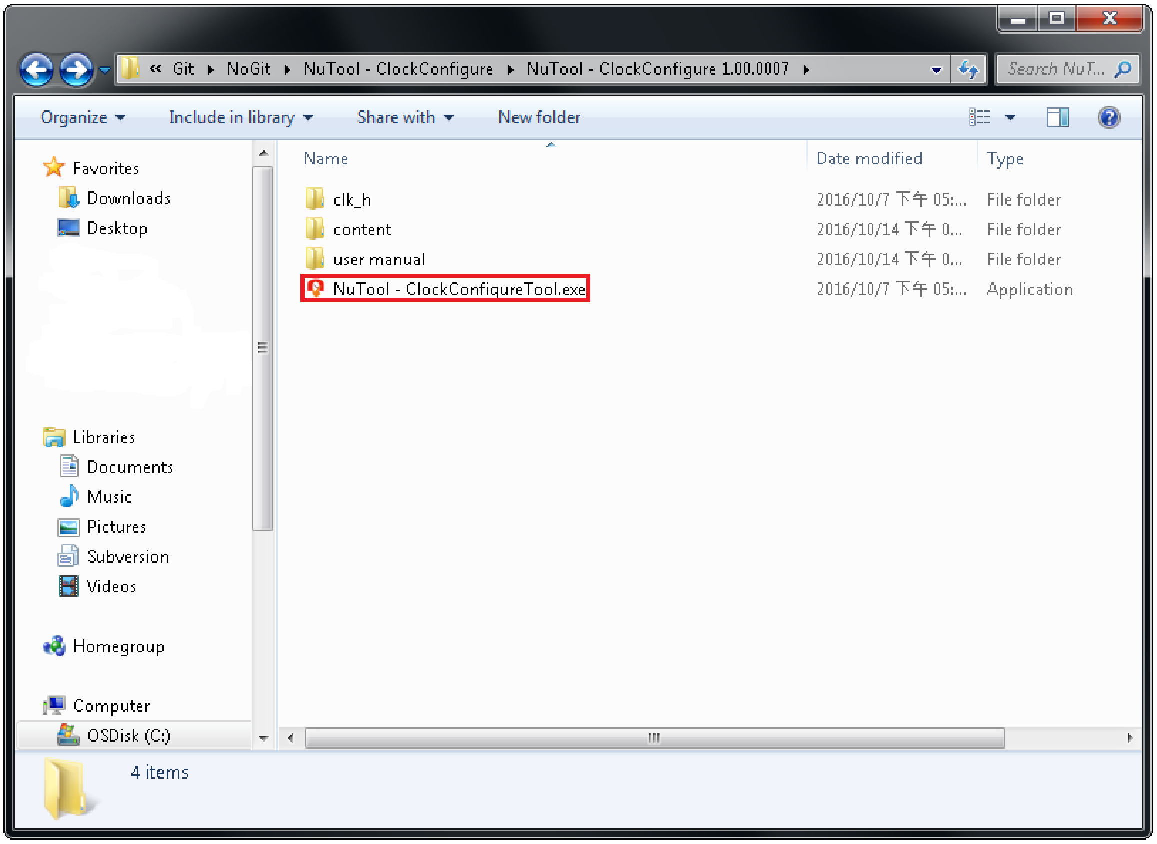
Note: To have a fully usable and pleasant experience with the application, it is strongly recommended that the version of the installed Internet Explorer (IE) be higher than 10.

2.2 Supported Chips

To see the list of supported chips, please refer to **Supported_Chips.htm** in the folder of user manual. The alternative way is to click the **Read User Manual** button on the toolbar.

2.3 Running the NuTool - ClockConfigure

To run the **NuTool - ClockConfigure**, double-click **NuTool – ClockConfigure.exe**. Note that the execution file and the related folders, such as the content folder, should stay in the same directory (referring to the following figure); otherwise, the application will not work properly.



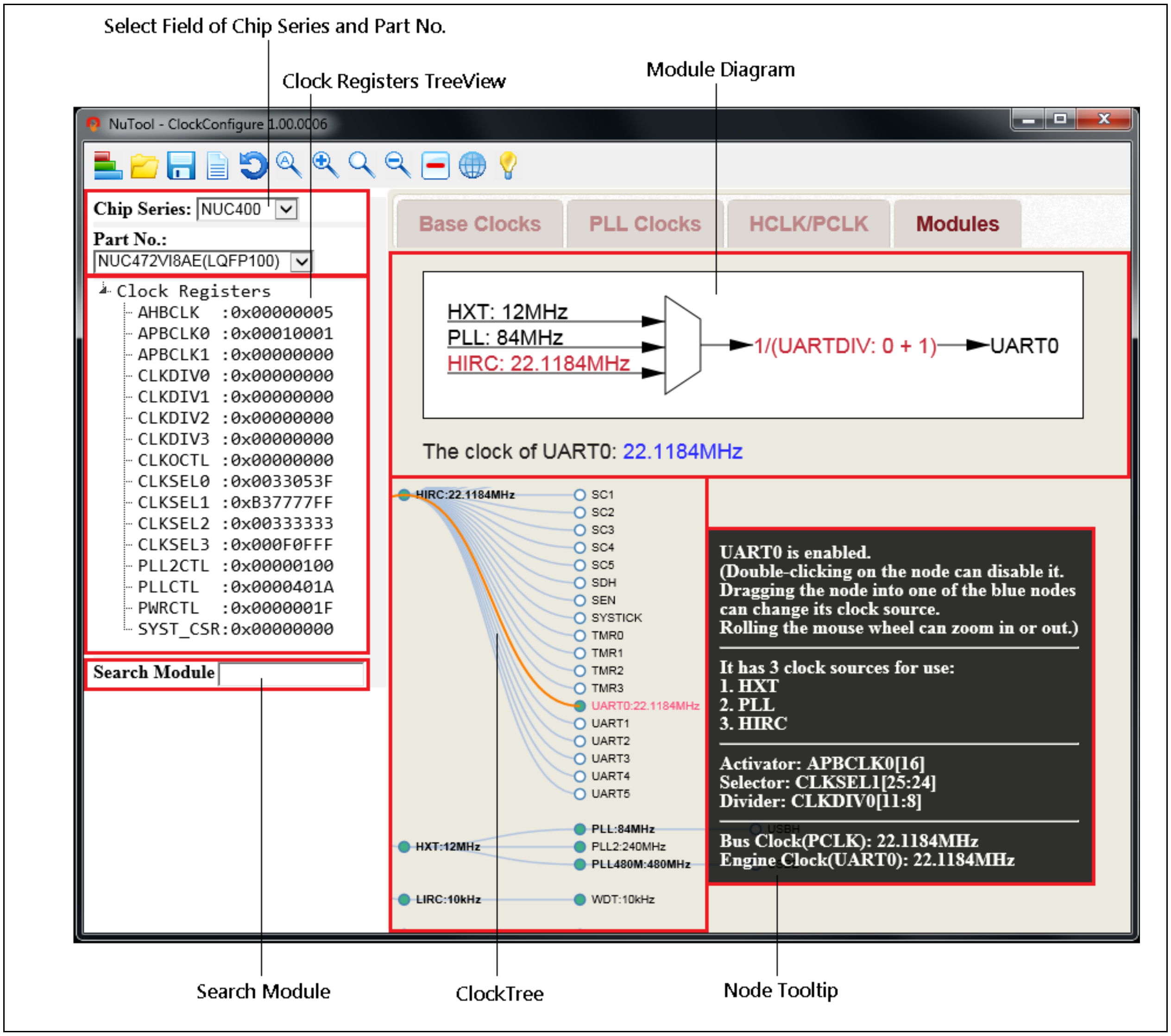
Name	Date modified	Type
clk_h	2016/10/7 下午 05:...	File folder
content	2016/10/14 下午 0...	File folder
user manual	2016/10/14 下午 0...	File folder
NuTool - ClockConfigureTool.exe	2016/10/7 下午 05:...	Application

Figure 2-1 NuTool - ClockConfigure.exe and Related Folders

3 User Interface Guide

3.1 GUI Overview

The ClockConfigure Window includes a variety of components. The name of each component is described in the following figure.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00010001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Search Module

The clock of UART0: 22.1184MHz

UART0 is enabled.
(Double-clicking on the node can disable it.
Dragging the node into one of the blue nodes can change its clock source.
Rolling the mouse wheel can zoom in or out.)

It has 3 clock sources for use:
1. HXT
2. PLL
3. HIRC

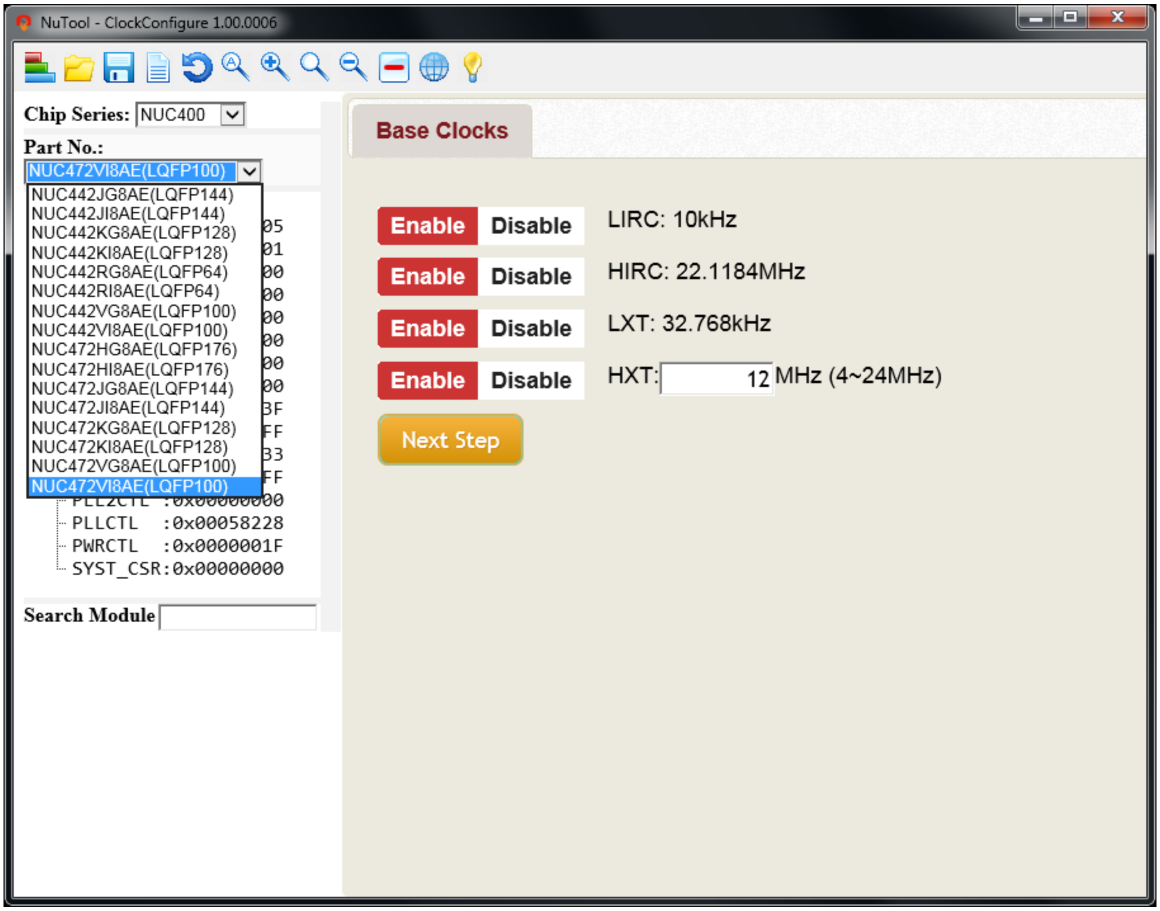
Activator: APBCLK0[16]
Selector: CLKSEL1[25:24]
Divider: CLKDIV0[11:8]

Bus Clock(PCLK): 22.1184MHz
Engine Clock(UART0): 22.1184MHz

Figure 3-1 ClockConfigure Window

3.2 Select Field of Chip Series and Part No.

The user can select the expected chip series and Part No. from the upper-left select field (referring to the following figure). If the select field and the Clock Registers TreeView are hidden, please click the **Switch the Left Panel** to show them.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
PLLCTL   :0x00058228
PWRCTL   :0x0000001F
SYST_CSR:0x00000000
```

LIRC: 10kHz

HIRC: 22.1184MHz

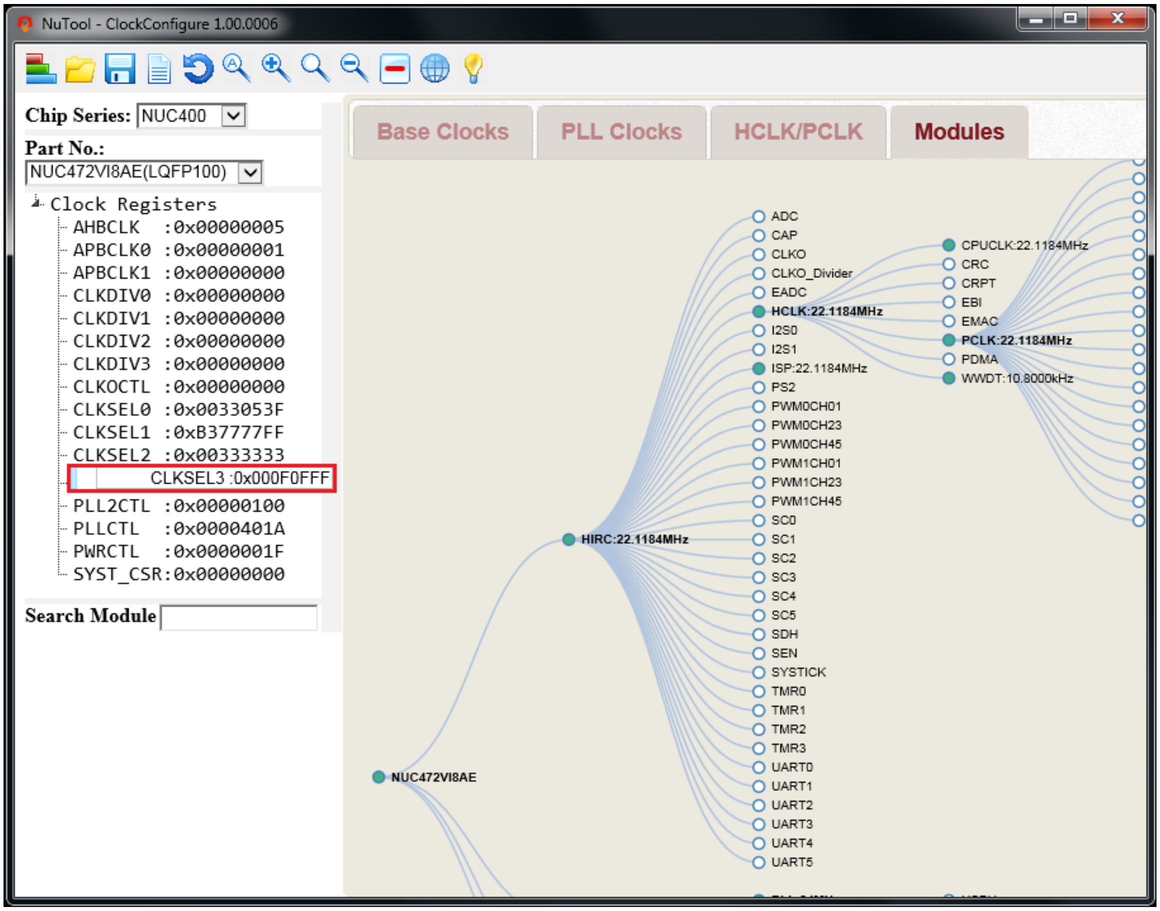
LXT: 32.768kHz

HXT: 12 MHz (4~24MHz)

Figure 3-2 Selecting Part Number

3.3 Clock Registers TreeView

The current values of clock registers are displayed in the upper-left TreeView. Moreover, the user can edit them directly by double-clicking on the expected one and enter a new value (referring to the following figure). After editing, the corresponding result will be updated immediately.



Chip Series: NUC400

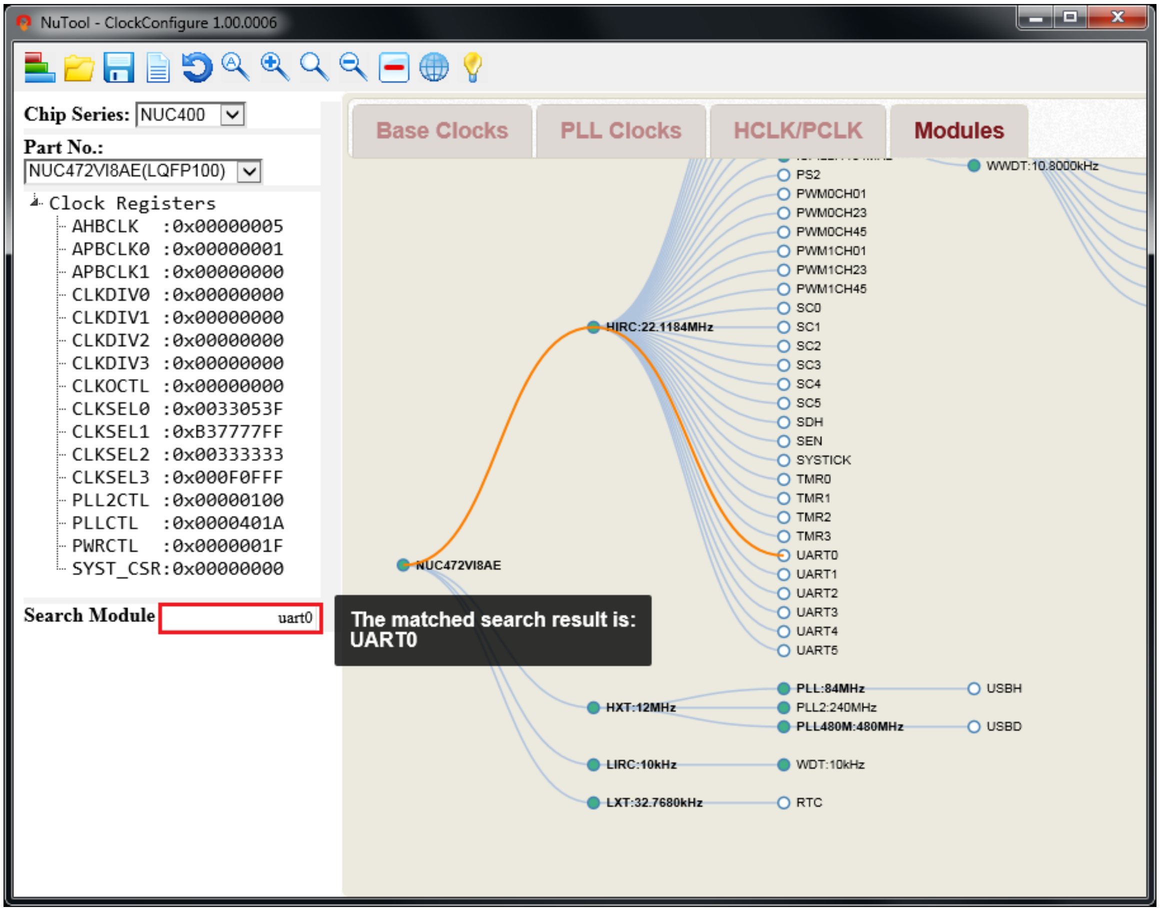
Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3 :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Figure 3-3 Editing a Clock Register

3.4 Search Module

To search a specific module in the ClockTree, the user can input the expected module name in the search field. After input, the matched node will be emphasized with an orange path from the root.



NuTool - ClockConfigure 1.00.0006

Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Search Module: uart0

The matched search result is:
UART0

Figure 3-4 Matched Search Result

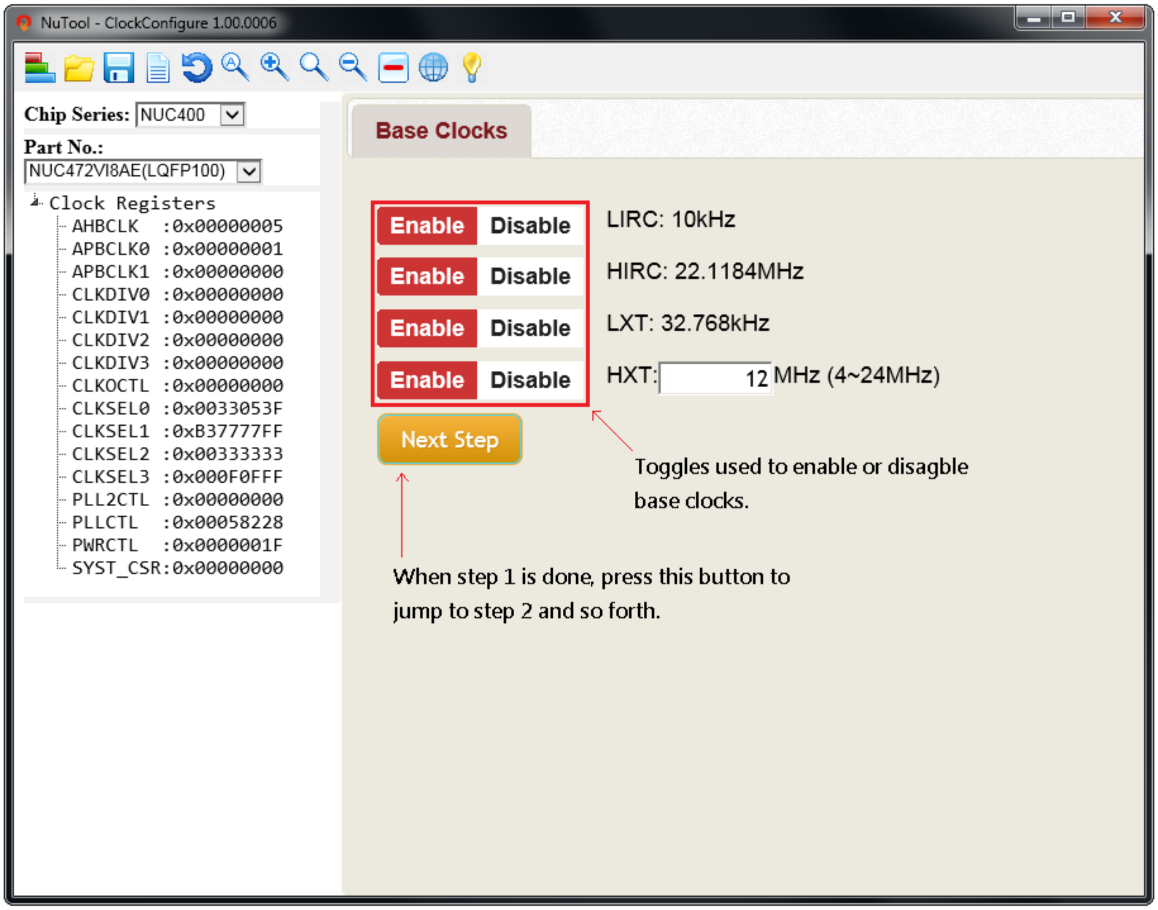
4 Flow of Configuration

4.1 Overview

At first, the user should decide the chip series and part number. The corresponding clock registers will be loaded into the upper-left TreeView region. In the following discussion, we presume the chip series is NUC400 and Part No. is NUC472VIBAE. Other chip may have a slight difference in the flow, but the basic logic is the same. For NCU400, there are four steps to complete the flow of configuration, i.e., Base Clocks, PLL Clocks, HCLK/PCLK and Modules.

4.2 Step 1: Base Clocks

In step 1, the user can enable or disable the base clocks of LIRC, HIRC, LXT and HXT (refer to the following figure). When step 1 is completed, push the button of “Next Step” to jump to step 2 and so forth.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000000
  PLLCTL   :0x00058228
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

LIRC: 10kHz

HIRC: 22.1184MHz

LXT: 32.768kHz

HXT: 12 MHz (4~24MHz)

Toggles used to enable or disagble base clocks.

When step 1 is done, press this button to jump to step 2 and so forth.

Figure 4-1Step 1: Base Clocks

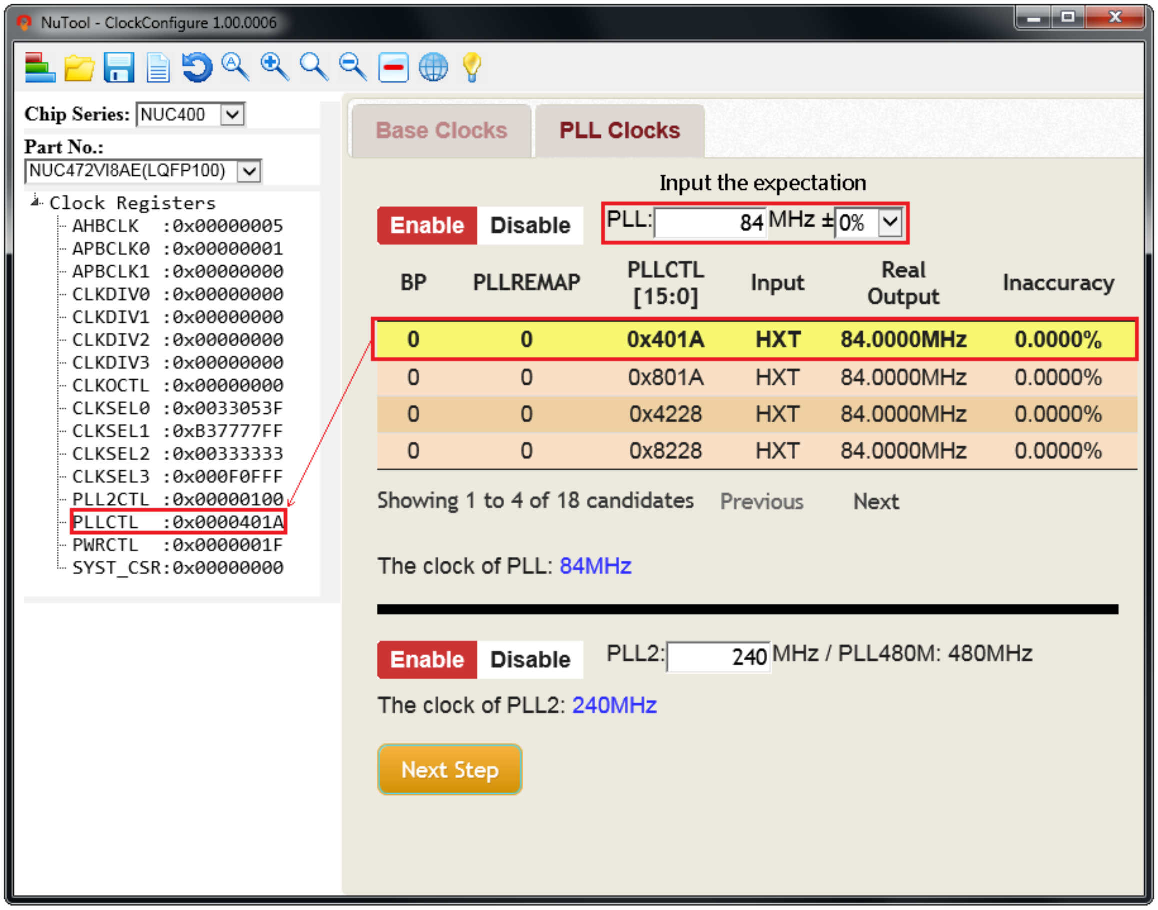
NUTOOL – CLOCKCONFIGURE USER MANUAL

4.3 Step 2: PLL Clocks

In step 2, there are PLL and PLL2 available to be configured.

4.3.1 PLL Part

The user can input his expectation to PLL frequency. All the possible candidates sorted by the inaccuracy will be listed in the table. Move the mouse into the table and choose one of candidates. The clock of PLL will be shown below the table. Note that all the manipulations will update the content of clock registers simultaneously (refer to the following figure).



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Input the expectation

Enable Disable PLL: 84 MHz ± 0%

BP	PLLREMAP	PLLCTL [15:0]	Input	Real Output	Inaccuracy
0	0	0x401A	HXT	84.0000MHz	0.0000%
0	0	0x801A	HXT	84.0000MHz	0.0000%
0	0	0x4228	HXT	84.0000MHz	0.0000%
0	0	0x8228	HXT	84.0000MHz	0.0000%

Showing 1 to 4 of 18 candidates Previous Next

The clock of PLL: 84MHz

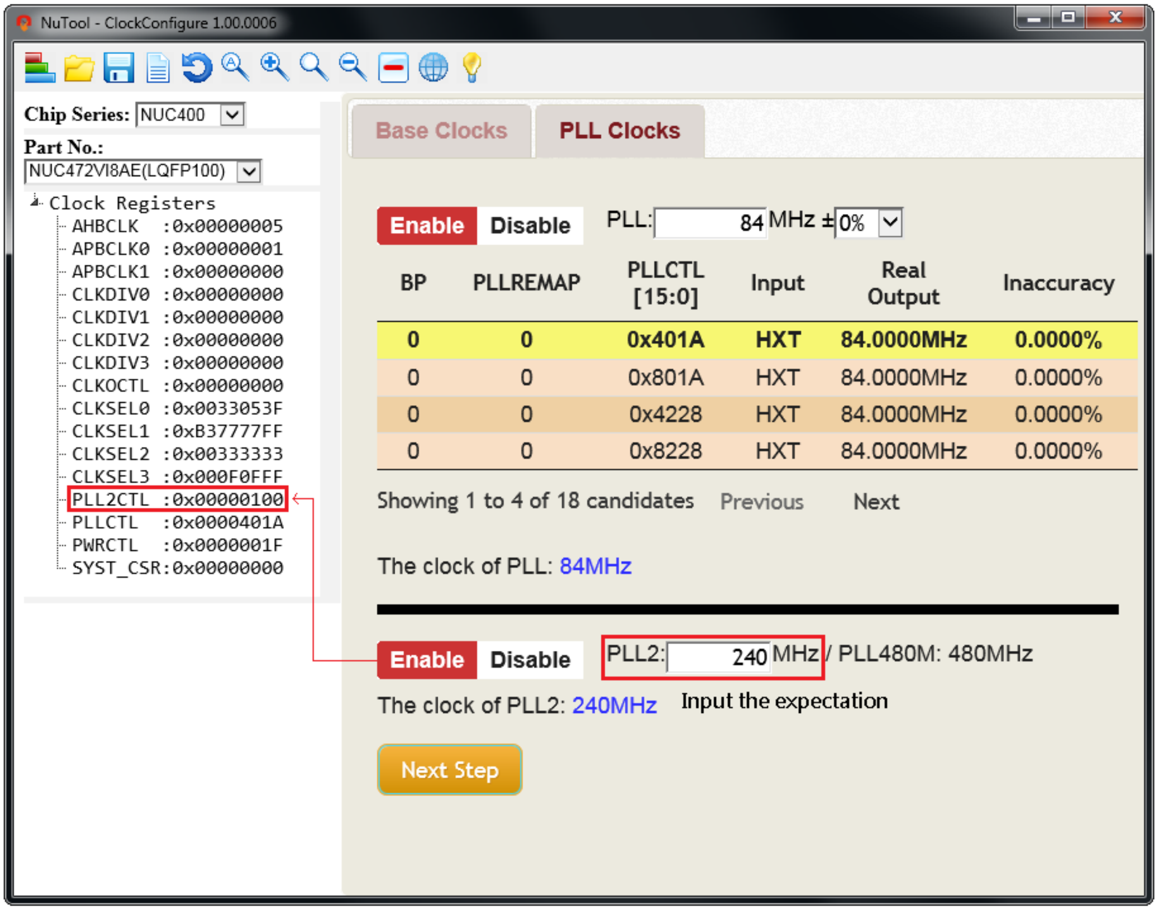
Enable Disable PLL2: 240 MHz / PLL480M: 480MHz

The clock of PLL2: 240MHz

Figure 4-2 Step 2: PLL Clocks (PLL Part)

4.3.2 PLL2 Part

The user can input his expectation to PLL2. The clock of PLL2 will be calculated and shown below the input of PLL2 (refer to the following figure).



NuTool - ClockConfigure 1.00.0006

Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

PLL: 84 MHz ±0%

BP	PLLREMAP	PLLCTL [15:0]	Input	Real Output	Inaccuracy
0	0	0x401A	HXT	84.0000MHz	0.0000%
0	0	0x801A	HXT	84.0000MHz	0.0000%
0	0	0x4228	HXT	84.0000MHz	0.0000%
0	0	0x8228	HXT	84.0000MHz	0.0000%

Showing 1 to 4 of 18 candidates

The clock of PLL: 84MHz

PLL2: 240 MHz / PLL480M: 480MHz

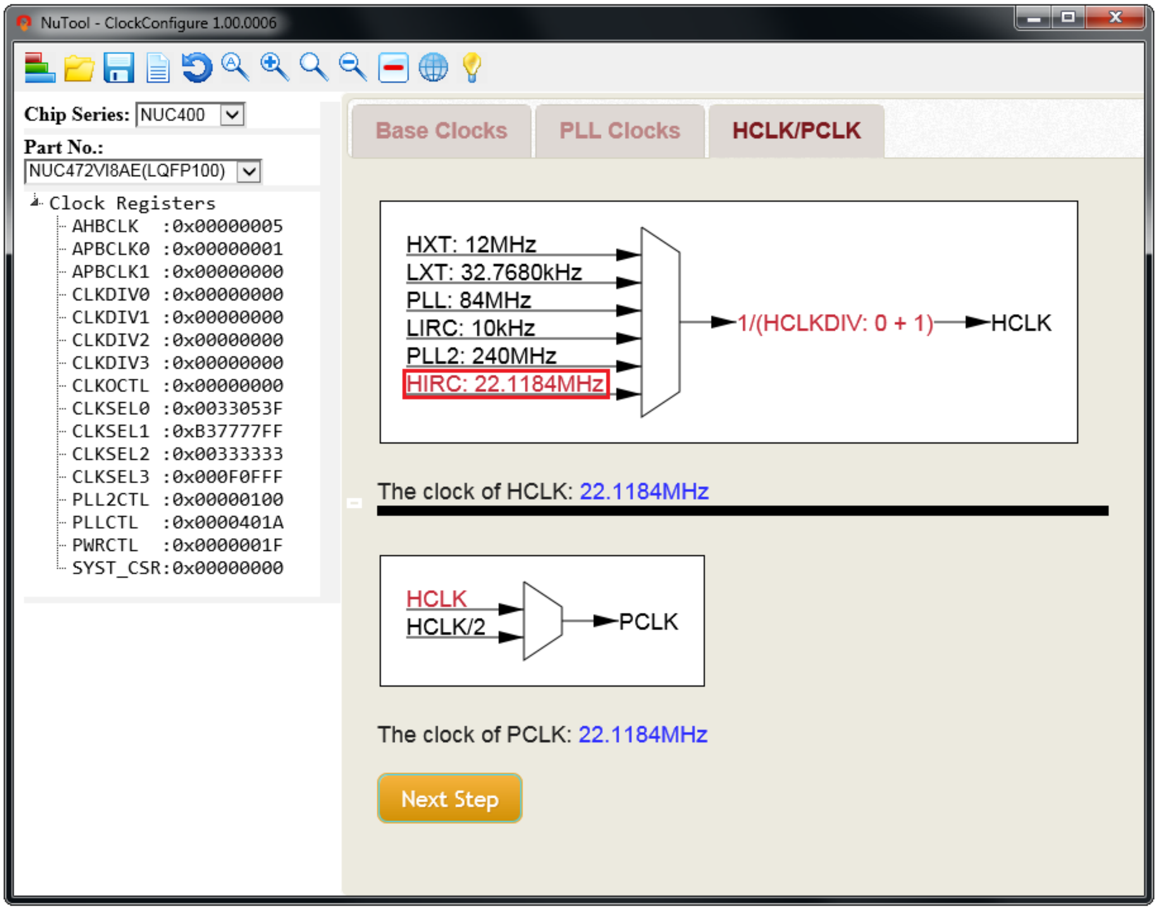
The clock of PLL2: 240MHz

Input the expectation

Figure 4-3 Step 2: PLL Clocks (PLL2 Part)

4.4 Step 3: HCLK/PCLK

In step 3, the feasible clock sources and HCLK's divider will be drawn in the diagram used to configure HCLK. The user can choose one of clock sources by moving the mouse into the diagram and directly clicking on the expected clock source (refer to the following figure). The chosen one will be highlighted with an brown color.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

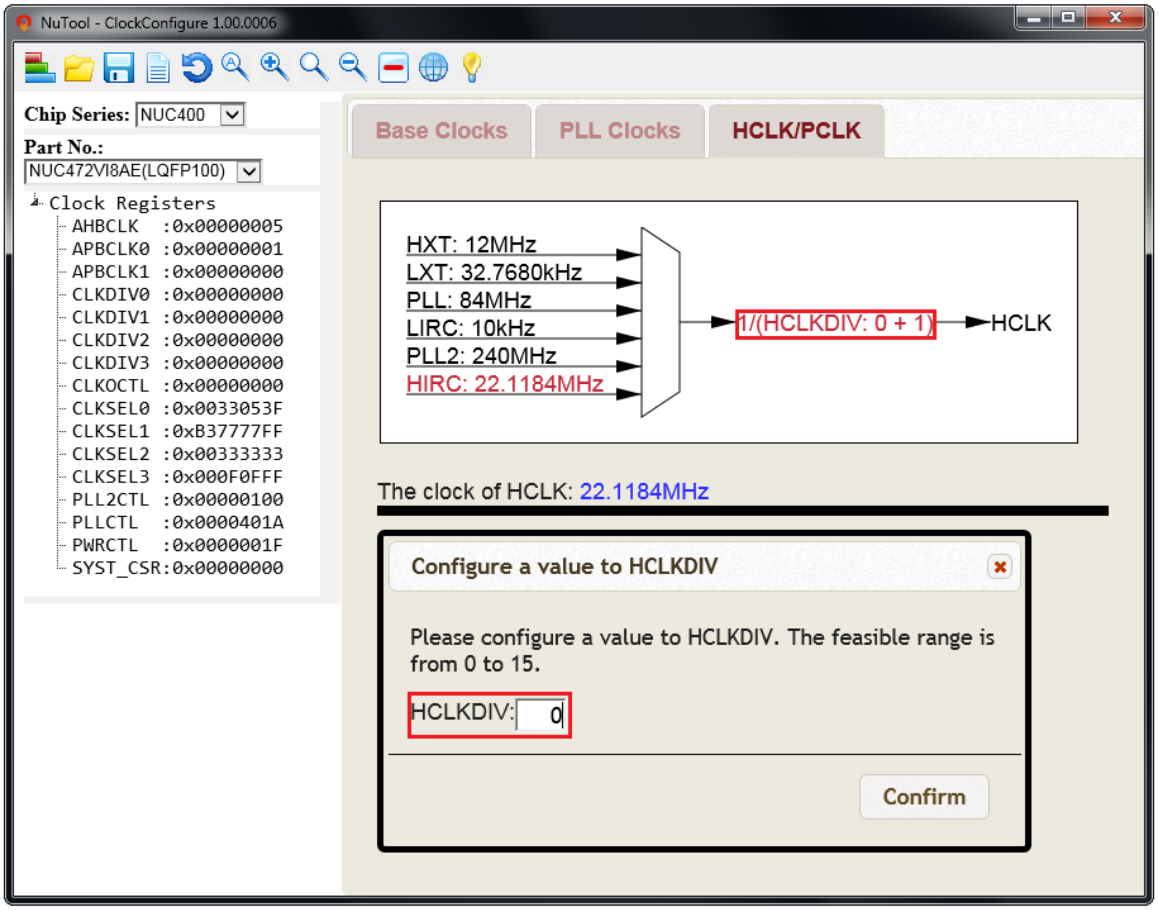
```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

The clock of HCLK: 22.1184MHz

The clock of PCLK: 22.1184MHz

Figure 4-4 Step 3: Choosing the Clock Source of HCLK

To configure the value of HCLK’s divider, move the mouse into the diagram and click on the divider region. A dialog will pop up to allow the user to input a value to HCLK’s divider (refer to the following figure). For instance, we input 0 to HCLKDIV. After pressing the confirm button, the clock of HCLK will be calculated and shown below the diagram. In this case, it would be 22.1184MHz.



Chip Series: NUC400
Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00000001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB37777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

The clock of HCLK: 22.1184MHz

Configure a value to HCLKDIV

Please configure a value to HCLKDIV. The feasible range is from 0 to 15.

HCLKDIV: 0

Figure 4-5 Step 3: Setting a Value to HCLK's Divider

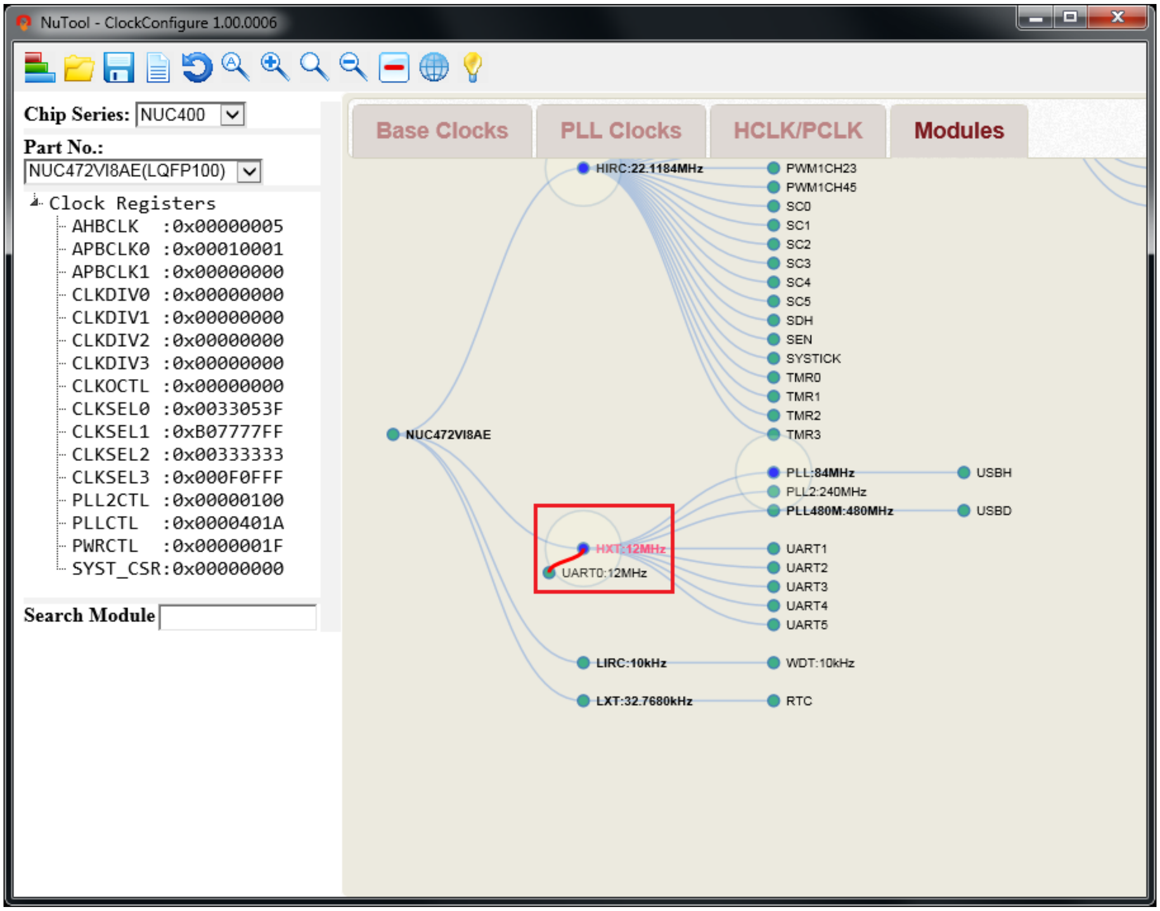
Similarly, the process of configuring PCLK requires the user’s decision for its clock source, such as HCLK or HCLK/2. For instance, we choose HCLK. The clock of PLL2 will be shown below the PLL2’s diagram. In this case, it would be 22.1184MHz.

4.5 Step 4: Modules

In the final step, there are two ways to configure modules, i.e. ClockTree and Module Diagram.

4.5.1 ClockTree

In ClockTree, the user can enable or disable modules by double-clicking on the corresponding nodes of the ClockTree. In addition, dragging a node into one of the blue nodes can change its clock source (refer to the following figure). The red connection line means that the module belongs to the target clock source. Only when the red connection line appears, the new change of the clock source could happen after dropping the node. However, the user is unable to configure the divider of any module here. The operation is allowed in the Module Diagram.



Chip Series: NUC400

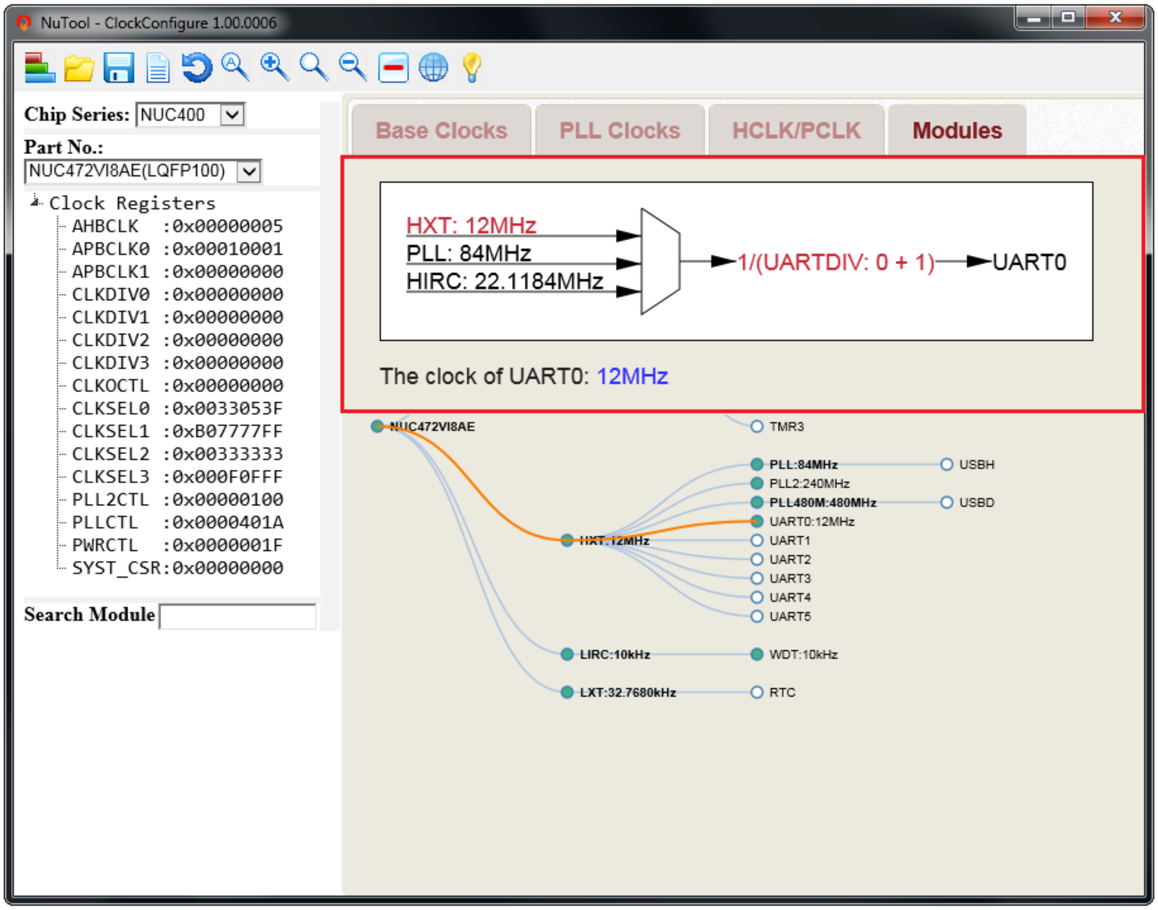
Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00010001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB07777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Figure 4-6 Step 4: Dragging UART0 Node into HXT Node

4.5.2 Module Diagram

When the module is enabled, single-clicking on the node can show the module diagram. The manipulaton of module diagram is the same as HCLK diagram mentioned in section 4.4.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00010001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x00000000
  CLKOCTL  :0x00000000
  CLKSEL0  :0x0033053F
  CLKSEL1  :0xB07777FF
  CLKSEL2  :0x00333333
  CLKSEL3  :0x000F0FFF
  PLL2CTL  :0x00000100
  PLLCTL   :0x0000401A
  PWRCTL   :0x0000001F
  SYST_CSR:0x00000000
```

Search Module

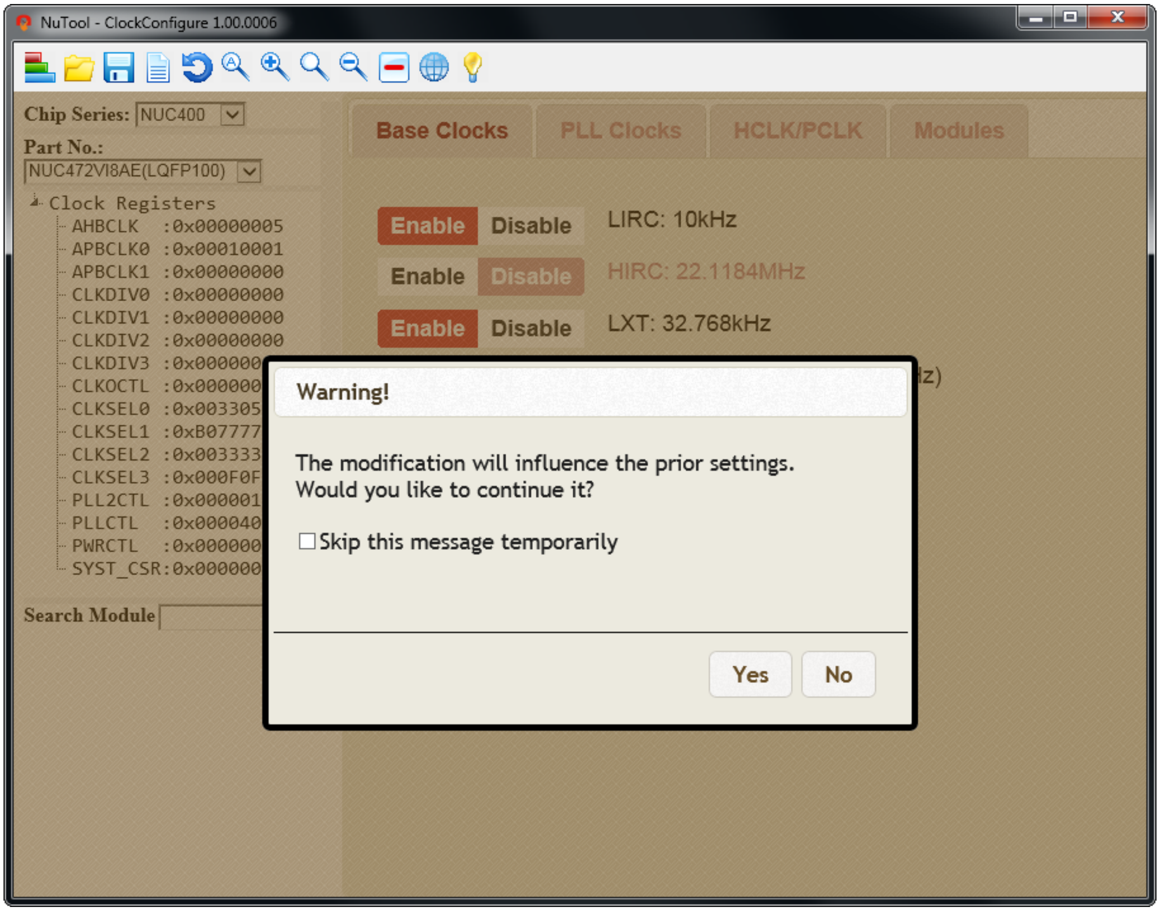
The clock of UART0: 12MHz

Figure 4-7 Step 4: UART0 Diagram

NUTOOL – CLOCKCONFIGURE USER MANUAL

4.6 Multi-way Configuring

For some reason, the user could want to change prior settings in the middle of making the configuration. For instance, after completing the earlier configuration, suddenly we want to disable HIRC. At the moment, a warning dialog pops up to ask if the user would like to continue it since the modification will influence the entire configuration (refer to the following figure). If the user answers ‘No’, HIRC will be still enabled. If the user answers ‘Yes’, all the entire configuration will be updated automatically. When we answer “Yes” and switch to the step 3 and 4, we will find that the clock source of HIRC is disabled in the diagram of HCLK and UART0. The above mechanism is called as “multi-way configuring”. It means the user can change the configuration at any time.



Chip Series: NUC400

Part No.: NUC472VI8AE(LQFP100)

```
Clock Registers
  AHBCLK   :0x00000005
  APBCLK0  :0x00010001
  APBCLK1  :0x00000000
  CLKDIV0  :0x00000000
  CLKDIV1  :0x00000000
  CLKDIV2  :0x00000000
  CLKDIV3  :0x000000
  CLKOCTL  :0x000000
  CLKSEL0  :0x003305
  CLKSEL1  :0xB07777
  CLKSEL2  :0x003333
  CLKSEL3  :0x000F0F
  PLL2CTL  :0x000001
  PLLCTL   :0x000040
  PWRCTL   :0x000000
  SYST_CSR:0x000000
```

Search Module

LIRC: 10kHz

HIRC: 22.1184MHz

LXT: 32.768kHz

Warning!

The modification will influence the prior settings.
Would you like to continue it?

☐ Skip this message temporarily

Figure 4-8 “Multi-way Configuring” Dialog Box

5 Toolbar

5.1 Switch the Left Panel

To show the select field and the Clock Registers TreeView, click the **Switch the Left Panel** button on the toolbar.

5.2 Load Configuration

The user can browse the previously saved configuration files (*.cfg) and select one of them to restore the configured MCU chip. To load the configuration, click the **Load Configuration** button on the toolbar, select the directory preserving the expected configuration file and click the Open button.

5.3 Save Configuration

To save the current configuration, take the following steps:

1. Click the **Save Configuration** button on the toolbar.
2. Browse a user-defined location and give a proper name to the configuration file (*.cfg).
3. Click the Save button. The current configuration will be saved as a .cfg file with a given name. The configuration file can be used to restore the configured MCU chip in the future.

5.4 Generate Code

To generate code to be included into the developing projects, click the **Generate Code** button on the toolbar.

5.5 Return to Default Settings

To return to Default Settings, click the **Return to Default Settings** button on the toolbar.

5.6 Switch Clock Tree

To show the clock tree which only contains the enabled modules, click the **Switch Clock Tree** button on the toolbar. As a result, a compact tree will show up.

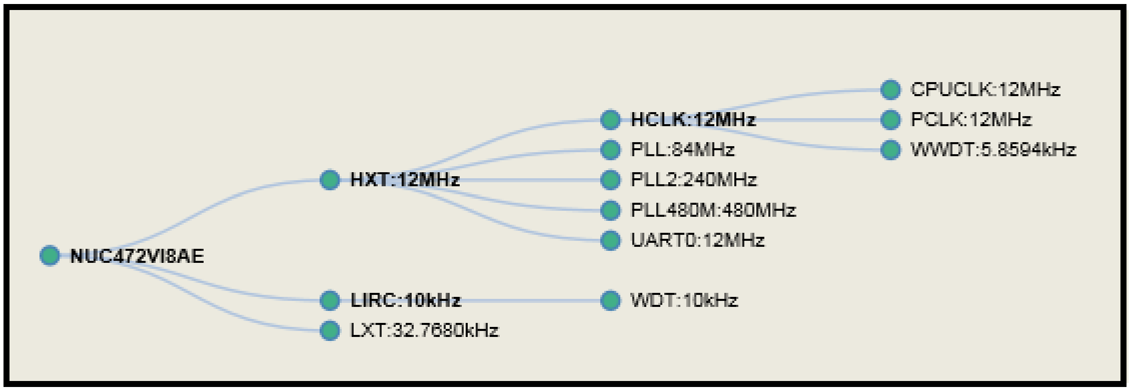


Figure 5-1 Compact Tree

5.7 Zoom In

To adjust the clock tree to a larger one, click the **Zoom In** button on the toolbar. Besides, the user can do the same thing by scrolling the mouse wheel up.

5.8 Best Fit

To adjust the clock tree to the normal size, click the **Best Fit** button on the toolbar.

5.9 Zoom Out

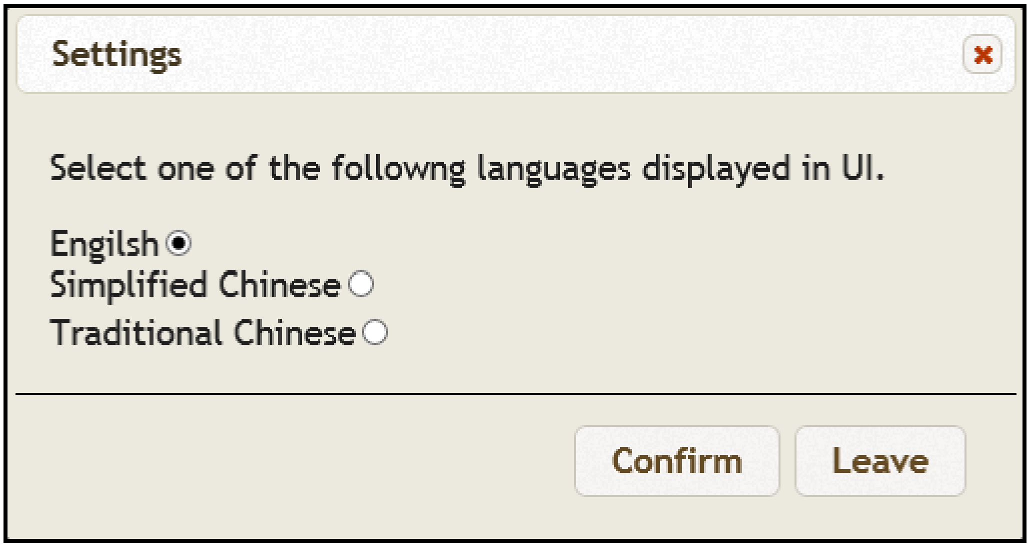
To adjust the clock tree to a smaller one, click the **Zoom Out** button on the toolbar. Besides, the user can do the same thing by scrolling the mouse wheel down.

5.10 Disable all Enabled Modules

To disable all enabled modules, click the **Disable all Enabled Modules** button on the toolbar.

5.11 Settings

To select UI language, click the **Settings** button on the toolbar. There are three languages supported in the application, including English, Simplified Chinese, and Traditional Chinese.



Select one of the followng languages displayed in UI.

Engilsh ●
Simplified Chinese ○
Traditional Chinese ○

Figure 5-2 “Settings” Dialog Box

5.12 Read User Manual

To read the user manual, click the **Read User Manual** button on the toolbar.

6 Revision History

Date	Revision	Description
2016.09.30	1.00	Initially released.
2018.08.03	1.01	1. Supported M480.
2019.04.29	1.02	1. Supported NUC126, M0564, M251 and M2351.
2019.07.01	1.03	1. Supported M031, NUC1261, NUC2201, NUC029xDE, NUC029xEE, NUC029xGE and NUC029TAE.
2019.11.01	1.04	1. Supported NUC029ZAN.