Emulating MDIO via M030G SPI

Example Code Introduction for 32-bit NuMicro® Family

Document Information

Application	This example code uses M030G SPI to emulate MDIO waveform for controlling Ethernet PHY (IP101GR).
BSP Version	M029G_M030G_M031G_Series_BSP_CMSIS_V3.03.000
Hardware	NuMaker-M030GTD V1.1

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1. Overview

This example code uses M030G SPI to emulate serial management interface (MDC/MDIO) waveform for controlling Ethernet PHY.

Most of the NuMicro Family does not support MDIO master interface for PHY device configuration. This example code provides the solution that can be widely used in the NuMicro Family for accessing Ethernet PHY.

This example code requires additional external hardware modules, including an Ethernet PHY. The part number of Ethernet PHY is IP101GR made by IC PLUS Corporation.

1.1 Principle

The following section will focus on how to generate the MDIO waveform. M030G acts as a SPI master and IP101GR as a SPI slave.

1.1.1 MDIO Data Format

The MDIO data format is shown in Figure 1-1 and MDIO data field description is shown in Table 1-1.

Preamble	ST	OP	PHY_ADR	REG_ADR	TA	DATA
32-bit	2-bit	2-bit	5-bit	5-bit	2-bit	16-bit

Figure 1-1 MDIO Data Format

Field	Width	Description
Preamble	32-bit	32 continuous bits of value 1.
ST	2-bit	Start of frame is 2'01.
OP	2-bit	Op code. 01 = Write operation 10 = Read operation
PHY_ADR	5-bit	PHY address.
REG_ADR	5-bit	Register address.
TA	2-bit	Turnaround time.
DATA	16-bit	Any 16-bit value. In Write operation, the MAC drives MDIO. In Read operation, the PHY drives MDIO.

Table 1-1 MDIO Field Description

Since MDIO line is the bi-directional data line, connect SPI_MOSI pin, SPI_MISO pin and MDIO pin together to realize the function. In Read operation, the program must configure the SPI_MOSI pin as GPIO input mode before reading data. Figure 1-3 and Figure 1-4 show the program flow to emulate MDIO Write and Read waveform, respectively. Figure 1-2 shows the operation flow in terminal.

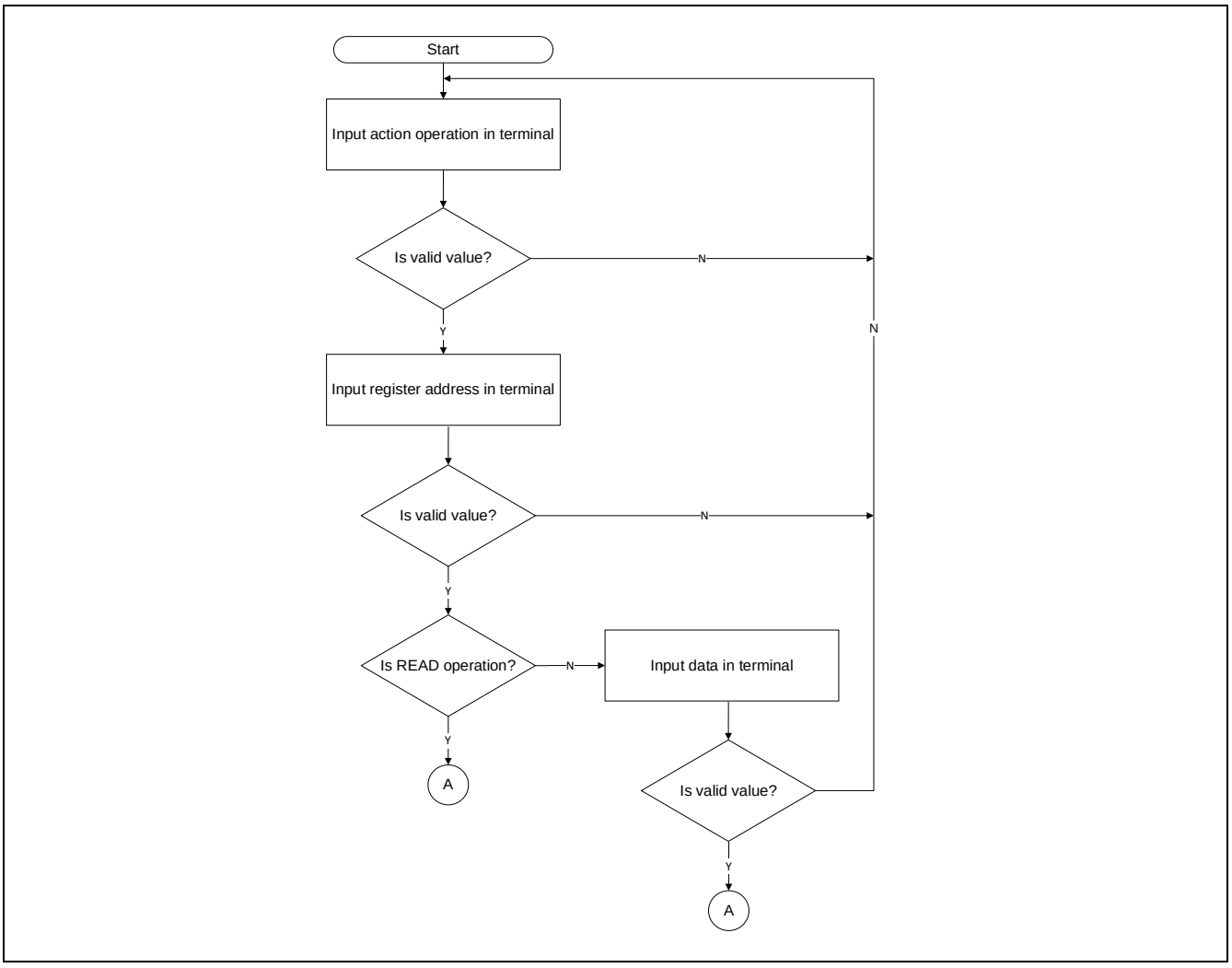

Figure 1-2 Operation Flow in Terminal

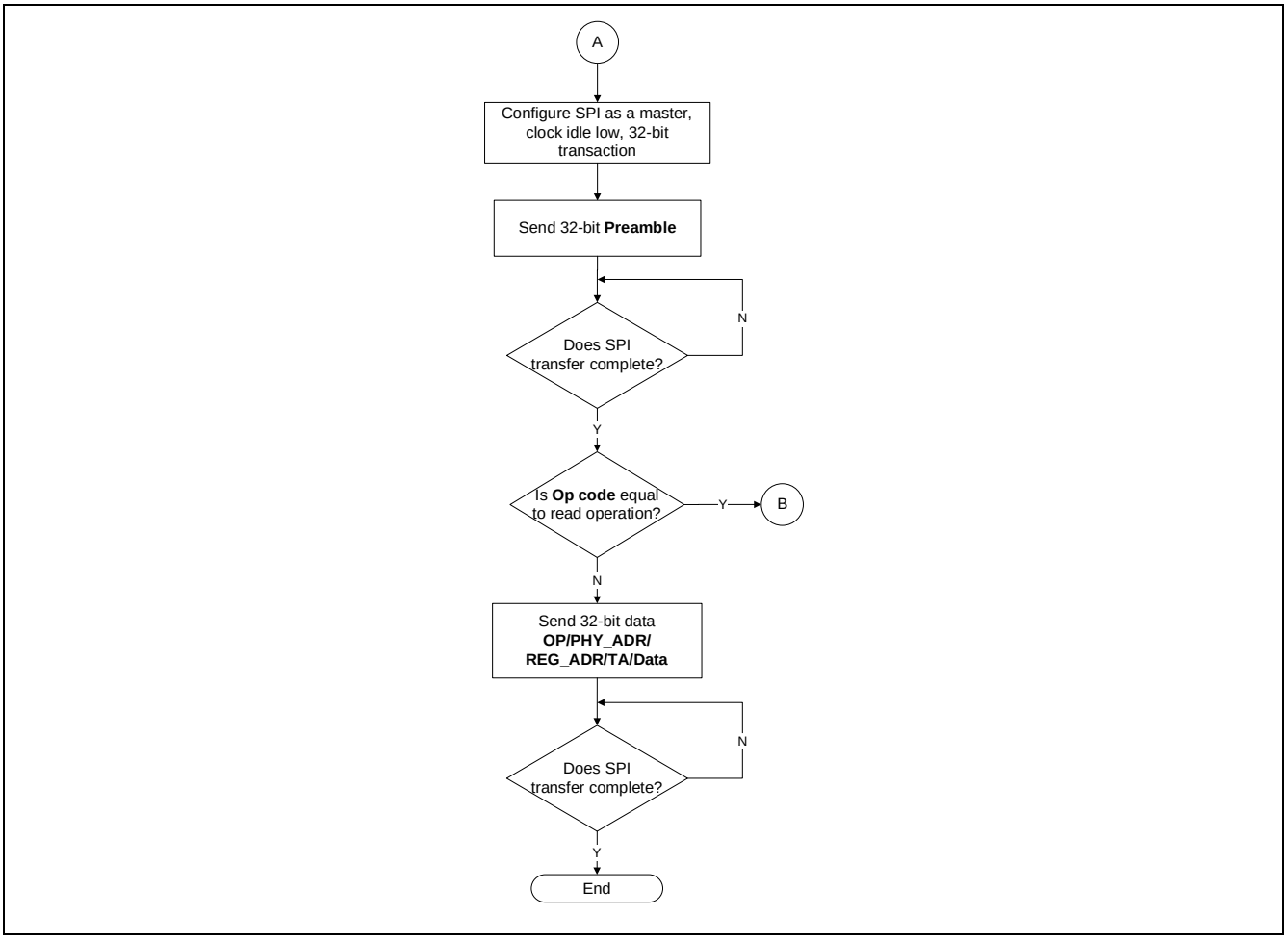

Figure 1-3 SPI Emulate MDIO Write Waveform

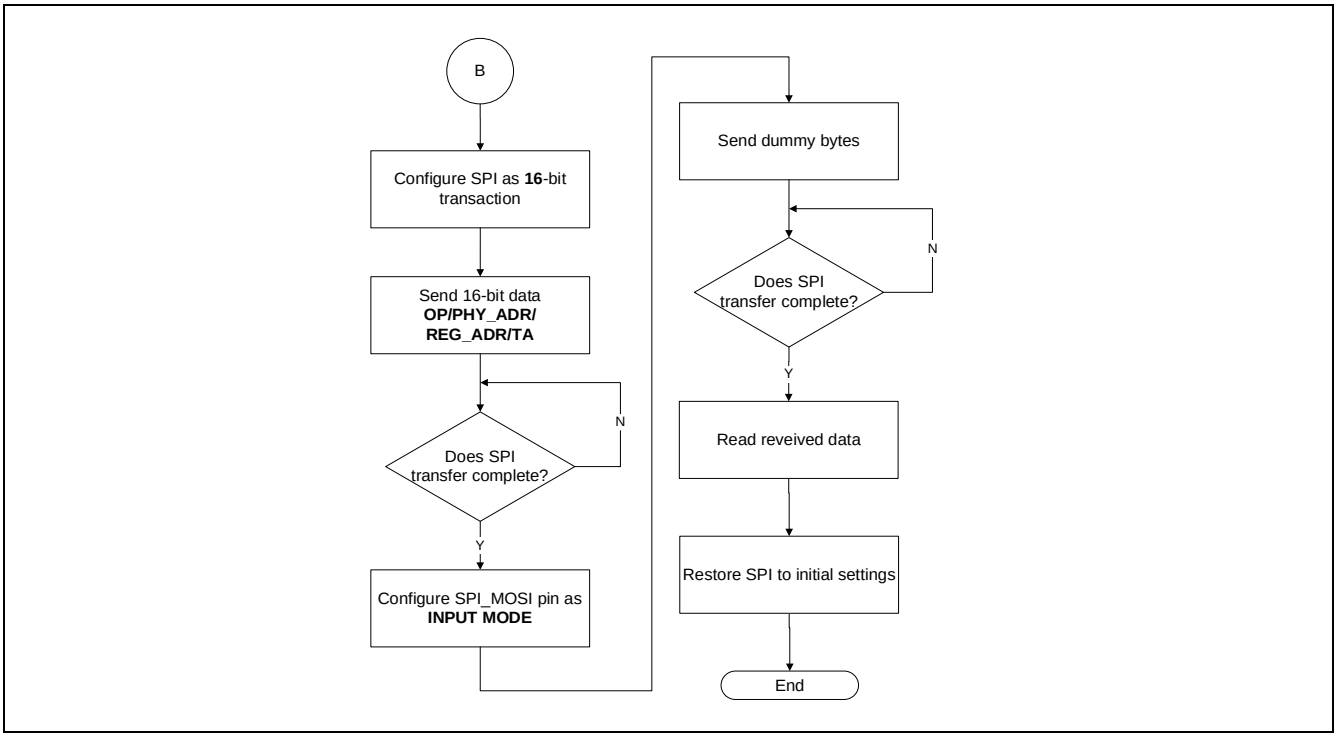

Figure 1-4 SPI Emulate MDIO Read Waveform

1.2 Demo Result

Start the computer terminal software, set UART baud rate to 115200 bps, no parity bit, data length is 8 bits, and the stop bit is 1 bit. After executing the program, the terminal displays the instructions.

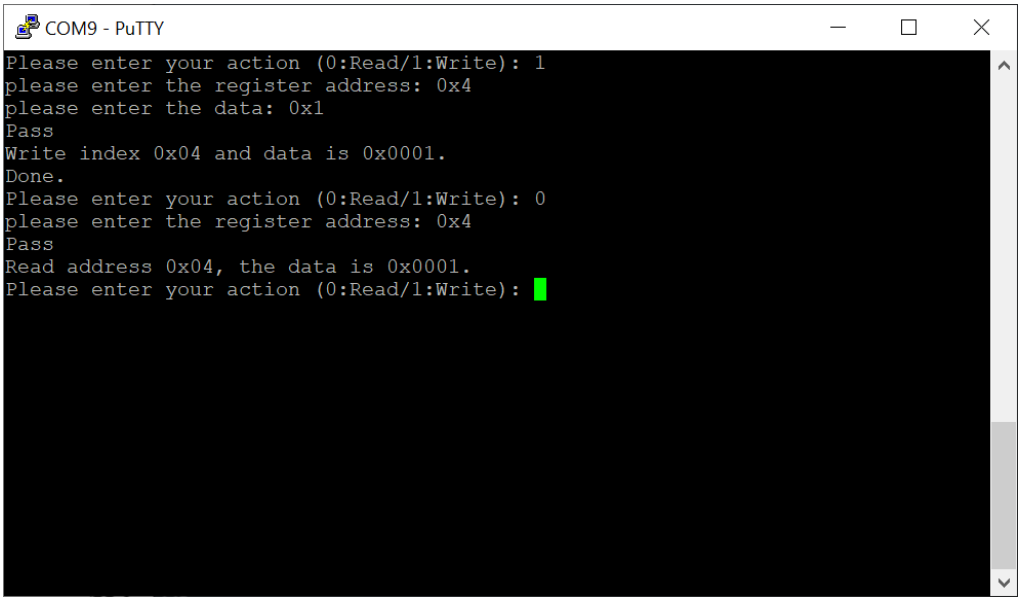

Figure 1-5 Screenshot of the Terminal

The logic analyzer display waveform of MDIO Write and Read operation are shown in Figure 1-6 and Figure 1-7, respectively, which show the information of configuring register 0x04 as 0x0001 and performing a verify operation.

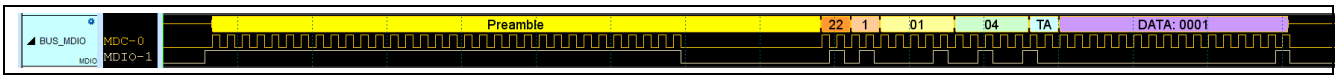

Figure 1-6 MDIO Write Results

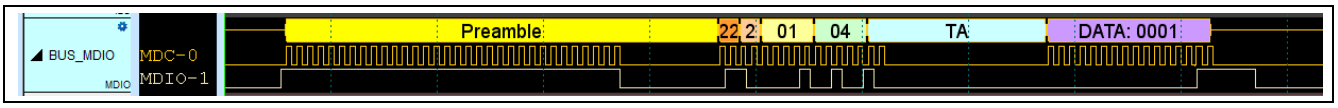

Figure 1-7 MDIO Read Results

2. Code Description

A function used to initialize SPI function. The code is located in *spi_transfer.c*.

```
void SPI_Init(void)
{
    /* Set IP clock divider. SPI clock rate = 1MHz */
    SPI_Open(SPI0, SPI_MASTER, SPI_MODE_0, 32, SPI_CLK_FREQ);

    /* Enable the automatic hardware slave select function. Select the SS pin and
       configure as low-active. */
    SPI_EnableAutoSS(SPI0, SPI_SS, SPI_SS_ACTIVE_LOW);
}
```

A function used to emulate MDIO waveform via SPI. The code is located in *spi_transfer.c*.

For the Write operation, the program:

- Sends the 32-bit preamble; and
- Sends the variable *MDIO_temp* consisting of 2-bit of ST, 2-bit of Op code, 5-bit of PHY address, 5-bit of register address, 2-bit of TA and 16-bit of data.

For the Read operation, the program:

- Sends the 32-bit preamble.
- Configures SPI as 16-bit transaction and sends the variable *MDIO_temp* consisting of 2-bit of ST, 2-bit of Op code, 5-bit of PHY address, 5-bit of register address and 2-bit of TA.
- Configures SPI_MOSI pin as GPIO input mode for receiving data; and
- After receiving data is finished, re-configures SPI function as initial state.

```
MDIO_RES SPI_MDIO_RW(unsigned char rw, unsigned char phy_addr, unsigned char reg_addr,
unsigned int w_data, unsigned int *r_data)
{
    unsigned int MDIO_temp = 0;

    /* Checking parameters validation */
    if (rw > 0x02)
        return RW_ERROR;

    if (phy_addr > MDIO_PHY_MAX)
        return phy_ERROR;

    if ((rw == MDIO_OP_W) && (w_data > W_DATA_MAX))
        return w_data_ERROR;

    if ((rw == MDIO_OP_R) && (w_data != W_DATA_MAX))
        return r_data_ERROR;

    /* Clear SPI FIFO */
```

```
    SPI_ClearTxFIFO(SPI0);
    SPI_ClearRxFIFO(SPI0);

    /* Prepare the MDIO package with 32-bit data, including 2-bit ST, 2-bit Op code,
    5-bit PHY address, 5-bit Register address, 2-bit TA and 16-bit Data */
    MDIO_temp = (MDIO_ST_CAUSE_22 << MDIO_ST_OFFSET) | (rw << MDIO_OP_OFFSET) |
                (phy_addr << MDIO_PHY_OFFSET) | (reg_addr << MDIO_REG_OFFSET) |
                (MDIO_TA << MDIO_TA_OFFSET) | w_data;

    /* READ operation with 16-bit data, including 2-bit ST, 2-bit Op code,
    5-bit PHY address and 5-bit Register address */
    if (rw == MDIO_OP_R)
        MDIO_temp = (MDIO_temp >> 16) & 0xFFFF;

    /* Send 32-bit preamble */
    SPI_WRITE_TX(SPI0, 0xffffffff);
    /* Check SPI0 busy status */
    while (SPI_IS_BUSY(SPI0));

    /* READ operation with 16-bit data, including 2-bit ST, 2-bit Op code,
    5-bit PHY address, 5-bit Register address and 2-bit TA*/
    /* WRITE operation with 32-bit data, including 2-bit ST, 2-bit Op code,
    5-bit PHY address, 5-bit Register address, 2-bit TA and 16-bit Data */
    if (rw == MDIO_OP_R)
        SPI_SET_DATA_WIDTH(SPI0, 16);

    SPI_WRITE_TX(SPI0, MDIO_temp);
    /* Check SPI0 busy status */
    while (SPI_IS_BUSY(SPI0));

    /* Read data from Ethernet PHY */
    if (rw == MDIO_OP_R)
    {
        /* Configure PA0(MOSI) as input mode for receiving data */
        SYS->GPA_MFPL = (SYS->GPA_MFPL & ~(SYS_GPA_MFPL_PA0MFP_Msk)) |
                        (SYS_GPA_MFPL_PA0MFP_GPIO);
        GPIO_SetMode(PA, BIT0, GPIO_MODE_INPUT);

        SPI_ClearRxFIFO(SPI0);
        /* Send dummy data for receiving data */
        SPI_WRITE_TX(SPI0, 0xFFFF);
        /* Check SPI0 busy status */
        while (SPI_IS_BUSY(SPI0));
        /* Read received data */
        r_data[reg_addr] = SPI_READ_RX(SPI0);

        /* Restore to initial settings */
        SYS->GPA_MFPL = (SYS->GPA_MFPL & ~(SYS_GPA_MFPL_PA0MFP_Msk)) |
                        (SYS_GPA_MFPL_PA0MFP_SPI0_MOSI);
        SPI_SET_DATA_WIDTH(SPI0, 32);
    }
    return PASS;
}
```

3. Software and Hardware Requirements

3.1 Software Requirements

- BSP version
  - M029G_M030G_M031G_Series_BSP_CMSIS_V3.03.000
- IDE version
  - Keil uVersion 5.38

3.2 Hardware Requirements

- Circuit components
  - NuMaker-M030GTD V1.1
- Pin Connect
  - Connect the SPI_MOSI (PA.0) pin and SPI_MISO (PA.1) pin to the Ethernet PHY MDIO and connect the SPI_CLK (PA.2) to Ethernet PHY MDC to control Ethernet PHY.
  - Connect the 4.7 kΩ pull-up resistor on MDIO pin.

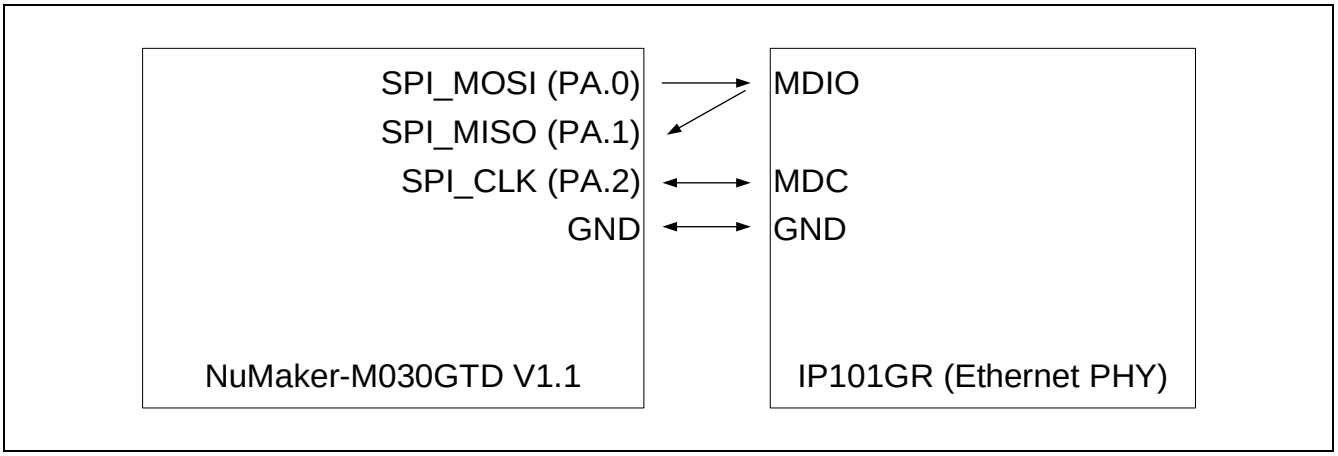

Figure 3-1 Pin Connect

4. Directory Information

The directory structure is shown below.

EC_M030G_SPI_Emulate_MDIO_V1.00	
Library	Sample code header and source files
CMSIS	Cortex® Microcontroller Software Interface Standard (CMSIS) by Arm® Corp.
Device	CMSIS compliant device header file
StdDriver	All peripheral driver header and source files
SampleCode	
ExampleCode	
Project	Source file of example code

Figure 4-1 Directory Structure

5. Example Code Execution

1. Browse the sample code folder as described in the Directory Information section and double-click *M030G_SPI_Emulate_MDIO.uvprojx*.
2. Enter Keil compile mode.
   - Build
   - Download
   - Start/Stop debug session
3. Enter debug mode.
   - Run

6. Revision History

Date	Revision	Description
2024.07.02	1.00	Initial version.

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