8W Mono Class D Amplifier with Klippel Controlled Sound DSP

Description

The NAU83G10 is a mono Class D audio amplifier with integrated Klippel Controlled Sound (KCS) technology based on the nonlinear mirror filter and current sensing for speaker parameter identification. The adaptive, nonlinear control system cancels the DC displacement, harmonic and intermodulation distortion generated by speaker nonlinearities, operates the voice coil at the optimum rest position and compensates for speaker parameter variation due to aging and climate changes. The new hardware and software capabilities in the NAU83G10VG allow to safely operate smaller speakers at the physical limits to generate more acoustical output at higher sound quality while providing reliable protection against thermal and mechanical overload compared to conventional linear algorithms.

The NAU83G10 can deliver up to 8W output power into 4Ω speaker at THDN 10%. It has a highly efficient Class D amplifier with an intelligently adaptive boost converter, which can boost the supply voltage up to 12V with 0.177V step accuracy while producing only 12 uV_{RMS} ultra-low idle output noise for a receiver speaker.

The NAU83G10 has on chip & low latency Tensilica HiFi Audio DSP along with a high quality 24-bit audio ADCs for current and voltage sense at the speaker terminal, where the gain variation of these V-Sense and I-Sense ADCs is minimized to less than +/- 1% over temperature and supply for a precise speaker control. In addition, the accurate AEC reference signal is available to the host processor, which can improve the barge-in performance by cancellation of nonlinear distortion by KCS.

The integrated SAR ADC can monitor the voltage level on the battery supply or external supply, and the audio gain can be controlled automatically by an integrated ALC depending upon the programmable battery threshold. It also support an input peak current limiter to regulate the battery current while preserving audio quality.

The NAU83G10 supports I2C control and I2S/PCM audio interfaces. It operates with analog supply voltages from 1.6V to 1.98V, while the battery supply voltage can operate from 2.9V to 5.5V. The operating temperature range is specified from -40°C to +85°C, and it is available in CSP 50 Ball package with a 0.5mm pitch.

Key HW Features

Powerful Mono Boosted Class-D Amplifier

- 8 W Output Power @4Ω, 10% THD+N, 5V VBat
- 6.5 W Output Power @8 Ω, 10% THD+N, 5V VBat
- 0.021% THD+N @ 8 Ω Load, 1W Output Power
- 12 μV_{RMS} Output Noise in Receiver mode
- 55 μV_{RMS} Output Noise in Speaker mode
- 92 dB PSRR for 200 mVpp ripple at 217 Hz
- Click-and-Pop Suppression (30 μV_{RMS})

Highly Efficient Class-H Boost Converter

- Programmable Boost Voltage of up to 12V
- Class H Envelope Tracking in 0.177 V step
- 78% Power Efficiency @ 1W Output Power, 5V Battery

Device Protection

- Under/Over Voltage Lock Out
- Over Current Protection
- Over Temperature Protection
- Clock Termination Protection

Programmable Serial Interfaces:

- I2C Interface
- I2S/PCM/TDM Interface

ALC

- Battery Tracking Limiter
- Brownout Prevention
- Battery Supply Current Limiter

Speaker Control Algorithm

- Klippel Controlled Sound (KCS) technology
- Integrated in Tensilica HiFi Audio DSP
- Adaptive nonlinear control based on I/V sensing
- Modeling dominant speaker nonlinearities (electrical, mechanical, acoustical)
- Active cancelation of harmonic distortion (THD), intermodulation (IMD) and DC-displacement generated by speaker nonlinearities
- Detection and compensation of speaker parameter changes due to aging, climate, load
- Measurement of voice coil rest position and active compensation of any coil offset x_{off}
- Predictive protection against mechanical and thermal overload (minimum latency < 0.05 ms)
- On-line diagnostic of the speaker properties (fatigue, speaker failures)

Package

- 50-Ball Wafer Level Chip Scale Package (WLCSP) (0.5 mm Pitch)

Applications

- Smartphones / Tablets
- Notebooks / Personal Computers / All In One PC
- Smart Speakers
- Home Appliances

Block Diagram

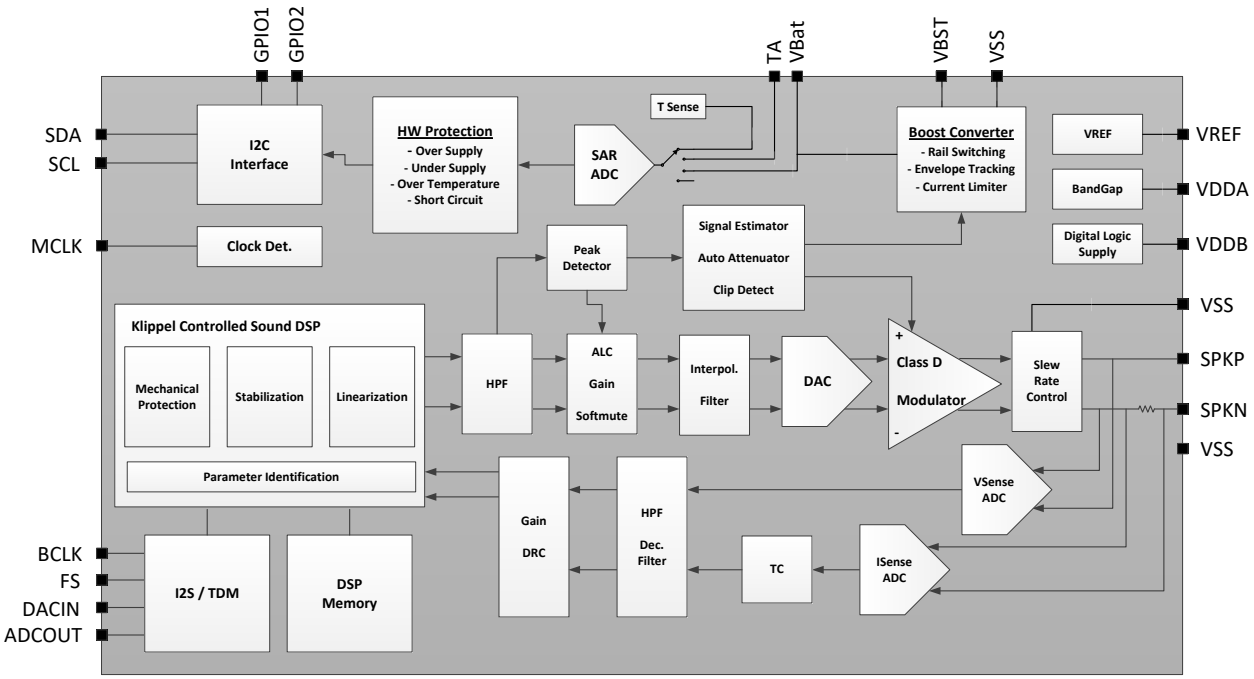


Figure 1: NAU83G10 Block Diagram

Pin Diagram

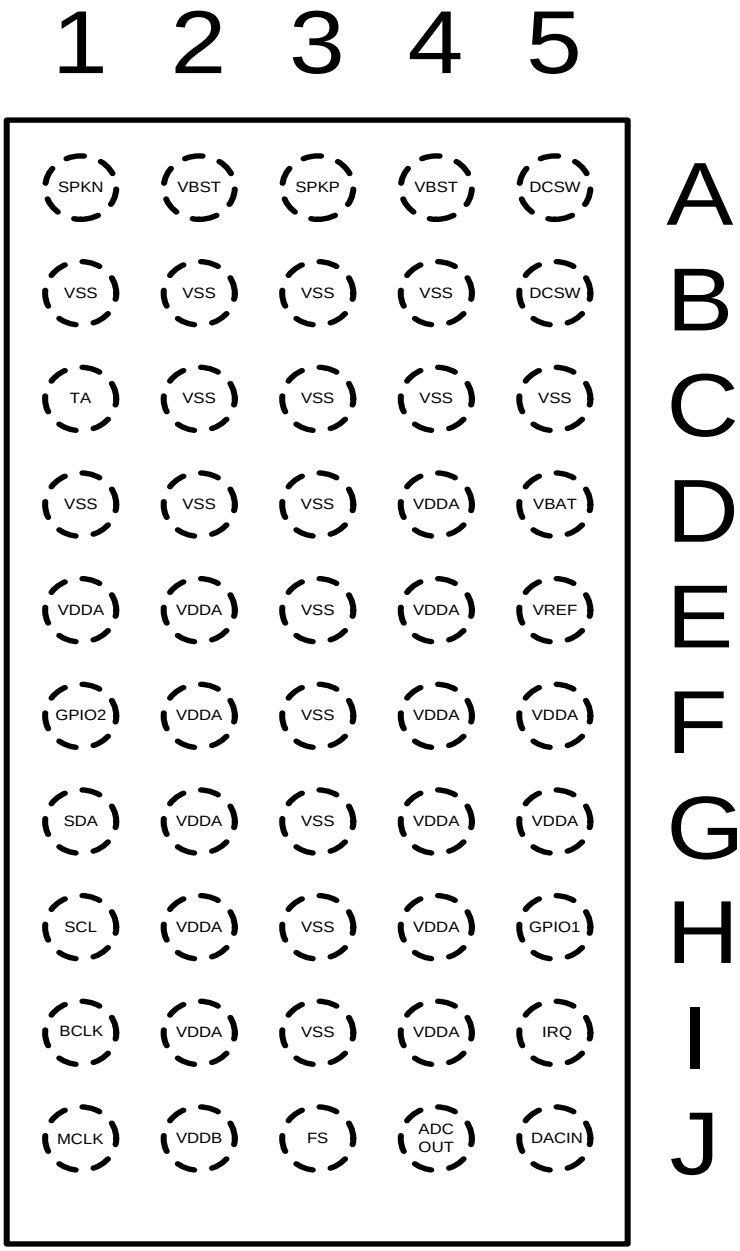


Figure 2: NAU83G10 Pin Diagram

Pin Descriptions

Table 1 NAU83G10 Pin Descriptions

Pin #	Name	Type	Description
A1	SPKN	Analog Output (VBST)	Class-D Negative Speaker Output Terminal
A2	VBST	Analog I/O (VBST)	DC-DC Boost Converter Output
A3	SPKP	Analog Output (VBST)	Class-D Positive Speaker Output Terminal
A4	VBST	Analog I/O (VBAT)	DC-DC Boost Converter Output
A5	DCSW	Analog I/O (VBAT)	DC-DC Boost Converter Switch
B1	VSS	Ground	Supply Ground
B2	VSS	Ground	Supply Ground
B3	VSS	Ground	Supply Ground
B4	VSS	Ground	Supply Ground
B5	DCSW	Analog I/O (VBST)	DC-DC Boost Converter Switch
C1	TA	Analog Input (VDDA)	Ambient Temperature Sense Input, tie to VSS if not used
C2	VSS	Ground	Supply Ground
C3	VSS	Ground	Supply Ground
C4	VSS	Ground	Supply Ground
C5	VSS	Ground	Supply Ground
D1	VSS	Ground	Supply Ground
D2	VSS	Ground	Supply Ground
D3	VSS	Ground	Supply Ground
D4	VDDA	Supply	Analog & Core Supply Voltage
D5	VBAT	Supply	Battery Supply Voltage
E1	VDDA	Supply	Analog & Core Supply Voltage
E2	VDDA	Supply	Analog & Core Supply Voltage
E3	VSS	Ground	Supply Ground
E4	VDDA	Supply	Analog & Core Supply Voltage
E5	VREF	Analog I/O (VDDA)	Internal DAC & ADC Voltage Reference Decoupling I/O
F1	GPIO2	Digital I/O (VDDB)	General Purpose IO2/Address Selection 2
F2	VDDA	Supply	Analog & Core Supply Voltage
F3	VSS	Ground	Supply Ground
F4	VDDA	Supply	Analog & Core Supply Voltage
F5	VDDA	Supply	Analog & Core Supply Voltage
G1	SDA	Digital I/O (VDDB)	Serial Data for I2C

Pin #	Name	Type	Description
G2	VDDA	Supply	Analog & Core Supply Voltage
G3	VSS	Ground	Supply Ground
G4	VDDA	Supply	Analog & Core Supply Voltage
G5	VDDA	Supply	Analog & Core Supply Voltage
H1	SCL	Digital Input (VDDB)	Serial Data Clock for I2C
H2	VDDA	Supply	Analog & Core Supply Voltage
H3	VSS	Ground	Supply Ground
H4	VDDA	Supply	Analog & Core Supply Voltage
H5	GPIO1	Digital I/O (VDDB)	General Purpose IO1/Address Selection 1
I1	BCLK	Digital I/O (VDDB)	Serial Audio Data Bit Clock I2S/PCM Input
I2	VDDA	Supply	Analog & Core Supply Voltage
I3	VSS	Ground	Supply Ground
I4	VDDA	Supply	Analog & Core Supply Voltage
I5	IRQ	Digital Output (VDDB)	Programmable Interrupt Output
J1	MCLK	Digital Input (VDDB)	Master Clock
J2	VDDB	Supply	Digital IO Supply
J3	FS	Digital I/O (VDDB)	Frame Sync I2S/PCM Input
J4	ADCOUT	Digital Output (VDDB)	Serial Audio I2S/PCM Data Output
J5	DACIN	Digital Input (VDDB)	Serial Audio Data I2S/PCM Input

Electrical Characteristics

Absolute Maximum Ratings

CAUTION: Do not operate at or near maximum ratings extended periods. Stresses above those listed in Table 2 may cause permanent damage to the device. Exposure to conditions beyond these ratings may adversely affect the life and reliability of the device and result in failures not covered by warranty.

Table 2 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDDB Digital I/O Supply Range	-0.3	4.0	V
VBAT Battery Supply Range	-0.3	6.0	V
VDDA Analog Supply Range	-0.3	2.2	V
Voltage Input Analog Range	VSS - 0.3	VDDA + 0.3	V
Voltage Input I/O Range	VSS - 0.3	VDDB + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

Operating Conditions

Table 3 Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	VBAT	2.90	4.2	5.50	V
Analog Supply Range	VDDA	1.62	1.8	1.98	V
Digital I/O Supply Range	VDDB	1.62	3.0	3.6	V
Ground	VSS		0		V
Industrial Operating Temperature		-40		+85	°C

CAUTION: The following conditions needed to be followed for regular operation: $V_{BAT} > V_{DD}A -1.2V$; VDDB > VDDA – 0.6V.

Electrical Parameters

Table 4 Electrical Parameters

Conditions: $V_{DD}A = V_{DD}B = 1.8V$; $V_{BAT} = 4.2V$. $R_L = 8\ \Omega + 33\ \mu H$, f = 1kHz, 48kHz sample rate, MCLK=12.88MHz, Boost Inductor = 1 µH , unless otherwise specified. Limits apply for $T_A = 25°C$

Symbol	Parameter		Conditions	Typical	Limit	Units
ISD	Shutdown Supply Current	$V_{DD}A$	all clocks off	12.0		µA
		$V_{DD}B$	all clocks off	0.3	2	
		V_{BAT}	all clocks off	0.4	4	
ISB	Standby Mode Supply Current	$V_{DD}A$	clocks off, clock gating on	12.0		µA
		$V_{DD}B$	clocks off, clock gating on	0.3		µA
		V_{BAT}	clocks off, clock gating on	0.4		µA
IDD	Operating Mode Supply Current	$V_{DD}A$	idle Channel, DSP off	7.6		mA
		$V_{DD}B$	idle Channel, DSP off	0.2		mA
		V_{BAT}	idle Channel, DSP off	3		mA
Class-D Channel						
P_O	Output Power		RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	6		W
			RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	6.5		W
			RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%	6.5		W
			RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%	8		W
THD+N	Total Harmonic Distortion + Noise		$R_L = 8\ \Omega + 33\ \mu H$, f=1kHz, $P_O = 1$ W	0.021		%
e_{OS}	Output Noise		A-Weighted, 20Hz-20kHz, Receiver mode or Auto attenuate, no DAC input signal, gain = 0dB	12		µVrms
			A-Weighted, 20Hz-20kHz, no DAC input signal, gain = 17.5dB	55		µVrms
PSRR	Power Supply Rejection Ratio		DC, V_{BAT} = 2.9V – 5.5V, GAIN = 17.5dB	92		dB
			f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	92		dB
			f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	92		dB
			f_{RIPPLE} = 4kHz, V_{RIPPLE} = 200mV_{P_P} GAIN = 17.5dB	88		dB
Fres	Frequency Response		F = 20Hz ~ 20KHz, 1Watt, $R_L = 8\ \Omega + 33$ µH	+-0.8		dB
V_{OS}	Output Offset Voltage		Idle Channel, Gain= 0dB	±0.7	±5	mV
Kpop	Pop and Click Noise		A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off	0.03		mVrms

Symbol	Parameter	Conditions	Typical	Limit	Units
		A-weighted, Idle DAC input, toggling between -120dBFs DAC In & 2048 zero samples	0.03		mVrms
Rdson-P	Driver P MOS-FET ON-resistance	V_{BAT}= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.127		Ohm
Rdson-N	Driver N MOS-FET ON- resistance	V_{BAT}= 5.0V. R_L = 8 Ω + 33 µH, DC Output Clipping	0.129		Ohm
Fsw	Switching Frequency	Average	300		kHz
Voltage Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise	VBAT = 5.5V, +10dBVrms, Class-D off	0.004		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	101		dB
FS_{ADC}	ADC Full Scale Input Level		15.4		V_{PK}
Current Sense ADC					
THD+N	ADC Total Harmonic Distortion + Noise		0.37		%
SNR	Signal to Noise Ratio	Flat, 20Hz – 20kHz	82		dB
FS_{ADC}	ADC Full Scale Input Level		4.04		A_{PK}
Battery Sense ADC					
INL	Integrated Non-Linearity	V_{BAT}= 2.9V-5.5V (gain & offset compensated)	+/-1		LSB
DNL	Differential Non-Linearity	V_{BAT}= 2.9V-5.5V	+/-1		LSB
Boost Converter					
Fsw	Switching Frequency		2.0		MHz
Vbstmax	Boost Converter Maximum Output Voltage		12		V
Vbstmin	Boost Converter Minimum Output Voltage		2.9		V
Vbststp	Boost Converter Step Voltage		0.177		V
Vovp	Boost Converter Overvoltage Protection Threshold		14		V
Rdson-P	Boost Converter P MOS-FET ON-resistance		0.1		Ohm
Rdson-N	Boost Converter N MOS-FET ON-resistance		0.1		Ohm
Boost Converter + Class-D					
Neff	Power Efficiency	Output Power = 0.45 W, VBAT= 5.0 V	78		%
		Output Power = 1.0 W, VBAT = 5.0 V	78		%
		Output Power = 6.0 W, VBAT = 5.0 V	70		%

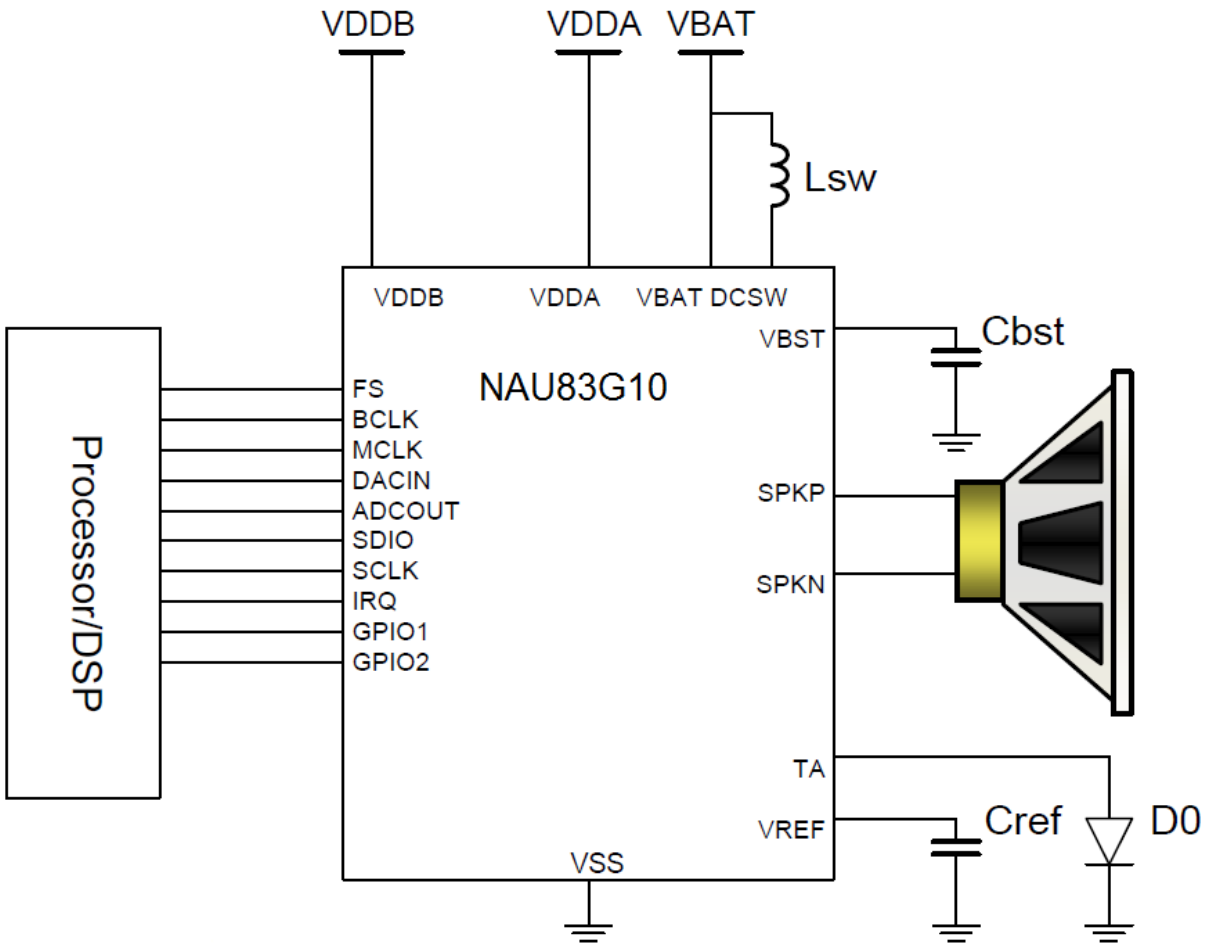
Digital I/O Characteristics

Table 5 Digital I/O Characteristics

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	$V_{DD}B$ = 1.8V			0.33*$V_{DD}B$	V
		$V_{DD}B$ = 3.3V			0.37*$V_{DD}B$	
Input HIGH level	V_{IH}	$V_{DD}B$ = 1.8V		0.67*$V_{DD}B$		V
		$V_{DD}B$ = 3.3V		0.63*$V_{DD}B$		
Output HIGH level	V_{OH}	I_{Load}= 1mA	$V_{DD}B$=1.8V	0.9*$V_{DD}B$		V
			$V_{DD}B$ = 3.3V	0.95*$V_{DD}B$		
Output LOW level	V_{OL}	I_{Load}= 1mA	$V_{DD}B$ = 1.8V		0.1*$V_{DD}B$	V
			$V_{DD}B$=3.3V		0.05*$V_{DD}B$	

System Diagram

Figure 3 System Diagram



Ordering Information

Table 6 Ordering Information

Part Number	Dimension	Package	Package Material
NAU83G10VG	2.57mm x 5.28mm	WLCSP 50-Balls	Green

NAU83G10VG = Part Name

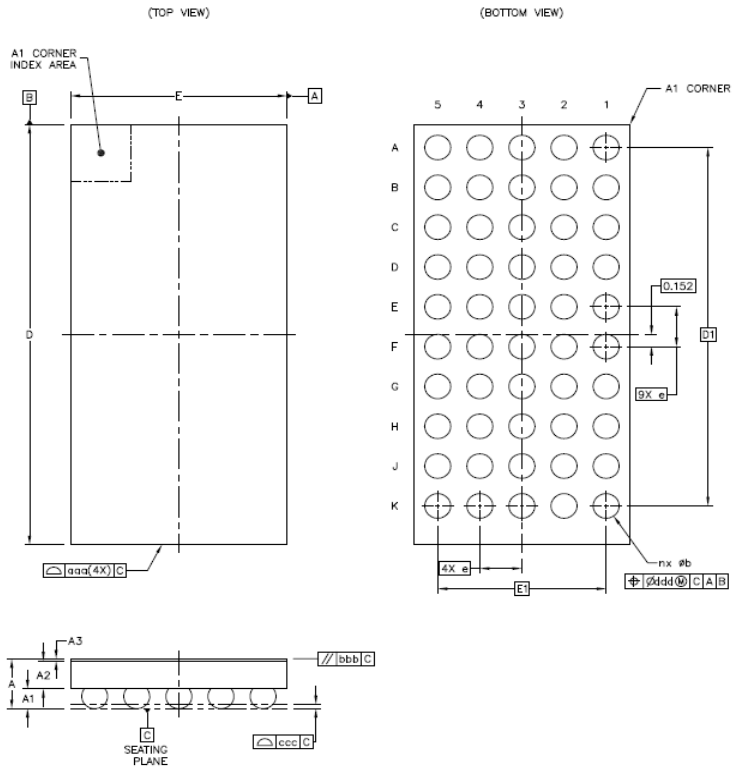
G = indicates Green Speaker Amplifier based on Klippel Control Sound (KCS)

V = indicates WLCSP packaging WLCSP

G = Lead-Free (Green) Packaging:

Package Information

Figure 4 WLCSP Package Dimentions (50 Balls with 0.5mm Pitch)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.567	0.625	0.683
STAND OFF		A1	0.22	---	0.28
WAFER THICKNESS		A2	0.325	0.35	0.375
FILM THICKNESS		A3	0.022	0.025	0.028
BODY SIZE	X	E	2.57		
	Y	D	5.28		
BALL/BUMP PITCH	X	SE	---		BSC
	Y	SD	---		BSC
EDGE BALL CENTER TO CENTER	X	E1	2		BSC
	Y	D1	4.5		BSC
PITCH		e	0.5		BSC
BALL DIAMETER (SIZE)			0.3		
BALL/BUMP WIDTH		b	0.28	---	0.34
BALL/BUMP COUNT		n	50		
PACKAGE EDGE TOLERANCE		aaa	0.03		
WAFER FLATNESS		bbb	0.06		
COPLANARITY		ccc	0.05		
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015		

Revision History

Table 7: Revision History

Version			Description
#	Date	Page(s)	
0.1	Apr 23, 2018	NA	Prelimnary Version
0.2	Sep 25, 2019		Updated
0.3	Oct 11, 2019		Added Klippel Logo, Updated with changes from Klippel
1.0	Apr 24, 2020	All	Update Document Format
1.1	July 17, 2020	1, 2, 12	Corrected the package dimension, and revised the output power SPEC for 4ohm load

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