

## Single P-channel MOSFET

# KFJ4B0421ZL

## Datasheet

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## 1. GENERAL DESCRIPTION

Single P-channel MOSFET for automotive.

## 2. FEATURES

- Drain-source On-state Resistance:  $R_{DS(on)}$  typ = 74 m $\Omega$  ( $V_{GS} = -10$  V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

## 3. MARKING SYMBOL: 1V

## 4. PACKAGING

Embossed type (Thermo-compression sealing): 20,000 pcs / reel (standard)

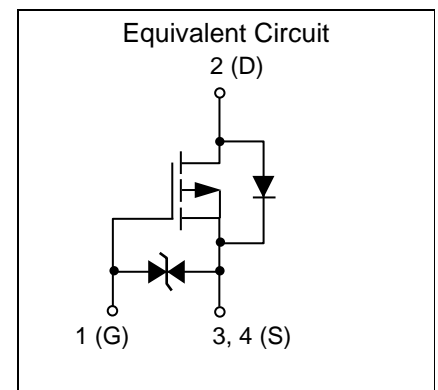
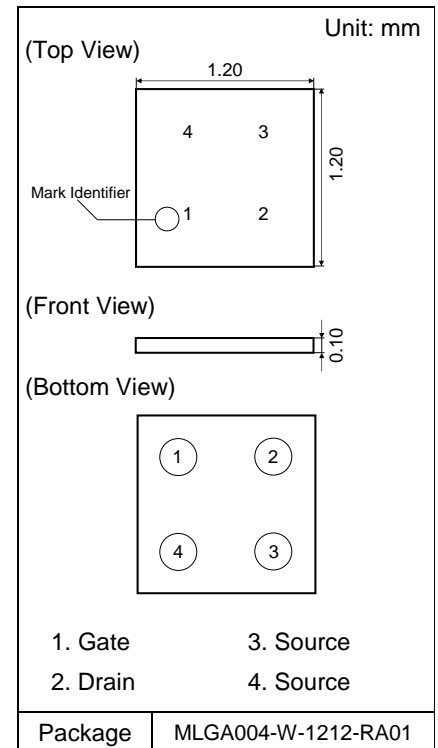
## 5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter		Symbol	Rating	Unit
Drain-source Voltage		VDS	- 40	V
Gate-source Voltage		VGS	- 20 / + 10	V
Drain Current	DC <sup>*1</sup>	ID1	- 2.0	A
	DC <sup>*2</sup>	ID2	- 3.2	
	DC <sup>*3</sup>	ID3	- 4.2	
	Pulsed <sup>*4</sup>	IDp	- 25.6	
Total Power Dissipation	DC <sup>*1</sup>	PD1	0.42	W
	DC <sup>*2</sup>	PD2	1.00	
	DC <sup>*3</sup>	PD3	1.70	
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C

## 6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 <sup>*1</sup>	300	°C / W
	Rth2 <sup>*2</sup>	125	
	Rth3 <sup>*3</sup>	73	

- Note
- \*1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad (65.4 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (616 mm<sup>2</sup> area, 36  $\mu\text{m}$  thickness).
  - \*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
  - \*4  $t = 10$   $\mu\text{s}$ , Duty Cycle  $\leq 1\%$ .



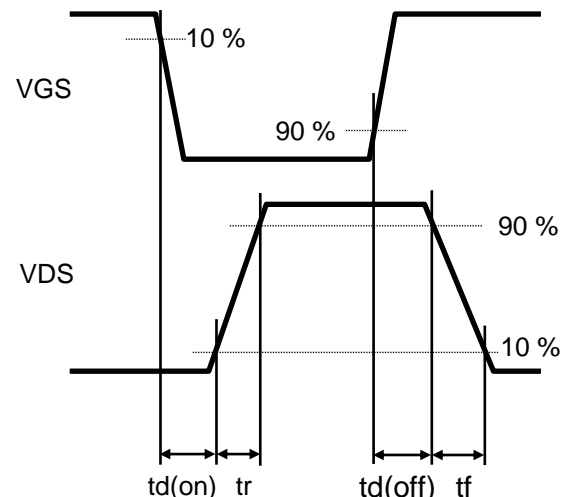
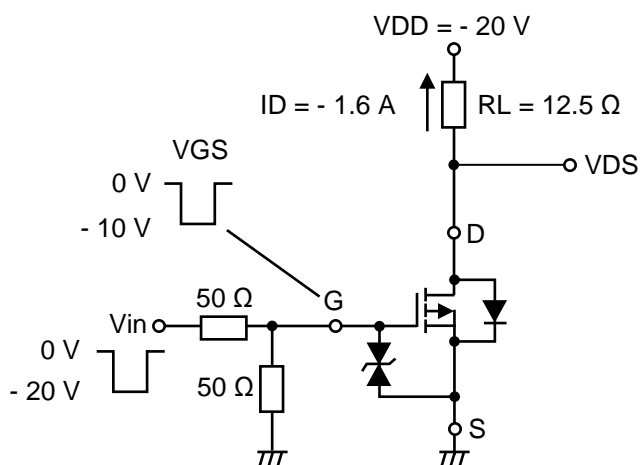
7. ELECTRICAL CHARACTERISTICS  $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$ 

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	VDSS	ID = - 1 mA, VGS = 0 V	- 40			V
Zero Gate Voltage Drain Current	IDSS	VDS = - 40 V, VGS = 0 V			- 1	$\mu\text{A}$
Gate-source Leakage Current	IGSS	VGS = - 16 V, VDS = 0 V			- 10	$\mu\text{A}$
		VGS = + 8 V, VDS = 0 V			10	
Gate-source Threshold Voltage	Vth	ID = - 3.02 mA, VDS = - 10 V	- 1	- 2	- 3	V
Drain-source On-state Resistance	RDS(on)1	ID = - 1.6 A, VGS = - 10 V	52	74	96	m $\Omega$
	RDS(on)2	ID = - 1.6 A, VGS = - 4.5 V	58	83	142	
Body Diode Forward Voltage	VF(s-d)	IF = - 1.6 A, VGS = 0 V		- 0.77	- 1.2	V
Input Capacitance <sup>*1</sup>	Ciss	VDS = - 20 V, VGS = 0 V f = 1 MHz		800		pF
Output Capacitance <sup>*1</sup>	Coss			70		
Reverse Transfer Capacitance <sup>*1</sup>	Crss			65		
Turn-on Delay Time <sup>*1, *2</sup>	td(on)	VDD = - 20 V, VGS = 0 to - 10 V		8		ns
Rise Time <sup>*1, *2</sup>	tr	ID = - 1.6 A		13		
Turn-off Delay Time <sup>*1, *2</sup>	td(off)	VDD = - 20 V, VGS = - 10 to 0 V		95		
Fall Time <sup>*1, *2</sup>	tf	ID = - 1.6 A		46		
Total Gate Charge <sup>*1</sup>	Qg1	VDD = - 20 V, VGS = - 4.5 V ID = - 3.2 A		8		nC
	Qg2	VDD = - 20 V, VGS = - 10 V ID = - 3.2 A		16		
Gate-source Charge <sup>*1</sup>	Qgs			2		
Gate-drain Charge <sup>*1</sup>	Qgd			4		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

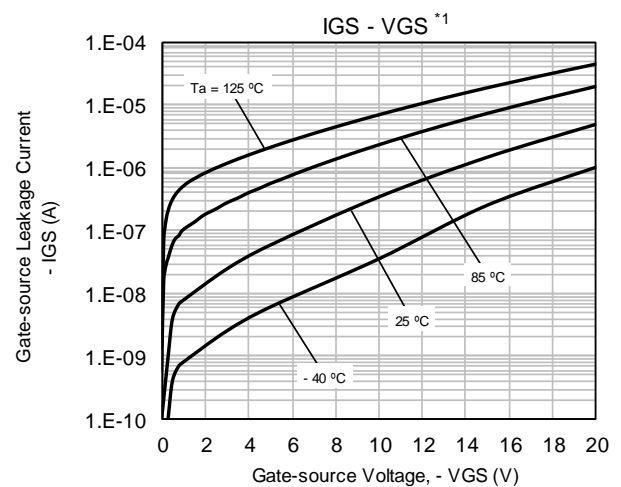
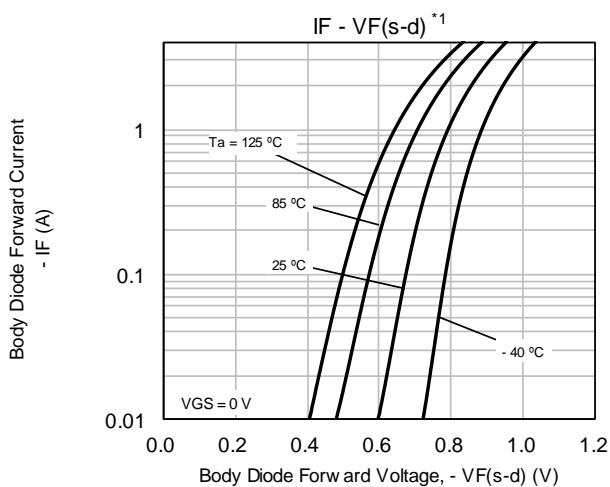
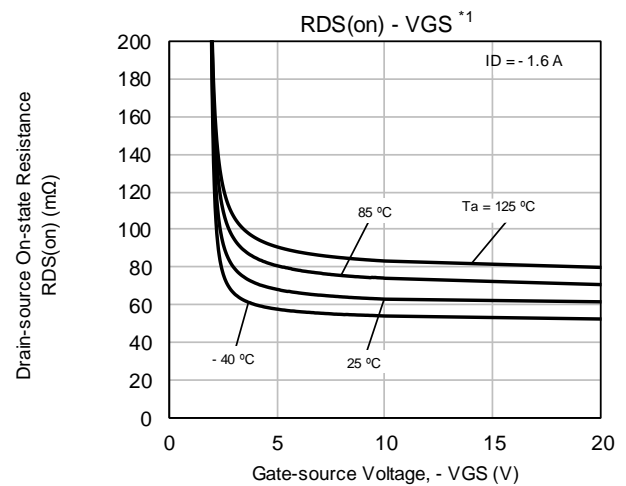
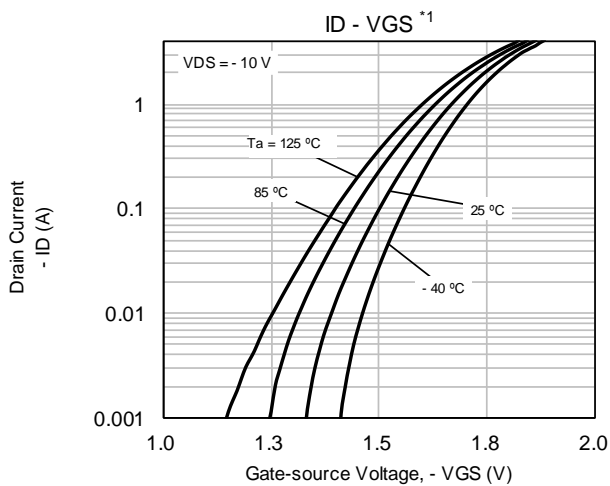
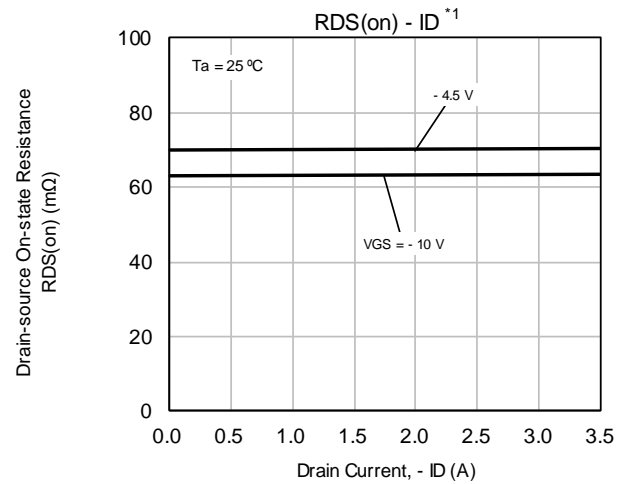
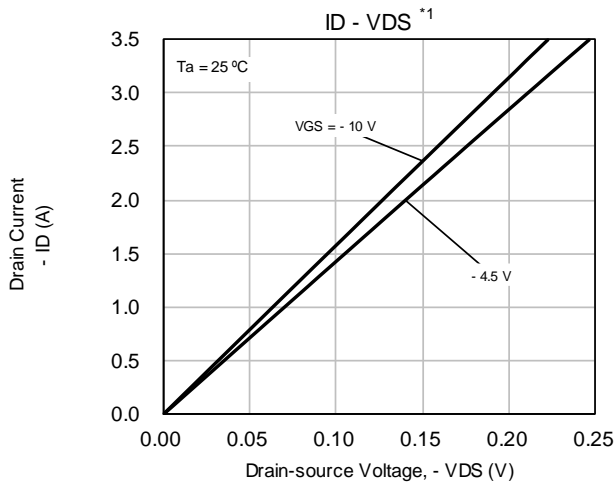
<sup>\*1</sup> Guaranteed by design, not subject to production testing.

<sup>\*2</sup> Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

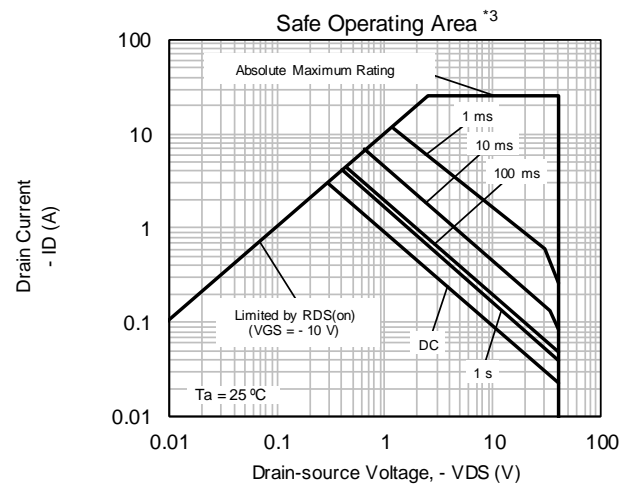
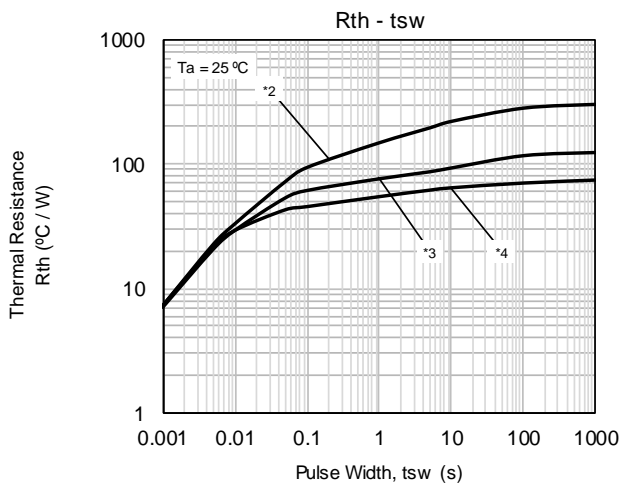
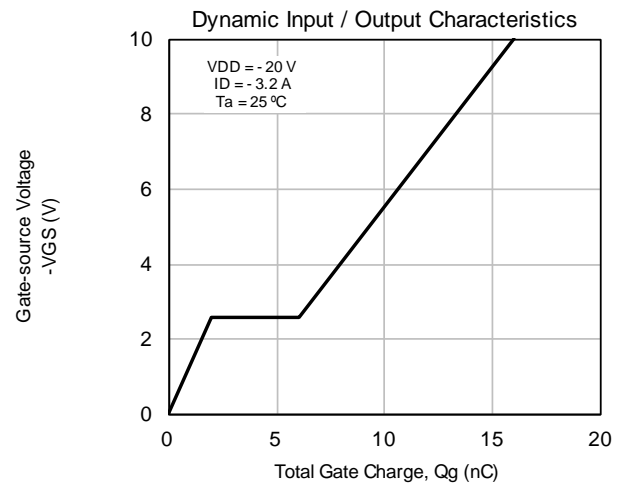
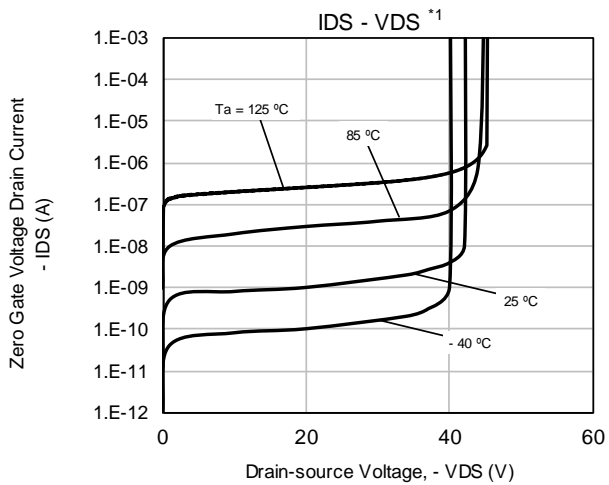
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC  $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$ 

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 k $\Omega$	H1C	> 1 to $\leq$ 2	kV

## 9. TECHNICAL DATA (Reference)



## TECHNICAL DATA (Reference)



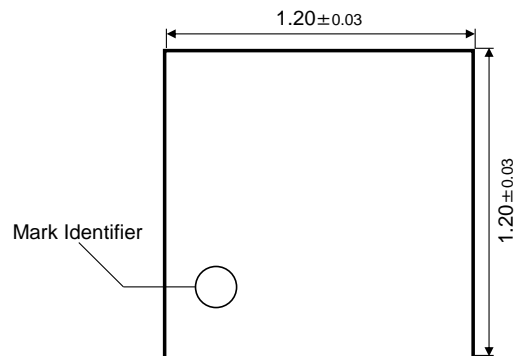
## Note

- \*1 Pulse measurement.
- \*2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board partially covered with copper pad ( 65.4 mm<sup>2</sup> area, 36 μm thickness ).
- \*3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).  
FR4 board fully covered with copper pad (616 mm<sup>2</sup> area, 36 μm thickness).
- \*4 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

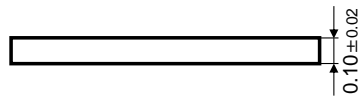
**10. OUTLINE**

(Top View)

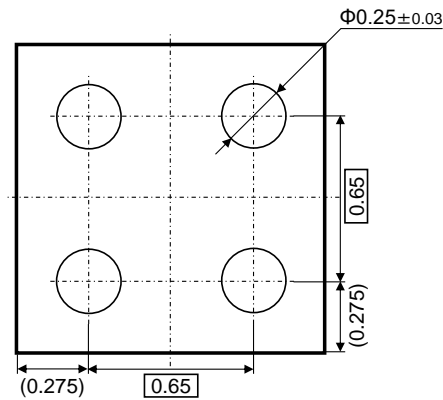
Unit: mm



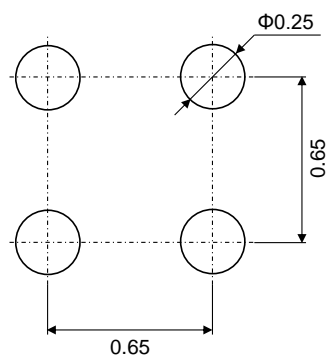
(Front View)



(Bottom View)

**11. LAND & STENCIL PATTERN (Reference)**

Unit: mm

**Important notice:**

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.

Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

**12. REVISION HISTORY**

Date	Revision	Description
2021.11.15	1.00	1. Initially issued.

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