KFK9B0652ZL

Single N-channel MOSFET

KFK9B0652ZL Datasheet

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KFK9B0652ZL

1. GENERAL DESCRIPTION

Single N-channel MOSFET for automotive.

2. FEATURES

- Drain-source On-state Resistance: RDS(on) typ = $18 \text{ m}\Omega \text{ (VGS = } 10 \text{ V)}$
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

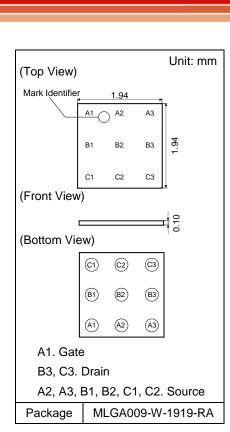
3. MARKING SYMBOL: WW

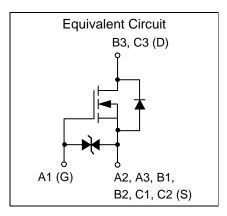
4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS Ta = $25 \degree C$

Parameter		Symbol	Rating	Unit	
Drain-source Voltage		VDS	60	V	
Gate-source Voltage		VGS	+ 20 / - 10	V	
Drain Current	DC *1	ID1	5.5		
	DC *2	ID2	8.3	٨	
	DC *3	ID3	10.0	A	
	Pulsed *4	IDp	66.4		
Total Power Dissipation	DC *1	PD1	0.71		
	DC *2	PD2	1.60	W	
	DC *3	PD3	2.31		
Operating Junction and Storage Temperature Range		Tj, Tstg	- 55 to + 150	°C	





6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
	Rth1 *1	175	
Thermal Resistance (ch-a)	Rth2 ^{*2}	79	°C / W
	Rth3 *3	54	

Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).

 $\label{eq:FR4} FR4 \mbox{ board partially covered with copper pad (79.2 \mbox{ mm}^2 \mbox{ area, 36 } \mu m \mbox{ thickness}).$

*3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).

*4 t = 10 $\mu s,~Duty~Cycle \leq$ 1 %.

FR4 board fully covered with copper pad (616 mm² area, 36 μ m thickness).

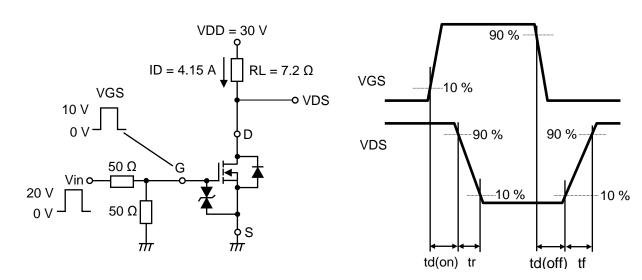
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7. ELECTRICAL CHARACTERISTICS Ta = $25 \degree C \pm 3 \degree C$

Parameter	Symbol	Conditions	Min	Тур	Max	Unit	
Drain-source Breakdown Voltage	VDSS	ID = 1 mA, VGS = 0 V	60			V	
Zero Gate Voltage Drain Current	IDSS	VDS = 60 V, VGS = 0 V			1	μA	
Gate-source Leakage Current	IGSS	VGS = + 16 V, VDS = 0 V			10	μA	
		VGS = - 8 V, VDS = 0 V			- 10		
Gate-source Threshold Voltage	Vth	ID = -1.85 mA, VDS = 10 V	1	2	3	V	
Drain aguras On state Registeres	RDS(on)1	ID = 2 A, VGS = 10 V	10	18	23	m0	
Drain-source On-state Resistance	RDS(on)2	ID = 2 A, VGS = 4.5 V	12	20	33	mΩ	
Body Diode Forward Voltage	VF(s-d)	IF = 2 A, VGS = 0 V		0.77	1.2	V	
Input Capacitance *1	Ciss	VDS = 30 V, VGS = 0 V		1400			
Output Capacitance *1	Coss			110		pF	
Reverse Transfer Capacitance *1	Crss	T = T MHZ		60			
Turn-on Delay Time *1, *2	td(on)	VDD = 30 V, VGS = 0 to 10 V		13			
Rise Time ^{*1, *2}	tr	$SS = \frac{VGS = + 16 V, VDS = 0 V}{VGS = -8 V, VDS = 0 V}$ th ID = -1.85 mA, VDS = 10 V 1 2 (on)1 ID = 2 A, VGS = 10 V 10 18 (on)2 ID = 2 A, VGS = 4.5 V 12 20 s-d) IF = 2 A, VGS = 0 V 0.77 ss VDS = 30 V, VGS = 0 V 1400 (ss f = 1 MHz 60 on) VDD = 30 V, VGS = 0 to 10 V 13 r ID = 4.15 A 25 off) VDD = 30 V, VGS = 10 to 0 V 80 f = 1 D = 4.15 A 60 yDD = 30 V, VGS = 4.5 V 13 ID = 4.15 A 60 yDD = 30 V, VGS = 4.5 V 13 ID = 8.3 A 13 yDD = 30 V, VGS = 10 V 4.5 ID = 8.3 A 4.5	25		1		
Turn-off Delay Time *1, *2	td(off)			80		ns	
Fall Time *1, *2	tf	ID = 4.15 A		60			
Total Gate Charge ^{*1}	Qg1	VDD = 30 V, VGS = 4.5 V		40			
		ID = 8.3 A	13				
	Qg2			26		nC	
Gate-source Charge *1	Qgs			4.5			
Gate-drain Charge *1	Qgd	ID = 0.3 A		5			

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors. *1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

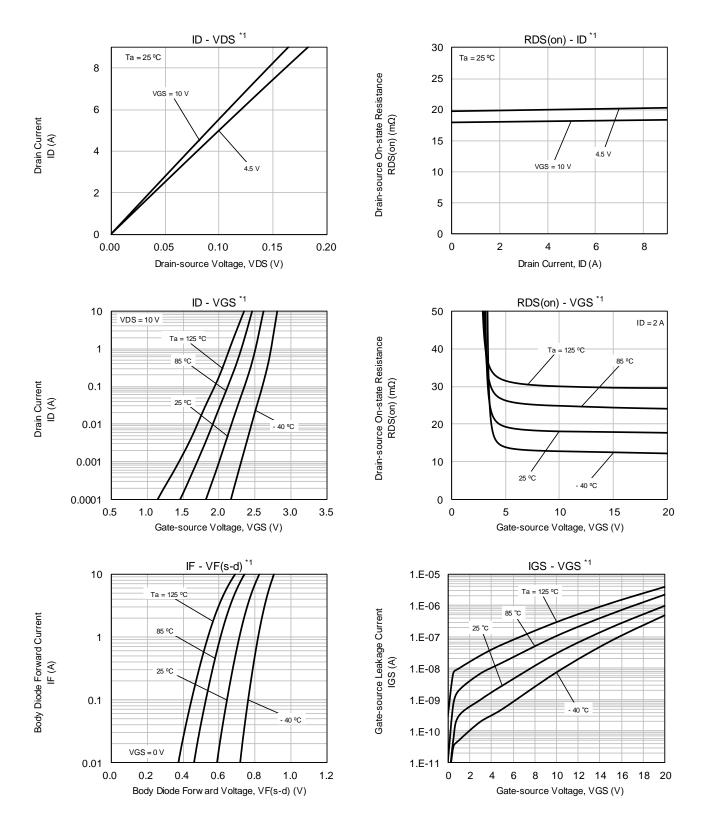


8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100 \text{ pF}, R = 1.5 \text{ k}\Omega$	H2	> 2 to \leq 4	kV

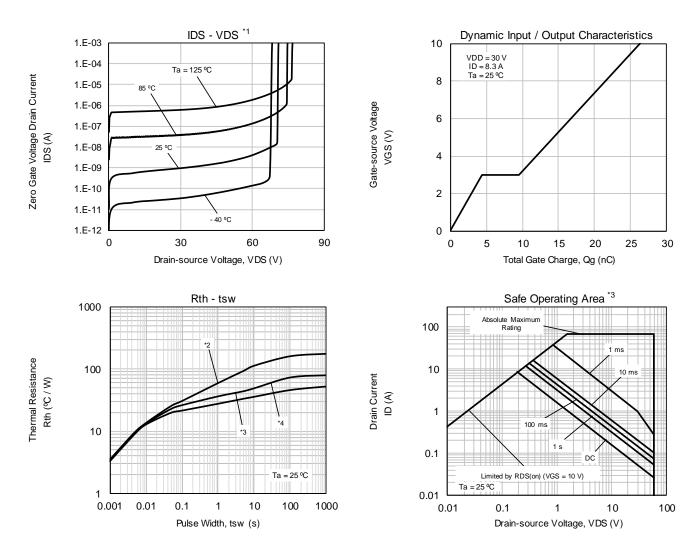
November 19, 2021

9. TECHNICAL DATA (Reference)



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TECHNICAL DATA (Reference)

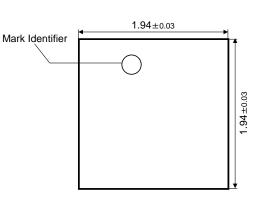


Note

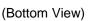
- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
- FR4 board partially covered with copper pad (79.2 mm² area, 36 μ m thickness). *3 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
- FR4 board fully covered with copper pad (616 mm^2 area, 36 μ m thickness).
- *4 Mounted on ceramic board (70 mm \times 70 mm \times t1.0 mm).

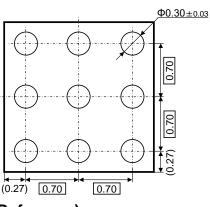
10. OUTLINE

(Top View)



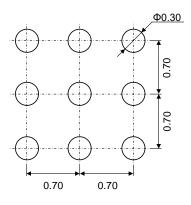
(Front View)





0.10±0.02

11. LAND & STENCIL PATTERN (Reference)



Unit: mm

Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design. Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

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Unit: mm

12. REVISION HISTORY

Date	Revision	Description	
2021.11.19	1.00	1. Initially issued.	

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