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8-BIT MICROCONTROLLER

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1. General Description

The W79E658 is a fast, 8051/52-compatible microcontroller with a redesigned processor core that eliminates wasted clock and memory cycles. Typically, the W79E658 executes instructions 1.5 to 3 times faster than that of the traditional 8051/52, depending on the type of instruction, and the overall performance is about 2.5 times better at the same crystal speed. As a result, with the fully-static CMOS design, the W79E658 can accomplish the same throughput with a lower clock speed, reducing power consumption.

The W79E658 provides 256 bytes of on-chip RAM; 1-KB of auxiliary RAM; seven 8-bit, bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; an UART serial port, 2 channels of I2C with master/slave capability and 8 channels of 10-bit ADC. These peripherals are all supported by ten interrupt sources with 2 levels of priority.

The W79E658 contains a 128-KB Flash EPROM whose contents may be updated in-system by a loader program stored in an auxiliary, 4-KB Flash EPROM. Once the contents are confirmed, it can be protected for security.

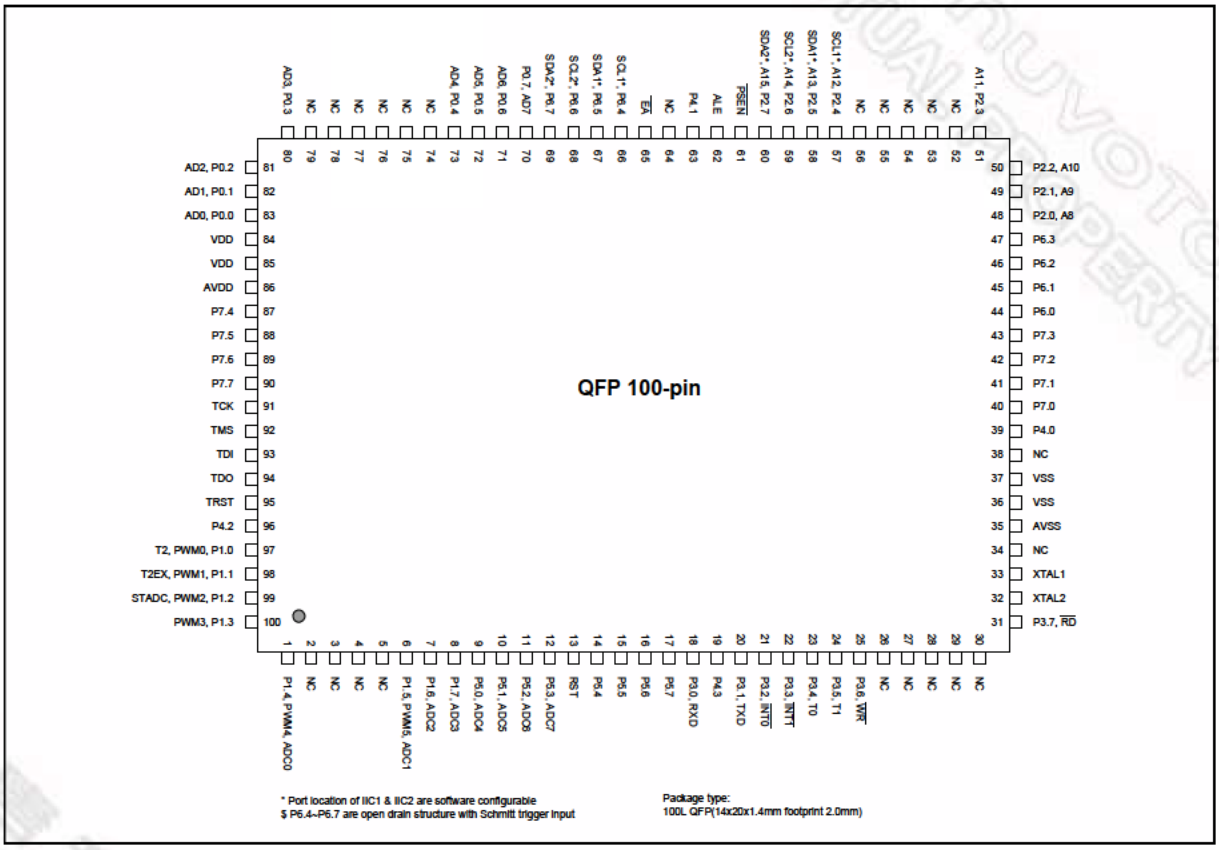
Note: If the applied V_{DD} is not stable, especially with long transition time of power on/off, it's recommended to apply an external RESET IC to the RST pin for improving the stability of system.

2. Features

- Fully-static-design 8-bit Turbo 51 CMOS microcontroller up to 40MHz
- 128-KB of in-system-programmable Flash EPROM (AP Flash EPROM with ISP)
- 4-KB of Auxiliary Flash EPROM for the loader program (LD Flash EPROM)
- 1-KB auxiliary RAM, software-selectable, accessed by MOVX instruction
- 256 bytes of scratch-pad RAM
- Seven 8-bit bi-directional ports
- All pins with Schmitt trigger inputs
- One 4-bit multipurpose I/O port4 with Chips select(CS) and boot function
- Three 16-bit timers
- 6 channels of 8-bit PWM
- One enhanced full-duplex UART with framing-error detection and automatic address recognition
- 2-channels of I2C with master/slave capability
- 10-bit ADC with 8-channel inputs
- Software programmable access cycle to external RAM/peripherals
- 10 interrupt sources with two levels of priority
- Software reset function
- Optional H/L state of ALE/PSEN during power down mode
- Built-in power management
- Code protection
- Development tool
  - JTAG ICE(In Circuit Emulator) tool
- Packages:
  - Lead Free(RoHS) QFP 100: W79E658A40FL, W79L658A25FL

DEVICE	OPERATING FREQUENCY	OPERATING VOLTAGE	PACKAGE
			LEAD FREE(ROHS)
W79E658A40FL	up to 40MHz	4.5V ~ 5.5V	QFP100
W79L658A25FL	up to 25MHz	3.0V ~ 4.5V	QFP100

3. Pin Configuration



* Port location of IIC1 & IIC2 are software configurable
$ P6.4~P6.7 are open drain structure with Schmitt trigger input

Package type:
100L QFP(14x20x1.4mm footprint 2.0mm)

4. Pin Description

SYMBOL	TYPE[1]	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data are not presented on the bus if the $\overline{EA}$ pin is high.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE enables the address latch that separates the address from the data on Port 0.
RST	I L	**RESET:** Set this pin high for two machine cycles while the oscillator is running to reset the device.
XTAL1	I	**CRYSTAL 1:** Crystal oscillator input or external clock input.
XTAL2	O	**CRYSTAL 2:** Crystal oscillator output.
V_{SS}	I	**GROUND**: ground potential.
V_{DD}	I	**POWER SUPPLY:** Supply voltage for operation.
AV_{SS}	I	**Analog GROUND:** for ADC
AV_{DD}	I	**Analog Power Supply:** for ADC
P0.0–P0.7	I/O D S H	**PORT 0:** 8-bit bi-directional I/O port with internal pull-up resisters This port also provides a multiplexed, low-order address / data bus during accesses to external memory.
P1.0–P1.7	I/O S H	**PORT 1:** 8-bit, bi-directional I/O port with internal pull-up resistors. This port also provides alternate functions as below. P1.0 ~ P1.5 provide PWM0 ~ PWM5. P1.4 ~ P1.7 provide ADC0 ~ ADC3. P1.0 alternately provides Timer2 external count input.(T2) P1.1 alternately provides Timer2 Reload/Capture/Direction control.(T2Ex)
P2.0–P2.7	I/O S H	**PORT 2:** 8-bit, bi-directional I/O port with internal pull-ups. This port also provides the upper address bits when accessing external memory. P2.4 to P2.7 can be software configured as I2C serial ports
P3.0–P3.7	I/O S H	**PORT 3:** 8-bit, bi-directional I/O port with internal pull-up resistors. All bits have alternate functions, which are described below: RXD (P3.0): Serial Port 0 input TXD (P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2): External Interrupt 0 $\overline{INT1}$(P3.3): External Interrupt 1 T0 (P3.4):Timer 0 External Input T1 (P3.5):Timer 1 External Input $\overline{WR}$ (P3.6): External Data Memory Write Strobe $\overline{RD}$ (P3.7): External Data Memory Read Strobe

PIN DESCRIPTION, continued

SYMBOL	TYPE	DESCRIPTIONS
P4.0–P4.3	I/O S H	**PORT 4:** 4-bit bi-directional I/O port. The P4.3 also provides the alternate function $\overline{\text{REBOOT}}$ which is H/W reboot from LD flash.
P5.0-P5.7	I/O H	**PORT 5:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable. The alternate functions of P5.0 to P5.3 are inputs of ADC4 to ADC7.
P6.0-P6.7	I/O D H	**PORT 6:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable. Pins P6.4 to P6.7 are open drain type and can be software configured as the I2C ports.
P7.0-P7.7	I/O H	**PORT 7:** A bi-directional I/O port with internal pull-ups. This port is not bit-addressable.
TCK[2]	I H	Used in debug mode with internal pull-up
TMS[2]	I H	Used in debug mode with internal pull-up
TDI[2]	I H	Used in debug mode with internal pull-up
TDO[2]	O L	Used in debug mode with internal weakly pull-low
TRST[2]	I H	Used in debug mode with internal pull-up

Note: 1. TYPE I : input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain S: Schmitt Trigger
2. Keep debug pins in NC(no connection) if chip is not in debug mode.

4.1 Port 4

SFR P4 at address A5H, is a 4-bit multipurpose programmable I/O port which functions are I/O, insert wait function and chip-select function. The Port 4 has four different operation modes:

In mode 0, P4.0 ~ P4.3 is a 4-bit bi-directional I/O port which is the same as port 1. The default Port 4 is a general I/O function.

In mode1, P4.0 ~ P4.3 are read data strobe signals which are synchronized with $\overline{\text{RD}}$ signal at specified addresses. These read data strobe signals can be used as chip-select signals for external peripherals.

In mode2, P4.0 ~ P4.3 are write data strobe signals which are synchronized with $\overline{\text{WR}}$ signal at specified addresses. These write data strobe signals can be used as chip-select signals for external peripherals.

In mode3, P4.0 ~ P4.3 are read/write data strobe signals which are synchronized with $\overline{\text{RD}}$ or $\overline{\text{WR}}$ signal at specified addresses. These read/write data strobe signals can be used as chip-select signals for external peripherals.

In mode1~mode3, Port 4 is configured with the feature of chip-select signals, the address range for chip-select signals depends on the contents of registers P4xAH and P4xAL, which contain the high-order byte and low-order byte, respectively, of the 16-bit address comparator for P4.x. The registers P4CONA and P4CONB contain the control bits to configure the Port 4 operation mode. This is illustrated in the following schematic.

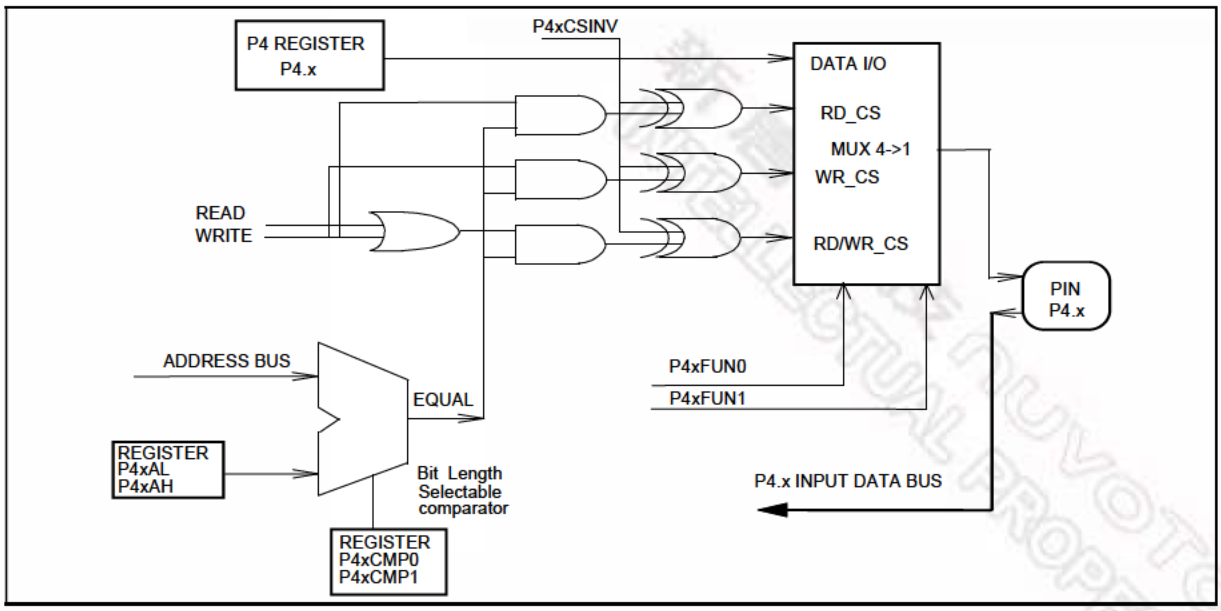


Figure 4-1

For example, the following program sets up P4.0 as a write-strobe signal for I/O port addresses 1234H – 1237H with positive polarity, while P4.1 – P4.3 are used as general I/O ports.

```
MOV  P40AH, #12H
MOV  P40AL, #34H      ; Base I/O address 1234H for P4.0
MOV  P4CONA, #00001010B    ; P4.0 is a write-strobe signal; address lines A0 and A1 are masked.
MOV  P4CONB, #00H   ; P4.1 – P4.3 are general I/O ports
MOV  P2ECON, #10H   ; Set P40SINV to 1 to invert the P4.0 write-strobe to positive polarity.
```

Then, any instruction MOVX @DPTR, A (where DPTR is in 1234H – 1237H) generates a positive-polarity, write-strobe signal on pin P4.0, while the instruction MOV P4, #XX puts bits 3 – 1 of data #XX on pins P4.3 – P4.1.

5. Memory Organization

The W79E658 separates the memory into two separate sections, the Program Memory and the Data Memory. Program Memory stores instruction op-codes, while Data Memory stores data or memory-mapped devices.

5.1 Program Memory (on-chip Flash)

The Program Memory on the standard 8052 can only be addressed to 64 Kbytes long. By invoking the banking methodology, W79E633 can extend to two 64KB flash EPROM banks, AP Flash0 (AP0) and AP Flash1 (AP1). All instructions are fetched from this area, and the MOVC instruction can also access this region. There is an auxiliary 4-KB Flash EPROM (LD Flash EPROM), where the loader program for In-System Programming (ISP) resides. Both AP Flash banks are re-programmed by serial or parallel download according to this loader program.

The default active bank is AP0. User can set the EN128K bit to switch from AP0 to AP1 as well as properly set DCP1[2:0] to select one pin of Port1 to be the A16 to access the AP1 address region.

ROM Banking Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	EN128K	DCP12	DCP11	DCP10

Mnemonic: ROMCON Address: ABh

EN128K On-chip ROM banking enable. Set this bit to enable AP Flash0 and AP Flash1 by banking mechanism. The P1.x is selected to be the auxiliary highest address line A16.

DCP1[2:0] A16 selection. By default, P1.7 is defined as A16.

A16	P1.0	P1.1	P1.2	P1.3	P1.4	P1.5	P1.6	P1.7
DCP1[2:0]	000	001	010	011	100	101	110	111

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5.2 Data Memory

The W79E658 can access up to 64Kbytes of external Data Memory. This memory region is accessed by the MOVX instructions. Unlike the 8051 derivatives, the W79E658 contains on-chip 1K-bytes of Data Memory, which only can be accessed by MOVX instructions. The 1-Kbytes of SRAM located between address 0000h and 03FFh is enabled by setting DMEO bit of PMR register. If MOVX instruction accesses the addresses greater than 03FFh CPU will automatically access external memory through Port 0 and 2. In default condition the 1K-bytes SRAM is disabled and any MOVX directed to the space between 0000h and FFFFh goes to the expanded bus on the Port 0 and 2. The W79E658 also has the standard 256 bytes of on-chip Scratchpad RAM. This can be accessed either by direct addressing or by indirect addressing. There are also some Special Function Registers (SFRs), which can only be accessed by direct addressing. Since the Scratchpad RAM is only 256 bytes, it can be used only when data contents are small.

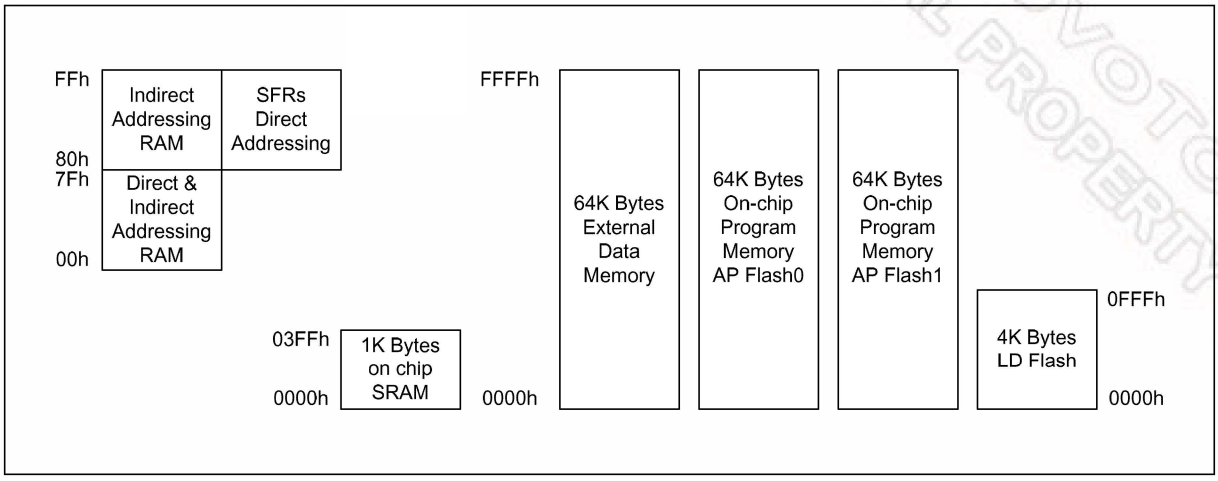


Figure 5-1 Memory Map

6. Special Function Registers

The W79E658 uses Special Function Registers (SFR) to control and monitor peripherals. The SFR reside in register locations 80-FFh and are only accessed by direct addressing. The W79E658 contains all the SFR present in the standard 8051/52, as well as some additional SFR, and, in some cases, unused bits in the standard 8051/52 have new functions. SFR whose addresses end in 0 or 8 (hex) are bit-addressable. The following table of SFR is condensed, with eight locations per row. Empty locations indicate that there are no registers at these addresses. When a bit or register is not implemented, it reads high.

Table 6-1 Special Function Register Location Table

F8	EIP	I2CON2	I2ADDR20	I2ADDR21	I2DATA2	I2STATUS2	I2CLK2	I2TIMER2
F0	B							
E8	EIE	I2CON	I2ADDR10	I2ADDR11	I2DATA	I2STATUS	I2CLK	I2TIMER
E0	ACC							
D8	WDCON	PWMP	PWM0	PWM1	PWMCON 1	PWM2	PWM3	
D0	PSW							WDCON2
C8	T2CON	T2MOD	RCAP2L	RCAP2H	TL2	TH2	PWMCON2	PWM4
C0	ADDCO N	ADCL	ADCH	PWM5	PMR	STATUS	ADCPS	TA
B8	IP	SADEN						
B0	P3	P5	P6	P7				
A8	IE	SADDR		ROMCON	SFRAL	SFRAH	SFRFD	SFRCN
A0	P2	XRAMAH	P4CSIN			P4		
98	SCON	SBUF	P42AL	P42AH	P43AL	P43AH		CHPCON
90	P1		P4CONA	P4CONB	P40AL	P40AH	P41AL	P41AH
88	TCON	TMOD	TL0	TL1	TH0	TH1	CKCON	
80	P0	SP	DPL	DPH				PCON

1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses. When a bit or register is not implemented, it will read high.

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Table 6-2 Special Function Registers

SYMBOL	DEFINITION	ADDRESS	MSB	BIT_ADDRESS, SYMBOL					LSB	RESET
I2TIMER2	I2C2 Timer Counter Register	FFH	-	-	-	-	-	ENTI2	DIV42	TIF2	0000 0000B
I2CLK2	I2C2 Clock Rate	FEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS2	I2C2 Status Register	FDH						-	-	-	0000 0000B
I2DAT2	I2C2 Data	FCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR21	I2C2 Slave Address1	FBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR20	I2C2 Slave Address0	FAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON2	I2C2 Control Register	F9H	-	ENS2	STA	STO	SI	AA	-	PSEL2	x000 00x0B
EIP	Extended Interrupt Priority	F8H	(FF) -	(FE) -	(FD) -	(FC) PWDI	(FB) -	(FA) -	(F9) PI2C2	(F8) PI2C1	0000 0000B
PCH	PC Counter high register	F2H									00000000B
PCL	PC Counter low register	F1H									00000000B
B	B Register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	0000 0000B
I2TIMER	I2C1 Timer Counter Register	EFH	-	-	-	-	-	ENTI	DIV4	TIF	0000 0000B
I2CLK	I2C1 Clock Rate	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C1 Status Register	EDH						-	-	-	0000 0000B
I2DAT	I2C1 Data	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR11	I2C1 Slave Address1	EBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR10	I2C1 Slave Address0	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON	I2C1 Control Register	E9H	-	ENS1	STA	STO	SI	AA	-	-	x000 00x0B
EIE	Extended Interrupt Enable	E8H	(EF) -	(EE) -	(ED) -	(EC) EWDI	(EB) -	(EA) -	(E9) EI2C2	(E8) EI2C1	0000 0000B
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	0000 0000B
PWM3	PWM3 Output	DEH									0000 0000B
PWM2	PWM2 Output	DDH									0000 0000B
PWMCON1	PWM Control Register1	DCH	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0	0000 0000B
PWM1	PWM1 Output	DBH									0000 0000B
PWM0	PWM0 Output	DAH									0000 0000B
PWMP	PWM Pre-scale Register	D9H									0000 0000B
WDCON	Watch-Dog Control	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0100 0000B
WDCON2	Watch-Dog Control2	D7H	-	-	-	-	-	-	-	STRLD	0000 0000B
PSW	Program Status Word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	0000 0000B

Table 6-3 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, SYMBOL LSB								RESET
PWM4	PWM4 Output	CFH									0000 0000B
PWMCON2	PWM Control Register 2	CEH	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4	0000 0000B
TH2	T2 reg. High	CDH									0000 0000B
TL2	T2 reg. Low	CCH									0000 0000B
RCAP2H	T2 Capture Low	CBH									0000 0000B
RCAP2L	T2 Capture High	CAH									0000 0000B
T2MOD	Timer 2 Mode	C9H	-	-	-	-	T2CR	-	-	DCEN	xxxx 0xx0B
T2CON	Timer 2 Control	C8H	(CF) TF2	(CE) EXF2	(CD) RCLK	(CC) TCLK	(CB) EXEN2	(CA) TR2	(C9) C/T2	(C8) CP/RL2	0000 0000B
TA	Time Access Register	C7H									0000 0000B
ADCPS	ADC Input Pin Switch	C6H	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0	0000 0000B
STATUS	Status Register	C5H	-	HIP	LIP	-	-	-	-	-	x00x xxxxB
PMR	Power Management Register	C4H	-	-	-	-	-	ALEOFF	-	DME0	xxxx x0x0B
PWM5	PWM5 Output	C3H									0000 0000B
ADCH	ADC converter Result High Byte	C2H	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2	xxxx xxxxxB
ADCL	ADC converter Result Low Byte	C1H	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0	00xx xxxxxB
ADCCON	ADC Control Register	C0H	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0	0x000000B
SADEN	Slave Address Mask	B9H									0000 0000B
IP	Interrupt Priority	B8H	(BF) -	(BE) PADC	(BD) PT2	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x000 0000B
P7	Port 7	B3H									1111 1111B
P6	Port 6	B2H									1111 1111B
P5	Port 5	B1H									1111 1111B
P3	Port 3	B0H	(B7) RD	(B6) WR	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	1111 1111B
SFRCN	F/W Flash Control	AFH	BANK	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0	0011 1111B
SFRFD	F/W Flash Data	AEH									xxxx xxxxxB
SFRAH	F/W Flash High Address	ADH									0000 0000B
SFRAL	F/W Flash Low Address	ACH									0000 0000B
ROMCON	ROM Control	ABH	-	-	-	-	EN128K	DCP12	DCP11	DCP10	00000111B
SADDR	Slave Address	A9H									0000 0000B
IE	Interrupt Enable	A8H	(AF) EA	(AE) EADC	(AD) ET2	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	0000 0000B

Table 6-4 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB BIT_ADDRESS, SYMBOL LSB								RESET
P4	Port 4	A5H	-	-	-	-					xxxx 1111B
P4CSIN	P4 CS SIGN	A2H	P43CSINV	P42CSINV	P41CSINV	P40CSINV	-	PWDNH	RMWFP	-	0000 0000B
XRAMAH	RAM High byte Address	A1H	-	-	-	-	-	-	0	0	0000 0000B
P2	Port 2	A0H	(A7) A15	(A6) A14	(A5) A13	(A4) A12	(A3) A11	(A2) A10	(A1) A9	(A0) A8	1111 1111B
CHPCON	On chip Programming Control	9FH	SWRST/REBOOT	-	LD/AP	-	0	0	LDSEL	ENP	0000 0000B
P43AH	HI Addr. Comparator of P4.3	9DH									0000 0000B
P43AL	LO Addr. Comparator of P4.3	9CH									0000 0000B
P42AH	HI Addr. Comparator of P4.2	9BH									0000 0000B
P42AL	LO Addr. Comparator of P4.2	9AH									0000 0000B
SBUF	Serial Buffer	99H									xxxx xxxxxB
SCON	Serial Control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	0000 0000B
P41AH	HI Addr. Comparator of P4.1	97H									0000 0000B
P41AL	LO Addr. Comparator of P4.1	96H									0000 0000B
P40AH	HI Addr. Comparator of P4.0	95H									0000 0000B
P40AL	LO Addr. Comparator of P4.0	94H									0000 0000B
P4CONB	P4 Control Register	93H	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0	0000 0000B
P4CONA	P4 Control Register	92H	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93) TXD_1	(92) RXD_1	(91) T2EX	(90) T2	1111 1111B
CKCON	Clock Control	8EH	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	0000 0001B
TH1	Timer High 1	8DH									0000 0000B
TH0	Timer High 0	8CH									0000 0000B
TL1	Timer Low 1	8BH									0000 0000B
TL0	Timer Low 0	8AH									0000 0000B
TMOD	Timer Mode	89H	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0	0000 0000B
TCON	Timer Control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	0000 0000B
PCON	Power Control	87H	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL	00xx 0000B
DPH	Data Pointer High	83H									0000 0000B
DPL	Data Pointer Low	82H									0000 0000B

Table 6-5 Special Function Registers, continued

SYMBOL	DEFINITION	ADDRESS	MSB			BIT_ADDRESS, SYMBOL				LSB	RESET
SP	Stack Pointer	81H									0000 0111B
P0	Port 0	80H	(87)	(86)	(85)	(84)	(83)	(82)	(81)	(80)	1111 1111B

Note: In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.

PORT 0

Bit:	7	6	5	4	3	2	1	0
	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

Mnemonic: P0 Address: 80h

Port 0 is bi-directional I/O port after chip is reset. Besides, it has internal pull-up resisters. This port also provides a multiplexed, low-order address/data bus when the W79E658 accesses external memory.

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

The Stack Pointer stores the address in Scratchpad RAM where the stack begins. It always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

This is the low byte of the standard-8051/52, 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

This is the low byte of the standard-8051/52, 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial-port baud rate in modes 1, 2 and 3.
6	SMOD0	0: Disable Framing Error Detection. SCON.7 acts as per the standard 8051/52 function. 1: Enable Framing Error Detection. SCON.7 indicates a Frame Error and acts as the FE flag.
5-4	-	Reserved
3	GF1	General-purpose user flag.
2	GF0	General-purpose user flag.
1	PD	1: Go into POWER DOWN mode. In this mode, all clocks and program execution are stopped.
0	IDL	1: Go into IDLE mode. In this mode, the CPU clock stops, so program execution stops too. However, the clock to the serial port, ADC, PWM timer and interrupt blocks does not stop, so these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 overflow flag: This bit is set when Timer 1 overflows. It is cleared automatically when the program executes the Timer-1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 run control: This bit turns the Timer 1 on or off by setting TR1 to 1 or 0.
5	TF0	Timer 0 overflow flag: This bit is set when Timer 0 overflows. It is cleared automatically when the program executes the Timer-0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 run control: This bit turns Timer 0 on or off by setting TR0 to 1 or 0.
3	IE1	Interrupt 1 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT1}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
2	IT1	Interrupt 1 type control: Specify falling-edge or low-level trigger for $\overline{INT1}$.
1	IE0	Interrupt 0 Edge Detect: Set by hardware when an edge / level is detected on $\overline{INT0}$. This bit is cleared by the hardware when the ISR is executed only if the interrupt is edge-triggered. Otherwise, it follows the pin.
0	IT0	Interrupt 0 type control: Specify falling-edge or low-level trigger for $\overline{INT0}$.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	Mode
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer-0 control bits. TH0 is an 8-bit timer only controlled by Timer-1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

TL0.7-0 Timer 0 LSB

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

TL1.7-0 Timer 1 LSB

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

TH0.7-0 Timer 0 MSB

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

TH1.7-0 Timer 1 MSB

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7	WD1	Watchdog Timer mode select bit 1. See table below.
6	WD0	Watchdog Timer mode select bit 0. See table below.
5	T2M	Timer 2 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
4	T1M	Timer 1 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
3	T0M	Timer 0 clock select: 1: divide-by-4 clock 0: divide-by-12 clock
2	MD2	Stretch MOVX select bit 2: MD2, MD1, and MD0 select the stretch value for the MOVX instruction. The $\overline{RD}$ or $\overline{WR}$ strobe is stretched by the selected interval, which enables the W79E658 to access faster or slower external memory devices or peripherals without the need for external circuits. By default, the stretch value is one. See table below. (Note: When accessing on-chip SRAM, these bits have no effect, and the MOVX instruction always takes two machine cycles.)
1	MD1	Stretch MOVX select bit 1. See MD2.
0	MD0	Stretch MOVX select bit 0. See MD2.

WD1, WD0: Mode Select bits:

These bits determine the time-out periods for the Watchdog Timer. The reset time-out period is 512 clocks more than the interrupt time-out period.

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT
0	0	2^{17}	2^{17} + 512
0	1	2^{20}	2^{20} + 512
1	0	2^{23}	2^{23} + 512
1	1	2^{26}	2^{26} + 512

MD2, MD1, MD0: Stretch MOVX select bits:

MD2	MD1	MD0	STRETCH VALUE	MOVX DURATION
0	0	0	0	2 machine cycles
0	0	1	1	3 machine cycles *(Default)*
0	1	0	2	4 machine cycles
0	1	1	3	5 machine cycles
1	0	0	4	6 machine cycles
1	0	1	5	7 machine cycles
1	1	0	6	8 machine cycles
1	1	1	7	9 machine cycles

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General-purpose digital input port or analog input port AD0~AD7. For digital input, port-read instructions read the port pins, while read-modify-write instructions read the port latch. Additional functions are described below.

	ALTERNATE FUNCTION1	ALTERNATE FUNCTION2	ALTERNATE FUNCTION3
P1.0	T2: External input for Timer/Counter 2	PWM0: PWM output ch0	-
P1.1	T2EX: Timer/Counter 2 Capture/Reload Trigger	PWM1: PWM output ch1	-
P1.2	STADC: External rising edge input to start ADC	PWM2: PWM output ch2	-
P1.3	-	PWM3: PWM output ch3	-
P1.4	-	PWM4: PWM output ch4	ADC0: Analog input0
P1.5	-	PWM5: PWM output ch5	ADC1: Analog input1
P1.6	-	-	ADC2: Analog input2
P1.7	-	-	ADC3: Analog input3

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1, P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P4.0 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P40AL Address: 94h

P4.0 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P40AH Address: 95h

P4.1 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P41AL Address: 96h

P4.1 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P41AH Address: 97h

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial Port mode select bit 0 or Framing Error Flag: This bit is controlled by the SMOD0 bit in the PCON register. (SM0) See table below. (FE) This bit indicates an invalid stop bit. It must be manually cleared by software.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Serial Port Clock or Multi-Processor Communication. (Mode 0) This bit controls the serial port clock. If set to zero, the serial port runs at a divide-by-12 clock of the oscillator. This is compatible with the standard 8051/52. If set to one, the serial clock is a divide-by-4 clock of the oscillator. (Mode 1) If SM2 is set to one, RI is not activated if a valid stop bit is not received. (Modes 2 / 3) This bit enables multi-processor communication. If SM2 is set to one, RI is not activated if RB8, the ninth data bit, is zero.
4	REN	Receive enable: 1: Enable serial reception 0: Disable serial reception
3	TB8	(Modes 2 / 3) This is the 9th bit to transmit. This bit is set by software.
2	RB8	(Mode 0) No function. (Mode 1) If SM2 = 0, RB8 is the stop bit that was received. (Modes 2 / 3) This is the 9th bit that was received.
1	TI	Transmit interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or at the beginning of the stop bit in the other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by the hardware at the end of the 8th bit in mode 0 or halfway through the stop bits in the other modes during serial reception. However, SM2 can restrict this behavior. This bit can only be cleared by software.

SM0, SM1: Mode Select bits:

SM0	SM1	MODE	DESCRIPTION	LENGTH	BAUD RATE
0	0	0	Synchronous	8	Tclk divided by 4 or 12
0	1	1	Asynchronous	10	Variable
1	0	2	Asynchronous	11	Tclk divided by 32 or 64
1	1	3	Asynchronous	11	Variable

Serial Data Buffer

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

SBUF.7-0 Serial data is read from or written to this location. It actually consists of two separate 8-bit registers. One is the receive buffer, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

P4.2 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P42AL Address: 9Ah

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P42AH Address: 9Bh

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: P43AL Address: 9Ch

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: P43AH Address: 9Dh

ISP Control Register

Bit:	7	6	5	4	3	2	1	0
	SWRST /HWB	-	LD/AP	-	-	-	LDSEL	ENP

Mnemonic: CHPCON Address: 9Fh

BIT	NAME	FUNCTION
7	W:SWRST R:HWB	Write access to this bit is different from read access. Set this bit to reset the device. This has the same effect as asserting the RST pin. The microcontroller returns to its initial state, and this bit is cleared automatically. Reading this bit indicates whether or not the device is in ISP hardware reboot mode.
6	-	Reserved
5	LD/AP (read-only)	0: CPU is executing AR Flash EPROM 1: CPU is executing LD Flash EPROM
4-2	-	Reserved
1	LDSEL (write-only)	Load ROM Location Selection. This bit should be set before entering ISP mode. 1: Run the program in LD Flash EPROM. 0: Run the program in AP Flash EPROM.

Continued

BIT	NAME	FUNCTION
0	ENP	In System Program Enable. 1: Enable in-system programming mode. The erase, program and read operations are executed according to various SFR settings. In this mode, the device runs in IDLE state, so PCON.1 has no effect. 0: Disable in-system programming mode. The device returns to normal operations, and PCON.1 is functional again.

The way to enter ISP mode is to set ENP to 1 and write LDSEL properly then force CPU in IDLE mode, after IDLE mode is released CPU will restart from AP or LD ROM according the value of LDSEL.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

Mnemonic: P2 Address: A0h

P2.7-0: Port 2 is a bi-directional I/O port with internal pull-up resistors. This port also provides the upper address bits for accesses to external memory.

Port 4 Chip-select Polarity

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	PWDNH	RMWFP	PUP0

Mnemonic: P4CSIN Address: A2h

BIT	NAME	FUNCTION
7-4	P4xINV	The Active Polarity of P4.x as P4.x is set as a chip-select strobe output. 1: Active High. 0: Active Low.
3	-	Reserved
2	PWDNH	Set ALE and $\overline{\text{PSEN}}$ state in power down mode. 1: ALE and $\overline{\text{PSEN}}$ output logic high in power down mode 0: ALE and $\overline{\text{PSEN}}$ output logic low in power down mode.
1	RMWFP	Control Read Path of Instruction “Read-Modify-Write”. When this bit is set, the read path of executing “read-modify-write” instruction is from port pin otherwise from SFR.
0	-	Reserved

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0: Port 4 is a bi-directional I/O port with internal pull-ups.

Interrupt Enable

Bit:	7	6	5	4	3	2	1	0
	EA	EADC	ET2	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/disable all interrupts.
6	EADC	Enable ADC interrupt.
5	ET2	Enable Timer 2 interrupt.
4	ES	Enable Serial Port interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

Slave Address

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

SADDR The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

ROM Banking Control

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	EN128K	DCP12	DCP11	DCP10

Mnemonic: ROMCON Address: ABh

BIT	NAME	FUNCTION
7-4	-	Reserved
3	EN128K	**On-chip ROM banking enable.** Set this bit to enable APFlash0 and APFlash1 by banking mechanism. The P1.x is selected to be the auxiliary highest address line A16.
2-0	DCP1[2:0]	A16 selection. By banking mechanism, address 16 (A16) indicates where the CPU fetches code from AP0(A16=0) or AP1(AP16=1). By default, P1.7 is defined as A16. See table below

ISP Address Low Byte

Bit:	7	6	5	4	3	2	1	0
	A7	A6	A5	A4	A3	A2	A1	A0

Mnemonic: SFRAL Address: ACh

Low byte destination address for In System Programming operations.

ISP Address High Byte

Bit:	7	6	5	4	3	2	1	0
	A15	A14	A13	A12	A11	A10	A9	A8

Mnemonic: SFRAH Address: ADh

Low byte destination address for In System Programming operations. (SFRAH, SFRAL) represents the address of the ROM byte that will be erased, programmed or read.

ISP Data Buffer

Bit:	7	6	5	4	3	2	1	0
	D7	D6	D5	D4	D3	D2	D1	D0

Mnemonic: SFRFD Address: AEh

In ISP mode, read/write a specific byte ROM content must go through SFRFD register.

ISP Operation Modes

Bit:	7	6	5	4	3	2	1	0
	BANK	WFWIN	NOE	NCE	CTRL3	CTRL2	CTRL1	CTRL0

Mnemonic: SFRCN Address: AFh

BANK Select APFlash banks for ISP. Set it 1 to access APFlash1, clear it for access to APFlash0.

WFWIN On-chip FLASH EPROM bank select for in-system programming.
0= AP FLASH EPROM bank is selected as destination for re-programming.
1= LD FLASH EPROM bank is selected as destination for re-programming.

NOE Flash EPROM output enable.

NCE Flash EPROM chip enable.

CTRL[3:0] The Flash Control Signals.

ISP MODE	BANK	WFWIN	NOE	NCE	CTRL[3:0]	SFRAH, SFRAL	SFRFD
Erase 4KB LDFlash	0	1	1	0	0010	X	X
Erase 64K APFlash0	0	0	1	0	0010	X	X
Erase 64K APFlash1	1	0	1	0	0010	X	X
Program 4KB LDFlash	0	1	1	0	0001	Address in	Data in
Program 64KB APFlash0	0	0	1	0	0001	Address in	Data in
Program 64KB APFlash1	1	0	1	0	0001	Address in	Data in
Read 4KB LDFlash	0	1	0	0	0000	Address in	Data out
Read 64KB APFlash0	0	0	0	0	0000	Address in	Data out
Read 64KB APFlash1	1	0	0	0	0000	Address in	Data out

PORT 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General-purpose I/O port. Each pin also has an alternative input or output function, which is described below.

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$: strobe for reading from external RAM
6	P3.6	$\overline{WR}$: strobe for writing to external RAM
5	P3.5	T1: Timer 1 external count input
4	P3.4	T0: Timer 0 external count input
3	P3.3	$\overline{INT1}$: External interrupt 1
2	P3.2	$\overline{INT0}$: External interrupt 0
1	P3.1	TxD: Serial port 0 output
0	P3.0	RxD: Serial port 0 input

PORT 5

Bit:	7	6	5	4	3	2	1	0
	P5.7	P5.6	P5.5	P5.4	P5.3	P5.2	P5.1	P5.0

Mnemonic: P5 Address: B1h

P5.7-0 A bi-directional I/O port with inernal pull-ups. This port is not bit-addressable. The alternate functions of P5.0 to P5.3 are inputs of ADC4 to ADC7.

PORT 6

Bit:	7	6	5	4	3	2	1	0
	P6.7	P6.6	P6.5	P6.4	P6.3	P6.2	P6.1	P6.0

Mnemonic: P6 Address: B2h

P6.7-0 A bi-directional I/O port with inernal pull-ups. This port is not bit-addressable. Pins P6.4 to P6.7 are open drain type and can be software configured as the I2C ports.

PORT 7

Bit:	7	6	5	4	3	2	1	0
	P7.7	P7.6	P7.5	P7.4	P7.3	P7.2	P7.1	P7.0

Mnemonic: P7 Address: B3h

P7.7-0 A bi-directional I/O port with inernal pull-ups. This port is not bit-addressable.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	PADC	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
7	-	Reserved. This bit reads high.
6	PADC	1: Set the priority of the ADC interrupt to the highest level.
5	PT2	1: Set the priority of the Timer 2 interrupt to the highest level.
4	PS	1: Set the priority of the Serial Port interrupt to the highest level.
3	PT1	1: Set the priority of the Timer 1 interrupt to the highest level.
2	PX1	1: Set the priority of external interrupt 1 to the highest level.
1	PT0	1: Set the priority of the Timer 0 interrupt to the highest level.
0	PX0	1: Set the priority of external interrupt 0 to the highest level.

Slave Address Mask Enable

Bit:	7	6	5	4	3	2	1	0
	SADEN.7	SADEN.6	SADEN.5	SADEN.4	SADEN.3	SADEN.2	SADEN.1	SADEN.0

Mnemonic: SADEN Address: B9h

SADEN[7:0] This register enables the Automatic Address Recognition feature for the serial port. When a bit in SADEN is set to 1, the same bit in SADDR is compared to incoming serial data. When a bit in SADEN is set to 0, the same bit becomes a "don't care" condition in the comparison. Disable Automatic Address Recognition by setting all the bits in SADEN to 0.

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: C0h

BIT	NAME	FUNCTION
7	ADCEN	Enable A/D Converter Function. 1: Enable ADC block.
6	-	Reserved
5	ADCEX	Enable STADC-triggered conversion 0: Conversion can only be started by software (i.e., by setting ADCS). 1: Conversion can be started by software or by a rising edge on STADC (pin P1.2).
4	ADCI	ADC Interrupt flag. This flag is set when the result of an A/D conversion is ready. This generates an ADC interrupt, if it is enabled. The flag must be cleared by the software. While this flag is 1, the ADC cannot start a new conversion. ADCI can not be set by software.

Continued

<table>
<tr><th>BIT</th><th>NAME</th><th>FUNCTION</th></tr>
<tr><td>3</td><td>ADCS</td><td>ADC Start and Status: Set this bit to start an A/D conversion. It may also be set by STADC if ADCEX is 1. This signal remains high while the ADC is busy and is reset right after ADCI is set. ADCS can not be reset by software, and the ADC cannot start a new conversion while ADCS is high.
<table>
<tr><th>ADCI</th><th>ADCS</th><th>ADC Status</th></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>ADC not busy; a conversion can be started
ADC busy; start of a new conversion is blocked
Conversion completed; start of a new conversion requires ADCI=0
Conversion completed; start of a new conversion requires ADCI=0</td></tr>
</table>
It is recommended to clear ADCI before ADCS is set. However, if ADCI is cleared and ADCS is set at the same time, a new A/D conversion may start on the same channel.</td></tr>
<tr><td>2</td><td>AADR2</td><td>See table below.</td></tr>
<tr><td>1</td><td>AADR1</td><td>See table below.</td></tr>
<tr><td>0</td><td>AADR0</td><td>See table below.</td></tr>
</table>

AADR2, AADR1, AADR0: ADC Analog Input Channel select bits:

These bits can only be changed when ADCI and ADCS are both zero.

AADR[2:0]	ADC selected input	AADR[2:0]	ADC selected input
000	ADCCH0 (P1.4)	100	ADCCH4 (P5.0)
001	ADCCH1 (P1.5)	101	ADCCH5 (P5.1)
010	ADCCH2 (P1.6)	110	ADCCH6 (P5.2)
011	ADCCH3 (P1.7)	111	ADCCH7 (P5.3)

ADC Converter Result Low Register

Bit:	7	6	5	4	3	2	1	0
	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0

Mnemonic: ADCL Address: C1h

ADCLK[1:0] ADC Clock Frequency Select. The 10-bit ADC needs a clock which frequency can not be over 4MHz to drive the converting. ADCLK[1:0] select the frequency of the clock to ADC block as below table.

ADCLK1	ADCLK0	ADC CLOCK FREQUENCY
0	0	Crystal clock / 4 (Default)
0	1	Crystal clock / 8
1	0	Crystal clock / 16
1	1	Reserved

ADC[1:0] 2 LSB of 10-bit A/D conversion result. These 2 bits are read only.

ADC Converter Result High Register

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: C2h

ADC[9:2] 8 MSB of 10-bit A/D conversion result. Register ADCH is read only.

PWM5 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM5 Address: C3H

POWER Management Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ALEOFF	-	DME0

Mnemonic: PMR Address: C4h

BIT	NAME	FUNCTION
7~3	-	Reserved.
2	ALEOFF	0: ALE expression is enabled during on-board program and data accesses. 1: ALE expression is disabled. Keep the logic in the high state. External memory accesses automatically enable ALE, regardless of ALEOFF.
1	-	Reserved.
0	DME0	On-chip MOVX SRAM enable bit. 1: Enable on-chip 1KB MOVX SRAM

STATUS Register

Bit:	7	6	5	4	3	2	1	0
	-	HIP	LIP	-	-	-	-	-

Mnemonic: STATUS Address: C5h

BIT	NAME	FUNCTION
7	-	Reserved.
6	HIP	High-Priority Interrupt Status. When set, it indicates that the software is servicing a high-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
5	LIP	Low-Priority Interrupt Status. When set, it indicates that the software is servicing a low-priority interrupt. This bit is cleared when the program executes the corresponding RETI instruction.
4-0	-	Reserved.

ADC Pin Switch

Bit:	7	6	5	4	3	2	1	0
	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0

Mnemonic: ADCPS Address: C6h

BIT	NAME	FUNCTION
7-0	ADCPS.7-0	Switch the mode of I/O pins, P1.7~P1.4 and P5.0~p5.3, to analog input mode. Analog inputs, ADC0-ADC3 which share the I/O pins from P1.4 to P1.7 and ADC4-ADC7 which share the I/O pins from P5.0 to P5.3. 1: The corresponding I/O pin functions as analog input. 0: The corresponding I/O pin functions as digital I/O.

ADCPS.3-0: Switch P1.7~P1.4 to analog input function

BIT	CORRESPONDING PIN	BIT	CORRESPONDING PIN
ADCPS.0	P1.4	ADCPS.4	P5.0
ADCPS.1	P1.5	ADCPS.5	P5.1
ADCPS.2	P1.6	ADCPS.6	P5.2
ADCPS.3	P1.7	ADCPS.7	P5.3

Timed Access

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

TA This register controls the access to protected bits. To access protected bits, the program must write AAH, followed immediately by 55H, to TA. This opens a window for three machine cycles, during which the program can write to protected bits.

TIMER 2 CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF2	EXF2	RCLK	TCLK	EXEN2	TR2	$C/\overline{T2}$	$CP/\overline{RL2}$

Mnemonic: T2CON Address: C8h

BIT	NAME	FUNCTION
7	TF2	Timer 2 Overflow flag: This bit is set when Timer 2 overflows. It is also set when the count is equal to the capture register in down-count mode. It can be set by the hardware only if RCLK and TCLK are both 0, and it can be set or cleared by software.
6	EXF2	Timer 2 External flag: A negative transition on the T2EX pin (P1.1) or a timer 2 underflow / overflow sets this flag according to the CP/RL2, EXEN2 and DCEN bits. This bit can also be set by the software. If set by a negative transition, this flag must be cleared by software. If set by a negative transition or by software, a Timer 2 interrupt is generated, if enabled.

Continued

BIT	NAME	FUNCTION
5	RCLK	Receive Clock flag: This bit determines the serial-port time base when receiving data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
4	TCLK	Transmit Clock flag: This bit determines the serial-port time base when transmitting data in Serial Port modes 1 or 3. 0: The Timer 1 overflow is used for baud-rate generation 1: The Timer 2 overflow is used for baud-rate generation, forcing Timer 2 into baud-rate generator mode.
3	EXEN2	Timer 2 External Enable: This bit enables the capture / reload function on the T2EX pin, as long as Timer 2 is not generating baud clocks for the serial port. 0: Ignore T2EX. 1: Negative transitions on T2EX result in capture or reload.
2	TR2	Timer 2 Run Control: This bit enables / disables Timer 2. When disabled, Timer 2 preserves the current values in TH2 and TL2.
1	$\overline{C/T2}$	Counter / Timer select: 0: Timer 2 operates as a timer at a speed depending on T2M bit (CKCON.5) 1: Timer 2 counts negative edges on the T2EX pin. Regardless of this bit, Timer 2 may be forced into baud-rate generator mode.
0	$\overline{CP/RL2}$	Capture / Reload select, when Timer 2 overflows or when a falling edge is detected on T2EX (and EXEN2 = 1). 0: Auto-reload Timer 2 1: Capture in Timer 2 If RCLK or TCLK is set, this bit does not function, and Timer 2 runs in auto-reload mode following each overflow.

TIMER 2 MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	T2CR	-	-	DCEN

Mnemonic: T2MOD Address: C9h

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	T2CR	Timer 2 Capture Reset. In Timer-2 Capture Mode, 1: Enable the function that automatically reset Timer 2 once the Timer 2 capture registers have captured the values in Timer 2.
2~1	-	Reserved.
0	DCEN	Down Count Enable: This bit controls the direction that Timer 2 counts in 16-bit auto-reload mode.

TIMER 2 CAPTURE LSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2L.7	RCAP2L.6	RCAP2L.5	RCAP2L.4	RCAP2L.3	RCAP2L.2	RCAP2L.1	RCAP2L.0

Mnemonic: RCAP2L Address: CAh

RCAP2L (Capture mode) This register captures the LSB of Timer 2 (TL2). (Auto-reload mode) This register is the LSB of the 16-bit reload value.

TIMER 2 CAPTURE MSB

Bit:	7	6	5	4	3	2	1	0
	RCAP2H.7	RCAP2H.6	RCAP2H.5	RCAP2H.4	RCAP2H.3	RCAP2H.2	RCAP2H.1	RCAP2H.0

Mnemonic: RCAP2H Address: CBh

RCAP2H (Capture mode) This register captures the MSB of Timer 2 (TH2). (Auto-reload mode) This register is the MSB of the 16-bit reload value.

TIMER 2 LSB

Bit:	7	6	5	4	3	2	1	0
	TL2.7	TL2.6	TL2.5	TL2.4	TL2.3	TL2.2	TL2.1	TL2.0

Mnemonic: TL2 Address: CCh

TL2 Timer 2 LSB

TIMER 2 MSB

Bit:	7	6	5	4	3	2	1	0
	TH2.7	TH2.6	TH2.5	TH2.4	TH2.3	TH2.2	TH2.1	TH2.0

Mnemonic: TH2 Address: CDh

TH2 Timer 2 MSB

PWM Control Register2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	PWM5OE	PWM4OE	ENPWM5	ENPWM4

Mnemonic: PWMCON2 Address: CEh

BIT	NAME	FUNCTION
7~4	-	Reserved.
3	PWM5OE	Output enable for PWM5 0: Disable PWM5 Output. 1: Enable PWM5 Output.
2	PWM4OE	Output enable for PWM4 0: Disable PWM4 Output. 1: Enable PWM4 Output.
1	ENPWM5	Enable PWM5 0: Disable PWM5. 1: Enable PWM5.
0	ENPWM4	Enable PWM4 0: Disable PWM4. 1: Enable PWM4.

PWM4 Register

Bit:	7	6	5	4	3	2	1	0

Mnemonic: PWM4 Address: CFH

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set when an arithmetic operation results in a carry being generated from the ALU. It is also used as the accumulator for bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high-order nibble.
5	F0	User flag 0: A general-purpose flag that can be set or cleared by the user.
4	RS1	Register Bank select bits. See table below.
3	RS0	Register Bank select bits. See table below.
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the eighth bit, or vice versa, as a result of the previous operation.
1	F1	User flag 1: A general-purpose flag that can be set or cleared by the user.
0	P	Parity flag: Set and cleared by the hardware to indicate an odd or even number of 1's in the accumulator.

RS1, RS0: Register Bank select bits:

RS1	RS0	REGISTER BANK	ADDRESS
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

WATCHDOG CONTROL 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	STRLD

Mnemonic: WDCON2 Address: D7h

STRLD Set this bit, CPU will re-start from LD Flash EPROM after watchdog reset. Clear this bit, CPU will re-start from AP Flash EPROM after watchdog reset. This register is protected by timer access (TA) register.

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	POR	-	-	WDIF	WTRF	EWT	RWT

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

The WDCON register is affected differently by different kinds of resets. After an external reset, the WDCON register is set to 0x0x0xx0b. After a Watchdog Timer reset, WTRF is set to 1, and the other bits are unaffected. On a power-on/-down reset, WTRF and EWT are set to 0, and POR is set to 1.

All the bits in this SFR have unrestricted read access. POR, EWT, WDIF and RWT are protected bits, so programs must follow the Timed Access procedure to write them. (See the TA Register description for more information.) This is illustrated in the following example.

```
TA      EG   C7H
WDCON   REG  D8H
CKCON   REG  8EH
             MOV   TA, #AAH
             MOV   TA, #55H
             SETB  WDCON.0              ; Reset Watchdog Timer
             ORL   CKCON, #11000000B    ; Select 26 bits Watchdog Timer
             MOV   TA, #AAH
             MOV   TA, #55H
             ORL   WDCON, #00000010B    ; Enable watchdog
```

The other bits in WDCON have unrestricted write access.

PWM Pre-scale Register

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWMP Address: D9h

PWMP.7-0 Adjust PWM frequency. $Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$

PWM0

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM0 Address: DAh

PWM0.7-0 Adjust PWM0 duty cycle. PWMn high/low ratio of PWMn $= \frac{PWMn}{255 - (PWMn)}$

PWM1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM1 Address: DBh

PWM1.7-0 Adjust PWM1 duty cycle.

PWM Control Register1

Bit:	7	6	5	4	3	2	1	0
	PWM3OE	PWM2OE	ENPWM3	ENPWM2	PWM1OE	PWM0OE	ENPWM1	ENPWM0

Mnemonic: PWMCON1 Address: DCh

BIT	NAME	FUNCTION
7	PWM3OE	Output enable for PWM3 0: Disable PWM3 Output. 1: Enable PWM3 Output.
6	PWM2OE	Output enable for PWM2 0: Disable PWM2 Output. 1: Enable PWM2 Output.
5	ENPWM3	Enable PWM3 0: Disable PWM3. 1: Enable PWM3.
4	ENPWM2	Enable PWM2 0: Disable PWM2. 1: Enable PWM2.

Continued

BIT	NAME	FUNCTION
3	PWM1OE	Output enable for PWM1 0: Disable PWM1 Output. 1: Enable PWM1 Output.
2	PWM0OE	Output enable for PWM0 0: Disable PWM0 Output. 1: Enable PWM0 Output.
1	ENPWM1	Enable PWM1 0: Disable PWM1. 1: Enable PWM1.
0	ENPWM0	Enable PWM0 0: Disable PWM0. 1: Enable PWM0.

PWM2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM2 Address: DDh

PWM2.7-0 Adjust PWM2 duty cycle.

PWM3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: PWM3 Address: DEh

PWM3.7-0 Adjust PWM3 duty cycle.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

ACC.7-0 The A (or ACC) register is the standard 8051/52 accumulator.

EXTENDED INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	EWDI	-	-	EI2C2	EI2C1

Mnemonic: EIE Address: E8h

EWDI Enable Watchdog timer interrupt

EI2C2 Enable I2C channel 2 interrupt

EI2C1 Enable I2C channel 1 interrupt

I2C Control Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	PSEL1

Mnemonic: I2CON Address: E9h

ENS1 Enable channel 1 of I2C serial function block. When ENS1=1 the channel 1 of I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware checks the bus condition, if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined "not addressed" slave mode.

SI I2C Port 1 Interrupt Flag. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C1 bits are both set, the I2C1 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

PSEL1 I2C Port1 Select bit. I2C port1 pair of SCL1 and SDA1, can be configured to pair of P2.4 and P2.5 if PSEL1=0 or to pair of P6.4 and P6.5 if PSEL1=1. The default value of bit PSEL1 is logic 0. Note that pin from P6.4 to P6.7 are open drain type.

I2C Channel 1 Address Register 0

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR10 Address: EAh

I2ADDR10.7-1 I2C1 Slave Address0. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR10 are matched with the received slave address.

GC Enable General Call Function. The GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

I2C Channel 1 Address Register 1

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	-

Mnemonic: I2ADDR11 Address: EBh

I2ADDR11.7-1 I2C1 Slave Address1. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR11 are matched with the received slave address.

Bit0 Reserved

I2C Data Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT Address: ECh

I2DAT.7-0 The data register of I2C channel 1.

I2C Status Register Channel 1

Bit:	7	6	5	4	3	2	1	0
						0	0	0

Mnemonic: I2STATUS Address: EDh

I2STATUS.7-0 The Status Register of I2C Channel 1(I2C1). The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, the I2C1 interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C Baud Rate Control Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK Address: EEh

I2CLK.7-0 The I2C clock rate control

I2C Timer Counter Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI	DIV4	TIF

Mnemonic: I2TIMER Address: EFh

ENTI Enable I2C 14-bits Time-out Counter. Setting ENTI to logic high will firstly reset the time-out counter and then start up counting. Clearing ENTI disables the 14-bit time-out counter. ENTI can be set to logic high only when SI=0.

DIV4 I2C Time-out Counter Clock Frequency Selection. DIV4 = 0 the clock frequency is coherent to the system clock Fosc. DIV4 = 1 the clock frequency is Fosc/4.

TIF I2C Time-out Flag. When the time-out counter overflows hardware will set this flag and request the I2C1 interrupt if I2C1 interrupt is enabled (EI2C1=1). This bit must be cleared by software.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

B.7-0 The B register is the standard 8051/52 register that serves as a second accumulator

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWDI	-	-	PI2C2	PI2C1

Mnemonic: EIP Address: F8h

PWDI Watchdog Timer Interrupt priority.

PI2C2 I2C Channel 2 Interrupt priority.

PI2C1 I2C Channel 1 Interrupt priority.

I2C Control Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	-	ENS2	STA	STO	SI	AA	-	PSEL2

Mnemonic: I2CON2 Address: F9h

ENS2 Enable channel 2 of I2C serial function block. When ENS2=1 the channel 2 of I2C serial function enables. The port latches of SDA2 and SCL2 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware will check the bus condition if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode.

SI I2C Port 2 Interrupt Flag. When a new SIO2 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C2 bits are both set, the I2C2 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

PSEL2 I2C Port2 Select bit. I2C port2 pair of SCL2 and SDA2, can be configured to pair of P2.6 and P2.7 if PSEL2=0 or to pair of P6.6 and P6.7 if PSEL2=1. The default value of bit PSEL2 is logic 0. Note that the pins from P6.4 to P6.7 are in open drain type.

I2C Channel 2 Address Register 0

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	GC

Mnemonic: I2ADDR20 Address: FAh

I2ADDR20.7-1 I2C2 Slave Address. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU’s own slave address. The I2C hardware will react if the contents of I2ADDR20 are matched with the received slave address.

GC Enable General Call Function. The GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

I2C Channel 2 Address Register 1

Bit:	7	6	5	4	3	2	1	0
	I2ADDR.7	I2ADDR.6	I2ADDR.5	I2ADDR.4	I2ADDR.3	I2ADDR.2	I2ADDR.1	-

Mnemonic: I2ADDR21 Address: FBh

I2ADDR21.7-1 I2C2 Slave Address. The 8051 uC can read from and write to this 8-bit, directly addressable SFR. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDR21 are matched with the received slave address.

Bit0 Reserved

I2C Data Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0

Mnemonic: I2DAT2 Address: FCh

I2DAT2.7-0 The data register of I2C Channel 2.

I2C Status Register Channel 2

Bit:	7	6	5	4	3	2	1	0
						0	0	0

Mnemonic: I2STATUS2 Address: FDh

I2STATUS2.7-0 The Status Register of I2C Channel 2(I2C2). The three least significant bits are always 0. The five most significant bits contain the status code. There are 23 possible status codes. When I2STATUS contains F8H, no serial interrupt is requested. All other I2STATUS values correspond to defined I2C states. When each of these states is entered, the I2C2 interrupt is requested (SI = 1). A valid status code is present in I2STATUS one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software. In addition, states 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the formation frame. Example of illegal position are during the serial transfer of an address byte, a data byte or an acknowledge bit.

I2C Baud Rate Control Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0

Mnemonic: I2CLK2 Address: FEh

I2CLK2.7-0 The I2C clock rate control

I2C Timer Counter Register Channel 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	ENTI2	DIV42	TIF2

Mnemonic: I2TIMER2 Address: FFh

ENTI2 Enable I2C 14-bits Time-out Counter. Setting ENTI to logic high will firstly reset the time-out counter and then start up counting. Clearing ENTI disables the 14-bit time-out counter. ENTI can be set to logic high only when SI=0.

DIV42 I2C Time-out Counter Clock Frequency Selection. DIV42= 0 the clock frequency is coherent to the system clock Fosc. DIV42 = 1 the clock frequency is Fosc/4.

TIF2 I2C Time-out Flag. When the time-out counter overflows hardware will set this flag and request the I2C2 interrupt if I2C2 interrupt is enabled (EI2C1=1). This bit must be cleared by software.

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7. Instruction Set

The W79E658 executes all the instructions of the standard 8051/52 family. The operations of these instructions, as well as their effect on flag and status bits, are exactly the same. However, the timing of these instructions is different in two ways. First, the W79E658 machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Second, the W79E658 can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can twice per machine cycle (i.e., six clocks per fetch).

The timing difference creates an advantage for the W79E658. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E658 reduces the number of dummy fetches and wasted cycles and improves overall efficiency, compared to the standard 8051/52.

Table 7-1 Instruction Set for W79E658

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3
ADDC A, @R1	37	1	1	4	12	3

Instruction Set for W79E658, continued

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5

OP-CODE	HEX CODE	BYTES	W79E658 MACHINE CYCLE	W79E658 CLOCK CYCLES	8032 CLOCK CYCLES	W79E658 VS. 8032 SPEED RATIO
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

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7.1 Instruction Timing

This section is important because some applications use software instructions to generate timing delays. It also provides more information about timing differences between the W79E658 and the standard 8051/52.

In the W79E658, each machine cycle is four clock periods long. Each clock period is called a state, and each machine cycle consists of four states: C1, C2 C3 and C4, in order. Both clock edges are used for internal timing, so the duty cycle of the clock should be as close to 50% as possible.

The W79E658 does one op-code fetch per machine cycle, so, in most instructions, the number of machine cycles required is equal to the number of bytes in the instruction. There are 256 available op-codes. 128 of them are single-cycle instructions, so many op-codes are executed in just four clock periods. Some of the other op-codes are two-cycle instructions, and most of these have two-byte op-codes. However, there are some instructions that have one-byte instructions yet take two cycles to execute. One important example is the MOVX instruction.

In the standard 8051/52, the MOVX instruction is always two machine cycles long. However, in the W79E658, the duration of this instruction is controlled by the software. It can vary from two to nine machine cycles long, and the $\overline{RD}$ and $\overline{WR}$ strobe lines are elongated proportionally. This is called stretching, and it gives a lot of flexibility when accessing fast and slow peripherals. It also reduces the amount of external circuitry and software overhead.

The rest of the instructions are three-, four- or five-cycle instructions. At the end of this section, there are timing diagrams that provide an example of each type of instruction (single-cycle, two-cycle, …).

In summary, there are five types of instructions in the W79E658, based on the number of machine cycles, and each machine cycle is four clock periods long. The standard 8051/52 has only three types of instructions, based on the number of machine cycles, but each machine cycle is twelve clock periods long. As a result, even though the number of categories is higher, each instruction in the W79E658 runs 1.5 to 3 times faster, based on the number of clock periods, than it does in the standard 8051/52.

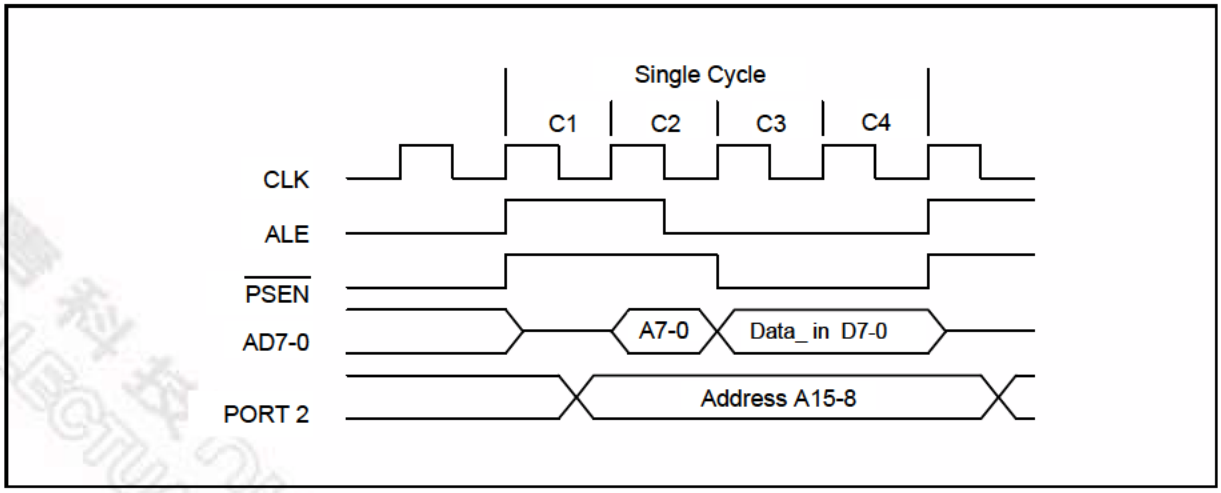


Figure 7-1 Single Cycle Instruction Timing

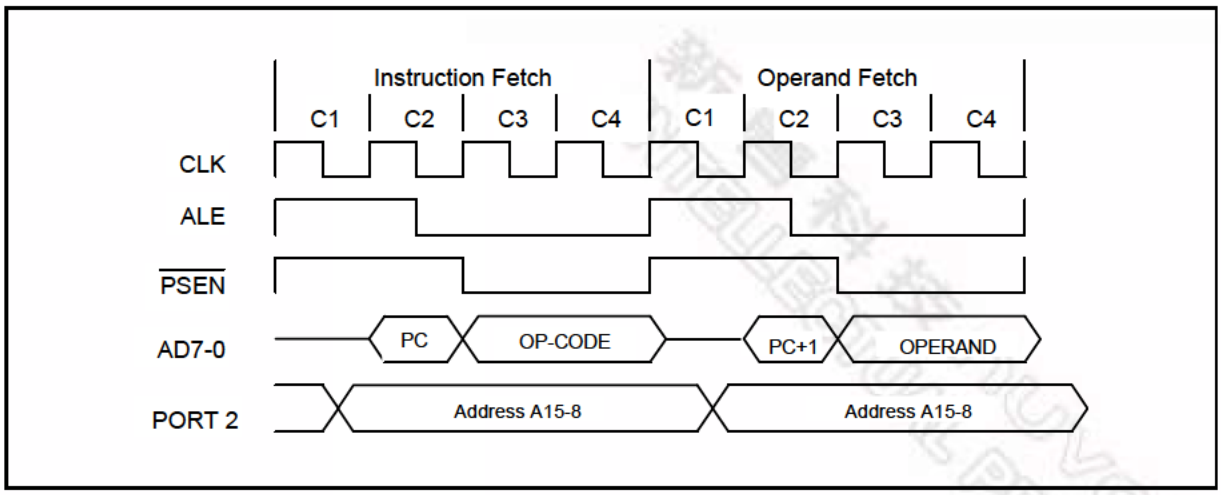


Figure 7-2 Two Cycle Instruction Timing

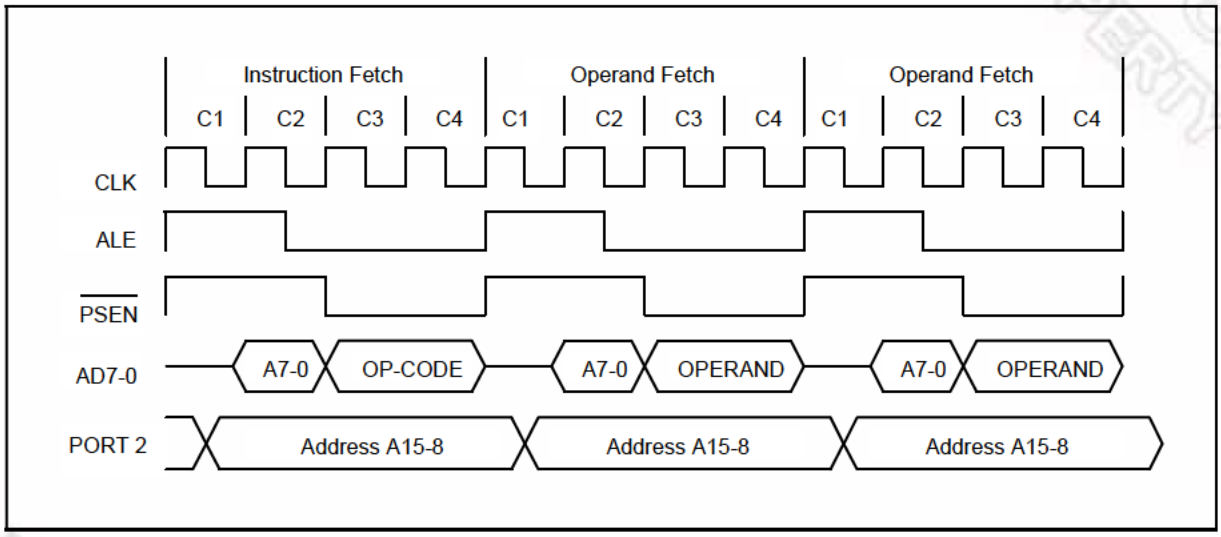


Figure 7-3 Three Cycle Instruction Timing

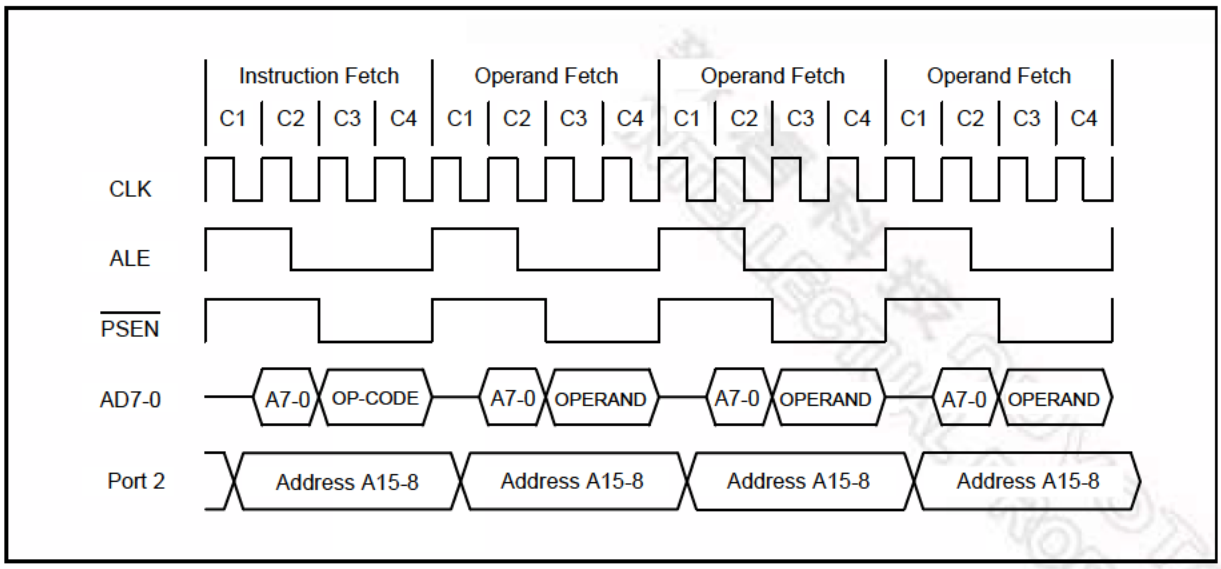


Figure 7-4 Four Cycle Instruction Timing

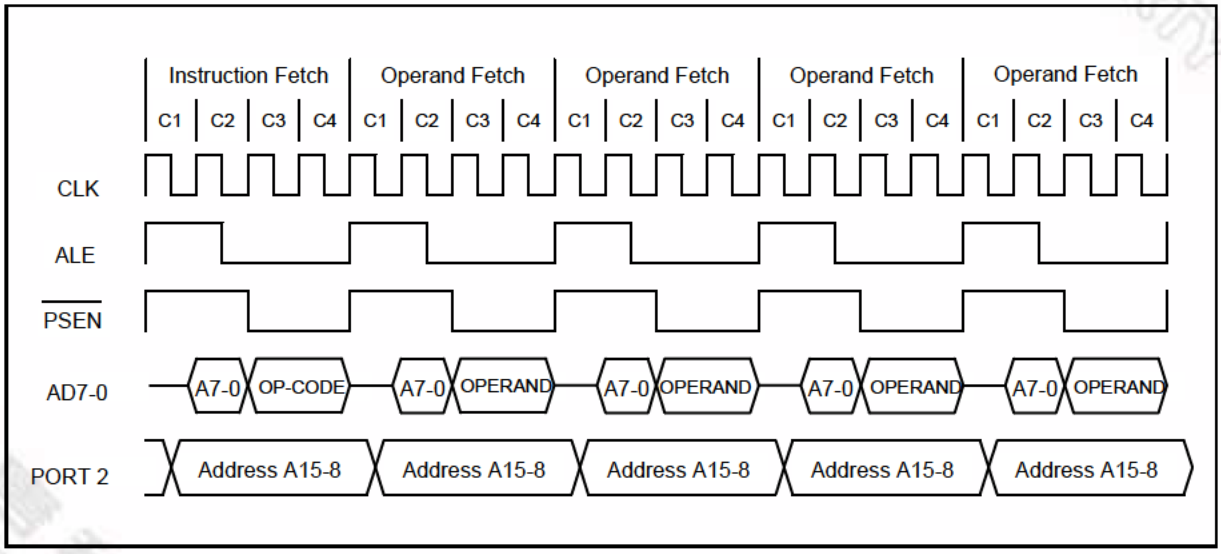


Figure 7-5 Five Cycle Instruction Timing

7.1.1 External Data Memory Access Timing

The timing for the MOVX instruction is another feature of the W79E658. In the standard 8051/52, the MOVX instruction has a fixed execution time of 2 machine cycles. However, in the W79E658, the duration of the access can be controlled by the user.

The instruction starts off as a normal op-code fetch that takes four clocks. In the next machine cycle, the W79E658 puts out the external memory address, and the actual access occurs. The user can control the duration of this access by setting the stretch value in CKCON, bits 2 – 0. As shown in the table below, these three bits can range from zero to seven, resulting in MOVX instructions that take two to nine machine cycles. The default value is one, resulting in a MOVX instruction of three machine cycles.

Stretching only affects the MOVX instruction. There is no effect on any other instruction or its timing, it is as if the state of the CPU is held for the desired period. The timing waveforms when the stretch value is zero, one, and two are shown below.

Table 7-2 Data Memory Cycle Stretch Values

M2	M1	M0	MACHINE CYCLES	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH IN CLOCKS	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 25 MHZ	$\overline{RD}$ OR $\overline{WR}$ STROBE WIDTH @ 40 MHZ
0	0	0	2	2	80 nS	50 nS
0	0	1	3 (default)	4	160 nS	100 nS
0	1	0	4	8	320 nS	200 nS
0	1	1	5	12	480 nS	300 nS
1	0	0	6	16	640 nS	400 nS
1	0	1	7	20	800 nS	500 nS
1	1	0	8	24	960 nS	600 nS
1	1	1	9	28	1120 nS	700 nS

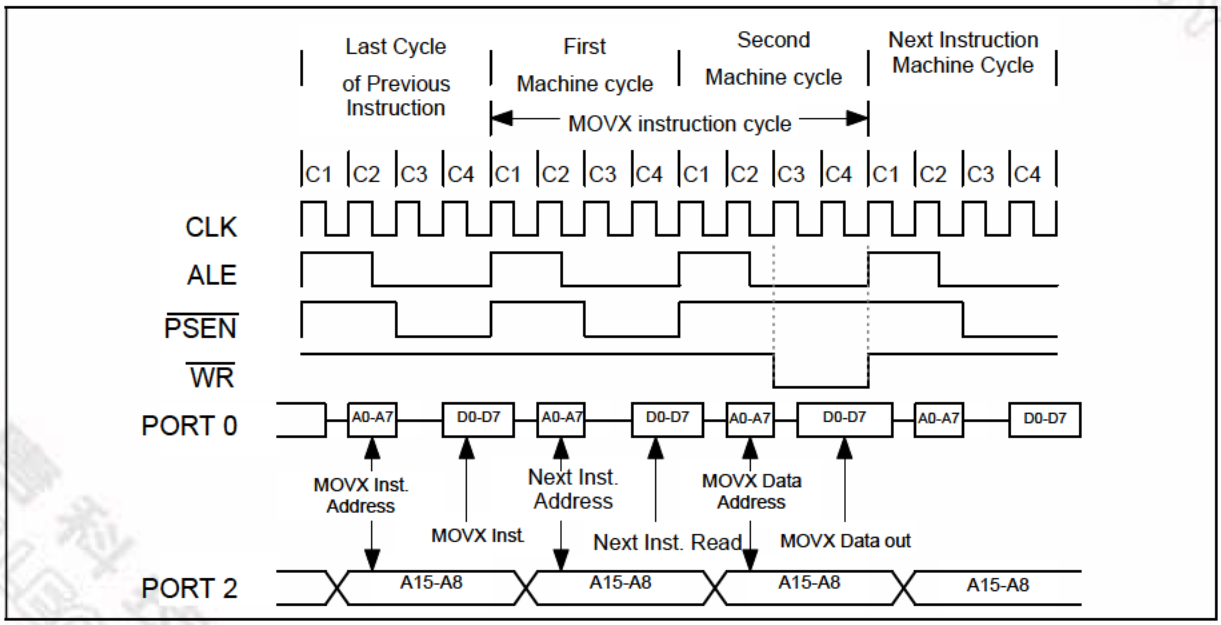


Figure 7-6 Data Memory Write with Stretch Value = 0

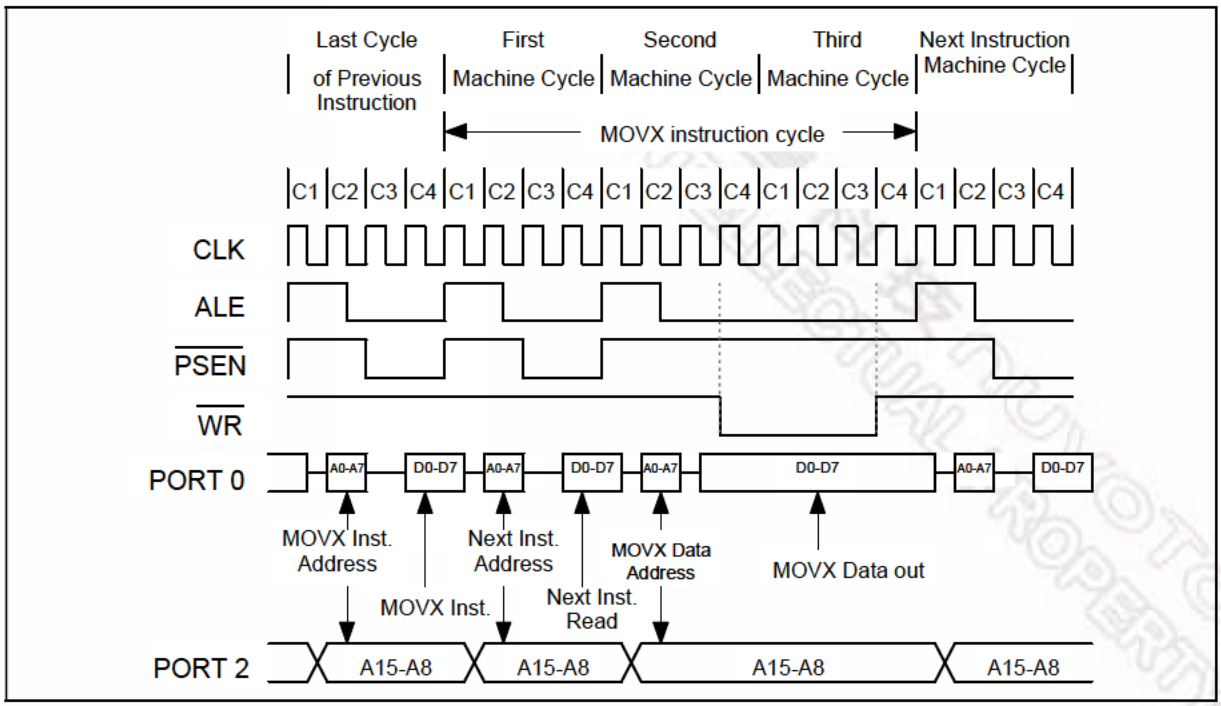


Figure 7-7 Data Memory Write with Stretch Value = 1

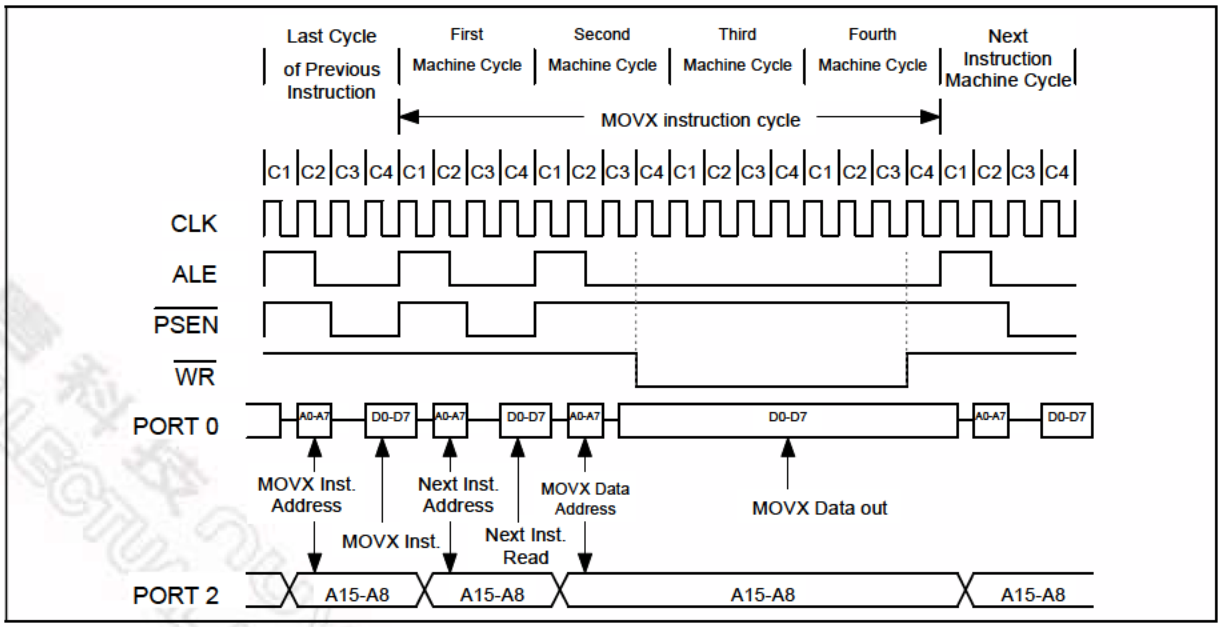


Figure 7-8 Data Memory Write with Stretch Value = 2

8. Power Management

The W79E658 provides idle mode and power-down mode to control power consumption. These modes are discussed in the next two sections, followed by a discussion of resets.

8.1 Idle Mode

Write a one to bit 0 in PCON at 87h to put the device in Idle mode. The instruction that sets the idle bit is the last instruction executed before the device goes into Idle mode. In Idle mode, the clock to the CPU is halted, but not the one to the Interrupt, Timer, Watchdog Timer, PWM, ADC, UART and I2C ports. This freezes the CPU state, including the Program Counter, Stack Pointer, Program Status Word, Accumulator and registers. The ALE and $\overline{PSEN}$ pins are held high, and port pins hold the same states they had when the device went into Idle mode. Table 8-1 below provides the values of various pins in Idle mode.

Idle mode can be terminated two ways. First, since the interrupt controller is still active, any enabled interrupt wakes up the processor. This automatically clears the Idle bit, terminates Idle mode, and executes the Interrupt Service Routine (ISR). After the ISR, the program resumes after the instruction that put the device into Idle mode.

Idle mode can also be exited by a reset, such as a high signal on the external RST pin, a power-on reset or a Watchdog Timer reset (if enabled). During reset, the program counter is reset to 0000h, so the instruction following the one that put the device into Idle mode is not executed. All the SFRs are also reset to their default values. Since the clock is already running, there is no delay, and execution starts immediately.

8.2 Power Down Mode

Write a one to bit 1 in PCON register at 87h to put the device in Power-Down mode. The instruction that sets the power-down bit is the last instruction executed before the device goes into Power-Down mode. In Power-Down mode, all the clocks and all activity stop completely, and power consumption is reduced to the lowest possible value. The ALE and $\overline{PSEN}$ pins are pulled low, and port pins output the values held by their respective registers. Table 8-1 provides the values of various pins in Power-Down mode.

The W79E658 can exit Power-Down mode two ways. First, it can be exited by a reset, such as a high signal on the external RST pin or a power-on reset. The Watchdog Timer cannot provide a reset to exit Power-Down mode because the clock has stopped. A reset terminates Power-Down mode, restarts the clock, and restarts program execution at 0000h.

The W79E658 can also exit Power-Down mode by an external interrupt pin, as long as the external input has been set to low level or falling edge detect, the corresponding interrupt is enabled, and the global enable (EA) bit is set. If these conditions are met, then a low-level or falling-edge signal on the external INT pin re-starts the oscillator. The device executes the interrupt service routine (ISR) for the corresponding external interrupt, and, afterwards, the program resumes execution after the one that put the device into Power-Down mode.

Table 8-1 Status of external pins during Idle and Power Down

MODE	PROGRAM MEMORY	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data

Power Down	External	0	0	Float	Data	Data	Data

9. Reset

The user has several hardware related options for placing the W79E658 into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software. There are two ways of putting the device into reset state. They are External reset and Watchdog reset.

9.1 Reset Conditions

There are three ways to reset the W79E658—External Reset, Watchdog Timer Reset and Power-On Reset. In general, most registers return to their default values regardless of the source of the reset, but a couple flags depend on the source. As a result, the user can use these flags to determine the cause of the reset.

The rest of this section discusses the three causes of resets and then elaborates on the reset state.

9.2 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST is one and remains there up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

9.3 Power-On Reset (POR)

If the power supply falls below V_{rst}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets.

9.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

9.5 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state and makes Port 0 float (as it does not have on-chip pull-up resistors). The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2 V, the minimum operating voltage for the RAM. If VDD falls below 2 V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depends on the source of the reset. The WDCON SFR is set to a 0x0x0xx0b on an external reset. WTRF is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF is not altered by an external reset. POR is set to 1 by a power-on reset. EWT is cleared to 0 on a Power-on reset and unaffected by other resets. All the bits in this SFR have unrestricted read access. The bits of POR, WDIF, EWT and RWT require Timed Access (TA) procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description. Table 9-1 lists the different reset values.

Table 9-1 The WDCON reset values in three reset conditions

WDCON	Watch-Dog Control	D8H	(DF) -	(DE) POR	(DD) -	(DC) -	(DB) WDIF	(DA) WTRF	(D9) EWT	(D8) RWT	0x0x 0xx0B External reset 0x0x 01x0B Watchdog reset 0100 0000B Power on reset

10. Interrupts

The W79E658 has a two priority level interrupt structure with 10 interrupt sources. Each interrupt source has a separate priority bit, interrupt flag, interrupt enable bit, and interrupt vector. In addition, all the interrupts can be globally disabled.

10.1 Interrupt Sources

External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be edge-triggered or level-triggered, depending on bits IT0 and IT1. In edge-triggered mode, the INTx input is sampled every machine cycle. If the sample is high in one cycle and low in the next, then a high-to-low transition is detected, and the interrupt request flag IEx in TCON is set. This flag requests the interrupt, and it is automatically cleared when the interrupt service routine is called. Since external interrupts are sampled every machine cycle, the input has to be held high or low for at least one complete machine cycle. In level-triggered mode, the requesting source has to hold the pin low until the interrupt is serviced. The IEx flag is not cleared automatically when the service routine is called, and, if the input continues to be held low after the service routine is completed, the signal may generate another interrupt request.

Timer 0 and 1 interrupts are generated by the TF0 and TF1 flags. These flags are set by a timer overflow, and they are cleared automatically when the interrupt service routine is called. The Timer 2 interrupt is generated by a logical-OR of the TF2 (overflow) and the EXF2 (capture / reload events) flags. The hardware does not clear these flags when the interrupt service routine is called, so the software has to resolve the cause of the interrupt and clear the appropriate flag(s).

When ADC conversion is completed hardware will set flag ADCI to logic high to request ADC interrupt if bit EADC (IE.6) is in high state. ADCI is cleared by software only. W79E658 provides 2 identically independent I2C serial ports, I2C1 and I2C2. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C2 bits are both set, the I2C2 interrupt is requested. **SI must be cleared by software**.

The Watchdog Timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by bit EIE.4, then an interrupt is generated.

All of the interrupt flags can be set or reset by software, as well as hardware, by setting or clearing the appropriate bit in the IE register. This register also has the global disable bit EA, which can be cleared to disable all interrupts.

10.2 Priority Level Structure

There are two priority levels for interrupts, high and low, and the priority of each interrupt source can be set individually. When two interrupts have the same priority, there is a pre-defined hierarchy to resolve simultaneous requests. This hierarchy is shown below, highest-priority interrupts first.

Table 10-1 Priority structure of interrupts

SOURCE	FLAG	VECTOR ADDRESS	FLAG CLEARED BY	PRIORITY LEVEL
External Interrupt 0	IE0	0003H	Hardware, software	1
Timer 0 Overflow	TF0	000BH	Hardware, software	2
External Interrupt 1	IE1	0013H	Hardware, software	3
Timer 1 Overflow	TF1	001BH	Hardware, software	4
Serial Port	RI + TI	0023H	Hardware, software	5
Timer 2 Overflow	TF2 + EXF2	002BH	Software	6
A/D Converter	ADCI	033H	Software	7
I2C Channel 1	I2C1 SI	03BH	Software	8
I2C Channel 2	I2C2 SI	043H	Software	9

Watchdog Timer	WDIF	0063H	Software	10 (lowest)

11. Programmable Timers/Counters

The W79E658 has three 16-bit programmable timer/counters.

11.1 Timer/Counters 0 & 1

TM0 and TM1 are 16-bit Timer/Counters and are nearly identical. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two timers can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/4 of the system clock. In "Counter" mode, the register is incremented on the falling edge of the corresponding external input pins, T0 for Timer 0 and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the minimum period at which counting will take place is double of the machine cycle. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

11.1.1 Time-Base Selection

The W79E658 can operate like the standard 8051/52 family, counting at the rate of 1/12 of the clock speed, or in turbo mode, counting at the rate of 1/4 clock speed. The speed is controlled by the T0M and T1M bits in CKCON, and the default value is zero, which uses the standard 8051/52 speed.

11.1.2 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (P3.4 for Timer 0) or T1 (P3.5 for Timer 1). For clock cycles, the time base may be 1/12 or 1/4 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated below.

11.1.3 Mode 1

Mode 1 is the same as Mode 0, except that the timer/counter is 16 bits, instead of 13 bits.

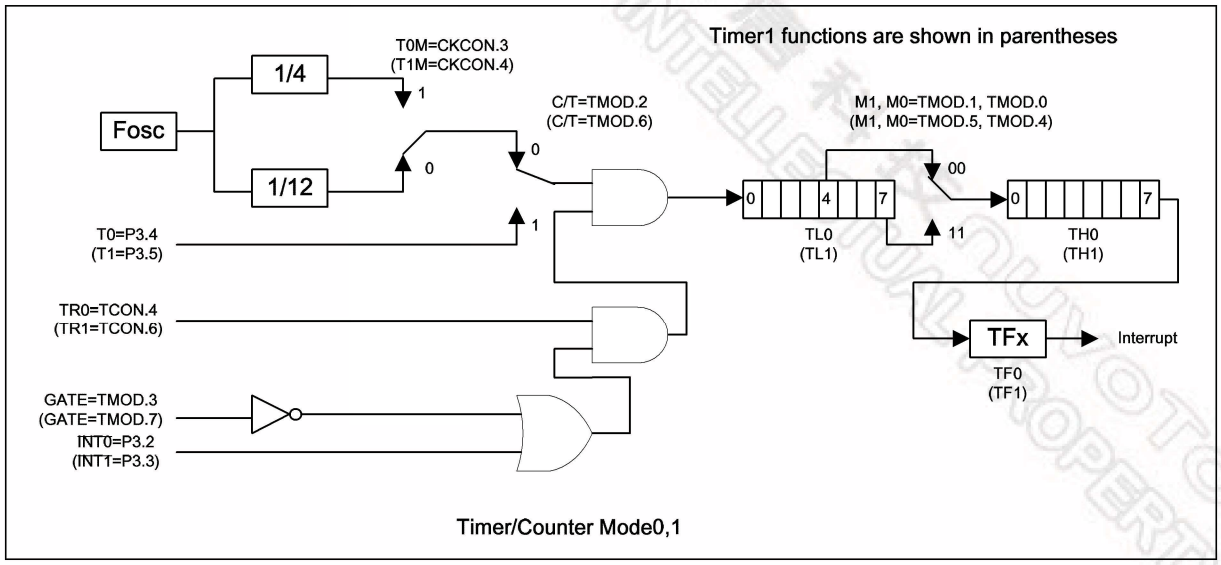


Figure 11-1 Timer/Counters 0/1 in Mode 0 & Mode 1

11.1.4 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as a 8 bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/4) or pulses on pin Tn.

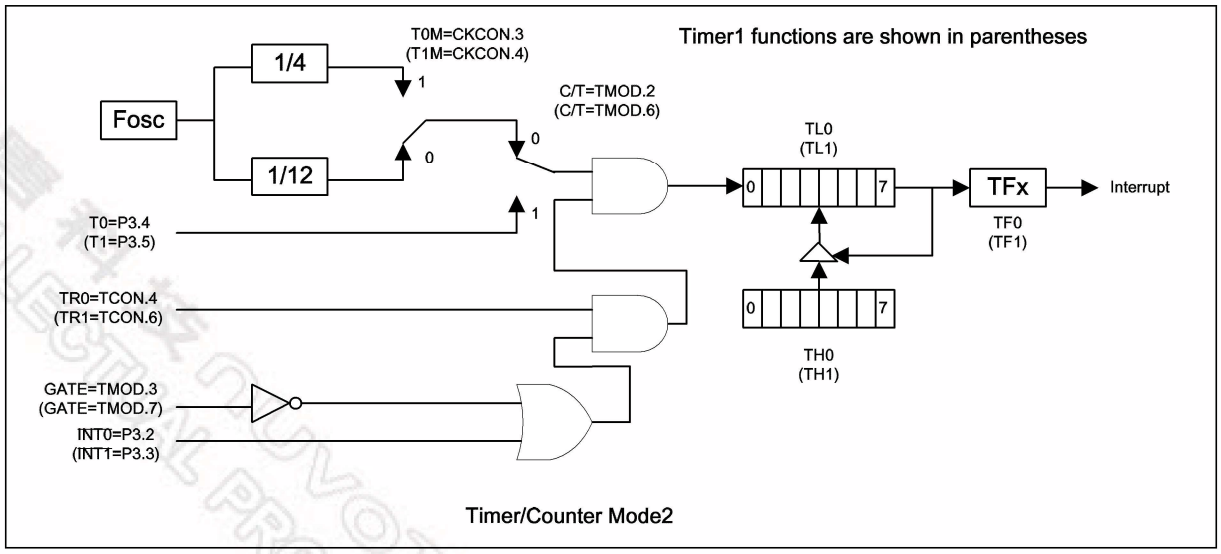


Figure 11-2 Timer/Counter 0/1 in Mode 2

11.1.5 Mode 3

Mode 3 is used when an extra 8-bit timer is needed. It has a different effect on Timer 0 and Timer 1. TL0 and TH0 become two separate 8 bit counters. TL0 uses the Timer 0 control bits C/$\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0, and it can be used to count clock cycles (clock/12 or clock/4) or falling edges on pin T0, as determined by C/$\overline{T}$ (TMOD.2). TH0 becomes a clock-cycle counter (clock/12 or clock/4) and takes over the Timer 1 enable bit TR1 and overflow flag TF1. In contrast, mode 3 simply freezes Timer 1. If Timer 0 is in mode 3, Timer 1 can still be used in modes 0, 1 and 2, but it no longer has control over TR1 and TF1. Therefore when Timer 0 is in Mode 3, Timer 1 can only count oscillator cycles, and it does not have an interrupt or flag. With these limitations, baud rate generation is its most practical application, but other time-base functions may be achieved by reading the registers.

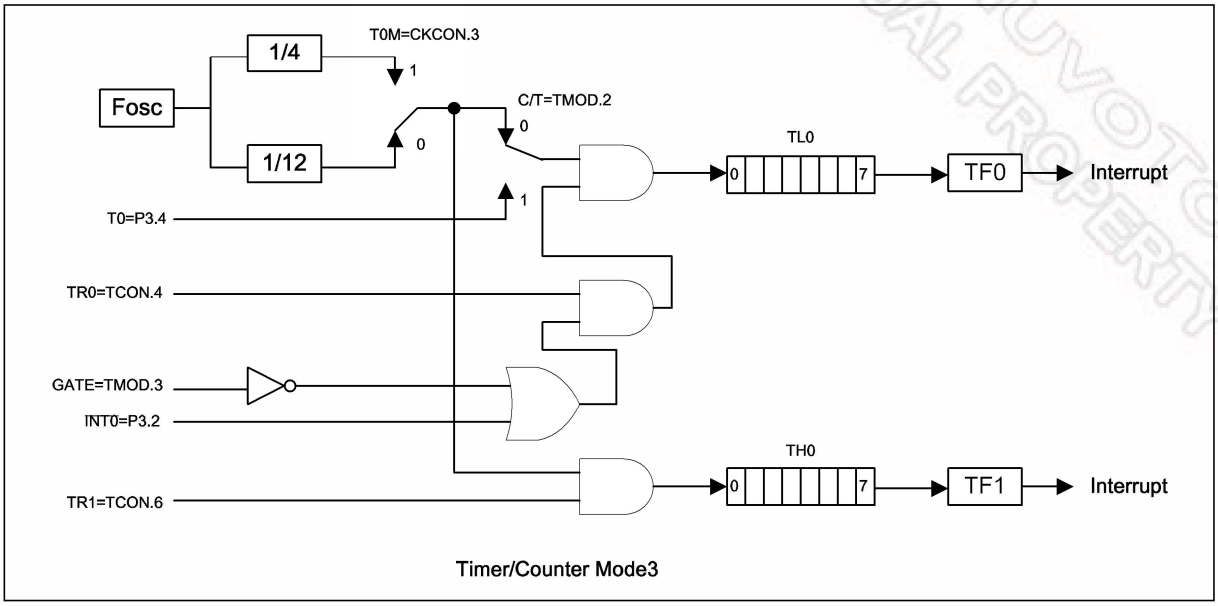


Figure 11-3 Timer/Counter 0 Mode 3

11.2 Timer/Counter 2

Timer/Counter 2 is a 16-bit up/down-counter equipped with a capture/reload capability. The clock source for Timer/Counter 2 may be the external T2 pin (C/$\overline{T2}$ = 1) or the crystal oscillator (C/$\overline{T2}$ = 0), divided by 12 or 4. The clock is enabled and disabled by TR2. Timer/Counter 2 runs in one of four operating modes, each of which is discussed below.

11.2.1 Capture Mode

Capture mode is enabled by setting CP/$\overline{RL2}$ in T2CON to 1. In capture mode, Timer/Counter 2 is a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the timer overflow flag TF2 is set, and an interrupt is generated, if enabled.

If the EXEN2 bit is set, a negative transition on the T2EX pin captures the current value of TL2 and TH2 in the RCAP2L and RCAP2H registers. It also sets the EXF2 bit in T2CON, which generates an interrupt if enabled. In addition, if the T2CR bit in T2MOD is set, the W79E658 resets Timer 2 automatically after the capture. This is illustrated below.

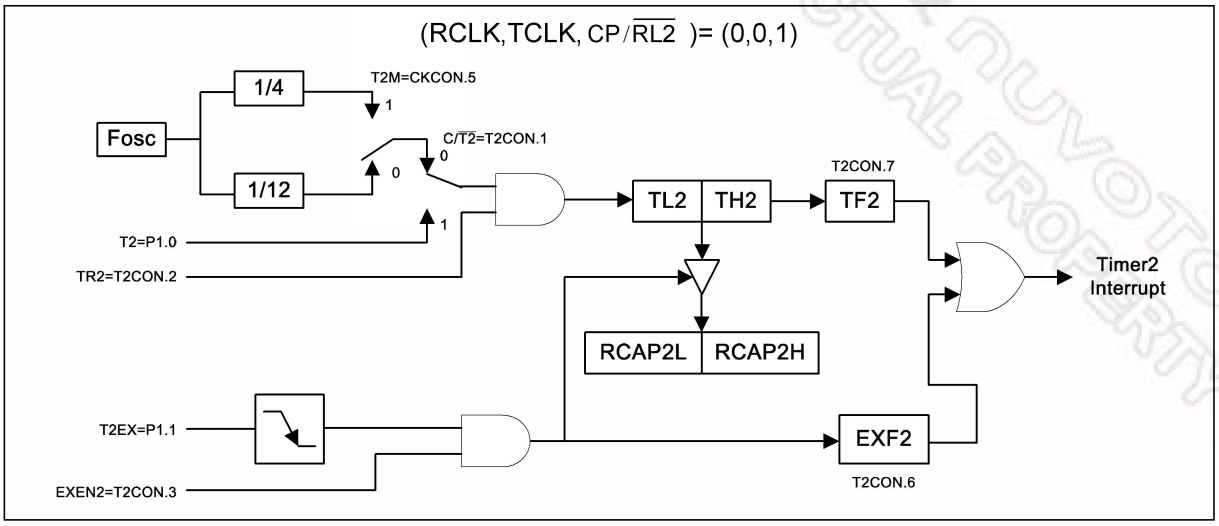


Figure 11-4 Timer2 16-Bit Capture Mode

11.2.2 Auto-reload Mode, Counting up

This mode is enabled by clearing CP/$\overline{RL2}$ in T2CON register and DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up-counter. When the counter rolls over from FFFFh to 0000h, the timer overflow flag TF2 is set, and TL2 and TH2 capture the contents of RCAP2L and RCAP2H, respectively. Alternatively, if EXEN2 is set, a negative transition on the T2EX pin causes a reload, which also sets the EXF2 bit in T2CON.

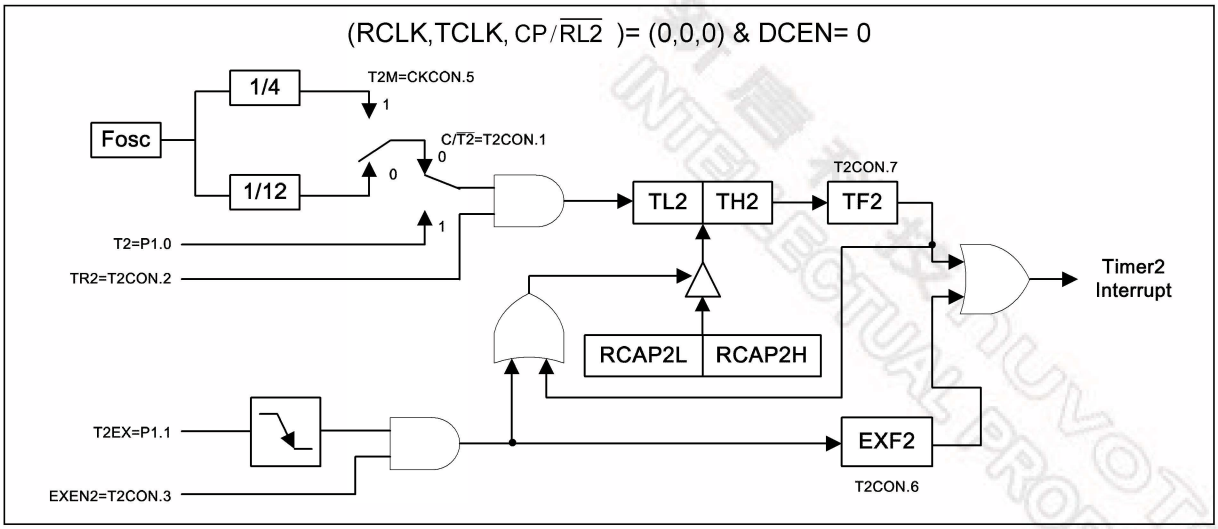


Figure 11-5 16-Bit Auto-reload Mode, Counting Up

11.2.3 Auto-reload Mode, Counting Up/Down

This mode is enabled by clearing CP / $\overline{RL2}$ in T2CON and setting DCEN in T2MOD. In this mode, Timer/Counter 2 is a 16-bit up/down-counter, whose direction is controlled by the T2EX pin (1 = up, 0 = down). If Timer/Counter 2 is counting up, an overflow reloads TL2 and TH2 with the contents of the capture registers RCAP2L and RCAP2H. If Timer/Counter 2 is counting down, TL2 and TH2 are loaded with FFFFh when the contents of Timer/Counter 2 equal the capture registers RCAP2L and RCAP2H. Regardless of direction, reloading sets the TF2 bit. It also toggles the EXF2 bit, but the EXF2 bit can not generate an interrupt in this mode. This is illustrated below.

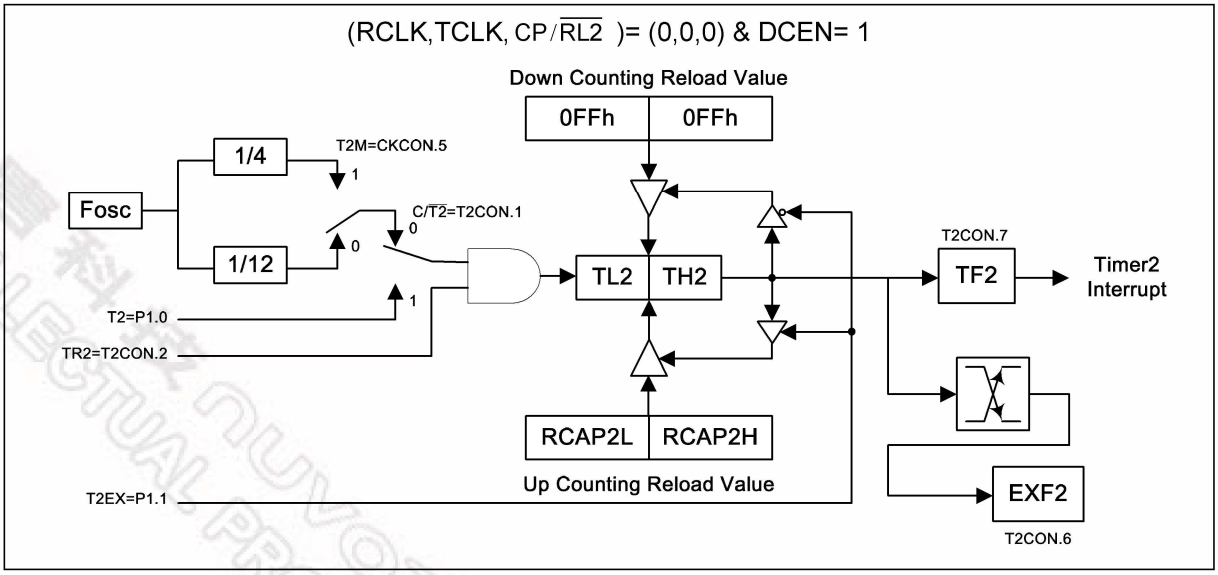


Figure 11-6 16-Bit Auto-reload Up/Down Counter

11.2.4 Baud Rate Generator Mode

Baud rate generator mode is enabled by setting either RCLK or TCLK in T2CON. In baud rate generator mode, Timer/Counter 2 is a 16-bit counter with auto-reload when the count rolls over from FFFFh. However, rolling-over does not set TF2. If EXEN2 is set, then a negative transition on the T2EX pin sets EXF2 bit in the T2CON register and causes an interrupt request.

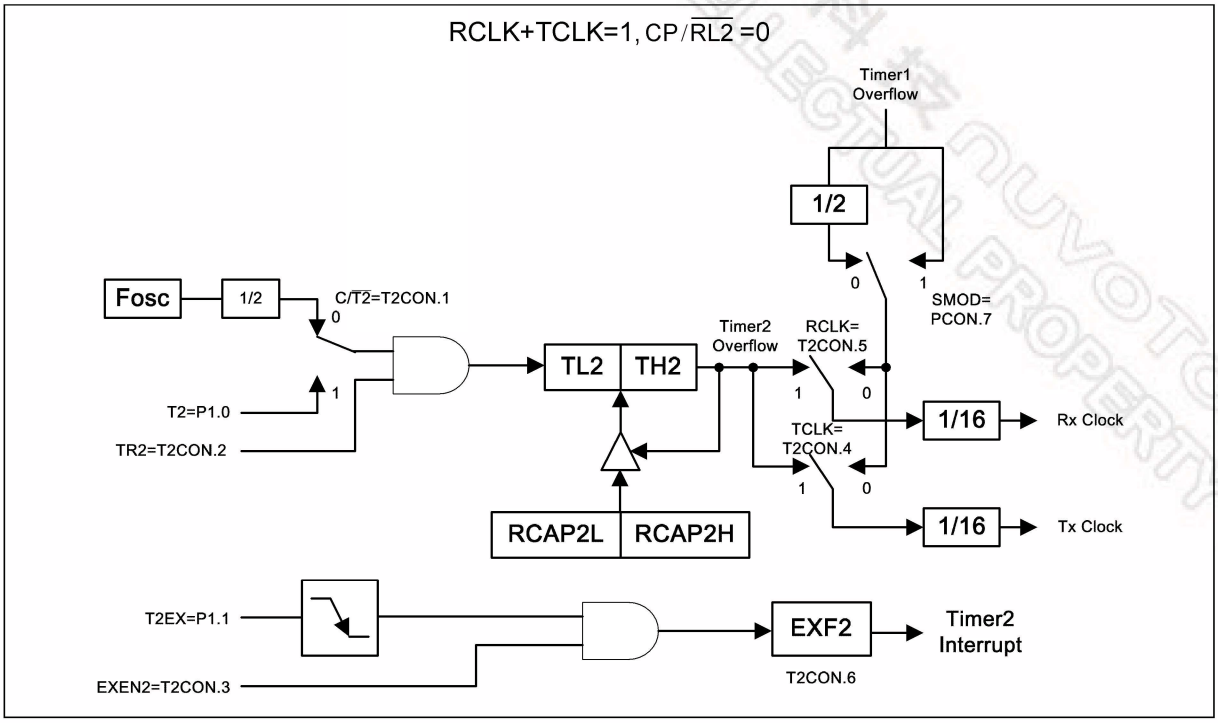


Figure 11-7 Baud Rate Generator Mode

12. Watchdog Timer

The Watchdog Timer is a free-running timer that can be programmed to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock to determine the time-out interval. When the time-out occurs, a flag is set, which can generate an interrupt or a system reset, if enabled. The interrupt occurs if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together.

The main use of the Watchdog Timer is as a system monitor. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. The Watchdog Timer helps the W79E658 recovers from these states. During development, the code is first written without the watchdog interrupt or reset. Then, the watchdog interrupt is enabled to identify code locations where the interrupt occurs, and instructions are inserted to reset the Watchdog Timer in these locations. In the final version, the watchdog interrupt is disabled, and the watchdog reset is enabled. If errant code is executed, the Watchdog Timer is not reset at the required times, so a Watchdog Timer reset occurs.

When used as a simple timer, the reset and interrupt functions are disabled. The Watchdog Timer can be started by RWT and sets the WDIF flag after the selected time interval. Meanwhile, the program polls the WDIF flag to find out when the selected time interval has passed. Alternatively, the Watchdog Timer can also be used as a very long timer. In this case, the interrupt feature is enabled.

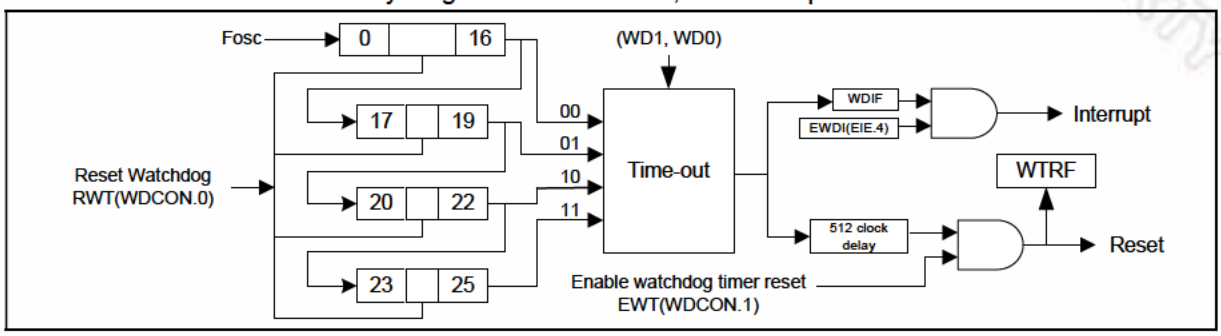


Figure 12-1 Watchdog Timer

The Watchdog Timer should be started by RWT because this ensures that the timer starts from a known state. The RWT bit is self-clearing; i.e., after writing a 1 to this bit, the bit is automatically cleared. After setting RWT, the Watchdog Timer begins counting clock cycles. The time-out interval is selected by WD1 and WD0 (CKCON.7 and CKCON.6).

Table 2 Time-out values for the Watchdog Timer

WD1	WD0	INTERRUPT TIME-OUT	RESET TIME-OUT	NUMBER OF CLOCKS	TIME @ 10 MHZ	TIME @ 11.0592 MHZ	TIME @ 25 MHZ
0	0	2^{17}	2^{17} + 512	131072	13.11 mS	11.85 mS	5.24 mS
0	1	2^{20}	2^{20} + 512	1048576	104.86 mS	94.81 mS	41.94 mS
1	0	2^{23}	2^{23} + 512	8388608	838.86 mS	758.52 mS	335.54 mS
1	1	2^{26}	2^{26} + 512	67108864	6710.89 mS	6068.15 mS	2684.35 mS

When the selected time-out occurs, the watchdog interrupt flag WDIF (WDCON.3) is set. Then, if there is no RWT and if the Watchdog Timer reset EWT (WDCON.1) is enabled, the Watchdog Timer reset occurs 512 clocks later. This reset lasts two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) is set, which indicates that the Watchdog Timer caused the reset.

The Watchdog Timer is disabled by a power-on/fail reset. The external reset and Watchdog Timer reset can not disable Watchdog Timer but restart the Timer.

The control bits that support the Watchdog Timer are discussed below.

Watchdog Timer Control (WDCON)

7	-	Reserved.
6	POR	Power-on reset flag. The hardware sets this flag during power–up, and it can only be cleared by software. This flag can also be written by software.
5-4	-	Reserved.
3	WDIF	Watchdog Timer Interrupt Flag. If the watchdog interrupt is enabled, the hardware sets this bit to indicate that the watchdog interrupt has occurred. If the interrupt is not enabled, this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
2	WTRF	Watchdog Timer Reset Flag. If EWT is 0, the Watchdog Timer has no affect on this bit. Otherwise, the hardware sets this bit when the Watchdog Timer causes a reset. It can be cleared by software or a power-fail reset. It can be also read by software, which helps determine the cause of a reset.
1	EWT	Enable Watchdog-Timer Reset. Set this bit to enable the Watchdog Timer Reset function.
0	RWT	Reset Watchdog Timer. Set this bit to reset the Watchdog Timer before a time-out occurs. This bit is automatically cleared by the hardware.

The EWT, WDIF and RWT bits are protected by the Timed Access procedure. This procedure prevents software, especially errant code, from accidentally enabling or disabling the Watchdog Timer. An example is provided below.

```
        org     63h
        mov     TA,#AAH
        mov     TA,#55H
        clr     WDIF
        jnb     execute_reset_flag,bypass_reset      ; Test if CPU need to reset.
        jmp     $                                    ; Wait to reset
bypass_reset:
        mov     TA,#AAH
        mov     TA,#55H
        setb    RWT
        reti

        org     300h
start:
        mov     ckcon,#01h                   ; select 2 ^ 17 timer
```

```
;       mov     ckcon,#61h              ; select 2 ^ 20 timer
;       mov     ckcon,#81h              ; select 2 ^ 23 timer
;       mov     ckcon,#c1h              ; select 2 ^ 26 timer
        mov     TA,#aah
        mov     TA,#55h
        mov     WDCON,#00000011B
        setb    EWDI
        setb    ea
        jmp     $                       ; wait time out
```

Clock Control

WD1, WD0: CKCON.7, CKCON.6 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the Watchdog Timer. The reset interval is 512 clocks longer than the selected interval. The default time-out is 2^{17} clocks, the shortest time-out period.

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13. Pulse-Width-Modulated (PWM) Outputs

There are six pulse-width-modulated (PWM) output channels that can generate pulses of programmable length and interval. The frequency is controlled by the 8-bit prescale PWMP, which supplies the clock for the 8-bit PWM counter that counts modular 255 (0 ~ 254). The same prescale and counter are shared by all the PWM channels. The PWM outputs are weakly pulled high.

Each channel is enabled and disabled by bit ENPWM*n* (n = 0 ~ 5). If channel *n* is enabled, the PWM counter is compared to the corresponding register PWM*n*. When PWM*n* is greater than the PWM counter, the corresponding PWM output is set high. When the register value is equal to or less than the counter value, the output is set low. Therefore, the pulse-width ratio is defined by the contents of PWM0, PWM1, PWM2, PWM3, PWM4 and PWM5 and may be programmed in increments of 1/255. This is illustrated below.

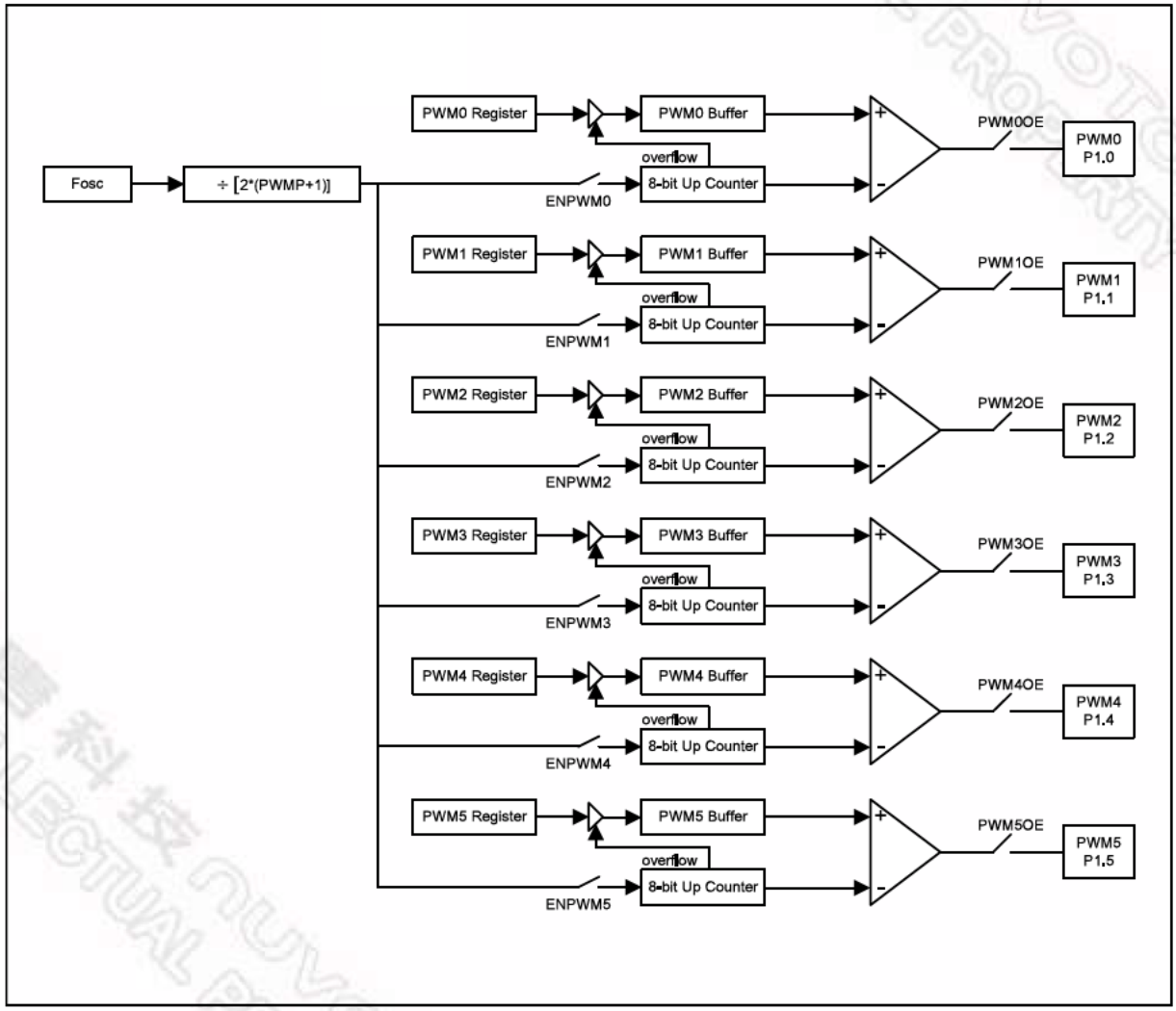


Figure 13-1 PWM block diagram

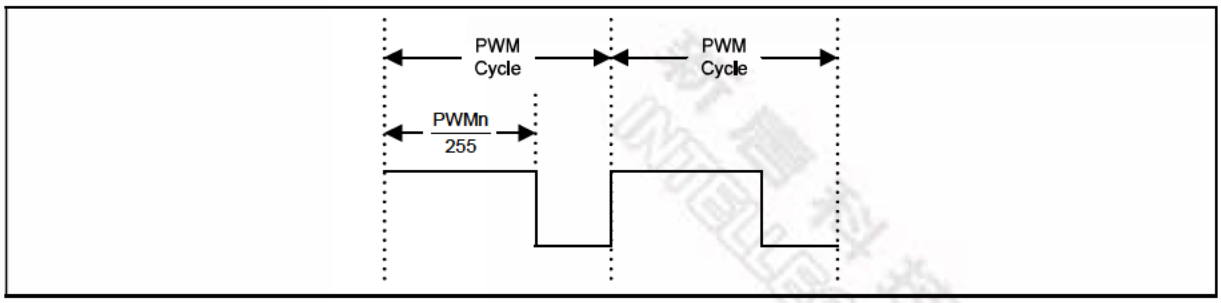


Figure 13-2 PWM Duty Ratio

If register PWM*n* is loaded with a new value, the associated output is updated immediately. By loading PWM*n* with 00H or FFH, the corresponding channel provides a constant high or low level output, respectively. Since the 8-bit counter counts modulo 255, it can never actually reach FFh, so the output remains low all the time.

Buffered PWM outputs may be used to drive DC motors. In this case, the rotation speed of the motor is proportional to the contents of PWM*n*. The repetition frequency Fpwm for channel *n* is given by:

$$Fpwm = \frac{Fosc}{2 \times (1 + PWMP) \times 255}$$

Prescale division factor = PWM + 1

$$\text{PWMn high/low ratio of PWMn} = \frac{(PWMn)}{255 - (PWMn)}$$

This gives a repetition frequency range of 123 Hz to 31.4 KHz (f_{osc} = 16 MHz).

Please refer as below code.

```
mov   pwmcon1, #00110011b        ; enable pwm3, 2, 1, 0
mov   pwmp, #40h                 ; Fpwm = Fosc/(2*(1+PWMP)*255)
mov   pwm0, #14h                 ; duty cycle high/low = PWM0/(255-PWM0)
mov   pwm1, #18h
mov   pwm2, #20h
mov   pwm3, #b0h
mov    pwmcon1, #11111111b       ; output enable pwm3, 2, 1, 0
```

14. Serial Port

The W79E658 serial port is a full-duplex port, and the W79E658 provides additional features, such as Frame Error Detection and Automatic Address Recognition. The serial port is capable of synchronous and asynchronous communication. In synchronous mode, the W79E658 generates the clock and operates in half-duplex mode. In asynchronous mode, the serial port can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF, but any write to SBUF writes to the transmit register while any read from SBUF reads from the receive buffer. The serial port can operate in four modes, as described below.

14.1 Mode 0

This mode provides half-duplex, synchronous communication with external devices. In this mode, serial data is transmitted and received on the RXD line, and the W79E658 provides the shift clock on TxD, whether the device is transmitting or receiving. Eight bits are transmitted or received per frame, LSB first. The baud rate is 1/12 or 1/4 of the oscillator frequency, as determined by the SM2 bit (SCON.5; 0 = 1/12; 1 = 1/4). This programmable baud rate is the only difference between the standard 8051/52 and the W79E658 in mode 0.

Any write to SBUF starts transmission. The shift clock is activated, and data is shifted out on RxD until all eight bits are transmitted. If SM2 is 1, the data appears on RxD one clock period before the falling edge of the shift clock on TxD. Then, the clock remains low for two clock periods before going high again. If SM2 is 0, the data appears on RxD three clock periods before the falling edge of the shift clock on TxD, and the clock on TxD remains low for six clock periods before going high again. This ensures that, at the receiving end, the data on the RxD line can be clocked on the rising edge of the shift clock or latched when the clock is low. The TI flag is set high in C1 following the end of transmission. The functional block diagram is shown below.

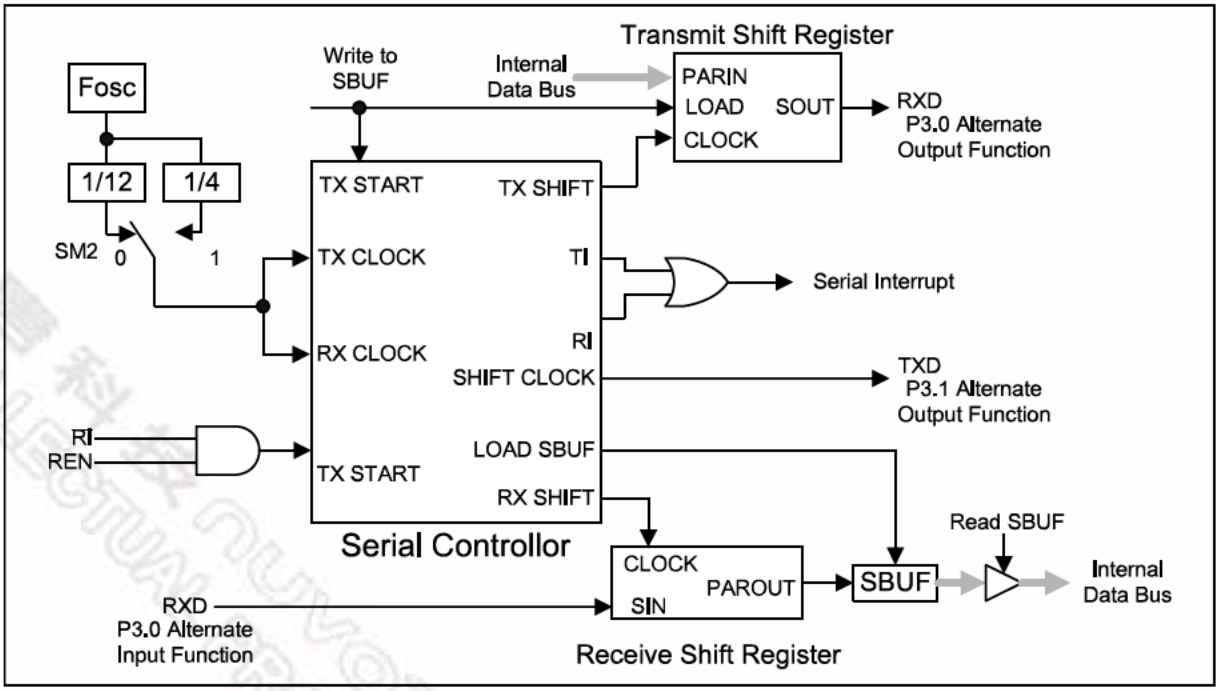


Figure 14-1 Serial Port Mode 0

The serial port receives data when REN is 1 and RI is zero. The shift clock (TxD) is activated, and the serial port latches data on the rising edge of the shift clock. The external device should, therefore, present data on the falling edge of the shift clock. This process continues until all eight bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock, which stops reception until RI is cleared by the software.

14.2 Mode 1

In Mode 1, full-duplex asynchronous communication is used. Frames consist of ten bits transmitted on TXD and received on RXD. The ten bits consist of a start bit (0), eight data bits (LSB first), and a stop bit (1). When receiving, the stop bit goes into RB8 in SCON. The baud rate in this mode is 1/16 or 1/32 of the Timer 1 overflow, and since Timer 1 can be set to a wide range of values, a wide variation of baud rates is possible.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed at C1 following the next rollover. After all eight bits are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the tenth rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted immediately, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in eight data bits, the stop bit is received. Then, if

1. RI is 0 and
2. SM2 is 0 or the received stop bit is 1

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame is lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD.

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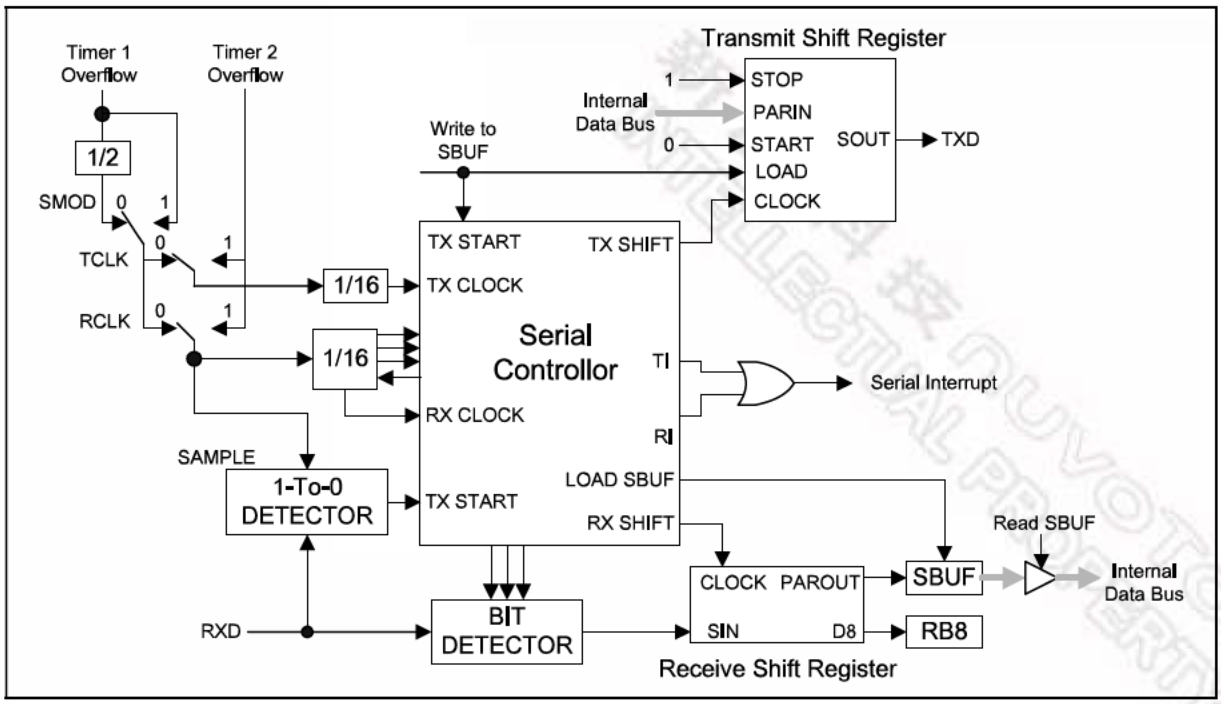


Figure 14-2 Serial Port Mode 1

14.3 Mode 2

In Mode 2, full-duplex asynchronous communication is used. Frames consist of eleven bits: one start bit (0), eight data bits (LSB first), a programmable ninth bit (TB8) and a stop bit (0). When receiving, the ninth bit is put into RB8. The baud rate is 1/16 or 1/32 of the oscillator frequency, as determined by SMOD in PCON.

Transmission begins with a write to SBUF but is synchronized with the divide-by-16 counter, not the write to SBUF. The start bit is put on TxD pin at C1 following the first roll-over of the divide-by-16 counter, and the next bit is placed on TxD at C1 following the next rollover. After all nine bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the next C1 state, or the 11th rollover of the divide-by-16 counter after the write to SBUF.

Reception is enabled when REN is high, and the serial port starts receiving data when it detects a falling edge on RxD. The falling-edge detector monitors the RxD line at 16 times the selected baud rate. When a falling edge is detected, the divide-by-16 counter is reset to align the bit boundaries with the rollovers of the counter. The 16 states of the counter divide the bit time into 16 slices. Bit detection is done on a best-of-three basis using samples at the 8th, 9th and 10th counter states. If the first bit after the falling edge is not 0, the start bit is invalid, reception is aborted, and the serial port resumes looking for a falling edge on RxD. If a valid start bit is detected, the rest of the bits are shifted into SBUF. After shifting in nine data bits, the stop bit is received. Then, if

1. RI is 0 and
2. SM2 is 0 or the received stop bit is 1

the stop bit goes into RB8, the eight data bits go into SBUF, and RI is set. Otherwise, the received frame may be lost. In the middle of the stop bit, the receiver resumes looking for a falling edge on RxD. The functional description is shown in the figure below.

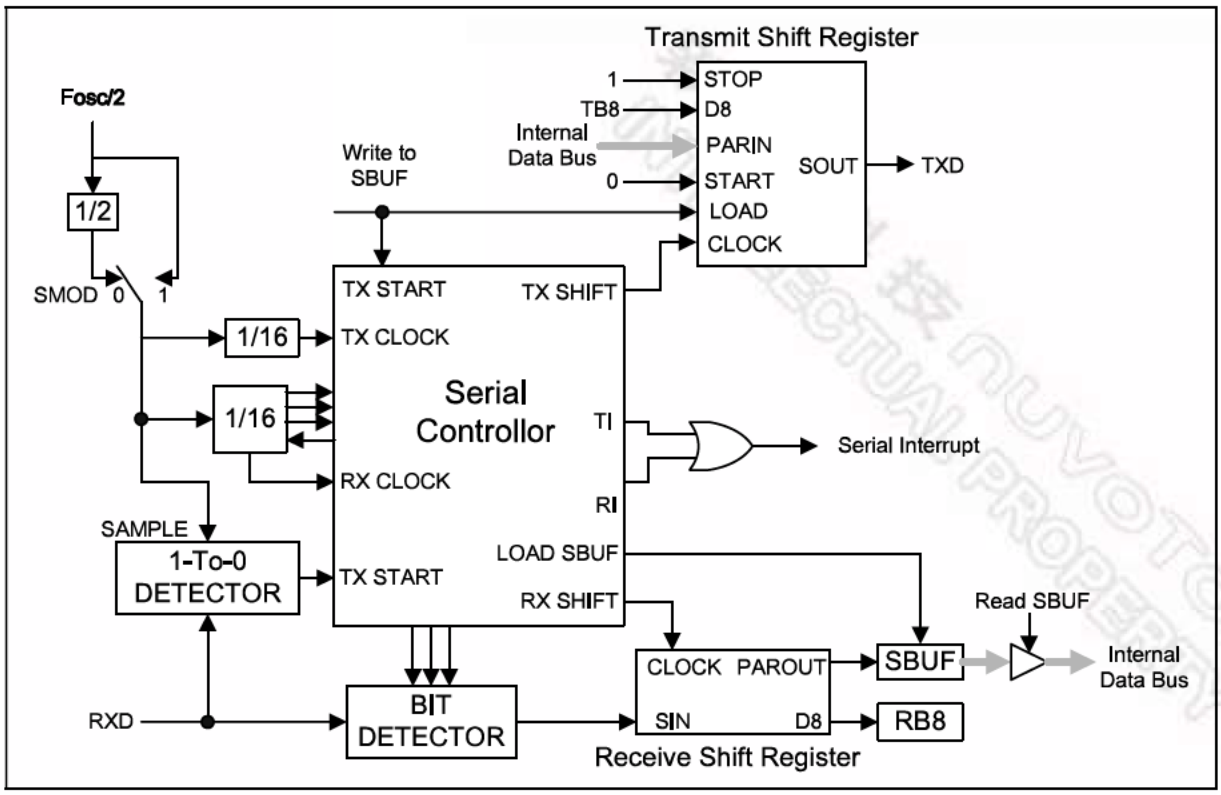


Figure 14-3 Serial Port Mode 2

14.4 Mode 3

This mode is the same as Mode 2, except that the baud rate is programmable. The program must select the mode and baud rate in SCON before any communication can take place. Timer 1 should be initialized if Mode 1 or Mode 3 will be used.

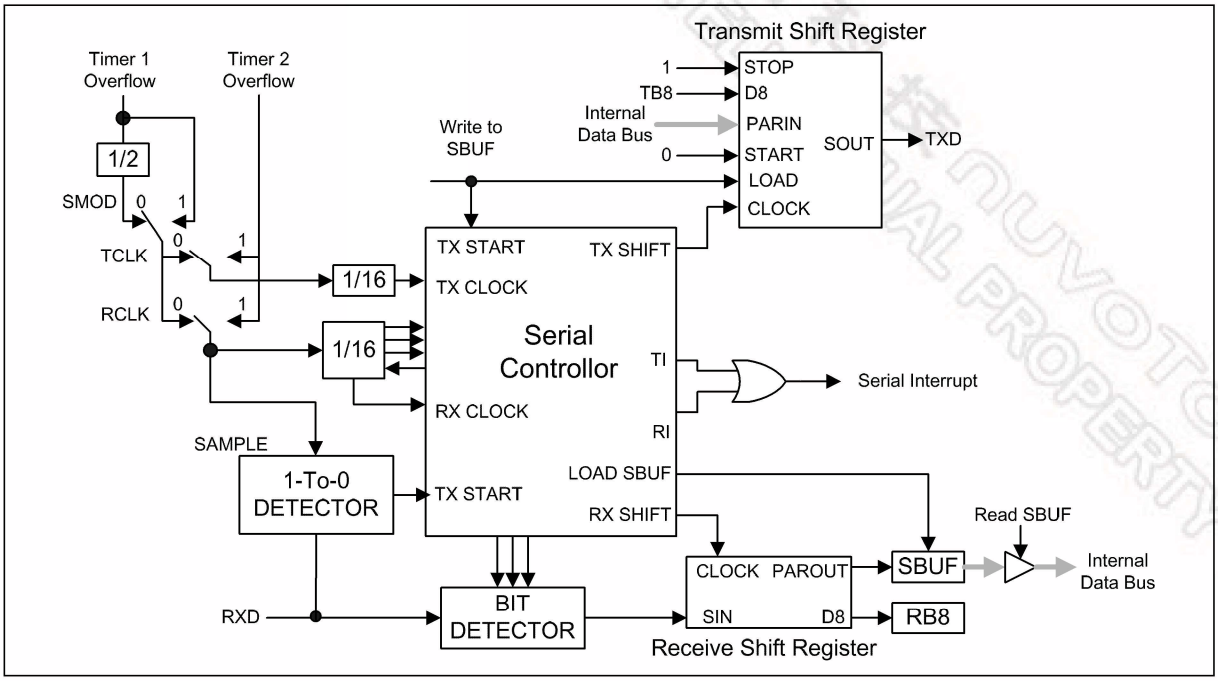


Figure 14-4 Serial Port Mode 3

Table 14-1 Serial Ports Modes

SM0	SM1	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	Synch.	4 or 12 OSC	8 bits	No	No	None
0	1	1	Asynch.	Timer 1 or 2	10 bits	1	1	None
1	0	2	Asynch.	32 or 64 OSC	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

14.5 Framing Error Detection

A frame error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically, a frame error is due to noise or contention on the serial communication line. The W79E658 has the ability to detect framing errors and set a flag that can be checked by software.

The frame error FE (FE_1) bit is located in SCON.7. This bit is SM0 in the standard 8051/52 family, but, in the W79E658, it serves a dual function and is called SM0/FE. There are actually two separate flags, SM0 and FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6). When SMOD0 is set to 1, the FE flag is accessed. When SMOD0 is set to 0, the SM0 flag is accessed.

The FE bit is set to 1 by the hardware, but it must be cleared by the software. Once FE is set, any frames received afterwards, even those without errors, do not clear the FE flag. The flag has to be cleared by the software. Note that SMOD0 must be set to 1 while reading or writing FE.

14.6 Multiprocessor Communications

Multiprocessor communication is available in modes 1, 2 and 3 and makes use of the 9th data bit and the automatic address recognition feature. This approach eliminates the software overhead required to check every received address and greatly simplifies the program.

In modes 2 and 3, address bytes are distinguished from data bytes by 9th bit set, which is set high in address bytes. When the master processor wants to transmit a block of data to one of the slaves, it first sends the address of the target slave(s). The slave processors have already set their SM2 bits high so that they are only interrupted by an address byte. The automatic address recognition feature then ensures that only the addressed slave is actually interrupted. This feature compares the received byte to the slave's Given or Broadcast address and only sets the RI flag if the bytes match. This slave then clears the SM2 bit, clearing the way to receive the data bytes. The unaddressed slaves are not affected, as they are still waiting for their address.

In mode 1, the 9th bit is the stop bit, which is 1 in valid frames. Therefore, if SM2 is 1, RI is only set if a valid frame is received and if the received byte matches the Given or Broadcast address.

The master processor can selectively communicate with groups of slaves using the Given Address or all the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN registers. The slave address is the 8-bit value specified in SADDR. SADEN is a mask for the value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is a don't-care condition in the address comparison. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This provides flexibility to address multiple slaves without changing addresses in SADDR.

The following example shows how to setup the Given Addresses to address different slaves.

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Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given Address for slaves 1 and 2 differ in the LSB. In slave 1, it is a don't-care, while, in slave 2, it is 1. Thus, to communicate with only slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly, bit 1 is 0 for slave 1 and don't-care for slave 2. Hence, to communicate only with slave 2, the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. Since bit 3 is don't-care for both slaves, two different addresses can address both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously using the Broadcast Address. The Broadcast Address is formed from the logical OR of the SADDR and SADEN registers. The zeros in the result are don't–care values. In most cases, the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111X) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN registers are located at addresses A9h and B9h, respectively. These two registers default to 00h, so the Given Address and Broadcast Address default to XXXX XXXX (i.e., all bits don't-care), which effectively removes the multiprocessor communications feature

15. I2C Serial Ports

W79E658 supports two identical but independent hardware I2C ports to transmit/receive data to and from the external devices. These two ports implement the following features:

- Function is compatible to standard mode of I2C bus with the baud rate up to 400KHz.
- Each port consists of a pair of SCL and SDA which can be assigned to port 2 or port 6 by software
- Each port supports two recognizable slave addresses.
- P2.4~P2.7 have internal pull-ups; P6.4~P6.7 are open drain type.
- Provide two individual interrupt sources.
- Produce interrupt request when status is changed.
- Provide time-out mechanism to protect bus hang up.

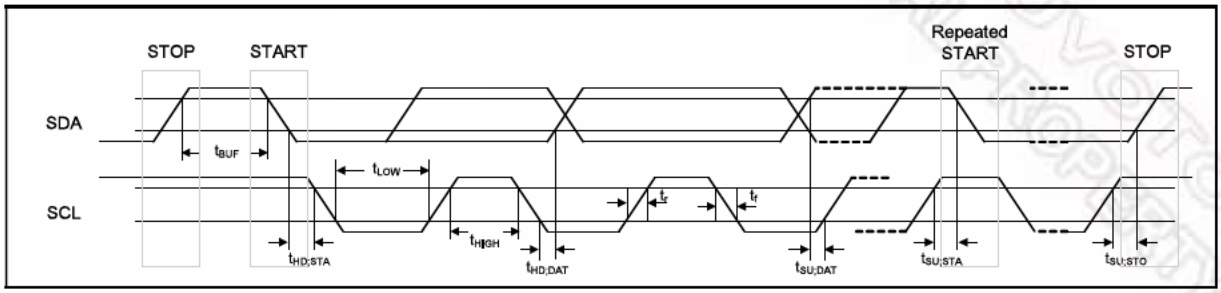


Figure 15-1 I2C Bus Timing

The I2C logic handles bytes transfer autonomously. It also keeps track of serial transfers, and a status register (I2STATUSx) reflects the status of the I2C bus.

The I2C port 1, SCL1 and SDA1 share the pair of P2.4 and P2.5 or the pair of P6.4 and P6.5 that is controlled by PSEL1 located at bit 0 of I2CON. Similarly, the I2C port 2, SCL2 and SDA2 share the pair of P2.6 and P2.7 or the pair of P6.6 and P6.7 that is controlled by PSEL2 located at bit 0 of I2CON2. When the I/O pins are used as I2C port, user must set the corresponding pins to logic high in advance.

When I2C port is enabled by setting ENSx to high, the internal states will be controlled by I2CONx and I2C logic hardware. Once a new status code is generated and stored in I2STATUSx the I2C interrupt flag (SI) will be set automatically, in the meanwhile, if EA and EI2Cx both are also in logic high, the I2C interrupt is requested. The 5 most significant bits of I2STATUSx stores the internal state code, the lowest 3 bits are always zero and the content remains until SI is cleared by software.

Since both I2C ports are similar, I2C port 1 is used to be the represent to explain I2C operation in following description.

15.1 The I2C Control Registers

Each I2C logic has 1 control register (I2CONx) to control the transmit/receive flow, 1 data register (I2DATx) to buffer the Tx/Rx data, 1 status register (I2STATUSx) to catch the state of Tx/Rx, 2 recognizable slave address registers for slave mode and 1 clock rate control block for master mode to generate the variable baud rate.

Table 15-1 Control Registers of I2C Ports

SYMBOL	DEFINITION	ADDRESS	MSB	BIT_ADDRESS, SYMBOL					LSB		RESET
I2TIMER2	I2C2 Timer Counter Register	FFH	-	-	-	-	-	ENTI2	DIV42	TIF2	0000 0000B
I2CLK2	I2C2 Clock Rate	FEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS2	I2C2 Status Register	FDH						-	-	-	0000 0000B
I2DAT2	I2C2 Data	FCH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR21	I2C2 Slave Address1	FBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR20	I2C2 Slave Address0	FAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON2	I2C2 Control Register	F9H	-	ENS2	STA	STO	SI	AA	-	PSEL2	x000 00x0B
I2TIMER	I2C1 Timer Counter Register	EFH	-	-	-	-	-	ENTI	DIV4	TIF	0000 0000B
I2CLK	I2C1 Clock Rate	EEH	I2CLK.7	I2CLK.6	I2CLK.5	I2CLK.4	I2CLK.3	I2CLK.2	I2CLK.1	I2CLK.0	0000 0000B
I2STATUS	I2C1 Status Register	EDH						-	-	-	0000 0000B
I2DAT	I2C1 Data	ECH	I2DAT.7	I2DAT.6	I2DAT.5	I2DAT.4	I2DAT.3	I2DAT.2	I2DAT.1	I2DAT.0	xxxx xxxxxB
I2ADDR11	I2C1 Slave Address1	EBH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	-	xxxx xxxxxB
I2ADDR10	I2C1 Slave Address0	EAH	ADDR.7	ADDR.6	ADDR.5	ADDR.4	ADDR.3	ADDR.2	ADDR.1	GC	xxxx xxxx0B
I2CON	I2C1 Control Register	E9H	-	ENS1	STA	STO	SI	AA	-	PSEL1	x000 00x0B

15.1.1 Slave Address Registers, I2ADDRxx

Each I2C port is equipped with two slave address registers. The contents of the register are irrelevant when I2C is in master mode. In the slave mode, the seven most significant bits must be loaded with the MCU's own slave address. The I2C hardware will react if the contents of I2ADDRxx are matched with the received slave address.

The I2C ports support the "General Call" function. If the GC bit is set the I2C port1 hardware will respond to General Call address (00H). Clear GC bit to disable general call function.

15.1.2 Data Register, I2DAT

This register contains a byte of serial data to be transmitted or a byte which has just been received. The CPU can read from or write to this 8-bit directly addressable SFR while it is not in the process of shifting a byte. Data in I2DAT remains stable as long as SI is set. The MSB is shifted out first. While data is being shifted out, data on the bus is simultaneously being shifted in; I2DAT always contains the last data byte present on the bus.

I2DAT and the acknowledge bit form a 9-bit shift register which shifts in or out an 8-bit byte, followed by an acknowledge bit. The acknowledge bit is controlled by the hardware and cannot be accessed by the CPU. Serial data is shifted into I2DAT on the rising edges of serial clock pulses on the SCL line. When a byte has been shifted into I2DAT, the serial data is available in I2DAT, and the acknowledge

bit (ACK or NACK) is returned by the control logic during the ninth clock pulse. Serial data is shifted out from I2DAT on the falling edges of SCL clock pulses.

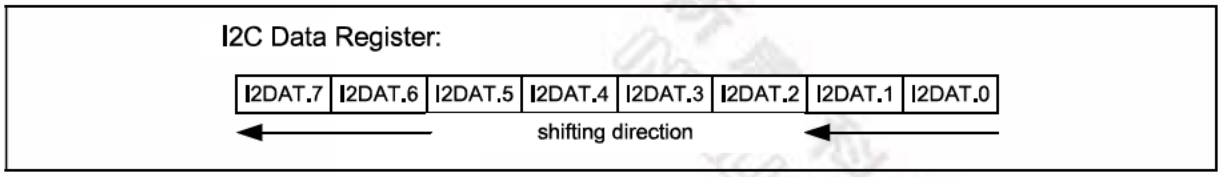


Figure 15-2 I2C Data Shift

15.1.3 Control Register, I2CONx

Two bits are affected by hardware: the SI bit is set when the I2C hardware requests a serial interrupt, and the STO bit is cleared when a STOP condition is present on the bus. The STO bit is also cleared when ENS1 = "0".

I2C Control Register Channel 1

Bit:	7	6	5	4	3	2	1	0
	-	ENS1	STA	STO	SI	AA	-	PSEL1

ENS1 Enable channel 1 of I2C serial function block. When ENS1=1 the channel 1 of I2C serial function enables. The port latches of SDA1 and SCL1 must be set to logic high.

STA I2C START Flag. Setting STA to logic 1 to enter master mode, the I2C hardware sends a START or repeat START condition to bus when the bus is free.

STO I2C STOP Flag. In master mode, setting STO to transmit a STOP condition to bus then I2C hardware checks the bus condition, if a STOP condition is detected this flag will be cleared by hardware automatically. In a slave mode, setting STO resets I2C hardware to the defined “not addressed” slave mode.

SI I2C Port 1 Interrupt Flag. When a new SIO1 state is present in the S1STA register, the SI flag is set by hardware, and if the EA and EI2C1 bits are both set, the I2C1 interrupt is requested. SI must be cleared by software.

AA Assert Acknowledge Flag. If AA is set to logic 1, an acknowledged signal (low level to SDA) will be returned during the acknowledge clock pulse on the SCL line. If AA is cleared, a non-acknowledged signal (high level to SDA) will be returned during the acknowledge clock pulse on the SCL line.

PSEL1 I2C Port1 Select bit. I2C port1 pair of SCL1 and SDA1, can be configured to pair of P2.4 and P2.5 if PSEL1=0 or to pair of P6.4 and P6.5 if PSEL1=1. The default value of bit PSEL1 is logic 0. Note that pin from P6.4 to P6.7 are open drain type.

15.1.4 Status Register, I2STATUSx

I2STATUSx is an 8-bit read-only register. The five most significant bits contain the status code. The three least significant bits are always 0. There are 23 possible status codes. When I2STATUSx contains F8H, no serial interrupt is requested. All other I2STATUSx values correspond to defined I2C ports states. When each of these states is entered, a status interrupt is requested (SI = 1). A valid status code is present in I2STATUSx one machine cycle after SI is set by hardware and is still present one machine cycle after SI has been reset by software.

In addition, state 00H stands for a Bus Error. A Bus Error occurs when a START or STOP condition is present at an illegal position in the format frame. Examples of illegal positions are during the serial transfer of an address byte, a data byte or an acknowledge bit.

15.1.5 I2C Clock Baud Rate Control, I2CLKx

The data baud rate of I2C is determined by I2CLKx register when I2C port is in a master mode. In the slave modes, SIO1 will automatically synchronize with any clock frequency up to 400 KHz from master I2C device.

The data baud rate of I2C setting conforms to the following equation.

Data Baud Rate of I2C = F_{CPU} / (I2CLKx + 1), where $F_{CPU} = F_{OSC}/4$.

For example, if F_{OSC}=16MHz (F_{CPU}=4MHz), the I2CLK=40(28H), the baud rate =4MHz/(40+1) = 97.56K bits/sec.

15.1.6 I2C Time-out Counter, I2Timerx

In W79E658, the I2C logic block provides a 14-bit timer-out counter that helps user to deal with bus pending problem. When SI is cleared user can set ENTI=1 to start the time-out counter. If I2C bus hangs up too long to get any valid signal from devices on the bus, the time-out counter overflows cause TIF=1 to request an I2C interrupt. The I2C interrupt is requested in the condition of either SI=1 or TIF=1. Flags SI and TIF must be cleared by software.

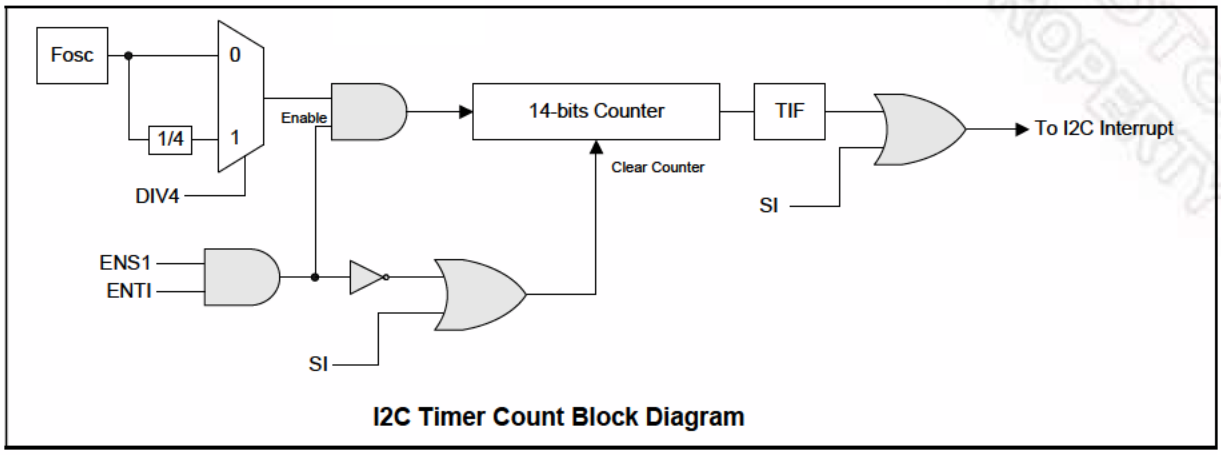


Figure 15-3 I2C Time-out Counter

15.2 Modes of Operation

The on-chip I2C ports support four operation modes, Master transmitter, Master receiver, Slave transmitter and Slave receiver.

In a given application, I2C port may operate as a master and as a slave. In the slave mode, the I2C port hardware looks for its own slave address and the general call address. If one of these addresses is detected, an interrupt is requested. When the microcontroller wishes to become the bus master, the hardware waits until the bus is free before the master mode is entered so that a possible slave action is not interrupted. If bus arbitration is lost in the master mode, I2C port switches to the slave mode immediately and can detect its own slave address in the same serial transfer.

15.2.1 Master Transmitter Mode

Serial data output through SDAx while SCLx outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the data direction bit. In this case the data direction bit (R/W) will be logic 0, and we say that a “W” is transmitted. Thus the first byte transmitted is SLA+W. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

15.2.2 Master Receiver Mode

In this case the data direction bit (R/W) will be logic 1, and we say that an "R" is transmitted. Thus the first byte transmitted is SLA+R. Serial data is received via SDAx while SCLx outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are output to indicate the beginning and end of a serial transfer.

15.2.3 Slave Receiver Mode

Serial data and the serial clock are received through SDAx and SCLx. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.

15.2.4 Slave Transmitter Mode

The first byte is received and handled as in the slave receiver mode. However, in this mode, the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted via SDAx while the serial clock is input through SCLx. START and STOP conditions are recognized as the beginning and end of a serial transfer.

15.3 Data Transfer Flow in Four Operating Modes

The four operating modes are: Master/Transmitter, Master/Receiver, Slave/Transmitter and Slave/Receiver. Bits STA, STO and AA in I2CONx decide the next action the I2C port hardware will take after SI is cleared. When the next action is completed, a new status code in I2STATUSx will be updated and SI will be set by hardware in the same time. Now, the interrupt service routine is entered (if the I2C interrupt is enabled), the new status code can be used to decide which appropriate service routine the software is to branch. Data transfers in each mode are shown in the following figures.

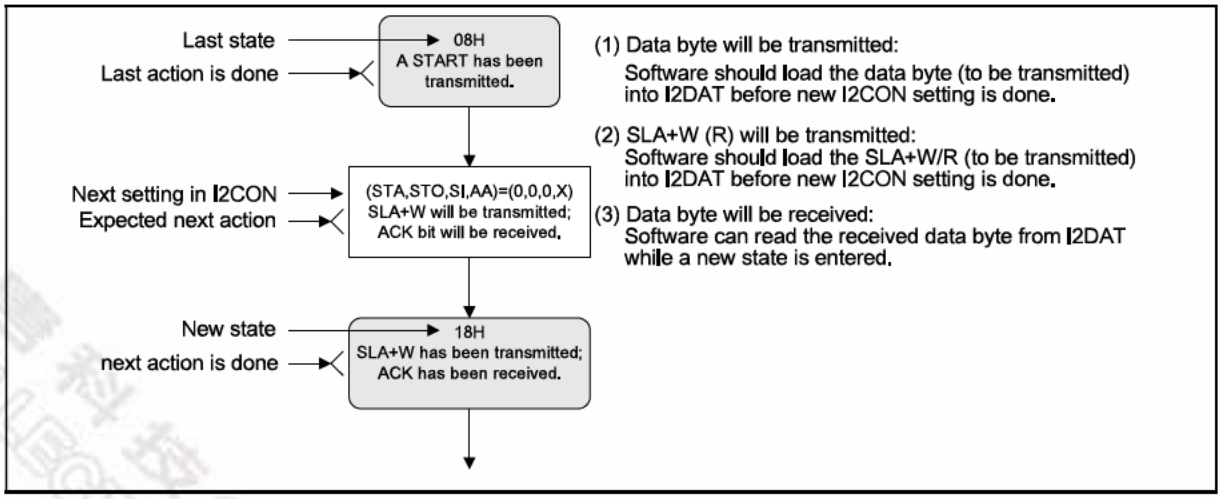


Figure 15-4 Legend for the following four figures

15.3.1 Master/Transmitter Mode

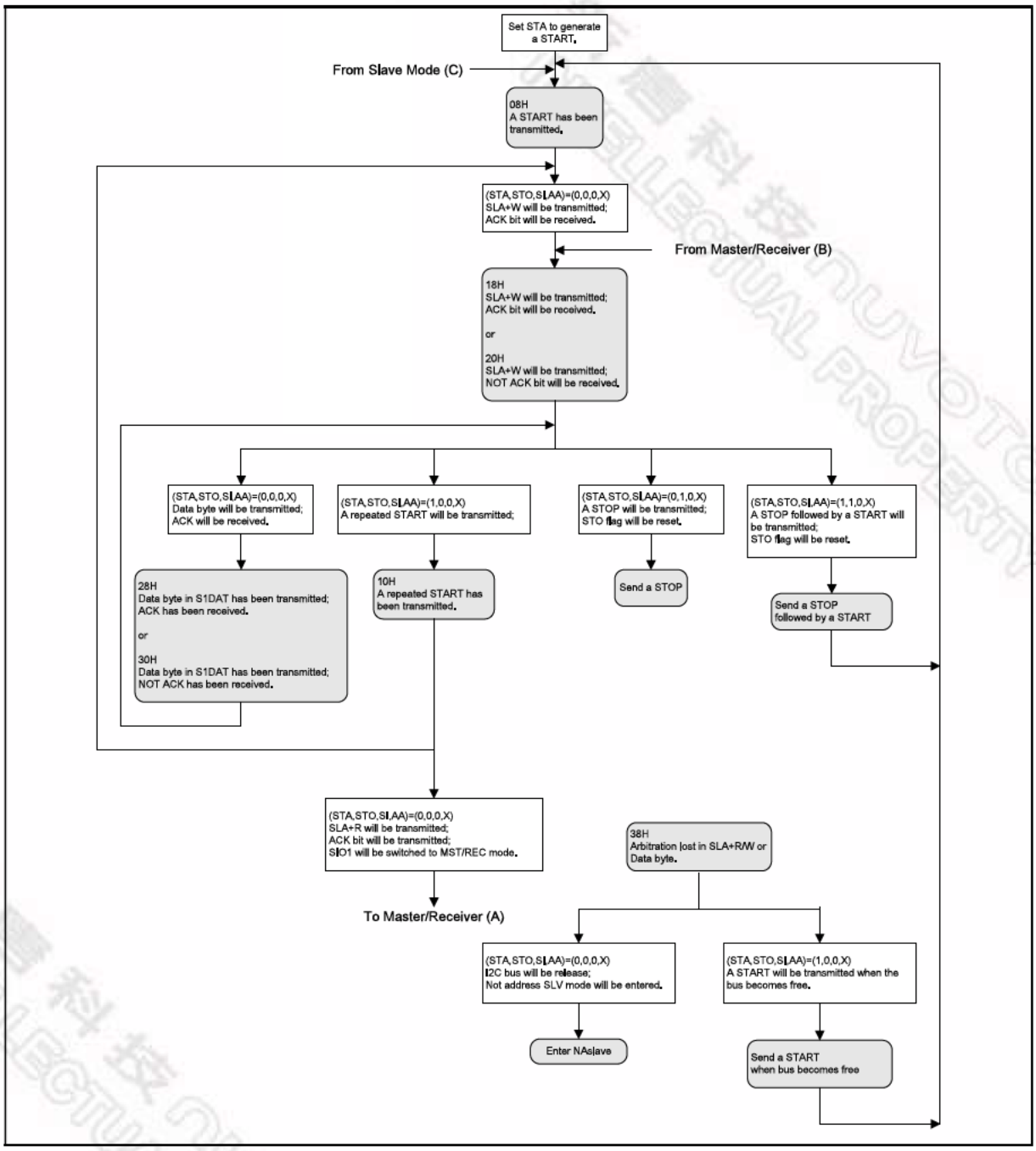


Figure 15-5 Master Transmitter Mode

15.3.2 Master/Receiver Mode

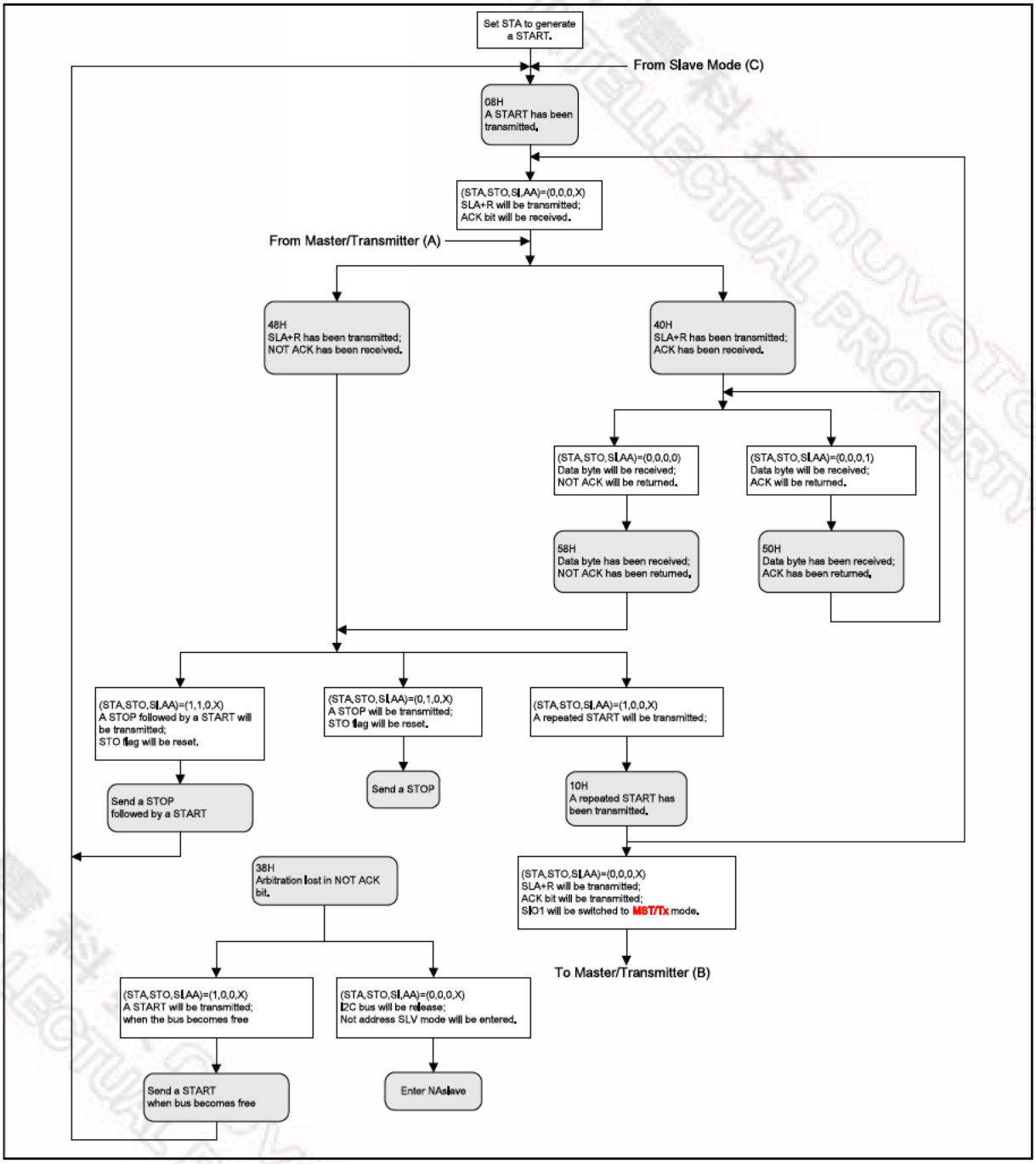


Figure 15-6 Master Receiver Mode

15.3.3 Slave/Transmitter Mode

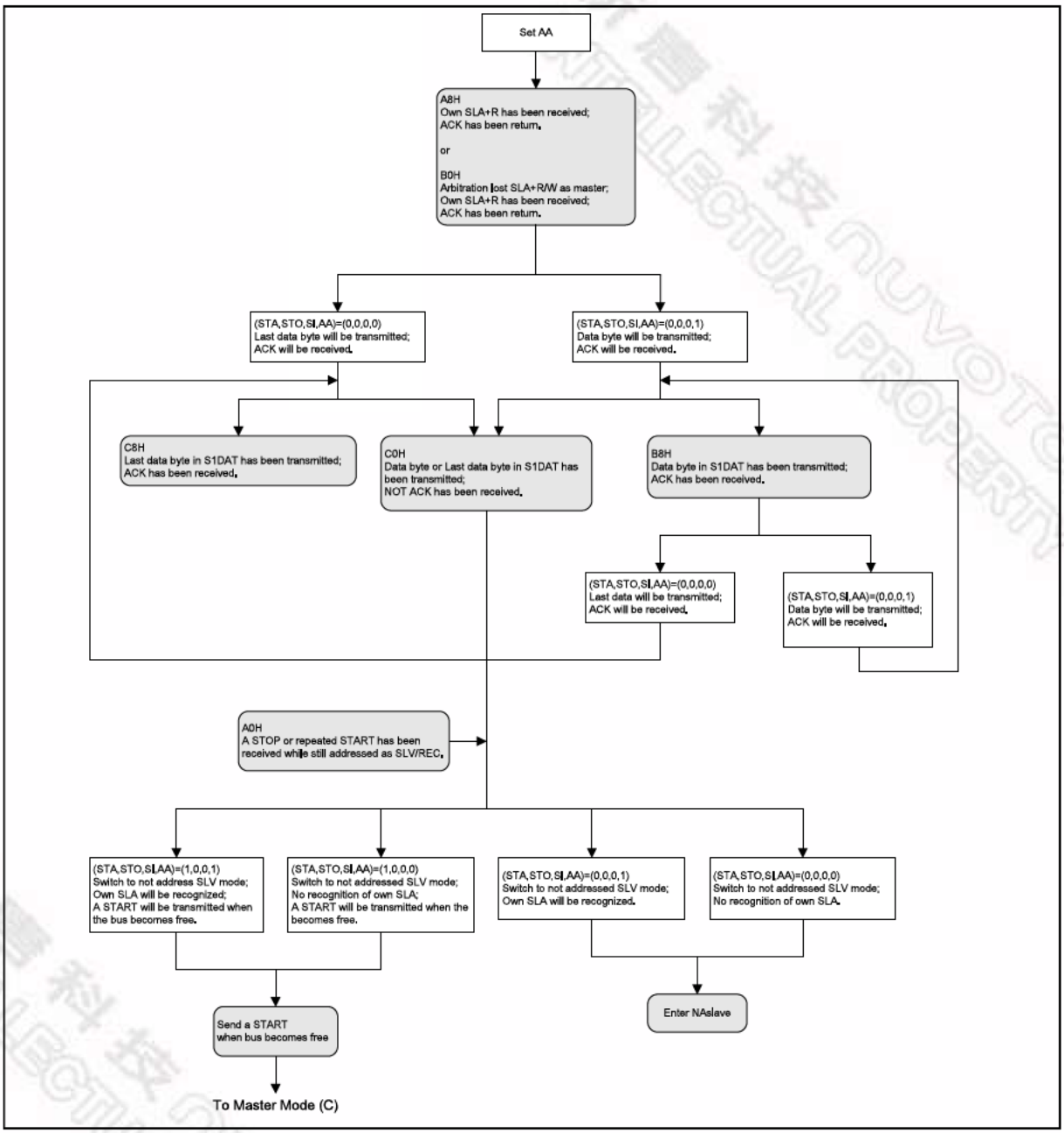


Figure 15-7 Slave Transmitter Mode

15.3.4 Slave/Receiver Mode

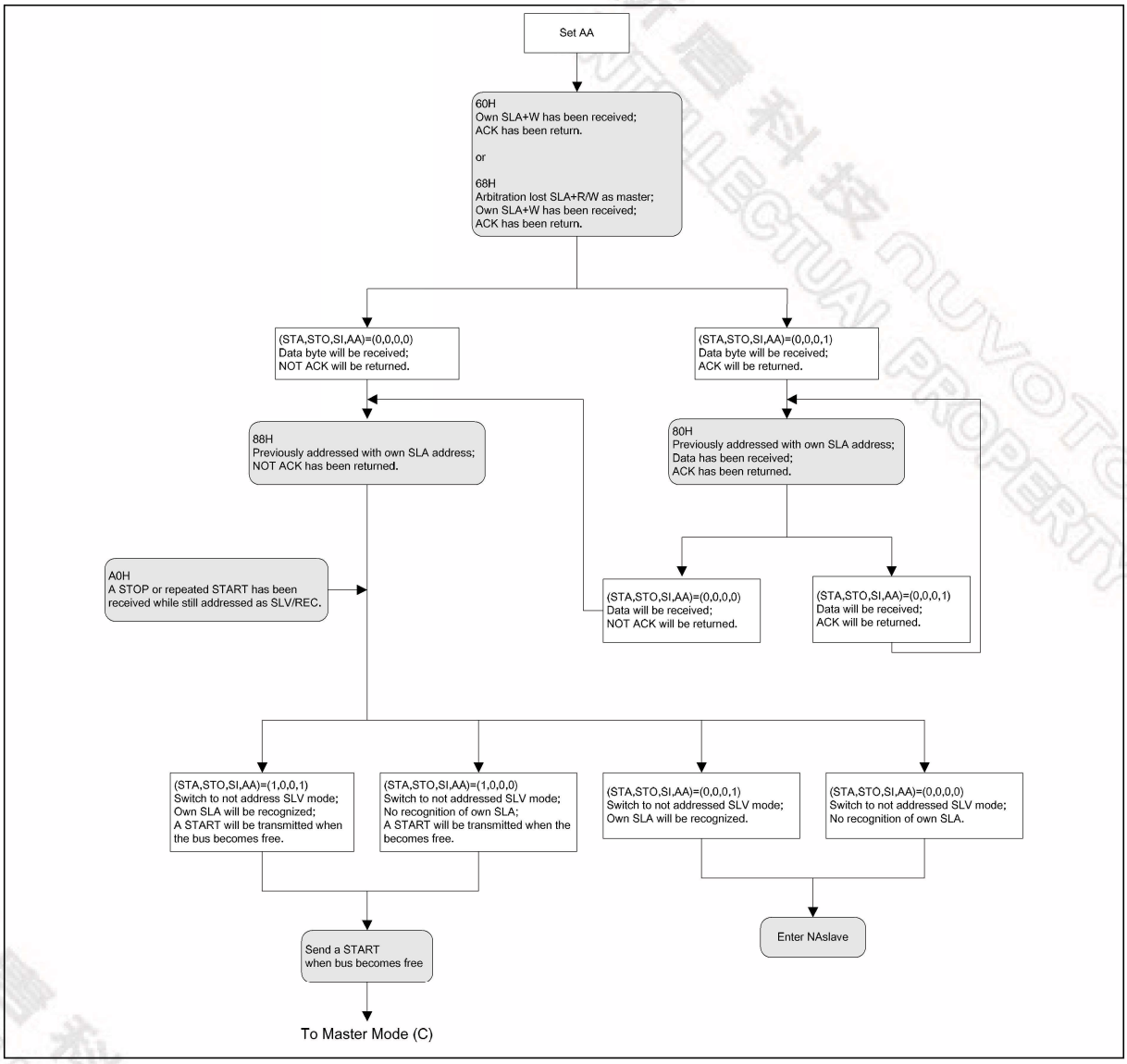


Figure 15-8 Slave Receiver Mode

15.3.5 GC Mode

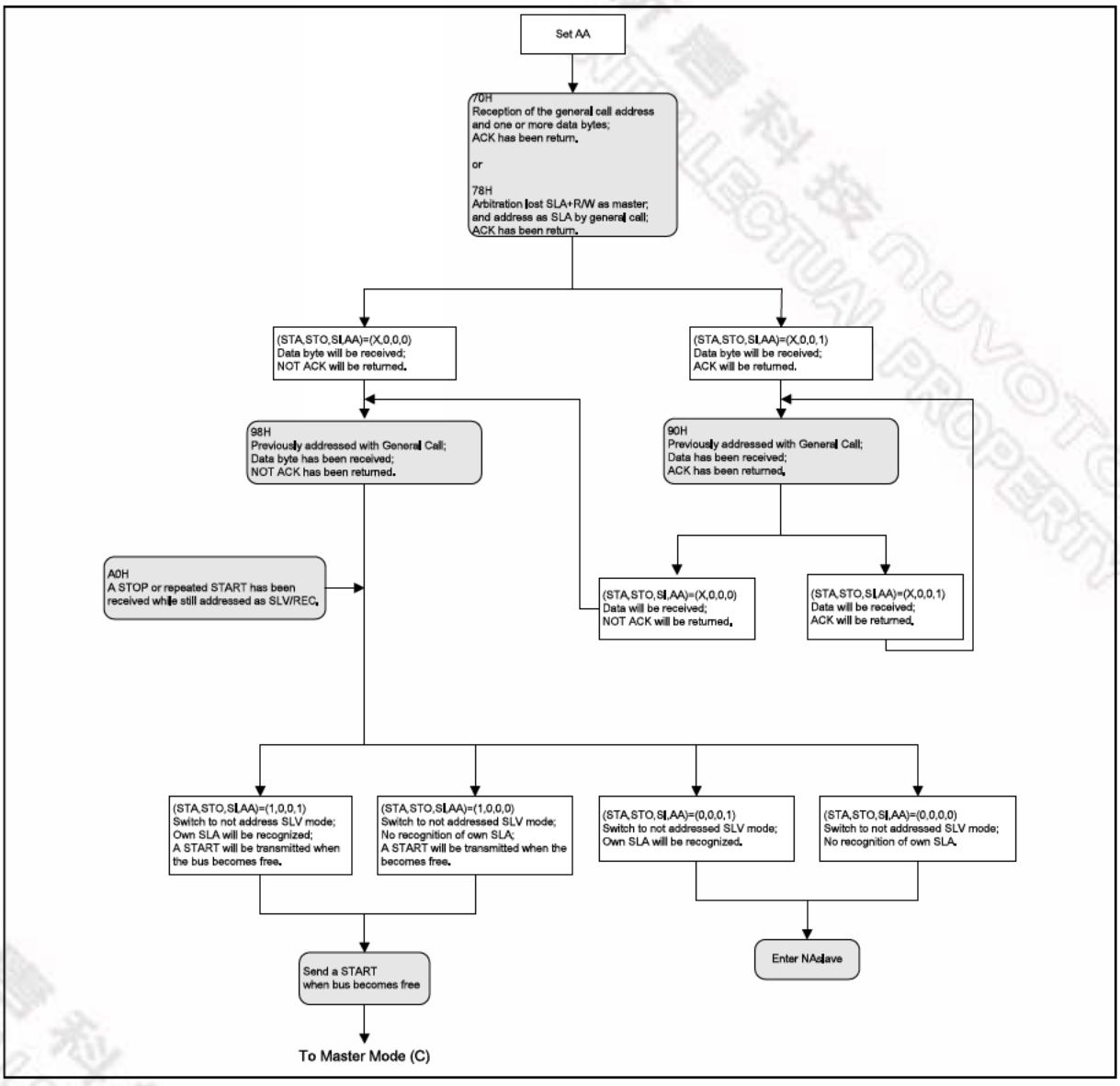


Figure 15-9 General Call Address

16. Analog-To-Digital Converter

The ADC contains a digital-to-analog converter (DAC) that converts the contents of a successive approximation register to a voltage (V_{DAC}), which is compared to the analog input voltage (Vin). The output of the comparator is then fed back to the successive approximation control logic that controls the successive approximation register. This is illustrated in the figure below.

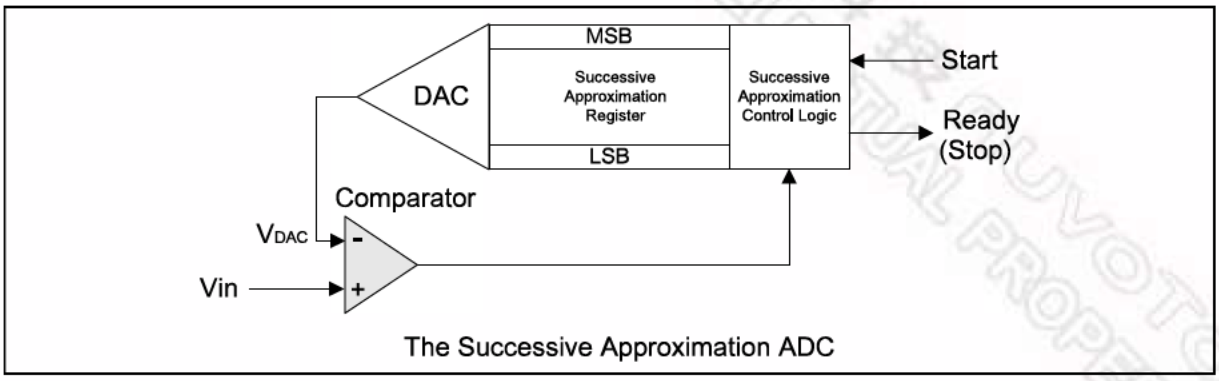


Figure 16-1 Successive Approximation ADC

16.1 Operation of ADC

The ADC circuit is enabled by ADCCEN. Control bits ADCCON.0, ADCCON.1 and ADCCON.2 are connected to an analog multiplexer that selects one of eight analog channels to convert (Vin). A conversion is initiated by setting the ADCS bit (ADDCON.3). The ADCS bit can be set by either hardware (P1.2) or software, according to the ADEX bit (ADCCON.5). If ADEX is 0, only the software can set ADCS. If ADEX is 1, the software can set ADCS, or it can be set by applying a rising edge to external pin STADC. The rising edge must consist of a low level on STADC for at least one machine cycle followed by a high level signal on STADC for at least one machine cycle, to make sure the W79E658 detects both parts of the transition. The low-to-high transition on STADC is then recognized at the end of a machine cycle, and the conversion commences at the beginning of the next cycle.

The conversion takes 50 machine cycles, and the end of the conversion is flagged by ADCI (ADCCON.4). The result is a 10-bit value: the upper eight bits are stored in register ADCH, and the two LSB are stored in ADCCON, bits 7 and 6. The program may ignore the two LSB in ADCCON and use the 8-bit value in ADCH instead.

Once an ADC conversion is in progress, another ADC start (by the hardware or software) has no effect on it, but a conversion in progress is aborted if the W79E658 enters power-down mode. The result of a completed conversion (once ADCI is set to 1) is unaffected in this case, however.

W79E658 supports 8 analog input ports which share the I/O pins from P1.4 to P1.7 and from P5.0 to P5.3. The bits ADCCH[7:0] in register ADCPS control the mode of the above 8 I/O pins to work as in digital I/O mode(default) or analog input mode.

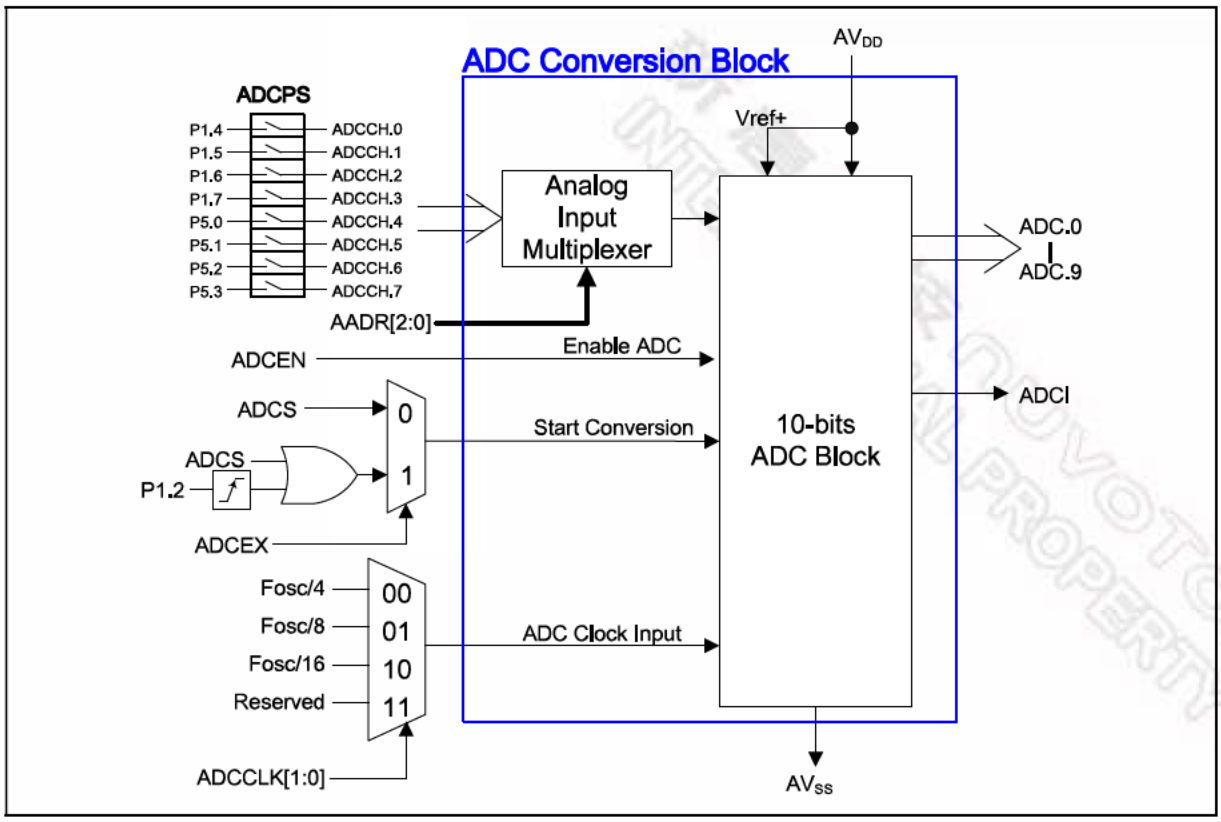


Figure 16-2 ADC Block Diagram

16.2 ADC Resolution and Analog Supply

The ADC circuit has its own supply pins AV_{DD} and AV_{SS}, which are connected to each end of the DAC's resistance-ladder. The ladder has 1023 equally-spaced taps, separated by a resistance of "R". The first tap is located 0.5 x R above AVss, and the last tap is located 0.5 x R below AV_{DD}, giving a total ladder resistance of 1024 x R. This structure ensures that the DAC is monotonic and results in a symmetrical quantization error.

For input voltages between AV_{SS} and [(AV_{SS}) + ½ LSB], the 10-bit result of an A/D conversion will be 0000000000B = 000H. For input voltages between [(AV_{DD}) – 3/2 LSB] and AV_{DD}, the result of a conversion will be 1111111111B = 3FFH. The input voltage (Vin) should be between AV_{DD} and AV_{SS}.

The result can always be calculated from the following formula:

$$\text{Result} = 1024 \times \frac{V_{in}}{AV_{DD}}$$

16.3 ADC Control Registers

ADC Control Register

Bit:	7	6	5	4	3	2	1	0
	ADCEN	-	ADCEX	ADCI	ADCS	AADR2	AADR1	AADR0

Mnemonic: ADCCON Address: C0h

ADCEN Enable A/D Converter Function. Set ADCEN to logic high to enable ADC block.

ADCEX Enable external start control of ADC conversion by a rising edge from P1.2. ADCEX=0: Disable external start. ADCEX=1: Enable external start control.

ADCI A/D Converting Complete/Interrupt Flag. This flag is set when ADC conversion is completed and will cause a hardware interrupt if ADC interrupt is enabled. It is cleared by software only.

ADCS A/D Converting Start. Setting this bit by software starts the conversion of the selected ADC input. ADCS remains high while ADC is converting signal and will be automatically cleared by hardware when ADC conversion is completed.

AADR[2:0] Select and enable analog input channel from ADC0 to ADC7.

AADR[2:0]	ADC SELECTED INPUT	AADR[2:0]	ADC SELECTED INPUT
000	ADCCH0 (P1.4)	100	ADCCH4 (P5.0)
001	ADCCH1 (P1.5)	101	ADCCH5 (P5.1)
010	ADCCH2 (P1.6)	110	ADCCH6 (P5.2)
011	ADCCH3 (P1.7)	111	ADCCH7 (P5.3)

The ADCI and ADCS control the ADC conversion as below:

ADCI	ADCS	ADC STATUS
0	0	ADC not busy; A conversion can be started.
0	1	ADC busy; Start of a new conversion is blocked.
1	0	Conversion completed; Start of a new conversion requires ADCI = 0.
1	1	This is an internal temporary state that user can ignore it.

ADC Converter Result Low Register

Bit:	7	6	5	4	3	2	1	0
	ADCLK1	ADCLK0	-	-	-	-	ADC.1	ADC.0

Mnemonic: ADCL Address: C1h

ADCLK[1:0] ADC Clock Frequency Select. The 10-bit ADC needs a clock to drive the converting that the clock frequency may not over 4MHz. ADCLK[1:0] controls the frequency of the clock to ADC block as below table.

ADCLK1	ADCLK0	ADC CLOCK FREQUENCY
0	0	Crystal clock / 4 (Default)
0	1	Crystal clock / 8
1	0	Crystal clock / 16
1	1	Reserved

ADC[1:0] 2 LSB of 10-bit A/D conversion result. The 2 bits are read only.

ADC Converter Result High Register

Bit:	7	6	5	4	3	2	1	0
	ADC.9	ADC.8	ADC.7	ADC.6	ADC.5	ADC.4	ADC.3	ADC.2

Mnemonic: ADCH Address: C2h

ADC[9:2] 8 MSB of 10-bit A/D conversion result. ADCH is a read only register.

ADC Pin Switch

Bit:	7	6	5	4	3	2	1	0
	ADCPS.7	ADCPS.6	ADCPS.5	ADCPS.4	ADCPS.3	ADCPS.2	ADCPS.1	ADCPS.0

Mnemonic: ADCPS Address: C6h

BIT	NAME	FUNCTION
7-0	ADCPS.7-0	Switch I/O pins P1.4~P1.7 and P5.0~P5.3 to analog inputs. Analog inputs, ADC0-ADC3 which share the I/O pins from P1.4 to P1.7 and ADC4-ADC7 which share the I/O pins from P5.0 to P5.3. 1: The corresponding I/O pin functions as analog input. 0: The corresponding I/O pin functions as digital I/O.

ADCPS.3-0: Switch P1.7~P1.4 to analog input function

BIT	CORRESPONDING PIN	BIT	CORRESPONDING PIN
ADCPS.0	P1.4	ADCPS.4	P5.0
ADCPS.1	P1.5	ADCPS.5	P5.1
ADCPS.2	P1.6	ADCPS.6	P5.2
ADCPS.3	P1.7	ADCPS.7	P5.3

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17. Timed Access Protection

The W79E658 has features like the Watchdog Timer, wait-state control signal and power-on/fail reset flag that are crucial to the proper operation of the system. If these features are unprotected, errant code may write critical control bits, resulting in incorrect operation and loss of control. To prevent this, the W79E658 provides has a timed-access protection scheme that controls write access to critical bits.

In this scheme, protected bits have a timed write-enable window. A write is successful only if this window is active; otherwise, the write is discarded. The write-enable window is opened in two steps. First, the software writes AAh to the Timed Access (TA) register. This starts a counter, which expires in three machine cycles. Then, if the software writes 55h to the TA register before the counter expires, the write-enable window is opened for three machine cycles. After three machine cycles, the window automatically closes, and the procedure must be repeated again to access protected bits.

The suggested code for opening the write-enable window is

```
TA      REG   0C7h          ; Define new register TA, located at 0C7h
        MOV   TA, #0AAh
        MOV   TA, #055h
```

Five examples, some correct and some incorrect, of using timed-access protection are shown below.

Example 1: Valid access

```
        MOV   TA, #0AAh          3 M/C   ; Note: M/C = Machine Cycles
        MOV   TA, #055h          3 M/C
        MOV   WDCON, #00h        3 M/C
```

Example 2: Valid access

```
        MOV   TA, #0AAh          3 M/C
        MOV   TA, #055h          3 M/C
        NOP                      1 M/C
        SETB  EWT                2 M/C
```

Example 3: Valid access

```
MOV     TA, #0Aah          3 M/C
MOV     TA, #055h          3 M/C
        ORL   WDCON, #00000010B  3M/C
```

Example 4: Invalid access

```
        MOV   TA, #0AAh          3 M/C
        MOV   TA, #055h          3 M/C
        NOP                      1 M/C
        NOP                      1 M/C
        CLR   POR                2 M/C
```

Example 5: Invalid Access

```
MOV   TA, #0AAh      3 M/C
NOP                  1 M/C
MOV   TA, #055h      3 M/C
SETB  EWT            2 M/C
```

In the first three examples, the protected bits are written before the window closes. In Example 4, however, the write occurs after the window has closed, so there is no change in the protected bit. In Example 5, the second write to TA occurs four machine cycles after the first write, so the timed access window in not opened at all, and the write to the protected bit fails.

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18. Port 4 Structure

Port 4 is a multi-function port that performs general purpose I/O port and chip-select strobe signals including read strobe, write strobe and read/write strobe signals. The 4 alternate modes are selected by P4xM1 and P4xM0. The function of chip-select strobe output provides that user can activate external devices by access to some specific address region.

Port 4 Control Register A

Bit:	7	6	5	4	3	2	1	0
	P41M1	P41M0	P41C1	P41C0	P40M1	P40M0	P40C1	P40C0

Mnemonic: P4CONA Address: 92h

Port 4 Control Register B

Bit:	7	6	5	4	3	2	1	0
	P43M1	P43M0	P43C1	P43C0	P42M1	P42M0	P42C1	P42C0

Mnemonic: P4CONB Address: 93h

BIT NAME	FUNCTION
P4xM1, P4xM0	Port 4 alternate modes. =00: Mode 0. P4.x is a general purpose I/O port which is the same as Port 1. =01: Mode 1. P4.x is a Read Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =10: Mode 2. P4.x is a Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0. =11: Mode 3. P4.x is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P4xAH, P4xAL and bits P4xC1, P4xC0
P4xC1, P4xC0	Port 4 Chip-select Mode address comparison: =00: Compare the full address (16 bits length) with the base address registers P4xAH and P4xAL. =01: Compare the 15 high bits (A15-A1) of address bus with the base address registers P4xAH and P4xAL. =10: Compare the 14 high bits (A15-A2) of address bus with the base address registers P4xAH and P4xAL. =11: Compare the 8 high bits (A15-A8) of address bus with the base address registers P4xAH and P4xAL.

P40AH, P40AL:

The Base address register for comparator of P4.0. P40AH contains the high-order byte of address, P40AL contains the low-order byte of address.

P41AH,P41AL:

The Base address register for comparator of P4.1. P41AH contains the high-order byte of address, P41AL contains the low-order byte of address.

P42AH, P42AL:

The Base address register for comparator of P4.2. P42AH contains the high-order byte of address, P42AL contains the low-order byte of address.

P43AH, P43AL:

The Base address register for comparator of P4.3. P43AH contains the high-order byte of address, P43AL contains the low-order byte of address.

PORT 4

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	P4.3	P4.2	P4.1	P4.0

Mnemonic: P4 Address: A5h

P4.3-0 Port 4 is a bi-directional I/O port with internal pull-ups.

Port 4 Chip-select Polarity

Bit:	7	6	5	4	3	2	1	0
	P43INV	P42INV	P42INV	P40INV	-	PWDNH	RMWFP	-

Mnemonic: P4CSIN Address: A2h

P4xINV The active polarity of P4.x when it is set as a chip-select strobe output. High = Active High. Low = Active Low.

PWDNH Set PWDNH to logic 1 then ALE and PSEN will keep high state, clear this bit to logic 0 then ALE and PSEN will output low during power down mode.

RMWFP Control Read Path of Instruction “Read-Modify-Write”. When this bit is set, the read path of executing “read-modify-write” instruction is from port pin otherwise from SFR.

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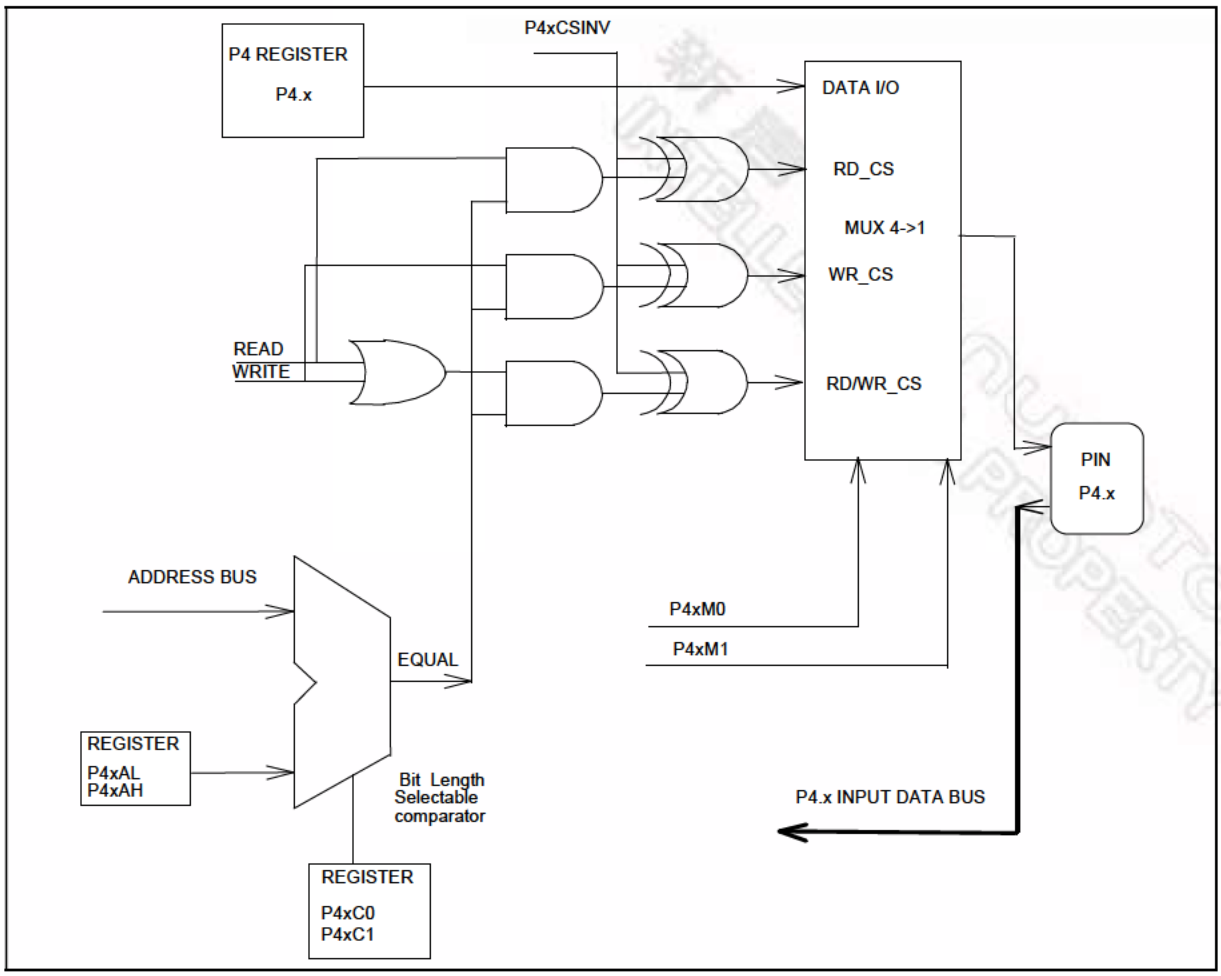


Figure 18-1 Port 4 Structure Diagram

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H ~1237H and positive polarity, and P4.1 ~ P4.3 are used as general I/O ports.

```
MOV    P40AH,#12H
MOV    P40AL,#34H          ;Define the base I/O address 1234H for P4.0 as an special function
MOV    P4CONA,#00001010B   ;Define the P4.0 as a write strobe signal pin and the compared address is [A15:A2]
MOV    P4CONB,#00H         ;P4.1~P4.3 as general I/O port which are the same as PORT1
MOV    P4CSIN,#10H         ;Write the P40CSINV =1 to inverse the P4.0 write strobe polarity
```

Then any instruction writes data to address from 1234H to 1237H, for example MOVX @DPTR,A (with DPTR=1234H~1237H), will generate the positive polarity write strobe signal at pin P4.0 . And the instruction of "MOV P4,#XX" will output the bit3 to bit1 of data #XX to pin P4.3~ P4.1.

19. H/W Reboot Mode (Boot From 4k Bytes Of LDFLASH)

The W79E658 boots from APFlash program by default at the external reset. On some occasions, for example to re-program APFlash in system, user can force W79E658 to boot from the LDFlash program (4K bytes) at the external reset. Pull both P2.7 and P2.6 or P4.3 which are controlled by option bit4 and bit5 to logic low at the external reset state will force W79E658 to reboot from LDFlash ROM. The setting is shown as below. It is necessary to add 10K pull-high resistors on P2.6, P2.7 and P4.3 pins.

Table 19-1 Reboot Mode

OPTION BITS	RST	P4.3	P2.7	P2.6	MODE
Bit4 L	H ↓	X	L	L	REBOOT
Bit5 L	H ↓	L	X	X	REBOOT

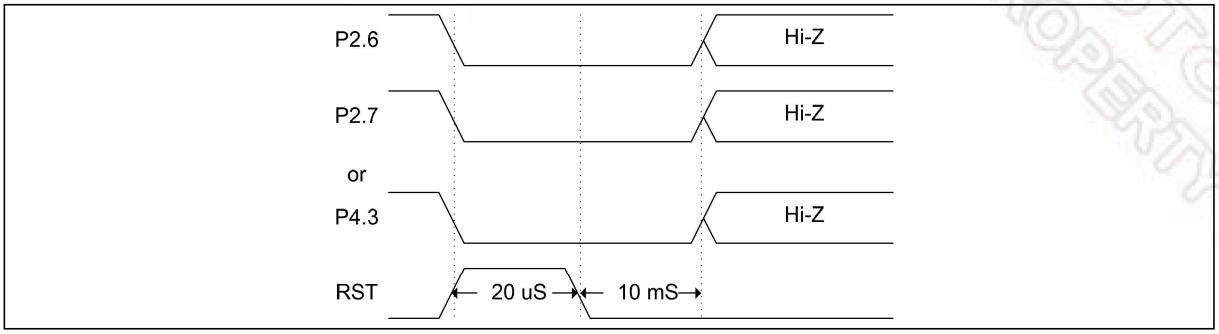


Figure 19-1 Timing of Entering Re-Boot Mode

Notes:

1. The possible situation that user need to enter REBOOT mode is when the APFlash program can not run normally and W79E658 can not jump to LDFlash to execute on chip programming function. Then user can use this REBOOT mode to force the CPU to jump to LDFlash and run on chip programming procedure. On the system board, user can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, user can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APFlash program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W79E658 to enter the REBOOT mode. After power on of personal computer, user can release both PLAY and EJECT buttons and run the on chip programming procedure to re-program the application code to the APFlash. Then user can back to normal condition of CD ROM.
2. In application system design, user must take care the P4.3, P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W79E658 entering the programming mode or REBOOT mode in normal operation.

20. In-System Programming

20.1 The Loader Program Locates at LDFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #03H value before CPU has entered idle state. CPU will switch to LDFlash memory and execute a reset action. H/W reboot mode will switch to LDFlash memory, too. Set SFRCN register where it locates at user's loader program to update APFlash memory. Set a SWRESET (CHPCON.7) to switch back APFlash after CPU has updated APFlash program. CPU will restart to run program from reset state.

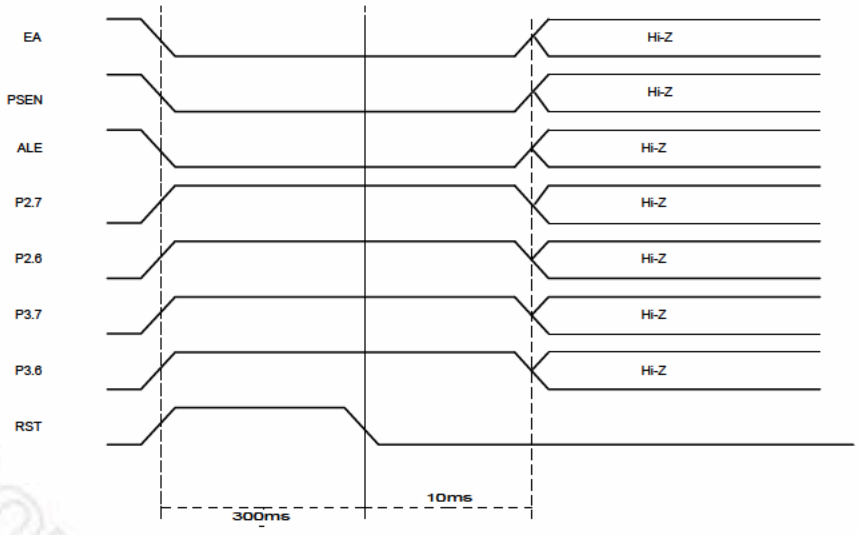
20.2 The Loader Program Locates at APFlash Memory

CPU is Free Run at APFlash memory. CHPCON register had been set #01H value before CPU has entered idle state. Set SFRCN register to update LDFlash. CPU will continue to run user's APFlash program after CPU has updated program. Please refer demonstrative code to understand other detail description.

21. H/W Writer Mode

This mode is for the writer to write / read Flash EPROM operation. A general user may not enter this mode.

The Timing For Entering Flash EPROM Mode on the Programmer



22. Security Bits

During the on-chip FLASH EPROM programming mode, the FLASH EPROM can be programmed and verified repeatedly. And the program code can be protected by setting security bits. The protection of FLASH EPROM and those operations on it are described below.

The W79E658 has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security bits can not be changed once they have been programmed from high to low. They can only be reset to the default value FFh through "Erase-All" operation. The contents of the Company ID and Device ID registers have been set in factory.

If user doesn't need ISP function, do not fill "FFh" code in LD Flash memory. The writer always writes both AP and LD flash in a completed program procedure.

Table 22-1 Security Bits

BIT	DESCRIPTION
B0	=0: Lock data out
B1	=0: MOVC Inhibited
B2	Reserved
B3	Reserved
B4	=1: Disable H/W reboot by P2.6 and P2.7 =0: Enable H/W reboot by P2.6 and P2.7
B5	=1: Disable H/W reboot by P4.3 =0: Enable H/W reboot by P4.3
B6	Reserved
B7	=1: Crystal > 24MHz =0: Crystal < 24MHz

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B0: Lock bit

This bit is used to protect the customer's program code in the W79E658. After the programmer finishes the programming and verifies sequence B0 can be cleared to logic 0 to protect code from reading by any access path. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

B1: MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

B4: H/W Reboot with P2.6 and P2.7

If this bit is set to logic 0, enable to reboot 4k LD Flash mode while RST =H, P2.6 = L and P2.7 = L state. CPU will start from LD Flash to update the user's program.

B5: H/W Reboot with P4.3

If this bit is set to logic 0, enable to reboot 4k LD Flash mode while RST =H and P4.3 = L state. CPU will start from LD Flash to update the user's program

B7: Select clock frequency.

If clock frequency is over 24MHz, then set this bit is H. If clock frequency is less than 24MHz, then clear this bit.

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23. Electrical Characteristics

23.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	RATING	UNIT
DC Power Supply	$V_{DD} - V_{SS}$	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_A	0	+70	°C
Storage Temperature	T_{st}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

23.2 DC Characteristics

($V_{DD} - V_{SS}$ = 5V ±10%, TA = 25°C, Fosc = 20 MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Operating Voltage	V_{DD}	4.5 3.0	5.5 4.5	V	For W79E658 version For W79L658 version
Operating Current	I_{DD}	-	30	mA	No load V_{DD} = RST = 5.5V
Idle Current	I_{IDLE}	-	24	mA	Idle mode V_{DD} = 5.5V
Power Down Current	I_{PWDN}	-	10	µA	Power-down mode V_{DD} = 5.5V
Input Current P0, P1, P2, P3,P4, P5, P6, P7	I_{IN1}	-50	+10	µA	V_{DD} = 5.5V V_{IN} = 0V or VDD
Input Current RST[*1]	I_{IN2}	-	100	µA	V_{DD} = 5.5V 0<V_{IN}<VDD
Input Leakage Current $\overline{EA}$	I_{LK}	-10	+10	µA	V_{DD} = 5.5V 0V<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P0, P1, P2, P3, P4, P5, P6, P7	I_{TL}[*4]	-500	-200	µA	V_{DD} = 5.5V V_{IN} = 2.0V
Input Low Voltage P0, P1, P2, P3, P4, P5, P6, P7, $\overline{EA}$	V_{IL1}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage RST[*1]	V_{IL2}	0	0.8	V	V_{DD} = 4.5V
Input Low Voltage XTAL1[*3]	V_{IL3}	0	0.8	V	V_{DD} = 4.5V
Input High Voltage P0, P1, P2, P3, P4, P5, P6, P7, $\overline{EA}$	V_{IH1}	2.4	V_{DD} +0.2	V	V_{DD} = 5.5V

Input High Voltage RST	V_{IH2}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V

DC Characteristics, continued

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Input High Voltage XTAL1[*3]	V_{IH3}	3.5	V_{DD} +0.2	V	V_{DD} = 5.5V
Sink current P1, P3, P4, P5, P6, P7	I_{sk1}	4	8	mA	V_{DD} =4.5V V_s = 0.45V
Sink current P0,P2, ALE, $\overline{PSEN}$	I_{sk2}	10	14	mA	V_{DD} =4.5V V_{OL} = 0.45V
Source current P1, P3, P4, P5, P6, P7	I_{sr1}	-180	-360	uA	V_{DD} =4.5V V_{OL} = 2.4V
Source current P0, P2, ALE, $\overline{PSEN}$	I_{sr2}	-10	-14	mA	V_{DD} =4.5V V_{OL} = 2.4V
Output Low Voltage P1, P3, P4, P5, P6, P7	V_{OL1}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +6 mA
Output Low Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OL2}	-	0.45	V	V_{DD} = 4.5V I_{OL} = +10 mA
Output High Voltage P1, P3, P4, P5, P6, P7	V_{OH1}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -180 μA
Output High Voltage P0, P2, ALE, $\overline{PSEN}$ [*2]	V_{OH2}	2.4	-	V	V_{DD} = 4.5V I_{OH} = -10mA

Notes:

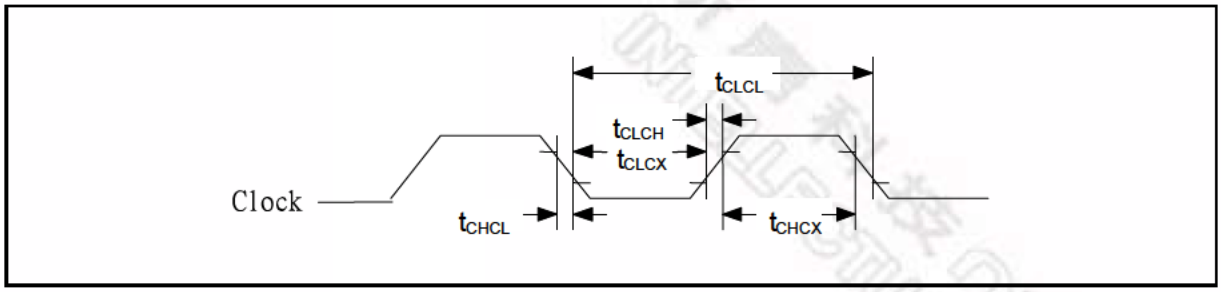
*1. RST pin is a Schmitt trigger input.

*2. P0, ALE and $\overline{PSEN}$ are tested in the external access mode.

*3. XTAL1 is a CMOS input.

*4. Pins of P0, P1, P2, P3, P4, P5, P6, P7 can source a transition current when they are being externally driven from 1 to 0. The transition
current reaches its maximum value when VIN approximates to 2V.

23.3 AC Characteristics



Note: Duty cycle is 50%.

23.3.1 External Clock Characteristics

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	12	-	-	nS	
Clock Low Time	t_{CLCX}	12	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

23.3.2 AC Specification

(V_{DD} – V_{SS} = 5V ±10%, TA = 25°C, Fosc = 20 MHz, unless otherwise specified.

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	40[1]	MHz
Oscillator Frequency	$1/t_{CLCL}$	0	33[2]	MHz
ALE Pulse Width	t_{LHLL}	$1.5t_{CLCL}$ - 5		nS
Address Valid to ALE Low	t_{AVLL}	$0.5t_{CLCL}$ - 5		nS
Address Hold After ALE Low	t_{LLAX1}	$0.5t_{CLCL}$ - 5		nS
Address Hold After ALE Low for MOVX Write	t_{LLAX2}	$0.5t_{CLCL}$ - 5		nS
ALE Low to Valid Instruction In	t_{LLIV}		$2.5t_{CLCL}$ - 20	nS
ALE Low to PSEN Low	t_{LLPL}	$0.5t_{CLCL}$ - 5		nS
$\overline{PSEN}$ Pulse Width	t_{PLPH}	$2.0t_{CLCL}$ - 5		nS
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}		$2.0t_{CLCL}$ - 20	nS
Input Instruction Hold After PSEN	t_{PXIX}	0		nS
Input Instruction Float After PSEN	t_{PXIZ}		t_{CLCL} - 5	nS
Port 0 Address to Valid Instr. In	t_{AVIV1}		$3.0t_{CLCL}$ - 20	nS

AC Specification, continued

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Port 2 Address to Valid Instr. In	t_{AVIV2}		$3.5t_{CLCL}$ - 20	nS
$\overline{PSEN}$ Low to Address Float	t_{PLAZ}	0		nS
Data Hold After Read	t_{RHDX}	0		nS
Data Float After Read	t_{RHDZ}		t_{CLCL} - 5	nS
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL}$ - 5	nS

Note: 1. CPU executes the program stored in the internal APFlash at V_{DD}=5.0V
2. CPU executes the program stored in the external memory at V_{DD}=5.0V

23.3.3 MOVX Characteristics Using Stretch Memory Cycle

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Data Access ALE Pulse Width	t_{LLHL2}	$1.5t_{CLCL}$ - 5 $2.0t_{CLCL}$ - 5		nS	t_{MCS} = 0 t_{MCS}>0
Address Hold After ALE Low for MOVX write	t_{LLAX2}	$0.5t_{CLCL}$ - 5		nS	
$\overline{RD}$ Pulse Width	t_{RLRH}	$2.0t_{CLCL}$ - 5 t_{MCS} - 10		nS	t_{MCS} = 0 t_{MCS}>0
$\overline{WR}$ Pulse Width	t_{WLWH}	$2.0t_{CLCL}$ - 5 t_{MCS} - 10		nS	t_{MCS} = 0 t_{MCS}>0
$\overline{RD}$ Low to Valid Data In	t_{RLDV}		$2.0t_{CLCL}$ - 20 t_{MCS} - 20	nS	t_{MCS} = 0 t_{MCS}>0
Data Hold after Read	t_{RHDX}	0		nS	
Data Float after Read	t_{RHDZ}		t_{CLCL} - 5 $2.0t_{CLCL}$ - 5	nS	t_{MCS} = 0 t_{MCS}>0
ALE Low to Valid Data In	t_{LLDV}		$2.5t_{CLCL}$ - 5 t_{MCS} + $2t_{CLCL}$ - 40	nS	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to Valid Data In	t_{AVDV1}		$3.0t_{CLCL}$ - 20 $2.0t_{CLCL}$ - 5	nS	t_{MCS} = 0 t_{MCS}>0
ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	t_{LLWL}	$0.5t_{CLCL}$ - 5 $1.5t_{CLCL}$ - 5	$0.5t_{CLCL}$ + 5 $1.5t_{CLCL}$ + 5	nS	t_{MCS} = 0 t_{MCS}>0
Port 0 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL}	t_{CLCL} - 5 $2.0t_{CLCL}$ - 5		nS	t_{MCS} = 0 t_{MCS}>0

MOVX Characteristics Using Stretch Memory Cycle, continued

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS	STRECH
Port 2 Address to $\overline{RD}$ or $\overline{WR}$ Low	t_{AVWL2}	$1.5t_{CLCL} - 5$ $2.5t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Valid to WR Transition	t_{QVWX}	-5 $1.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
Data Hold after Write	t_{WHQX}	$t_{CLCL} - 5$ $2.0t_{CLCL} - 5$		nS	$t_{MCS} = 0$ $t_{MCS}>0$
$\overline{RD}$ Low to Address Float	t_{RLAZ}		$0.5t_{CLCL} - 5$	nS	
$\overline{RD}$ or WR high to ALE high	t_{WHLH}	0 $1.0t_{CLCL} - 5$	10 $1.0t_{CLCL} + 5$	nS	$t_{MCS} = 0$ $t_{MCS}>0$

Note: t_{MCS} is a time period related to the Stretch memory cycle selection. The following table shows the time period of t_{MCS} for each selection of the Stretch value.

M2	M1	M0	MOVX CYCLES	T_{MCS}
0	0	0	2 machine cycles	0
0	0	1	3 machine cycles	4 t_{CLCL}
0	1	0	4 machine cycles	8 t_{CLCL}
0	1	1	5 machine cycles	12 t_{CLCL}
1	0	0	6 machine cycles	16 t_{CLCL}
1	0	1	7 machine cycles	20 t_{CLCL}
1	1	0	8 machine cycles	24 t_{CLCL}
1	1	1	9 machine cycles	28 t_{CLCL}

Explanation of Logics Symbols

In order to maintain compatibility with the original 8051 family, this device specifies the same parameter for each device, using the same symbols. The explanation of the symbols is as follows.

t	Time	A	Address
C	Clock	D	Input Data
H	Logic level high	L	Logic level low
I	Instruction	P	$\overline{PSEN}$
Q	Output Data	R	$\overline{RD}$ signal
V	Valid	W	$\overline{WR}$ signal
X	No longer a valid state	Z	Tri-state

23.4 The ADC Converter DC ELECTRICAL CHARACTERISTICS

(V_{DD}–V_{SS} = 3.0~5V±10%, T_A = -40~85°C, Fosc = 20MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION			TEST CONDITIONS
		MIN.	MAX.	UNIT	
Analog input	AVin	V_{SS}-0.2	V_{DD}+0.2	V	
ADC clock	ADCCLK	200KHz	5MHz	Hz	ADC circuit input clock
Conversion time	t_C	$52t_{ADC}$[1]		us	
Differential non-linearity	DNL	-1	+1	LSB	
Integral non-linearity	INL	-2	+2	LSB	Fosc=20MHz
		-5	+5	LSB	Fosc=40MHz
Offset error	Ofe	-1.5	+1.5	LSB	Fosc=20MHz
		-2.5	+2.5	LSB	Fosc=40MHz
Gain error	Ge	-1	+1	%	
Absolute voltage error	Ae	-5	+5	LSB	Fosc=20MHz
		-11	+11	LSB	Fosc=40MHz

Notes: 1. t_{ADC}: The period time of ADC input clock.

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I2C Bus Timing Characteristics

PARAMETER	SYMBOL	STANDARD MODE I2C BUS		UNIT
		MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	kHz
bus free time between a STOP and START condition	t_{BUF}	4.7	-	uS
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{Hd;STA}$	4.0	-	uS
Low period of the SCL clock	t_{LOW}	4.7	-	uS
HIGH period of the SCL clock	t_{HIGH}	4.0	-	uS
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	-	uS
Data hold time	$t_{HD;DAT}$	5.0	-	uS
Data set-up time	$t_{SU;DAT}$	250	-	nS
Rise time of both SDA and SCL signals	t_r	-	1000	nS
Fall time of both SDA and SCL signals	t_f	-	300	nS
Set-up time for STOP condition	$t_{SU;STO}$	4.0	-	uS
Capacitive load for each bus line	C_b	-	400	pF

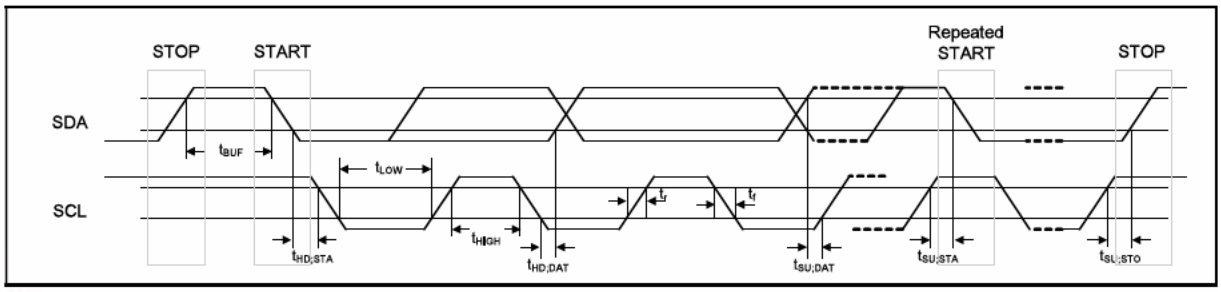
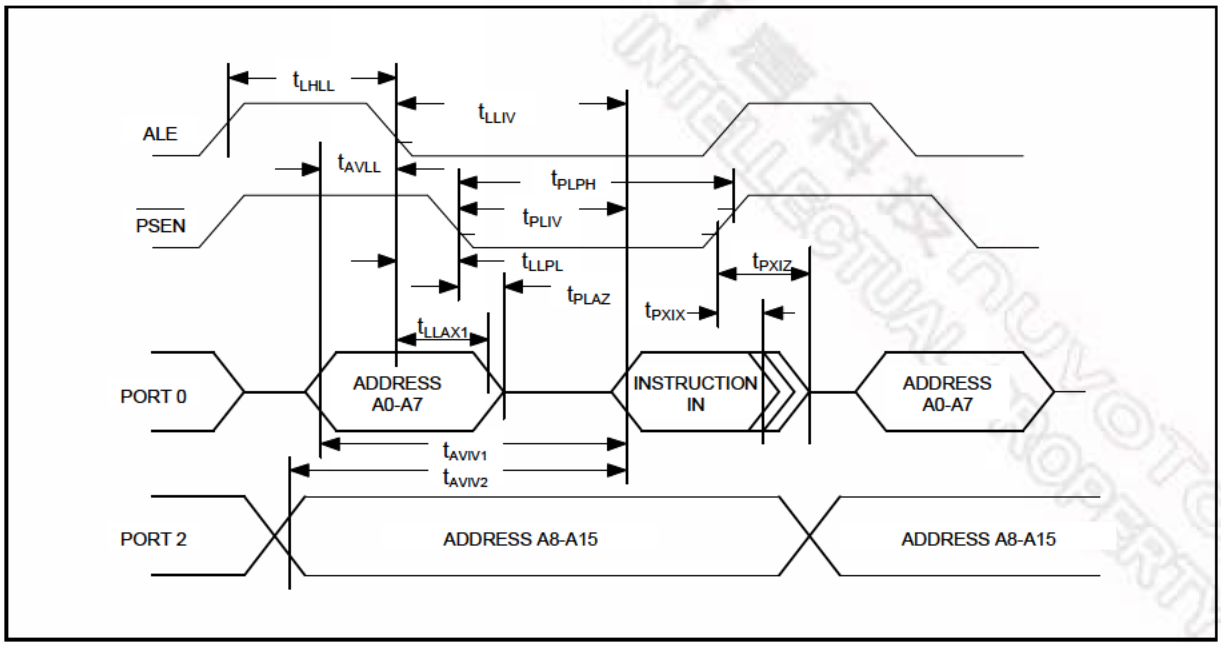
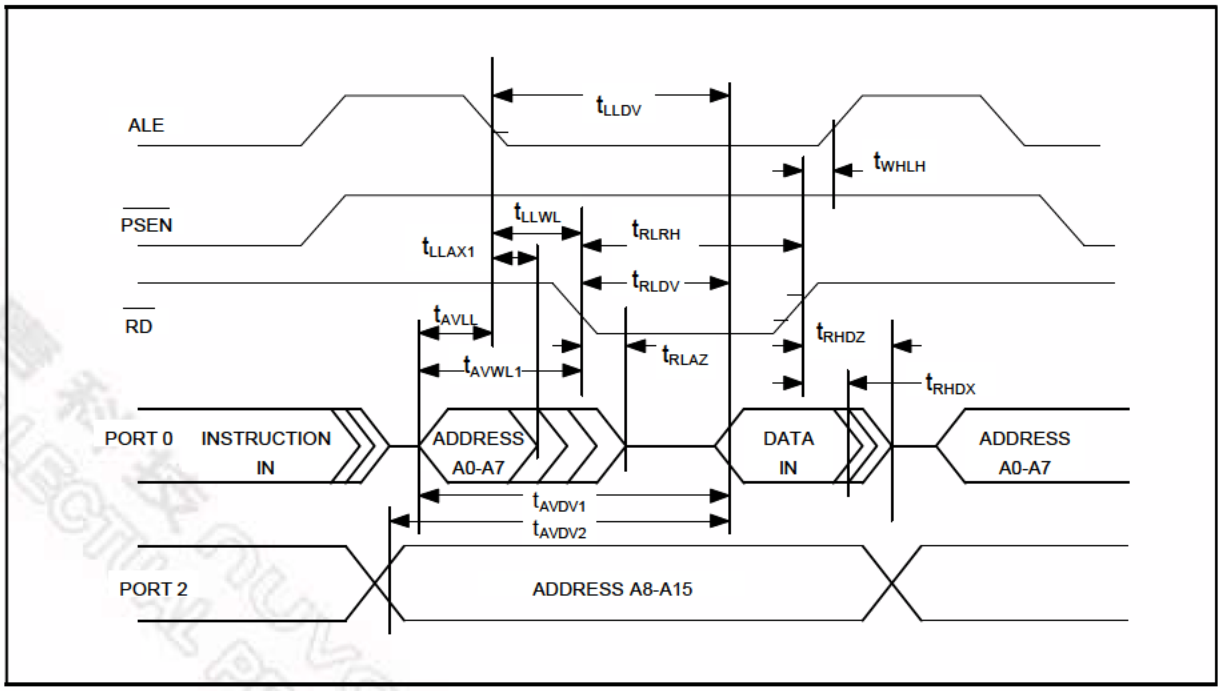


Figure 23-1 I2C Bus Timing

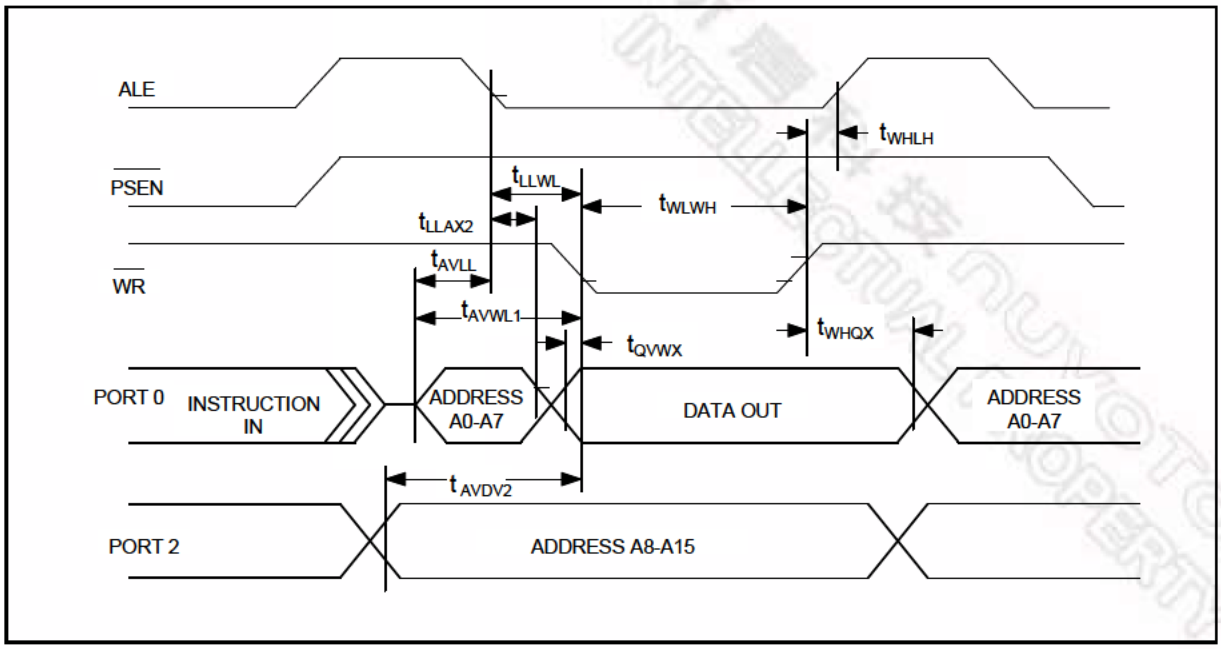
23.5 Program Memory Read Cycle



23.6 Data Memory Read Cycle



23.7 Data Memory Write Cycle



24. Typical Application Circuits

24.1 Expanded External Program Memory and Crystal

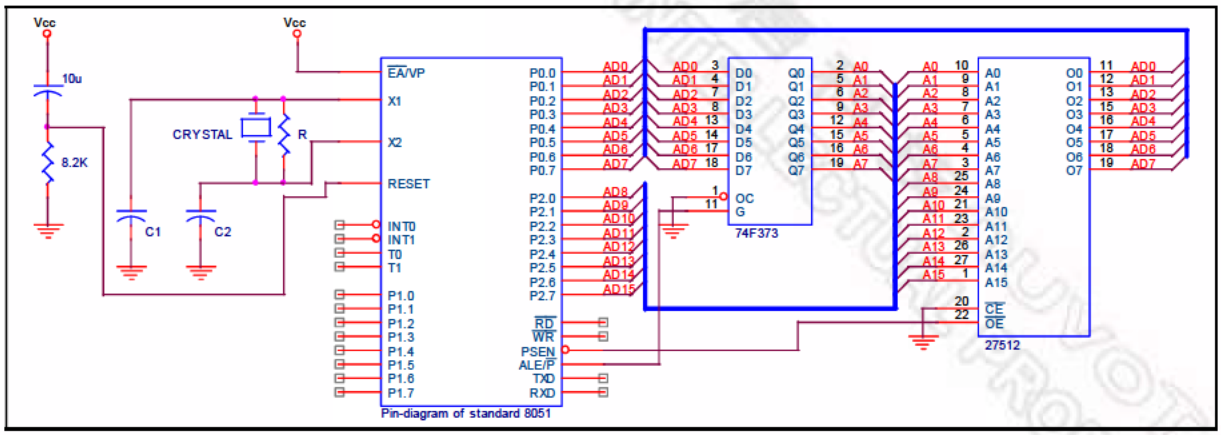


Figure 24-1

CRYSTAL	C1	C2	R
16 MHz	20P	20P	-
24 MHz	12P	12P	-
33 MHz	10P	10P	3.3K
40 MHz	1P	1P	3.3K

The above table shows the reference values for crystal applications.

Note: C1, C2, R components refer to Figure A.

24.2 Expanded External Data Memory and Oscillator

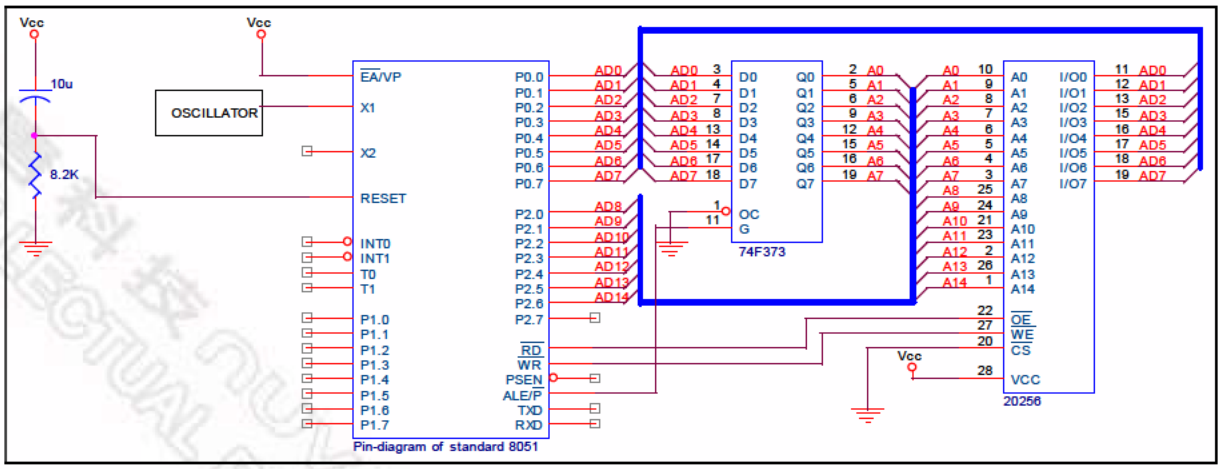
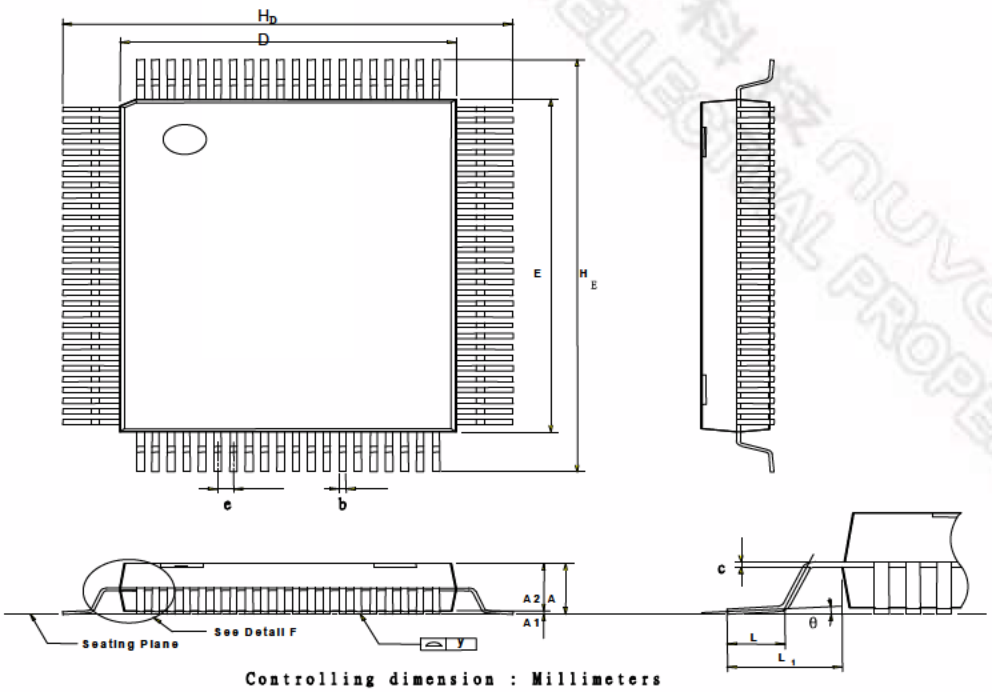


Figure 24-2

25. Package Dimensions

25.1 100L QFP(14x20x2.75mm footprint 4.8mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.004	—	0.020	0.01	—	0.50
A_2	0.098	-----	0.114	2.50	-----	2.90
b	0.008	0.012	0.016	0.20	0.30	0.40
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.547	0.551	0.555	13.90	14.00	14.10
E	0.783	0.787	0.791	19.90	20.00	20.10
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.732	0.740	0.748	18.60	18.80	19.00
H_E	0.969	0.976	0.984	24.60	24.80	25.00
L	0.039	0.047	0.055	1.00	1.20	1.40
L_1	—	0.064	—	—	2.40	—
y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

26. Application Note

In-system Programming Software Examples

This application note illustrates the in-system programmability of the Nuvoton W79E658 Flash EPROM microcontroller. In this example, microcontroller will boot from 64 KB APFlash0 bank and waiting for a key to enter in-system programming mode for re-programming the contents of 64 KB APFlash0. While entering in-system programming mode, microcontroller executes the loader program in 4KB LDFlash bank. The loader program erases the 64 KB APFlash0 then reads the new code data from external SRAM buffer (or through other interfaces) to update the 64KB APFlash0.

If the customer uses the reboot mode to update his program, please enable this b3 or b4 of security bits from the writer. Please refer security bits for detail description

EXAMPLE 1:

```
;*****************************************************************************************************************
;* Example of APFlash program: Program will scan the P1.0. if P1.0 = 0, enters in-system
;* programming mode for updating the content of APFlash code else executes the current ROM code.
;* XTAL = 24 MHz
;*****************************************************************************************************************
.chip 8052
.RAMCHK OFF
.symbols

CHPCON      EQU         9FH
TA          EQU         C7H
SFRAL       EQU         ACH
SFRAH       EQU         ADH
SFRFD       EQU         AEH
SFRCN       EQU         AFH

        ORG    0H
        LJMP   100H             ; JUMP TO MAIN PROGRAM
;*************************************************************************
;*  TIMER0 SERVICE VECTOR ORG = 000BH
;*************************************************************************
        ORG   00BH
        CLR  TR0                ; TR0 = 0, STOP TIMER0
        MOV  TL0,R6
        MOV  TH0,R7
        RETI
;*************************************************************************
;*  APFlash MAIN PROGRAM
;*************************************************************************
        ORG    100H
```

```
MAIN_APFlash:
        MOV  A,P1               ; SCAN P1.0
        ANL  A,#01H
        CJNE  A,#01H,PROGRAM_APFlash     ; IF P1.0 = 0, ENTER IN-SYSTEM PROGRAMMING
                                         ; MODE
JMP  NORMAL_MODE

PROGRAM_64:
        MOV  TA, #AAH           ; CHPCON register is written protect by TA register.
        MOV  TA, #55H
        MOV  CHPCON, #03H  ; CHPCON = 03H, ENTER IN-SYSTEM PROGRAMMING MODE
        MOV  SFRCN, #0H
        MOV  TCON, #00H         ; TR = 0 TIMER0 STOP
        MOV  IP, #00H           ; IP = 00H
        MOV  IE, #82H           ; TIMER0 INTERRUPT ENABLE FOR WAKE-UP FROM IDLE MODE
        MOV  R6, #F0H           ; TL0 = F0H
        MOV  R7, #FFH           ; TH0 = FFH
        MOV  TL0, R6
        MOV  TH0, R7
        MOV  TMOD, #01H         ; TMOD = 01H, SET TIMER0 A 16-BIT TIMER
        MOV  TCON, #10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON, #01H         ; ENTER IDLE MODE FOR LAUNCHING THE IN-SYSTEM
                                ; PROGRAMMING
;************** ********************************************************************
;* Normal mode APFlash program: depending user's application
;*******************************************************************************
NORMAL_MODE:
                                .
                                ; User's application program
                                .
                                .
                                .
```

EXAMPLE 2:

```
;*****************************************************************************************************************
;* Example of 4KB LDFlash program: This loader program will erase the APFlash first, then reads the
new ;* code from external SRAM and program them into APFlash bank. XTAL = 24 MHz
;*****************************************************************************************************************
.chip 8052
.RAMCHK OFF
.symbols

CHPCON        EQU          9FH
```

```
TA              EQU             C7H
SFRAL           EQU             ACH
SFRAH           EQU             ADH
SFRFD           EQU             AEH
SFRCN           EQU             AFH

                ORG 000H
                LJMP 100H                   ; JUMP TO MAIN PROGRAM
;*******************************************************************
;* 1. TIMER0 SERVICE VECTOR ORG = 0BH
;*******************************************************************
                ORG 000BH
                CLR   TR0                   ; TR0 = 0, STOP TIMER0
                MOV  TL0, R6
                MOV  TH0, R7
                RETI
;*******************************************************************
;*  4KB LDFlash MAIN PROGRAM
;*******************************************************************
        ORG 100H
MAIN_4K:
        MOV  TA,#AAH
        MOV  TA,#55H
        MOV  CHPCON,#03H   ; CHPCON = 03H, ENABLE IN-SYSTEM PROGRAMMING.
        MOV  SFRCN,#0H
        MOV  TCON,#00H     ; TCON = 00H, TR = 0 TIMER0 STOP
        MOV  TMOD,#01H     ; TMOD = 01H, SET TIMER0 A 16BIT TIMER
        MOV  IP,#00H       ; IP = 00H
        MOV  IE,#82H       ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  R6,#F0H
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7
        MOV  TCON,#10H     ; TCON = 10H, TR0 = 1, GO
        MOV  PCON,#01H     ; ENTER IDLE MODE

 UPDATE_APFlash:
        MOV  TCON,#00H     ; TCON = 00H , TR = 0 TIM0 STOP
        MOV  IP,#00H       ; IP = 00H
        MOV  IE,#82H       ; IE = 82H, TIMER0 INTERRUPT ENABLED
        MOV  TMOD,#01H     ; TMOD = 01H, MODE1
        MOV  R6,#D0H       ; SET WAKE-UP TIME FOR ERASE OPERATION, ABOUT 15 ms
```

```
                                ; DEPENDING ON USER'S SYSTEM CLOCK RATE.
        MOV  R7,#8AH
        MOV  TL0,R6
        MOV  TH0,R7

ERASE_P_4K:
        MOV  SFRCN,#22H     ; SFRCN = 22H, ERASE APFlash0
                            ; SFRCN = A2H, ERASE APFlash1
        MOV  TCON,#10H      ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H      ; ENTER IDLE MODE (FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************
        MOV  SFRCN,#0H      ; SFRCN = 00H, READ APFlash0
                            ; SFRCN = 80H, READ APFlash1
        MOV  SFRAH,#0H      ; START ADDRESS = 0H
        MOV  SFRAL,#0H
        MOV  R6,#FDH        ; SET TIMER FOR READ OPERATION, ABOUT 1.5 μS.
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7

blank_check_loop:
        SETB  TR0           ; enable TIMER 0
        MOV  PCON,#01H      ; enter idle mode
        MOV  A,SFRFD        ; read one byte
        CJNE  A,#FFH,blank_check_error
        INC  SFRAL          ; next address
        MOV  A,SFRAL
        JNZ   blank_check_loop
        INC  SFRAH
        MOV  A,SFRAH
        CJNE  A,#0H,blank_check_loop   ; end address = FFFFH
        JMP  PROGRAM_APFlashROM

blank_check_error:
        JMP  $

;*************************************************************************
;* RE-PROGRAMMING APFlash BANK
;*************************************************************************
PROGRAM_APFlashROM:
```

```
        MOV  R2,#00H          ; Target low byte address
        MOV  R1,#00H          ; TARGET HIGH BYTE ADDRESS
        MOV  DPTR,#0H
        MOV  SFRAH,R1         ; SFRAH, Target  high address
        MOV  SFRCN,#21H       ; SFRCN = 21H, PROGRAM APFlash0
                              ; SFRCN = A1H, PROGRAM APFlash1
        MOV  R6,#9CH          ; SET TIMER FOR PROGRAMMING, ABOUT 50 μS.
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7

PROG_D_APFlash:
        MOV  SFRAL,R2         ; SFRAL = LOW BYTE ADDRESS
        CALL  GET_BYTE_FROM_PC_TO_ACC        ; THIS PROGRAM IS BASED ON USER'S
                                             ;CIRCUIT.
        MOV  @DPTR,A          ; SAVE DATA  INTO SRAM TO VERIFY CODE.
        MOV  SFRFD,A          ; SFRFD = data IN
        MOV  TCON,#10H        ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H        ; ENTER IDLE MODE (PRORGAMMING)
        INC  DPTR
        INC  R2
        CJNE  R2,#0H,PROG_D_APFlash
        INC  R1
        MOV  SFRAH,R1
        CJNE  R1,#0H,PROG_D_APFlash

;*******************************************************************************
; * VERIFY APFlash BANK
;*******************************************************************************
        MOV  R4,#03H          ; ERROR COUNTER
        MOV  R6,#FDH          ; SET TIMER FOR READ VERIFY, ABOUT 1.5 μS.
        MOV  R7,#FFH
        MOV  TL0,R6
        MOV  TH0,R7
        MOV  DPTR,#0H         ; The start address of sample code
        MOV  R2,#0H           ; Target  low byte address
        MOV  R1,#0H           ; Target  high byte address
        MOV  SFRAH,R1         ; SFRAH, Target high address
        MOV  SFRCN,#00H       ; SFRCN = 00H, Read APFlash0
                              ; SFRCN = 80H , Read APFlash1

READ_VERIFY_APFlash:
```

```
        MOV  SFRAL,R2          ; SFRAL = LOW ADDRESS
        MOV  TCON,#10H         ; TCON = 10H, TR0 = 1,GO
        MOV  PCON,#01H
        INC  R2
        MOVX  A,@DPTR
        INC  DPTR
        CJNE  A,SFRFD,ERROR_APFlash
        CJNE  R2,#0H,READ_VERIFY_APFlash
        INC  R1
        MOV  SFRAH,R1
        CJNE  R1,#0H,READ_VERIFY_APFlash

;*****************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*****************************************************************************
        MOV  TA,#AAH
        MOV  TA,#55H
        MOV  CHPCON,#83H            ; SOFTWARE RESET. CPU will restart from APFlash0

ERROR_APFlash:
        DJNZ  R4,UPDATE_APFlash     ; IF ERROR OCCURS, REPEAT 3 TIMES.
.                                   ; IN-SYST PROGRAMMING FAIL, USER'S PROCESS TO
                                    ;DEAL WITH IT.
                        .
                        .
                        .
```

27. Version History

VERSION	DATE	PAGE	DESCRIPTION
A1.0	April 20, 2007	-	Initial Issued
A2.0	December 24, 2007	7 7 100 21,74	1. Add pin description of debug pins. 2. Revise the description of P4 mode1 3. Separate operating voltage to 2 items. 4. Revise the content of UART mode select table. (SM0, SM1) is exchanged.
A3.0	January 6, 2009	4	1. Add a note for V_{DD} during power on/off.
A4.0	March 03, 2010	6 100	1. Revise the I/O structure description of Port0. 2. Revise the "DC Characteristics" value.
A5.0	Oct 08, 2010	5,104	1. Revise the operating voltage of W79L658A from 3.0~5.5V to 3.0V~4.5V.

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