8-BIT MICROCONTROLLER

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1. GENERAL DESCRIPTION

The W78C438C is a high-performance single-chip CMOS 8-bit microcontroller that is a derivative of the W78C58 microcontroller family. The W78C438C is functionally compatible with the W78C32, except that it provides either a 64 KB program/1 MB data memory address or memory-mapped chip select logic, five general I/O ports, and four external interrupts.

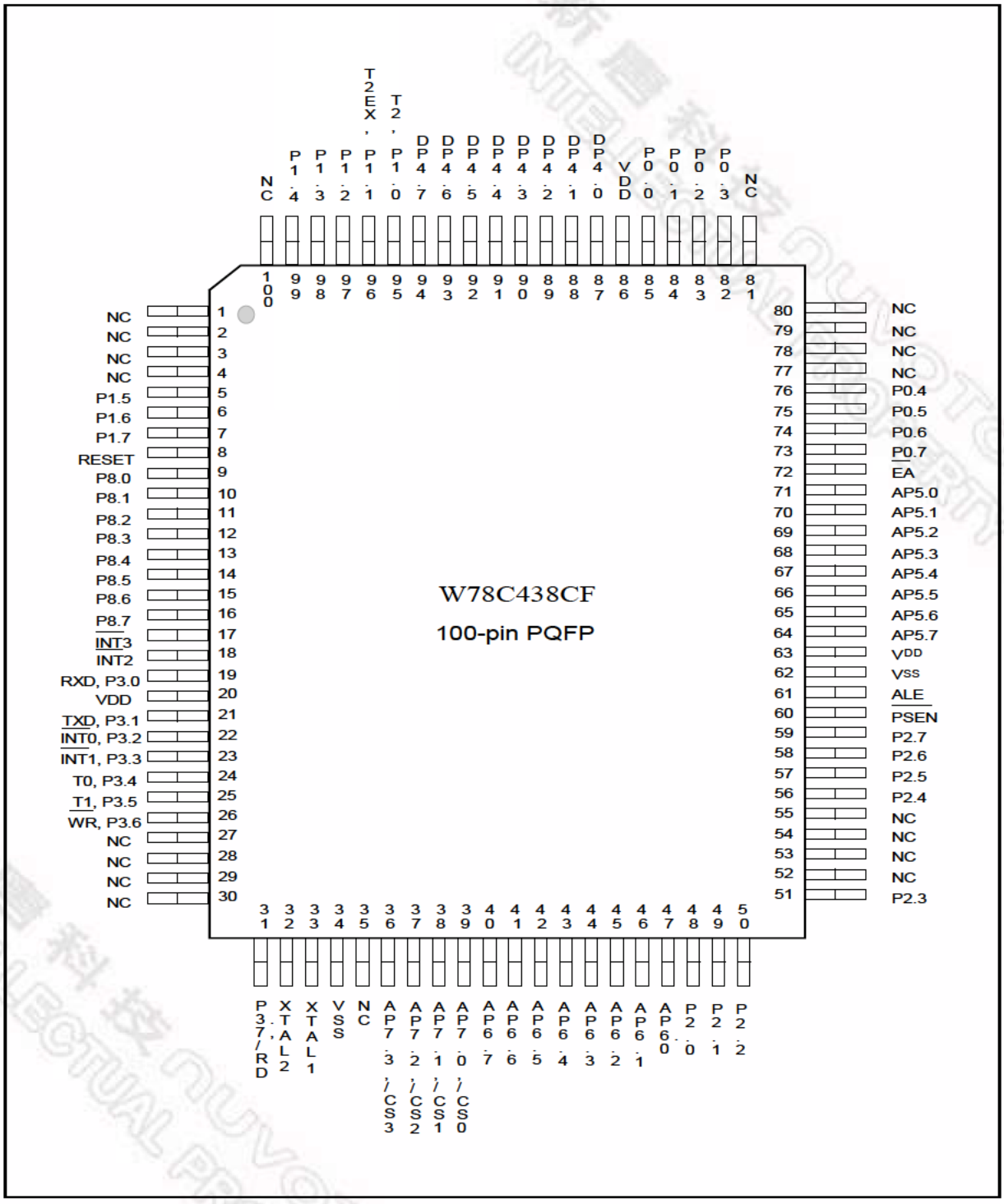
In the W78C32, two I/O ports, Port 1 and Port 3, are available for general-purpose use (Port 3 also supports alternative functions), and Port 2 and Port 0 are used as the address bus and data bus, respectively. To enable Port 0 and Port 2 to also be used as general purpose I/O ports, the W78C438C provides two dedicated address ports (AP5 and AP6) that serve as address output for 64 KB of memory and one address/data port (DP4) that serves as ROM code input and external RAM data input/output. Unlike the W78C32, this product does not require an external latch device for multiplexing low byte addresses. The W78C438C also provides four pins (AP7.0–AP7.3) to support either 64 KB program/1 MB data memory space or memory-mapped chip select logic, one parallel I/O port (Port 8) without bit addressing mode, and two additional external interrupts ($\overline{INT2}$, $\overline{INT3}$) .

The W78C438C is programmed in a manner fully compatible with that used to program the W78C32, except that the external data RAM is accessed by the "MOVX @Ri" instruction. Address paging is performed by loading page addresses into the HB (high byte) register, which is not a standard register in the W78C32, before execution of the "MOVX @Ri" instruction.

2. FEATURES

- 8-bit CMOS microcontroller
- Fully static design
- DC to 40 MHz operation
- ROM-less operation
- 256-byte on-chip scratchpad RAM
- Either 64 KB program/1 MB data memory address space or 4 memory-mapped chip select pins
- One 8-bit data/address port
- Two 8-bit and one 4-bit (optional) address ports
- Five 8-bit bidirectional I/O ports
  - Four 8-bit bit-addressable I/O ports and one 8-bit parallel I/O port
- Eight-source, two-level interrupt capability
- Three 16-bit timer/counters
- Four external interrupts
- One full-duplex serial channel
- Built-in power management
  - Idle mode
  - Power-down mode
- Packages:
  - Lead Free (RoHS) PQFP 100: W78C438C40FL

3. PIN CONFIGURATIONS



4. PIN DESCRIPTION

P0.0–P0.7 I/O Port 0

These pins function the same as those in the W78C32, except that a multiplexed address/data bus is not provided during accesses to external memory.

P1.0–P1.7 I/O Port 1

Functions are the same as in the W78C32.

P2.0–P2.7 I/O Port 2

Functions are the same as in the W78C32, except that an upper address bus is not provided during accesses to external memory.

P3.0–P3.7 I/O Port 3

Functions are the same as in the W78C32.

DP4.0–DP4.7 Data/Address Bus

DP4 provides multiplexed low-byte address/data during access to external memory.

AP5.0–AP5.7 Address Bus

AP5 outputs the <7:0> address of the external ROM multiplexed with the <7:0> address of the external data RAM.

AP6.0–AP6.7 Address Bus

AP6 outputs the <15:8> address of the external ROM multiplexed with the <15:8> address of the external data RAM. During the execution of "MOVX @Ri," the output of AP6 comes from the HB register, which is the page register for the high byte address, and its address is 0A1H.

AP7.0–AP7.3 Address Bus/Chip Select Pins

Set bit 7 of the EPMA (Extended Program Memory Address) register to determine the functions of port 7. When this bit is "0" (default value), AP7 allows the external memory data to be accessed by outputting the <19:16> address of the external memory from bits<3:0> of the EPMA register during the execution of "MOVC A, @A+DPTR" or "MOVX dest, src." At all other times, AP7<3:0> will output 0H.

When this bit is "1," AP7<3:0> (CS3–0) are the chip select pins, which support memory-mapped peripheral device select, and only one pin is active low at any one time. These pins are decoded by AP6<7:6>. For details, see the table below.

AP6.7	AP6.6	DESCRIPTION
0	0	AP70: low; others: high
0	1	AP71: low; others: high
1	0	AP72: low; others: high
1	1	AP73: low; others: high

P8.0–P8.7 I/O Port

Functions are the same as those of Port 1 in the W78C31, except that they are mapped by the P8 register and not bit-addressable. The P8 register is not a standard register in the W78C32. Its address is at 0A6H.

$\overline{\text{INT2}}$, $\overline{\text{INT3}}$ External Interrupt, Input

Functions are similar to those of external $\overline{\text{INT0}}$, $\overline{\text{INT1}}$ in the W78C32, except that the functions/status of these interrupts are determined/shown by the bits in the XICON (External Interrupt Control) register. The XICON register is bit-addressable but is not a standard register in the W78C32. Its address is at 0C0H. For details, see the Functional Description below.

$\overline{\text{EA}}$ External Address, Input

Functions same as W78C32.

RST, XTAL1, XTAL2, $\overline{\text{PSEN}}$, ALE

Functions same as W78C32.

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5. FUNCTIONAL DESCRIPTION

The W78C438C is a functional extension of the W78C58 microcontroller. It contains a 256 × 8 RAM, 64 KB program/1 MB data memory address or memory-mapped chip select logic, two 8-bit address ports, one 8-bit data port, five general I/O ports, four external interrupts, three timers/counters, and one serial port.

5.1 Dedicated Data and Address Port

The W78C438C provides four general-purpose I/O ports for W78C32 applications; the address and data bus are separated from Port 0 and Port 2 so that these ports can be used as general-purpose I/O ports. In this product, DP4 is the data bus for external ROM and RAM, AP5<7:0> are the low byte address, AP6<7:0> are the high byte address, $\overline{PSEN}$ enables the external ROM to DP4, and P3.6 ($\overline{WR}$) and P3.7 ($\overline{RD}$) are the write/read control signals for the external RAM. The external latch for multiplexing the low byte address is no longer needed in this product. The W78C438C uses AP5 and AP6 to support 64 KB external program memory and 64 KB external data memory, just as a standard W78C32 does.

The W78C438C provides four pins, AP7.3–AP7.0 (CS3–CS0), to support either 64 KB program/1 MB data memory space or memory-mapped chip select logic. Bit 7 of the EPMA (Extended Program Memory Address) register, which is described in Table 1 below, determines the functions of these pins.

When this bit is "0" (the default value), AP7<3:0> support external program/data memory addresses up to 64 KB/1 MB for applications which need additional external memory to store large amounts of data.

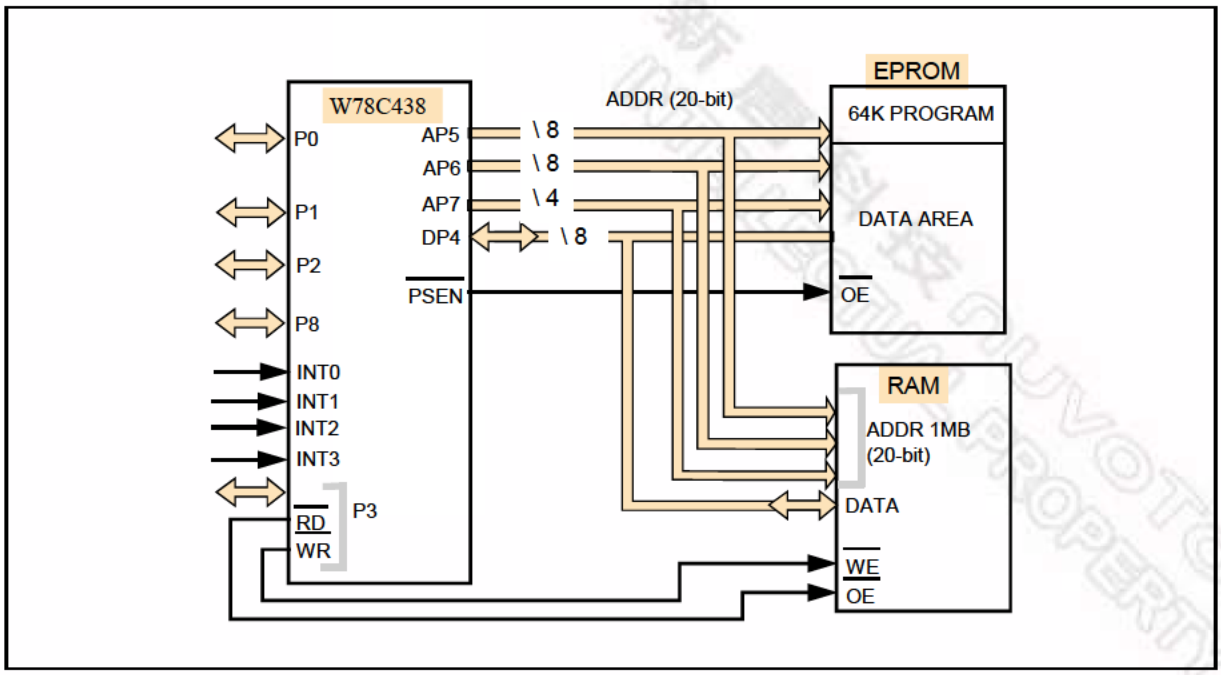
Although there is 1M bytes memory space, instructions stored here can not be run at full range of this area except the first 64 Kbytes. It is owing to the fact that during the instruction fetch cycle, AP7<3:0> always output 0s to address lines A19–A16. This limits the program code to store at address 0–0FFFFH (64K). The rest of the area (10000H–FFFFFH) can be treated as ROM data storage which can be read by "MOVC A, @A+DPTR" instruction.

When "MOVC A, @A+DPTR" is executed to read the external ROM data or "MOVX dest, src" is executed to access the external RAM data, AP7<3:0> output address <19:16> from bits <3:0> of the EPMA (Extended Program Memory Address) register. At other times, AP7<3:0> always output 0H to ensure the instruction fetch is within the 64K program memory address. Different banks can be selected by modifying the content of the EPMA register before the execution of "MOVC A, @A+DPTR" or "MOVX dest, src."

[Example]. Access the external ROM/RAM data from external memory space.

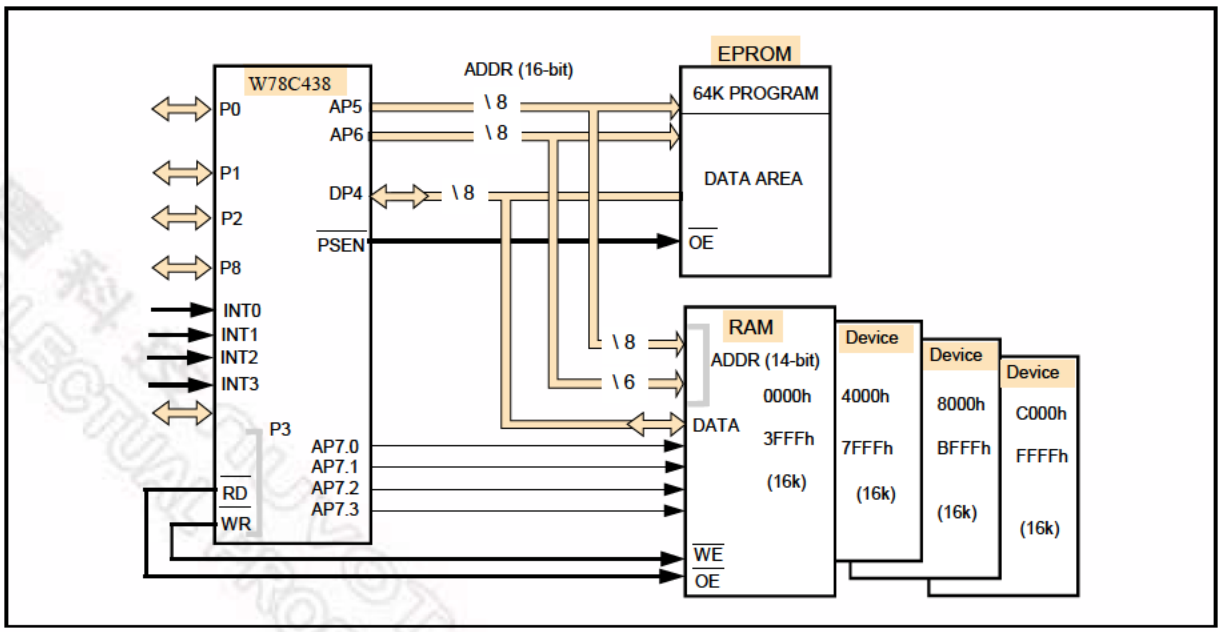
```
CLR     A               ; Clear Accumulator.
MOV     DPTR, #0H       ; Clear DPTR.
MOV     0A2H, #02       ; Initialize EPMA(0A2H). EPMA.7 = 0: extended memory space
                        ; EPMA.<3:0> = 0010B,   the address range: 20000–2FFFFH.
MOVC    A, @A+DPTR      ; Read the external ROM data from location 20000H.
MOVX    A, @DPTR        ; Read the external RAM data from location 20000H.
CLR     A
MOV     0A2H, #03H      ; EPMA.<3:0> = 0011B, the address range: 30000H–3FFFFH.
MOVC    A, @A+DPTR      ; Read the external ROM data from location 30000H.
MOVX    @DPTR, A        ; Write the contents of Accumulator to external RAM data.
                        ; location 30000H.
```

(A) EPMA.7 = 0



When bit 7 of the EPMA is "1," AP7<3:0> are the output pins that support memory-mapped peripheral chip select logic, which eliminates the need for glue logic. These pins are decoded by AP6<7:6>. Only one pin is active low at any time. That is, they are active individually with 16K address resolution. For example, CS0 is active low in the address range from 0000H to 3FFFH, CS1 is active low in the address range from 4000H to 7FFFH, and so forth.

(B) EPMA.7 = 1



The EPMA register is a nonstandard 8-bit SFR at address 0A2H in the standard W78C32. To read/write the EPMA register, one can use the "MOV direct" instruction or "read-modify-write" instructions. Bits <6:4> of the EPMA register are reserved bits, and their output values are 111B if they are read. The content of EPMA is 70H after a reset. The EPMA register does not support bit-addressable instructions.

BIT	NAME	FUNCTION
7	EPMA7	EPMA7 = 0: 64 KB program/1 MB data memory space mode EPMA7 = 1: memory-mapped chip select mode
6	EPMA6	Reserved
5	EPMA5	Reserved
4	EPMA4	Reserved
3	EPMA3	Value of AP7.3
2	EPMA2	Value of AP7.2
1	EPMA1	Value of AP7.1
0	EPMA0	Value of AP7.0

Table 1. Functional Description of EPMA Register

5.2 Additional I/O Port

The W78C438C provides one parallel I/O port, Port 8. Its function is the same as that of Port 1 in the W78C31, except that it is mapped by the P8 register and is not bit-addressable. The P8 register is not a standard register in the standard W78C32. Its address is at 0A6H. To read/write the P8 register, one can use the "MOV direct" instruction or "read-modify-write" instructions.

```
[Example]:  MOV    0A6H, A     ; Output data via Port 8.
            MOV    A, 0A6H     ; Input data via Port 8.
```

5.3 Additional External Interrupt

The W78C438C provides two additional external interrupts, $\overline{INT2}$ and $\overline{INT3}$, whose functions are similar to those of external interrupts 0 and 1 in the W78C32. The functions (or the status) of these interrupts are determined by (or shown by) the bits in the XICON (External Interrupt Control) register. For details, see Table 2. The XICON register is bit-addressable but is not a standard register in the standard 80C32. Its address is at 0C0H. To set/clear the bit of the XICON register, one can use the "SETB($\overline{CLR}$) bit" instruction. For example, "SETB 0C2H" sets the EX2 bit of XICON. The interrupt vector addresses and the priority polling sequence within the same level are shown in Table 3.

[Example].

```
        SETB    0C0H    ; INT2 is falling-edge triggered.
        SETB    0C3H    ; INT2 is high-priority.
        SETB    0C2H    ; Enable INT2.
        CLR     0C4H    ; INT3 is low-level triggered.
```

BIT	ADDR.	NAME	FUNCTION
7	0C7H	PX3	High/low priority level for $\overline{\text{INT3}}$ is specified when this bit is set/cleared by software.
6	0C6H	EX3	Enable/disable interrupt from $\overline{\text{INT3}}$ when this bit is set/cleared by software.
5	0C5H	IE3	If IT3 is "1," IE3 is set/cleared automatically by hardware when interrupt is detected/serviced.
4	0C4H	IT3	$\overline{\text{INT3}}$ is falling-edge/low-level triggered when this bit is set/cleared by software.
3	0C3H	PX2	High/low priority level for $\overline{\text{INT2}}$ is specified when this bit is set/cleared by software.
2	0C2H	EX2	Enable/disable interrupt from $\overline{\text{INT2}}$ when this bit is set/cleared by software.
1	0C1H	IE2	If IT2 is "1," IE2 is set/cleared automatically by hardware when interrupt is detected/serviced.
0	0C0H	IT2	$\overline{\text{INT2}}$ is falling-edge/low-level triggered when this bit is set/cleared by software.

Table 2. Functions of XICON Register

INTERRUPT SOURCE	VECTOR ADDRESS	PRIORITY SEQUENCE
External Interrupt 0	03H	0 (Highest)
Timer/Counter 0	0BH	1
External Interrupt 1	13H	2
Timer/Counter 1	1BH	3
Serial Port	23H	4
Timer/Counter 2	2BH	5
External Interrupt 2	33H	6
External Interrupt 3	3BH	7 (Lowest)

Table 3. Priority of Interrupts

5.4 Newly Added Special Function Registers

The W78C438C uses four newly defined special function registers, which are described in Table 4. To read/write these registers, use the "MOV direct" or "read-modify-write" instructions.

	REGISTER	ADDR.	FUNCTION	LENGTH	R/W TYPE	VALUE AFTER RESET
1	HB	A1H	During the execution of "MOVX @Ri," the content of HB is output to AP6.	8	R/W	00H
2	EPMA	A2H	EPMA.7 determines functions of AP7. EPMA.3–EPMA.0 determine values of AP7<3:0> when EPMA.7 is "0."	8	R/W	70H
3	P8	A6H	The content of P8 is output to port 8.	8	R/W	0FFH
4	XICON	C0H	The bits of XICON determine/show the functions/status of $\overline{INT2}$ – $\overline{INT3}$. *Bit-addressable.*	8	R/W	00H

Table 4. Newly Added Special Function Registers of the W78C438C

Notes:

1. The instructions used to access these nonstandard registers may cause assembling errors with respect to the 2500 A. D. assembler, but these errors can be ignored by adding directive ".RAMCHK OFF" ahead these instructions.
2. In the newly added SFR of W78C438C, only XICON register is bit-addressable.

5.5 Power Reduction Function

The W78C438C supports power reduction just as the W78C32 does. The following table shows the status of the external pins during the idle and power-down modes.

FUNCTION	ALE, $\overline{PSEN}$	P0–P3, P8	DP4	AP5, AP6	AP7
Idle	1 1	Port Data	Floating	Address	Note
Power Down	0 0	Port Data	Floating	Address	Note

Note: AP7 is either 0 or a value decoded by AP6<7:6>, depending on the value of EPMA.7.

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5.6 Programming Difference

The W78C438C is programmed in the same way as the W78C32, except that the external data RAM is accessed by a "MOVX @Ri" instruction. To support address paging, there is an additional 8-bit SFR "HB" (high byte), which is a nonstandard register, at address 0A1H. During execution of the "MOVX @Ri" instruction, the contents of HB are output to AP6. The page address is modified by loading the HB register with a new value before execution of the "MOVX @Ri" instruction. To read/write the HB register, one can use the "MOV direct" instruction or "read-modify-write" instructions. The HB register does not support bit-addressable instructions.

```
[Example].   MOV    R1, #0H       ; R1 = 0.
             MOV    0A1H, #0FFH   ; HB contents  FFH.
             MOVX   A, @R1        ; Read the contents of external RAM location FF00H into
                                  ; Accumulator.
             MOV    0A1H, #12H    ; HB contents 12H.
             MOVX   @R1, A        ; Copies the contents of Accumulator into external RAM
                                  ; location 1200H.
```

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6. ELECRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Operating Temperature	T_{OPR}	0	70	°C
Storage Temperature	T_{STG}	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

6.2 D.C. Characteristics

(V_{DD} – V_{SS} = 5V ±10%, T_A = 25° C, F_{OSC} = 20 MHz, unless otherwise specified.)

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Oper. Voltage	V_{DD}		4.5	5	5.5	V
Oper. Current	I_{DD}	* No load	-	-	20	mA
Idle Current	I_{IDLE}	Program idle mode	-	-	7	mA
Pwdn Current	I_{PWDN}	Program power-down mode	-	-	50	µA
Input Leakage Current	I_{LK1}	$\overline{INT2}$, $\overline{INT3}$ Internal pull-high Notes 1, 2	-300	-	+10	µA
Input Leakage Current	I_{LK2}	RESET Internal pull-low Notes 1, 2	-10	-	+300	µA
Input Leakage Current	I_{LK3}	$\overline{EA}$, Port 0, DP4 Note 1	-10	-	+10	µA
Input Leakage Current	I_{LK4}	P1, P2, P3, P8 Note 1	-50	-	+10	µA
Output Low Voltage	V_{OL1}	I_{OL1} = 2 mA (Port 1, 2, 3, 8)	-	-	0.45	V
Output High Voltage	V_{OH1}	I_{OH1} = -100 µA (Port 1, 2, 3, 8)	2.4	-	-	V
Output Low Voltage	V_{OL2}	I_{OL2} = 4mA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	-	-	0.45	V
Output High Voltage	V_{OH2}	I_{OH2} = -400 µA Note 3 (ALE, $\overline{PSEN}$, P0, DP4)	2.4	-	-	V
Output Low Voltage	V_{OL3}	I_{OL2} = 2 mA (AP5, AP6, AP7)	-	-	0.45	V
Output High Voltage	V_{OH3}	I_{OH2} = -100 µA (AP5, AP6, AP7)	2.4	-	-	V
Input Voltage	V_{ILT}	V_{DD} = 5V ±10%	0	-	0.8	V
Input Voltage	V_{IHT}	V_{DD} = 5V ±10%	2.4	-	Note 4	V

D.C. Characteristics, continued

PARAMETER	SYM.	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{ILC}	V_{DD} = 5V ±10%, XTAL1 Note 5	0	-	0.8	V
Input Voltage	V_{IHC}	V_{DD} = 5V ±10%, XTAL1 Note 5	3.5	-	Note 4	V
Input Voltage	V_{ILR}	V_{DD} = 5V ±10%, RESET Note 5	0	-	0.8	V
Input Voltage	V_{IHR}	V_{DD} = 5V ±10%, RESET Note 5	2.4	-	Note 4	V

Notes:

1. $0 < V_{IN} < V_{DD}$, for $\overline{INT2}$, $\overline{INT3}$, RESET, $\overline{EA}$, Port 0, DP4, P1, P2, P3 and P8 inputs in leakage.
2. Using an internal pull low/high resistor (approx. 30K).
3. ALE, $\overline{PSEN}$, P0 and DP4 in external program or data access mode.
4. The maximum input voltage is V_{DD} +0.2V.
5. XTAL1 is a CMOS input and RESET is a Schmitt trigger input.

6.3 A.C. Characteristics

AC specifications are a function of the particular process used to manufacture the product, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (T_{CP}), and actual parts will usually experience less than a ±20 nS variation.

6.3.1 Clock Input Waveform

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	F_{OP}	0	-	40	MHz	1
Clock Period	T_{CP}	25	-	-	nS	2
Clock High	T_{CH}	10	-	-	nS	3
Clock Low	T_{CL}	10	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.
2. The T_{CP} specification is used as a reference in other specifications.
3. There are no duty cycle requirements on the XTAL1 input.

6.3.2 Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{PSEN}$ Low	T_{APL}	2 T_{CP}	-	-	nS
$\overline{PSEN}$ Low to Data Valid	T_{PDV}	-	-	2 T_{CP}	nS

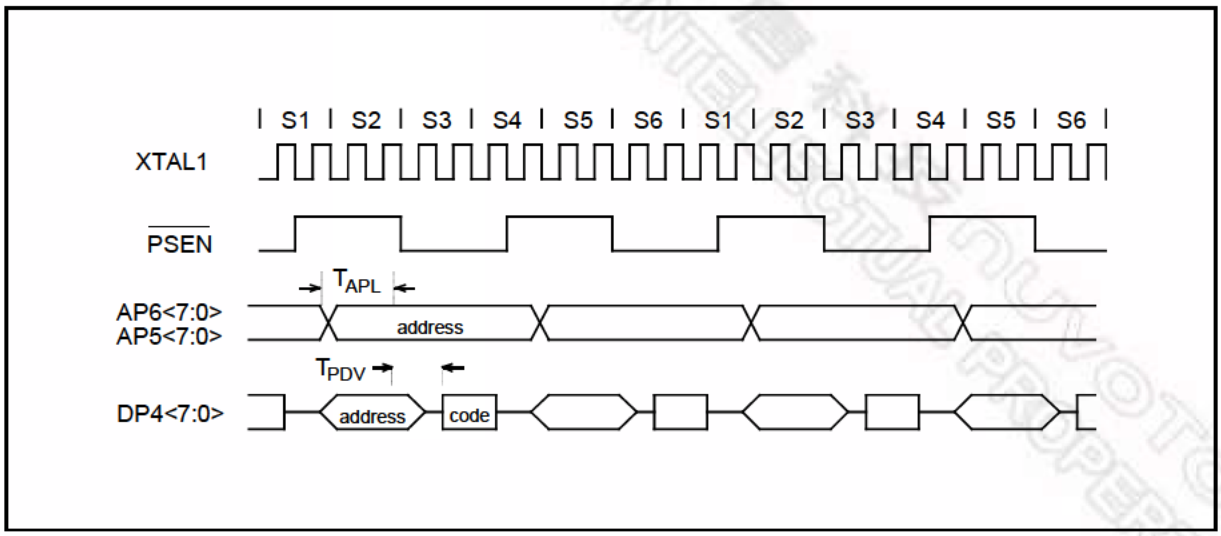
6.3.3 Data Memory Read/Write Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Address Valid to $\overline{RD}$ Low	TARL	4 TCP	-	4 TCP +Δ	nS
$\overline{RD}$ Low to Data Valid	TRDV	-	-	4 TCP	nS
Data Hold After $\overline{RD}$ High	TRDQ	0	-	2 TCP	nS
$\overline{RD}$ Pulse Width	TRS	6 TCP -Δ	6 TCP	-	nS
Address Valid to $\overline{WR}$ Low	TAWL	4 TCP	-	4 TCP +Δ	nS
Data Valid to $\overline{WR}$ Low	TDWL	1 TCP	-	-	nS
Data Hold After $\overline{WR}$ High	TWDQ	1 TCP	-	-	nS
$\overline{WR}$ Pulse Width	TWS	6 TCP -Δ	6 TCP	-	nS

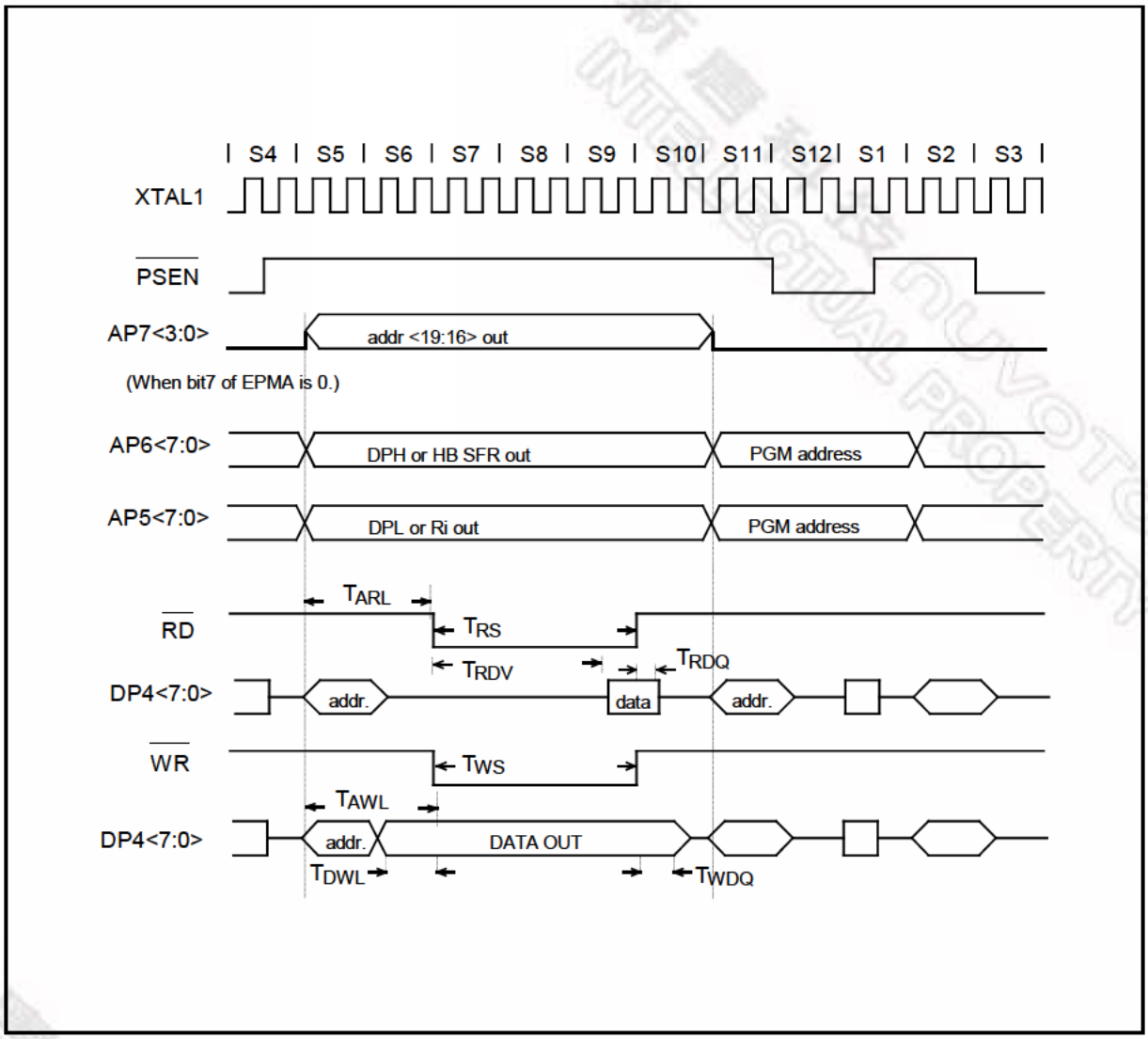
Note: "Δ" (due to buffer driving delay and wire loading) is 20 nS.

7. TIMING WAVEFORMS

7.1 Program Fetch Cycle



7.2 Data Memory Read/Write Cycle



8. TYPICAL APPLICATION CIRCUITS

8.1 Using 128K × 8 bit External EPROM (W27E010)

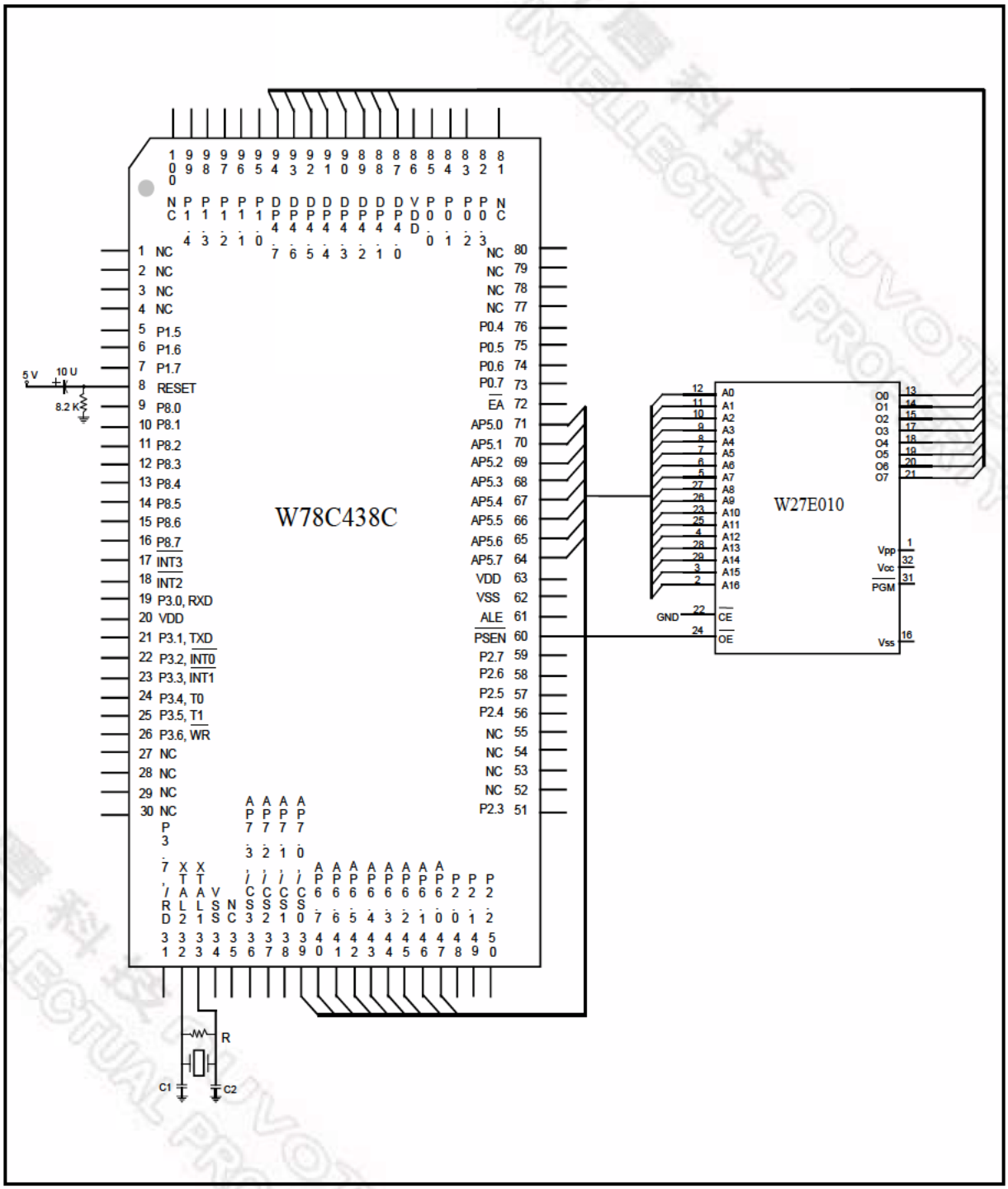


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	–
24 MHz	15P	15P	–
33 MHz	10P	10P	6.8K
40 MHz	5P	5P	6.8K

Above table shows the reference values for crystal applications.

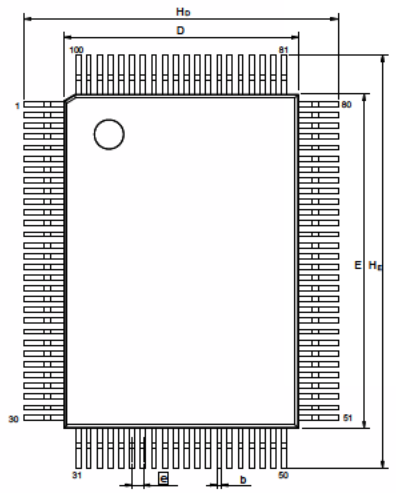
Notes:

1. For C1, C2, R components refer to Figure A.
2. It is recommended that the crystals be replaced with oscillators for applications above 35 MHz.

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9. PACKAGE DIMENSIONS

9.1 100-pin QFP



Symbol	Dimension in inches			Dimension in mm		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	0.130	—	—	3.30
A_1	0.004	—	—	0.10	—	—
A_2	0.107	0.112	0.117	2.718	2.845	2.972
b	0.010	0.012	0.016	0.254	0.305	0.407
c	0.004	0.006	0.010	0.101	0.152	0.254
D	0.546	0.551	0.556	13.87	14.00	14.13
E	0.782	0.787	0.792	19.87	20.00	20.13
e	0.020	0.026	0.032	0.498	0.65	0.802
H_D	0.728	0.740	0.752	18.49	18.80	19.10
H_E	0.964	0.976	0.988	24.49	24.80	25.10
L	0.039	0.047	0.055	0.991	1.194	1.397
L_1	0.087	0.095	0.103	2.21	2.413	2.616
y	—	—	0.004	—	—	0.102
θ	0°	—	12°	0°	—	12°

Notes:
1. Dimension D & E do not include interlead flash.
2. Dimension b does not include dambar protrusion/intrusion.
3. Controlling dimension: Millimeters
4. General appearance spec. should be based on final visual inspection spec.

10. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	July, 1998	-	Initial issued
A2	June, 2004	2	Revise part number in the item of packages
A3	April 19, 2005	19	Add Important Notice
A4	July 27, 2005	2	Add Lead free (RoHS) part number
A5	October 3, 2006		Remove block diagram
A6	December 4, 2006	2	Remove all Leaded package parts
A7	March 10, 2010	2	Remove the package parts of "Lead Free (RoHS) PLCC 84 W78C438C40PL"

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.

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