NuMicro® Family
ARM926EJ-S™-based 32-bit Microprocessor

NUC980 Series
Datasheet

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1 GENERAL DESCRIPTION

The NUC980 series 32-bit microprocessor is powered by the Arm926EJ-S™ processor core with 16 KB I-cache, 16 KB D-cache and MMU running up to 300 MHz. Its SDRAM interface supports DDR2 type running up to 150 MHz. The NUC980 series supports built-in 16KB embedded SRAM and 16.5 KB IBR (Internal Boot ROM) for booting from USB, NAND, SD/eMMC and SPI Flash, and industrial operating temperature from -40°C to 85°C. In addition, the NUC980 series provides built-in SDRAM in LQFP package to ease PCB design and reduce the BOM cost.

The NUC980 series is equipped with a large number of high speed digital peripherals, such as two 10/100 Mbps Ethernet MAC supporting RMII, a USB 2.0 high speed host/device, a USB 2.0 high speed host controller, up to six USB 1.1 host lite interfaces, two CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor, two SD interfaces supporting SD/SDHC/SDIO card, a NAND Flash interface supporting SLC and MLC type NAND Flash, an I2S interface supporting I2S and PCM protocol, Also the NUC980 series offers a built-in hardware cryptography accelerator that supports RSA, ECC, AES, SHA, HMAC and a random number generator (RNG).

The NUC980 series provides up to ten UART interfaces, two ISO-7816-3 interfaces, a Quad-SPI interface, two SPI interfaces, up to four I2C interfaces, four CAN 2.0B interfaces, eight channels PWM output, eight channels 12-bit SAR ADC, six 32-bit timers, WDT (Watchdog Timer), WWDT(Window Watchdog Timer), 32.768 kHz XTL and RTC (Real Time Clock). The NUC980 series also supports two 10-channel peripheral DMA (PDMA) for automatic data transfer between memories and peripherals.

Key Features

- 300 MHz ARM® ARM926EJ-S™ MPU with 16 KB I-cache, 16 KB D-cache
- Memory Manager Unit (MMU)
- Built-in 128 MB/64MB DDR2 SDRAM Memory in LQFP package
- Supports booting from SPI ROM/SPI NAND Flash/NAND/eMMC/SD Card and USB device
- Supports up to 100MHz Quad-SPI
- Dual Ethernet MAC
- Four CAN 2.0B interfaces
- Six USB FS Lite hosts
- Two USB High speed hosts
- One USB High speed device
- Two CCIR656/601 Camera interfaces
- Supports PRNG, AES256, SHA, ECC, and RAS2048

Applications

- Smart Home gateway
- Fingerprint Machine.
- Power concentrator
- Data Collector
- Smart Home Appliance
- Serial server
- 2D/1D Barcode reader
- Barcode printer
- Power Distribution Unit
- Ethernet Industrial Control
- SNMP Card
- Ethernet RTU/ DTU

2 FEATURES DESCRIPTION

Core And System	
Boot Loader	• Factory pre-loaded 16.5 KB mask ROM supporting four booting modes – Boot from USB – Boot from SD/eMMC – Boot from NAND Flash – Boot from SPI Flash (SPI-NOR/SPI-NAND)
Arm926EJ-S™	• Arm926EJ-S™ processor core running up to 300 MHz • Built-in 16 KB instruction cache and 16 KB data cache • Built-in Memory Management Unit (MMU) • Supports JTAG debug interface
Advanced Interrupt Controller	• Up to 64 interrupt sources including 4 external interrupts. • Configurable normal (IRQ) or fast interrupt mode (FIQ). • Configurable 8-level interrupt priority scheme.
Low Voltage Detect (LVD)	• Two-level LVD with low voltage detect interrupt. (2.8V/2.6V)
Low Voltage Reset (LVR)	• LVR with 2.4V threshold voltage level.
Memories	
SDRAM	• Built-in 128MB/ 64MB DDR2 SDRAM Memory in LQFP package • Clock speed up to 150 MHz • Supports 16-bit data width
SRAM	• Up to 16 KB on-chip SRAM • Byte-, half-word- and word-access • PDMA operation
Peripheral DMA (PDMA)	• Two sets of PDMA with ten independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 12 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation

Internal Clock Source	• Two on-chip PLL up to 500 MHz on-chip PLL, sourced from HXT, allows CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain (VBAT33) • The RTC clock source includes Low-speed external crystal oscillator (LXT) • The RTC block includes 64 bytes backup registers • Able to wake up CPU • Supports ±5ppm within 5 seconds software clock accuracy compensation • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Selectable 12-hour or 24-hour mode • Automatic leap year recognition • Supports 1 Hz clock to be Timer capture source for calibration
Timers	
32-bit Timer	• Six sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports internal capture source from RTC 1 Hz clock for interval measurement resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
PWM (PWM)	• Eight 16-bit down-count counters with four 8-bit prescalar for eight PWM output channels. • Supports complementary mode for 4 complementary paired PWM output channels
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from HXT, HXT/512 (default selection), PCLK2/4096 or LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset.
Window Watchdog	• Clock sourced from HXT, HXT/512 (default selection), PCLK2/4096 or LXT; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• One 12-bit, 9-ch 200k SPS SAR ADC with up to 8 single-ended input channels; 10-bit accuracy is guaranteed. • One internal channels for band-gap VBG input. • Supports external V_{REF} pin.

Communication Interfaces	
Low-power UART	• 10 sets of UARTs with up to 17.45 MHz baud rate. • Auto-Baud Rate measurement and baud rate compensation function. • Supports low power UART (LPUART): baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode even system clock is stopped. • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode. • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports wake-up function • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • PDMA operation.
Smart Card Interface	• Two sets of ISO-7816-3 which are compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function. • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal.
I^2C	• Four sets of I^2C devices with Master/Slave mode. • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation
Quad SPI	• One set of SPI Quad controller with Master/Slave mode, up to 96 MHz at 2.97V~3.63V stsyem voltage. • Supports Dual and Quad I/O Transfer mode (NUC980DR63YC only supports Dual mode)

	• Supports one/two data channel half-duplex transfer • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation.
SPI	• Up to two sets of SPI controllers with Master/Slave mode. • SPI provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers. • Able to communicate at up to 96 Mbit/s • Configurable bit length of a transfer word from 8 to 32-bit. • MSB first or LSB first transfer sequence. • Byte reorder function. • Supports Byte or Word Suspend mode. • Supports one data channel half-duplex transfer. • Supports receive-only mode. • PDMA operation.
I^2S	• One set of I^2S controller with I^2S protocol and PCM protocol. • Supports mono and stereo audio data with 8-, 16- and 24-bit word sizes. • Four 8-level 24-bit FIFO data buffers for left/right channel record and left/right playback. • Built-in DMA function • Supports 2 buffer address for left/right channel and 2 slots data transfer. **I^2S Mode** • Supports record and playback. • Supports master and slave mode. • Supports Philips standard and MSB-justified data format. **PCM Mode** • Supports record and playback. • Supports master mode. • Supports PCM standard data format.
Controller Area Network (CAN)	• Four CAN 2.0B interfaces • Each supports 32 Message Objects; each Message Object has its own identifier mask. • Programmable FIFO mode (concatenation of Message Object). • Disabled Automatic Re-transmission mode for Time Triggered CAN applications. • Supports power-down wake-up function.
Secure Digital Host Controller (SDHC)	• Two sets of Secure Digital Host Controllers, compliant with SD Memory Card Specification Version 2.0.

	• Supports 50 MHz to achieve 200 Mbps at 3.3V operation. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card.
NAND Flash Controller	• Supports SLC and MLC type NAND Flash device. • Supports 2KB, 4KB and 8KB page size NAND Flash device. • 8-bit data width. • Supports ECC8, ECC12 and ECC24 BCH algorithm with ECC code generation, error detection and error correction. • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and NAND Flash.
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter. • Each bank supports dedicated external chip select pin with polarity control and up to 1 MB addressing space. • 8-/16-bit data width. • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R). • Supports address bus and data bus separate mode. • Supports LCD interface i80 mode. • PDMA operation.
GPIO	• Supports four I/O modes: Bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode. • Selectable TTL/Schmitt trigger input. • Configured as interrupt source with edge/level trigger setting. • Supports independent pull-up/pull-down control. • Supports 5V-tolerance function except analog I/O. (Except PB.0 ~ 7; All USB High Speed PIN.)
Advanced Connectivity	
USB 1.1 Host Lite	• Compliant with USB Revision 2.0 Specification. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Supports Control, Bulk, Interrupt, Isochronous and Split transfers. • Supports an integrated Root Hub. • Up to six USB Host Lite ports. • Built-in DMA. • Apply to USB dongle devices or USB cable length is limited to less than 1 meter.
USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed Host/Device** • One set of on-chip USB 2.0 high speed dual role transceiver configurable as host, device or ID-dependent. • One set of on-chip USB 2.0 high speed transceiver with host only. **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification. • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0.

	• Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Integrated with a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Built-in DMA. **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports one dedicate control endpoint and 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction. • 4096 bytes configurable RAM for endpoint buffer and up to 1024 bytes packet size. • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode. • Suspend, resume and remote wake-up capability. • Built-in DMA.
Ethernet MAC	• IEEE Std. 802.3 CSMA/CD protocol. • Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol. • Two sets of Ethernet MAC. • Supports both half and full duplex for 10 Mbps or 100 Mbps operation. • RMII (Reduced Media Independent Interface) and serial management interface (MDC/MDIO). • Pause and remote pause function for flow control. • Long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception. • CAM function for Ethernet MAC address recognition. • Supports Magic Packet recognition to wake system up from Power-down mode. • Built-in DMA.
CMOS Sensor Interface	• Two sets of CMOS sensor interfaces supporting CCIR601 and CCIR656 type sensor. • Resolution up to 3M pixels. • Supports YUV422 and RGB565 color format for data output by CMOS image sensor. • Supports YUV422, RGB565, RGB555 and Y-only color format with planar and packet data format for data storing to system memory. • Supports image cropping and cropping window up to 4096x2048. • Supports vertical and horizontal scaling-down with N/M scaling factor. • Supports Negative, Sepia and Posterization color effects
Cryptography Accelerator	
Rivest、Shamir and Adleman Cryptography (RSA)	• Hardware RSA accelerator. • Supports both encryption and decryption. • Supports up to 2048 bits.
Elliptic Curve	• Hardware ECC accelerator.

Cryptography (ECC)	• Supports 192-bit and 256-bit key length. • Supports both prime field GF(p) and binary field GF(2m). • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes. • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes. • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes. • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m). • Supports modulus division, multiplication, addition and subtraction operations in GF(p).
Advanced Encryption Standard (AES)	• Hardware AES accelerator. • Supports 128-bit, 192-bit and 256-bit key length and key expander, and compliant with FIPS 197. • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum.
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator. • Supports SHA-160, SHA-224, SHA-256, SHA-384 and SHA-512. • Compliant with FIPS 180/180-2.
keyed-Hash Message Authentication Code (HMAC)	• Hardware HMAC accelerator. • Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512. • Compliant with FIPS 180/180-2.
PRNG	• Supports 64-/128-/192-/256-bit random number generator.

3 PARTS INFORMATION

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1 Package Type

Part No.	LQFP64-EP	LQFP128	LQFP216
NUC980	NUC980DRxxYC	NUC980DKxxYC	NUC980DFxxYC

Figure 3-1 NUC980 Series Package Type

3.2 NUC980 Series Part Selection Guide

Part Number		NUC980				
		DF71YC	DK71YC	DF63YC	DK63YC	DR63YC
DDR Size(MB)		128	128	64	64	64
I/O		104	92	104	92	40
32-bit Timer		6	6	6	6	6
RTC		√	√	√	√	-
Connectivity	UART	10	10	10	10	8
	ISO-7816	2	2	2	2	2
	Quad SPI	1	1	1	1	0
	SPI	2	2	2	2	2
	I²S	1	1	1	1	1
	I²C	4	4	4	4	2
	CAN	4	4	4	4	2
	SDHC/SDIO	2	2	2	2	1* (storage only)
Crypto	PRNG 256	√	√	√	√	√
	AES 256	√	√	√	√	√
	RSA 2048	√	√	√	√	√
	ECC	√	√	√	√	√
	HMAC SHA 512	√	√	√	√	√
	SHA 512	√	√	√	√	√
External Bus Interface		√	√	√	√	-
Camera Interface		2	2	2	2	1
SPI NOR/NAND		√	√	√	√	SPI NOR only
NAND Flash Interface		√	√	√	√	√
16-bit PWM		8	8	8	8	5
10/100Mb Ethernet MAC		2	2	2	2	1
USB 1.1 FS Host Lite		6	6	6	6	6
USB 2.0 HS Host		1	1	1	1	-
USB 2.0 HS Host / Device		1	1	1	1	1
12-bit ADC		8	8	8	8	2
Package		LQFP216	LQFP128	LQFP216	LQFP128	LQFP64-EP

Table 3.2-1 NUC980 Series Part Selection Guide

3.3 NUC980 Series Naming Rule

NUC	9	80	D	K	6	1	Y	C
Nuvoton MCU	Core	Series	Package	Pin count	SDRAM Size	Vonder ID	PB Free	Support CAN
	ARM 926		D: LQFP	K: 128 pin	7: 128MB			C: CAN
				F: 216 pin	6: 64MB			N/A: Non CAN
				R: 64 pin				

Figure 3.3-1 NUC980 Series Selection Code

4 PIN CONFIGURATION

4.1 Pin Configuration

4.1.1 NUC980DRxxYx LQFP64-EP Pin Diagram

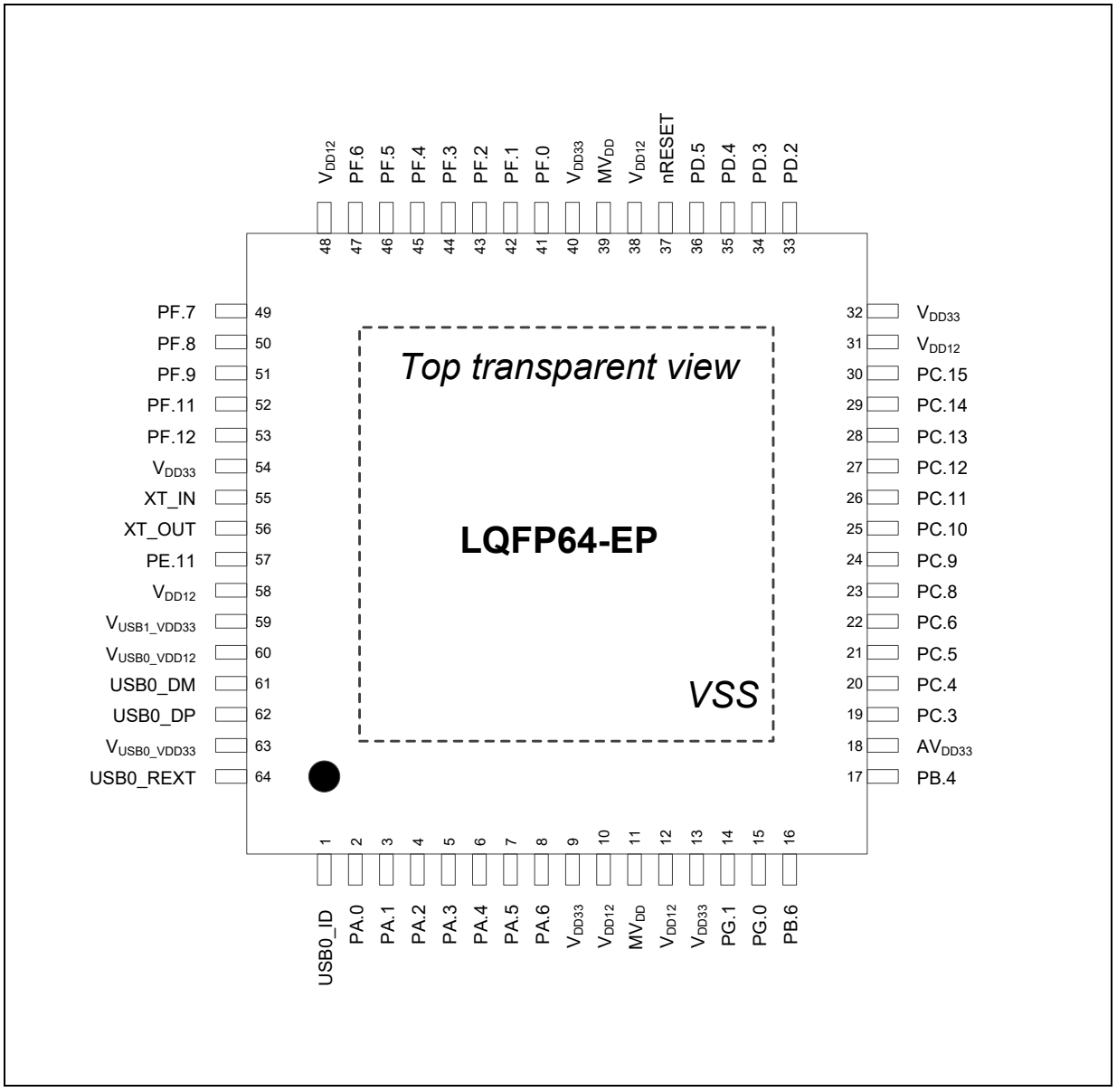


Figure 4.1-1 NUC980DRxxYx LQFP 64-pin with EX-PAD Diagram

4.1.2 NUC980DKxxYx LQFP128 Pin Diagram

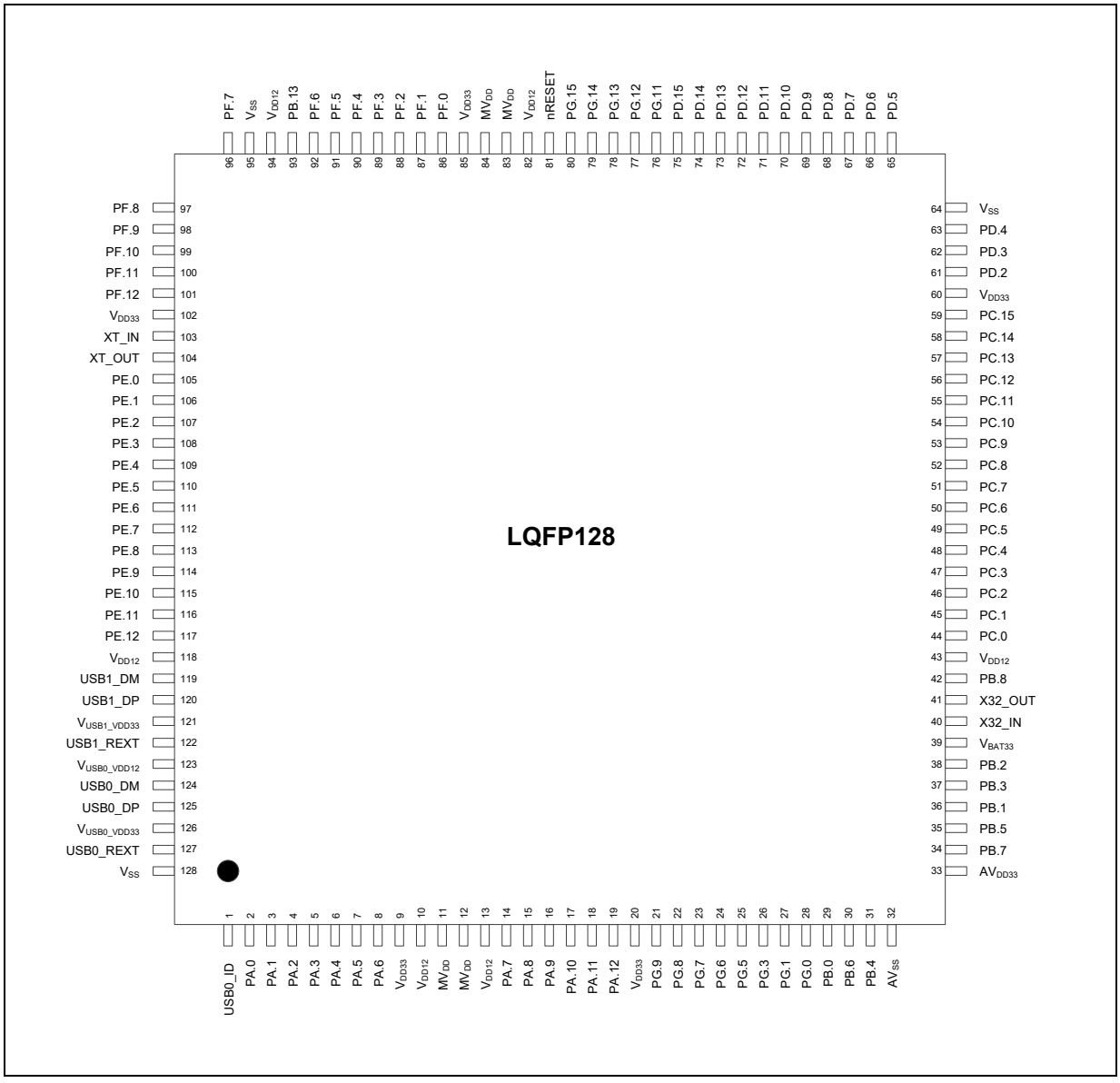


Figure 4.1-2 NUC980DKxxYx LQFP 128-pin Diagram

4.1.3 NUC980DFxxYx LQFP216 Pin Diagram

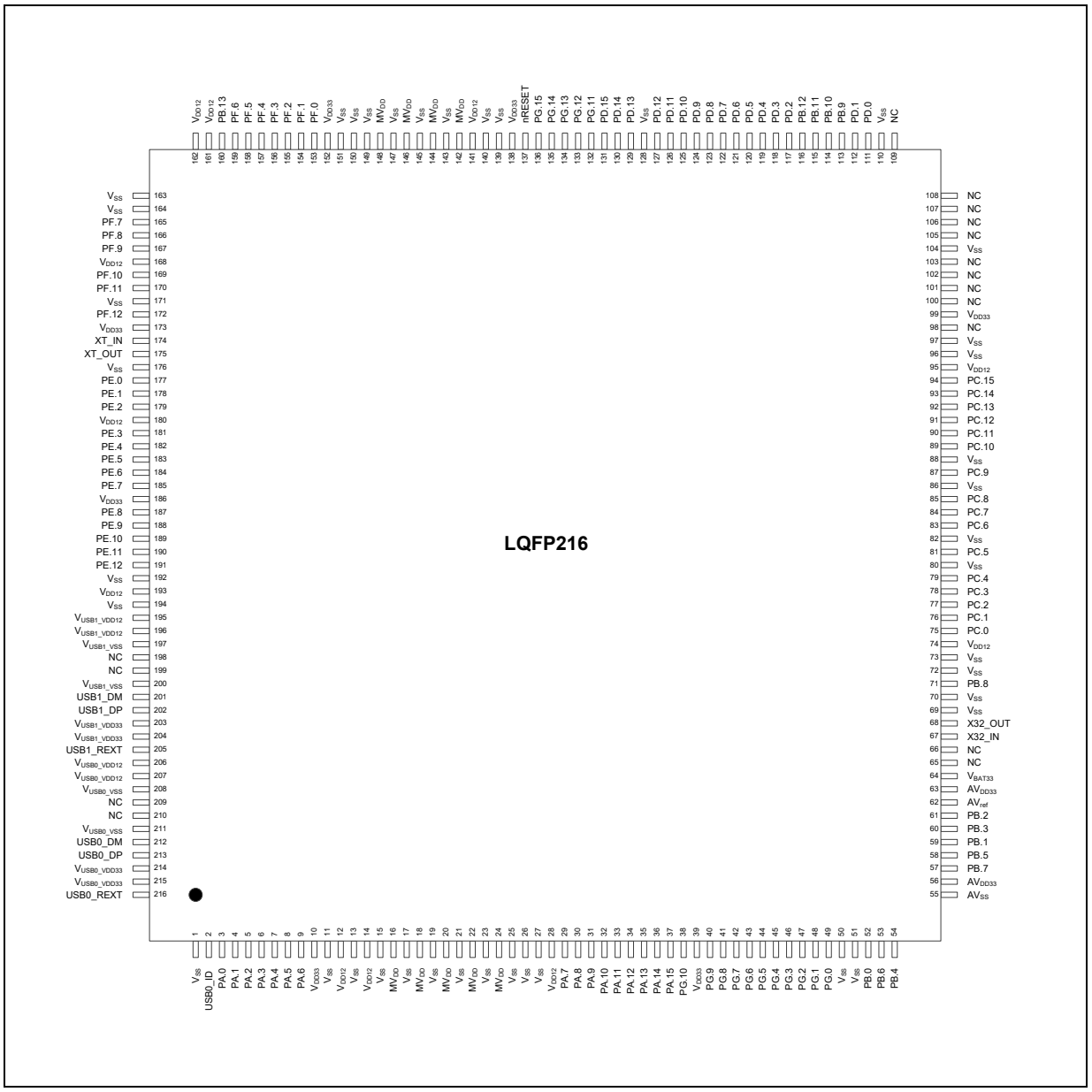


Figure 4.1-3 NUC980DFxxYx LQFP 216-pin Diagram

4.2 Pin Description

4.2.1 NUC980 Pin Description

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		1	V_{SS}	P	MFP0	Ground pin for digital circuit
1	1	2	USB0_ID	IU	-	USB0 Host/Device identification with an internal pull-up 1: Device (default) 0: Host
2	2	3	PA.0	I/O	MFP0	General purpose digital I/O pin
			QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin
			I2C0_SDA	I/O	MFP3	I^2C0 data input/output pin
			UART1_RXD	I	MFP4	UART1 data receiver input pin
			EINT0	I	MFP5	External interrupt 0 input pin
			TM0_ECNT	I/O	MFP6	Timer0 event counter input/toggle output pin
			CAN3_RXD	I	MFP7	CAN3 bus receiver input
3	3	4	PA.1	I/O	MFP0	General purpose digital I/O pin
			EBI_nCS2	O	MFP1	EBI chip select 2 output pin
			EBI_MCLK	O	MFP2	EBI external clock output pin
			I2C0_SCL	I/O	MFP3	I^2C0 clock pin
			UART1_TXD	O	MFP4	UART1 data transmitter output pin
			EINT1	I	MFP5	External interrupt 1 input pin
			TM1_ECNT	I/O	MFP6	Timer1 event counter input/toggle output pin
			CAN3_TXD	O	MFP7	CAN3 bus transmitter output
4	4	5	PA.2	I/O	MFP0	General purpose digital I/O pin
			UART6_CTS	I	MFP1	UART6 clear to Send input pin
			I2S_LRCK	O	MFP2	I^2S left right channel clock output pin
			SC0_CD	I	MFP3	Smart Card 0 card detect pin
			JTAG1_TDO	O	MFP4	JTAG1 data output pin
			TM2_ECNT	I/O	MFP6	Timer2 event counter input/toggle output pin
5	5	6	PA.3	I/O	MFP0	General purpose digital I/O pin
			UART6_RTS	O	MFP1	UART6 request to Send output pin
			I2S_BCLK	O	MFP2	I^2S bit clock output pin
			SC0_PWR	O	MFP3	Smart Card 0 power pin
			JTAG1_TCK	I	MFP4	JTAG1 clock input pin
			TM3_ECNT	I/O	MFP6	Timer3 event counter input/toggle output pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
6	6	7	PA.4	I/O	MFP0	General purpose digital I/O pin
			UART6_RXD	I	MFP1	UART6 data receiver input pin
			I2S_DI	I	MFP2	I^2S data input pin
			SC0_DAT	I/O	MFP3	Smart Card 0 data pin
			JTAG1_TMS	I	MFP4	JTAG1 test mode selection input pin
			TM4_ECNT	I/O	MFP6	Timer4 event counter input/toggle output pin
7	7	8	PA.5	I/O	MFP0	General purpose digital I/O pin
			UART6_TXD	O	MFP1	UART6 data transmitter output pin
			I2S_DO	O	MFP2	I^2S data output pin
			SC0_CLK	O	MFP3	Smart Card 0 clock pin
			JTAG1_TDI	I	MFP4	JTAG1 data input pin
			TM5_ECNT	I/O	MFP6	Timer5 event counter input/toggle output pin
8	8	9	PA.6	I/O	MFP0	General purpose digital I/O pin
			EBI_nCS1	O	MFP1	EBI chip select 1 output pin
			I2S_MCLK	O	MFP2	I^2S master clock output pin
			SC0_RST	O	MFP3	Smart Card 0 reset pin
			JTAG1_nTRST	I	MFP4	JTAG1 reset input pin
9	9	10	V_{DD33}	P	MFP0	Power supply for I/O power pin
		11	V_{SS}	P	MFP0	Ground pin for digital circuit
10	10	12	V_{DD12}	P	MFP0	Power supply for Internal core power pin
		13	V_{SS}	P	MFP0	Ground pin for digital circuit
		14	V_{DD12}	P	MFP0	Power supply for Internal core power pin
		15	V_{SS}	P	MFP0	Ground pin for digital circuit
11	11	16	MV_{DD}	P	MFP0	Power supply for Memory ports
		17	V_{SS}	P	MFP0	Ground pin for digital circuit
		18	MV_{DD}	P	MFP0	Power supply for Memory ports
		19	V_{SS}	P	MFP0	Ground pin for digital circuit
		20	MV_{DD}	P	MFP0	Power supply for Memory ports
		21	V_{SS}	P	MFP0	Ground pin for digital circuit
	12	22	MV_{DD}	P	MFP0	Power supply for Memory ports
		23	V_{SS}	P	MFP0	Ground pin for digital circuit
		24	MV_{DD}	P	MFP0	Power supply for Memory ports
		25	V_{SS}	P	MFP0	Ground pin for digital circuit

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		26	V_{SS}	P	MFP0	Ground pin for digital circuit
		27	V_{SS}	P	MFP0	Ground pin for digital circuit
12	13	28	V_{DD12}	P	MFP0	Power supply for Internal core power pin
	14	29	PA.7	I/O	MFP0	General purpose digital I/O pin
			EBI_nWE	O	MFP1	EBI write enable output pin
			UART2_CTS	I	MFP2	UART2 clear to Send input pin
			TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin
	15	30	PA.8	I/O	MFP0	General purpose digital I/O pin
			EBI_nRE	O	MFP1	EBI read enable output pin
			UART2_RTS	O	MFP2	UART2 request to Send output pin
			TM3_TGL	I/O	MFP3	Timer3 event counter input/toggle output pin
	16	31	PA.9	I/O	MFP0	General purpose digital I/O pin
			EBI_nCS0	O	MFP1	EBI chip select 0 output pin
			UART2_RXD	I	MFP2	UART2 data receiver input pin
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin
	17	32	PA.10	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR10	O	MFP1	EBI address bus bit 10
			UART2_TXD	O	MFP2	UART2 data transmitter output pin
			TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin
	18	33	PA.11	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR9	O	MFP1	EBI address bus bit 9
			UART8_RXD	I	MFP2	UART8 data receiver input pin
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin
	19	34	PA.12	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR8	O	MFP1	EBI address bus bit 8
			UART8_TXD	O	MFP2	UART8 data transmitter output pin
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
		35	PA.13	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR13	O	MFP1	EBI address bus bit 13
			I2C1_SDA	I/O	MFP2	I^2C1 data input/output pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
			USBHL5_DM	A	MFP4	USB 1.1 host lite port 5 differential signal D-
			CAN1_RXD	I	MFP5	CAN1 bus receiver input

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART7_TXD	O	MFP6	UART7 data transmitter output pin
			PWM03	O	MFP7	PWM03 counter synchronous trigger output pin
			EINT0	I	MFP8	External interrupt 0 input pin
		36	PA.14	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR14	O	MFP1	EBI address bus bit 14
			I2C1_SCL	I/O	MFP2	I^2C1 clock pin
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
			USBHL5_DP	A	MFP4	USB 1.1 host lite port 5 differential signal D+
			CAN1_TXD	O	MFP5	CAN1 bus transmitter output
			UART7_RXD	I	MFP6	UART7 data receiver input pin
			PWM02	O	MFP7	PWM02 counter synchronous trigger output pin
			EINT1	I	MFP8	External interrupt 1 input pin
		37	PA.15	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR19	O	MFP1	EBI address bus bit 19
			I2C0_SDA	I/O	MFP2	I^2C0 data input/output pin
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
			USBHL4_DM	A	MFP4	USB 1.1 host lite port 4 differential signal D-
			CAN2_RXD	I	MFP5	CAN2 bus receiver input
			SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin
			PWM01	O	MFP7	PWM01 counter synchronous trigger output pin
			I2S_LRCK	O	MFP8	I^2S left right channel clock output pin
		38	PG.10	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA0	I/O	MFP1	EBI data bus bit 0
			I2C0_SCL	I/O	MFP2	I^2C0 clock pin
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin
			USBHL4_DP	A	MFP4	USB 1.1 host lite port 4 differential signal D+
			CAN2_TXD	O	MFP5	CAN2 bus transmitter output
			SPI1_CLK	I/O	MFP6	SPI1 serial clock pin
			PWM00	O	MFP7	PWM00 counter synchronous trigger output pin
			I2S_BCLK	O	MFP8	I^2S bit clock output pin
13	20	39	V_{DD33}	P	MFP0	Power supply for I/O power pin
	21	40	PG.9	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR7	O	MFP1	EBI address bus bit 7

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART8_CTS	I	MFP2	UART8 clear to Send input pin
			PWM13	O	MFP6	PWM13 counter synchronous trigger output pin
			CFG.9_PwrOnSet9	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	22	41	PG.8	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR6	O	MFP1	EBI address bus bit 6
			UART8_RTS	O	MFP2	UART8 request to Send output pin
			PWM12	O	MFP6	PWM12 counter synchronous trigger output pin
			CFG.8_PwrOnSet8	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	23	42	PG.7	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR5	O	MFP1	EBI address bus bit 5
			UART5_TXD	O	MFP2	UART5 data transmitter output pin
			PWM11	O	MFP6	PWM11 counter synchronous trigger output pin
			CFG.7_PwrOnSet7	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	24	43	PG.6	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR4	O	MFP1	EBI address bus bit 4
			UART5_RXD	I	MFP2	UART5 data receiver input pin
			PWM10	O	MFP6	PWM10 counter synchronous trigger output pin
			CFG.6_PwrOnSet6	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	25	44	PG.5	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR12	O	MFP1	EBI address bus bit 12
			UART5_RTS	O	MFP2	UART5 request to Send output pin
			CFG.5_PwrOnSet5	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		45	PG.4	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR18	O	MFP1	EBI address bus bit 18
			UART5_CTS	I	MFP2	UART5 clear to Send input pin
			CFG.4_PwrOnSet4	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
	26	46	PG.3	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR3	O	MFP1	EBI address bus bit 3
			UART2_RTS	O	MFP2	UART2 request to Send output pin
			PWM03	O	MFP6	PWM03 counter synchronous trigger output pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			CFG.3_PwrOnSet3	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		47	PG.2	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR2	O	MFP1	EBI address bus bit 2
			UART2_CTS	I	MFP2	UART2 clear to Send input pin
			PWM02	O	MFP6	PWM02 counter synchronous trigger output pin
			CFG.2_PwrOnSet2	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
14	27	48	PG.1	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR1	O	MFP1	EBI address bus bit 1
			UART2_TXD	O	MFP2	UART2 data transmitter output pin
			PWM01	O	MFP6	PWM01 counter synchronous trigger output pin
			CFG.1_PwrOnSet1	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
15	28	49	PG.0	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR0	O	MFP1	EBI address bus bit 0
			UART2_RXD	I	MFP2	UART2 data receiver input pin
			CLK_OUT	O	MFP3	Internal clock selection output pin
			PWM00	O	MFP6	PWM00 counter synchronous trigger output pin
			CFG.0_PwrOnSet0	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
		50	V_{SS}	P	MFP0	Ground pin for digital circuit
		51	V_{SS}	P	MFP0	Ground pin for digital circuit
	29	52	PB.0	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR12	O	MFP1	EBI address bus bit 12
			UART2_CTS	I	MFP2	UART2 clear to Send input pin
			ADC_AIN0	A	MFP8	ADC channel 0 analog input
16	30	53	PB.6	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR13	O	MFP1	EBI address bus bit 13
			I2C1_SDA	I/O	MFP2	I^2C1 data input/output pin
			I2S_LRCK	O	MFP3	I^2S left right channel clock output pin
			USBHL0_DM	A	MFP4	USB 1.1 host lite port 0 differential signal D-
			UART7_TXD	O	MFP5	UART7 data transmitter output pin
			SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin
			ADC_AIN6	A	MFP8	ADC channel 6 analog input

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
17	31	54	PB.4	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR14	O	MFP1	EBI address bus bit 14
			I2C1_SCL	I/O	MFP2	I^2C1 clock pin
			I2S_BCLK	O	MFP3	I^2S bit clock output pin
			USBHL0_DP	A	MFP4	USB 1.1 host lite port 0 differential signal D+
			UART7_RXD	I	MFP5	UART7 data receiver input pin
			SPI1_CLK	I/O	MFP6	SPI1 serial clock pin
			ADC_AIN4	A	MFP8	ADC channel 4 analog input
	32	55	AV_{SS}	P	MFP0	Ground pin for analog SAR-ADC
18	33	56	AV_{DD33}	P	MFP0	Power supply for analog SAR-ADC, DC3.3V
	34	57	PB.7	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR15	O	MFP1	EBI address bus bit 15
			I2C2_SDA	I/O	MFP2	I^2C2 data input/output pin
			I2S_DI	I	MFP3	I^2S data input pin
			USBHL0_DM	A	MFP4	USB 1.1 host lite port 0 differential signal D-
			UART7_CTS	I	MFP5	UART7 clear to Send input pin
			SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin
			ADC_AIN7	A	MFP8	ADC channel 7 analog input
	35	58	PB.5	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR16	O	MFP1	EBI address bus bit 16
			I2C2_SCL	I/O	MFP2	I^2C2 clock pin
			I2S_DO	O	MFP3	I^2S data output pin
			USBHL0_DP	A	MFP4	USB 1.1 host lite port 0 differential signal D+
			UART7_RTS	O	MFP5	UART7 request to Send output pin
			SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin
			ADC_AIN5	A	MFP8	ADC channel 5 analog input
	36	59	PB.1	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR17	O	MFP1	EBI address bus bit 17
			I2C3_SDA	I/O	MFP2	I^2C3 data input/output pin
			I2S_MCLK	O	MFP3	I^2S master clock output pin
			CAN2_RXD	I	MFP4	CAN2 bus receiver input
			TM0_EXT	I/O	MFP5	Timer0 external capture input/toggle output pin
			SPI1_SS1	I/O	MFP6	SPI1 slave select 1 pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART9_TXD	O	MFP7	UART9 data transmitter output pin
			ADC_AIN1	A	MFP8	ADC channel 1 analog input
	37	60	PB.3	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR18	O	MFP1	EBI address bus bit 18
			I2C3_SCL	I/O	MFP2	I^2C3 clock pin
			EINT2	I	MFP3	External interrupt 2 input pin
			CAN2_TXD	O	MFP4	CAN2 bus transmitter output
			TM0_TGL	I/O	MFP5	Timer0 event counter input/toggle output pin
			SPI0_SS1	I/O	MFP6	SPI0 slave select 1 pin
			UART9_RXD	I	MFP7	UART9 data receiver input pin
			ADC_AIN3	A	MFP8	ADC channel 3 analog input
	38	61	PB.2	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR2	O	MFP1	EBI address bus bit 2
			UART9_RTS	O	MFP7	UART9 request to Send output pin
			ADC_AIN2	A	MFP8	ADC channel 2 analog input
		62	AV_{ref}	A	MFP0	ADC reference voltage input
		63	AV_{DD33}	P	MFP0	Power supply for analog SAR-ADC, DC 3.3V
	39	64	V_{BAT33}	P	MFP0	Power supply by batteries for RTC
		65	NC	-		No connect
		66	NC	-		No connect
	40	67	X32_IN	I	MFP0	External 32.768 kHz crystal input pin
	41	68	X32_OUT	O	MFP0	External 32.768 kHz crystal output pin
		69	V_{SS}	P	MFP0	Ground pin for digital circuit
		70	V_{SS}	P	MFP0	Ground pin for digital circuit
	42	71	PB.8	I/O	MFP0	General purpose digital I/O pin
			EBI_ADDR11	O	MFP1	EBI address bus bit 11
			I2C2_SCL	I/O	MFP2	I^2C2 clock pin
			CAN2_RXD	I	MFP3	CAN2 bus receiver input
			UART8_TXD	O	MFP4	UART8 data transmitter output pin
			SD0_nCD	I	MFP6	SD0 card detect input pin
			TM0_EXT	I/O	MFP7	Timer0 external capture input/toggle output pin
		72	V_{SS}	P	MFP0	Ground pin for digital circuit
		73	V_{SS}	P	MFP0	Ground pin for digital circuit

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
	43	74	V_{DD12}	P	MFP0	Power supply Internal core power pin
	44	75	PC.0	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA0	I/O	MFP1	EBI data bus bit 0
			I2C2_SDA	I/O	MFP2	I^2C2 data input/output pin
			CAN2_TXD	O	MFP3	CAN2 bus transmitter output
			UART8_RXD	I	MFP4	UART8 data receiver input pin
			SPI0_SS1	I/O	MFP5	SPI0 slave select 1 pin
			TM0_TGL	I/O	MFP7	Timer0 event counter input/toggle output pin
	45	76	PC.1	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA1	I/O	MFP1	EBI data bus bit 1
			NAND_nCS0	O	MFP3	NAND flash chip enable input
			UART7_TXD	O	MFP4	UART7 data transmitter output pin
	46	77	PC.2	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA2	I/O	MFP1	EBI data bus bit 2
			NAND_nWP	O	MFP3	NAND flash write protect input
			UART7_RXD	I	MFP4	UART7 data receiver input pin
19	47	78	PC.3	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA3	I/O	MFP1	EBI data bus bit 3
			VCAP0_CLKO	O	MFP2	Video image interface 0 sensor clock pin
			NAND_ALE	O	MFP3	NAND flash address latch enable
			I2C1_SCL	I/O	MFP4	I^2C1 clock pin
			UART3_TXD	O	MFP5	UART3 data transmitter output pin
			CAN0_RXD	I	MFP7	CAN0 bus receiver input
20	48	79	PC.4	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA4	I/O	MFP1	EBI data bus bit 4
			VCAP0_PCLK	I	MFP2	Video image interface 0 pixel clock pin
			NAND_CLE	O	MFP3	NAND flash command latch enable
			I2C1_SDA	I/O	MFP4	I^2C1 data input/output pin
			UART3_RXD	I	MFP5	UART3 data receiver input pin
			SPI0_MOSI	I/O	MFP6	SPI0 MOSI (Master Out, Slave In) pin
			CAN0_TXD	O	MFP7	CAN0 bus transmitter outpu
		80	V_{SS}	P	MFP0	Ground pin for digital circuit
21	49	81	PC.5	I/O	MFP0	General purpose digital I/O pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			EBI_DATA5	I/O	MFP1	EBI data bus bit 5
			VCAP0_HSYNC	I	MFP2	Video image interface 0 horizontal sync. Pin
			NAND_nWE	O	MFP3	NAND flash write enable
			SPI0_SS0	I/O	MFP5	SPI0 slave select 0 pin
			SD0_CMD/ eMMC0_CMD	I/O	MFP6	SD0 command/response pin eMMC0 command/response pin
			UART1_TXD	O	MFP7	UART1 data transmitter output pin
		82	V_{SS}	P	MFP0	Ground pin for digital circuit
22	50	83	PC.6	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA6	I/O	MFP1	EBI data bus bit 6
			VCAP0_VSYNC	I	MFP2	Video image interface 0 vertical sync. Pin
			NAND_nRE	O	MFP3	NAND flash read enable
			SC1_RST	O	MFP4	Smart Card 1 reset pin
			SPI0_CLK	I/O	MFP5	SPI0 serial clock pin
			SD0_CLK/ eMMC0_CLK	O	MFP6	SD0 clock output pin eMMC0 clock output pin
			UART1_RXD	I	MFP7	UART1 data receiver input pin
	51	84	PC.7	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA7	I/O	MFP1	EBI data bus bit 7
			VCAP0_FIELD	I	MFP2	Video image interface 0 frame sync. Pin
			NAND_RDY0	I	MFP3	NAND flash ready/busy input
			SC1_CLK	O	MFP4	Smart Card 1 clock pin
			SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin
			SD0_DATA0/ eMMC0_DATA0	I/O	MFP6	SD0 data line bit 0 eMMC0 data line bit 0
			UART1_RTS	O	MFP7	UART1 request to Send output pin
23	52	85	PC.8	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA8	I/O	MFP1	EBI data bus bit 8
			VCAP0_DATA0	I	MFP2	Video image interface 0 data 0 pin
			NAND_DATA0	I/O	MFP3	NAND flash data bus bit 0
			SC1_DAT	I/O	MFP4	Smart Card 1 data pin
			SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin
			SD0_DATA1/	I/O	MFP6	SD0 data line bit 1

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			eMMC0_DATA1			eMMC0 data line bit 1
			UART1_CTS	I	MFP7	UART1 clear to Send input pin
		86	V_{SS}	P	MFP0	Ground pin for digital circuit
24	53	87	PC.9	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA9	I/O	MFP1	EBI data bus bit 9
			VCAP0_DATA1	I	MFP2	Video image interface 0 data 1 pin
			NAND_DATA1	I/O	MFP3	NAND flash data bus bit 1
			SC1_PWR	O	MFP4	Smart Card 1 power pin
			SD0_DATA2/ eMMC0_DATA2	I/O	MFP6	SD0 data line bit 2 eMMC0 data line bit 2
			UART4_TXD	O	MFP7	UART4 data transmitter output pin
		88	V_{SS}	P	MFP0	Ground pin for digital circuit
25	54	89	PC.10	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA10	I/O	MFP1	EBI data bus bit 10
			VCAP0_DATA2	I	MFP2	Video image interface 0 data 2 pin
			NAND_DATA2	I/O	MFP3	NAND flash data bus bit 2
			SC1_CD	I	MFP4	Smart Card 1 card detect pin
			SD0_DATA3/ eMMC0_DATA3	I/O	MFP6	SD0 data line bit 3 eMMC0 data line bit 3
			UART4_RXD	I	MFP7	UART4 data receiver input pin
26	55	90	PC.11	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA11	I/O	MFP1	EBI data bus bit 11
			VCAP0_DATA3	I	MFP2	Video image interface 0 data 3 pin
			NAND_DATA3	I/O	MFP3	NAND flash data bus bit 3
			SC0_RST	O	MFP4	Smart Card 0 reset pin
27	56	91	PC.12	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA12	I/O	MFP1	EBI data bus bit 12
			VCAP0_DATA4	I	MFP2	Video image interface 0 data 4 pin
			NAND_DATA4	I/O	MFP3	NAND flash data bus bit 4
			SC0_CLK	O	MFP4	Smart Card 0 clock pin
			SD0_nCD	I	MFP6	SD0 card detect input pin
			UART8_TXD	O	MFP7	UART8 data transmitter output pin
28	57	92	PC.13	I/O	MFP0	General purpose digital I/O pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			EBI_DATA13	I/O	MFP1	EBI data bus bit 13
			VCAP0_DATA5	I	MFP2	Video image interface 0 data 5 pin
			NAND_DATA5	I/O	MFP3	NAND flash data bus bit 5
			SC0_DAT	I/O	MFP4	Smart Card 0 data pin
			UART8_RXD	I	MFP7	UART8 data receiver input pin
29	58	93	PC.14	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA14	I/O	MFP1	EBI data bus bit 14
			VCAP0_DATA6	I	MFP2	Video image interface 0 data 6 pin
			NAND_DATA6	I/O	MFP3	NAND flash data bus bit 6
			SC0_PWR	O	MFP4	Smart Card 0 power pin
			SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin
			UART8_RTS	O	MFP7	UART8 request to Send output pin
30	59	94	PC.15	I/O	MFP0	General purpose digital I/O pin
			EBI_DATA15	I/O	MFP1	EBI data bus bit 15
			VCAP0_DATA7	I	MFP2	Video image interface 0 data 7 pin
			NAND_DATA7	I/O	MFP3	NAND flash date bus bit 7
			SC0_CD	I	MFP4	Smart Card 0 card detect pin
			UART8_CTS	I	MFP7	UART8 clear to Send input pin
31		95	V_{DD12}	P	MFP0	Power supply for Internal core power pin
		96	V_{SS}	P	MFP0	Ground pin for digital circuit
		97	V_{SS}	P	MFP0	Ground pin for digital circuit
		98	NC	-		No connect
32	60	99	V_{DD33}	P	MFP0	Power supply for I/O power pin
		100	NC	-		No connect
		101	NC	-		No connect
		102	NC	-		No connect
		103	NC	-		No connect
		104	V_{SS}	P	MFP0	Ground pin for digital circuit
		105	NC	-		No connect
		106	NC	-		No connect
		107	NC	-		No connect
		108	NC	-		No connect
		109	NC	-		No connect

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		110	V_{SS}	P	MFP0	Ground pin for digital circuit
		111	PD.0	I/O	MFP0	General purpose digital I/O pin
			QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin
			UART5_TXD	O	MFP2	UART5 data transmitter output pin
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
			EINT2	I	MFP4	External interrupt 2 input pin
		112	PD.1	I/O	MFP0	General purpose digital I/O pin
			SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin
			UART5_RXD	I	MFP2	UART5 data receiver input pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
			EINT3	I	MFP4	External interrupt 3 input pin
		113	PB.9	I/O	MFP0	General purpose digital I/O pin
			UART3_TXD	O	MFP1	UART3 data transmitter output pin
			PWM13	O	MFP2	PWM13 counter synchronous trigger output pin
			TM0_TGL	I/O	MFP3	Timer0 event counter input/toggle output pin
			USBHL0_DM	A	MFP4	USB 1.1 host lite port 0 differential signal D-
			SPI1_SS0	I/O	MFP5	SPI1 slave select 0 pin
		114	PB.10	I/O	MFP0	General purpose digital I/O pin
			UART3_RXD	I	MFP1	UART3 data receiver input pin
			PWM12	O	MFP2	PWM12 counter synchronous trigger output pin
			TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin
			USBHL0_DP	A	MFP4	USB 1.1 host lite port 0 differential signal D+
			SPI1_CLK	I/O	MFP5	SPI1 serial clock pin
		115	PB.11	I/O	MFP0	General purpose digital I/O pin
			UART3_RTS	O	MFP1	UART3 request to Send output pin
			PWM11	O	MFP2	PWM11 counter synchronous trigger output pin
			TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin
			USBHL5_DM	A	MFP4	USB 1.1 host lite port 5 differential signal D-
			SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin
		116	PB.12	I/O	MFP0	General purpose digital I/O pin
			UART3_CTS	I	MFP1	UART3 clear to Send input pin
			PWM10	O	MFP2	PWM10 counter synchronous trigger output pin
			TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			USBHL5_DP	A	MFP4	USB 1.1 host lite port 5 differential signal D+
			SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin
33	61	117	PD.2	I/O	MFP0	General purpose digital I/O pin
			QSPI0_SS0	I/O	MFP1	Quad SPI0 slave select 0 pin.(booting)
			UART3_TXD	O	MFP2	UART3 data transmitter output pin
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin
34	62	118	PD.3	I/O	MFP0	General purpose digital I/O pin
			QSPI0_CLK	I/O	MFP1	Quad SPI0 serial clock pin.(booting)
			UART3_RXD	I	MFP2	UART3 data receiver input pin
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
35	63	119	PD.4	I/O	MFP0	General purpose digital I/O pin
			QSPI0_MOSI0	I/O	MFP1	Quad SPI0 MOSI0 (Master Out, Slave In) pin. Data 0 of quad mode.(booting)
			UART3_RTS	O	MFP2	UART3 request to Send output pin
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
	64		V_{SS}	P	MFP0	Ground pin for digital circuit
36	65	120	PD.5	I/O	MFP0	General purpose digital I/O pin
			QSPI0_MISO0	I/O	MFP1	Quad SPI0 MISO0 (Master In, Slave Out) pin. Data 1 of quad mode.(booting)
			UART3_CTS	I	MFP2	UART3 clear to Send input pin
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin
	66	121	PD.6	I/O	MFP0	General purpose digital I/O pin
			QSPI0_MOSI1	I/O	MFP1	Quad SPI0 MOSI1 (Master Out, Slave In) pin. Data 2 of quad mode.(booting)
			UART2_TXD	O	MFP2	UART2 data transmitter output pin
			TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin
			CAN0_RXD	I	MFP4	CAN0 bus receiver input
	67	122	PD.7	I/O	MFP0	General purpose digital I/O pin
			QSPI0_MISO1	I/O	MFP1	Quad SPI0 MISO1 (Master In, Slave Out) pin. Data 3 of quad mode.(booting)
			UART2_RXD	I	MFP2	UART2 data receiver input pin
			TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin
			CAN0_TXD	O	MFP4	CAN0 bus transmitter output
	68	123	PD.8	I/O	MFP0	General purpose digital I/O pin
			SPI0_SS0	I/O	MFP1	SPI0 slave select 0 pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART6_CTS	I	MFP2	UART6 clear to Send input pin
			TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin
	69	124	PD.9	I/O	MFP0	General purpose digital I/O pin
			SPI0_CLK	I/O	MFP1	SPI0 serial clock pin
			UART6_RTS	O	MFP2	UART6 request to Send output pin
			TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin
	70	125	PD.10	I/O	MFP0	General purpose digital I/O pin
			SPI0_MOSI	I/O	MFP1	SPI0 MOSI (Master Out, Slave In) pin
			UART6_TXD	O	MFP2	UART6 data transmitter output pin
			TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin
	71	126	PD.11	I/O	MFP0	General purpose digital I/O pin
			SPI0_MISO	I/O	MFP1	SPI0 MISO (Master In, Slave Out) pin
			UART6_RXD	I	MFP2	UART6 data receiver input pin
			TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin
	72	127	PD.12	I/O	MFP0	General purpose digital I/O pin
			UART4_TXD	O	MFP1	UART4 data transmitter output pin
			TM2_TGL	I/O	MFP2	Timer2 event counter input/toggle output pin
			CAN2_RXD	I	MFP4	CAN2 bus receiver input
			PWM00	O	MFP6	PWM00 counter synchronous trigger output pin
			EBI_DATA1	I/O	MFP8	EBI data bus bit 1
		128	V_{SS}	P	MFP0	Ground pin for digital circuit
	73	129	PD.13	I/O	MFP0	General purpose digital I/O pin
			UART4_RXD	I	MFP1	UART4 data receiver input pin
			TM2_EXT	I/O	MFP2	Timer2 external capture input/toggle output pin
			CAN2_TXD	O	MFP4	CAN2 bus transmitter output
			PWM01	O	MFP6	PWM01 counter synchronous trigger output pin
			EBI_DATA2	I/O	MFP8	EBI data bus bit 2
	74	130	PD.14	I/O	MFP0	General purpose digital I/O pin
			UART4_RTS	O	MFP1	UART4 request to Send output pin
			TM3_TGL	I/O	MFP2	Timer3 event counter input/toggle output pin
			I2C3_SCL	I/O	MFP3	I^2C3 clock pin
			CAN1_RXD	I	MFP4	CAN1 bus receiver input
			USBHL0_DM	A	MFP5	USB 1.1 host lite port 0 differential signal D-

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			PWM02	O	MFP6	PWM02 counter synchronous trigger output pin
			EBI_DATA3	I/O	MFP8	EBI data bus bit 3
	75	131	PD.15	I/O	MFP0	General purpose digital I/O pin
			UART4_CTS	I	MFP1	UART4 clear to Send input pin
			TM3_EXT	I/O	MFP2	Timer3 external capture input/toggle output pin
			I2C3_SDA	I/O	MFP3	I^2C3 data input/output pin
			CAN1_TXD	O	MFP4	CAN1 bus transmitter output
			USBHL0_DP	A	MFP5	USB 1.1 host lite port 0 differential signal D+
			PWM03	O	MFP6	PWM03 counter synchronous trigger output pin
			EBI_DATA4	I/O	MFP8	EBI data bus bit 4
	76	132	PG.11	I/O	MFP0	General purpose digital I/O pin
			SPI1_SS0	I/O	MFP2	SPI1 slave select 0 pin
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
			CAN0_RXD	I	MFP4	CAN0 bus receiver input
			UART5_CTS	I	MFP5	UART5 clear to Send input pin
			PWM10	O	MFP6	PWM10 counter synchronous trigger output pin
			JTAG0_TDO	O	MFP7	JTAG0 data output pin
	77	133	PG.12	I/O	MFP0	General purpose digital I/O pin
			SPI1_CLK	I/O	MFP2	SPI1 serial clock pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
			CAN0_TXD	O	MFP4	CAN0 bus transmitter output
			UART5_RTS	O	MFP5	UART5 request to Send output pin
			PWM11	O	MFP6	PWM11 counter synchronous trigger output pin
			JTAG0_TCK	I	MFP7	JTAG0 clock input pin
	78	134	PG.13	I/O	MFP0	General purpose digital I/O pin
			SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin
			CAN1_RXD	I	MFP4	CAN1 bus receiver input
			UART5_RXD	I	MFP5	UART5 data receiver input pin
			PWM12	O	MFP6	PWM12 counter synchronous trigger output pin
			JTAG0_TMS	I	MFP7	JTAG0 test mode selection input pin
	79	135	PG.14	I/O	MFP0	General purpose digital I/O pin
			SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin
			CAN1_TXD	O	MFP4	CAN1 bus transmitter output

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART5_TXD	O	MFP5	UART5 data transmitter output pin
			PWM13	O	MFP6	PWM13 counter synchronous trigger output pin
			JTAG0_TDI	I	MFP7	JTAG0 data input pin
	80	136	PG.15	I/O	MFP0	General purpose digital I/O pin
			SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin
			SPI1_SS1	I/O	MFP2	SPI1 slave select 1 pin
			EINT3	I	MFP4	External interrupt 3 input pin
			JTAG0_nTRST	I	MFP7	JTAG0 reset input pin
37	81	137	nRESET	IU	MFP0	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state
			WDT_nRST	O	MFP1	Watch dog timer reset trigger output
		138	V_{DD33}	P	MFP0	Power supply for I/O power pin
		139	V_{SS}	P	MFP0	Ground pin for digital circuit
		140	V_{SS}	P	MFP0	Ground pin for digital circuit
38	82	141	V_{DD12}	P	MFP0	Power supply for internal core power pin
39	83	142	MV_{DD}	P	MFP0	Power supply for Memory ports
		143	V_{SS}	P	MFP0	Ground pin for digital circuit
		144	MV_{DD}	P	MFP0	Power supply for Memory ports
		145	V_{SS}	P	MFP0	Ground pin for digital circuit
	84	146	MV_{DD}	P	MFP0	Power supply for Memory ports
		147	V_{SS}	P	MFP0	Ground pin for digital circuit
		148	MV_{DD}	P	MFP0	Power supply for Memory ports
		149	V_{SS}	P	MFP0	Ground pin for digital circuit
		150	V_{SS}	P	MFP0	Ground pin for digital circuit
		151	V_{SS}	P	MFP0	Ground pin for digital circuit
40	85	152	V_{DD33}	P	MFP0	Power supply for I/O power pin
41	86	153	PF.0	I/O	MFP0	General purpose digital I/O pin
			RMII1_RXERR	I	MFP1	RMII1 Receive Data Error input pin
			SD1_CMD/ eMMC1_CMD	I/O	MFP2	SD1 command/response pin eMMC1 command/response pin
			TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin
			SC1_RST	O	MFP4	Smart Card 1 reset pin
			UART7_CTS	I	MFP5	UART7 clear to Send input pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			USBHL1_DM	A	MFP6	USB 1.1 host lite port 1 differential signal D-
			EBI_DATA5	I/O	MFP8	EBI data bus bit 5
42	87	154	PF.1	I/O	MFP0	General purpose digital I/O pin
			RMII1_CRSDV	I	MFP1	RMII1 Carrier Sense/Receive Data input pin
			SD1_CLK/ eMMC1_CLK	O	MFP2	SD1 clock output pin eMMC1 clock output pin
			TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin
			SC1_CLK	O	MFP4	Smart Card 1 clock pin
			UART7_RTS	O	MFP5	UART7 request to Send output pin
			USBHL1_DP	A	MFP6	USB 1.1 host lite port 1 differential signal D+
			EBI_DATA6	I/O	MFP8	EBI data bus bit 6
43	88	155	PF.2	I/O	MFP0	General purpose digital I/O pin
			RMII1_RXD1	I	MFP1	RMII1 Receive Data bus bit 1
			SD1_DATA0/ eMMC1_DATA0	I/O	MFP2	SD1 data line bit 0 eMMC1 data line bit 0
			TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin
			SC1_DAT	I/O	MFP4	Smart Card 1 data pin
			UART7_RXD	I	MFP5	UART7 data receiver input pin
			USBHL2_DM	A	MFP6	USB 1.1 host lite port 2 differential signal D-
			EBI_DATA7	I/O	MFP8	EBI data bus bit 7
44	89	156	PF.3	I/O	MFP0	General purpose digital I/O pin
			RMII1_RXD0	I	MFP1	RMII1 Receive Data bus bit 0
			SD1_DATA1/ eMMC1_DATA1	I/O	MFP2	SD1 data line bit 1 eMMC1 data line bit 1
			TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin
			SC1_PWR	O	MFP4	Smart Card 1 power pin
			UART7_TXD	O	MFP5	UART7 data transmitter output pin
			USBHL2_DP	A	MFP6	USB 1.1 host lite port 2 differential signal D+
			EBI_DATA8	I/O	MFP8	EBI data bus bit 8
45	90	157	PF.4	I/O	MFP0	General purpose digital I/O pin
			RMII1_REFCLK	I	MFP1	RMII1 mode clock input pin
			SD1_DATA2/ eMMC1_DATA2	I/O	MFP2	SD1 data line bit 2 eMMC1 data line bit 2

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin
			SC1_CD	I	MFP4	Smart Card 1 card detect pin
			UART3_CTS	I	MFP5	UART3 clear to Send input pin
			USBHL3_DM	A	MFP6	USB 1.1 host lite port 3 differential signal D-
			EBI_DATA9	I/O	MFP8	EBI data bus bit 9
46	91	158	PF.5	I/O	MFP0	General purpose digital I/O pin
			RMII1_TXEN	O	MFP1	RMII1 Transmit Enable output pin
			SD1_DATA3/ eMMC1_DATA3	I/O	MFP2	SD1 data line bit 3 eMMC1 data line bit 3
			TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin
			PWM00	O	MFP4	PWM00 counter synchronous trigger output pin
			UART3_RTS	O	MFP5	UART3 request to Send output pin
			USBHL3_DP	A	MFP6	USB 1.1 host lite port 3 differential signal D+
			EBI_DATA10	I/O	MFP8	EBI data bus bit 10
47	92	159	PF.6	I/O	MFP0	General purpose digital I/O pin
			RMII1_TXD1	O	MFP1	RMII1 Transmit Data bus bit 1
			SD1_nCD	I	MFP2	SD1 card detect input pin
			TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin.
			PWM01	O	MFP4	PWM01 counter synchronous trigger output pin
			UART3_RXD	I	MFP5	UART3 data receiver input pin
			USBHL4_DM	A	MFP6	USB 1.1 host lite port 4 differential signal D-
			EBI_DATA11	I/O	MFP8	EBI data bus bit 11
	93	160	PB.13	I/O	MFP0	General purpose digital I/O pin
			EINT2	I	MFP2	External interrupt 2 input pin
			TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
			PWM02	O	MFP4	PWM02 counter synchronous trigger output pin
			UART3_TXD	O	MFP5	UART3 data transmitter output pin
			USBHL4_DP	A	MFP6	USB 1.1 host lite port 4 differential signal D+
			EBI_DATA0	I/O	MFP8	EBI data bus bit 0
48	94	161	V_{DD12}	P	MFP0	Power supply for internal core power pin
		162	V_{DD12}	P	MFP0	Power supply for internal core power pin
		163	V_{SS}	P	MFP0	Ground pin for digital circuit
	95	164	V_{SS}	P	MFP0	Ground pin for digital circuit

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
49	96	165	PF.7	I/O	MFP0	General purpose digital I/O pin
			RMII1_TXD0	O	MFP1	RMII1 Transmit Data bus bit 0
			UART1_CTS	I	MFP2	UART1 clear to Send input pin
			TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
			PWM02	O	MFP4	PWM02 counter synchronous trigger output pin
			UART3_TXD	O	MFP5	UART3 data transmitter output pin
			USBHL4_DP	A	MFP6	USB 1.1 host lite port 4 differential signal D+
			EBI_DATA12	I/O	MFP8	EBI data bus bit 12
50	97	166	PF.8	I/O	MFP0	General purpose digital I/O pin
			RMII1_MDIO	I/O	MFP1	RMII1 PHY Management Data pin
			UART1_RTS	O	MFP2	UART1 request to Send output pin
			TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
			PWM03	O	MFP4	PWM03 counter synchronous trigger output pin
			USBHL5_DM	A	MFP6	USB 1.1 host lite port 5 differential signal D-
			EBI_DATA13	I/O	MFP8	EBI data bus bit 13
51	98	167	PF.9	I/O	MFP0	General purpose digital I/O pin
			RMII1_MDC	O	MFP1	RMII1 PHY Management Clock output pin
			UART1_RXD	I	MFP2	UART1 data receiver input pin
			TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
			PWM10	O	MFP4	PWM10 counter synchronous trigger output pin
			USBHL5_DP	A	MFP6	USB 1.1 host lite port 5 differential signal D+
			EBI_DATA14	I/O	MFP8	EBI data bus bit 14
		168	V_{DD12}	P	MFP0	Power supply for internal core power pin
	99	169	PF.10	I/O	MFP0	General purpose digital I/O pin
			UART1_TXD	O	MFP2	UART1 data transmitter output pin
			TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin
			PWM11	O	MFP4	PWM11 counter synchronous trigger output pin
			VCAP1_PCLK	I	MFP7	Video image interface 1 pixel clock pin
			EBI_DATA15	I/O	MFP8	EBI data bus bit 15
52	100	170	PF.11	I/O	MFP0	General purpose digital I/O pin
			UART0_RXD	I	MFP1	UART0 data receiver input pin
		171	V_{SS}	P	MFP0	Ground pin for digital circuit
53	101	172	PF.12	I/O	MFP0	General purpose digital I/O pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART0_TXD	O	MFP1	UART0 data transmitter output pin
54	102	173	V_{DD33}	P	MFP0	Power supply for I/O power pin
55	103	174	XT_IN	I	MFP0	External 12 MHz crystal input pin
56	104	175	XT_OUT	O	MFP0	External 12 MHz crystal output pin
		176	V_{SS}	P	MFP0	Ground pin for digital circuit
	105	177	PE.0	I/O	MFP0	General purpose digital I/O pin
			RMII0_RXERR	I	MFP1	RMII0 Receive Data Error input pin
			CAN0_RXD	I	MFP2	CAN0 bus receiver input
			UART4_CTS	I	MFP5	UART4 clear to Send input pin
			USBHL1_DM	A	MFP6	USB 1.1 host lite port 1 differential signal D-
			VCAP1_HSYNC	I	MFP7	Video image interface 1 horizontal sync. Pin
	106	178	PE.1	I/O	MFP0	General purpose digital I/O pin
			RMII0_CRSDV	I	MFP1	RMII0 Carrier Sense/Receive Data input pin
			CAN0_TXD	O	MFP2	CAN0 bus transmitter output
			UART4_RTS	O	MFP5	UART4 request to Send output pin
			USBHL1_DP	A	MFP6	USB 1.1 host lite port 1 differential signal D+
			VCAP1_VSYNC	I	MFP7	Video image interface 1 vertical sync. Pin
	107	179	PE.2	I/O	MFP0	General purpose digital I/O pin
			RMII0_RXD1	I	MFP1	RMII0 Receive Data bus bit 1
			CAN1_RXD	I	MFP2	CAN1 bus receiver input
			UART4_RXD	I	MFP5	UART4 data receiver input pin
			USBHL2_DM	A	MFP6	USB 1.1 host lite port 2 differential signal D-
			VCAP1_DATA0	I	MFP7	Video image interface 1 data 0 pin
		180	V_{DD12}	P	MFP0	Power supply for internal core power pin
	108	181	PE.3	I/O	MFP0	General purpose digital I/O pin
			RMII0_RXD0	I	MFP1	RMII0 Receive Data bus bit 0
			CAN1_TXD	O	MFP2	CAN1 bus transmitter output
			UART4_TXD	O	MFP5	UART4 data transmitter output pin
			USBHL2_DP	A	MFP6	USB 1.1 host lite port 2 differential signal D+
			VCAP1_DATA1	I	MFP7	Video image interface 1 data 1 pin
	109	182	PE.4	I/O	MFP0	General purpose digital I/O pin
			RMII0_REFCLK	I	MFP1	RMII0 mode clock input pin
			CAN2_RXD	I	MFP2	CAN2 bus receiver input

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			UART9_CTS	I	MFP5	UART9 clear to Send input pin
			USBHL3_DM	A	MFP6	USB 1.1 host lite port 3 differential signal D-
			VCAP1_DATA2	I	MFP7	Video image interface 1 data 2 pin
	110	183	PE.5	I/O	MFP0	General purpose digital I/O pin
			RMII0_TXEN	O	MFP1	RMII0 Transmit Enable output pin
			CAN2_TXD	O	MFP2	CAN2 bus transmitter output
			UART9_RTS	O	MFP5	UART9 request to Send output pin
			USBHL3_DP	A	MFP6	USB 1.1 host lite port 3 differential signal D+
			VCAP1_DATA3	I	MFP7	Video image interface 1 data 3 pin
	111	184	PE.6	I/O	MFP0	General purpose digital I/O pin
			RMII0_TXD1	O	MFP1	RMII0 Transmit Data bus bit 1
			CAN3_RXD	I	MFP2	CAN3 bus receiver input
			UART9_RXD	I	MFP5	UART9 data receiver input pin
			USBHL4_DM	A	MFP6	USB 1.1 host lite port 4 differential signal D-
			VCAP1_DATA4	I	MFP7	Video image interface 1 data 4 pin
	112	185	PE.7	I/O	MFP0	General purpose digital I/O pin
			RMII0_TXD0	O	MFP1	RMII0 Transmit Data bus bit 0
			CAN3_TXD	O	MFP2	CAN3 bus transmitter output.
			UART9_TXD	O	MFP5	UART9 data transmitter output pin
			USBHL4_DP	A	MFP6	USB 1.1 host lite port 4 differential signal D+
			VCAP1_DATA5	I	MFP7	Video image interface 1 data 5 pin
		186	V_{DD33}	P	MFP0	Power supply for I/O power pin
	113	187	PE.8	I/O	MFP0	General purpose digital I/O pin
			RMII0_MDIO	I/O	MFP1	RMII0 PHY Management Data pin
			UART6_RXD	I	MFP5	UART6 data receiver input pin
			USBHL5_DM	A	MFP6	USB 1.1 host lite port 5 differential signal D-
			VCAP1_DATA6	I	MFP7	Video image interface 1 data 6 pin
	114	188	PE.9	I/O	MFP0	General purpose digital I/O pin
			RMII0_MDC	O	MFP1	RMII0 PHY Management Clock output pin
			UART6_TXD	O	MFP5	UART6 data transmitter output pin
			USBHL5_DP	A	MFP6	USB 1.1 host lite port 5 differential signal D+
			VCAP1_DATA7	I	MFP7	Video image interface 1 data 7 pin
	115	189	PE.10	I/O	MFP0	General purpose digital I/O pin

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
			USB_OVC	I	MFP1	HSUSB host bus power over voltage detector
			CAN3_RXD	I	MFP2	CAN3 bus receiver input
			UART9_RXD	I	MFP3	UART9 data receiver input pin
			PWM12	O	MFP4	PWM12 counter synchronous trigger output pin
			EINT2	I	MFP5	External interrupt 2 input pin
			I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin
			VCAP1_FIELD	I	MFP7	Video image interface 1 frame sync. Pin
57	116	190	PE.11	I/O	MFP0	General purpose digital I/O pin
			USB0_VBUSVLD	I	MFP1	USB0 VBUS valid indication pin
	117	191	PE.12	I/O	MFP0	General purpose digital I/O pin
			USBH_PWREN	O	MFP1	HSUSB host power control pin
			CAN3_TXD	O	MFP2	CAN3 bus transmitter output
			UART9_TXD	O	MFP3	UART9 data transmitter output pin
			PWM13	O	MFP4	PWM13 counter synchronous trigger output pin
			EINT3	I	MFP5	External interrupt 3 input pin
			I2C0_SCL	I/O	MFP6	I^2C0 clock pin
			VCAP1_CLKO	O	MFP7	Video image interface sensor 1 clock pin
		192	V_{SS}	P	MFP0	Ground pin for digital circuit
58	118	193	V_{DD12}	P	MFP0	Power supply for internal core power pin
		194	V_{SS}	P	MFP0	Ground pin for digital circuit
		195	V_{USB1_VDD12}	P	MFP0	Power supply for USB1 VDD12
		196	V_{USB1_VDD12}	P	MFP0	Power supply for USB1 VDD12
		197	V_{USB1_VSS}	P	MFP0	Ground pin for USB1
		198	NC			No connect
		199	NC			No connect
		200	V_{USB1_VSS}	P	MFP0	Ground pin for USB1
	119	201	USB1_DM	A	MFP0	USB1 differential signal D-
	120	202	USB1_DP	A	MFP0	USB1 differential signal D+
59	121	203	V_{USB1_VDD33}	P	MFP0	Power supply for USB1 VDD33
		204	V_{USB1_VDD33}	P	MFP0	Power supply for USB1 VDD33
	122	205	USB1_REXT	A	MFP0	USB1 module reference resister (external 12.1K to GND)
60	123	206	V_{USB0_VDD12}	P	MFP0	Power supply for USB0 VDD12
		207	V_{USB0_VDD12}	P	MFP0	Power supply for USB0 VDD12

64 Pin	128 Pin	216 Pin	Pin Name	Type	MFP	Description
		208	V_{USB0_VSS}	P	MFP0	Ground pin for USB0
		209	NC			No connect
		210	NC			No connect
		211	V_{USB0_VSS}	P	MFP0	Ground pin for USB0.
61	124	212	USB0_DM	A	MFP0	USB0 differential signal D-
62	125	213	USB0_DP	A	MFP0	USB0 differential signal D+
63	126	214	V_{USB0_VDD33}	P	MFP0	Power supply for USB0 VDD33
		215	V_{USB0_VDD33}	P	MFP0	Power supply for USB0 VDD33
64	127	216	USB0_REXT	A	MFP0	USB0 module reference resister (external 12.1K to GND)
EPAD	128		V_{SS}	P	MFP0	Ground pin for digital circuit

Note: Pin Type:

1. I = Digital Input;
2. IU= Digital Input with internal pull high; (Rpu value please refer the GPIO Characteristics of DC Electrical Characteristics)
3. O= Digital Output;
4. I/O= Bi-direction;
5. A = Analog;
6. P = Power Pin;
7. AP = Analog Power

4.2.2 NUC980 Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ADC	ADC_AIN0	PB.0	MFP8	A	ADC channel 0 analog input
	ADC_AIN1	PB.1	MFP8	A	ADC channel 1 analog input
	ADC_AIN2	PB.2	MFP8	A	ADC channel 2 analog input
	ADC_AIN3	PB.3	MFP8	A	ADC channel 3 analog input
	ADC_AIN4	PB.4	MFP8	A	ADC channel 4 analog input
	ADC_AIN5	PB.5	MFP8	A	ADC channel 5 analog input
	ADC_AIN6	PB.6	MFP8	A	ADC channel 6 analog input
	ADC_AIN7	PB.7	MFP8	A	ADC channel 7 analog input
CAN0	CAN0_RXD	PC.3	MFP7	I	CAN0 bus receiver input
		PD.6	MFP4	I	
		PG.11	MFP4	I	
		PE.0	MFP2	I	
	CAN0_TXD	PC.4	MFP7	O	CAN0 bus transmitter output
		PD.7	MFP4	O	
		PG.12	MFP4	O	
		PE.1	MFP2	O	
CAN1	CAN1_RXD	PA.13	MFP5	I	CAN1 bus receiver input
		PD.14	MFP4	I	
		PG.13	MFP4	I	
		PE.2	MFP2	I	
	CAN1_TXD	PA.14	MFP5	O	CAN1 bus transmitter output
		PD.15	MFP4	O	
		PG.14	MFP4	O	
		PE.3	MFP2	O	
CAN2	CAN2_RXD	PA.15	MFP5	I	CAN2 bus receiver input
		PB.1	MFP4	I	
		PB.8	MFP3	I	
		PD.12	MFP4	I	
		PE.4	MFP2	I	
	CAN2_TXD	PG.10	MFP5	O	CAN2 bus transmitter output
		PB.3	MFP4	O	
		PC.0	MFP3	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PD.13	MFP4	O	
		PE.5	MFP2	O	
CAN3	CAN3_RXD	PA.0	MFP7	I	CAN3 bus receiver input
		PE.6	MFP2	I	
		PE.10	MFP2	I	
	CAN3_TXD	PA.1	MFP7	O	CAN3 bus transmitter output
		PE.7	MFP2	O	
		PE.12	MFP2	O	
CFG.0	CFG.0_PwrOnSet0	PG.0	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.1	CFG.1_PwrOnSet1	PG.1	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.2	CFG.2_PwrOnSet2	PG.2	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.3	CFG.3_PwrOnSet3	PG.3	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.4	CFG.4_PwrOnSet4	PG.4	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.5	CFG.5_PwrOnSet5	PG.5	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.6	CFG.6_PwrOnSet6	PG.6	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.7	CFG.7_PwrOnSet7	PG.7	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.8	CFG.8_PwrOnSet8	PG.8	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CFG.9	CFG.9_PwrOnSet9	PG.9	-	IU	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset.
CLK	CLK_OUT	PG.0	MFP3	O	Internal clock selection output pin
EBI	EBI_ADDR0	PG.0	MFP1	O	EBI address bus bit 0
	EBI_ADDR1	PG.1	MFP1	O	EBI address bus bit 1
	EBI_ADDR2	PG.2	MFP1	O	EBI address bus bit 2
		PB.2	MFP1	O	
	EBI_ADDR3	PG.3	MFP1	O	EBI address bus bit 3

Group	Pin Name	GPIO	MFP	Type	Description
	EBI_ADDR4	PG.6	MFP1	O	EBI address bus bit 4
	EBI_ADDR5	PG.7	MFP1	O	EBI address bus bit 5
	EBI_ADDR6	PG.8	MFP1	O	EBI address bus bit 6
	EBI_ADDR7	PG.9	MFP1	O	EBI address bus bit 7
	EBI_ADDR8	PA.12	MFP1	O	EBI address bus bit 8
	EBI_ADDR9	PA.11	MFP1	O	EBI address bus bit 9
	EBI_ADDR10	PA.10	MFP1	O	EBI address bus bit 10
	EBI_ADDR11	PB.8	MFP1	O	EBI address bus bit 11
	EBI_ADDR12	PG.5	MFP1	O	EBI address bus bit 12
		PB.0	MFP1	O	
	EBI_ADDR13	PA.13	MFP1	O	EBI address bus bit 13
		PB.6	MFP1	O	
	EBI_ADDR14	PA.14	MFP1	O	EBI address bus bit 14
		PB.4	MFP1	O	
	EBI_ADDR15	PB.7	MFP1	O	EBI address bus bit 15
	EBI_ADDR16	PB.5	MFP1	O	EBI address bus bit 16
	EBI_ADDR17	PB.1	MFP1	O	EBI address bus bit 17
	EBI_ADDR18	PG.4	MFP1	O	EBI address bus bit 18
		PB.3	MFP1	O	
	EBI_ADDR19	PA.15	MFP1	O	EBI address bus bit 19
	EBI_DATA0	PG.10	MFP1	I/O	EBI data bus bit 0
		PC.0	MFP1	I/O	
		PB.13	MFP8	I/O	
	EBI_DATA1	PC.1	MFP1	I/O	EBI data bus bit 1
		PD.12	MFP8	I/O	
	EBI_DATA2	PC.2	MFP1	I/O	EBI data bus bit 2
		PD.13	MFP8	I/O	
	EBI_DATA3	PC.3	MFP1	I/O	EBI data bus bit 3
		PD.14	MFP8	I/O	
	EBI_DATA4	PC.4	MFP1	I/O	EBI data bus bit 4
		PD.15	MFP8	I/O	
	EBI_DATA5	PC.5	MFP1	I/O	EBI data bus bit 5
		PF.0	MFP8	I/O	
	EBI_DATA6	PC.6	MFP1	I/O	EBI data bus bit 6

Group	Pin Name	GPIO	MFP	Type	Description
		PF.1	MFP8	I/O	
	EBI_DATA7	PC.7	MFP1	I/O	EBI data bus bit 7
		PF.2	MFP8	I/O	
	EBI_DATA8	PC.8	MFP1	I/O	EBI data bus bit 8
		PF.3	MFP8	I/O	
	EBI_DATA9	PC.9	MFP1	I/O	EBI data bus bit 9
		PF.4	MFP8	I/O	
	EBI_DATA10	PC.10	MFP1	I/O	EBI data bus bit 10
		PF.5	MFP8	I/O	
	EBI_DATA11	PC.11	MFP1	I/O	EBI data bus bit 11
		PF.6	MFP8	I/O	
	EBI_DATA12	PC.12	MFP1	I/O	EBI data bus bit 12
		PF.7	MFP8	I/O	
	EBI_DATA13	PC.13	MFP1	I/O	EBI data bus bit 13
		PF.8	MFP8	I/O	
	EBI_DATA14	PC.14	MFP1	I/O	EBI data bus bit 14
		PF.9	MFP8	I/O	
	EBI_DATA15	PC.15	MFP1	I/O	EBI data bus bit 15
		PF.10	MFP8	I/O	
	EBI_MCLK	PA.1	MFP2	O	EBI external clock output pin
	EBI_nCS0	PA.9	MFP1	O	EBI chip select 0 output pin
	EBI_nCS1	PA.6	MFP1	O	EBI chip select 1 output pin
	EBI_nCS2	PA.1	MFP1	O	EBI chip select 2 output pin
	EBI_nRE	PA.8	MFP1	O	EBI read enable output pin
	EBI_nWE	PA.7	MFP1	O	EBI write enable output pin
EINT0	EINT0	PA.0	MFP5	I	External interrupt 0 input pin
		PA.13	MFP8	I	
EINT1	EINT1	PA.1	MFP5	I	External interrupt 1 input pin
		PA.14	MFP8	I	
EINT2	EINT2	PB.3	MFP3	I	External interrupt 2 input pin
		PD.0	MFP4	I	
		PB.13	MFP2	I	
		PE.10	MFP5	I	
EINT3	EINT3	PD.1	MFP4	I	External interrupt 3 input pin

Group	Pin Name	GPIO	MFP	Type	Description
		PG.15	MFP4	I	
		PE.12	MFP5	I	
I2C0	I2C0_SCL	PA.1	MFP3	I/O	I2C0 clock pin
		PG.10	MFP2	I/O	
		PE.12	MFP6	I/O	
	I2C0_SDA	PA.0	MFP3	I/O	I2C0 data input/output pin
		PA.15	MFP2	I/O	
		PE.10	MFP6	I/O	
I2C1	I2C1_SCL	PA.14	MFP2	I/O	I2C1 clock pin
		PB.4	MFP2	I/O	
		PC.3	MFP4	I/O	
	I2C1_SDA	PA.13	MFP2	I/O	I2C1 data input/output pin
		PB.6	MFP2	I/O	
		PC.4	MFP4	I/O	
I2C2	I2C2_SCL	PB.5	MFP2	I/O	I2C2 clock pin
		PB.8	MFP2	I/O	
	I2C2_SDA	PB.7	MFP2	I/O	I2C2 data input/output pin
		PC.0	MFP2	I/O	
I2C3	I2C3_SCL	PB.3	MFP2	I/O	I2C3 clock pin
		PD.14	MFP3	I/O	
	I2C3_SDA	PB.1	MFP2	I/O	I2C3 data input/output pin
		PD.15	MFP3	I/O	
I2S	I2S_BCLK	PA.3	MFP2	O	I2S_ bit clock output pin
		PG.10	MFP8	O	
		PB.4	MFP3	O	
	I2S_DI	PA.4	MFP2	I	I2S_ data input pin
		PB.7	MFP3	I	
	I2S_DO	PA.5	MFP2	O	I2S_ data output pin
		PB.5	MFP3	O	
	I2S_LRCK	PA.2	MFP2	O	I2S_ left right channel clock output pin
		PA.15	MFP8	O	
		PB.6	MFP3	O	
	I2S_MCLK	PA.6	MFP2	O	I2S_ master clock output pin
		PB.1	MFP3	O	

Group	Pin Name	GPIO	MFP	Type	Description
JTAG0	JTAG0_TCK	PG.12	MFP7	I	JTAG0 clock input pin
	JTAG0_TDI	PG.14	MFP7	I	JTAG0 data input pin
	JTAG0_TDO	PG.11	MFP7	O	JTAG0 data output pin
	JTAG0_TMS	PG.13	MFP7	I	JTAG0 test mode selection input pin
	JTAG0_nTRST	PG.15	MFP7	I	JTAG0 reset input pin
JTAG1	JTAG1_TCK	PA.3	MFP4	I	JTAG1 clock input pin
	JTAG1_TDI	PA.5	MFP4	I	JTAG1 data input pin
	JTAG1_TDO	PA.2	MFP4	O	JTAG1 data output pin
	JTAG1_TMS	PA.4	MFP4	I	JTAG1 test mode selection input pin
	JTAG1_nTRST	PA.6	MFP4	I	JTAG1 reset input pin
NAND	NAND_ALE	PC.3	MFP3	O	NAND Flash address latch enable
	NAND_CLE	PC.4	MFP3	O	NAND Flash command latch enable
	NAND_DATA0	PC.8	MFP3	I/O	NAND Flash data bus bit 0
	NAND_DATA1	PC.9	MFP3	I/O	NAND Flash data bus bit 1
	NAND_DATA2	PC.10	MFP3	I/O	NAND Flash data bus bit 2
	NAND_DATA3	PC.11	MFP3	I/O	NAND Flash data bus bit 3
	NAND_DATA4	PC.12	MFP3	I/O	NAND Flash data bus bit 4
	NAND_DATA5	PC.13	MFP3	I/O	NAND Flash data bus bit 5
	NAND_DATA6	PC.14	MFP3	I/O	NAND Flash data bus bit 6
	NAND_DATA7	PC.15	MFP3	I/O	NAND Flash data bus bit 7
	NAND_RDY0	PC.7	MFP3	I	NAND Flash ready/busy pin
	NAND_nCS0	PC.1	MFP3	O	NAND Flash chip enable input
	NAND_nRE	PC.6	MFP3	O	NAND Flash read enable
	NAND_nWE	PC.5	MFP3	O	NAND Flash write enable
	NAND_nWP	PC.2	MFP3	O	NAND Flash write protect input.
PWM0	PWM00	PG.10	MFP7	O	PWM00 counter synchronous trigger output pin
		PG.0	MFP6	O	
		PD.12	MFP6	O	
		PF.5	MFP4	O	
	PWM01	PA.15	MFP7	O	PWM01 counter synchronous trigger output pin
		PG.1	MFP6	O	
		PD.13	MFP6	O	
		PF.6	MFP4	O	
	PWM02	PA.14	MFP7	O	PWM02 counter synchronous trigger output pin

Group	Pin Name	GPIO	MFP	Type	Description
		PG.2	MFP6	O	
		PD.14	MFP6	O	
		PB.13	MFP4	O	
		PF.7	MFP4	O	
	PWM03	PA.13	MFP7	O	PWM03 counter synchronous trigger output pin
		PG.3	MFP6	O	
		PD.15	MFP6	O	
		PF.8	MFP4	O	
PWM1	PWM10	PG.6	MFP6	O	PWM10 counter synchronous trigger output pin
		PB.12	MFP2	O	
		PG.11	MFP6	O	
		PF.9	MFP4	O	
	PWM11	PG.7	MFP6	O	PWM11 counter synchronous trigger output pin
		PB.11	MFP2	O	
		PG.12	MFP6	O	
		PF.10	MFP4	O	
	PWM12	PG.8	MFP6	O	PWM12 counter synchronous trigger output pin
		PB.10	MFP2	O	
		PG.13	MFP6	O	
		PE.10	MFP4	O	
	PWM13	PG.9	MFP6	O	PWM13 counter synchronous trigger output pin
		PB.9	MFP2	O	
		PG.14	MFP6	O	
		PE.12	MFP4	O	
QSPI0	QSPI0_CLK	PD.3	MFP1	I/O	Quad SPI0 serial clock pin
	QSPI0_MISO0	PD.5	MFP1	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin
	QSPI0_MISO1	PD.7	MFP1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin
	QSPI0_MOSI0	PD.4	MFP1	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin
	QSPI0_MOSI1	PD.6	MFP1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin
	QSPI0_SS0	PD.2	MFP1	I/O	Quad SPI0 slave select 0 pin
	QSPI0_SS1	PA.0	MFP1	I/O	Quad SPI0 slave select 1 pin
		PD.0	MFP1	I/O	
RMII0	RMII0_CRSDV	PE.1	MFP1	I	RMII0 Carrier Sense/Receive Data input pin
	RMII0_MDC	PE.9	MFP1	O	RMII0 PHY Management Clock output pin

Group	Pin Name	GPIO	MFP	Type	Description
	RMII0_MDIO	PE.8	MFP1	I/O	RMII0 PHY Management Data pin
	RMII0_REFCLK	PE.4	MFP1	I	RMII0 mode clock input pin
	RMII0_RXD0	PE.3	MFP1	I	RMII0 Receive Data bus bit 0
	RMII0_RXD1	PE.2	MFP1	I	RMII0 Receive Data bus bit 1
	RMII0_RXERR	PE.0	MFP1	I	RMII0 Receive Data Error input pin
	RMII0_TXD0	PE.7	MFP1	O	RMII0 Transmit Data bus bit 0
	RMII0_TXD1	PE.6	MFP1	O	RMII0 Transmit Data bus bit 1
	RMII0_TXEN	PE.5	MFP1	O	RMII0 Transmit Enable output pin
RMII1	RMII1_CRSDV	PF.1	MFP1	I	RMII1 Carrier Sense/Receive Data input pin
	RMII1_MDC	PF.9	MFP1	O	RMII1 PHY Management Clock output pin
	RMII1_MDIO	PF.8	MFP1	I/O	RMII1 PHY Management Data pin
	RMII1_REFCLK	PF.4	MFP1	I	RMII1 mode clock input pin
	RMII1_RXD0	PF.3	MFP1	I	RMII1 Receive Data bus bit 0
	RMII1_RXD1	PF.2	MFP1	I	RMII1 Receive Data bus bit 1
	RMII1_RXERR	PF.0	MFP1	I	RMII1 Receive Data Error input pin
	RMII1_TXD0	PF.7	MFP1	O	RMII1 Transmit Data bus bit 0
	RMII1_TXD1	PF.6	MFP1	O	RMII1 Transmit Data bus bit 1
	RMII1_TXEN	PF.5	MFP1	O	RMII1 Transmit Enable output pin
SC0	SC0_CD	PA.2	MFP3	I	Smart Card 0 card detect pin
		PC.15	MFP4	I	
	SC0_CLK	PA.5	MFP3	O	Smart Card 0 clock pin
		PC.12	MFP4	O	
	SC0_DAT	PA.4	MFP3	I/O	Smart Card 0 data pin
		PC.13	MFP4	I/O	
	SC0_PWR	PA.3	MFP3	O	Smart Card 0 power pin
		PC.14	MFP4	O	
	SC0_RST	PA.6	MFP3	O	Smart Card 0 reset pin
		PC.11	MFP4	O	
SC1	SC1_CD	PC.10	MFP4	I	Smart Card 1 card detect pin
		PF.4	MFP4	I	
	SC1_CLK	PC.7	MFP4	O	Smart Card 1 clock pin
		PF.1	MFP4	O	
	SC1_DAT	PC.8	MFP4	I/O	Smart Card 1 data pin
		PF.2	MFP4	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	SC1_PWR	PC.9	MFP4	O	Smart Card 1 power pin
		PF.3	MFP4	O	
	SC1_RST	PC.6	MFP4	O	Smart Card 1 reset pin
		PF.0	MFP4	O	
SD0	SD0_CLK	PC.6	MFP6	O	SD0 clock output pin
	SD0_CMD	PC.5	MFP6	I/O	SD0 command/response pin
	SD0_DATA0	PC.7	MFP6	I/O	SD0 data line bit 0
	SD0_DATA1	PC.8	MFP6	I/O	SD0 data line bit 1
	SD0_DATA2	PC.9	MFP6	I/O	SD0 data line bit 2
	SD0_DATA3	PC.10	MFP6	I/O	SD0 data line bit 3
	SD0_nCD	PB.8	MFP6	I	SD0 card detect input pin
		PC.12	MFP6	I	
SD1	SD1_CLK	PF.1	MFP2	O	SD1 clock output pin
	SD1_CMD	PF.0	MFP2	I/O	SD1 command/response pin
	SD1_DATA0	PF.2	MFP2	I/O	SD1 data line bit 0
	SD1_DATA1	PF.3	MFP2	I/O	SD1 data line bit 1
	SD1_DATA2	PF.4	MFP2	I/O	SD1 data line bit 2
	SD1_DATA3	PF.5	MFP2	I/O	SD1 data line bit 3
	SD1_nCD	PF.6	MFP2	I	SD1 card detect input pin
SPI0	SPI0_CLK	PC.6	MFP5	I/O	SPI0 serial clock pin
		PD.9	MFP1	I/O	
	SPI0_MISO	PC.8	MFP5	I/O	SPI0 MISO (Master In, Slave Out) pin
		PD.11	MFP1	I/O	
	SPI0_MOSI	PC.4	MFP6	I/O	SPI0 MOSI (Master Out, Slave In) pin
		PC.7	MFP5	I/O	
		PC.14	MFP5	I/O	
		PD.10	MFP1	I/O	
	SPI0_SS0	PC.5	MFP5	I/O	SPI0 slave select 0 pin
		PD.8	MFP1	I/O	
	SPI0_SS1	PB.3	MFP6	I/O	SPI0 slave select 1 pin
		PC.0	MFP5	I/O	
		PD.1	MFP1	I/O	
		PG.15	MFP1	I/O	
SPI1	SPI1_CLK	PG.10	MFP6	I/O	SPI1 serial clock pin

Group	Pin Name	GPIO	MFP	Type	Description
		PB.4	MFP6	I/O	
		PB.10	MFP5	I/O	
		PG.12	MFP2	I/O	
	SPI1_MISO	PB.5	MFP6	I/O	SPI1 MISO (Master In, Slave Out) pin
		PB.12	MFP5	I/O	
		PG.14	MFP2	I/O	
	SPI1_MOSI	PB.7	MFP6	I/O	SPI1 MOSI (Master Out, Slave In) pin
		PB.11	MFP5	I/O	
		PG.13	MFP2	I/O	
	SPI1_SS0	PA.15	MFP6	I/O	SPI1 slave select 0 pin
		PB.6	MFP6	I/O	
		PB.9	MFP5	I/O	
		PG.11	MFP2	I/O	
	SPI1_SS1	PB.1	MFP6	I/O	SPI1 slave select 1 pin
		PG.15	MFP2	I/O	
TM0	TM0_EXT	PB.1	MFP5	I/O	Timer0 external capture input/toggle output pin
		PB.8	MFP7	I/O	
		PB.10	MFP3	I/O	
	TM0_ECNT	PA.0	MFP6	I/O	Timer0 event counter input/toggle output pin
		PD.6	MFP3	I/O	
		PF.0	MFP3	I/O	
	TM0_TGL	PB.3	MFP5	I/O	Timer0 event counter input/toggle output pin
		PC.0	MFP7	I/O	
		PB.9	MFP3	I/O	
TM1	TM1_EXT	PA.13	MFP3	I/O	Timer1 external capture input/toggle output pin
		PD.1	MFP3	I/O	
		PG.12	MFP3	I/O	
		PF.9	MFP3	I/O	
	TM1_ECNT	PA.1	MFP6	I/O	Timer1 event counter input/toggle output pin
		PD.7	MFP3	I/O	
		PF.1	MFP3	I/O	
	TM1_TGL	PA.14	MFP3	I/O	Timer1 event counter input/toggle output pin
		PD.0	MFP3	I/O	
		PG.11	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.8	MFP3	I/O	
TM2	TM2_EXT	PA.9	MFP3	I/O	Timer2 external capture input/toggle output pin
		PB.11	MFP3	I/O	
		PD.13	MFP2	I/O	
	TM2_ECNT	PA.2	MFP6	I/O	Timer2 event counter input/toggle output pin
		PD.8	MFP3	I/O	
		PF.2	MFP3	I/O	
	TM2_TGL	PA.10	MFP3	I/O	Timer2 event counter input/toggle output pin
		PB.12	MFP3	I/O	
		PD.12	MFP2	I/O	
TM3	TM3_EXT	PA.7	MFP3	I/O	Timer3 external capture input/toggle output pin
		PD.15	MFP2	I/O	
	TM3_ECNT	PA.3	MFP6	I/O	Timer3 event counter input/toggle output pin
		PD.9	MFP3	I/O	
		PF.3	MFP3	I/O	
	TM3_TGL	PA.8	MFP3	I/O	Timer3 event counter input/toggle output pin
		PD.14	MFP2	I/O	
TM4	TM4_EXT	PA.11	MFP3	I/O	Timer4 external capture input/toggle output pin
		PD.2	MFP3	I/O	
		PF.6	MFP3	I/O	
	TM4_ECNT	PA.4	MFP6	I/O	Timer4 event counter input/toggle output pin
		PD.10	MFP3	I/O	
		PF.4	MFP3	I/O	
	TM4_TGL	PA.12	MFP3	I/O	Timer4 event counter input/toggle output pin
		PD.3	MFP3	I/O	
		PB.13	MFP3	I/O	
TM5	TM5_EXT	PA.15	MFP3	I/O	Timer5 external capture input/toggle output pin
		PD.4	MFP3	I/O	
		PF.7	MFP3	I/O	
	TM5_ECNT	PA.5	MFP6	I/O	Timer5 event counter input/toggle output pin
		PD.11	MFP3	I/O	
		PF.5	MFP3	I/O	
	TM5_TGL	PG.10	MFP3	I/O	Timer5 event counter input/toggle output pin
		PD.5	MFP3	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.10	MFP3	I/O	
UART0	UART0_RXD	PF.11	MFP1	I	UART0 data receiver input pin
	UART0_TXD	PF.12	MFP1	O	UART0 data transmitter output pin
UART1	UART1_CTS	PC.8	MFP7	I	UART1 clear to Send input pin
		PF.7	MFP2	I	
	UART1_RTS	PC.7	MFP7	O	UART1 request to Send output pin
		PF.8	MFP2	O	
	UART1_RXD	PA.0	MFP4	I	UART1 data receiver input pin
		PC.6	MFP7	I	
		PF.9	MFP2	I	
	UART1_TXD	PA.1	MFP4	O	UART1 data transmitter output pin
		PC.5	MFP7	O	
		PF.10	MFP2	O	
UART2	UART2_CTS	PA.7	MFP2	I	UART2 clear to Send input pin
		PG.2	MFP2	I	
		PB.0	MFP2	I	
	UART2_RTS	PA.8	MFP2	O	UART2 request to Send output pin
		PG.3	MFP2	O	
	UART2_RXD	PA.9	MFP2	I	UART2 data receiver input pin
		PG.0	MFP2	I	
		PD.7	MFP2	I	
	UART2_TXD	PA.10	MFP2	O	UART2 data transmitter output pin
		PG.1	MFP2	O	
		PD.6	MFP2	O	
UART3	UART3_CTS	PB.12	MFP1	I	UART3 clear to Send input pin
		PD.5	MFP2	I	
		PF.4	MFP5	I	
	UART3_RTS	PB.11	MFP1	O	UART3 request to Send output pin
		PD.4	MFP2	O	
		PF.5	MFP5	O	
	UART3_RXD	PC.4	MFP5	I	UART3 data receiver input pin
		PB.10	MFP1	I	
		PD.3	MFP2	I	
		PF.6	MFP5	I	

Group	Pin Name	GPIO	MFP	Type	Description
	UART3_TXD	PC.3	MFP5	O	UART3 data transmitter output pin
		PB.9	MFP1	O	
		PD.2	MFP2	O	
		PB.13	MFP5	O	
		PF.7	MFP5	O	
UART4	UART4_CTS	PD.15	MFP1	I	UART4 clear to Send input pin
		PE.0	MFP5	I	
	UART4_RTS	PD.14	MFP1	O	UART4 request to Send output pin
		PE.1	MFP5	O	
	UART4_RXD	PC.10	MFP7	I	UART4 data receiver input pin
		PD.13	MFP1	I	
		PE.2	MFP5	I	
	UART4_TXD	PC.9	MFP7	O	UART4 data transmitter output pin
		PD.12	MFP1	O	
		PE.3	MFP5	O	
UART5	UART5_CTS	PG.4	MFP2	I	UART5 clear to Send input pin
		PG.11	MFP5	I	
	UART5_RTS	PG.5	MFP2	O	UART5 request to Send output pin
		PG.12	MFP5	O	
	UART5_RXD	PG.6	MFP2	I	UART5 data receiver input pin
		PD.1	MFP2	I	
		PG.13	MFP5	I	
	UART5_TXD	PG.7	MFP2	O	UART5 data transmitter output pin
		PD.0	MFP2	O	
		PG.14	MFP5	O	
UART6	UART6_CTS	PA.2	MFP1	I	UART6 clear to Send input pin
		PD.8	MFP2	I	
	UART6_RTS	PA.3	MFP1	O	UART6 request to Send output pin
		PD.9	MFP2	O	
	UART6_RXD	PA.4	MFP1	I	UART6 data receiver input pin
		PD.11	MFP2	I	
		PE.8	MFP5	I	
	UART6_TXD	PA.5	MFP1	O	UART6 data transmitter output pin
		PD.10	MFP2	O	

Group	Pin Name	GPIO	MFP	Type	Description
		PE.9	MFP5	O	
UART7	UART7_CTS	PB.7	MFP5	I	UART7 clear to Send input pin
		PF.0	MFP5	I	
	UART7_RTS	PB.5	MFP5	O	UART7 request to Send output pin
		PF.1	MFP5	O	
	UART7_RXD	PA.14	MFP6	I	UART7 data receiver input pin
		PB.4	MFP5	I	
		PC.2	MFP4	I	
		PF.2	MFP5	I	
	UART7_TXD	PA.13	MFP6	O	UART7 data transmitter output pin
		PB.6	MFP5	O	
		PC.1	MFP4	O	
		PF.3	MFP5	O	
UART8	UART8_CTS	PG.9	MFP2	I	UART8 clear to Send input pin
		PC.15	MFP7	I	
	UART8_RTS	PG.8	MFP2	O	UART8 request to Send output pin
		PC.14	MFP7	O	
	UART8_RXD	PA.11	MFP2	I	UART8 data receiver input pin
		PC.0	MFP4	I	
		PC.13	MFP7	I	
	UART8_TXD	PA.12	MFP2	O	UART8 data transmitter output pin
		PB.8	MFP4	O	
		PC.12	MFP7	O	
UART9	UART9_CTS	PE.4	MFP5	I	UART9 clear to Send input pin
	UART9_RTS	PB.2	MFP7	O	UART9 request to Send output pin
		PE.5	MFP5	O	
	UART9_RXD	PB.3	MFP7	I	UART9 data receiver input pin
		PE.6	MFP5	I	
		PE.10	MFP3	I	
	UART9_TXD	PB.1	MFP7	O	UART9 data transmitter output pin
		PE.7	MFP5	O	
		PE.12	MFP3	O	
USB0	USB0_VBUSVLD	PE.11	MFP1	I	USB0 VBUS valid indication pin
USBHL0	USBHL0_DM	PB.6	MFP4	A	USB 1.1 Host Lite port 0 differential signal D-

Group	Pin Name	GPIO	MFP	Type	Description
		PB.7	MFP4	A	
		PB.9	MFP4	A	
		PD.14	MFP5	A	
	USBHL0_DP	PB.4	MFP4	A	USB 1.1 Host Lite port 0 differential signal D+
		PB.5	MFP4	A	
		PB.10	MFP4	A	
		PD.15	MFP5	A	
USBHL1	USBHL1_DM	PF.0	MFP6	A	USB 1.1 Host Lite port 1 differential signal D-
		PE.0	MFP6	A	
	USBHL1_DP	PF.1	MFP6	A	USB 1.1 Host Lite port 1 differential signal D+
		PE.1	MFP6	A	
USBHL2	USBHL2_DM	PF.2	MFP6	A	USB 1.1 Host Lite port 2 differential signal D-
		PE.2	MFP6	A	
	USBHL2_DP	PF.3	MFP6	A	USB 1.1 Host Lite port 2 differential signal D+
		PE.3	MFP6	A	
USBHL3	USBHL3_DM	PF.4	MFP6	A	USB 1.1 Host Lite port 3 differential signal D-
		PE.4	MFP6	A	
	USBHL3_DP	PF.5	MFP6	A	USB 1.1 Host Lite port 3 differential signal D+
		PE.5	MFP6	A	
USBHL4	USBHL4_DM	PA.15	MFP4	A	USB 1.1 Host Lite port 4 differential signal D-
		PF.6	MFP6	A	
		PE.6	MFP6	A	
	USBHL4_DP	PG.10	MFP4	A	USB 1.1 Host Lite port 4 differential signal D+
		PB.13	MFP6	A	
		PF.7	MFP6	A	
		PE.7	MFP6	A	
USBHL5	USBHL5_DM	PA.13	MFP4	A	USB 1.1 Host Lite port 5 differential signal D-
		PB.11	MFP4	A	
		PF.8	MFP6	A	
		PE.8	MFP6	A	
	USBHL5_DP	PA.14	MFP4	A	USB 1.1 Host Lite port 5 differential signal D+
		PB.12	MFP4	A	
		PF.9	MFP6	A	
		PE.9	MFP6	A	

Group	Pin Name	GPIO	MFP	Type	Description
USBH	USBH_PWREN	PE.12	MFP1	O	HSUSB host power control pin
USB	USB_OVC	PE.10	MFP1	I	USB host bus power over voltage detector
VCAP0	VCAP0_CLKO	PC.3	MFP2	O	Video image interface 0 sensor clock pin
	VCAP0_DATA0	PC.8	MFP2	I	Video image interface 0 data 0 pin
	VCAP0_DATA1	PC.9	MFP2	I	Video image interface 0 data 1 pin
	VCAP0_DATA2	PC.10	MFP2	I	Video image interface 0 data 2 pin
	VCAP0_DATA3	PC.11	MFP2	I	Video image interface 0 data 3 pin
	VCAP0_DATA4	PC.12	MFP2	I	Video image interface 0 data 4 pin
	VCAP0_DATA5	PC.13	MFP2	I	Video image interface 0 data 5 pin
	VCAP0_DATA6	PC.14	MFP2	I	Video image interface 0 data 6 pin
	VCAP0_DATA7	PC.15	MFP2	I	Video image interface 0 data 7 pin
	VCAP0_FIELD	PC.7	MFP2	I	Video image interface 0 frame sync. Pin
	VCAP0_HSYNC	PC.5	MFP2	I	Video image interface 0 horizontal sync. Pin
	VCAP0_PCLK	PC.4	MFP2	I	Video image interface 0 pixel clock pin
	VCAP0_VSYNC	PC.6	MFP2	I	Video image interface 0 vertical sync. Pin
VCAP1	VCAP1_CLKO	PE.12	MFP7	O	Video image interface 1 sensor clock pin
	VCAP1_DATA0	PE.2	MFP7	I	Video image interface 1 data 0 pin
	VCAP1_DATA1	PE.3	MFP7	I	Video image interface 1 data 1 pin
	VCAP1_DATA2	PE.4	MFP7	I	Video image interface 1 data 2 pin
	VCAP1_DATA3	PE.5	MFP7	I	Video image interface 1 data 3 pin
	VCAP1_DATA4	PE.6	MFP7	I	Video image interface 1 data 4 pin
	VCAP1_DATA5	PE.7	MFP7	I	Video image interface 1 data 5 pin
	VCAP1_DATA6	PE.8	MFP7	I	Video image interface 1 data 6 pin
	VCAP1_DATA7	PE.9	MFP7	I	Video image interface 1 data 7 pin
	VCAP1_FIELD	PE.10	MFP7	I	Video image interface 1 frame sync. Pin
	VCAP1_HSYNC	PE.0	MFP7	I	Video image interface 1 horizontal sync. Pin
	VCAP1_PCLK	PF.10	MFP7	I	Video image interface 1 pixel clock pin
	VCAP1_VSYNC	PE.1	MFP7	I	Video image interface 1 vertical sync. Pin
WDT	WDT_nRST	nRESET	MFP1	O	Watch dog timer reset trigger output
eMMC0	eMMC0_CLK	PC.6	MFP6	O	eMMC0 clock output pin
	eMMC0_CMD	PC.5	MFP6	I/O	eMMC0 command/response pin
	eMMC0_DATA0	PC.7	MFP6	I/O	eMMC0 data line bit 0
	eMMC0_DATA1	PC.8	MFP6	I/O	eMMC0 data line bit 1
	eMMC0_DATA2	PC.9	MFP6	I/O	eMMC0 data line bit 2

Group	Pin Name	GPIO	MFP	Type	Description
	eMMC0_DATA3	PC.10	MFP6	I/O	eMMC0 data line bit 3
eMMC1	eMMC1_CLK	PF.1	MFP2	O	eMMC1 clock output pin
	eMMC1_CMD	PF.0	MFP2	I/O	eMMC1 command/response pin
	eMMC1_DATA0	PF.2	MFP2	I/O	eMMC1 data line bit 0
	eMMC1_DATA1	PF.3	MFP2	I/O	eMMC1 data line bit 1
	eMMC1_DATA2	PF.4	MFP2	I/O	eMMC1 data line bit 2
	eMMC1_DATA3	PF.5	MFP2	I/O	eMMC1 data line bit 3

4.2.3 NUC980 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin
	QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin
	I2C0_SDA	I/O	MFP3	I2C0 data input/output pin
	UART1_RXD	I	MFP4	UART1 data receiver input pin
	EINT0	I	MFP5	External interrupt 0 input pin
	TM0_ECNT	I/O	MFP6	Timer0 event counter input/toggle output pin
	CAN3_RXD	I	MFP7	CAN3 bus receiver input
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin
	EBI_nCS2	O	MFP1	EBI chip select 2 output pin
	EBI_MCLK	O	MFP2	EBI external clock output pin
	I2C0_SCL	I/O	MFP3	I2C0 clock pin
	UART1_TXD	O	MFP4	UART1 data transmitter output pin
	EINT1	I	MFP5	External interrupt 1 input pin
	TM1_ECNT	I/O	MFP6	Timer1 event counter input/toggle output pin
	CAN3_TXD	O	MFP7	CAN3 bus transmitter output
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin
	UART6_CTS	I	MFP1	UART6 clear to Send input pin
	I2S_LRCK	O	MFP2	I2S_ left right channel clock output pin
	SC0_CD	I	MFP3	Smart Card 0 card detect pin
	JTAG1_TDO	O	MFP4	JTAG1 data output pin
	TM2_ECNT	I/O	MFP6	Timer2 event counter input/toggle output pin
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin
	UART6_RTS	O	MFP1	UART6 request to Send output pin
	I2S_BCLK	O	MFP2	I2S_ bit clock output pin
	SC0_PWR	O	MFP3	Smart Card 0 power pin
	JTAG1_TCK	I	MFP4	JTAG1 clock input pin
	TM3_ECNT	I/O	MFP6	Timer3 event counter input/toggle output pin
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin
	UART6_RXD	I	MFP1	UART6 data receiver input pin
	I2S_DI	I	MFP2	I2S_ data input pin
	SC0_DAT	I/O	MFP3	Smart Card 0 data pin
	JTAG1_TMS	I	MFP4	JTAG1 test mode selection input pin
	TM4_ECNT	I/O	MFP6	Timer4 event counter input/toggle output pin

	Pin Name	Type	MFP	Description
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin
	UART6_TXD	O	MFP1	UART6 data transmitter output pin
	I2S_DO	O	MFP2	I2S_ data output pin
	SC0_CLK	O	MFP3	Smart Card 0 clock pin
	JTAG1_TDI	I	MFP4	JTAG1 data input pin
	TM5_ECNT	I/O	MFP6	Timer5 event counter input/toggle output pin
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin
	EBI_nCS1	O	MFP1	EBI chip select 1 output pin
	I2S_MCLK	O	MFP2	I2S_ master clock output pin
	SC0_RST	O	MFP3	Smart Card 0 reset pin
	JTAG1_nTRST	I	MFP4	JTAG1 reset input pin
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin
	EBI_nWE	O	MFP1	EBI write enable output pin
	UART2_CTS	I	MFP2	UART2 clear to Send input pin
	TM3_EXT	I/O	MFP3	Timer3 external capture input/toggle output pin
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin
	EBI_nRE	O	MFP1	EBI read enable output pin
	UART2_RTS	O	MFP2	UART2 request to Send output pin
	TM3_TGL	I/O	MFP3	Timer3 event counter input/toggle output pin
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin
	EBI_nCS0	O	MFP1	EBI chip select 0 output pin
	UART2_RXD	I	MFP2	UART2 data receiver input pin
	TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR10	O	MFP1	EBI address bus bit 10
	UART2_TXD	O	MFP2	UART2 data transmitter output pin
	TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR9	O	MFP1	EBI address bus bit 9
	UART8_RXD	I	MFP2	UART8 data receiver input pin
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR8	O	MFP1	EBI address bus bit 8
	UART8_TXD	O	MFP2	UART8 data transmitter output pin

	Pin Name	Type	MFP	Description
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR13	O	MFP1	EBI address bus bit 13
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
	USBHL5_DM	A	MFP4	USB 1.1 Host Lite port 5 differential signal D-
	CAN1_RXD	I	MFP5	CAN1 bus receiver input
	UART7_TXD	O	MFP6	UART7 data transmitter output pin
	PWM03	O	MFP7	PWM03 counter synchronous trigger output pin
	EINT0	I	MFP8	External interrupt 0 input pin
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR14	O	MFP1	EBI address bus bit 14
	I2C1_SCL	I/O	MFP2	I2C1 clock pin
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
	USBHL5_DP	A	MFP4	USB 1.1 Host Lite port 5 differential signal D+
	CAN1_TXD	O	MFP5	CAN1 bus transmitter output
	UART7_RXD	I	MFP6	UART7 data receiver input pin
	PWM02	O	MFP7	PWM02 counter synchronous trigger output pin
	EINT1	I	MFP8	External interrupt 1 input pin
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR19	O	MFP1	EBI address bus bit 19
	I2C0_SDA	I/O	MFP2	I2C0 data input/output pin
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
	USBHL4_DM	A	MFP4	USB 1.1 Host Lite port 4 differential signal D-
	CAN2_RXD	I	MFP5	CAN2 bus receiver input
	SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin
	PWM01	O	MFP7	PWM01 counter synchronous trigger output pin
	I2S_LRCK	O	MFP8	I2S_ left right channel clock output pin
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR12	O	MFP1	EBI address bus bit 12
	UART2_CTS	I	MFP2	UART2 clear to Send input pin
	ADC_AIN0	A	MFP8	ADC channel 0 analog input
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR17	O	MFP1	EBI address bus bit 17

	Pin Name	Type	MFP	Description
	I2C3_SDA	I/O	MFP2	I2C3 data input/output pin
	I2S_MCLK	O	MFP3	I2S_ master clock output pin
	CAN2_RXD	I	MFP4	CAN2 bus receiver input
	TM0_EXT	I/O	MFP5	Timer0 external capture input/toggle output pin
	SPI1_SS1	I/O	MFP6	SPI1 slave select 1 pin
	UART9_TXD	O	MFP7	UART9 data transmitter output pin
	ADC_AIN1	A	MFP8	ADC channel 1 analog input
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR2	O	MFP1	EBI address bus bit 2
	UART9_RTS	O	MFP7	UART9 request to Send output pin
	ADC_AIN2	A	MFP8	ADC channel 2 analog input
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR18	O	MFP1	EBI address bus bit 18
	I2C3_SCL	I/O	MFP2	I2C3 clock pin
	EINT2	I	MFP3	External interrupt 2 input pin
	CAN2_TXD	O	MFP4	CAN2 bus transmitter output
	TM0_TGL	I/O	MFP5	Timer0 event counter input/toggle output pin
	SPI0_SS1	I/O	MFP6	SPI0 slave select 1 pin
	UART9_RXD	I	MFP7	UART9 data receiver input pin
	ADC_AIN3	A	MFP8	ADC channel 3 analog input
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR14	O	MFP1	EBI address bus bit 14
	I2C1_SCL	I/O	MFP2	I2C1 clock pin
	I2S_BCLK	O	MFP3	I2S_ bit clock output pin
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite port 0 differential signal D+
	UART7_RXD	I	MFP5	UART7 data receiver input pin
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin
	ADC_AIN4	A	MFP8	ADC channel 4 analog input
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR16	O	MFP1	EBI address bus bit 16
	I2C2_SCL	I/O	MFP2	I2C2 clock pin
	I2S_DO	O	MFP3	I2S_ data output pin
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite port 0 differential signal D+
	UART7_RTS	O	MFP5	UART7 request to Send output pin

	Pin Name	Type	MFP	Description
	SPI1_MISO	I/O	MFP6	SPI1 MISO (Master In, Slave Out) pin
	ADC_AIN5	A	MFP8	ADC channel 5 analog input
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR13	O	MFP1	EBI address bus bit 13
	I2C1_SDA	I/O	MFP2	I2C1 data input/output pin
	I2S_LRCK	O	MFP3	I2S_ left right channel clock output pin
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite port 0 differential signal D-
	UART7_TXD	O	MFP5	UART7 data transmitter output pin
	SPI1_SS0	I/O	MFP6	SPI1 slave select 0 pin
	ADC_AIN6	A	MFP8	ADC channel 6 analog input
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR15	O	MFP1	EBI address bus bit 15
	I2C2_SDA	I/O	MFP2	I2C2 data input/output pin
	I2S_DI	I	MFP3	I2S_ data input pin
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite port 0 differential signal D-
	UART7_CTS	I	MFP5	UART7 clear to Send input pin
	SPI1_MOSI	I/O	MFP6	SPI1 MOSI (Master Out, Slave In) pin
	ADC_AIN7	A	MFP8	ADC channel 7 analog input
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR11	O	MFP1	EBI address bus bit 11
	I2C2_SCL	I/O	MFP2	I2C2 clock pin
	CAN2_RXD	I	MFP3	CAN2 bus receiver input
	UART8_TXD	O	MFP4	UART8 data transmitter output pin
	SD0_nCD	I	MFP6	SD0 card detect input pin
	TM0_EXT	I/O	MFP7	Timer0 external capture input/toggle output pin
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin
	UART3_TXD	O	MFP1	UART3 data transmitter output pin
	PWM13	O	MFP2	PWM13 counter synchronous trigger output pin
	TM0_TGL	I/O	MFP3	Timer0 event counter input/toggle output pin
	USBHL0_DM	A	MFP4	USB 1.1 Host Lite port 0 differential signal D-
	SPI1_SS0	I/O	MFP5	SPI1 slave select 0 pin
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin
	UART3_RXD	I	MFP1	UART3 data receiver input pin
	PWM12	O	MFP2	PWM12 counter synchronous trigger output pin

	Pin Name	Type	MFP	Description
	TM0_EXT	I/O	MFP3	Timer0 external capture input/toggle output pin
	USBHL0_DP	A	MFP4	USB 1.1 Host Lite port 0 differential signal D+
	SPI1_CLK	I/O	MFP5	SPI1 serial clock pin
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin
	UART3_RTS	O	MFP1	UART3 request to Send output pin
	PWM11	O	MFP2	PWM11 counter synchronous trigger output pin
	TM2_EXT	I/O	MFP3	Timer2 external capture input/toggle output pin
	USBHL5_DM	A	MFP4	USB 1.1 Host Lite port 5 differential signal D-
	SPI1_MOSI	I/O	MFP5	SPI1 MOSI (Master Out, Slave In) pin
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin
	UART3_CTS	I	MFP1	UART3 clear to Send input pin
	PWM10	O	MFP2	PWM10 counter synchronous trigger output pin
	TM2_TGL	I/O	MFP3	Timer2 event counter input/toggle output pin
	USBHL5_DP	A	MFP4	USB 1.1 Host Lite port 5 differential signal D+
	SPI1_MISO	I/O	MFP5	SPI1 MISO (Master In, Slave Out) pin
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin
	EINT2	I	MFP2	External interrupt 2 input pin
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
	PWM02	O	MFP4	PWM02 counter synchronous trigger output pin
	UART3_TXD	O	MFP5	UART3 data transmitter output pin
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite port 4 differential signal D+
	EBI_DATA0	I/O	MFP8	EBI data bus bit 0
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA0	I/O	MFP1	EBI data bus bit 0
	I2C2_SDA	I/O	MFP2	I2C2 data input/output pin
	CAN2_TXD	O	MFP3	CAN2 bus transmitter output
	UART8_RXD	I	MFP4	UART8 data receiver input pin
	SPI0_SS1	I/O	MFP5	SPI0 slave select 1 pin
	TM0_TGL	I/O	MFP7	Timer0 event counter input/toggle output pin
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA1	I/O	MFP1	EBI data bus bit 1
	NAND_nCS0	O	MFP3	NAND Flash chip enable input
	UART7_TXD	O	MFP4	UART7 data transmitter output pin
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin

	Pin Name	Type	MFP	Description
	EBI_DATA2	I/O	MFP1	EBI data bus bit 2
	NAND_nWP	O	MFP3	NAND Flash write protect input
	UART7_RXD	I	MFP4	UART7 data receiver input pin
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA3	I/O	MFP1	EBI data bus bit 3
	VCAP0_CLKO	O	MFP2	Video image interface 0 sensor clock pin
	NAND_ALE	O	MFP3	NAND Flash address latch enable
	I2C1_SCL	I/O	MFP4	I2C1 clock pin
	UART3_TXD	O	MFP5	UART3 data transmitter output pin
	CAN0_RXD	I	MFP7	CAN0 bus receiver input
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA4	I/O	MFP1	EBI data bus bit 4
	VCAP0_PCLK	I	MFP2	Video image interface 0 pixel clock pin
	NAND_CLE	O	MFP3	NAND Flash command latch enable
	I2C1_SDA	I/O	MFP4	I2C1 data input/output pin
	UART3_RXD	I	MFP5	UART3 data receiver input pin
	SPI0_MOSI	I/O	MFP6	SPI0 MOSI (Master Out, Slave In) pin
	CAN0_TXD	O	MFP7	CAN0 bus transmitter output
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA5	I/O	MFP1	EBI data bus bit 5
	VCAP0_HSYNC	I	MFP2	Video image interface 0 horizontal sync. Pin
	NAND_nWE	O	MFP3	NAND Flash write enable
	SPI0_SS0	I/O	MFP5	SPI0 slave select 0 pin
	SD0_CMD/eMMC0_CMD	I/O	MFP6	SD0 command/response pin eMMC0 command/response pin
	UART1_TXD	O	MFP7	UART1 data transmitter output pin
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA6	I/O	MFP1	EBI data bus bit 6
	VCAP0_VSYNC	I	MFP2	Video image interface 0 vertical sync. Pin
	NAND_nRE	O	MFP3	NAND Flash read enable
	SC1_RST	O	MFP4	Smart Card 1 reset pin
	SPI0_CLK	I/O	MFP5	SPI0 serial clock pin
	SD0_CLK/eMMC0_CLK	O	MFP6	SD0 clock output pin eMMC0 clock output pin

	Pin Name	Type	MFP	Description
	UART1_RXD	I	MFP7	UART1 data receiver input pin
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA7	I/O	MFP1	EBI data bus bit 7
	VCAP0_FIELD	I	MFP2	Video image interface 0 frame sync. Pin
	NAND_RDY0	I	MFP3	NAND Flash ready/busy pin
	SC1_CLK	O	MFP4	Smart Card 1 clock pin
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin
	SD0_DATA0/eMMC0_DATA0	I/O	MFP6	SD0 data line bit 0 eMMC0 data line bit 0
	UART1_RTS	O	MFP7	UART1 request to Send output pin
PC.8	PC.8	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA8	I/O	MFP1	EBI data bus bit 8
	VCAP0_DATA0	I	MFP2	Video image interface 0 data 0 pin
	NAND_DATA0	I/O	MFP3	NAND Flash data bus bit 0
	SC1_DAT	I/O	MFP4	Smart Card 1 data pin
	SPI0_MISO	I/O	MFP5	SPI0 MISO (Master In, Slave Out) pin
	SD0_DATA1/eMMC0_DATA1	I/O	MFP6	SD0 data line bit 1 eMMC0 data line bit 1
	UART1_CTS	I	MFP7	UART1 clear to Send input pin
PC.9	PC.9	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA9	I/O	MFP1	EBI data bus bit 9
	VCAP0_DATA1	I	MFP2	Video image interface 0 data 1 pin
	NAND_DATA1	I/O	MFP3	NAND Flash data bus bit 1
	SC1_PWR	O	MFP4	Smart Card 1 power pin
	SD0_DATA2/eMMC0_DATA2	I/O	MFP6	SD0 data line bit 2 eMMC0 data line bit 2
	UART4_TXD	O	MFP7	UART4 data transmitter output pin
PC.10	PC.10	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA10	I/O	MFP1	EBI data bus bit 10
	VCAP0_DATA2	I	MFP2	Video image interface 0 data 2 pin
	NAND_DATA2	I/O	MFP3	NAND Flash data bus bit 2
	SC1_CD	I	MFP4	Smart Card 1 card detect pin
	SD0_DATA3/eMMC0_DATA3	I/O	MFP6	SD0 data line bit 3 eMMC0 data line bit 3

	Pin Name	Type	MFP	Description
	UART4_RXD	I	MFP7	UART4 data receiver input pin
PC.11	PC.11	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA11	I/O	MFP1	EBI data bus bit 11
	VCAP0_DATA3	I	MFP2	Video image interface 0 data 3 pin
	NAND_DATA3	I/O	MFP3	NAND Flash data bus bit 3
	SC0_RST	O	MFP4	Smart Card 0 reset pin
PC.12	PC.12	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA12	I/O	MFP1	EBI data bus bit 12
	VCAP0_DATA4	I	MFP2	Video image interface 0 data 4 pin
	NAND_DATA4	I/O	MFP3	NAND Flash data bus bit 4
	SC0_CLK	O	MFP4	Smart Card 0 clock pin
	SD0_nCD	I	MFP6	SD0 card detect input pin
	UART8_TXD	O	MFP7	UART8 data transmitter output pin
PC.13	PC.13	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA13	I/O	MFP1	EBI data bus bit 13
	VCAP0_DATA5	I	MFP2	Video image interface 0 data 5 pin
	NAND_DATA5	I/O	MFP3	NAND Flash data bus bit 5
	SC0_DAT	I/O	MFP4	Smart Card 0 data pin
	UART8_RXD	I	MFP7	UART8 data receiver input pin
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA14	I/O	MFP1	EBI data bus bit 14
	VCAP0_DATA6	I	MFP2	Video image interface 0 data 6 pin
	NAND_DATA6	I/O	MFP3	NAND Flash data bus bit 6
	SC0_PWR	O	MFP4	Smart Card 0 power pin
	SPI0_MOSI	I/O	MFP5	SPI0 MOSI (Master Out, Slave In) pin
	UART8_RTS	O	MFP7	UART8 request to Send output pin
PC.15	PC.15	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA15	I/O	MFP1	EBI data bus bit 15
	VCAP0_DATA7	I	MFP2	Video image interface 0 data 7 pin
	NAND_DATA7	I/O	MFP3	NAND Flash data bus bit 7
	SC0_CD	I	MFP4	Smart Card 0 card detect pin
	UART8_CTS	I	MFP7	UART8 clear to Send input pin
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin
	QSPI0_SS1	I/O	MFP1	Quad SPI0 slave select 1 pin

	Pin Name	Type	MFP	Description
	UART5_TXD	O	MFP2	UART5 data transmitter output pin
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
	EINT2	I	MFP4	External interrupt 2 input pin
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin
	SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin
	UART5_RXD	I	MFP2	UART5 data receiver input pin
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
	EINT3	I	MFP4	External interrupt 3 input pin
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin
	QSPI0_SS0	I/O	MFP1	Quad SPI0 slave select 0 pin
	UART3_TXD	O	MFP2	UART3 data transmitter output pin
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin
	QSPI0_CLK	I/O	MFP1	Quad SPI0 serial clock pin
	UART3_RXD	I	MFP2	UART3 data receiver input pin
	TM4_TGL	I/O	MFP3	Timer4 event counter input/toggle output pin
PD.4	PD.4	I/O	MFP0	General purpose digital I/O pin
	QSPI0_MOSI0	I/O	MFP1	Quad SPI0 MOSI0 (Master Out, Slave In) pin
	UART3_RTS	O	MFP2	UART3 request to Send output pin
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
PD.5	PD.5	I/O	MFP0	General purpose digital I/O pin
	QSPI0_MISO0	I/O	MFP1	Quad SPI0 MISO0 (Master In, Slave Out) pin
	UART3_CTS	I	MFP2	UART3 clear to Send input pin
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin
PD.6	PD.6	I/O	MFP0	General purpose digital I/O pin
	QSPI0_MOSI1	I/O	MFP1	Quad SPI0 MOSI1 (Master Out, Slave In) pin
	UART2_TXD	O	MFP2	UART2 data transmitter output pin
	TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin
	CAN0_RXD	I	MFP4	CAN0 bus receiver input
PD.7	PD.7	I/O	MFP0	General purpose digital I/O pin
	QSPI0_MISO1	I/O	MFP1	Quad SPI0 MISO1 (Master In, Slave Out) pin
	UART2_RXD	I	MFP2	UART2 data receiver input pin
	TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output

	Pin Name	Type	MFP	Description
PD.8	PD.8	I/O	MFP0	General purpose digital I/O pin
	SPI0_SS0	I/O	MFP1	SPI0 slave select 0 pin
	UART6_CTS	I	MFP2	UART6 clear to Send input pin
	TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin
PD.9	PD.9	I/O	MFP0	General purpose digital I/O pin
	SPI0_CLK	I/O	MFP1	SPI0 serial clock pin
	UART6_RTS	O	MFP2	UART6 request to Send output pin
	TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin
PD.10	PD.10	I/O	MFP0	General purpose digital I/O pin
	SPI0_MOSI	I/O	MFP1	SPI0 MOSI (Master Out, Slave In) pin
	UART6_TXD	O	MFP2	UART6 data transmitter output pin
	TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin
PD.11	PD.11	I/O	MFP0	General purpose digital I/O pin
	SPI0_MISO	I/O	MFP1	SPI0 MISO (Master In, Slave Out) pin
	UART6_RXD	I	MFP2	UART6 data receiver input pin
	TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin
PD.12	PD.12	I/O	MFP0	General purpose digital I/O pin
	UART4_TXD	O	MFP1	UART4 data transmitter output pin
	TM2_TGL	I/O	MFP2	Timer2 event counter input/toggle output pin
	CAN2_RXD	I	MFP4	CAN2 bus receiver input
	PWM00	O	MFP6	PWM00 counter synchronous trigger output pin
	EBI_DATA1	I/O	MFP8	EBI data bus bit 1
PD.13	PD.13	I/O	MFP0	General purpose digital I/O pin
	UART4_RXD	I	MFP1	UART4 data receiver input pin
	TM2_EXT	I/O	MFP2	Timer2 external capture input/toggle output pin
	CAN2_TXD	O	MFP4	CAN2 bus transmitter output
	PWM01	O	MFP6	PWM01 counter synchronous trigger output pin
	EBI_DATA2	I/O	MFP8	EBI data bus bit 2
PD.14	PD.14	I/O	MFP0	General purpose digital I/O pin
	UART4_RTS	O	MFP1	UART4 request to Send output pin
	TM3_TGL	I/O	MFP2	Timer3 event counter input/toggle output pin
	I2C3_SCL	I/O	MFP3	I2C3 clock pin
	CAN1_RXD	I	MFP4	CAN1 bus receiver input
	USBHL0_DM	A	MFP5	USB 1.1 Host Lite port 0 differential signal D-

	Pin Name	Type	MFP	Description
	PWM02	O	MFP6	PWM02 counter synchronous trigger output pin
	EBI_DATA3	I/O	MFP8	EBI data bus bit 3
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin
	UART4_CTS	I	MFP1	UART4 clear to Send input pin
	TM3_EXT	I/O	MFP2	Timer3 external capture input/toggle output pin
	I2C3_SDA	I/O	MFP3	I2C3 data input/output pin
	CAN1_TXD	O	MFP4	CAN1 bus transmitter output
	USBHL0_DP	A	MFP5	USB 1.1 Host Lite port 0 differential signal D+
	PWM03	O	MFP6	PWM03 counter synchronous trigger output pin
	EBI_DATA4	I/O	MFP8	EBI data bus bit 4
PE.0	PE.0	I/O	MFP0	General purpose digital I/O pin
	RMII0_RXERR	I	MFP1	RMII0 Receive Data Error input pin
	CAN0_RXD	I	MFP2	CAN0 bus receiver input
	UART4_CTS	I	MFP5	UART4 clear to Send input pin
	USBHL1_DM	A	MFP6	USB 1.1 Host Lite port 1 differential signal D-
	VCAP1_HSYNC	I	MFP7	Video image interface 1 horizontal sync. Pin
PE.1	PE.1	I/O	MFP0	General purpose digital I/O pin
	RMII0_CRSDV	I	MFP1	RMII0 Carrier Sense/Receive Data input pin
	CAN0_TXD	O	MFP2	CAN0 bus transmitter output
	UART4_RTS	O	MFP5	UART4 request to Send output pin
	USBHL1_DP	A	MFP6	USB 1.1 Host Lite port 1 differential signal D+
	VCAP1_VSYNC	I	MFP7	Video image interface 1 vertical sync. Pin
PE.2	PE.2	I/O	MFP0	General purpose digital I/O pin
	RMII0_RXD1	I	MFP1	RMII0 Receive Data bus bit 1
	CAN1_RXD	I	MFP2	CAN1 bus receiver input
	UART4_RXD	I	MFP5	UART4 data receiver input pin
	USBHL2_DM	A	MFP6	USB 1.1 Host Lite port 2 differential signal D-
	VCAP1_DATA0	I	MFP7	Video image interface 1 data 0 pin
PE.3	PE.3	I/O	MFP0	General purpose digital I/O pin
	RMII0_RXD0	I	MFP1	RMII0 Receive Data bus bit 0
	CAN1_TXD	O	MFP2	CAN1 bus transmitter output
	UART4_TXD	O	MFP5	UART4 data transmitter output pin
	USBHL2_DP	A	MFP6	USB 1.1 Host Lite port 2 differential signal D+
	VCAP1_DATA1	I	MFP7	Video image interface 1 data 1 pin

	Pin Name	Type	MFP	Description
PE.4	PE.4	I/O	MFP0	General purpose digital I/O pin
	RMII0_REFCLK	I	MFP1	RMII0 mode clock input pin
	CAN2_RXD	I	MFP2	CAN2 bus receiver input
	UART9_CTS	I	MFP5	UART9 clear to Send input pin
	USBHL3_DM	A	MFP6	USB 1.1 Host Lite port 3 differential signal D-
	VCAP1_DATA2	I	MFP7	Video image interface 1 data 2 pin
PE.5	PE.5	I/O	MFP0	General purpose digital I/O pin
	RMII0_TXEN	O	MFP1	RMII0 Transmit Enable output pin
	CAN2_TXD	O	MFP2	CAN2 bus transmitter output
	UART9_RTS	O	MFP5	UART9 request to Send output pin
	USBHL3_DP	A	MFP6	USB 1.1 Host Lite port 3 differential signal D+
	VCAP1_DATA3	I	MFP7	Video image interface 1 data 3 pin
PE.6	PE.6	I/O	MFP0	General purpose digital I/O pin
	RMII0_TXD1	O	MFP1	RMII0 Transmit Data bus bit 1
	CAN3_RXD	I	MFP2	CAN3 bus receiver input
	UART9_RXD	I	MFP5	UART9 data receiver input pin
	USBHL4_DM	A	MFP6	USB 1.1 Host Lite port 4 differential signal D-
	VCAP1_DATA4	I	MFP7	Video image interface 1 data 4 pin
PE.7	PE.7	I/O	MFP0	General purpose digital I/O pin
	RMII0_TXD0	O	MFP1	RMII0 Transmit Data bus bit 0
	CAN3_TXD	O	MFP2	CAN3 bus transmitter output
	UART9_TXD	O	MFP5	UART9 data transmitter output pin
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite port 4 differential signal D+
	VCAP1_DATA5	I	MFP7	Video image interface 1 data 5 pin
PE.8	PE.8	I/O	MFP0	General purpose digital I/O pin
	RMII0_MDIO	I/O	MFP1	RMII0 PHY Management Data pin
	UART6_RXD	I	MFP5	UART6 data receiver input pin
	USBHL5_DM	A	MFP6	USB 1.1 Host Lite port 5 differential signal D-
	VCAP1_DATA6	I	MFP7	Video image interface 1 data 6 pin
PE.9	PE.9	I/O	MFP0	General purpose digital I/O pin
	RMII0_MDC	O	MFP1	RMII0 PHY Management Clock output pin
	UART6_TXD	O	MFP5	UART6 data transmitter output pin
	USBHL5_DP	A	MFP6	USB 1.1 Host Lite port 5 differential signal D+
	VCAP1_DATA7	1	MFP7	Video image interface 1 data 7 pin

	Pin Name	Type	MFP	Description
PE.10	PE.10	I/O	MFP0	General purpose digital I/O pin
	USB_OVC	I	MFP1	USB host bus power over voltage detector
	CAN3_RXD	I	MFP2	CAN3 bus receiver input
	UART9_RXD	I	MFP3	UART9 data receiver input pin
	PWM12	O	MFP4	PWM12 counter synchronous trigger output pin
	EINT2	I	MFP5	External interrupt 2 input pin
	I2C0_SDA	I/O	MFP6	I2C0 data input/output pin
	VCAP1_FIELD	I	MFP7	Video image interface 1 frame sync. Pin
PE.11	PE.11	I/O	MFP0	General purpose digital I/O pin
	USB0_VBUSVLD	I	MFP1	USB0 VBUS valid indication pin
PE.12	PE.12	I/O	MFP0	General purpose digital I/O pin
	USBH_PWREN	O	MFP1	HSUSB host power control pin
	CAN3_TXD	O	MFP2	CAN3 bus transmitter output
	UART9_TXD	O	MFP3	UART9 data transmitter output pin
	PWM13	O	MFP4	PWM13 counter synchronous trigger output pin
	EINT3	I	MFP5	External interrupt 3 input pin
	I2C0_SCL	I/O	MFP6	I2C0 clock pin
	VCAP1_CLKO	O	MFP7	Video image interface 1 sensor clock pin
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin
	RMII1_RXERR	I	MFP1	RMII1 Receive Data Error input pin
	SD1_CMD/eMMC1_CMD	I/O	MFP2	SD1 command/response pin eMMC1 command/response pin
	TM0_ECNT	I/O	MFP3	Timer0 event counter input/toggle output pin
	SC1_RST	O	MFP4	Smart Card 1 reset pin
	UART7_CTS	I	MFP5	UART7 clear to Send input pin
	USBHL1_DM	A	MFP6	USB 1.1 Host Lite port 1 differential signal D-
	EBI_DATA5	I/O	MFP8	EBI data bus bit 5
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin
	RMII1_CRSDV	I	MFP1	RMII1 Carrier Sense/Receive Data input pin
	SD1_CLK/eMMC1_CLK	O	MFP2	SD1 clock output pin eMMC1 clock output pin
	TM1_ECNT	I/O	MFP3	Timer1 event counter input/toggle output pin
	SC1_CLK	O	MFP4	Smart Card 1 clock pin
	UART7_RTS	O	MFP5	UART7 request to Send output pin

	Pin Name	Type	MFP	Description
	USBHL1_DP	A	MFP6	USB 1.1 Host Lite port 1 differential signal D+
	EBI_DATA6	I/O	MFP8	EBI data bus bit 6
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin
	RMII1_RXD1	I	MFP1	RMII1 Receive Data bus bit 1
	SD1_DATA0/eMMC1_DATA0	I/O	MFP2	SD1 data line bit 0 eMMC1 data line bit 0
	TM2_ECNT	I/O	MFP3	Timer2 event counter input/toggle output pin
	SC1_DAT	I/O	MFP4	Smart Card 1 data pin
	UART7_RXD	I	MFP5	UART7 data receiver input pin
	USBHL2_DM	A	MFP6	USB 1.1 Host Lite port 2 differential signal D-
	EBI_DATA7	I/O	MFP8	EBI data bus bit 7
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin
	RMII1_RXD0	I	MFP1	RMII1 Receive Data bus bit 0
	SD1_DATA1/eMMC1_DATA1	I/O	MFP2	SD1 data line bit 1 eMMC1 data line bit 1
	TM3_ECNT	I/O	MFP3	Timer3 event counter input/toggle output pin
	SC1_PWR	O	MFP4	Smart Card 1 power pin
	UART7_TXD	O	MFP5	UART7 data transmitter output pin
	USBHL2_DP	A	MFP6	USB 1.1 Host Lite port 2 differential signal D+
	EBI_DATA8	I/O	MFP8	EBI data bus bit 8
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin
	RMII1_REFCLK	I	MFP1	RMII1 mode clock input pin
	SD1_DATA2/eMMC1_DATA2	I/O	MFP2	SD1 data line bit 2 eMMC1 data line bit 2
	TM4_ECNT	I/O	MFP3	Timer4 event counter input/toggle output pin
	SC1_CD	I	MFP4	Smart Card 1 card detect pin
	UART3_CTS	I	MFP5	UART3 clear to Send input pin
	USBHL3_DM	A	MFP6	USB 1.1 Host Lite port 3 differential signal D-
	EBI_DATA9	I/O	MFP8	EBI data bus bit 9
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin
	RMII1_TXEN	O	MFP1	RMII1 Transmit Enable output pin
	SD1_DATA3/eMMC1_DATA3	I/O	MFP2	SD1 data line bit 3 eMMC1 data line bit 3
	TM5_ECNT	I/O	MFP3	Timer5 event counter input/toggle output pin

	Pin Name	Type	MFP	Description
	PWM00	O	MFP4	PWM00 counter synchronous trigger output pin
	UART3_RTS	O	MFP5	UART3 request to Send output pin
	USBHL3_DP	A	MFP6	USB 1.1 Host Lite port 3 differential signal D+
	EBI_DATA10	I/O	MFP8	EBI data bus bit 10
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin
	RMII1_TXD1	O	MFP1	RMII1 Transmit Data bus bit 1
	SD1_nCD	I	MFP2	SD1 card detect input pin
	TM4_EXT	I/O	MFP3	Timer4 external capture input/toggle output pin
	PWM01	O	MFP4	PWM01 counter synchronous trigger output pin
	UART3_RXD	I	MFP5	UART3 data receiver input pin
	USBHL4_DM	A	MFP6	USB 1.1 Host Lite port 4 differential signal D-
	EBI_DATA11	I/O	MFP8	EBI data bus bit 11
PF.7	PF.7	I/O	MFP0	General purpose digital I/O pin
	RMII1_TXD0	O	MFP1	RMII1 Transmit Data bus bit 0
	UART1_CTS	I	MFP2	UART1 clear to Send input pin
	TM5_EXT	I/O	MFP3	Timer5 external capture input/toggle output pin
	PWM02	O	MFP4	PWM02 counter synchronous trigger output pin
	UART3_TXD	O	MFP5	UART3 data transmitter output pin
	USBHL4_DP	A	MFP6	USB 1.1 Host Lite port 4 differential signal D+
	EBI_DATA12	I/O	MFP8	EBI data bus bit 12
PF.8	PF.8	I/O	MFP0	General purpose digital I/O pin
	RMII1_MDIO	I/O	MFP1	RMII1 PHY Management Data pin
	UART1_RTS	O	MFP2	UART1 request to Send output pin
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
	PWM03	O	MFP4	PWM03 counter synchronous trigger output pin
	USBHL5_DM	A	MFP6	USB 1.1 Host Lite port 5 differential signal D-
	EBI_DATA13	I/O	MFP8	EBI data bus bit 13
PF.9	PF.9	I/O	MFP0	General purpose digital I/O pin
	RMII1_MDC	O	MFP1	RMII1 PHY Management Clock output pin
	UART1_RXD	I	MFP2	UART1 data receiver input pin
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
	PWM10	O	MFP4	PWM10 counter synchronous trigger output pin
	USBHL5_DP	A	MFP6	USB 1.1 Host Lite port 5 differential signal D+
	EBI_DATA14	I/O	MFP8	EBI data bus bit 14

	Pin Name	Type	MFP	Description
PF.10	PF.10	I/O	MFP0	General purpose digital I/O pin
	UART1_TXD	O	MFP2	UART1 data transmitter output pin
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin
	PWM11	O	MFP4	PWM11 counter synchronous trigger output pin
	VCAP1_PCLK	I	MFP7	Video image interface 1 pixel clock pin
	EBI_DATA15	I/O	MFP8	EBI data bus bit 15
PF.11	PF.11	I/O	MFP0	General purpose digital I/O pin
	UART0_RXD	I	MFP1	UART0 data receiver input pin
PF.12	PF.12	I/O	MFP0	General purpose digital I/O pin
	UART0_TXD	O	MFP1	UART0 data transmitter output pin
PG.0	PG.0	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR0	O	MFP1	EBI address bus bit 0
	UART2_RXD	I	MFP2	UART2 data receiver input pin
	CLK_OUT	O	MFP3	Internal clock selection output pin
	PWM00	O	MFP6	PWM00 counter synchronous trigger output pin
	CFG.0_PwrOnSet0	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.1	PG.1	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR1	O	MFP1	EBI address bus bit 1
	UART2_TXD	O	MFP2	UART2 data transmitter output pin
	PWM01	O	MFP6	PWM01 counter synchronous trigger output pin
	CFG.1_PwrOnSet1	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.2	PG.2	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR2	O	MFP1	EBI address bus bit 2
	UART2_CTS	I	MFP2	UART2 clear to Send input pin
	PWM02	O	MFP6	PWM02 counter synchronous trigger output pin
	CFG.2_PwrOnSet2	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.3	PG.3	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR3	O	MFP1	EBI address bus bit 3
	UART2_RTS	O	MFP2	UART2 request to Send output pin
	PWM03	O	MFP6	PWM03 counter synchronous trigger output pin
	CFG.3_PwrOnSet3	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.4	PG.4	I/O	MFP0	General purpose digital I/O pin

	Pin Name	Type	MFP	Description
	EBI_ADDR18	O	MFP1	EBI address bus bit 18
	UART5_CTS	I	MFP2	UART5 clear to Send input pin
	CFG.4_PwrOnSet4	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.5	PG.5	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR12	O	MFP1	EBI address bus bit 12
	UART5_RTS	O	MFP2	UART5 request to Send output pin
	CFG.5_PwrOnSet5	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.6	PG.6	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR4	O	MFP1	EBI address bus bit 4
	UART5_RXD	I	MFP2	UART5 data receiver input pin
	PWM10	O	MFP6	PWM10 counter synchronous trigger output pin
	CFG.6_PwrOnSet6	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.7	PG.7	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR5	O	MFP1	EBI address bus bit 5
	UART5_TXD	O	MFP2	UART5 data transmitter output pin
	PWM11	O	MFP6	PWM11 counter synchronous trigger output pin
	CFG.7_PwrOnSet7	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.8	PG.8	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR6	O	MFP1	EBI address bus bit 6
	UART8_RTS	O	MFP2	UART8 request to Send output pin
	PWM12	O	MFP6	PWM12 counter synchronous trigger output pin
	CFG.8_PwrOnSet8	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.9	PG.9	I/O	MFP0	General purpose digital I/O pin
	EBI_ADDR7	O	MFP1	EBI address bus bit 7
	UART8_CTS	I	MFP2	UART8 clear to Send input pin
	PWM13	O	MFP6	PWM13 counter synchronous trigger output pin
	CFG.9_PwrOnSet9	IU	-	System configuration and power on setting with an internal pull-up. Internal pull-up only active automatically during reset
PG.10	PG.10	I/O	MFP0	General purpose digital I/O pin
	EBI_DATA0	I/O	MFP1	EBI data bus bit 0
	I2C0_SCL	I/O	MFP2	I2C0 clock pin
	TM5_TGL	I/O	MFP3	Timer5 event counter input/toggle output pin

	Pin Name	Type	MFP	Description
	USBHL4_DP	A	MFP4	USB 1.1 Host Lite port 4 differential signal D+
	CAN2_TXD	O	MFP5	CAN2 bus transmitter output
	SPI1_CLK	I/O	MFP6	SPI1 serial clock pin
	PWM00	O	MFP7	PWM00 counter synchronous trigger output pin
	I2S_BCLK	O	MFP8	I2S_ bit clock output pin
PG.11	PG.11	I/O	MFP0	General purpose digital I/O pin
	SPI1_SS0	I/O	MFP2	SPI1 slave select 0 pin
	TM1_TGL	I/O	MFP3	Timer1 event counter input/toggle output pin
	CAN0_RXD	I	MFP4	CAN0 bus receiver input
	UART5_CTS	I	MFP5	UART5 clear to Send input pin
	PWM10	O	MFP6	PWM10 counter synchronous trigger output pin
	JTAG0_TDO	O	MFP7	JTAG0 data output pin
PG.12	PG.12	I/O	MFP0	General purpose digital I/O pin
	SPI1_CLK	I/O	MFP2	SPI1 serial clock pin
	TM1_EXT	I/O	MFP3	Timer1 external capture input/toggle output pin
	CAN0_TXD	O	MFP4	CAN0 bus transmitter output
	UART5_RTS	O	MFP5	UART5 request to Send output pin
	PWM11	O	MFP6	PWM11 counter synchronous trigger output pin
	JTAG0_TCK	I	MFP7	JTAG0 clock input pin
PG.13	PG.13	I/O	MFP0	General purpose digital I/O pin
	SPI1_MOSI	I/O	MFP2	SPI1 MOSI (Master Out, Slave In) pin
	CAN1_RXD	I	MFP4	CAN1 bus receiver input
	UART5_RXD	I	MFP5	UART5 data receiver input pin
	PWM12	O	MFP6	PWM12 counter synchronous trigger output pin
	JTAG0_TMS	I	MFP7	JTAG0 test mode selection input pin
PG.14	PG.14	I/O	MFP0	General purpose digital I/O pin
	SPI1_MISO	I/O	MFP2	SPI1 MISO (Master In, Slave Out) pin
	CAN1_TXD	O	MFP4	CAN1 bus transmitter output
	UART5_TXD	O	MFP5	UART5 data transmitter output pin
	PWM13	O	MFP6	PWM13 counter synchronous trigger output pin
	JTAG0_TDI	I	MFP7	JTAG0 data input pin
PG.15	PG.15	I/O	MFP0	General purpose digital I/O pin
	SPI0_SS1	I/O	MFP1	SPI0 slave select 1 pin
	SPI1_SS1	I/O	MFP2	SPI1 slave select 1 pin

	Pin Name	Type	MFP	Description
	EINT3	I	MFP4	External interrupt 3 input pin
	JTAG0_nTRST	I	MFP7	JTAG0 reset input pin

5 BLOCK DIAGRAM

5.1 NUC980 Series Block Diagram

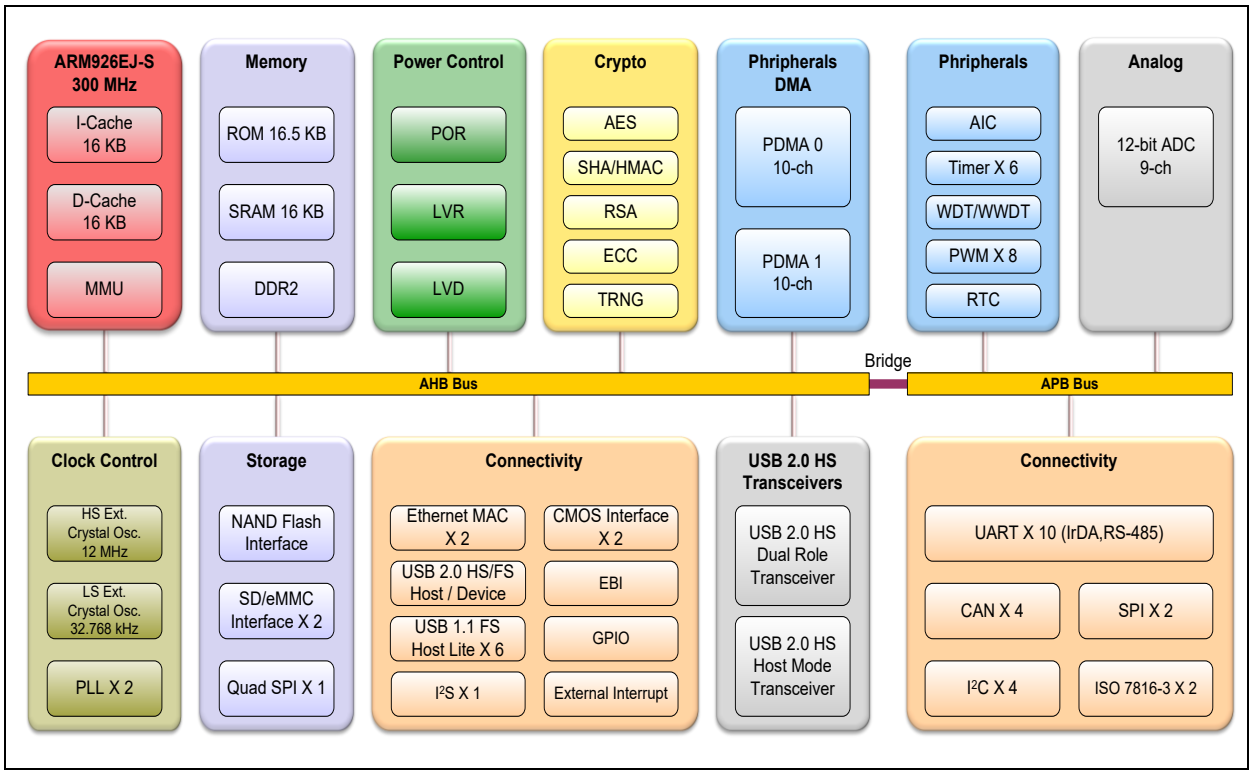


Figure 5.1-1 NUC980 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM® ARM926EJ-S CPU Core

6.1.1 Overview

The ARM926EJ-S CPU core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S CPU core is targeted at multi-tasking applications where full memory management, high performance, and low power are all important.

The ARM926EJ-S CPU core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to choose between high performance and high code density. The ARM926EJ-S CPU core includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead.

The ARM926EJ-S processor provides support for external coprocessor enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S CPU core implements ARM architecture version 5TEJ.

The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core.
- A Memory Management Unit (MMU).
- Separate instruction and data cache.
- Separate instruction and data AMBA AHB bus interfaces.

6.2 System Manager

6.2.1 Overview

The system management describes the following information and functions.

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Product Identifier (PDID), Power-On Setting, System Wake-Up, Reset Control for on-chip controllers/peripherals, and multi-function pin control.
- System Control registers

6.2.2 System Reset

The system reset can be issued by one of the following listed events. For these reset event flags can be read by RSTSTS register.

- Power-On Reset
- Low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- CPU Reset
- System Reset

6.2.3 System Power Distribution

In this chip, the power distribution is divided into six segments.

- Analog power from AV_{DD33} provides 3.3V voltage to analog components operation. These analog components including POR33, 12-bit SAR-ADC, LVD and LVR.
- Digital power from V_{DD12} provides 1.2V voltage to POR12, APLL, APLL, SRAM (16 kB) and all digital logic except RTC.
- Digital power from $VBAT_{33}$ provides 3.3V voltage to LXT and RTC logic.
- USB PHY power from V_{USB0_VDD33}, V_{USB0_VDD12} provides 3.3V and 1.2 respectively to USB 2.0 PHY 0, while V_{USB1_VDD33}, V_{USB1_VDD12} provides 3.3V and 1.2 respectively to USB 2.0 PHY 1.
- I/O power from MV_{DD} provides 1.8V to I/O pins used to connect DDR2 SDRAM.
- I/O power from V_{DD33} provides 3.3V to HXT and I/O pins (PA ~ PG).

Figure 6.2-1 shows the power distribution of the NUC980 series.

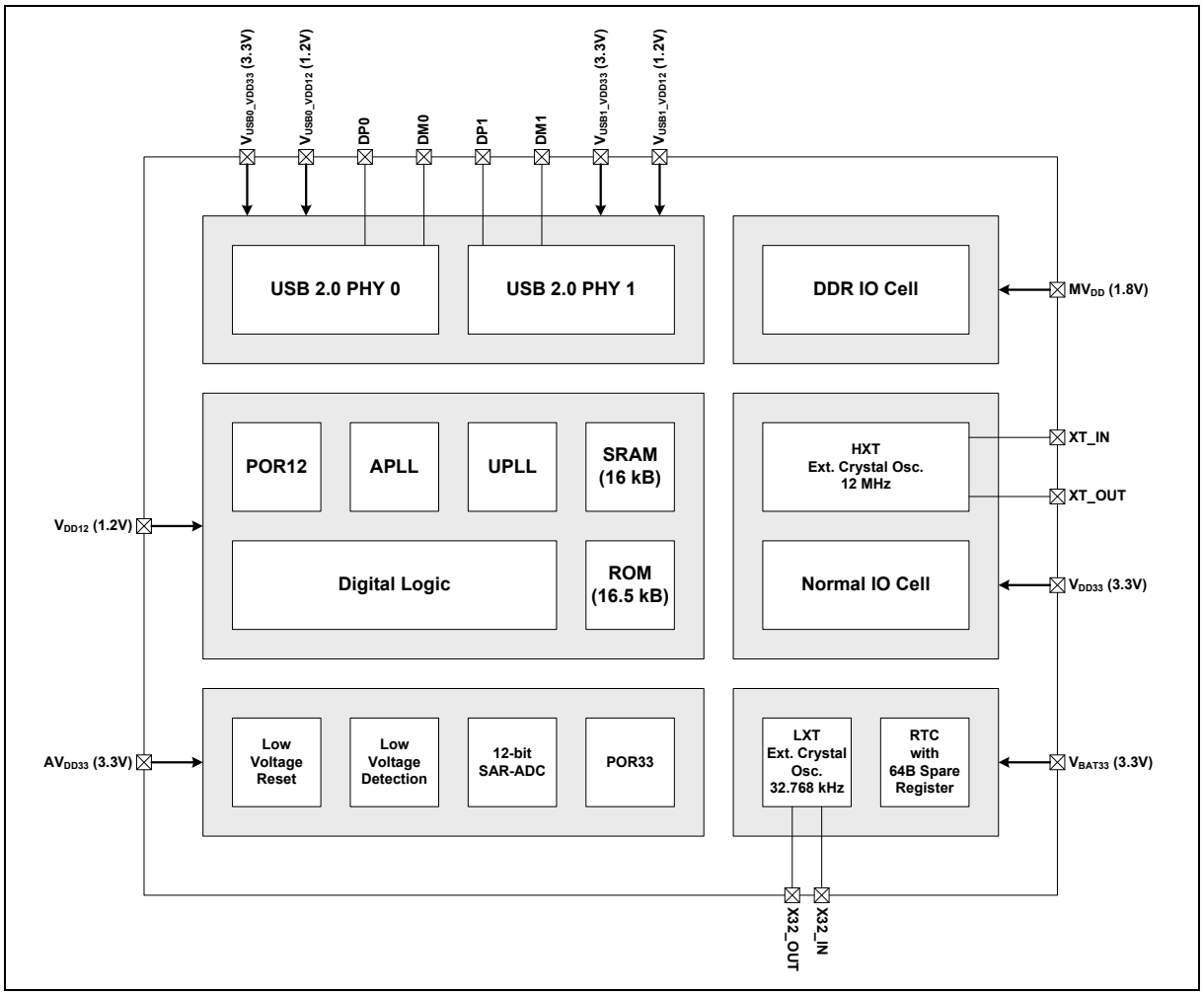


Figure 6.2-1 NUC980 Series Power Distribution Diagram

6.2.4 System Memory Map

This chip supports only little-endian data format and provides 4G-byte addressing space. Figure 6.2-2 describes the memory space definition.

The memory space from 0x0000_0000 to 0x1FFF_FFFF is for SDRAM and external devices. The memory space from 0x3C00_0000 to 0x3C00_3FFF is for embedded 16 Kbytes SRAM. The memory space for On-Chip Controllers and Peripherals is from 0xB000_0000 to 0xB00A_3FFF while the memory space from 0xFFFF_0000 to 0xFFFF_41FF is for 16.5 Kbytes internal Boot ROM.

This chip provides the shadow memory function. The memory space from 0x8000_0000 to 0x9FFF_FFFF is the shadow memory space for memory space from 0x0000_0000 to 0x1FFF_FFFF. The memory space from 0xBC00_0000 to 0xBC00_3FFF is the shadow memory space for memory space from 0x3C00_0000 to 0x3C00_3FFF. If the DMA of On-Chip Controller wants to access this 16 Kbytes embedded SRAM, it's necessary to use memory space from 0xBC00_0000 to 0xBC00_3FFF

The reserved memory space is un-accessible. Chip's behavior is undefined and unpredictable while accessing to reserved memory space.

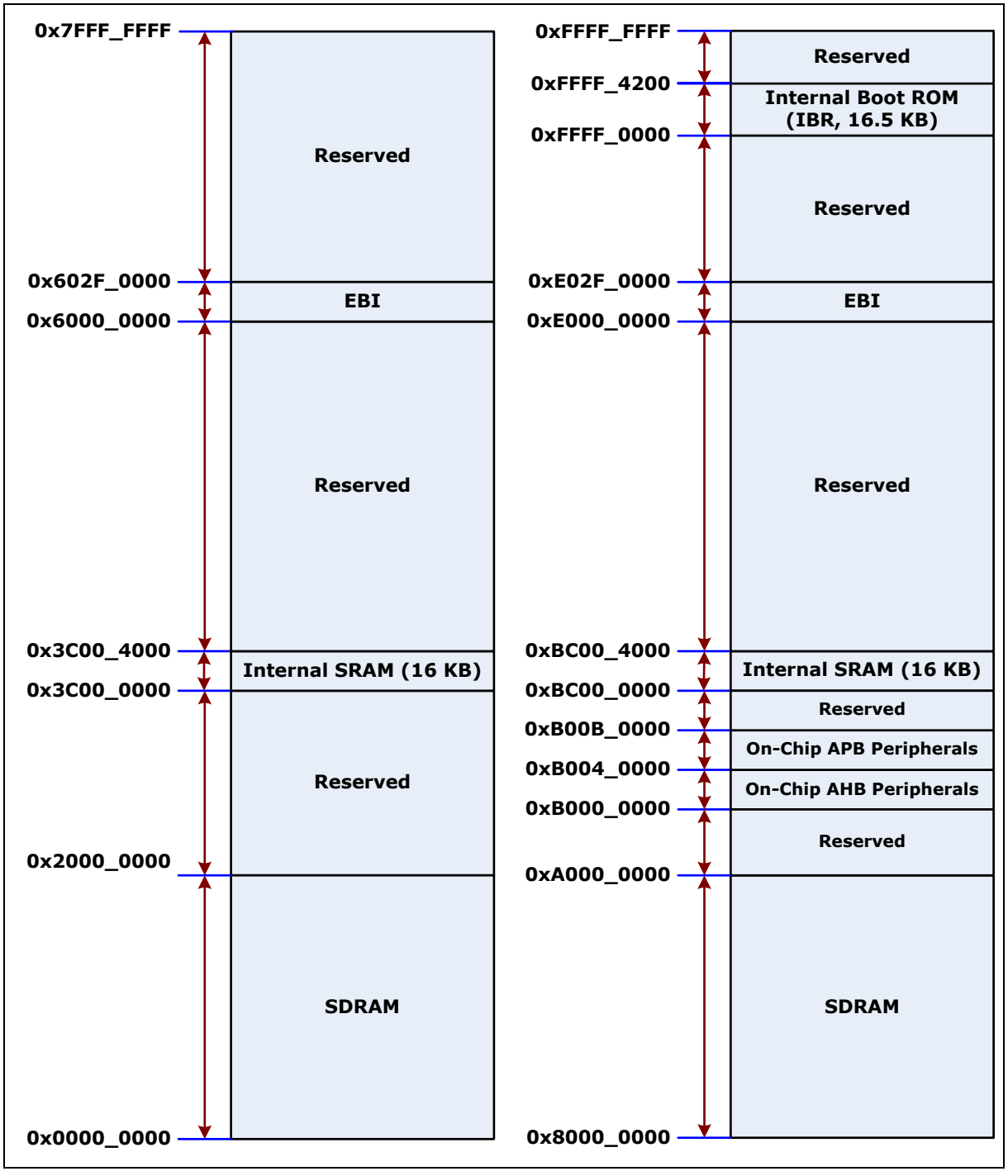


Figure 6.2-2 NUC980 System Memory Map Diagram

The addressing space assigned to each on-chip controller or peripheral described in Table 6.2-1. The detailed register definition, addressing space, and programming details will be described in the following sections.

Addressing Space	Token	Modules
SDRAM, External Devices and SRAM Memory Space		
0x0000_0000 – 0x1FFF_FFFF	SDRAM_BA	SDRAM Memory Space
0x6000_0000 – 0x602F_FFFF	EXDEV_BA	External Devices Memory Space
0x3C00_0000 – 0x3C00_3FFF	SRAM_BA	SRAM Memory Space (16 KB)
Internal Boot ROM (IBR) Memory Space (0xFFFF_0000 ~ 0xFFFF_41FF)		
0xFFFF_0000 – 0xFFFF_41FF	IBR_BA	Internal Boot ROM (IBR) Memory Space (16.5 KB)
AHB Modules Memory Space (0xB000_0000 – 0xB003_FFFF)		
0xB000_0000 – 0xB000_01FF	SYS_BA	System Global Control Registers
0xB000_0200 – 0xB000_02FF	CLK_BA	Clock Control Registers
0xB000_2000 – 0xB000_2FFF	SDIC_BA	SDRAM Control Registers
0xB000_4000 – 0xB000_4FFF	GPIO_BA	GPIO Control Registers
0xB000_8000 – 0xB000_8FFF	PDMA0_BA	PDMA 0 Control Registers
0xB000_9000 – 0xB000_9FFF	PDMA1_BA	PDMA 1 Control Registers
0xB001_0000 – 0xB001_0FFF	EBI_BA	EBI Control Registers
0xB001_2000 – 0xB001_2FFF	EMAC0_BA	Ethernet MAC 0 Control Registers
0xB002_4000 – 0xB002_4FFF	CAP0_BA	Capture Sensor Interface 0 Control Registers
0xB001_5000 – 0xB001_5FFF	HSUSBH_BA	High Speed USB 2.0 Host Control Registers
0xB001_6000 – 0xB001_6FFF	HSUSBD_BA	High Speed USB 2.0 Device Control Registers
0xB001_7000 – 0xB001_7FFF	USBH_BA	USB 2.0 Host Control Registers
0xB001_8000 – 0xB001_8FFF	SDH_BA	SD/SDIO Host Control Registers
0xB001_9000 – 0xB001_9FFF	FMI_BA	Flash Memory Interface (FMI) Control Registers
0xB001_C000 – 0xB001_EFFF	CRYPTO_BA	Cryptographic Accelerator Control Registers
0xB002_0000 – 0xB002_0FFF	I2S_BA	I^2S Interface Control Registers
0xB002_2000 – 0xB002_2FFF	EMAC1_BA	Ethernet MAC 1 Control Registers
0xB001_4000 – 0xB001_4FFF	CAP1_BA	Capture Sensor Interface 1 Control Registers
APB Modules Memory Space (0xB004_0000 ~ 0xB00A_FFFF)		
0xB004_0000 – 0xB004_00FF	WDT_BA	Watch-Dog Timer Control Registers
0xB004_0100 – 0xB004_01FF	WWDT_BA	Windowed Watch-Dog Timer Control Registers
0xB004_1000 – 0xB004_1FFF	RTC_BA	Real Time Clock (RTC) Control Registers
0xB004_2000 – 0xB004_2FFF	AIC_BA	Advance Interrupt Control Registers
0xB004_3000 – 0xB004_3FFF	ADC_BA	ADC Control Registers
0xB005_0000 – 0xB005_0FFF	TMR_BA01	Timer 0 and Timer 1 Control Registers
0xB005_1000 – 0xB005_1FFF	TMR_BA23	Timer 2 and Timer 3 Control Registers
0xB005_2000 – 0xB005_2FFF	TMR_BA45	Timer 4 and Timer 5 Control Registers

0xB005_8000 – 0xB005_8FFF	PWM0_BA	PWM 0 Control Registers
0xB005_9000 – 0xB005_9FFF	PWM1_BA	PWM 1 Control Registers
0xB006_0000 – 0xB006_0FFF	QSPI0_BA	QSPI 0 Control Registers
0xB006_1000 – 0xB006_1FFF	SPI0_BA	SPI 0 Control Registers
0xB006_2000 – 0xB006_2FFF	SPI1_BA	SPI 1 Control Registers
0xB007_0000 – 0xB007_0FFF	UART0_BA	UART 0 Control Registers
0xB007_1000 – 0xB007_1FFF	UART1_BA	UART 1 Control Registers
0xB007_2000 – 0xB007_2FFF	UART2_BA	UART 2 Control Registers
0xB007_3000 – 0xB007_3FFF	UART3_BA	UART 3 Control Registers
0xB007_4000 – 0xB007_4FFF	UART4_BA	UART 4 Control Registers
0xB007_5000 – 0xB007_5FFF	UART5_BA	UART 5 Control Registers
0xB007_6000 – 0xB007_6FFF	UART6_BA	UART 6 Control Registers
0xB007_7000 – 0xB007_7FFF	UART7_BA	UART 7 Control Registers
0xB007_8000 – 0xB007_8FFF	UART8_BA	UART 8 Control Registers
0xB007_9000 – 0xB007_9FFF	UART9_BA	UART 9 Control Registers
0xB008_0000 – 0xB008_0FFF	I2C0_BA	I^2C 0 Control Registers
0xB008_1000 – 0xB008_1FFF	I2C1_BA	I^2C 1 Control Registers
0xB008_2000 – 0xB008_2FFF	I2C2_BA	I^2C 2 Control Registers
0xB008_3000 – 0xB008_3FFF	I2C3_BA	I^2C 3 Control Registers
0xB009_0000 – 0xB009_0FFF	SC0_BA	Smart Card 0 Control Registers
0xB009_1000 – 0xB009_1FFF	SC1_BA	Smart Card 1 Control Registers
0xB00A_0000 – 0xB00A_0FFF	CAN0_BA	CAN 0 Control Registers
0xB00A_1000 – 0xB00A_1FFF	CAN1_BA	CAN 1 Control Registers
0xB00A_2000 – 0xB00A_2FFF	CAN2_BA	CAN 2 Control Registers
0xB00A_3000 – 0xB00A_3FFF	CAN3_BA	CAN 3 Control Registers

Table 6.2-1 Address Space Assignments for On-Chip Controllers

6.2.5 Power-On Setting

After power on reset, Power-On setting registers are latched to configure this chip. Table 6.2-2 describes the definition of each power-on setting bit.

Power-On Setting Pin	Description	Power-on Setting Register Bit
USB0_ID	USB Port 0 Role Selection 0 = USB Port 0 act as a USB host. 1 = USB Port 0 act as a USB device.	USBID (SYS_PWRON[16])
PG[1:0]	Boot Source Selection 00 = Boot from USB. 01 = Boor from SD0/eMMC. 10 = Boot from NAND Flash. 11 = Boot from SPI Flash.	BTSSEL (SYS_PWRON[1:0])
PG.2	QSPI0_CLK Frequency Selection 0 = QSPI0_CLK frequency is 30 MHz. 1 = QSPI0_CLK frequency is 50 MHz.	QSPI0CKSEL (SYS_PWRON[2])
PG.3	Watchdog Timer (WDT) Enabled/Disabled Selection 0 = After power-on, WDT Disabled. 1 = after power-on WDT Enabled.	WDTON (SYS_PWRON[3])
PG.4	JTAG Interface Selection 0 = Pin PA[6:2] used as JTAG interface. 1 = Pin PG[15:11] used as JTAG interface.	JTAGSEL (SYS_PWRON[4])
PG.5	UART 0 Debug Message Output ON/OFF Selection 0 = UART 0 debug message output ON and pin PF[12:11] used as the UART0 functionality. 1 = UART 0 debug message output OFF and pin PF[12:11] used as the GPIO functionality.	URDBGON (SYS_PWRON[5])
PG[7:6]	NAND Flash Page Size selection 00 = NAND Flash page size is 2KB. 01 = NAND Flash page size is 4KB. 10 = NAND Flash page size is 8KB. 11 = Ignore Power-On Setting.	NPAGESEL (SYS_PWRON[7:6])
PG[9:8]	Miscellaneous Configuration When BTSSEL = 01, Boot from SD/eMMC, the MISCCFG defines the GPC or GPF used as the booting source. 11 = GPC group used as the booting source. Others = GPF group used as the booting source. When BTSSEL = 10, Boot from NAND Flash, the MISCCFG defines the ECC type. 00 = No ECC 01 = ECC is BCH T12 10 = ECC is BCH T24 11 = Ignore power-on setting When BTSEL = 11, Boot from SPI Flash, the MISCCFG defines the SPI Flash type and data width. 00 = SPI-NAND Flash with 1-bit mode. 01 = SPI-NAND Flash with 4-bit mode. 10 = SPI-NOR Flash with 4-bit mode. 11 = SPI-NOR Flash with 1-bit mode.	MISCCFG (SYS_PWRON[9:8])

Table 6.2-2 Power-On Setting Bit Description

6.2.6 Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYS Base Address: **SYS_BA = 0xB000_0000**				
SYS_PDID	SYS_BA+0x000	R	Product Identifier Register	0x1030_D016[1]
SYS_PWRON	SYS_BA+0x004	R/W	Power-on Setting Register	0xXXXX_XXXX[2]
SYS_LVRDCR	SYS_BA+0x020	R/W	Low Voltage Reset & Detect Control Register	0x0000_0001
SYS_MISCFCR	SYS_BA+0x030	R/W	Miscellaneous Function Control Register	0x0000_0200
SYS_MISCIER	SYS_BA+0x040	R/W	Miscellaneous Interrupt Enable Register	0x0000_0000
SYS_MISCISR	SYS_BA+0x044	R/W	Miscellaneous Interrupt Status Register	0x0001_0000
SYS_WKUPSER0	SYS_BA+0x050	R/W	System Wakeup Source Enable Register 0	0x0000_0000
SYS_WKUPSER1	SYS_BA+0x054	R/W	System Wakeup Source Enable Register 1	0x0000_0000
SYS_WKUPSSR0	SYS_BA+0x058	R/W	System Wakeup Source Status Register 0	0x0000_0000
SYS_WKUPSSR1	SYS_BA+0x05C	R/W	System Wakeup Source Status Register 1	0x0000_0000
SYS_AHBIPRST	SYS_BA+0x060	R/W	AHB IP Reset Control Register	0x0000_0000
SYS_APBIPRST0	SYS_BA+0x064	R/W	APB IP Reset Control Register 0	0x0000_0000
SYS_APBIPRST1	SYS_BA+0x068	R/W	APB IP Reset Control Register 1	0x0000_0000
SYS_RSTSTS	SYS_BA+0x06C	R/W	Reset Source Active Status Register	0x0000_00XX
SYS_GPA_MFPL	SYS_BA+0x070	R/W	GPIOA Low Byte Multiple Function Control Register	0x0XXX_XX00
SYS_GPA_MFPH	SYS_BA+0x074	R/W	GPIOA High Byte Multiple Function Control Register	0x0000_0000
SYS_GPB_MFPL	SYS_BA+0x078	R/W	GPIOB Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPB_MFPH	SYS_BA+0x07C	R/W	GPIOB High Byte Multiple Function Control Register	0x0000_0000
SYS_GPC_MFPL	SYS_BA+0x080	R/W	GPIOC Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPC_MFPH	SYS_BA+0x084	R/W	GPIOC High Byte Multiple Function Control Register	0x0000_0000
SYS_GPD_MFPL	SYS_BA+0x088	R/W	GPIOD Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPD_MFPH	SYS_BA+0x08C	R/W	GPIOD High Byte Multiple Function Control Register	0x0000_0000
SYS_GPE_MFPL	SYS_BA+0x090	R/W	GPIOE Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPE_MFPH	SYS_BA+0x094	R/W	GPIOE High Byte Multiple Function Control Register	0x0000_0000
SYS_GPF_MFPL	SYS_BA+0x098	R/W	GPIOF Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPF_MFPH	SYS_BA+0x09C	R/W	GPIOF High Byte Multiple Function Control Register	0x0000_0000

SYS_GPG_MFPL	SYS_BA+0x0A0	R/W	GPIOG Low Byte Multiple Function Control Register	0x0000_0000
SYS_GPG_MFPH	SYS_BA+0x0A4	R/W	GPIOG High Byte Multiple Function Control Register	0xXXXX_X000
SYS_DDR_DSCTL	SYS_BA+0x0F0	R/W	DDR I/O Driving Strength Control Register	0x0000_0000
SYS_GPBL_DSCTL	SYS_BA+0x0F4	R/W	GPIOB Low Byte Driving Strength Control Register	0x4444_4444
SYS_PORDISCR	SYS_BA+0x100	R/W	Power-On-reset Disable Control Register	0x0000_00XX
SYS_RSTDEBCTL	SYS_BA+0x10C	R/W	Reset Pin De-bounce Control Register	0x0000_04B0
SYS_REGWPCTL	SYS_BA+0x1FC	R/W	Register Write-protection Control Register	0x0000_0000

Note: [1] Dependents on part number.

Note: [2] Dependents on power-on setting.

6.2.7 Register Description

Product Identifier Register (SYS_PDID)

Register	Offset	R/W	Description	Reset Value
SYS_PDID	SYS_BA+0x000	R	Product Identifier Register	0x1030_D016

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
PRDNUML6				PRDNUML5			
15	14	13	12	11	10	9	8
PRDNUML4				PRDNUML3			
7	6	5	4	3	2	1	0
PRDNUML2				PRDNUML1			

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:20]	**PRDNUML6**	**Product Number Letter 6** 0 = D. 1 = F. 2 = G. 3 = H.
[19:16]	**PRDNUML5**	**Product Number Letter 5** 0 = A. 1 = B.
[15:12]	**PRDNUML4**	**Product Number Letter 4** 0xD
[11:8]	**PRDNUML3**	**Product Number Letter 3** 0x0
[7:4]	**PRDNUML2**	**Product Number Letter 2** 0x1
[3:0]	**PRDNUML1**	**Product Number Letter 1** 0x6

Power-on Setting Register (SYS_PWRON)

Register	Offset	R/W	Description	Reset Value
SYS_PWRON	SYS_BA+0x004	R/W	Power-on Setting Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved			USERID				
23	22	21	20	19	18	17	16
Reserved	DRAMSIZE			Reserved		TICMOD	USBID
15	14	13	12	11	10	9	8
Reserved						MISCCFG	
7	6	5	4	3	2	1	0
NPAGESEL		URDBGON	JTAGSEL	WDTON	QSPI0CKSEL	BTSSEL	

Bits	Description	
[31:29]	**Reserved**	Reserved.
[28:24]	**USERID**	**User ID (Read Only)** A user defined ID.
[23]	**Reserved**	Reserved.
[22:20]	**DRAMSIZE**	**DRAM Size** 000 = Reserved. 001 = 2 MB 010 = Reserved. 011 = 8 MB 100 = 16 MB 101 = 32 MB 110 = 64 MB 111 = 128 MB
[19:18]	**Reserved**	Reserved.
[17]	**TICMOD**	**TIC Mode Enable Bit** 0= TIC interface Disabled. 1= TIC interface Enabled.
[16]	**USBID**	**USB ID Pin Status** 0= USB port 0 used as a USB device. 1= USB port 0 used as a USB host.

[9:8]	**MISCCFG**	**Miscellaneous Configuration** When pin nRESET transited from low to high, the value of pin PG[9:8] latched to MISCCFG. When BTSSEL = 01, Boot from SD/eMMC, the MISCCFG defines the SD0/eMMC0 or SD1/eMMC1 used as the booting source. 11 = SD0/eMMC0 (GPC group) used as the booting source. Others = SD1/eMMC1 (GPF group) used as the booting source. When BTSSEL = 10, Boot from NAND Flash, the MISCCFG defines the ECC type. 00 = ECC is BCH T8. 01 = ECC is BCH T12. 10 = ECC is BCH T24. 11 = Ignore power-on setting. When BTSEL = 11, Boot from SPI Flash, the MISCCFG defines the SPI Flash type and data width. 00 = SPI-NAND Flash with 1-bit mode. 01 = SPI-NAND Flash with 4-bit mode. 10 = SPI-NOR Flash with 4-bit mode. 11 = SPI-NOR Flash with 1-bit mode.
[7:6]	**NPAGESEL**	**NAND Flash Page Size Selection** When pin nRESET transited from low to high, the value of pin PG[7:6] latched to NPAGESEL. 00= NAND Flash page size is 2KB. 01= NAND Flash page size is 4KB. 10= NAND Flash page size is 8KB. 11= Ignore power-on setting.
[5]	**URDBGON**	**UART 0 Debug Message Output ON/OFF Selection** When pin nRESET transited from low to high, the value of pin PG.5 latched to URDBGON. 0= UART 0 debug message output ON. 1= UART 0 debug message output OFF.
[4]	**JTAGSEL**	**JTAG Interface Selection** When pin nRESET transited from low to high, the value of pin PG.4 latched to JTAGSEL. 0 = Pin PA[6:2] used as JTAG interface. 1 = Pin PG[15:11] used as JTAG interface.
[3]	**WDTON**	**Watchdog Timer (WDT) ON/OFF Selection** When pin nRESET transited from low to high, the value of pin PG.3 latched to WDTON. 0 = After power-on, WDT Disabled. 1 = after power-on WDT Enabled.
[2]	**QSPI0CKSEL**	**QSPI0_CLK Frequency Selection** When pin nRESET transited from low to high, the value of pin PG.2 latched to QSPI0CKSEL. 0 = QSPI0_CLK frequency is 37.5 MHz. 1 = QSPI0_CLK frequency is 75 MHz.

[1:0]	**BTSSEL**	**Boot Source Selection** When pin nRESET transited from low to high, the value of pin PG[1:0] latched to BTSSEL. 00= Boot from USB. 01= Boot from SD/eMMC. 10= Boot from NAND Flash. 11= Boot from SPI Flash.

Low Voltage Reset & Detect Control Register (SYS_LVRDCR)

Register	Offset	R/W	Description	Reset Value
SYS_LVRDCR	SYS_BA+0x020	R/W	Low Voltage Reset & Detect Control Register	0x0000_0001

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved						LVD_SEL	LVD_EN
7	6	5	4	3	2	1	0
Reserved							LVR_EN

Bits	Description	
[31:10]	**Reserved**	Reserved.
[9]	**LVD_SEL**	**Low Voltage Detect Threshold Selection** 0 = Low voltage detection level is 2.6V. 1 = Low voltage detection level is 2.8V.
[8]	**LVD_EN**	**Low Voltage Detect Enable Bit** 0 = Low voltage detect function Disabled. 1 = Low voltage detect function Enabled.
[7:1]	**Reserved**	Reserved.
[0]	**LVR_EN**	**Low Voltage Reset Enable Bit** 0 = Low voltage reset function Disabled. 1 = Low voltage reset function Enabled.

Miscellaneous Function Control Register (SYS_MISCFCR)

Register	Offset	R/W	Description	Reset Value
SYS_MISCFCR	SYS_BA+0x030	R/W	Miscellaneous Function Control Register	0x0000_0200

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved			GPIOLBEN	USRHDSEN	Reserved	HDSPUEN	WDTRSTEN
7	6	5	4	3	2	1	0
Reserved							

Bits	Description	
[31:13]	**Reserved**	Reserved.
[12]	**GPIOLBEN**	**GPIO Pin Loop-back Enable Bit** 0 = GPIO input status didn't reflect pin status if the GPIO configured as functional pin. 1 = GPIO input status did reflect pin status even if the GPIO configured as functional pin.
[11]	**USRHDSEN**	**User Configurable USB Host Device Role Selection Enable Bit** 0 = USB host/device role selection decided by HDS pin. 1 = USB host/device role selection decided by USBID (SYS_PWRON[16]).
[10]	**Reserved**	Reserved.
[9]	**HDSPUEN**	**HDS Pin Internal Pull-up Enable Bit** 0 = HDS pin internal pull-up resister Disabled. 1 = HDS pin internal pull-up resister Enabled.
[8]	**WDTRSTEN**	**WatchDog Timer Reset Connection Enable Bit** This bit is used to enable the function that connect watch-dog timer reset to nRESET pin. If this bit is enabled, the watch-dog timer reset is connected to nRESET pin internally 0 = Watch-dog timer reset not connected to nRESET pin internally. 1 = Watch-dog timer reset connected to nRESET pin internally.
[7:0]	**Reserved**	Reserved.

Miscellaneous Interrupt Enable Register (SYS_MISCIER)

Register	Offset	R/W	Description	Reset Value
SYS_MISCIER	SYS_BA+0x040	R/W	Miscellaneous Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USBIDC_IEN	LVD_IEN

Bits	Description	
[31:2]	**Reserved**	Reserved.
[1]	**USBIDC_IEN**	**USB0_ID Pin Status Change Interrupt Enable Bit** 0 = HDS status change interrupt Disabled. 1 = HDS status change interrupt Enabled.
[0]	**LVD_IEN**	**Low Voltage Detect Interrupt Enable Bit** 0 = Low voltage detect interrupt Disabled. 1 = Low voltage detect interrupt Enabled.

Miscellaneous Interrupt Status Register (SYS_MISCISR)

Register	Offset	R/W	Description	Reset Value
SYS_MISCISR	SYS_BA+0x044	R/W	Miscellaneous Interrupt Status Register	0x0001_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved						USB0_IDS	IBR_RUN_F
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved						USBIDC_IS	LVD_IS

Bits	Description	
[31:18]	**Reserved**	Reserved.
[17]	**USB0_IDS**	**USB0_ID Status** 0 = USB port 0 used as a USB device port. 1 = USB port 0 used as a USB host port.
[16]	**IBR_RUN_F**	**IBR Run Flag** 0 = CPU didn't execute instruction in 0xFFFF_0000 yet. 1 = CPU executed instruction in 0xFFFF_0000.
[15:2]	**Reserved**	Reserved.
[1]	**USBIDC_IS**	**USB0_ID Pin State Change Interrupt Status** 0 = USB0_ID state didn't change. 1 = USB0_ID state changed from low to high or from high to low.
[0]	**LVD_IS**	**Low Voltage Detect Interrupt Status** 0 = No low voltage event. 1 = Low voltage event detected.

System Wakeup Source Enable Register 0 (SYS_WKUPSER0)

Register	Offset	R/W	Description	Reset Value
SYS_WKUPSER0	SYS_BA+0x050	R/W	System Wakeup Source Enable Register 0	0x0000_0000

31	30	29	28	27	26	25	24
Reserved						UR9WKEN	UR8WKEN
23	22	21	20	19	18	17	16
UR7WKEN	UR6WKEN	UR5WKEN	UR4WKEN	UR3WKEN	UR2WKEN	UR1WKEN	UR0WKEN
15	14	13	12	11	10	9	8
Reserved		TMR5WKEN	TMR4WKEN	TMR3WKEN	TMR2WKEN	TMR1WKEN	TMR0WKEN
7	6	5	4	3	2	1	0
EINT3WKEN	EINT2WKEN	EINT1WKEN	EINT0WKEN	GPIOWKEN	Reserved	Reserved	WDTWKEN

Bits	Description	
[31:26]	**Reserved**	Reserved.
[25]	**UR9WKEN**	**UART 9 Wake System Up Enable Bit** 0 = UART 9 wake system up function Disabled. 1 = UART 9 wake system up function Enabled.
[24]	**UR8WKEN**	**UART 8 Wake System Up Enable Bit** 0 = UART 8 wake system up function Disabled. 1 = UART 8 wake system up function Enabled.
[23]	**UR7WKEN**	**UART 7 Wake System Up Enable Bit** 0 = UART 7 wake system up function Disabled. 1 = UART 7 wake system up function Enabled.
[22]	**UR6WKEN**	**UART 6 Wake System Up Enable Bit** 0 = UART 6 wake system up function Disabled. 1 = UART 6 wake system up function Enabled.
[21]	**UR5WKEN**	**UART 5 Wake System Up Enable Bit** 0 = UART 5 wake system up function Disabled. 1 = UART 5 wake system up function Enabled.
[20]	**UR4WKEN**	**UART 4 Wake System Up Enable Bit** 0 = UART 4 wake system up function Disabled. 1 = UART 4 wake system up function Enabled.
[19]	**UR3WKEN**	**UART 3 Wake System Up Enable Bit** 0 = UART 3 wake system up function Disabled. 1 = UART 3 wake system up function Enabled.
[18]	**UR2WKEN**	**UART 2 Wake System Up Enable Bit** 0 = UART 2 wake system up function Disabled. 1 = UART 2 wake system up function Enabled.

[17]	**UR1WKEN**	**UART 1 Wake System Up Enable Bit** 0 = UART 1 wake system up function Disabled. 1 = UART 1 wake system up function Enabled.
[16]	**UR0WKEN**	**UART 0 Wake System Up Enable Bit** 0 = UART 0 wake system up function Disabled. 1 = UART 0 wake system up function Enabled.
[15:14]	**Reserved**	Reserved.
[13]	**TMR5WKEN**	**TIMER 5 Wake System Up Enable Bit** 0 = TIMER 5 wake system up function Disabled. 1 = TIMER 5 wake system up function Enabled.
[12]	**TMR4WKEN**	**TIMER 4 Wake System Up Enable Bit** 0 = TIMER 4 wake system up function Disabled. 1 = TIMER 4 wake system up function Enabled.
[11]	**TMR3WKEN**	**TIMER 3 Wake System Up Enable Bit** 0 = TIMER 3 wake system up function Disabled. 1 = TIMER 3 wake system up function Enabled.
[10]	**TMR2WKEN**	**TIMER 2 Wake System Up Enable Bit** 0 = TIMER 2 wake system up function Disabled. 1 = TIMER 2 wake system up function Enabled.
[9]	**TMR1WKEN**	**TIMER 1 Wake System Up Enable Bit** 0 = TIMER 1 wake system up function Disabled. 1 = TIMER 1 wake system up function Enabled.
[8]	**TMR0WKEN**	**TIMER 0 Wake System Up Enable Bit** 0 = TIMER 0 wake system up function Disabled. 1 = TIMER 0 wake system up function Enabled.
[7]	**EINT3WKEN**	**External Interrupt 3 Wake System Up Enable Bit** 0 = External Interrupt 3 wake system up function Disabled. 1 = External Interrupt 3 wake system up function Enabled.
[6]	**EINT2WKEN**	**External Interrupt 2 Wake System Up Enable Bit** 0 = External Interrupt 2 wake system up function Disabled. 1 = External Interrupt 2 wake system up function Enabled.
[5]	**EINT1WKEN**	**External Interrupt 1 Wake System Up Enable Bit** 0 = External Interrupt 1 wake system up function Disabled. 1 = External Interrupt 1 wake system up function Enabled.
[4]	**EINT0WKEN**	**External Interrupt 0 Wake System Up Enable Bit** 0 = External Interrupt 0 wake system up function Disabled. 1 = External Interrupt 0 wake system up function Enabled.
[3]	**GPIOWKEN**	**GPIO Wake System Up Enable Bit** 0 = GPIO wake system up function Disabled. 1 = GPIO wake system up function Enabled.
[2:1]	**Reserved**	Reserved.

[0]	**WDTWKEN**	**WDT Wake System Up Enable Bit** 0 = WDT wake system up function Disabled. 1 = WDT wake system up function Enabled.

System Wakeup Source Enable Register 1 (SYS_WKUPSER1)

Register	Offset	R/W	Description	Reset Value
SYS_WKUPSER1	SYS_BA+0x054	R/W	System Wakeup Source Enable Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved			SDHWKEN	USBDWKEN	USBHWKEN	EMAC1WKEN	EMAC0WKEN
15	14	13	12	11	10	9	8
LVDWKEN	Reserved			CAN3WKEN	CAN2WKEN	CAN1WKEN	CAN0WKEN
7	6	5	4	3	2	1	0
RTCWKEN	Reserved			I2C3WKEN	I2C2WKEN	I2C1WKEN	I2C0WKEN

Bits	Description	
[31:21]	**Reserved**	Reserved.
[20]	**SDHWKEN**	**SDH Wake System Up Enable Bit** 0 = SDH wake system up function Disabled. 1 = SDH wake system up function Enabled.
[19]	**USBDWKEN**	**USB Device Wake System Up Enable Bit** 0 = USB device wake system up function Disabled. 1 = USB device wake system up function Enabled.
[18]	**USBHWKEN**	**USB Host Wake System Up Enable Bit** 0 = USB host wake system up function Disabled. 1 = USB host wake system up function Enabled.
[17]	**EMAC1WKEN**	**Ethernet MAC 1 Wake System Up Enable Bit** 0 = Ethernet MAC 1 wake system up function Disabled. 1 = Ethernet MAC 1 wake system up function Enabled.
[16]	**EMAC0WKEN**	**Ethernet MAC 0 Wake System Up Enable Bit** 0 = Ethernet MAC 0 wake system up function Disabled. 1 = Ethernet MAC 0 wake system up function Enabled.
[15]	**LVDWKEN**	**Low Voltage Detect Wake System Up Enable Bit** 0 = Low Voltage Detect wake system up function Disabled. 1 = Low Voltage Detect wake system up function Enabled.
[14:12]	**Reserved**	Reserved.
[11]	**CAN3WKEN**	**CAN 3 Wake System Up Enable Bit** 0 = CAN 3 wake system up function Disabled. 1 = CAN 3 wake system up function Enabled.

[10]	**CAN2WKEN**	**CAN 2 Wake System Up Enable Bit** 0 = CAN 2 wake system up function Disabled. 1 = CAN 2 wake system up function Enabled.
[9]	**CAN1WKEN**	**CAN 1 Wake System Up Enable Bit** 0 = CAN 1 wake system up function Disabled. 1 = CAN 1 wake system up function Enabled.
[8]	**CAN0WKEN**	**CAN 0 Wake System Up Enable Bit** 0 = CAN 0 wake system up function Disabled. 1 = CAN 0 wake system up function Enabled.
[7]	**RTCWKEN**	**RTC Wake System Up Enable Bit** 0 = RTC wake system up function Disabled. 1 = RTC wake system up function Enabled.
[6:4]	**Reserved**	Reserved.
[3]	**I2C3WKEN**	**I^2C 3 Wake System Up Enable Bit** 0 = I^2C 3 wake system up function Disabled. 1 = I^2C 3 wake system up function Enabled.
[2]	**I2C2WKEN**	**I^2C 2 Wake System Up Enable Bit** 0 = I^2C 2 wake system up function Disabled. 1 = I^2C 2 wake system up function Enabled.
[1]	**I2C1WKEN**	**I^2C 1 Wake System Up Enable Bit** 0 = I^2C 1 wake system up function Disabled. 1 = I^2C 1 wake system up function Enabled.
[0]	**I2C0WKEN**	**I^2C 0 Wake System Up Enable Bit** 0 = I^2C 0 wake system up function Disabled. 1 = I^2C 0 wake system up function Enabled.

System Wakeup Source Status Register 0 (SYS_WKUPSSR0)

Register	Offset	R/W	Description	Reset Value
SYS_WKUPSSR0	SYS_BA+0x058	R/W	System Wakeup Source Status Register 0	0x0000_0000

31	30	29	28	27	26	25	24
Reserved						UR9WKST	UR8WKST
23	22	21	20	19	18	17	16
UR7WKST	UR6WKST	UR5WKST	UR4WKST	UR3WKST	UR2WKST	UR1WKST	UR0WKST
15	14	13	12	11	10	9	8
Reserved		TMR5WKST	TMR4WKST	TMR3WKST	TMR2WKST	TMR1WKST	TMR0WKST
7	6	5	4	3	2	1	0
EINT3WKST	EINT2WKST	EINT1WKST	EINT0WKST	GPIOWKST	Reserved	Reserved	WDTWKST

Bits	Description	
[31:26]	**Reserved**	Reserved.
[25]	**UR9WKST**	**UART 9 Wake System Up Status** 0 = UART 9 didn't wake system up. 1 = UART 9 wake system up.
[24]	**UR8WKST**	**UART 8 Wake System Up Status** 0 = UART 8 didn't wake system up. 1 = UART 8 wake system up.
[23]	**UR7WKST**	**UART 7 Wake System Up Status** 0 = UART 7 didn't wake system up. 1 = UART 7 wake system up.
[22]	**UR6WKST**	**UART 6 Wake System Up Status** 0 = UART 6 didn't wake system up. 1 = UART 6 wake system up.
[21]	**UR5WKST**	**UART 5 Wake System Up Status** 0 = UART 5 didn't wake system up. 1 = UART 5 wake system up.
[20]	**UR4WKST**	**UART 4 Wake System Up Status** 0 = UART 4 didn't wake system up. 1 = UART 4 wake system up.
[19]	**UR3WKST**	**UART 3 Wake System Up Status** 0 = UART 3 didn't wake system up. 1 = UART 3 wake system up.
[18]	**UR2WKST**	**UART 2 Wake System Up Status** 0 = UART 2 didn't wake system up. 1 = UART 2 wake system up.

[17]	**UR1WKST**	**UART 1 Wake System Up Status** 0 = UART 1 didn't wake system up. 1 = UART 1 wake system up.
[16]	**UR0WKST**	**UART 0 Wake System Up Status** 0 = UART 0 didn't wake system up. 1 = UART 0 wake system up.
[15:14]	**Reserved**	Reserved.
[13]	**TMR5WKST**	**TIMER 5 Wake System Up Status** 0 = TIMER 5 didn't wake system up. 1 = TIMER 5 wake system up.
[12]	**TMR4WKST**	**TIMER 4 Wake System Up Status** 0 = TIMER 4 didn't wake system up. 1 = TIMER 4 wake system up.
[11]	**TMR3WKST**	**TIMER 3 Wake System Up Status** 0 = TIMER 3 didn't wake system up. 1 = TIMER 3 wake system up.
[10]	**TMR2WKST**	**TIMER 2 Wake System Up Status** 0 = TIMER 2 didn't wake system up. 1 = TIMER 2 wake system up.
[9]	**TMR1WKST**	**TIMER 1 Wake System Up Status** 0 = TIMER 1 didn't wake system up. 1 = TIMER 1 wake system up.
[8]	**TMR0WKST**	**TIMER 0 Wake System Up Status** 0 = TIMER 0 didn't wake system up. 1 = TIMER 0 wake system up.
[7]	**EINT3WKST**	**External Interrupt 3 Wake System Up Status** 0 = External Interrupt 3 didn't wake system up. 1 = External Interrupt 3 wake system up.
[6]	**EINT2WKST**	**External Interrupt 2 Wake System Up Status** 0 = External Interrupt 2 didn't wake system up. 1 = External Interrupt 2 wake system up.
[5]	**EINT1WKST**	**External Interrupt 1 Wake System Up Status** 0 = External Interrupt 1 didn't wake system up. 1 = External Interrupt 1 wake system up.
[4]	**EINT0WKST**	**External Interrupt 0 Wake System Up Status** 0 = External Interrupt 0 didn't wake system up. 1 = External Interrupt 0 wake system up.
[3]	**GPIOWKST**	**GPIO Wake System Up Status** 0 = GPIO didn't wake system up. 1 = GPIO wake system up.
[2:1]	**Reserved**	Reserved.

[0]	**WDTWKST**	**WDT Wake System Up Status** 0 = WDT didn't wake system up. 1 = WDT wake system up.

System Wakeup Source Status Register 1 (SYS_WKUPSSR1)

Register	Offset	R/W	Description	Reset Value
SYS_WKUPSSR1	SYS_BA+0x05C	R/W	System Wakeup Source Status Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							ADCWKST
23	22	21	20	19	18	17	16
Reserved			SDHWKST	USBDWKST	USBHWKST	EMAC1WKST	EMAC0WKST
15	14	13	12	11	10	9	8
LVDWKST	Reserved			CAN3WKST	CAN2WKST	CAN1WKST	CAN0WKST
7	6	5	4	3	2	1	0
RTCWKST	Reserved			I2C3WKST	I2C2WKST	I2C1WKST	I2C0WKST

Bits	Description	
[31:25]	**Reserved**	Reserved.
[24]	**ADCWKST**	**ADC Wake System Up Status** 0 = ADC didn't wake system up. 1 = ADC wake system up.
[23:21]	**Reserved**	Reserved.
[20]	**SDHWKST**	**SDH Wake System Up Status** 0 = SDH didn't wake system up. 1 = SDH wake system up.
[19]	**USBDWKST**	**USB Device Wake System Up Status** 0 = USB device didn't wake system up. 1 = USB device wake system up.
[18]	**USBHWKST**	**USB Host Wake System Up Status** 0 = USB host didn't wake system up. 1 = USB host wake system up.
[17]	**EMAC1WKST**	**Ethernet MAC 1 Wake System Up Status** 0 = Ethernet MAC 1 didn't wake system up. 1 = Ethernet MAC 1 wake system up.
[16]	**EMAC0WKST**	**Ethernet MAC 0 Wake System Up Status** 0 = Ethernet MAC 0 didn't wake system up. 1 = Ethernet MAC 0 wake system up.
[15]	**LVDWKST**	**Low Voltage Detect Wake System Up Status** 0 = Low Voltage Detect didn't wake system up. 1 = Low Voltage Detect wake system up.
[14:12]	**Reserved**	Reserved.

[11]	**CAN3WKST**	**CAN 3 Wake System Up Status** 0 = CAN 3 didn't wake system up. 1 = CAN 3 wake system up.
[10]	**CAN2WKST**	**CAN 2 Wake System Up Status** 0 = CAN 2 didn't wake system up. 1 = CAN 2 wake system up.
[9]	**CAN1WKST**	**CAN 1 Wake System Up Status** 0 = CAN 1 didn't wake system up. 1 = CAN 1 wake system up.
[8]	**CAN0WKST**	**CAN 0 Wake System Up Status** 0 = CAN 0 didn't wake system up. 1 = CAN 0 wake system up.
[7]	**RTCWKST**	**RTC Wake System Up Status** 0 = RTC didn't wake system up. 1 = RTC wake system up.
[6:4]	**Reserved**	Reserved.
[3]	**I2C3WKST**	**I^2C 3 Wake System Up Status** 0 = I^2C 3 didn't wake system up. 1 = I^2C 3 wake system up.
[2]	**I2C2WKST**	**I^2C 2 Wake System Up Status** 0 = I^2C 2 didn't wake system up. 1 = I^2C 2 wake system up.
[1]	**I2C1WKST**	**I^2C 1 Wake System Up Status** 0 = I^2C 1 didn't wake system up. 1 = I^2C 1 wake system up.
[0]	**I2C0WKST**	**I^2C 0 Wake System Up Status** 0 = I^2C 0 didn't wake system up. 1 = I^2C 0 wake system up.

AHB IP Reset Control Register (SYS_AHBIPRST)

Register	Offset	R/W	Description	Reset Value
SYS_AHBIPRST	SYS_BA+0x060	R/W	AHB IP Reset Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							SDHRST
23	22	21	20	19	18	17	16
CRYPTORST	Reserved		FMIRST	USBDRST	USBHRST	EMAC1RST	EMAC0RST
15	14	13	12	11	10	9	8
Reserved				VCAP1RST	VCAP0RST	Reserved	I2SRST
7	6	5	4	3	2	1	0
GPIORST	SDICRST	PDMA1RST	PDMA0RST	EBIRST	CPURST	Reserved	CHIPRST

Bits	Description	
[31:25]	**Reserved**	Reserved.
[24]	**SDHRST**	**SDIO Controller Reset Enable Bit** 0 = SDIO controller reset Disabled. 1 = SDIO controller reset Enabled.
[23]	**CRYPTORST**	**Cryptographic Accelerator Reset Enable Bit** 0 = Cryptographic Accelerator reset Disabled. 1 = Cryptographic Accelerator reset Enabled.
[22:21]	**Reserved**	Reserved.
[20]	**FMIRST**	**FMI Controller Reset Enable Bit** 0 = FMI controller reset Disabled. 1 = FMI controller reset Enabled.
[19]	**USBDRST**	**USB Device Controller Reset Enable Bit** 0 = USB device controller reset Disabled. 1 = USB device controller reset Enabled.
[18]	**USBHRST**	**USB Host Controller (EHCI/OHCI) Reset Enable Bit** 0 = USB host controller (EHCI/OHCI) reset Disabled. 1 = USB host controller (EHCI/OHCI) reset Enabled.
[17]	**EMAC1RST**	**Ethernet MAC 1 Reset Enable Bit** 0 = Ethernet MAC 1 reset Disabled. 1 = Ethernet MAC 1 reset Enabled.
[16]	**EMAC0RST**	**Ethernet MAC 0 Reset Enable Bit** 0 = Ethernet MAC 0 reset Disabled. 1 = Ethernet MAC 0 reset Enabled.
[15:12]	**Reserved**	Reserved.

[11]	**VCAP1RST**	**Capture Sensor Interface 1 Reset Enable Bit** 0 = Capture sensor interface 1 reset Disabled. 1 = Capture sensor interface 1 reset Enabled.
[10]	**VCAP0RST**	**Capture Sensor Interface 0 Reset Enable Bit** 0 = Capture sensor interface 0 reset Disabled. 1 = Capture sensor interface 0 reset Enabled.
[9]	**Reserved**	Reserved.
[8]	**I2S**	**I²S Controller Reset Enable Bit** 0 = I²S controller reset Disabled. 1 = I²S controller reset Enabled.
[7]	**GPIORST**	**GPIO Reset Enable Bit** 0 = GPIO reset Disabled. 1 = GPIO reset Enabled.
[6]	**SDICRST**	**SDRAM Controller Reset Enable Bit** 0 = SDRAM controller reset Disabled. 1 = SDRAM Controller reset Enabled.
[5]	**PDMA1RST**	**PDMA1 Reset Enable Bit** 0 = PDMA1 reset Disabled. 1 = PDMA1 reset Enabled.
[4]	**PDMA0RST**	**PDMA0 Reset Enable Bit** 0 = PDMA0 reset Disabled. 1 = PDMA0 reset Enabled.
[2]	**CPURST**	**CPU Pulse Reset Enable Bit** This bit is used to generate a reset pulse to Arm926EJ-S™ CPU. When set this bit high, reset controller generates a 6 system clock long reset pulse to Arm926EJ-S™ CPU. After the reset completed, this bit will be clear to low automatically. 0 = CPU pulse reset Disabled. 1 = CPU pulse reset Enabled.
[1]	**Reserved**	Reserved.
[0]	**CHIP**	**Chip Reset Enable Bit** 0 = Chip reset Disabled. 1 = Chip reset Enabled.

APB IP Reset Control Register 0 (SYS_APBIPRST0)

Register	Offset	R/W	Description	Reset Value
SYS_APBIPRST0	SYS_BA+0x064	R/W	APB IP Reset Control Register 0	0x0000_0000

31	30	29	28	27	26	25	24
Reserved					Reserved	UART9RST	UART8RST
23	22	21	20	19	18	17	16
UART7RST	UART6RST	UART5RST	UART4RST	UART3RST	UART2RST	UART1RST	UART0RST
15	14	13	12	11	10	9	8
Reserved		TIMER5RST	TIMER4RST	TIMER3RST	TIMER2RST	TIMER1RST	TIMER0RST
7	6	5	4	3	2	1	0
Reserved			AICRST	Reserved			

Bits	Description	
[31:26]	**Reserved**	Reserved.
[25]	**UART9RST**	**UART 9 Reset Enable Bit** 0 = UART 9 reset Disabled. 1 = UART 9 reset Enabled.
[24]	**UART8RST**	**UART 8 Reset Enable Bit** 0 = UART 8 reset Disabled. 1 = UART 8 reset Enabled.
[23]	**UART7RST**	**UART 7 Reset Enable Bit** 0 = UART 7 reset Disabled. 1 = UART 7 reset Enabled.
[22]	**UART6RST**	**UART 6 Reset Enable Bit** 0 = UART 6 reset Disabled. 1 = UART 6 reset Enabled.
[21]	**UART5RST**	**UART 5 Reset Enable Bit** 0 = UART 5 reset Disabled. 1 = UART 5 reset Enabled.
[20]	**UART4RST**	**UART 4 Reset Enable Bit** 0 = UART 4 reset Disabled. 1 = UART 4 reset Enabled.
[19]	**UART3RST**	**UART 3 Reset Enable Bit** 0 = UART 3 reset Disabled. 1 = UART 3 reset Enabled.
[18]	**UART2RST**	**UART 2 Reset Enable Bit** 0 = UART 2 reset Disabled. 1 = UART 2 reset Enabled.

[17]	**UART1RST**	**UART 1 Reset Enable Bit** 0 = UART 1 reset Disabled. 1 = UART 1 reset Enabled.
[16]	**UART0RST**	**UART 0 Reset Enable Bit** 0 = UART 0 reset Disabled. 1 = UART 0 reset Enabled.
[15:14]	**Reserved**	Reserved.
[13]	**TIMER5RST**	**TIMER 5 Reset Enable Bit** 0 = TIMER 5 reset Disabled. 1 = TIMER 5 reset Enabled.
[12]	**TIMER4RST**	**TIMER 4 Reset Enable Bit** 0 = TIMER 4 reset Disabled. 1 = TIMER 4 reset Enabled.
[11]	**TIMER3RST**	**TIMER 3 Reset Enable Bit** 0 = TIMER 3 reset Disabled. 1 = TIMER 3 reset Enabled.
[10]	**TIMER2RST**	**TIMER 2 Reset Enable Bit** 0 = TIMER 2 reset Disabled. 1 = TIMER 2 reset Enabled.
[9]	**TIMER1RST**	**TIMER 1 Reset Enable Bit** 0 = TIMER 1 reset Disabled. 1 = TIMER 1 reset Enabled.
[8]	**TIMER0RST**	**TIMER 0 Reset Enable Bit** 0 = TIMER 0 reset Disabled. 1 = TIMER 0 reset Enabled.
[7:5]	**Reserved**	Reserved.
[4]	**AICRST**	**AIC Reset Enable Bit** 0 = AIC reset Disabled. 1 = AIC reset Enabled.
[3:0]	**Reserved**	Reserved.

APB IP Reset Control Register 1 (SYS_APBIPRST1)

Register	Offset	R/W	Description	Reset Value
SYS_APBIPRST1	SYS_BA+0x068	R/W	APB IP Reset Control Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved				PWM1RST	PWM0RST	Reserved	ADCRST
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		SMC1RST	SMC0RST	CAN3RST	CAN2RST	CAN1RST	CAN0RST
7	6	5	4	3	2	1	0
Reserved	SPI1RST	SPI0RST	QSPI0RST	I2C3RST	I2C2RST	I2C1RST	I2C0RST

Bits	Description	
[31:28]	**Reserved**	Reserved.
[27]	**PWM1RST**	**PWM1 Reset Enable Bit** 0 = PWM1 reset Disabled. 1 = PWM1 reset Enabled.
[26]	**PWM0RST**	**PWM0 Reset Enable Bit** 0 = PWM0 reset Disabled. 1 = PWM0 reset Enabled.
[25]	**Reserved**	Reserved.
[24]	**ADCRST**	**ADC Reset Enable Bit** 0 = ADC reset Disabled. 1 = ADC reset Enabled.
[23:14]	**Reserved**	Reserved.
[13]	**SMC1RST**	**SMC 1 Reset Enable Bit** 0 = SMC 1 reset Disabled. 1 = SMC 1 reset Enabled.
[12]	**SMC0RST**	**SMC 0 Reset Enable Bit** 0 = SMC 0 reset Disabled. 1 = SMC 0 reset Enabled.
[11]	**CAN3RST**	**CAN 3 Reset Enable Bit** 0 = CAN 3 reset Disabled. 1 = CAN 3 reset Enabled.
[10]	**CAN2RST**	**CAN 2 Reset Enable Bit** 0 = CAN 2 reset Disabled. 1 = CAN 2 reset Enabled.

[9]	**CAN1RST**	**CAN 1 Reset Enable Bit** 0 = CAN 1 reset Disabled. 1 = CAN 1 reset Enabled.
[8]	**CAN0RST**	**CAN 0 Reset Enable Bit** 0 = CAN 0 reset Disabled. 1 = CAN 0 reset Enabled.
[7]	**Reserved**	Reserved.
[6]	**SPI1RST**	**SPI 1 Reset Enable Bit** 0 = SPI 1 reset Disabled. 1 = SPI 1 reset Enabled.
[5]	**SPI0RST**	**SPI 1 Reset Enable Bit** 0 = SPI 0 reset Disabled. 1 = SPI 0 reset Enabled.
[4]	**QSPI0RST**	**QSPI 0 Reset Enable Bit** 0 = QSPI 0 reset Disabled. 1 = QSPI 0 reset Enabled.
[3]	**I2C3RST**	**I^2C 3 Reset Enable Bit** 0 = I^2C 3 reset Disabled. 1 = I^2C 3 reset Enabled.
[2]	**I2C2RST**	**I^2C 1 Reset Enable Bit** 0 = I^2C 2 reset Disabled. 1 = I^2C 2 reset Enabled.
[1]	**I2C1RST**	**I^2C 1 Reset Enable Bit** 0 = I^2C 1 reset Disabled. 1 = I^2C 1 reset Enabled.
[0]	**I2C0RST**	**I^2C 0 Reset Enable Bit** 0 = I^2C 0 reset Disabled. 1 = I^2C 0 reset Enabled.

Reset Source Active Status Register (SYS_RSTSTS)

Register	Offset	R/W	Description	Reset Value
SYS_RSTSTS	SYS_BA+0x06C	R/W	Reset Source Active Status Register	0x0000_00XX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved		WDTRSTS	CPURSTS	CHIPRSTS	LVRRSTS	PINRSTS	PORRSTS

Bits	Description	
[31:5]	**Reserved**	Reserved.
[5]	**WDTRSTS**	**Chip Reset by Watchdog Timer Status** 0 = No reset from watchdog timer. 1 = Watchdog timer had issued reset signal to reset the chip.
[4]	**CPURSTS**	**CPU Reset by CPU_LVL (AHBIPRST[1]) or CPU_PLS (AHBIPRST[2]) Status** 0 = No CPU reset from CPU_LVL (AHBIPRST[1]) or CPU_PLS (AHBIPRST[2]). 1 = CPU_LVL (AHBIPRST[1]) or CPU_PLS (AHBIPRST[2]) has been high to reset the CPU.
[3]	**CHIPRSTS**	**Chip Reset by CHIP (AHBIPRST[0]) Status** 0 = No reset from CHIP (AHBIPRST[0]). 1 = CHIP (AHBIPRST[0]) has been high to reset CPU.
[2]	**LVRRSTS**	**Chip Reset by LVRD Status** 0 = No reset from LVRD. 1 = LVRD had issued reset signal to reset the chip.
[1]	**PINRSTS**	**Chip Reset by NRESET Pin Status** 0 = No reset from nRESET pin. 1 = nRESET pin had issued reset signal to reset the chip.
[0]	**PORRSTS**	**Chip Reset by POR Status** 0 = No reset from POR. 1 = POR had issued reset signal to reset the chip.

GPIOA Low Byte Multiple Function Control Register (SYS_GPA_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPA_MFPL	SYS_BA+0x070	R/W	GPIOA Low Byte Multiple Function Control Register	0x0XXX_XX00

31	30	29	28	27	26	25	24
MFP_GPA7				MFP_GPA6			
23	22	21	20	19	18	17	16
MFP_GPA5				MFP_GPA4			
15	14	13	12	11	10	9	8
MFP_GPA3				MFP_GPA2			
7	6	5	4	3	2	1	0
MFP_GPA1				MFP_GPA0			

Bits	Description	
[31:28]	MFP_GPA7	Pin PA.7 Multi-function Pin Selection
[27:24]	MFP_GPA6	Pin PA.6 Multi-function Pin Selection
[23:20]	MFP_GPA5	Pin PA.5 Multi-function Pin Selection
[19:16]	MFP_GPA4	Pin PA.4 Multi-function Pin Selection
[15:12]	MFP_GPA3	Pin PA.3 Multi-function Pin Selection
[11:8]	MFP_GPA2	Pin PA.2 Multi-function Pin Selection
[7:4]	MFP_GPA1	Pin PA.1 Multi-function Pin Selection
[3:0]	MFP_GPA0	Pin PA.0 Multi-function Pin Selection

GPIOA High Byte Multiple Function Control Register (SYS_GPA_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPA_MFPH	SYS_BA+0x074	R/W	GPIOA High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPA15				MFP_GPA14			
23	22	21	20	19	18	17	16
MFP_GPA13				MFP_GPA12			
15	14	13	12	11	10	9	8
MFP_GPA11				MFP_GPA10			
7	6	5	4	3	2	1	0
MFP_GPA9				MFP_GPA8			

Bits	Description	
[31:28]	MFP_GPA15	Pin PA.15 Multi-function Pin Selection
[27:24]	MFP_GPA14	Pin PA.14 Multi-function Pin Selection
[23:20]	MFP_GPA13	Pin PA.13 Multi-function Pin Selection
[19:16]	MFP_GPA12	Pin PA.12 Multi-function Pin Selection
[15:12]	MFP_GPA11	Pin PA.11 Multi-function Pin Selection
[11:8]	MFP_GPA10	Pin PA.10 Multi-function Pin Selection
[7:4]	MFP_GPA9	Pin PA.9 Multi-function Pin Selection
[3:0]	MFP_GPA8	Pin PA.8 Multi-function Pin Selection

GPIOB Low Byte Multiple Function Control Register (SYS_GPB_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPB_MFPL	SYS_BA+0x078	R/W	GPIOB Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPB7				MFP_GPB6			
23	22	21	20	19	18	17	16
MFP_GPB5				MFP_GPB4			
15	14	13	12	11	10	9	8
MFP_GPB3				MFP_GPB2			
7	6	5	4	3	2	1	0
MFP_GPB1				MFP_GPB0			

Bits	Description	
[31:28]	MFP_GPB7	Pin PB.7 Multi-function Pin Selection
[27:24]	MFP_GPB6	Pin PB.6 Multi-function Pin Selection
[23:20]	MFP_GPB5	Pin PB.5 Multi-function Pin Selection
[19:16]	MFP_GPB4	Pin PB.4 Multi-function Pin Selection
[15:12]	MFP_GPB3	Pin PB.3 Multi-function Pin Selection
[11:8]	MFP_GPB2	Pin PB.2 Multi-function Pin Selection
[7:4]	MFP_GPB1	Pin PB.1 Multi-function Pin Selection
[3:0]	MFP_GPB0	Pin PB.0 Multi-function Pin Selection

GPIOB High Byte Multiple Function Control Register (SYS_GPB_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPB_MFPH	SYS_BA+0x07C	R/W	GPIOB High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
MFP_GPB13				MFP_GPB12			
15	14	13	12	11	10	9	8
MFP_GPB11				MFP_GPB10			
7	6	5	4	3	2	1	0
MFP_GPB9				MFP_GPB8			

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:20]	**MFP_GPB13**	**Pin PB.13 Multi-function Pin Selection**
[19:16]	**MFP_GPB12**	**Pin PB.12 Multi-function Pin Selection**
[15:12]	**MFP_GPB11**	**Pin PB.11 Multi-function Pin Selection**
[11:8]	**MFP_GPB10**	**Pin PB.10 Multi-function Pin Selection**
[7:4]	**MFP_GPB9**	**Pin PB.9 Multi-function Pin Selection**
[3:0]	**MFP_GPB8**	**Pin PB.8 Multi-function Pin Selection**

GPIOC Low Byte Multiple Function Control Register (SYS_GPC_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPC_MFPL	SYS_BA+0x080	R/W	GPIOC Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPC7				MFP_GPC6			
23	22	21	20	19	18	17	16
MFP_GPC5				MFP_GPC4			
15	14	13	12	11	10	9	8
MFP_GPC3				MFP_GPC2			
7	6	5	4	3	2	1	0
MFP_GPC1				MFP_GPC0			

Bits	Description	
[31:28]	MFP_GPC7	Pin PC.7 Multi-function Pin Selection
[27:24]	MFP_GPC6	Pin PC.6 Multi-function Pin Selection
[23:20]	MFP_GPC5	Pin PC.5 Multi-function Pin Selection
[19:16]	MFP_GPC4	Pin PC.4 Multi-function Pin Selection
[15:12]	MFP_GPC3	Pin PC.3 Multi-function Pin Selection
[11:8]	MFP_GPC2	Pin PC.2 Multi-function Pin Selection
[7:4]	MFP_GPC1	Pin PC.1 Multi-function Pin Selection
[3:0]	MFP_GPC0	Pin PC.0 Multi-function Pin Selection

GPIOC High Byte Multiple Function Control Register (SYS_GPC_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPC_MFPH	SYS_BA+0x084	R/W	GPIOC High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPC15				MFP_GPC14			
23	22	21	20	19	18	17	16
MFP_GPC13				MFP_GPC12			
15	14	13	12	11	10	9	8
MFP_GPC11				MFP_GPC10			
7	6	5	4	3	2	1	0
MFP_GPC9				MFP_GPC8			

Bits	Description	
[31:28]	MFP_GPC15	Pin PC.15 Multi-function Pin Selection
[27:24]	MFP_GPC14	Pin PC.14 Multi-function Pin Selection
[23:20]	MFP_GPC13	Pin PC.13 Multi-function Pin Selection
[19:16]	MFP_GPC12	Pin PC.12 Multi-function Pin Selection
[15:12]	MFP_GPC11	Pin PC.11 Multi-function Pin Selection
[11:8]	MFP_GPC10	Pin PC.10 Multi-function Pin Selection
[7:4]	MFP_GPC9	Pin PC.9 Multi-function Pin Selection
[3:0]	MFP_GPC8	Pin PC.8 Multi-function Pin Selection

GPIOD Low Byte Multiple Function Control Register (SYS_GPD_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPD_MFPL	SYS_BA+0x088	R/W	GPIOD Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPD7				MFP_GPD6			
23	22	21	20	19	18	17	16
MFP_GPD5				MFP_GPD4			
15	14	13	12	11	10	9	8
MFP_GPD3				MFP_GPD2			
7	6	5	4	3	2	1	0
MFP_GPD1				MFP_GPD0			

Bits	Description	
[31:28]	MFP_GPD7	Pin PD.7 Multi-function Pin Selection
[27:24]	MFP_GPD6	Pin PD.6 Multi-function Pin Selection
[23:20]	MFP_GPD5	Pin PD.5 Multi-function Pin Selection
[19:16]	MFP_GPD4	Pin PD.4 Multi-function Pin Selection
[15:12]	MFP_GPD3	Pin PD.3 Multi-function Pin Selection
[11:8]	MFP_GPD2	Pin PD.2 Multi-function Pin Selection
[7:4]	MFP_GPD1	Pin PD.1 Multi-function Pin Selection
[3:0]	MFP_GPD0	Pin PD.0 Multi-function Pin Selection

GPIOD High Byte Multiple Function Control Register (SYS_GPD_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPD_MFPH	SYS_BA+0x08C	R/W	GPIOD High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPD15				MFP_GPD14			
23	22	21	20	19	18	17	16
MFP_GPD13				MFP_GPD12			
15	14	13	12	11	10	9	8
MFP_GPD11				MFP_GPD10			
7	6	5	4	3	2	1	0
MFP_GPD9				MFP_GPD8			

Bits	Description	
[31:28]	MFP_GPD15	Pin PD.15 Multi-function Pin Selection
[27:24]	MFP_GPD14	Pin PD.14 Multi-function Pin Selection
[23:20]	MFP_GPD13	Pin PD.13 Multi-function Pin Selection
[19:16]	MFP_GPD12	Pin PD.12 Multi-function Pin Selection
[15:12]	MFP_GPD11	Pin PD.11 Multi-function Pin Selection
[11:8]	MFP_GPD10	Pin PD.10 Multi-function Pin Selection
[7:4]	MFP_GPD9	Pin PD.9 Multi-function Pin Selection
[3:0]	MFP_GPD8	Pin PD.8 Multi-function Pin Selection

GPIOE Low Byte Multiple Function Control Register (SYS_GPE_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPE_MFPL	SYS_BA+0x090	R/W	GPIOE Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPE7				MFP_GPE6			
23	22	21	20	19	18	17	16
MFP_GPE5				MFP_GPE4			
15	14	13	12	11	10	9	8
MFP_GPE3				MFP_GPE2			
7	6	5	4	3	2	1	0
MFP_GPE1				MFP_GPE0			

Bits	Description	
[31:28]	MFP_GPE7	Pin PE.7 Multi-function Pin Selection
[27:24]	MFP_GPE6	Pin PE.6 Multi-function Pin Selection
[23:20]	MFP_GPE5	Pin PE.5 Multi-function Pin Selection
[19:16]	MFP_GPE4	Pin PE.4 Multi-function Pin Selection
[15:12]	MFP_GPE3	Pin PE.3 Multi-function Pin Selection
[11:8]	MFP_GPE2	Pin PE.2 Multi-function Pin Selection
[7:4]	MFP_GPE1	Pin PE.1 Multi-function Pin Selection
[3:0]	MFP_GPE0	Pin PE.0 Multi-function Pin Selection

GPIOE High Byte Multiple Function Control Register (SYS_GPE_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPE_MFPH	SYS_BA+0x094	R/W	GPIOE High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				MFP_GPE12			
15	14	13	12	11	10	9	8
MFP_GPE11				MFP_GPE10			
7	6	5	4	3	2	1	0
MFP_GPE9				MFP_GPE8			

Bits	Description	
[31:20]	**Reserved**	Reserved.
[19:16]	**MFP_GPE12**	**Pin PE.12 Multi-function Pin Selection**
[15:12]	**MFP_GPE11**	**Pin PE.11 Multi-function Pin Selection**
[11:8]	**MFP_GPE10**	**Pin PE.10 Multi-function Pin Selection**
[7:4]	**MFP_GPE9**	**Pin PE.9 Multi-function Pin Selection**
[3:0]	**MFP_GPE8**	**Pin PE.8 Multi-function Pin Selection**

GPIOF Low Byte Multiple Function Control Register (SYS_GPF_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPF_MFPL	SYS_BA+0x098	R/W	GPIOF Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPF7				MFP_GPF6			
23	22	21	20	19	18	17	16
MFP_GPF5				MFP_GPF4			
15	14	13	12	11	10	9	8
MFP_GPF3				MFP_GPF2			
7	6	5	4	3	2	1	0
MFP_GPF1				MFP_GPF0			

Bits	Description	
[31:28]	MFP_GPF7	Pin PF.7 Multi-function Pin Selection
[27:24]	MFP_GPF6	Pin PF.6 Multi-function Pin Selection
[23:20]	MFP_GPF5	Pin PF.5 Multi-function Pin Selection
[19:16]	MFP_GPF4	Pin PF.4 Multi-function Pin Selection
[15:12]	MFP_GPF3	Pin PF.3 Multi-function Pin Selection
[11:8]	MFP_GPF2	Pin PF.2 Multi-function Pin Selection
[7:4]	MFP_GPF1	Pin PF.1 Multi-function Pin Selection
[3:0]	MFP_GPF0	Pin PF.0 Multi-function Pin Selection

GPIOF High Byte Multiple Function Control Register (SYS_GPF_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPF_MFPH	SYS_BA+0x09C	R/W	GPIOF High Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved				MFP_GPF12			
15	14	13	12	11	10	9	8
MFP_GPF11				MFP_GPF10			
7	6	5	4	3	2	1	0
MFP_GPF9				MFP_GPF8			

Bits	Description	
[31:20]	**Reserved**	Reserved.
[19:16]	**MFP_GPF12**	**Pin PF.12 Multi-function Pin Selection**
[15:12]	**MFP_GPF11**	**Pin PF.11 Multi-function Pin Selection**
[11:8]	**MFP_GPF10**	**Pin PF.10 Multi-function Pin Selection**
[7:4]	**MFP_GPF9**	**Pin PF.9 Multi-function Pin Selection**
[3:0]	**MFP_GPF8**	**Pin PF.8 Multi-function Pin Selection**

GPIOG Low Byte Multiple Function Control Register (SYS_GPG_MFPL)

Register	Offset	R/W	Description	Reset Value
SYS_GPG_MFPL	SYS_BA+0x0A0	R/W	GPIOG Low Byte Multiple Function Control Register	0x0000_0000

31	30	29	28	27	26	25	24
MFP_GPG7				MFP_GPG6			
23	22	21	20	19	18	17	16
MFP_GPG5				MFP_GPG4			
15	14	13	12	11	10	9	8
MFP_GPG3				MFP_GPG2			
7	6	5	4	3	2	1	0
MFP_GPG1				MFP_GPG0			

Bits	Description	
[31:28]	MFP_GPG7	Pin PG.7 Multi-function Pin Selection
[27:24]	MFP_GPG6	Pin PG.6 Multi-function Pin Selection
[23:20]	MFP_GPG5	Pin PG.5 Multi-function Pin Selection
[19:16]	MFP_GPG4	Pin PG.4 Multi-function Pin Selection
[15:12]	MFP_GPG3	Pin PG.3 Multi-function Pin Selection
[11:8]	MFP_GPG2	Pin PG.2 Multi-function Pin Selection
[7:4]	MFP_GPG1	Pin PG.1 Multi-function Pin Selection
[3:0]	MFP_GPG0	Pin PG.0 Multi-function Pin Selection

GPIOG High Byte Multiple Function Control Register (SYS_GPG_MFPH)

Register	Offset	R/W	Description	Reset Value
SYS_GPG_MFPH	SYS_BA+0x0A4	R/W	GPIOG High Byte Multiple Function Control Register	0xXXXX_X000

31	30	29	28	27	26	25	24
MFP_GPG15				MFP_GPG14			
23	22	21	20	19	18	17	16
MFP_GPG13				MFP_GPG12			
15	14	13	12	11	10	9	8
MFP_GPG11				MFP_GPG10			
7	6	5	4	3	2	1	0
MFP_GPG9				MFP_GPG8			

Bits	Description	
[31:28]	MFP_GPG15	Pin PG.15 Multi-function Pin Selection
[27:24]	MFP_GPG14	Pin PG.14 Multi-function Pin Selection
[23:20]	MFP_GPG13	Pin PG.13 Multi-function Pin Selection
[19:16]	MFP_GPG12	Pin PG.12 Multi-function Pin Selection
[15:12]	MFP_GPG11	Pin PG.11 Multi-function Pin Selection
[11:8]	MFP_GPG10	Pin PG.10 Multi-function Pin Selection
[7:4]	MFP_GPG9	Pin PG.9 Multi-function Pin Selection
[3:0]	MFP_GPG8	Pin PG.8 Multi-function Pin Selection

DDR I/O Driving Strength Control Register (SYS_DDR_DSCTL)

Register	Offset	R/W	Description	Reset Value
SYS_DDR_DSCTL	SYS_BA+0x0F0	R/W	DDR I/O Driving Strength Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
DATA_DS		ADDR_DS		CTRL_DS		CLK_DS	

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7:6]	**DATA_DS**	**DDR Data I/O Driving Strength Selection** This bit controls the driving strength for DDR I/O used as data. 00 = Reserved. 01 = Reduced Strength. 10 = Reserved. 11 = Full Strength.
[5:4]	**ADDR_DS**	**DDR Address I/O Driving Strength Selection** This bit controls the driving strength for DDR I/O used as address. 00 = Reserved. 01 = Reduced Strength. 10 = Reserved. 11 = Full Strength.
[3:2]	**CTRL_DS**	**DDR Control I/O Driving Strength Selection** This bit controls the driving strength for DDR I/O used as control signals. 00 = Reserved. 01 = Reduced Strength. 10 = Reserved. 11 = Full Strength.
[1:0]	**CLK_DS**	**DDR Clock I/O Driving Strength Selection** This bit controls the driving strength for DDR I/O used as clock. 00 = Reserved. 01 = Reduced Strength. 10 = Reserved. 11 = Full Strength.

GPIOB Low Byte Driving Strength Control Register (SYS_GPBL_DSCTL)

Register	Offset	R/W	Description	Reset Value
SYS_GPBL_DSCTL	SYS_BA+0x0F4	R/W	GPIOB Low Byte Driving Strength Control Register	0x4444_4444

31	30	29	28	27	26	25	24
DS_GPB7				DS_GPB6			
23	22	21	20	19	18	17	16
DS_GPB5				DS_GPB4			
15	14	13	12	11	10	9	8
DS_GPB3				DS_GPB2			
7	6	5	4	3	2	1	0
DS_GPB1				DS_GPB0			

Bits	Description	
[31:28]	DS_GPB7	**Pin PB.7 Driving Strength Selection** This field controls the pin PB.7 driving strength 000 = Pin PB.7 driving strength is 2.2mA. 001 = Pin PB.7 driving strength is 6.5mA. 010 = Pin PB.7 driving strength is 8.7mA. 011 = Pin PB.7 driving strength is 13.0mA. 100 = Pin PB.7 driving strength is 15.2mA. 101 = Pin PB.7 driving strength is 19.5mA. 110 = Pin PB.7 driving strength is 21.7mA. 111 = Pin PB.7 driving strength is 26.1mA. Others = Reserved.
[27:24]	DS_GPB6	**Pin PB.6 Driving Strength Selection** This field controls the pin PB.6 driving strength 000 = Pin PB.6 driving strength is 2.2mA. 001 = Pin PB.6 driving strength is 6.5mA. 010 = Pin PB.6 driving strength is 8.7mA. 011 = Pin PB.6 driving strength is 13.0mA. 100 = Pin PB.6 driving strength is 15.2mA. 101 = Pin PB.6 driving strength is 19.5mA. 110 = Pin PB.6 driving strength is 21.7mA. 111 = Pin PB.6 driving strength is 26.1mA. Others = Reserved.

[23:20]	**DS_GPB5**	**Pin PB.5 Driving Strength Selection** This field controls the pin PB.5 driving strength 000 = Pin PB.5 driving strength is 2.2mA. 001 = Pin PB.5 driving strength is 6.5mA. 010 = Pin PB.5 driving strength is 8.7mA. 011 = Pin PB.5 driving strength is 13.0mA. 100 = Pin PB.5 driving strength is 15.2mA. 101 = Pin PB.5 driving strength is 19.5mA. 110 = Pin PB.5 driving strength is 21.7mA. 111 = Pin PB.5 driving strength is 26.1mA. Others = Reserved.
[19:16]	**DS_GPB4**	**Pin PB.4 Driving Strength Selection** This field controls the pin PB.4 driving strength 000 = Pin PB.4 driving strength is 2.2mA. 001 = Pin PB.4 driving strength is 6.5mA. 010 = Pin PB.4 driving strength is 8.7mA. 011 = Pin PB.4 driving strength is 13.0mA. 100 = Pin PB.4 driving strength is 15.2mA. 101 = Pin PB.4 driving strength is 19.5mA. 110 = Pin PB.4 driving strength is 21.7mA. 111 = Pin PB.4 driving strength is 26.1mA. Others = Reserved.
[15:12]	**DS_GPB3**	**Pin PB.3 Driving Strength Selection** This field controls the pin PB.3 driving strength 000 = Pin PB.3 driving strength is 2.2mA. 001 = Pin PB.3 driving strength is 6.5mA. 010 = Pin PB.3 driving strength is 8.7mA. 011 = Pin PB.3 driving strength is 13.0mA. 100 = Pin PB.3 driving strength is 15.2mA. 101 = Pin PB.3 driving strength is 19.5mA. 110 = Pin PB.3 driving strength is 21.7mA. 111 = Pin PB.3 driving strength is 26.1mA. Others = Reserved.
[11:8]	**DS_GPB2**	**Pin PB.2 Driving Strength Selection** This field controls the pin PB.2 driving strength 000 = Pin PB.2 driving strength is 2.2mA. 001 = Pin PB.2 driving strength is 6.5mA. 010 = Pin PB.2 driving strength is 8.7mA. 011 = Pin PB.2 driving strength is 13.0mA. 100 = Pin PB.2 driving strength is 15.2mA. 101 = Pin PB.2 driving strength is 19.5mA. 110 = Pin PB.2 driving strength is 21.7mA. 111 = Pin PB.2 driving strength is 26.1mA. Others = Reserved.

[7:4]	**DS_GPB1**	**Pin PB.1 Driving Strength Selection** This field controls the pin PB.1 driving strength 000 = Pin PB.1 driving strength is 2.2mA. 001 = Pin PB.1 driving strength is 6.5mA. 010 = Pin PB.1 driving strength is 8.7mA. 011 = Pin PB.1 driving strength is 13.0mA. 100 = Pin PB.1 driving strength is 15.2mA. 101 = Pin PB.1 driving strength is 19.5mA. 110 = Pin PB.1 driving strength is 21.7mA. 111 = Pin PB.1 driving strength is 26.1mA. Others = Reserved.
[3:0]	**DS_GPB0**	**Pin PB.0 Driving Strength Selection** This field controls the pin PB.0 driving strength 000 = Pin PB.0 driving strength is 2.2mA. 001 = Pin PB.0 driving strength is 6.5mA. 010 = Pin PB.0 driving strength is 8.7mA. 011 = Pin PB.0 driving strength is 13.0mA. 100 = Pin PB.0 driving strength is 15.2mA. 101 = Pin PB.0 driving strength is 19.5mA. 110 = Pin PB.0 driving strength is 21.7mA. 111 = Pin PB.0 driving strength is 26.1mA. Others = Reserved.

Power-On-reset Disable Control Register (SYS_PORDISCR)

Register	Offset	R/W	Description	Reset Value
SYS_PORDISCR	SYS_BA+0x100	R/W	Power-On-reset Disable Control Register	0x0000_00XX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
POR_DIS_CODE							
7	6	5	4	3	2	1	0
POR_DIS_CODE							

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15:0]	**POR_DIS_CODE**	**Power-on-reset Disable Code (Write-protection Bits)** When powered on, the Power-On-Reset (POR) circuit generates a reset signal to reset whole chip function. However, after power is ready, the POR circuit would consume a few power. To minimize the POR circuit power consumption, user to disable POR circuit by writing 0x5AA5 to this field. The POR circuit will become active again when this field is set to other value or chip is reset by other reset source, including /RESET pin, Watchdog, LVR reset and the software chip reset function. This field is protected. It means that before programming it, user has to write “59h”, “16h” and “88h” to address 0xB000_01FC continuously to disable the register protection. Refer to the register REGWRPROT at address SYS_BA+0x1FC for detail.

Reset Pin De-bounce Control Register (SYS_RSTDEBCTL)

Register	Offset	R/W	Description	Reset Value
SYS_RSTDEBCTL	SYS_BA+0x10C	R/W	Reset Pin De-bounce Control Register	0x0000_04B0

31	30	29	28	27	26	25	24
RSTDEBEN	Reserved						
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
DEBCNT							
7	6	5	4	3	2	1	0
DEBCNT							

Bits	Description	
[31]	**RSTDEBEN**	**Reset Pin De-bounce Enable Bit** 0 = Reset pin de-bounce Disabled. (Default) 1 = Reset pin de-bounce Enabled.
[31:16]	**Reserved**	Reserved.
[15:0]	**DEBCNT**	**Power-on-reset Disable Code (Write-protection Bits)** This 16-bit external RESET De-bounce Counter can specify the external RESET de-bounce time up to around 5.46ms (0xFFFF) @ XIN=12 MHz. The default external RESET de-bounce time is 0.1ms (0x04B0) @ XIN = 12 MHz.

Register Write-protection Control Register (SYS_REGWPCTL)

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register REGWRPROT address at 0xB000_01FC continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

After the protection is disabled, user can check the protection disable bit at address 0xB000_01FC bit0, 1 is protection disable, and 0 is protection enable. Then user can update the target protected register value and then write any data to the address “0xB000_01FC” to enable register protection.

This register is write for disable/enable register protection and read for the REGWPCTL status

Register	Offset	R/W	Description	Reset Value
SYS_REGWPCTL	SYS_BA+0x1FC	R/W	Register Write-protection Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
REGWPCTL							

Bits	Description	
[31:8]	**Reserved**	Reserved.
[7:0]	**REGWPCTL**	**Register Write Protection Code** Some registers have write-protection function. Writing these registers has to disable the protected function by writing the sequence value “59h”, “16h”, “88h” to this field. After this sequence is completed, the REGWPCTL bit will be set to 1 and write-protection registers can be normal write. **REGWPCTL[0]** **Register Write Protection Disable Index** 0 = Write-protection Enabled for writing protected registers. Any write to the protected register is ignored. 1 = Write-protection Disabled for writing protected registers.

[0]	**REGWPCTL**	**Register Write-protection Disable Indicator (Read Only)** 0 = Write-protection Enabled for writing protected registers. Any write to the protected register is ignored. 1 = Write-protection Disabled for writing protected registers. The protected registers are: SYS_PDID: Product Identifier Register, address 0xB000_0000. SYS_PWRON: Power-On Setting Register, address 0xB000_0004. SYS_MISCFCR: Miscellaneous Function Control Register, address 0xB000_0030. SYS_AHBIPRST: AHB IP Reset Control Register, address 0xB000_0060. SYS_APBIPRST0: APB IP Reset Control Register 0, address 0xB000_0064. SYS_APBIPRST1: APB IP Reset Control Register 1, address 0xB000_0068. SYS_PORDISCR: Power-On-Reset Disable Control Register, address 0xB000_0100. SYS_RSTDEBCTL: Reset Pin De-bounce Control Register, address 0xB000_010C. WDT_CTL: WDT Control Register, address 0xB004_0000 WDT_ALTCTL: WDT Alternative Control Register, address 0xB004_0004

6.3 Clock Controller

6.3.1 Overview

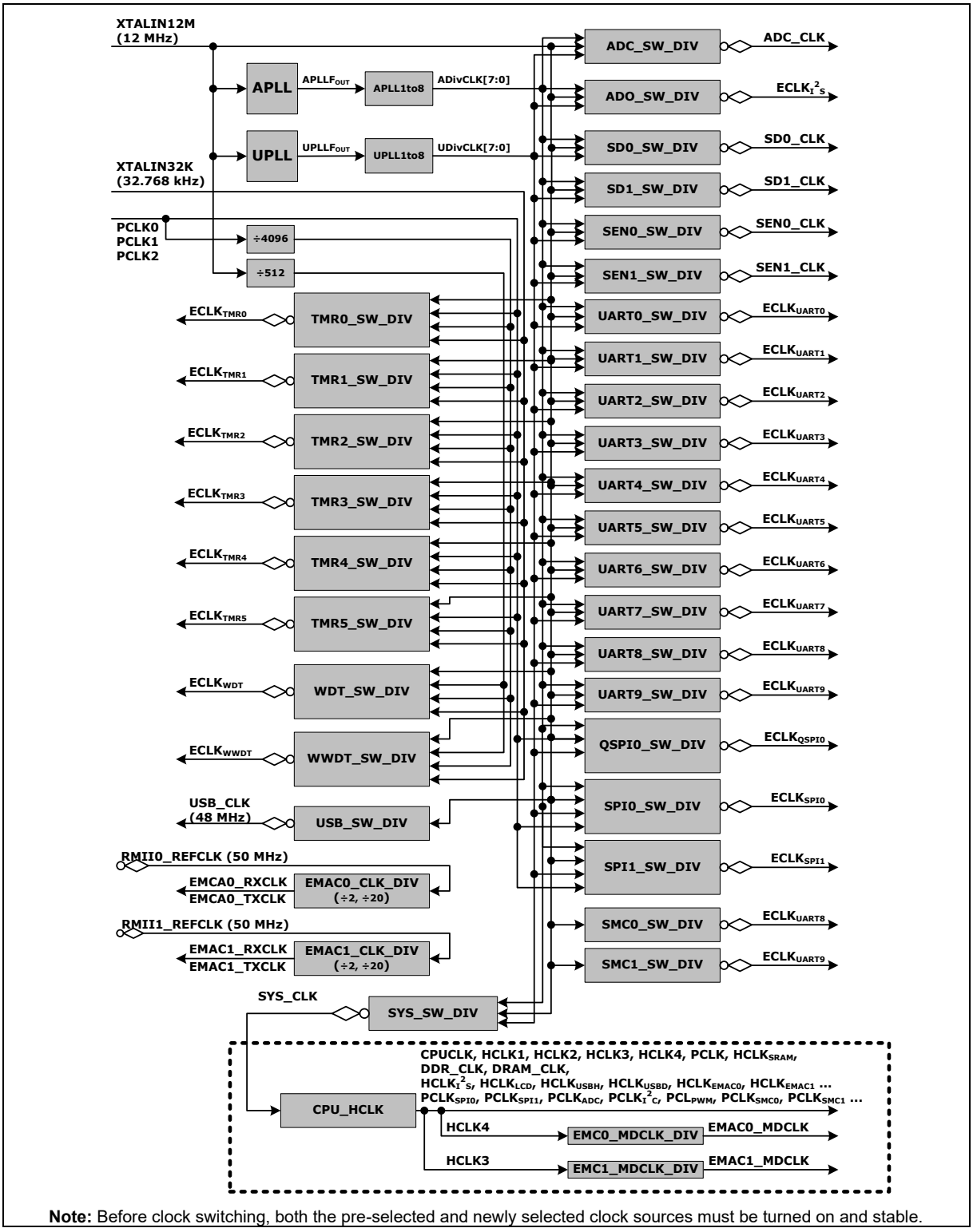
The clock controller generates all clocks for Video, Audio, CPU, system bus and all functionalities. This chip includes two PLL modules. The clock source for each functionality comes from the PLL, or from the external crystal input directly. For each clock there is a bit on the CLKEN register to control the clock ON or OFF individually, and the divider setting is in the CLK_DIVCTL register. The register can also be used to control the clock enable or disable for power control.

6.3.2 Features

- Supports two PLLs, up to 500 MHz, for high performance system operation
- External 12 MHz high speed crystal input for precise timing operation
- External 32.768 kHz low speed crystal input for RTC function and low speed clock source

6.3.3 Block Diagram

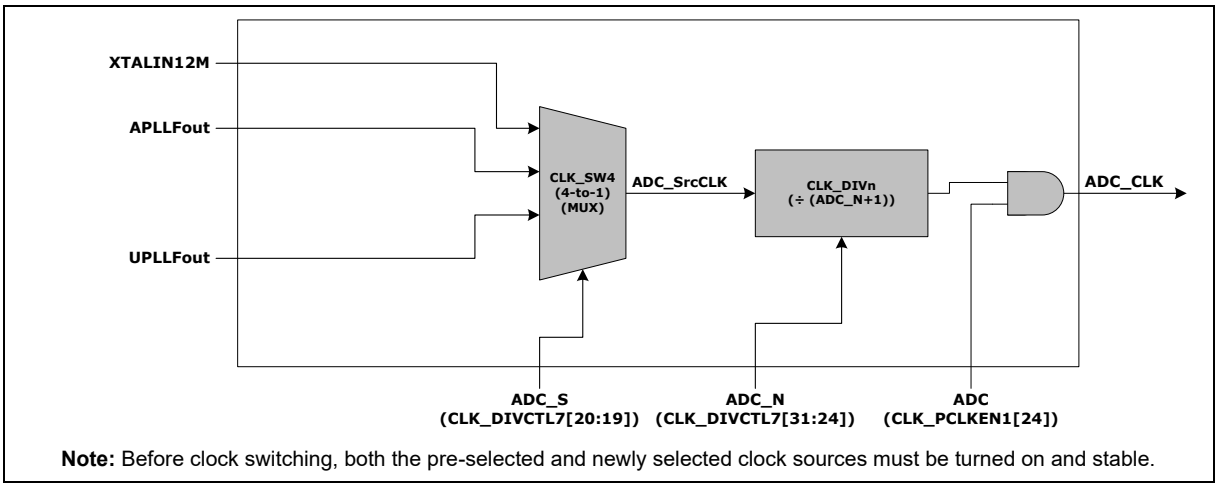
6.3.3.1 Clock Controller Top View



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-1 Clock Controller Block Diagram

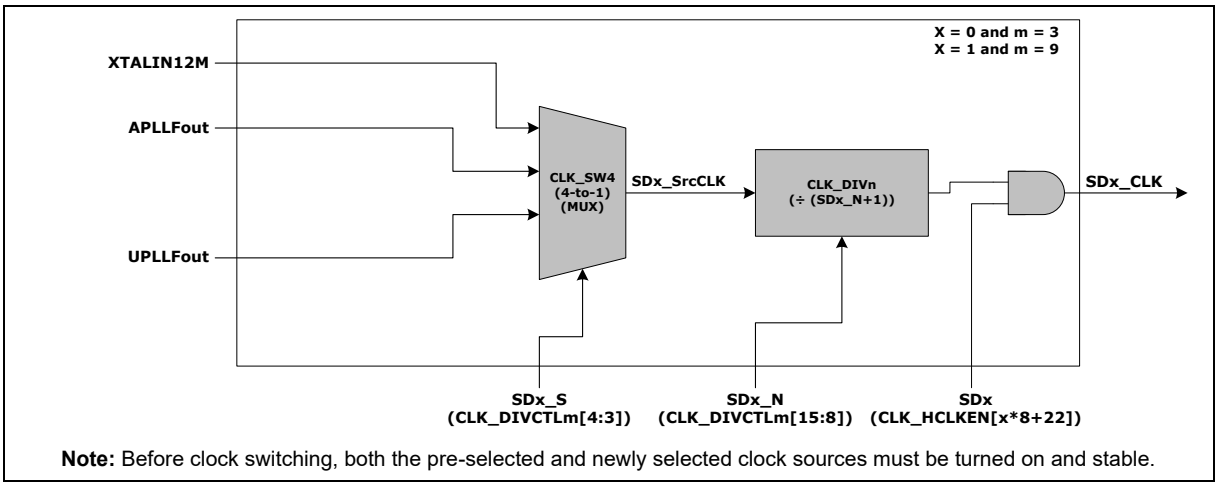
6.3.3.2 ADC Controller Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-2 ADC Controller Clock Divider Block Diagram

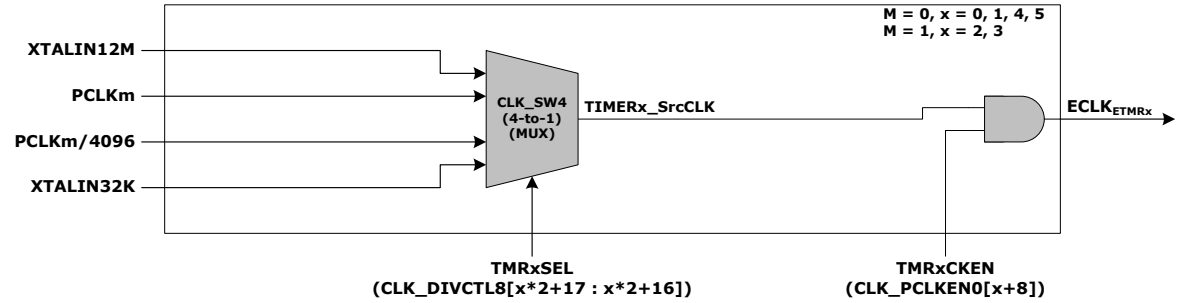
6.3.3.3 SD Card Host Controller Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-3 SD Card Host Controller Clock Divider Block Diagram

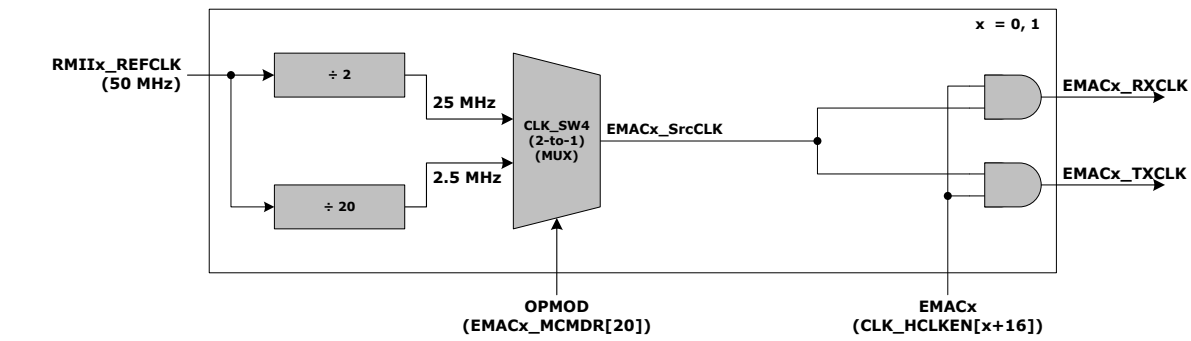
6.3.3.4 Timer Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-4 Timer Clock Divider Clock Diagram

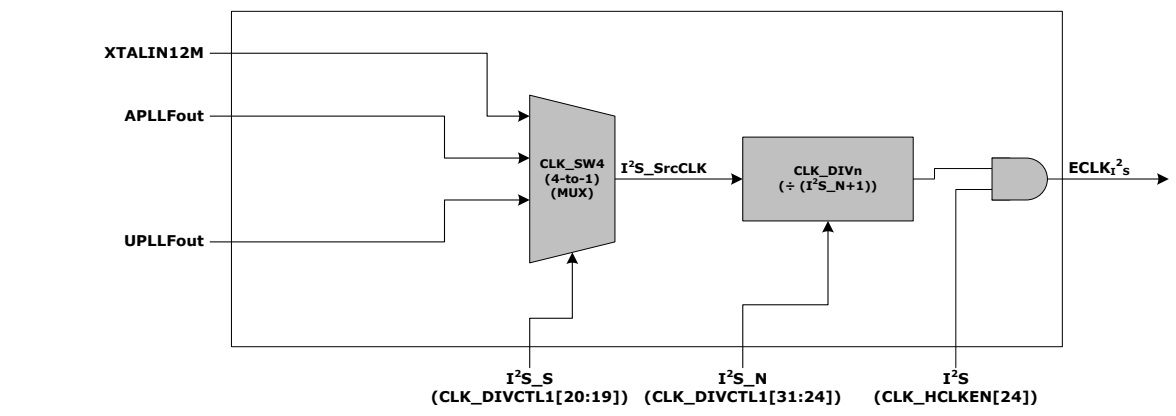
6.3.3.5 Ethernet MAC Controller Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-5 Ethernet MAC Controller Clock Divider Block Diagram

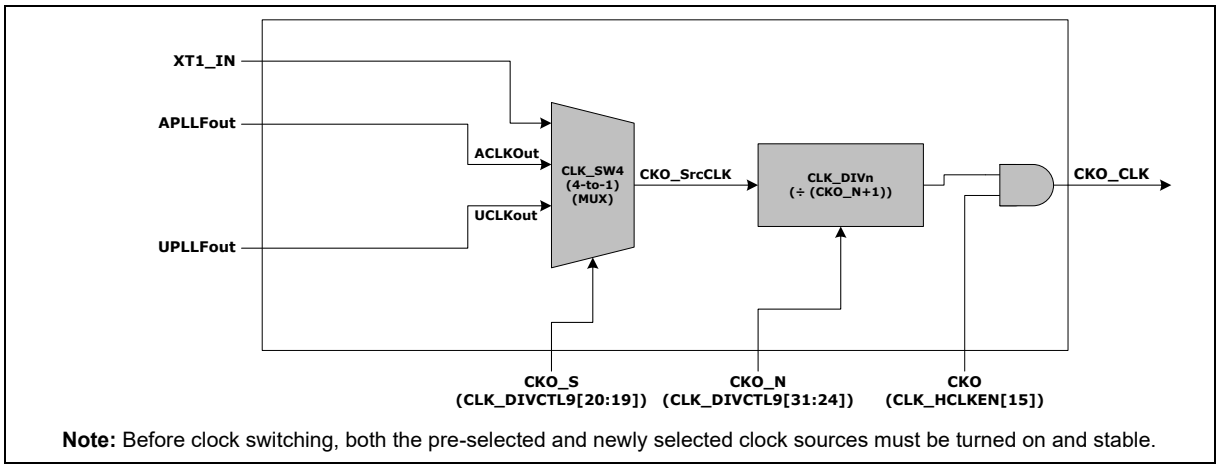
6.3.3.6 I^2S Controller Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-6 I^2S Controller Clock Divider Block Diagram

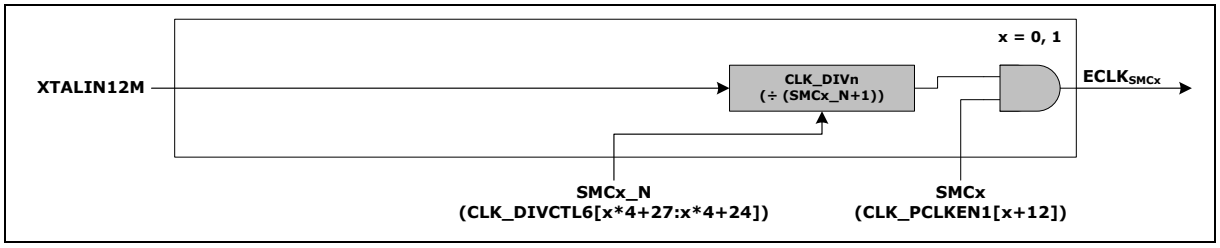
6.3.3.7 Reference Clock Output Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-7 Reference Clock Output Divider Block Diagram

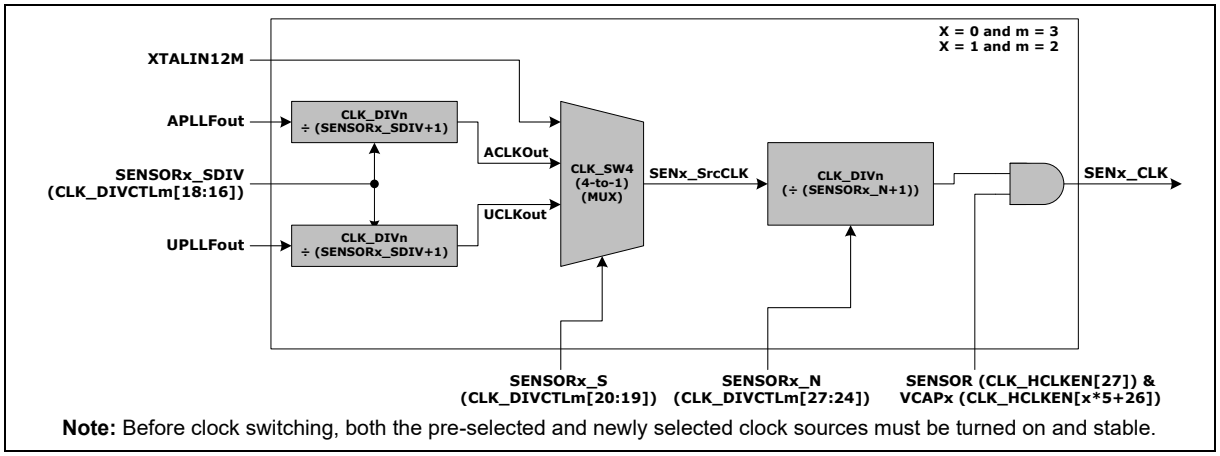
6.3.3.8 Smart Card Host Controller Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-8 Smart Card Host Controller Clock Divider Block Diagram

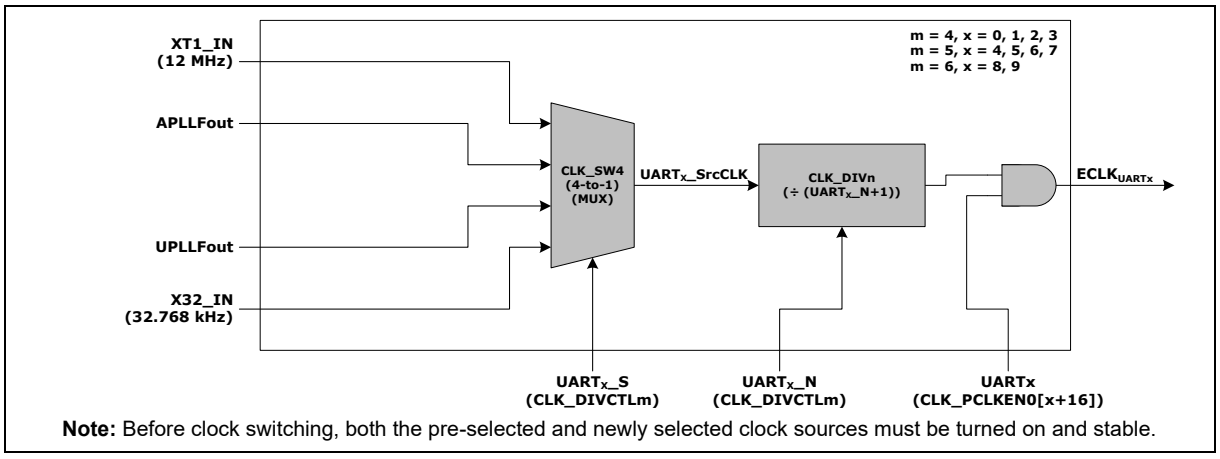
6.3.3.9 CMOS Sensor Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-9 CMOS Sensor Controller Divider Block Diagram

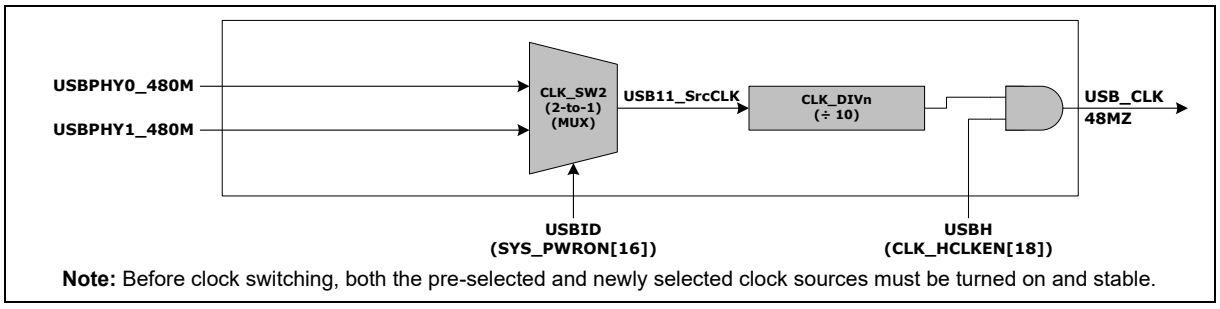
6.3.3.10 UART Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-10 UART Clock Divider Block Diagram

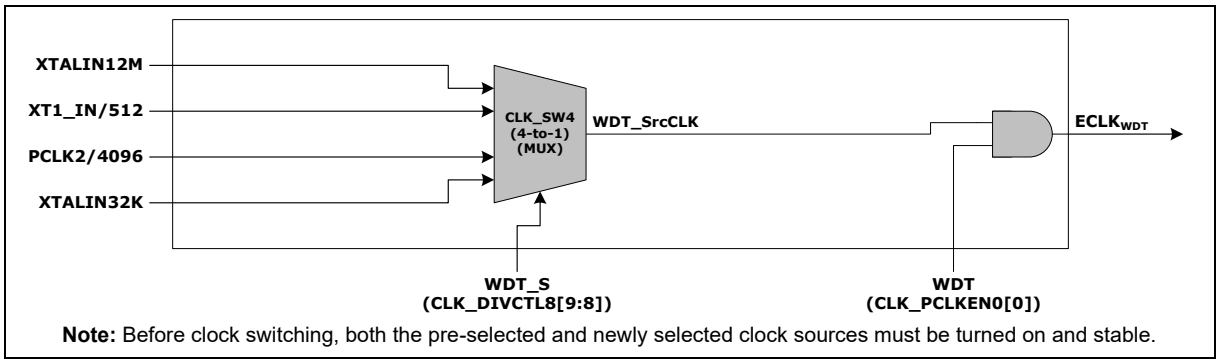
6.3.3.11 USB 1.1 Host 48 MHz Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-11 USB 1.1 Host Controller 48 MHz Clock Divider Block Diagram

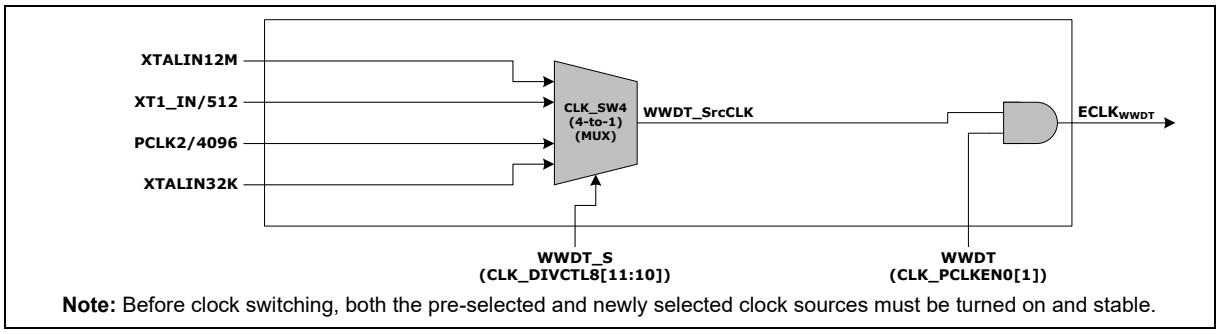
6.3.3.12 Watchdog Timer Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-12 Watchdog Timer Clock Divider Block Diagram

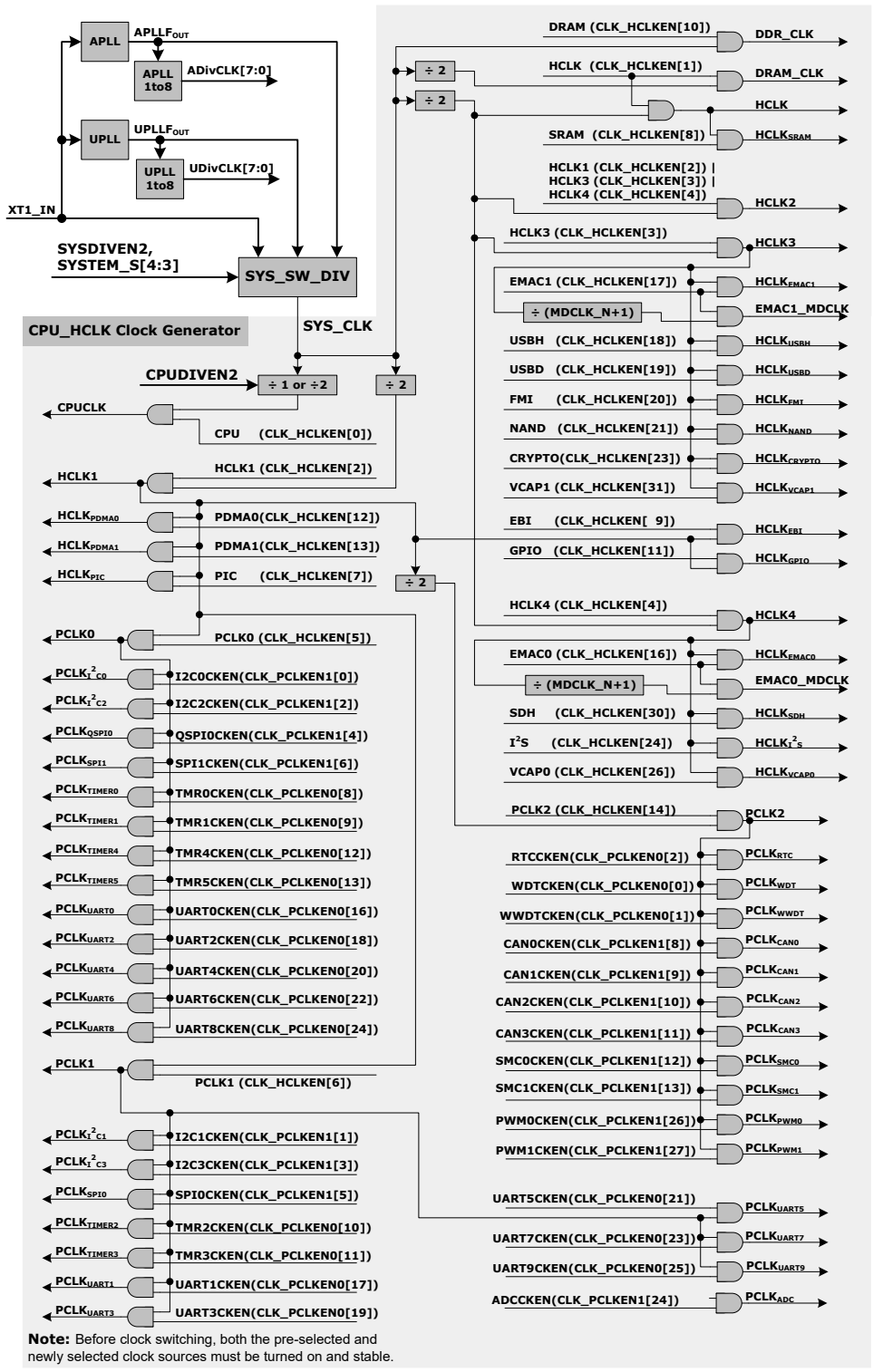
6.3.3.13 Windowed Watchdog Timer Clock Divider



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-13 Windowed Watchdog Timer Clock Divider Block Diagram

6.3.3.14 CPU_HCLK Clock Generator



Note: Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-14 CPU_HCLK Clock Generator Block Diagram

6.3.4 Functional Description

6.3.4.1 Power Management

This chip provides four power management scenarios, including Power-down, Idle and Normal Operating modes, to manage the power consumption. The peripheral clocks can be Enabled / Disabled individually by controlling the corresponding bit in CLKSEL control register. User can turn-off the unused modules' clock for power saving.

6.3.4.2 Normal Operating Mode

In this mode, CPU runs normally and clocks of all functionalities are on. The clock frequency of CPU, DRAM, AHB peripherals and APB peripherals are 300 MHz, 150 MHz, 150 MHz and 75 MHz, respectively.

6.3.4.3 Idle Mode

When CPU is not busy, user can put Arm926EJ-S™ processor into a low-power state by the wait for interrupt instruction:

MCR p15, 0, <Rd>, c7, c0, 4

This instruction switches the Arm926EJ-S™ processor into a low-power state until either an interrupt (IRQ or FIQ) or a debug request occurs.

In this mode, the clocks of all functionalities are on. The clock frequency of DRAM, AHB peripherals and APB peripherals are 150 MHz, 150 MHz and 75 MHz.

6.3.4.4 Power-down Mode

To reduce power consumption further, user could put the chip into Power-down mode by clearing XTAL_EN (CLK_PMCON[0]) to 0 before waiting for interrupt instruction:

MCR p15, 0, <Rd>, c7, c0, 4

In this mode, all clocks (clocks for all functionalities, CPU and the HXT (Ext. Crystall Osc. 12 MHz) stop, except LXT (Ext. Crystal Osc. 32.768 kHz), with SRAM retention.

The mechanisms shown below could wake chip up from Power-down mode:

- EINT0, EINT1, EINT2 or EINT3 (External Interrupt) pin toggled.
- GPIO pin toggled.
- Timer 0/1/2/3/4/5 timeout or capture interrupt is active.
- WDT time-out interrupt is active.
- RTC alarm or relative alarm interrupt is active.
- UART 0/1/2/3/4/5/6/7/8/9
  - UARTx_nCTS pin toggleed (x is 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9).
  - UARTx_RXD pin goes low level (x is 0, 1, 2, 3, 4, 5, 6, 7, 8 or 9).
  - Received data FIFO reached threshold.
  - Received data FIFO threshold time-out.
  - RS-485 address match (AAD Mode).
- I^2C slave mode address match.
- EMAC 0/1 received a Magic Packet.
- HSUSBD detected a VBUS change event or USB bus RESET/RESUME event.
- USB 1.1 host controller detected a connect/dis-connect/remote-wakeup event.
- CANx_RXD pin goes low level (x is 0, 1, 2 or 3).

- SDH detected card pulg/un-plug event or SDIO card interrupt.

6.3.5 Registers Map

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
CLK Base Address: **CLK_BA = 0xB000_0200**				
CLK_PMCON	CLK_BA+0x000	R/W	Power Management Control Register	0xFFFF_FF03
CLK_HCLKEN	CLK_BA+0x010	R/W	AHB Devices Clock Enable Control Register	0x0000_4527
CLK_PCLKEN0	CLK_BA+0x018	R/W	APB Devices Clock Enable Control Register 0	0x0000_000X
CLK_PCLKEN1	CLK_BA+0x01C	R/W	APB Devices Clock Enable Control Register 1	0x0000_0000
CLK_DIVCTL0	CLK_BA+0x020	R/W	Clock Divider Control Register 0	0x0000_00XX
CLK_DIVCTL1	CLK_BA+0x024	R/W	Clock Divider Control Register 1	0x0000_0000
CLK_DIVCTL2	CLK_BA+0x028	R/W	Clock Divider Control Register 2	0x0000_1500
CLK_DIVCTL3	CLK_BA+0x02C	R/W	Clock Divider Control Register 3	0x0000_0000
CLK_DIVCTL4	CLK_BA+0x030	R/W	Clock Divider Control Register 4	0x0000_0000
CLK_DIVCTL5	CLK_BA+0x034	R/W	Clock Divider Control Register 5	0x0000_0000
CLK_DIVCTL6	CLK_BA+0x038	R/W	Clock Divider Control Register 6	0x0000_0000
CLK_DIVCTL7	CLK_BA+0x03C	R/W	Clock Divider Control Register 7	0x0000_0000
CLK_DIVCTL8	CLK_BA+0x040	R/W	Clock Divider Control Register 8	0x0000_0500
CLK_DIVCTL9	CLK_BA+0x044	R/W	Clock Divider Control Register 9	0x0000_0000
CLK_APLLCON	CLK_BA+0x060	R/W	APLL Control Register	0x1000_0018
CLK_UPLLCON	CLK_BA+0x064	R/W	UPLL Control Register	0xX000_0018
CLK_PLLSTBCNTR	CLK_BA+0x080	R/W	PLL Stable Counter and Test Clock Control Register	0x0000_1800

6.3.6 Register Description

Power Management Control Register (CLK_PMCON)

The chip clock source is from an external crystal. The crystal oscillator can be control on/off by the register XTAL_EN. When turn off the crystal, the chip into power down state. To avoid outputting an unstable clock to system, clock controller implements a pre-scalar counter. After the clock counter count pre-scalar x 256 crystal cycle, the clock controller starts to output the clock to system.

Register	Offset	R/W	Description	Reset Value
CLK_PMCON	CLK_BA+0x000	R/W	Power Management Control Register	0xFFFF_FF03

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
PRESCALE							
15	14	13	12	11	10	9	8
PRESCALE							
7	6	5	4	3	2	1	0
Reserved		SEN1_OFF_ST	SEN0_OFF_ST	Reserved		XIN_CTL	XTAL_EN

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:8]	**PRESCALE**	**Pre-scalar Counter** Assume the crystal is stable after the Pre-Scalar x 256 crystal cycles. Clock controller wouldn't output clock to system before the counter reaching (pre-scalar x 256).
[7:6]	**Reserved**	Reserved.
[5]	**SEN1_OFF_ST**	**Sensor 1 Clock Level on Clock Off State** 0 = Sensor 1 clock keep on low level. 1 = Sensor 1 clock keep on high level.
[4]	**SEN0_OFF_ST**	**Sensor Clock Level on Clock Off State** 0 = Sensor 0 clock keep on low level. 1 = Sensor 0 clock keep on high level.
[3:2]	**Reserved**	Reserved.
[1]	**XIN_CTL**	**Pre-scalar Counter Enable Bit** Crystal pre-divide control for Wake-up from power down mode The chip will delay 256 x pre-scalar cycles after the reset signal to wait the Crystal to stable 0 = The pre-scalar counter Disabled (assume the crystal is stable). 1 = The pre-scalar counter Enabled.
[0]	**XTAL_EN**	**Crystal (Power-down) Control** 0 = Crystal off (Power-down mode). 1 = Crystal on (Normal operating mode).

AHB Devices Clock Enable Control Register (CLK_HCLKEN)

Register	Offset	R/W	Description	Reset Value
CLK_HCLKEN	CLK_BA+0x010	R/W	AHB Devices Clock Enable Control Register	0x0000_4527

31	30	29	28	27	26	25	24
VCAP1	SD1	Reserved	Reserved	SENSOR	VCAP0	Reserved	I2S
23	22	21	20	19	18	17	16
CRYPTO	SD0	NAND	FMI	USBD	USBH	EMAC1	EMAC0
15	14	13	12	11	10	9	8
CKO	PCLK2	PDMA1	PDMA0	GPIO	SDIC	EBI	SRAM
7	6	5	4	3	2	1	0
TIC	PCLK1	PCLK0	HCLK4	HCLK3	HCLK1	HCLK	CPU

Bits	Description	
[31]	**VCAP1**	**CMOS Sensor Interface Controller 1 Clock Enable Bit** 0 = CMOS sensor interface controller 1 clock Disabled. 1 = CMOS sensor interface controller 1 clock Enabled.
[30]	**SD1**	**SD Card Controller 1 Clock Enable Bit** 0 = SD card controller 1 clock Disabled. 1 = SD card controller 1 clock Enabled.
[29:28]	**Reserved**	Reserved.
[27]	**SENSOR**	**CMOS Sensor Reference Clock Output Enable Bit** 0 = CMOS sensor reference clock output Disabled. 1 = CMOS sensor reference clock output Enabled. **Note1:** The reference clock output for CMOS sensor interface 0 only Enabled when both VCAP0 and SENSOR Enabled. **Note2:** The reference clock output for CMOS sensor interface 1 only Enabled when both VCAP1 and SENSOR Enabled.
[26]	**VCAP0**	**CMOS Sensor Interface Controller 0 Clock Enable Bit** 0 = CMOS sensor interface controller 0 clock Disabled. 1 = CMOS sensor interface controller 0 clock Enabled.
[25]	**Reserved**	Reserved.
[24]	**I2S**	**I^2S Controller Clock Enable Bit** 0 = I^2S controller clock Disabled. 1 = I^2S controller clock Enabled.
[23]	**CRYPTO**	**Crypto Engine Clock Enable Bit** 0 = Crypto engine clock Disabled. 1 = Crypto engine clock Enabled.
[22]	**SD0**	**SD Card Controller 0 Clock Enable Bit** 0 = SD card controller 0 clock Disabled. 1 = SD card controller 0 clock Enabled.
[21]	**NAND**	**NAND Engine Clock Enable Bit** 0 = NAND controller clock Disabled. 1 = NAND controller clock Enabled.
[20]	**FMI**	**FMI Controller Clock Enable Bit** 0 = FMI controller clock Disabled. 1 = FMI controller clock Enabled.
[19]	**USBD**	**USB Device Controller Clock Enable Bit** 0 = USB device controller clock Disabled. 1 = USB device controller clock Enabled.
[18]	**USBH**	**USB Host Controller Clock Enable Bit** 0 = USB host controller clock Disabled. 1 = USB host controller clock Enabled.
[17]	**EMAC1**	**Ethernet MAC Controller 1 Clock Enable Bit** 0 = Ethernet MAC controller 1 clock Disabled. 1 = Ethernet MAC controller 1 clock Enabled.

[16]	**EMAC0**	**Ethernet MAC Controller 0 Clock Enable Bit** 0 = Ethernet MAC controller 0 clock Disabled. 1 = Ethernet MAC controller 0 clock Enabled.
[15]	**CKO**	**Reference Clock Output Enable Bit** 0 = Reference clock output Disabled. 1 = Reference clock output Enabled.
[14]	**PCLK2**	**Internal APB-2 Bus Clock Enable Bit** 0 = Internal APB-2 bus clock Disabled. 1 = Internal APB-2 bus clock Enabled.
[13]	**PDMA1**	**PDMA 1 Clock Enable Bit** 0 = PDMA 1 clock Disabled. 1 = PDMA 1 clock Enabled.
[12]	**PDMA0**	**PDMA 0 Clock Enable Bit** 0 = PDMA 0 clock Disabled. 1 = PDMA 0 clock Enabled.
[11]	**GPIO**	**GPIO Clock Enable Bit** 0 = GPIO clock Disabled. 1 = GPIO clock Enabled.
[10]	**SDIC**	**SDIC Clock Enable Bit** 0 = DDR clock Disabled. 1 = DDR clock Enabled.
[9]	**EBI**	**EBI Controller Clock Enable Bit** 0 = EBI controller clock Disabled. 1 = EBI controller clock Enabled.
[8]	**SRAM**	**SRAM Controller Clock Enable Bit** 0 = SRAM controller clock Disabled. 1 = SRAM controller clock Enabled.
[7]	**TIC**	**TIC Clock Enable Bit** 0 = TIC clock Disabled. 1 = TIC clock Enabled.
[6]	**PCLK1**	**Internal APB-1 Bus Clock Enable Bit** 0 = Internal APB-1 bus clock Disabled. 1 = Internal APB-1 bus clock Enabled.
[5]	**PCLK0**	**Internal APB-0 Bus Clock Enable Bit** 0 = Internal APB-1 bus clock Disabled. 1 = Internal APB-1 bus clock Enabled.
[4]	**HCLK4**	**Internal AHB-4 Bus Clock Enable Bit** 0 = Internal AHB-4 bus clock Disabled. 1 = Internal AHB-4 bus clock Enabled.
[3]	**HCLK3**	**Internal AHB-3 Bus Clock Enable Bit** 0 = Internal AHB-3 bus clock Disabled. 1 = Internal AHB-3 bus clock Enabled.

[2]	**HCLK1**	**Internal AHB-1 Bus Clock Enable Bit** 0 = Internal AHB-1 bus clock Disabled. 1 = Internal AHB-1 bus clock Enabled.
[1]	**HCLK**	**Internal AHB Bus Clock Enable Bit** 0 = Internal AHB bus clock Disabled. 1 = Internal AHB bus clock Enabled.
[0]	**CPU**	**Arm926EJ-S™ CPU Clock Enable Bit** 0 = Arm926EJ-S™ CPU clock Disabled. 1 = Arm926EJ-S™ CPU clock Enabled.

APB Devices Clock Enable Control Register 0 (CLK_PCLKEN0)

Register	Offset	R/W	Description	Reset Value
CLK_PCLKEN0	CLK_BA+0x018	R/W	APB Devices Clock Enable Control Register 0	0x0000_000X

31	30	29	28	27	26	25	24
Reserved						UART9CKEN	UART8CKEN
23	22	21	20	19	18	17	16
UART7CKEN	UART6CKEN	UART5CKEN	UART4CKEN	UART3CKEN	UART2CKEN	UART1CKEN	UART0CKEN
15	14	13	12	11	10	9	8
Reserved		TMR5CKEN	TMR4CKEN	TMR3CKEN	TMR2CKEN	TMR1CKEN	TMR0CKEN
7	6	5	4	3	2	1	0
Reserved				Reserved	RTCCKEN	WWDTCKEN	WDTCKEN

Bits	Description	
[31:26]	**Reserved**	Reserved.
[25]	**UART9CKEN**	**UART 9 Clock Enable Bit** 0 = UART 9 clock Disabled. 1 = UART 9 clock Enabled.
[24]	**UART8CKEN**	**UART 8 Clock Enable Bit** 0 = UART 8 clock Disabled. 1 = UART 8 clock Enabled.
[23]	**UART7CKEN**	**UART 7 Clock Enable Bit** 0 = UART 7 clock Disabled. 1 = UART 7 clock Enabled.
[22]	**UART6CKEN**	**UART 6 Clock Enable Bit** 0 = UART 6 clock Disabled. 1 = UART 6 clock Enabled.
[21]	**UART5CKEN**	**UART 5 Clock Enable Bit** 0 = UART 5 clock Disabled. 1 = UART 5 clock Enabled.
[20]	**UART4CKEN**	**UART 4 Clock Enable Bit** 0 = UART 4 clock Disabled. 1 = UART 4 clock Enabled.
[19]	**UART3CKEN**	**UART 3 Clock Enable Bit** 0 = UART 3 clock Disabled. 1 = UART 3 clock Enabled.
[18]	**UART2CKEN**	**UART 2 Clock Enable Bit** 0 = UART 2 clock Disabled. 1 = UART 2 clock Enabled.
[17]	**UART1CKEN**	**UART 1 Clock Enable Bit** 0 = UART 1 clock Disabled. 1 = UART 1 clock Enabled.
[16]	**UART0CKEN**	**UART 0 Clock Enable Bit** 0 = UART 0 clock Disabled. 1 = UART 0 clock Enabled.
[15:14]	**Reserved**	Reserved.
[13]	**TMR5CKEN**	**Timer 5 Clock Enable Bit** 0 = Timer 5 clock Disabled. 1 = Timer 5 clock Enabled.
[12]	**TMR4CKEN**	**Timer 4 Clock Enable Bit** 0 = Timer 4 clock Disabled. 1 = Timer 4 clock Enabled.
[11]	**TMR3CKEN**	**Timer 3 Clock Enable Bit** 0 = Timer 3 clock Disabled. 1 = Timer 3 clock Enabled.

[10]	**TMR2CKEN**	**Timer 2 Clock Enable Bit** 0 = Timer 2 clock Disabled. 1 = Timer 2 clock Enabled.
[9]	**TMR1CKEN**	**Timer 1 Clock Enable Bit** 0 = Timer 1 clock Disabled. 1 = Timer 1 clock Enabled.
[8]	**TMR0CKEN**	**Timer 0 Clock Enable Bit** 0 = Timer 0 clock Disabled. 1 = Timer 0 clock Enabled.
[7:3]	**Reserved**	Reserved.
[2]	**RTCCKEN**	**RTC Clock Enable Bit** 0 = RTC clock Disabled. 1 =RTC clock Enabled.
[1]	**WWDTCKEN**	**Windowed Watch-dog Clock Enable Bit** 0 = Windowed Watch-dog clock Disabled. 1 = Windowed Watch-dog clock Enabled.
[0]	**WDTCKEN**	**Watch-dog Clock Enable Bit** 0 = Watch-dog clock Disabled. 1 = Watch-dog clock Enabled. **Note:** If WDT default Enabled (WDTON(SYS_PWRON[3])=1), this bit is read-only and read back value is always 1.

APB Devices Clock Enable Control Register 1 (CLK_PCLKEN1)

Register	Offset	R/W	Description	Reset Value
CLK_PCLKEN1	CLK_BA+0x01C	R/W	APB Devices Clock Enable Control Register 1	0x0000_0000

31	30	29	28	27	26	25	24
Reserved				PWM1CKEN	PWM0CKEN	Reserved	ADCCKEN
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved		SMC1CKEN	SMC0CKEN	CAN3CKEN	CAN2CKEN	CAN1CKEN	CAN0CKEN
7	6	5	4	3	2	1	0
Reserved	SPI1CKEN	SPI0CKEN	QSPI0CKEN	I2C3CKEN	I2C2CKEN	I2C1CKEN	I2C0CKEN

Bits	Description	
[31:26]	**Reserved**	Reserved.
[27]	**PWM1CKEN**	**PWM 1 Clock Enable Bit** 0 = PWM 1 clock Disabled. 1 = PWM 1 clock Enabled.
[26]	**PWM0CKEN**	**PWM 0 Clock Enable Bit** 0 = PWM 0 clock Disabled. 1 = PWM 0 clock Enabled.
[25]	**Reserved**	Reserved.
[24]	**ADCCKEN**	**ADC Controller Clock Enable Bit** 0 = ADC controller clock Disabled. 1 = ADC controller clock Enabled.
[23:14]	**Reserved**	Reserved.
[13]	**SMC1CKEN**	**Smart Card Interface 1 Clock Enable Bit** 0 = Smart Card interface 1 clock Disabled. 1 = Smart Card interface 1 clock Enabled.
[12]	**SMC0CKEN**	**Smart Card Interface 0 Clock Enable Bit** 0 = Smart Card interface 0 clock Disabled. 1 = Smart Card interface 0 clock Enabled.
[11]	**CAN3CKEN**	**CAN 3 Clock Enable Bit** 0 = CAN 3 clock Disabled. 1 = CAN 3 clock Enabled.
[10]	**CAN2CKEN**	**CAN 2 Clock Enable Bit** 0 = CAN 2 clock Disabled. 1 = CAN 2 clock Enabled.
[9]	**CAN1CKEN**	**CAN 1 Clock Enable Bit** 0 = CAN 1 clock Disabled. 1 = CAN 1 clock Enabled.
[8]	**CAN0CKEN**	**CAN 0 Clock Enable Bit** 0 = CAN 0 clock Disabled. 1 = CAN 0 clock Enabled.
[7]	**Reserved**	Reserved.
[6]	**SPI1CKEN**	**SPI 1 Clock Enable Bit** 0 = SPI 1 clock Disabled. 1 = SPI 1 clock Enabled.
[5]	**SPI0CKEN**	**SPI 0 Clock Enable Bit** 0 = SPI 0 clock Disabled. 1 = SPI 0 clock Enabled.
[4]	**QSPI0CKEN**	**QSPI 0 Clock Enable Bit** 0 = QSPI 0 clock Disabled. 1 = QSPI 0 clock Enabled.

[3]	**I2C3CKEN**	**I²C 3 Clock Enable Bit** 0 = I²C 3 clock Disabled. 1 = I²C 3 clock Enabled.
[2]	**I2C2CKEN**	**I²C 2 Clock Enable Bit** 0 = I²C 2 clock Disabled. 1 = I²C 2 clock Enabled.
[1]	**I2C1CKEN**	**I²C 1 Clock Enable Bit** 0 = I²C 1 clock Disabled. 1 = I²C 1 clock Enabled.
[0]	**I2C0CKEN**	**I²C 0 Clock Enable Bit** 0 = I²C 0 clock Disabled. 1 = I²C 0 clock Enabled.

Clock Divider Control Register 0 (CLK_DIVCTL0)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL0	CLK_BA+0x020	R/W	Clock Divider Control Register 0	0x0000_00XX

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							CPUDIV2EN
15	14	13	12	11	10	9	8
Reserved							SYSDIV2EN
7	6	5	4	3	2	1	0
Reserved			SYSTEM_S		Reserved		

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**CPUDIV2EN**	**CPU Clock Divided by 2 Enable Bit** This field defines if CPUCLK for Arm926EJ-S™ CPU is SYS_CLK devided by 2 or not. 0 = The frequency of CPUCLK is equal to SYS_CLK. 1 = The frequency of CPUCLK is SYS_CLK devided by 2.
[15:9]	**Reserved**	Reserved.
[8]	**SYSDIV2EN**	**System Clock Divided by 2 Enable Bit** This field defines if SYS_CLK is SYSTEM_SrcCLK devided by 2 or not. 0 = The frequency of SYS_CLK is equal to SYSTEM_SrcCLK. 1 = The frequency of SYS_CLK is SYSTEM_SrcCLK devided by 2.
[7:5]	**Reserved**	Reserved.
[4:3]	**SYSTEM_S**	**System Clock Source Selection** This field selects which clock is used to be the source of system clock SYS_CLK. 00 = SYSTEM_SrcCLK is from XIN. 01 = Reserved. 10 = SYSTEM_SrcCLK is from APLLFout. 11 = SYSTEM_SrcCLK is from UPLLFout.
[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 1 (CLK_DIVCTL1)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL1	CLK_BA+0x024	R/W	Clock Divider Control Register 1	0x0000_0000

31	30	29	28	27	26	25	24
I2S_N							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved			**I2S_S**		**Reserved**		
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:24]	**I2S_N**	**I²S Controller Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for I²S controller. The actual clock divide number is (I2S_N + 1). So, ECLKi2s = I2S_SrcCLK / (I2S_N + 1).
[23:21]	**Reserved**	Reserved.
[20:19]	**I2S_S**	**I²S Controller Clock Source Selection** This field selects which clock is used to be the source of engine clock for I²S controller. 00 = I2S_SrcCLK is from XIN. 01 = Reserved. 10 = I2S_SrcCLK is from ACLKOut. 11 = I2S_SrcCLK is from UCLKOut.
[18:0]	**Reserved**	Reserved.

Clock Divider Control Register 2 (CLK_DIVCTL2)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL2	CLK_BA+0x028	R/W	Clock Divider Control Register 2	0x0000_1500

31	30	29	28	27	26	25	24
Reserved				SENSOR1_N			
23	22	21	20	19	18	17	16
Reserved			SENSOR1_S		SENSOR1_SDIV		
15	14	13	12	11	10	9	8
Reserved		SPI1_S		SPI0_S		QSPI0_S	
7	6	5	4	3	2	1	0
Reserved			USB_S		Reserved		

Bits	Description	
[31:28]	**Reserved**	Reserved.
[27:24]	**SENSOR1_N**	**Sensor 1 Clock Divider** This field defines the clock divide number for clock divider to generate the sensor 1 clock. The actual clock divide number is (SENSOR1_N + 1). So, SEN1_CLK = SEN1_SrcCLK / (SENSOR1_N + 1).
[23:21]	**Reserved**	Reserved.
[20:19]	**SENSOR1_S**	**Sensor 1 Clock Source Selection** This field selects which clock is used to be the source of sensor 1 clock. 00 = SEN1_SrcCLK is from XIN. 01 = Reserved. 10 = SEN1_SrcCLK is from ACLKOut. 11 = SEN1_SrcCLK is from UCLKOut.
[18:16]	**SENSOR1_SDIV**	**Sensor 1 Source Clock Divider** This field defines the source clock divide number for clock divider of APLL and UPLL output. This field only takes effect while the SENSOR1_S (CLK_DIVCTL3[20:19]) is 2'b10 (APLL) or 2'b11 (UPLL). If SENSOR1_S (CLK_DIVCTL3[20:19]) is 2'b10, ACLKOut = APLLFout ÷ (SENSOR1_SDIV + 1). If SENSOR1_S (CLK_DIVCTL3[20:19]) is 2'b11, UCLKOut = UPLLFout ÷ (SENSOR1_SDIV + 1).
[15:14]	**Reserved**	Reserved.
[13:12]	**SPI1_S**	**SPI 1 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for SPI 1. 00 = SPI1_SrcCLK is from XIN. 01 = SPI1_SrcCLK is from PCLK0. 10 = SPI1_SrcCLK is from ACLKOut. 11 = SPI1_SrcCLK is from UCLKOut.
[11:10]	**SPI0_S**	**SPI 0 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for SPI 0. 00 = SPI0_SrcCLK is from XIN. 01 = SPI0_SrcCLK is from PCLK1. 10 = SPI0_SrcCLK is from ACLKOut. 11 = SPI0_SrcCLK is from UCLKOut.
[9:8]	**QSPI0_S**	**QSPI 0 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for QSPI 0. 00 = QSPI0_SrcCLK is from XIN. 01 = QSPI0_SrcCLK is from PCLK0. 10 = QSPI0_SrcCLK is from ACLKOut. 11 = QSPI0_SrcCLK is from UCLKOut.
[7:5]	**Reserved**	Reserved.

[4:3]	**USB_S**	**USB 1.1 Engine Clock Source Selection** This field selects which clock is used to be the source of 48 MHz clock for USB 1.1 host controller. 00 = Reserved. 01 = Reserved. 10 = USB11_SrcCLK is from 480 MHz outputted by USB PHY 0. 11 = USB11_SrcCLK is from 480 MHz outputted by USB PHY 1.
[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 3 (CLK_DIVCTL3)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL3	CLK_BA+0x02C	R/W	Clock Divider Control Register 3	0x0000_0000

31	30	29	28	27	26	25	24
Reserved				SENSOR0_N			
23	22	21	20	19	18	17	16
Reserved			SENSOR0_S		SENSOR0_SDIV		
15	14	13	12	11	10	9	8
SD0_N							
7	6	5	4	3	2	1	0
Reserved			SD0_S		Reserved		

Bits	Description	
[31:28]	**Reserved**	Reserved.
[27:24]	**SENSOR0_N**	**Sensor 0 Clock Divider** This field defines the clock divide number for clock divider to generate the sensor 0 clock. The actual clock divide number is (SENSOR0_N + 1). So, SEN0_CLK = SEN0_SrcCLK / (SENSOR0_N + 1).
[33:21]	**Reserved**	Reserved.
[20:19]	**SENSOR0_S**	**Sensor 0 Clock Source Selection** This field selects which clock is used to be the source of sensor 0 clock. 00 = SEN0_SrcCLK is from XIN. 01 = Reserved. 10 = SEN0_SrcCLK is from ACLKOut. 11 = SEN0_SrcCLK is from UCLKOut.
[18:16]	**SENSOR0_SDIV**	**Sensor 0 Source Clock Divider** This field defines the source clock divide number for clock divider of APLL and UPLL output. This field only takes effect while the SENSOR0_S (CLK_DIVCTL3[20:19]) is 2'b10 (APLL) or 2'b11 (UPLL). If SENSOR0_S (CLK_DIVCTL3[20:19]) is 2'b10, ACLKOut = APLLFout ÷ (SENSOR0_SDIV + 1). If SENSOR0_S (CLK_DIVCTL3[20:19]) is 2'b11, UCLKOut = UPLLFout ÷ (SENSOR0_SDIV + 1).
[15:8]	**SD0_N**	**SD Card Controller 0 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for SD card controller 0. The actual clock divide number is (SD0_N + 1). So, SD0_CLK = SD0_SrcCLK / (SD0_N + 1).
[7:5]	**Reserved**	Reserved.
[4:3]	**SD0_S**	**SD Card Controller 0 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for SD card controller 0. 00: SD0_SrcCLK = XIN. 01: SD0_SrcCLK = Reserved. 10: SD0_SrcCLK = ACLKOut. 11: SD0_SrcCLK = UCLKOut.
[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 4 (CLK_DIVCTL4)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL4	CLK_BA+0x030	R/W	Clock Divider Control Register 4	0x0000_0000

31	30	29	28	27	26	25	24
UART3_N			UART3_S		Reserved		
23	22	21	20	19	18	17	16
UART2_N			UART2_S		Reserved		
15	14	13	12	11	10	9	8
UART1_N			UART1_S		Reserved		
7	6	5	4	3	2	1	0
UART0_N			UART0_S		Reserved		

Bits	Description	
[31:29]	**UART3_N**	**UART3 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART3. The actual clock divide number is (UART3_N + 1). So, ECLKuart3 = UART3_SrcCLK / (UART3_N + 1).
[28:27]	**UART3_S**	**UART3 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART3 controller. 00 = UART3_SrcCLK is from XIN. 01 = UART3_SrcCLK is from LXT. 10 = UART3_SrcCLK is from ACLKOut. 11 = UART3_SrcCLK is from UCLKOut.
[26:24]	**Reserved**	Reserved.
[23:21]	**UART2_N**	**UART2 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART2. The actual clock divide number is (UART2_N + 1). So, ECLKuart2 = UART2_SrcCLK / (UART2_N + 1).
[20:19]	**UART2_S**	**UART2 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART2 controller. 00 = UART2_SrcCLK is from XIN. 01 = UART2_SrcCLK is from LXT. 10 = UART2_SrcCLK is from ACLKOut. 11 = UART2_SrcCLK is from UCLKOut.
[18:16]	**Reserved**	Reserved.
[15:13]	**UART1_N**	**UART1 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART1. The actual clock divide number is (UART1_N + 1). So, ECLKuart1 = UART1_SrcCLK / (UART1_N + 1).
[12:11]	**UART1_S**	**UART1 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART1 controller. 00 = UART1_SrcCLK is from XIN. 01 = UART1_SrcCLK is from LXT. 10 = UART1_SrcCLK is from ACLKOut. 11 = UART1_SrcCLK is from UCLKOut.
[10:8]	**Reserved**	Rserved
[7:5]	**UART0_N**	**UART0 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART0. The actual clock divide number is (UART0_N + 1). So, ECLKuart0 = UART0_SrcCLK / (UART0_N + 1).
[4:3]	**UART0_S**	**UART0 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART0 controller. 00 = UART0_SrcCLK is from XIN. 01 = UART0_SrcCLK is from LXT. 10 = UART0_SrcCLK is from ACLKOut. 11 = UART0_SrcCLK is from UCLKOut.

[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 5 (CLK_DIVCTL5)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL5	CLK_BA+0x034	R/W	Clock Divider Control Register 5	0x0000_0000

31	30	29	28	27	26	25	24
UART7_N			UART7_S		Reserved		
23	22	21	20	19	18	17	16
UART6_N			UART6_S		Reserved		
15	14	13	12	11	10	9	8
UART5_N			UART5_S		Reserved		
7	6	5	4	3	2	1	0
UART4_N			UART4_S		Reserved		

Bits	Description	
[31:29]	**UART7_N**	**UART7 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART7. The actual clock divide number is (UART7_N + 1). So, ECLKuart7 = UART7_SrcCLK / (UART7_N + 1).
[28:27]	**UART7_S**	**UART7 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART7 controller. 00 = UART7_SrcCLK is from XIN. 01 = UART7_SrcCLK is from LXT. 10 = UART7_SrcCLK is from ACLKOut. 11 = UART7_SrcCLK is from UCLKOut.
[26:24]	**Reserved**	Reserved.
[23:21]	**UART6_N**	**UART6 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART6. The actual clock divide number is (UART6_N + 1). So, ECLKuart6 = UART6_SrcCLK / (UART6_N + 1).
[20:19]	**UART6_S**	**UART6 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART6 controller. 00 = UART6_SrcCLK is from XIN. 01 = UART6_SrcCLK is from LXT. 10 = UART6_SrcCLK is from ACLKOut. 11 = UART6_SrcCLK is from UCLKOut.
[18:16]	**Reserved**	Reserved.
[15:13]	**UART5_N**	**UART5 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART5. The actual clock divide number is (UART5_N + 1). So, ECLKuart5 = UART5_SrcCLK / (UART5_N + 1).
[12:11]	**UART5_S**	**UART5 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART5 controller. 00 = UART5_SrcCLK is from XIN. 01 = UART5_SrcCLK is from LXT. 10 = UART5_SrcCLK is from ACLKOut. 11 = UART5_SrcCLK is from UCLKOut.
[10:8]	**Reserved**	Reserved.
[7:5]	**UART4_N**	**UART4 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART4. The actual clock divide number is (UART4_N + 1). So, ECLKuart4 = UART4_SrcCLK / (UART4_N + 1).

[4:3]	**UART4_S**	**UART4 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART4 controller. 00 = UART4_SrcCLK is from XIN. 01 = UART4_SrcCLK is from LXT. 10 = UART4_SrcCLK is from ACLKOut. 11 = UART4_SrcCLK is from UCLKOut.
[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 6 (CLK_DIVCTL6)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL6	CLK_BA+0x038	R/W	Clock Divider Control Register 6	0x0000_0000

31	30	29	28	27	26	25	24
SMC1_N				SMC0_N			
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
UART9_N			UART9_S		Reserved		
7	6	5	4	3	2	1	0
UART8_N			UART8_S		Reserved		

Bits	Description	
[30:28]	**SMC1_N**	**Smart Card 1 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for Smart card controller. The actual clock divide number is (SMC1_N + 1). So, ECLKsmc1 = XIN12M / (SMC1_N + 1).
[27:24]	**SMC0_N**	**Smart Card 0 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for Smart card controller. The actual clock divide number is (SMC0_N + 1). So, ECLKsmc0 = XIN12M / (SMC0_N + 1).
[23:16]	**Reserved**	Reserved.
[15:13]	**UART9_N**	**UART9 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART9. The actual clock divide number is (UART9_N + 1). So, ECLKuart9 = UART9_SrcCLK / (UART9_N + 1).
[12:11]	**UART9_S**	**UART9 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART9 controller. 00 = UART9_SrcCLK is from XIN. 01 = UART9_SrcCLK is from LXT. 10 = UART9_SrcCLK is from ACLKOut. 11 = UART9_SrcCLK is from UCLKOut.
[10:8]	**Reserved**	Reserved.
[7:5]	**UART8_N**	**UART8 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for UART8. The actual clock divide number is (UART8_N + 1). So, ECLKuart8 = UART8_SrcCLK / (UART8_N + 1).
[4:3]	**UART8_S**	**UART8 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for UART8 controller. 00 = UART8_SrcCLK is from XIN. 01 = UART8_SrcCLK is from LXT. 10 = UART8_SrcCLK is from ACLKOut. 11 = UART8_SrcCLK is from UCLKOut.
[2:0]	**Reserved**	Reserved.

Clock Divider Control Register 7 (CLK_DIVCTL7)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL7	CLK_BA+0x03C	R/W	Clock Divider Control Register 7	0x0000_0000

31	30	29	28	27	26	25	24
ADC_N							
23	22	21	20	19	18	17	16
Reserved			ADC_S		Reserved		
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved							

Bits	Description	
[31:24]	**ADC_N**	**ADC Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for ADC. The actual clock divide number is (ADC_N + 1). So, ADC_CLK = ADC_SrcCLK / (ADC_N + 1).
[23:21]	**Reserved**	Reserved.
[20:19]	**ADC_S**	**ADC Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for ADC controller. 00 = ADC_SrcCLK is from XIN. 01 = Reserved. 10 = ADC_SrcCLK is from APLLFOut. 11 = ADC_SrcCLK is from UPLLFOut.
[18:0]	**Reserved**	Reserved.

Clock Divider Control Register 8 (CLK_DIVCTL8)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL8	CLK_BA+0x040	R/W	Clock Divider Control Register 8	0x0000_0500

31	30	29	28	27	26	25	24
Reserved				TMR5SEL		TMR4SEL	
23	22	21	20	19	18	17	16
TMR3SEL		TMR2SEL		TMR1SEL		TMR0SEL	
15	14	13	12	11	10	9	8
Reserved				WWDTSEL		WDTSEL	
7	6	5	4	3	2	1	0
MDCLKDIV							

Bits	Description	
[27:26]	**TMR5SEL**	**Timer 5 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 5 controller. 00: TIMER5_SrcCLK = XIN. 01: TIMER5_SrcCLK = PCLK0. 10: TIMER5_SrcCLK = PCLK0/4096. 11: TIMER5_SrcCLK = 32.768 kHz.
[25:24]	**TMR4SEL**	**Timer 4 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 4 controller. 00: TIMER4_SrcCLK = XIN. 01: TIMER4_SrcCLK = PCLK0. 10: TIMER4_SrcCLK = PCLK0/4096. 11: TIMER4_SrcCLK = 32.768 kHz.
[23:22]	**TMR3SEL**	**Timer 3 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 3 controller. 00: TIMER3_SrcCLK = XIN. 01: TIMER3_SrcCLK = PCLK1. 10: TIMER3_SrcCLK = PCLK1/4096. 11: TIMER3_SrcCLK = 32.768 kHz.
[21:20]	**TMR2SEL**	**Timer 2 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 2 controller. 00: TIMER2_SrcCLK = XIN. 01: TIMER2_SrcCLK = PCLK1. 10: TIMER2_SrcCLK = PCLK1/4096. 11: TIMER2_SrcCLK = 32.768 kHz.
[19:18]	**TMR1SEL**	**Timer 1 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 1 controller. 00: TIMER1_SrcCLK = XIN. 01: TIMER1_SrcCLK = PCLK0. 10: TIMER1_SrcCLK = PCLK0/4096. 11: TIMER1_SrcCLK = 32.768 kHz.
[17:16]	**TMR0SEL**	**Timer 0 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for Timer 0 controller. 00: TIMER0_SrcCLK = XIN. 01: TIMER0_SrcCLK = PCLK0. 10: TIMER0_SrcCLK = PCLK0/4096. 11: TIMER0_SrcCLK = 32.768 kHz.
[11:10]	**WWDTSEL**	**WWDT Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for WWDT controller. 00: WWDT_SrcCLK = XIN. 01: WWDT_SrcCLK = XIN/512. 10: WWDT_SrcCLK = PCLK2/4096. 11: WWDT_SrcCLK = 32.768 kHz.

[9:8]	**WDTSEL**	**WDT Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for WDT controller. 00: WDT_SrcCLK = XIN. 01: WDT_SrcCLK = XIN/512. 10: WDT_SrcCLK = PCLK2/4096. 11: WDT_SrcCLK = 32.768 kHz.
[7:0]	**MDCLKDIV**	**MII Management Interface Clock** This field defines the clock divide number for clock divider to generate the clock for MII management interface. The actual clock divide number is (MDCLK_N + 1). So, MDCLK = HCLK / (MDCLK_N + 1).

Clock Divider Control Register 9 (CLK_DIVCTL9)

Register	Offset	R/W	Description	Reset Value
CLK_DIVCTL9	CLK_BA+0x044	R/W	Clock Divider Control Register 9	0x0000_0000

31	30	29	28	27	26	25	24
CKO_N							
23	22	21	20	19	18	17	16
Reserved			CKO_S		Reserved		
15	14	13	12	11	10	9	8
SD1_N							
7	6	5	4	3	2	1	0
Reserved			SD1_S		Reserved		

Bits	Description	
[31:24]	**CKO_N**	**Reference Clock Out Divide** This field defines the clock divide number for clock divider to generate the reference clock output The actual clock divide number is (CKO_N + 1). So, CKO_CLK = CKO_SrcCLK / (CKO_N + 1).
[23:21]	**Reserved**	Reserved.
[20:19]	**CKO_S**	**Reference Clock Out Source Selection** This field selects which clock is used to be the source of reference clock output. 00 = CKO_SrcCLK is from XIN. 01 = CKO_SrcCLK is from LXT. 10 = CKO_SrcCLK is from ACLKOut. 11 = CKO_SrcCLK is from UCLKOut.
[18:16]	**Reserved**	Reserved.
[15:8]	**SD1_N**	**SD Card Controller 1 Engine Clock Divider** This field defines the clock divide number for clock divider to generate the engine clock for SD card controller 1. The actual clock divide number is (SD1_N + 1). So, SD1_CLK = SD1_SrcCLK / (SD1_N + 1).
[7:5]	**Reserved**	Reserved.
[4:3]	**SD1_S**	**SD Card Controller 1 Engine Clock Source Selection** This field selects which clock is used to be the source of engine clock for SD card controller 1. 00 = SD1_SrcCLK is from XIN. 01 = Reserved. 10 = SD1_SrcCLK is from ACLKOut. 11 = SD1_SrcCLK is from UCLKOut.
[2:0]	**Reserved**	Reserved.

APLL Control Register (CLK_APLLCON), UPLL Control Register (CLK_UPLLCON)

Register	Offset	R/W	Description	Reset Value
CLK_APLLCON	CLK_BA+0x060	R/W	APLL Control Register	0x1000_0018
CLK_UPLLCON	CLK_BA+0x064	R/W	UPLL Control Register	0xX000_0018

31	30	29	28	27	26	25	24
PLL_STB	RESETN	BYPASS	PD	FRAC			
23	22	21	20	19	18	17	16
FRAC							
15	14	13	12	11	10	9	8
OUT_DV			IN_DV				
7	6	5	4	3	2	1	0
IN_DV	FB_DV						

Bits	Description	
[31]	PLL_STB	**PLL Stable Flag** 0 = PLL is not stable. 1 = PLL is stable (500us after PLL setting changed).
[30]	RESETN	**Reset Mode Enable Bit** 0 = PLL is in reset mode. 1 = PLL is in normal operation mode (Default).
[29]	BYPASS	**Bypass Mode Enable Bit** 0 = PLL is in normal operation mode (Default). 1 = PLL is in bypass mode.
[28]	PD	**Power Down Mode Enable Bit** 0 = PLL is in normal operation mode. 1 = PLL is in power down mode (Default).
[27:16]	FRAC	**PLL VCO Output Clock Feedback Divider Fraction Part** Set the fraction part (X) of feedback divider factor. Write a non-zero value to this field enables the fraction mode automatically. Please keep this field in 0x0 if don't want to use the PLL fraction mode. The X = FRAC[11:0] / 2^{12}.
[15:13]	OUT_DV	**PLL Output Divider** Set the output divider factor (P) from 1 to 8. The P = OUT_DV[2:0] + 1.
[12:7]	IN_DV	**Reference Input Divider** Set the reference divider factor (M) from 1 to 64. The M = IN_DV[5:0] + 1.

[6:0]	**FB_DV**	**PLL VCO Output Clock Feedback Divider Integer Part** Set the feedback divider factor (N) from 1 to 128. The N = FB_DV[6:0] + 1.

The formula to calculate the PLL output frequency shown below:

$$F_{pllout} = 12\ \text{MHz} \times \frac{N}{M \times P}$$

$$F_{vco} = 12\ \text{MHz} \times \frac{N}{M}$$

$$200\ \text{MHz} < F_{vco} < 500\ MHz$$

$$F_{pfd} = \frac{12\ MHz}{M} = \frac{F_{vco}}{N}$$

N	F_{pfd} Range
1	$11.0 \le F_{pfd} \le 80$
2	$7.0 \le F_{pfd} \le 80$
3	$5.0 \le F_{pfd} \le 80$
4	$4.0 \le F_{pfd} \le 80$
5	$3.5 \le F_{pfd} \le 80$
6	$3.0 \le F_{pfd} \le 80$
7 ~ 8	$2.5 \le F_{pfd} \le 80$
9 ~ 10	$3.5 \le F_{pfd} \le 80$
11 ~ 40	$3.0 \le F_{pfd} \le 80$
41 ~ 128	$2.5 \le F_{pfd} \le 80$

Table 6.3-1 The Mapping of N and F_{pfd} Range

PLL Stable Counter and Test Clock Control Register (CLK_PLLSTBCNTR)

Register	Offset	R/W	Description	Reset Value
CLK_PLLSTBCNTR	CLK_BA+0x080	R/W	PLL Stable Counter and Test Clock Control Register	0x0000_1800

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PLLSTBCNT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PLLSTBCNT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[15:0]	**PLLSTBCNT**	PLL Stable Counter

6.4 Advanced Interrpt Controller

6.4.1 Overview

An interrupt can temporarily change the sequence of program execution to react to some specific events, such as power failure, watchdog timer timeout, transmit/receive requests from Ethernet MAC Controller, and so on. There are two interrupt types the CPU can process. The first type is the Fast Interrupt Request (FIQ) for servicing timing-critical events, and the second type is the Interrupt Request (IRQ) for servicing other general-purpose events. An FIQ interrupt occurs when the signal nFIQ to the CPU is asserted, and a IRQ interrupt occurs when the signal nIRQ to the CPU is asserted.

A FIQ interrupt has higher priority than an IRQ interrupt to be processed by CPU. An IRQ service routine in-process can be interrupted by a new coming FIQ interrupt; however, a FIQ service routine in-process cannot be interrupted by a new coming IRQ interrupt.

The Advanced Interrupt Controller (AIC) can process up to 64 interrupt sources. Currently, 62 interrupt sources are supported in the system. AIC assigns every interrupt source a unique source number. For example, the watchdog timer interrupt is assigned to source number 1, and window WDT interrupt is assigned to source number 2.

Every interrupt source can be configured to have one of eight priority levels, numbered from 0 to 7. Interrupt sources with priority level 0 have the highest priority, and interrupt sources with priority level 7 have the lowest priority. For those interrupt sources with the same priority levels, an interrupt source with a lower source number will have higher priority.

An interrupt request generated by an interrupt source with priority level 0 will become a FIQ interrupt to the CPU. An interrupt request generated by an interrupt source with priority levels from 1 to 7 will become a IRQ interrupt to the CPU.

Each interrupt source can be configured as disabled or enabled. An interrupt request from a disabled interrupt source is always ignored by AIC, no matter what its source number and priority level are.

AIC supports four trigger types for every interrupt source: high-level trigger, low-level trigger, rising-edge trigger, and falling-edge trigger.

6.4.2 Features

- AMBA APB interface
- 62 interrupt sources
- Configurable 8 priority levels for each interrupt source
- Configurable 4 trigger types for each interrupt source
- Configurable disabled/enabled status for each interrupt source
- Readable on the current logic value of each interrupt source
- Arbitration of interrupt requests from two or more interrupt sources
- Easy programming of interrupt service routines

6.5 SDRAM Interface Controller

6.5.1 Overview

The SDRAM Controller support DDR2 type SDRAM. The memory device size type can be up to 1G bits. Only 16-bit data bus width is supported. The total system memory size can up to 128M bytes for different SDRAM configuration.

The SDRAM controller interface to three isolated AHB. All these AHB masters can access the memory independent. Except the memory access, the masters of AHB also could access the SDRAM control registers.

For performance and function issue, the SDRAM controller also supports the proprietary Enhanced-AHB. The EAHB add the down-count address mode, byte-enable signal and explicit burst access number. The explicit access number function is reached by modify the HBURST signal to EHBURST and it represent the access number. The maximum EAHB access number is 16. The SDRAM controller also builds a BIST module to test the external memory device.

An internal arbiter is used to schedule the access from the masters and the BIST request, the BIST request with the highest priority and the then the AHB3 master, AHB2 master and AHB1 master.

The SDRAM controller uses 3 pipe queues to improve the SDRAM command and data bus efficiency. The request in queue0 is the SDRAM active data access request. Simultaneous, the requests in queue1 can request the controller to issue the ACTIVE or PRECHARGE command to reduce the access latency for the later command. The queue1 also can issue the READ or WRITE command to close the SDRAM command when advance pipe queue

The SDRAM refresh rate is programmable. The Refresh and Power-on control module generate the refresh request signal and SDRAM power on sequence. The SDRAM controller also supports software reset, SDRAM self-refresh and auto power down function.

6.5.2 Features

- Built-in 128MB/ 64MB DDR2 SDRAM Memory in LQFP package
- Clock speed up to 150 MHz
- Support 16-bit data bus width

6.6 External Bus Interface

6.6.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.6.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)
- Supports address bus and data bus separate mode

6.7 General Purpose I/O

6.7.1 Overview

This chip has up to 104 General-Purpose I/O (GPIO) pins and can be shared with other function pins depending on the chip configuration. These 104 pins are arranged in 7 ports named as PA, PB, PC, PD, PE, PF and PG. PA, PC, PD and PG has 16 pins on port. PB has 14 pins on port. PE and PF has 13 pins on port. Each of the 104 I/O pins is independent and can be easily configured by user to meet various system configurations and design requirements.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output or Open-drain output. After reset, all 104 I/O pins are configured in General-Purpose I/O Input mode.

6.7.2 Features

- Three I/O modes:
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode in PB.0~PB.7
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

6.8 Peripheral DMA Controller

6.8.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 20 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.8.2 Features

- Supports 2 PDMA controller, PDMA0 and PDMA1
- Supports 10 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, SPI, I2C and Timer request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function from channel 0 to channel 9
- Supports stride function from channel 0 to channel 5

6.9 Timer Controller (TMR)

6.9.1 Overview

The timer controller includes six 32-bit timers, Timer0 ~ Timer5, allowing user to easily implement a timer control applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.9.2 Features

- Six sets of 32-bit timers with 24-bit up counter and one 8-bit prescale counter
- Independent Clock Source for each Timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function to count input event from pin TMx_ECNT (x = 0~5)
- Supports toggle output to pin TMx_TGL (x = 0~5)
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports event capture from external pin TMx_EXT (x = 0~5) for interval measurement
- Supports event capture from RTC 1Hz signal for RTC clock calibration
- Supports event capture from external pin TMx_EXT (x = 0~5) to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt or capture interrupt to trigger PDMA.
- Supports Inter-Timer trigger that Timer 0 can trigger Timer 1, Timer 2 can trigger Timer 3, and Timer4 can trigger Timer5.

6.10 Pulse Width Modulation (PWM)

6.10.1 Overview

This chip has 2 PWM controllers, PWM0 and PWM1. Each PWM controller has 4 independent PWM outputs.

PWM0 has 4 independent PWM outputs, CH0~CH3, or 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators. PWM1 has 4 independent PWM outputs, CH4~CH7, or 2 complementary PWM pairs, (CH4, CH5), (CH6, CH7) with 2 programmable dead-zone generators. Each PWM pair has one prescaler, one clock divider, two clock selectors, two 16-bit PWM counters, two 16-bit comparators, and one dead-zone e generator. They are all driven by APB system clock (PCLK) in chip. Each PWM channel can be used as a timer and issue interrupt independently.

Two channels PWM Timers in one pair share the same prescaler. The Clock divider provides each PWM channel with 5 divided clock sources (1, 1/2, 1/4, 1/8, 1/16). Each channel receives its own clock signal from clock divider which receives clock from 8-bit prescaler. The 16-bit down-counter in each channel receive clock signal from clock selector and can be used to handle one PWM period. The 16-bit comparator compares PWM counter value with threshold value in register CMR (PWM_CMR[15:0]) loaded previously to generate PWM duty cycle. The clock signal from clock divider is called PWM clock. Dead-Zone generator utilize PWM clock as clock source. Once Dead-Zone generator is enabled, two outputs of the corresponding PWM channel pair will be replaced by the output of Dead-Zone generator. The Dead-Zone generator is used to control off-chip power device.

To prevent PWM driving output pin with unsteady waveform, 16-bit down-counter and 16-bit comparator are implemented with double buffering feature. User can feel free to write data to counter buffer register and comparator buffer register without generating glitch. When 16-bit down-counter reaches zero, the interrupt request is generated to inform CPU that time is up. When counter reaches zero, if counter is set as periodic mode, it is reloaded automatically and start to generate next cycle. User can set PWM counter as one-shot mode instead of periodic mode. If counter is set as one-shot mode, counter will stop and generate one interrupt request when it reaches zero. The value of comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

6.10.2 Features

- 8 PWM channels with a 16-bit down counter and an interrupt each
- 4 complementary PWM pairs, (CH0, CH1), (CH2, CH3), (CH4, CH5), (CH6, CH7), each with a programmable dead-zone generator
- Internal 8-bit prescaler and a clock divider for each PWM paired channel
- Independent clock source selection for each PWM channel
- Internal 16-bit down counter and 16-bit comparator for each independent PWM channel
- PWM down-counter supports One-shot or Periodic mode

6.11 Watchdog Timer

6.11.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

6.11.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (24 ~ 220) and the time-out interval is 0.48828125ms ~ 32s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting WDTON (SYS_PWRON [3])
- Supports WDT time-out wake-up function only if WDT clock source is selected as LXT.

6.12 Windowed Watchdog Timer (WWDT)

6.12.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.12.2 Features

- 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible.
- Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter.

6.13 Real Time Clock (RTC)

6.13.1 Overview

The Real Time Clock (RTC) controller provides the real time clock and calendar information. The clock source of RTC controller is from an external 32.768 kHz low-speed crystal which connected at pins X32_IN and X32_OUT (refer to pin Description). The RTC controller provides the real time clock (hour, minute, second) in RTC_TIME (RTC Time Loading Register) as well as calendar information (year, month, day) in RTC_CAL (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in RTC_TALM (RTC Time Alarm Register) and alarm calendar in RTC_CALM (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD (Binary Coded Decimal) format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by RTC_TICK (RTC_TICK[2:0] Time Tick Register). When real time and calendar message in RTC_TIME and RTC_CAL are equal to alarm time and calendar settings in RTC_TALM and RTC_CALM, the ALMIF (RTC_INTSTS [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the ALMIEN (RTC_INTEN [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the corresponding interrupt enable bit (ALMIEN or TICKIEN) is set to 1 before chip enters Idle or Power-down mode.

Real Time Clock (RTC) block can operate with independent power supply (RTC_VDD) while the system power is off.

6.13.2 Features

- Supports real time counter and calendar counter for RTC time and calendar check.
- Supports time (hour, minute, second) and calendar (year, month, day) alarm and alarm mask settings.
- Selectable 12-hour or 24-hour time scale.
- Supports Leap Year indication.
- Supports Day of the Week counter.
- Supports frequency compensation mechanism for 32.768 kHz clock source.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm match interrupt.
- Supports chip wake-up from Idle or Power-down mode while alarm or relative alarm interrupt is generated.
- Supports 64 bytes spare registers to store user's important information.
- Supports power on/off control mechanism to control system core power.

6.14 UART Interface Controller (UART)

6.14.1 Overview

The chip provides ten channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN and, RS-485 function modes and auto-baud rate measuring function.

6.14.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART1 /UART2 with LIN function)
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
- Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function

6.15 Smart Card Host Interface

6.15.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

6.15.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Reset (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.16 I²C Serial Interface Controller

6.16.1 Overview

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are four sets of I2C controllers which support Power-down wake-up function.

6.16.2 Features

The I2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I2C bus include:

- Supports up to three I2C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I2C interrupt if the I2C bus hangs up and timer-out counter overflows
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports setup/hold time programmable

6.17 Serial Peripheral Interface (SPI)

6.17.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to one set of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

6.17.2 Features

- Up to two sets of SPI controllers
- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 30 MHz (when chip works at VDD = 2.97~3.63V)
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 4-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.18 Quad Serial Peripheral Interface (QSPI)

6.18.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.18.2 Features

- Supports Master or Slave mode operation
- Master mode up to 100 MHz and Slave mode up to 100 MHz (when chip works at VDD = 2.97~3.63V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.19 I²S Controller (I²S)

6.19.1 Overview

The I2S controller consists of I2S and PCM protocols to interface with external audio CODEC. The I2S and PCM interface supports 8, 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

The following are the property of the DMA.

- When 16-bit precision, the DMA always 8-beat incrementing burst (FIFO_TH = 0) or 4-beat incrementing burst (FIFO_TH = 1).
- When 24/20/18-bit precision, the DMA always 16-beat incrementing burst (FIFO_TH = 0) or 8-beat incrementing burst (FIFO_TH = 1).
- Always bus lock when 4-beat or 8-beat or 16-beat incrementing burst.
- When reach eighth, quarter, middle and end address of destination address, a DMA_IRQ is triggered to CPU automatically.

An AHB master port and an AHB slave port are offered in I2S controller.

6.19.2 Features

- Support I2S interface record and playback
  - Left/right channel
  - 8, 16, 20, 24-bit data precision
  - Mater and slave mode
- Support PCM interface record and playback
  - Two slots
  - 8, 16, 20, 24-bit data precision
  - Master mode
- Use DMA to playback and record data, with interrupt
- Support two addresses for left/right channel data and different slots

6.20 Ethernet MAC Controller (EMAC)

6.20.1 Overview

This chip provides 2 Ethernet MAC Controller (EMAC) for Network application.

The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses; Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller.

The EMAC supports RMII (Reduced MII) interface to connect with external Ethernet PHY.

6.20.2 Features

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports RMII interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function

6.21 High Speed USB 2.0 Device Controller (HSUSBD)

6.21.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISOCHRONOUS. The USB device controller has a built-in DMA to relieve the load of CPU.

6.21.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4096 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

6.22 USB 2.0 Host Controller (USBH)

6.22.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with eight USB ports (two ports with on-chip USB 2.0 high speed transceiver and up to six USB 1.1 Host Lite ports), a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

6.22.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports a USB host port with on-chip USB2.0 high speed transceiver shared with USB device (dual-role function).
- Supports a USB host only port with on-chip USB2.0 high speed transceiver.
- Supports up to six USB 1.1 Host Lite ports.
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

6.23 Controller Area Network (CAN)

6.23.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.23.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.24 Flash Memory Interface (FMI)

6.24.1 Overview

The Flash Memory Interface (FMI) in this chip has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (ex. SDRAM) and shared buffer (128 bytes), and the FMI unit control the interface of SD0/eMMC0 or NAND Flash. The interface controller can support SD0/eMMC0 and NAND-type Flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.24.2 Features

- Supports single DMA channel and address in non-word boundary.
- Supports hardware Scatter-Gather function.
- Supports 128Bytes shared buffer for data exchange between system memory and Flash device. (Separate into two 64 bytes ping-pong FIFO).
- Supports SD0/eMMC0 Flash device.
- Supports SLC and MLC NAND type Flash.
- Adjustable NAND page sizes. (2048B+spare area, 4096B+spare area and 8192B+spare area).
- Supports up to 8bit/12bit/24bit hardware ECC calculation circuit to protect data communication.
- Supports programmable NAND timing cycle

6.25 Secure Digital Host Controller (SDH)

6.25.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SD Host Controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.25.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function..
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.26 Cryptographic Accelerator (CRYPTO)

6.26.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA, HMAC, RSA and ECC algorithms.

The PRNG core supports 64 bits, 128 bits, 192 bits, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512 and corresponding HMAC algorithms.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with 1024 and 2048 bit RSA cryptography.

6.26.2 Features

- PRNG
  - Supports 64 bits, 128 bits , 192 bits, and 256 bits random number generation
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB , CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode
  - Supports key expander
- SHA
  - Supports FIPS NIST 180, 180-2
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, and SHA-512
- HMAC
  - Supports FIPS NIST 180, 180-2
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512
- ECC
  - Supports both prime field GF(p) and binary filed GF(2m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)
- RSA
  - Supports both encryption and decryption

- Supports up to 2048 bits

6.27 Capture Sensor Interface Controller (CAP)

6.27.1 Overview

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO output them into frame buffer.

6.27.2 Features

- 8-bit RGB565 sensor
- 8-bit YUV422 sensor
- Supports CCIR601 YCbCr color range scale to full YUV color range
- Supports 4 packaging format for packet data output: YUYV, Y only, RGB565, RGB555
- Supports YUV422 planar data output
- Supports the CROP function to crop input image to the required size for digital application
- Supports the down scaling function to scale input image to the required size for digital application
- Supports frame rate control
- Supports field detection and even/odd field skip mechanism
- Supports packet output dual buffer control through hardware buffer controller
- Supports negative/sepia/posterization color effect

6.28 Analog to Digitial Converter (ADC)

6.28.1 Overview

The NuMicro® NUC980 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with 9 input channels.

6.28.2 Features

- Resolution: 12-bit resolution
- DNL: +/-1.5 LSB, INL: +/-3 LSB
- Data Rate up to 200kSPS
- Analog Input Range: V_{REF} to AGND, can be rail-to-rail
- Analog Supply: 2.7-3.6V
- Digital Supply: 1.2V
- 9 Single-Ended analog inputs
- Auto Power Down
- Low Power Consumption: 2170uW (at 200k SPS), < 1uA

7 ELECTRICAL CHARACTERISTICS

7.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
V_{VDD12}–V_{VSS}	Core DC Power Supply	-0.3	+1.5	V
V_{VDD33}–V_{VSS}	I/O DC Power Supply	-0.3	+4.6	V
MV_{DD} - $MV_{VSS(2)}$	I/O DC Power Supply for DDR2 Type SDRAM	-0.3	+2.3	V
V_{IN}	Input Voltage	V_{VSS}-0.3	+5	V
T_A	Ambient Operating Temperature	-40	+85	°C
T_J	Junction Operating Temperature	-40	+125	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into CORE_VDD	-	200	mA
I_{SS}	Maximum Current out of CORE_VSS	-	200	mA
I_{IO}	Maximum Current sunk by a I/O pin	-	20	mA
	Maximum Current sourced by a I/O pin	-	30	mA
	Maximum Current sunk by total I/O pins	-	200	mA
	Maximum Current sourced by total I/O pins	-	200	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

7.2 DC Electrical Characteristics

7.2.1 NUC980 Series DC Electrical Characteristics

(VDD33-VSS=3.3V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
Core Operation voltage	V_{DD12}	1.14	1.2	1.32	V	
I/O Operation Voltage	V_{DD33}	2.97	3.3	3.63	V	
Memory I/O Operation Voltage for DDR2	MV_{DD}	1.70	1.8	1.90	V	
Battery Operation Voltage	V_{BAT33}	2.0	3.3	3.63	V	
USB Operation Voltage (1)	V_{USB0_VDD12} V_{USB1_VDD12}	1.14	1.2	1.32	V	
USB Operation Voltage (2)	V_{USB0_VDD33} V_{USB1_VDD33}	2.97	3.3	3.63	V	
Power Ground	V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD33}	2.97	3.3	3.63	V	
Analog Reference Voltage	AVref	0		AV_{DD33}	V	
Current Consumption of Normal Operating Mode 1	I_{VDD12}		150		mA	V_{DD12} = 1.2V MV_{DD} = 1.8V V_{DD33} = 3.3V TA = 25°C, F_{OSC} = 12 MHz Frequency of CPUCLK/DDR2_CLK is 300/150 MHz. All IPs on, all GPIO are input with pull-up.
	I_{MVDD_1}		50		mA	
	$I_{USB0_VDD12_1}$		7.5		mA	
	$I_{USB1_VDD12_1}$		7.5		mA	
	$I_{USB0_VDD33_1}$		35		mA	
	$I_{USB1_VDD33_1}$		35		mA	
	I_{VBAT33_1}		100		uA	
Current Consumption of Normal Operating Mode 2	I_{VDD12}		132		mA	V_{DD12} = 1.2V MV_{DD} = 1.8V V_{DD33} = 3.3V TA = 25°C, F_{OSC} = 12 MHz Frequency of CPUCLK/DDR2_CLK is 264/132 MHz. All IPs on, all GPIO are input with pull-up.
	I_{MVDD_2}		44		mA	
	$I_{USB0_VDD12_2}$		7.5		mA	
	$I_{USB1_VDD12_2}$		7.5		mA	
	$I_{USB0_VDD33_2}$		35		mA	
	$I_{USB1_VDD33_2}$		35		mA	
	I_{VBAT33_2}		100		uA	
Current Consumption of Power Down Mode	I_{STDBY_VDD12}		3		mA	V_{DD12} = 1.2V
	I_{STDBY_MVDD}		6		mA	MV_{DD} = 1.8V

Parameter	Sym.	Specification				Test Conditions
		MIN.	TYP.	Max.	Unit	
	I_{STDBY_VDD33}		5		μA	V_{DD33} = 3.3V
	$I_{STDBY_USB0_VDD33}$		0		μA	V_{USB0_VDD33} = 3.3V
	$I_{STDBY_USB1_VDD33}$		0		μA	V_{USB1_VDD33} = 3.3V
	$I_{STDBY_USB0_VDD12}$		2.5		μA	V_{USB0_VDD12} = 1.2V
	$I_{STDBY_USB1_VDD12}$		2.5		μA	V_{USB1_VDD12} = 1.2V
	I_{STDBY_AVDD33}		25		μA	AV_{DD33} = 3.3V
	I_{STDBY_VBAT33}		100		μA	V_{BAT33} = 3.3V
System Power Off & RTC V_{BAT33} Power only	I_{VBAT33}		10		uA	

7.2.2 NUC980 Series GPIO Characteristics

(V_{DD33}-V_{SS}=3.3 V, TA = 25°C, F_{OSC} = 12 MHz unless otherwise specified.)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input Leakage Current PA, PB, PC, PD, PE, PF, PG	I_{LK1}	-10	-	10	μA	V_{VDD33} = 3.63V 0V < V_{IN} < V_{VDD33}
Input Low Voltage PA, PB, PC, PD, PE, PF, PG (TTL input)	V_{IL1}	-	-	0.8	V	V_{DD33} = 3.63V
Input High Voltage PA, PB, PC, PD, PE, PF, PG (TTL input)	V_{IH1}	2.0	-	-	V	V_{DD33} = 3.63V
Input Low Voltage PA, PB, PC, PD, PE, PF, PG, (Schmitt input)	V_{IL2}			0.3*V_{DD33}	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PG, (Schmitt input)	V_{IH2}	0.7*V_{DD33}			V	
Output Low Voltage PA, PB, PC, PD, PE, PF, PG	V_{OL}			0.4	V	
Output High Voltage PA, PB, PC, PD, PE, PF, PG	V_{OH}	2.4			V	
Hysteresis voltage PA, PB, PC, PD, PE, PF, PG (Schmitt input)	V_{HY}		0.2*V_{DD33}		V	
Source Current PA, PB, PC, PD, PE, PF, PG, (Push-pull Mode)	I_{SR21}		8		mA	V_{DD33} = 3.63V V_{IN}=V_{DD33}-0.4
Sink Current PA, PB, PC, PD, PE, PF, PG (Push-pull Mode)	I_{SK1}		8		mA	V_{DD33} = 3.63V V_{IN}=V_{SS}+0.4
Input Pull-up Resistance PA, PB, PC, PD, PE, PF, PG, HDS	R_{PU}	-	-	82	kΩ	V_{DD33}=3.63V, apply GPIO pin Vin= 0V and measure the input current Reverse the current to Resistor value, R=V/I
Input Pull-down Resistance PA, PB, PC, PD, PE, PF, PG	R_{PD}	-	-	91	kΩ	V_{DD33}=3.63V, apply GPIO pin Vin= 3.63V and measure the input current Reverse the current to Resistor value, R=V/I

7.3 AC Electrical Characteristics

7.3.1 External 12MHz High Speed Crystal

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.97	3.3	3.63	V	$V_{HXT} = V_{DD33}$
T_A	Temperature	-40	-	85	°C	-
f_{HXT}	Clock Frequency	-	12	-	MHz	-
I_{HXT}	Operating Current	-	0.8	-	mA	TA=25°C, AV_{DD33}=3.3V

Note: Guaranteed by characterization results, not tested in production.

7.3.1.1 Typical Crystal Application Circuits

Crystal	ESR (ohm)	C1, C2
12 MHz	< 50	15 pf

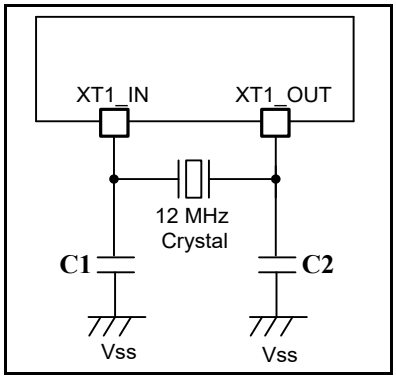


Figure 7.3-1 Typical HXT Crystal Application Circuit

7.3.2 External 32.768 kHz Low Speed Crystal

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{LXT}	Operation Voltage	2.97	3.3	3.63	V	$V_{LXT} = V_{BAT33}$
T_A	Temperature	-40	-	85	°C	-
f_{LXT}	Clock Frequency	-	32.768	-	kHz	-
I_{LXT}	Operating Current		1.6		uA	TA=25°C, V_{BAT33}=3.3V

Note: Guaranteed by characterization results, not tested in production.

7.3.2.1 Typical Crystal Application Circuits

Crystal	C1	C2
32.768 kHz	15 pf	15 pf

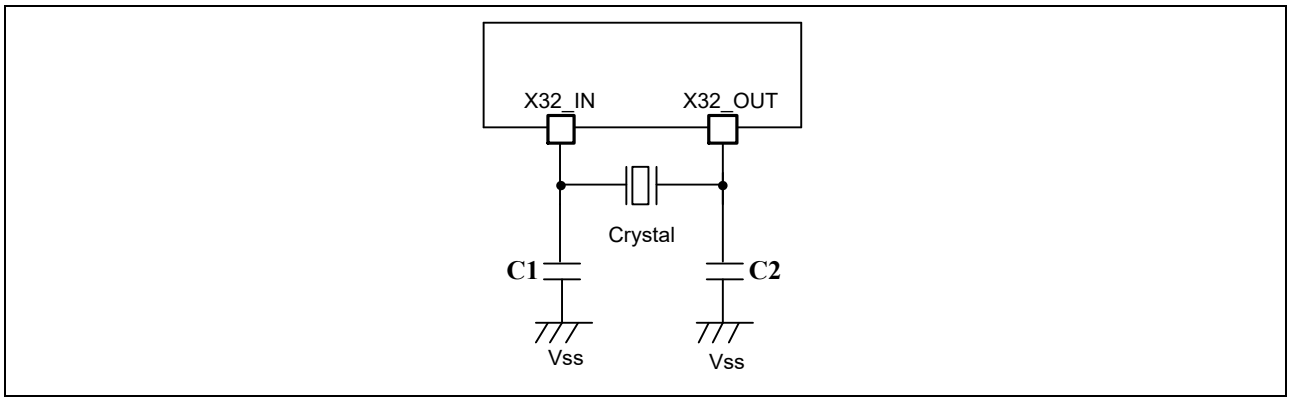


Figure 7.3-2 Typical LXT Crystal Application Circuit

7.3.3 Power Sequence & nRESET Timing

7.3.3.1 Power up Sequence

Power up Sequence & nRESET Timing Case 1

When $T_{VDD33} \geq T_{MVDD} \geq T_{VDD12}$ (the time of delay gap between < 0.5mS is prefer).

Note:

1. The time of delay gap is meaning that timing between T_{VDD33} with T_{VDD12}.
2. If the time of delay gap < 0.5mS will be effective to prevent that transient phenomenon by power-on.

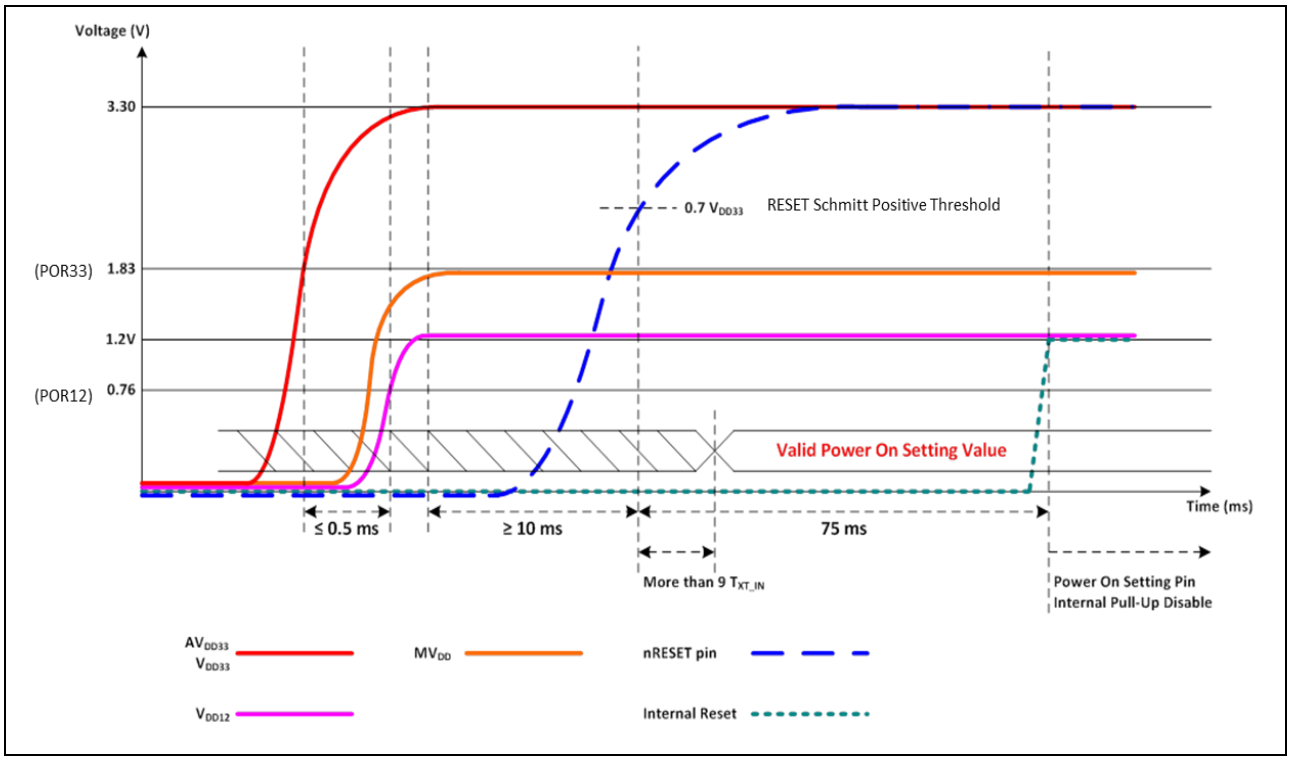


Figure 7.3-3 Power up Sequence & nRESET timing Case 1

Power up Sequence & nRESET Timing Case 2

When $T_{VDD12} \geq T_{MVDD} \geq T_{VDD33}$, it is acceptable as the below figure. (the time of delay gap between < 1mS is prefer)

Note:

1. The time of delay gap is meaning that timing between T_{VDD12} with T_{VDD33}.
2. The time of delay gap < 1mS is prefer although NUC980 has that protection of latchup prevention.

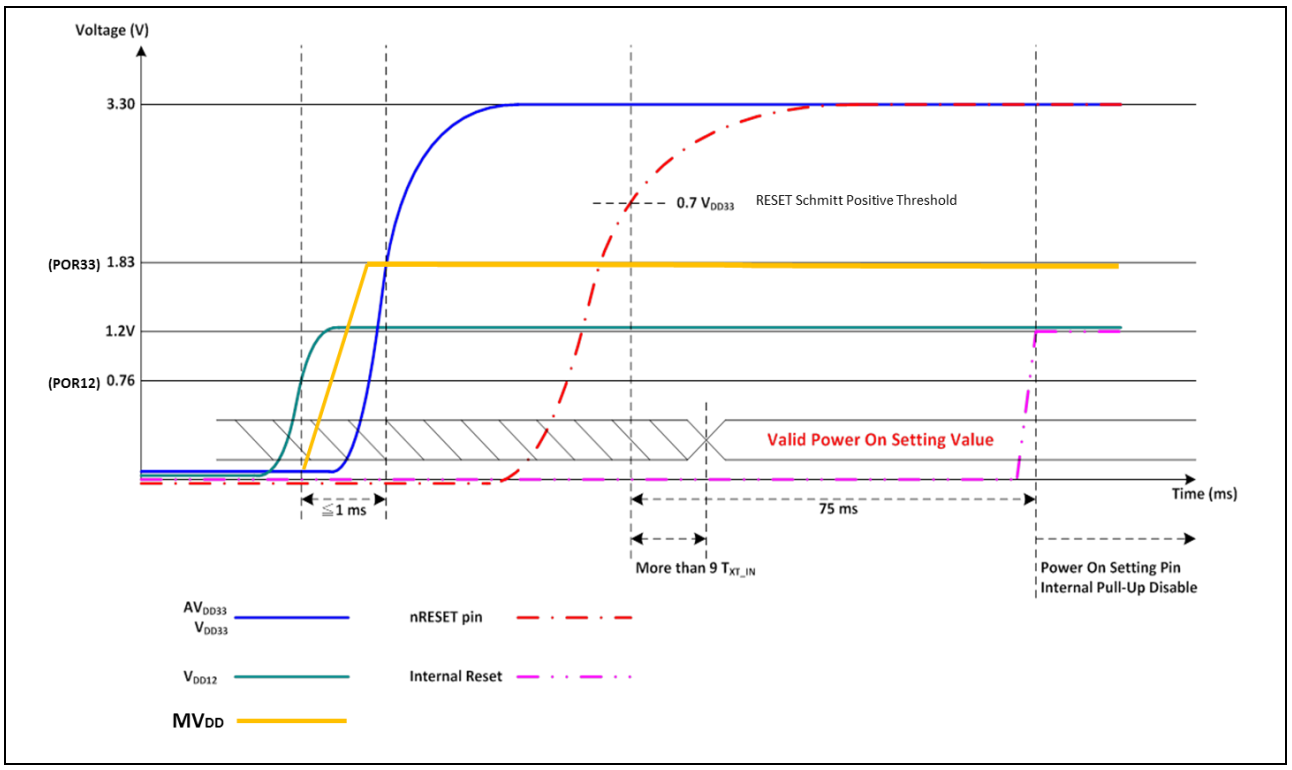


Figure 7.3-4 Power up Sequence & nRESET timing Case 2

7.3.3.2 Power down Sequence,

Power down sequence between AV_{DD33}/V_{DD33}, V_{DD12} and MV_{DD} is don't care.

Note:

1. T_{VDD12} represents V_{DD12} powered time.
2. T_{MVDD} represents MV_{DD} powered time.
3. T_{VDD33} represents V_{DD33}/AV_{DD33} powered.

7.3.4 nRESET PIN characteristics

Symbol	Parameter	Min.	Typ.	Max.	unit	Test Conditions
V_{ILR}	Negative going threshold (Schmitt input), nRESET	-	-	$0.3*V_{DD33}$	V	V_{DD33} = 3.3V
V_{IHR}	Positive going threshold (Schmitt Input), nRESET	$0.7*V_{DD33}$	-	-	V	V_{DD33} = 3.3V
R_{RST}	Internal nRESET pin pull up resistor	-	-	84	KΩ	V_{DD33}=3.63V, apply nRESET pin Vin= 3.63V and measure the input current Reverse the current to Resistor value, R=V/I
t_{FR1}	nRESET input filtered time		32		uS	V_{DD33} = 3.3V

Note: Guaranteed by characterization and design results, not tested in production.

7.3.5 PLL characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock			12		MHz
f_{PLL_OUT}	PLL multiplier output clock		25		500	MHz
T_S	PLL stable time[*1]		100		200	µs
Jitter	Cycle-to-cycle Jitter[*2]	Peak to peak @ 300M		150		ps
I_{DD12}	Power consumption	V_{DD12}=1.2V@500MHz			3	mA

Note: Guaranteed by characterization and design results, not tested in production.

7.3.6 EBI Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{tACS}	Address Setup Time to EBI_nCS Falling Edge	-	0	-	T_{HCLK}[1]	-
T_{tCOS}	EBI_nCS Setup Time to EBI_nWE or EBI_nOE Falling Edge	-	1	-	T_{HCLK}[1]	-
T_{tACC}	EBI_nWE or EBI_nOE Active Low Time	1	-	32	T_{HCLK}[1]	-
T_{tCOH}	EBI_nCS Hold Time from EBI_nWE or EBI_nOE Rising Edge	0	-	8	T_{HCLK}[1]	-
$T_{SU_EBI_RD}$	EBI_DATA Read Setup Time to EBI_nOE Rising Edge	1	-	-	T_{HCLK}[1]	-

Notes:

1. T_{HCLK} is the period of EBI's operating clock.

Table 7.3-1 EBI Characteristics

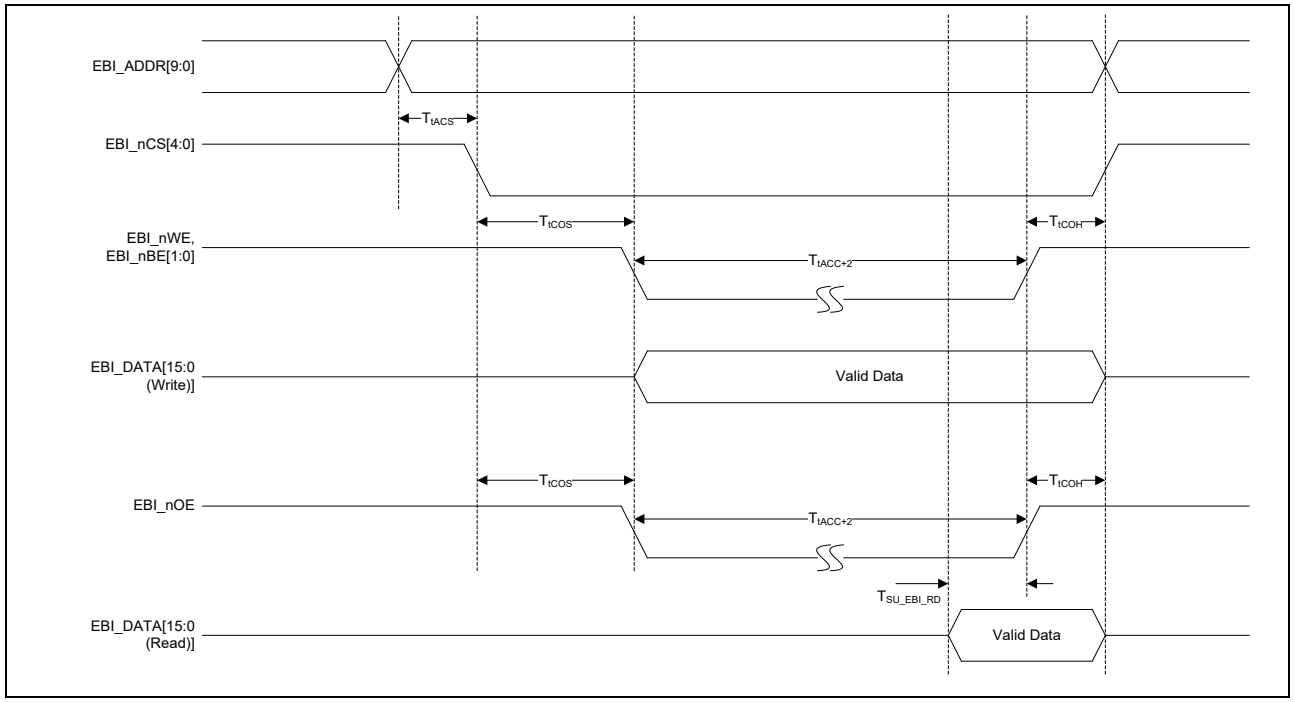


Figure 7.3-5 External Bus Interface Timing Diagram

7.3.7 I2C Interface Timing

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I^2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I^2C frequency.
3. I^2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 7.3-2 I^2C Interface Characteristics

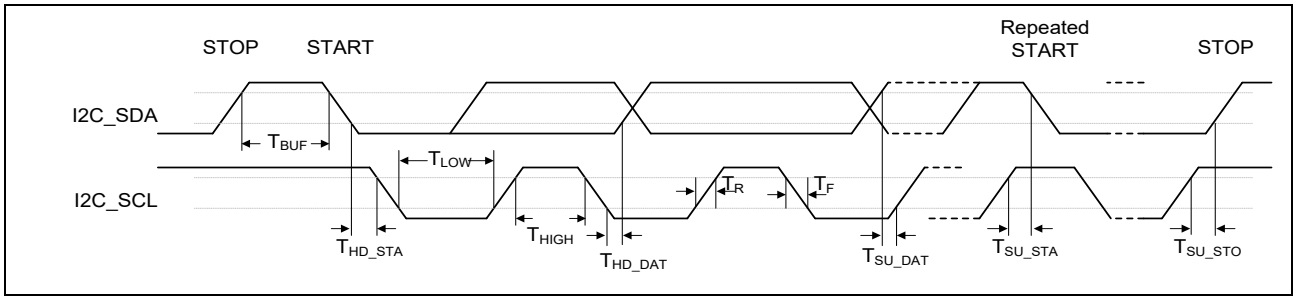


Figure 7.3-6 I2C Interface Timing Diagram

7.3.8 SPI Interface Timing

7.3.8.1 SPI Master Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	2.97V ≤ V_{DD} ≤ 3.63V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	1.8	-	-	ns	
t_{DH}	Data input hold time	3.8	-	-	ns	
t_V	Data output valid time	-	-	1.1	ns	
Note:						

Table 7.3-3 SPI Master Mode Characteristics

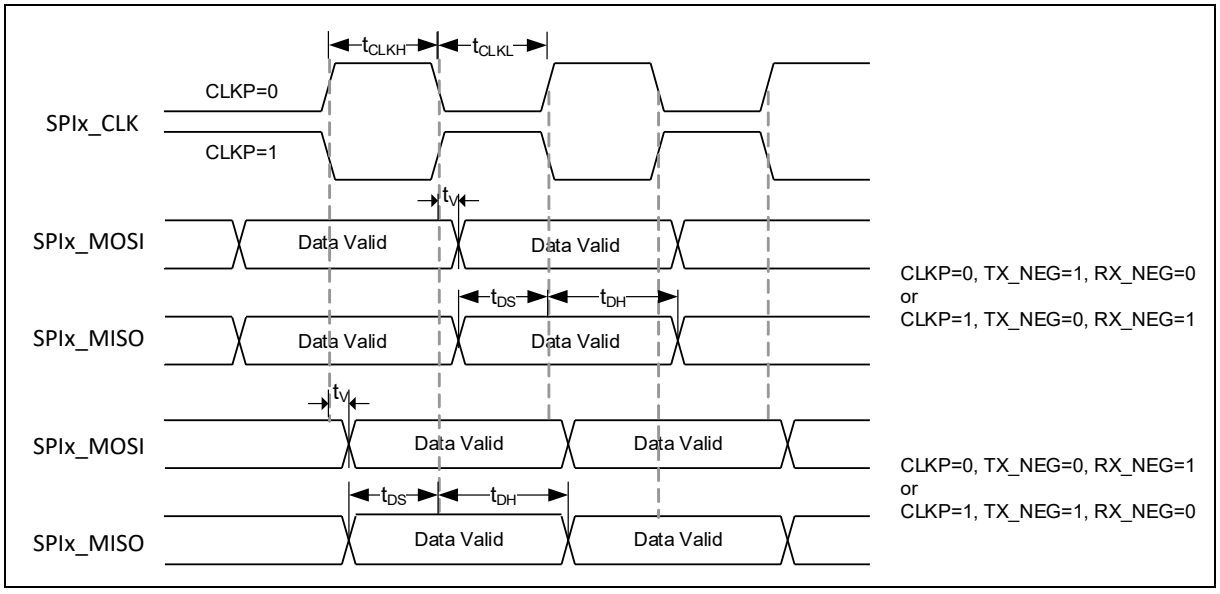


Figure 7.3-7 SPI Master Mode Timing Diagram

7.3.8.2 SPI Slave Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	30	MHz	2.97V ≤ V_{DD} ≤ 3.63V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.97V ≤ V_{DD} ≤ 3.63V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1	-	-	ns	
t_{DH}	Data input hold time	3	-	-	ns	
t_V	Data output valid time	-	-	10	ns	2.97V ≤ V_{DD} ≤ 3.63V, CL = 30 pF
Note:						

Table 7.3-4 SPI Slave Mode Characteristics

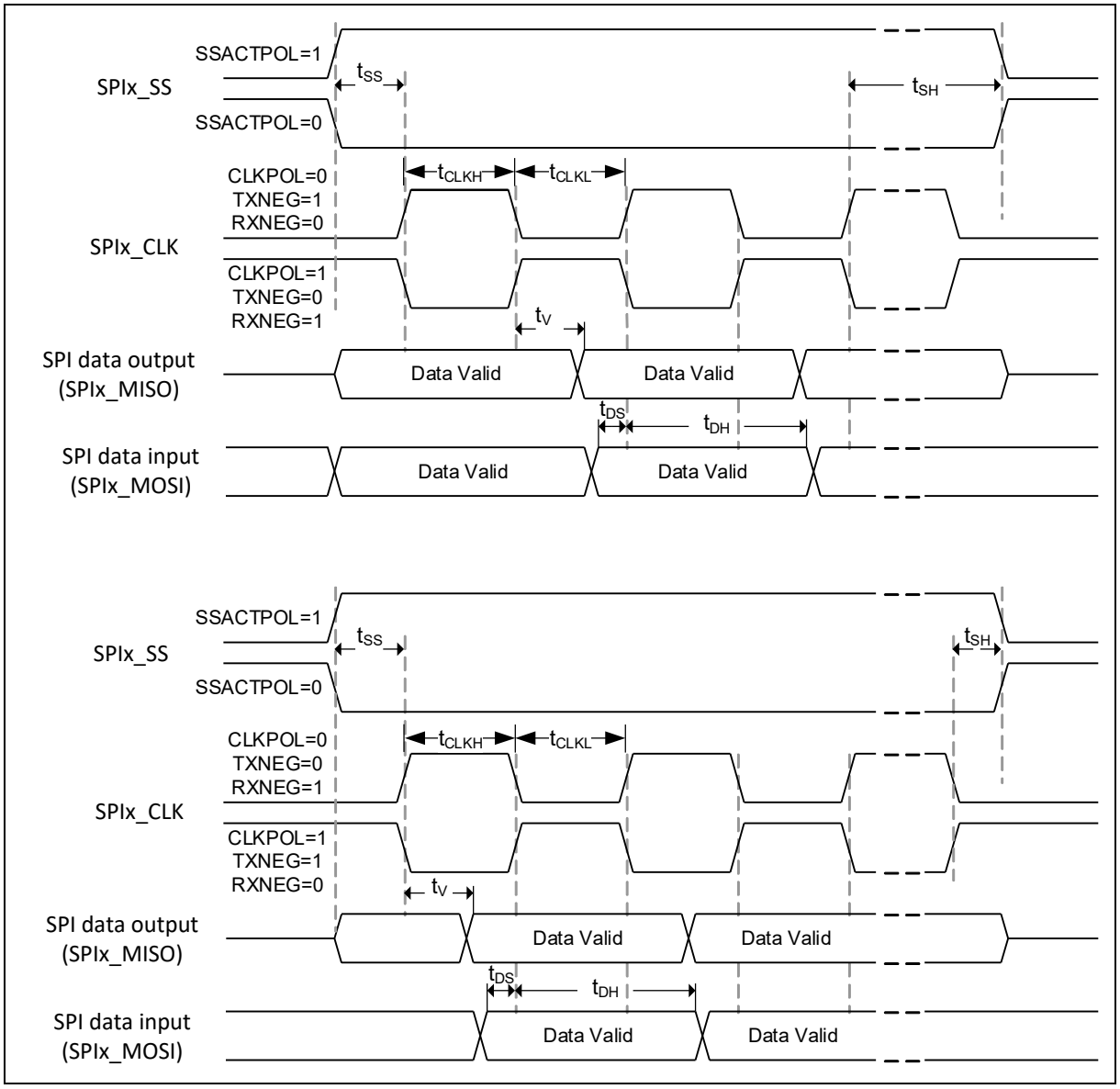


Figure 7.3-8 SPI Slave Mode Timing Diagram

7.3.9 QSPI Interface Timing

7.3.9.1 QSPI Master Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	2.97V ≤ V_{DD} ≤ 3.63V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	1.8	-	-	ns	
t_{DH}	Data input hold time	3.8	-	-	ns	
t_V	Data output valid time	-	-	1.5	ns	
Note:						

Table 7.3-5 QSPI Master Mode Characteristics

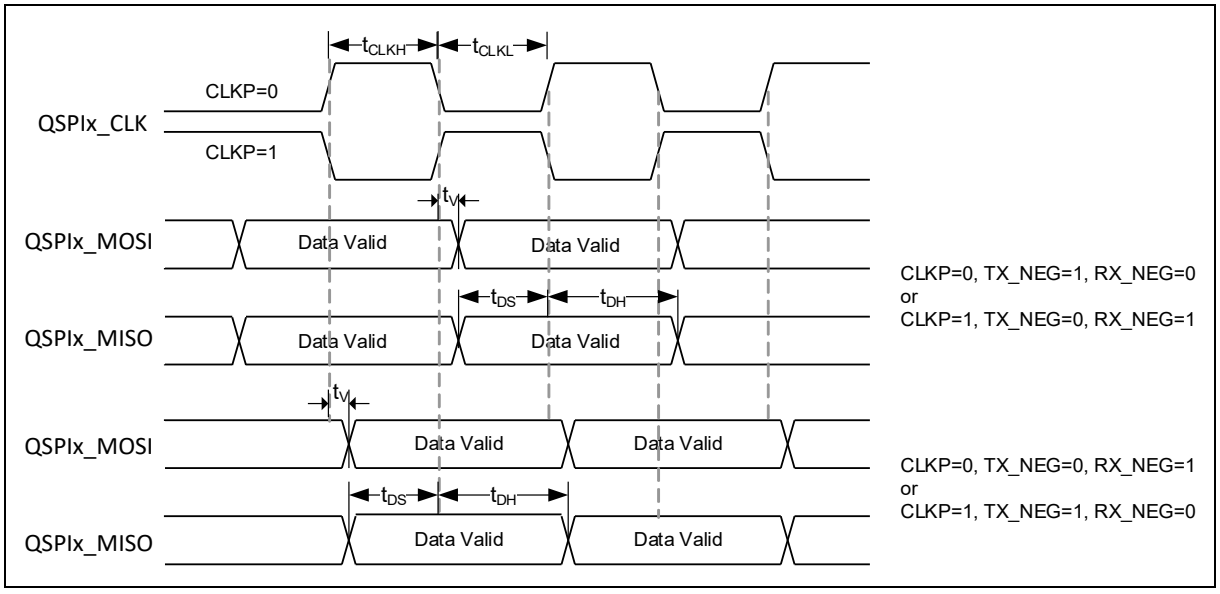


Figure 7.3-9 QSPI Master Mode Timing Diagram

7.3.9.2 QSPI Slave Mode Timing

Symbol	Parameter	Specificaitons				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	30	MHz	2.97V ≤ V_{DD} ≤ 3.63V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	2.97V ≤ V_{DD} ≤ 3.63V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	2.1	-	-	ns	
t_{DH}	Data input hold time	4.1	-	-	ns	
t_V	Data output valid time	-	-	11.5	ns	2.97V ≤ V_{DD} ≤ 3.69V, CL = 30 pF
Note:						

Table 7.3-6 QSPI Slave Mode Characteristics

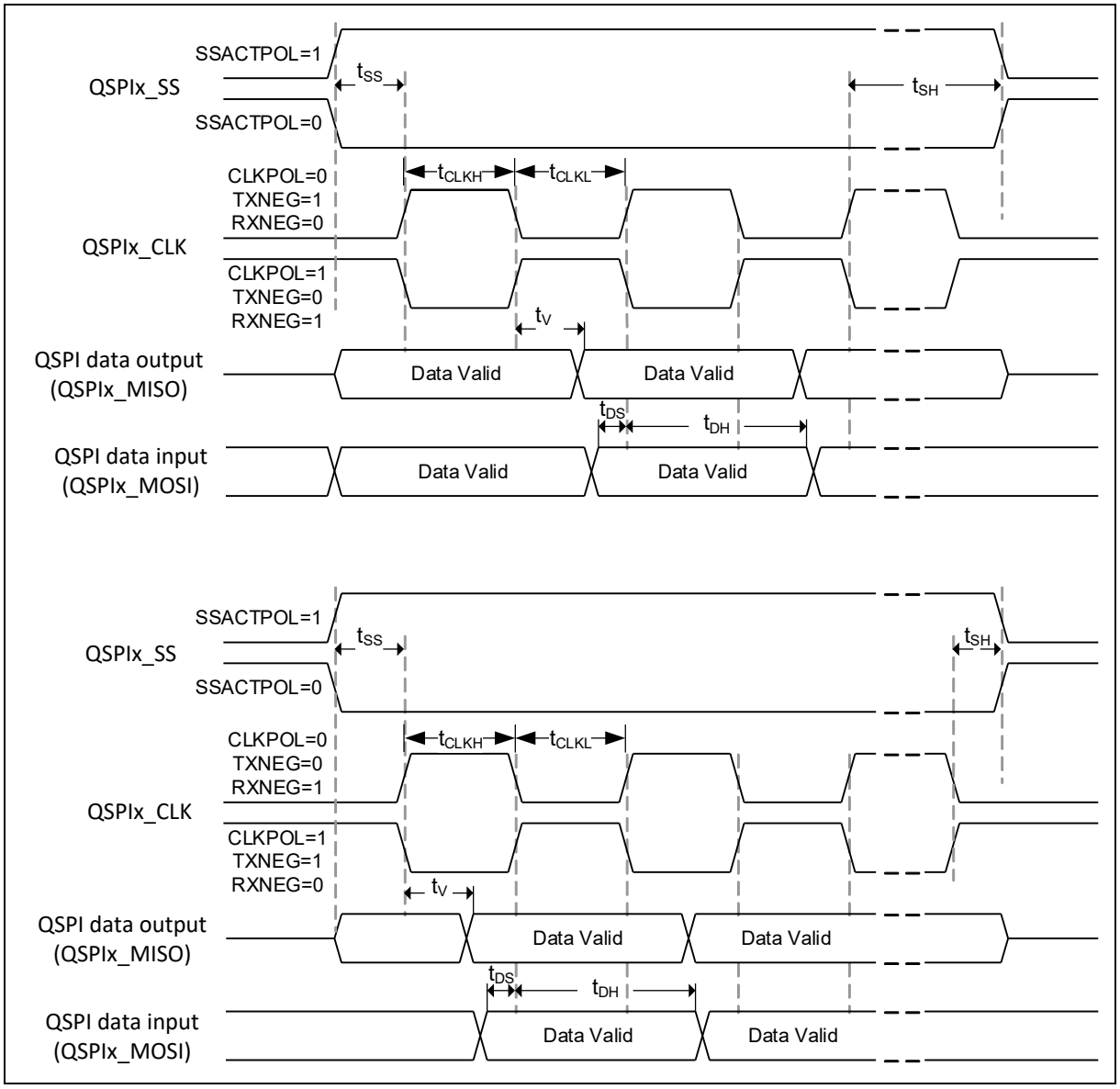


Figure 7.3-10 QSPI Slave Mode Timing Diagram

7.3.10 I2S Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_I2S_BITCLK}$	I2S_BITCLK Period	50	-	-	ns	-
$T_{H_I2S_BITCLK}$	I2S_BITCLK High Time	25	-	-	ns	-
$T_{L_I2S_BITCLK}$	I2S_BITCLK Low Time	25	-	-	ns	-
$T_{DLY_I2S_DO}$	I2S_BITCLK Rising to Valid I2S_WS or I2S_DATAO Delay	-	-	6	ns	-
$T_{HD_I2S_DO}$	I2S_WS or I2S_DATAO Hold Time from I2S_BITCLK Rising	1	-	-	ns	
$T_{SU_I2S_DI}$	I2S_DATAI Setup Time to I2S_BITCLK Rising	5	-	-	ns	-
$T_{HD_I2S_DI}$	I2S_DATAI Hold Time from I2S_BITCLK Rising	3	-	-	ns	-

Table 7.3-7 I²S Interface Characteristics

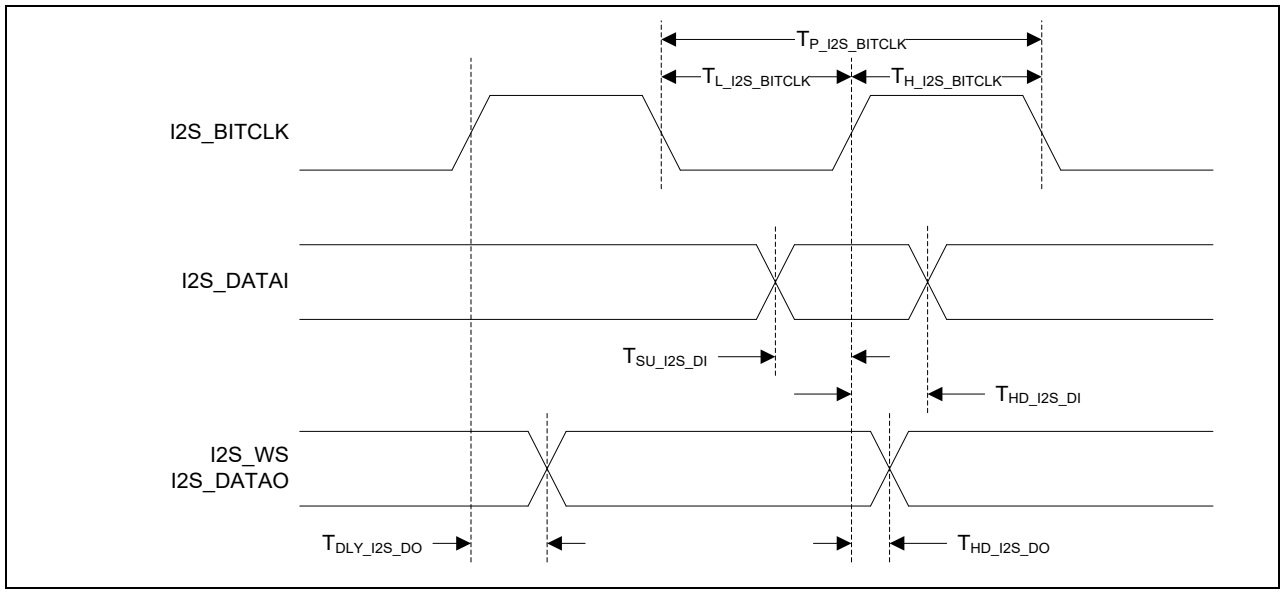


Figure 7.3-11 I2S Interface Timing Diagram

7.3.11 Ethernet Interface Timing

7.3.11.1 RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_RMII_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H_RMII_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L_RMII_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY_RMII_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	17.3	ns	-
$T_{SU_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

Table 7.3-8 RMII Interface Characteristics

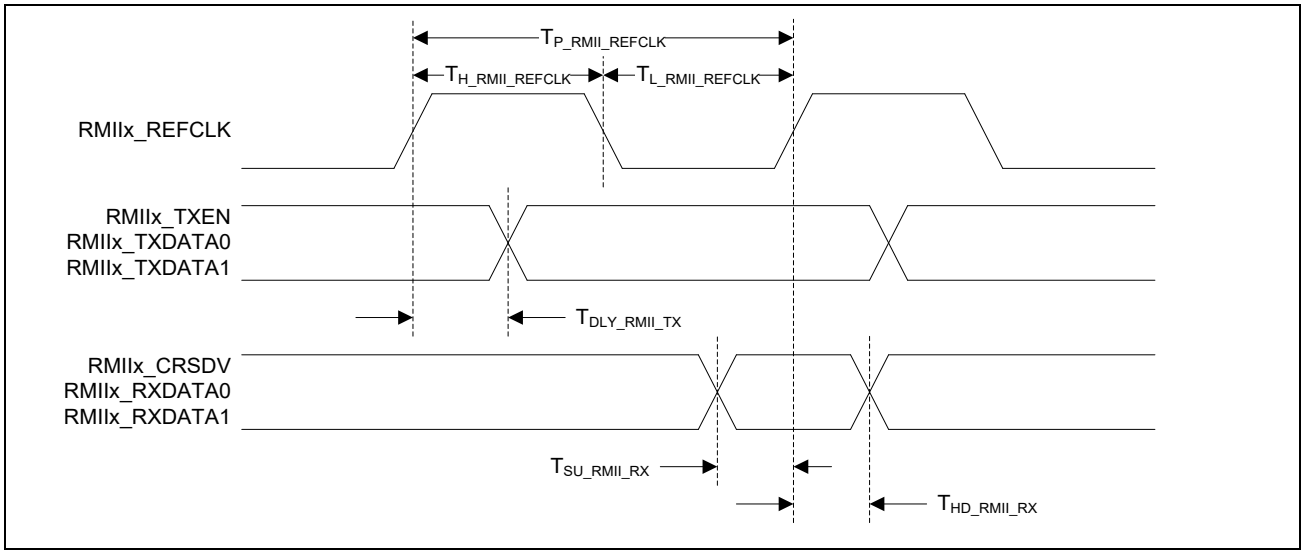


Figure 7.3-12 RMII Interface Timing Diagram

7.3.11.2 Ethernet PHY Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_RMII_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H_RMII_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L_RMII_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY_RMII_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU_RMII_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD_RMII_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

Table 7.3-9 Ethernet PHY Management Interface Characteristics

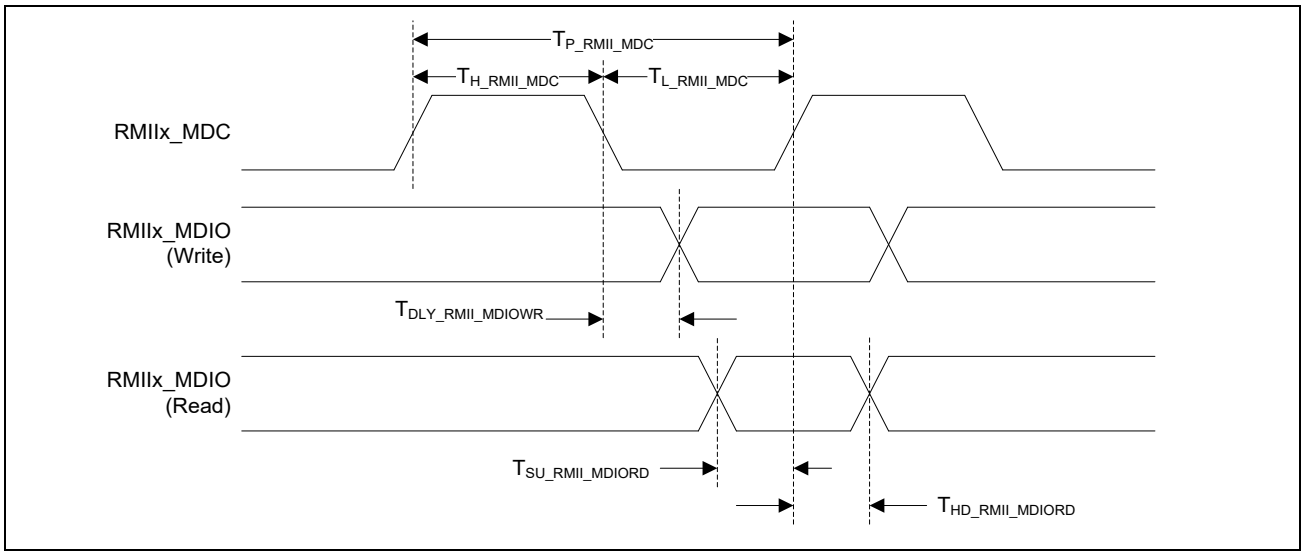


Figure 7.3-13 Ethernet PHY Management Interface Timing Diagram

7.3.12 NAND Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{H_NAND_nWE}$	NAND_nWE High Time	-	13.34[1]	-	ns	-
$T_{L_NAND_nWE}$	NAND_nWE Low Time	-	40[2]	-	ns	-
$T_{DLY_DATA_OUT}$	NAND_nRE Falling to Valid NAND_DATA Delay	-	-	35[3]	ns	-
$T_{HD_DATA_OUT}$	NAND_DATA Hold Time from NAND_nRE Rising	-	-	30[3]	ns	-
$T_{SU_DATA_IN}$	NAND_DATA Setup Time to NAND_nWE Rising	20[3]	-	-	ns	-
$T_{HD_DATA_IN}$	NAND_DATA Hold Time from NAND_nWE Rising	10[3]	-	-	ns	-

Notes:

1. NAND controller operating clock is 150 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.
2. NAND controller operating clock is 150 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.
3. NAND controller operating clock is 150 MHz.

Table 7.3-10 NAND Interface Characteristics

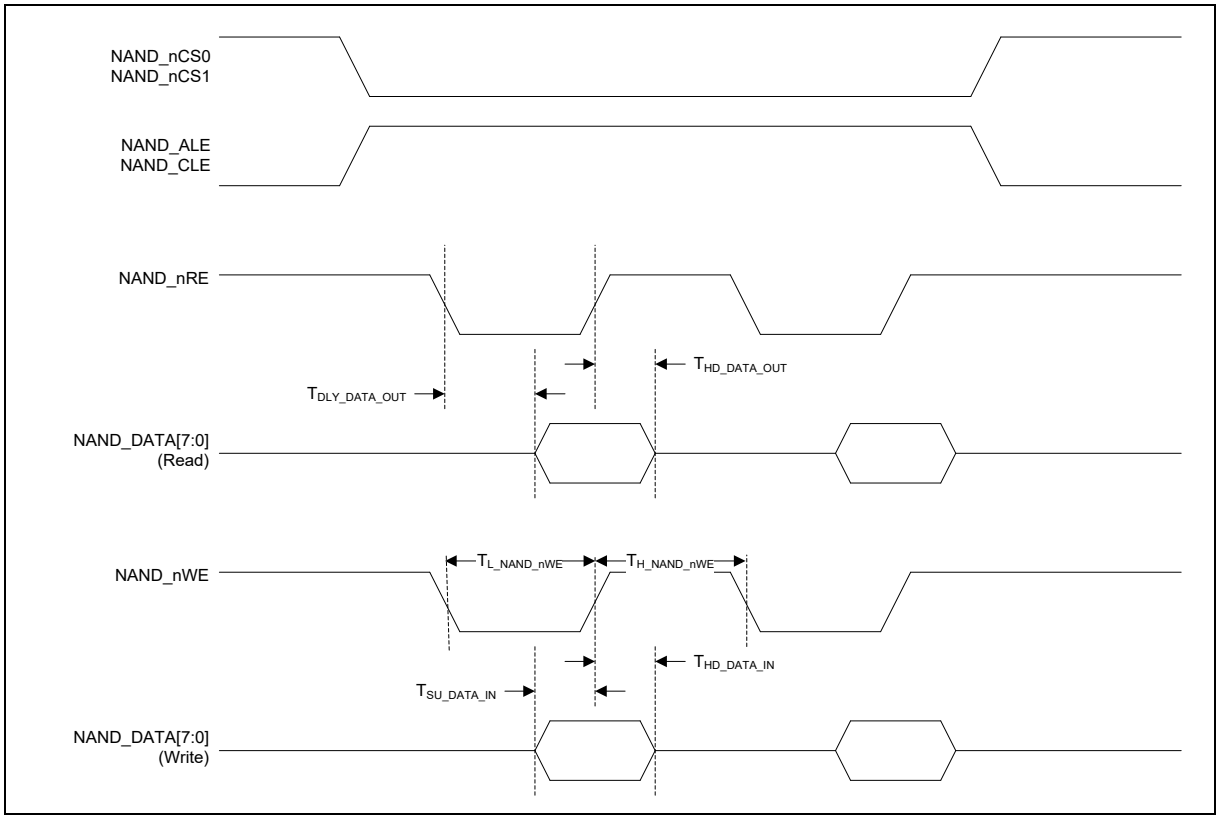


Figure 7.3-14 NAND Interface Timing Diagram

7.3.13 SD Interface Timing

7.3.13.1 Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P_SD_CLK_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H_SD_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Table 7.3-11 SD Interface Default Mode Characteristics

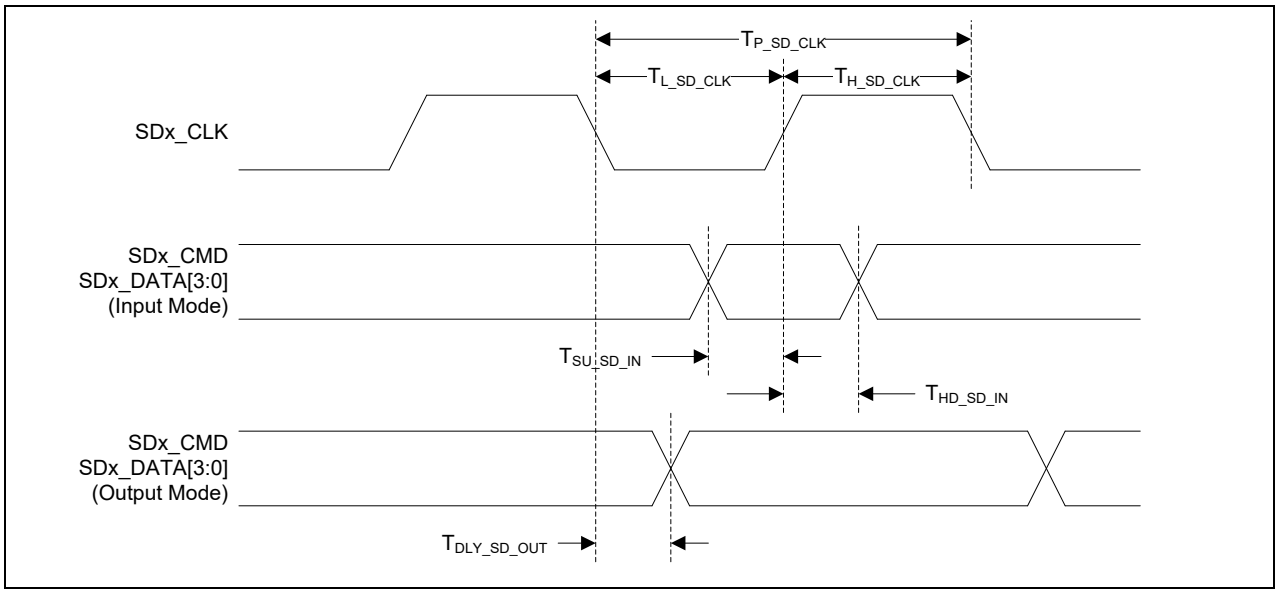


Figure 7.3-15 SD Interface Default Mode Timing Diagram

7.3.13.2 High-Speed Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H_SD_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD_SD_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Table 7.3-12 SD Interface High-Speed Mode Characteristics

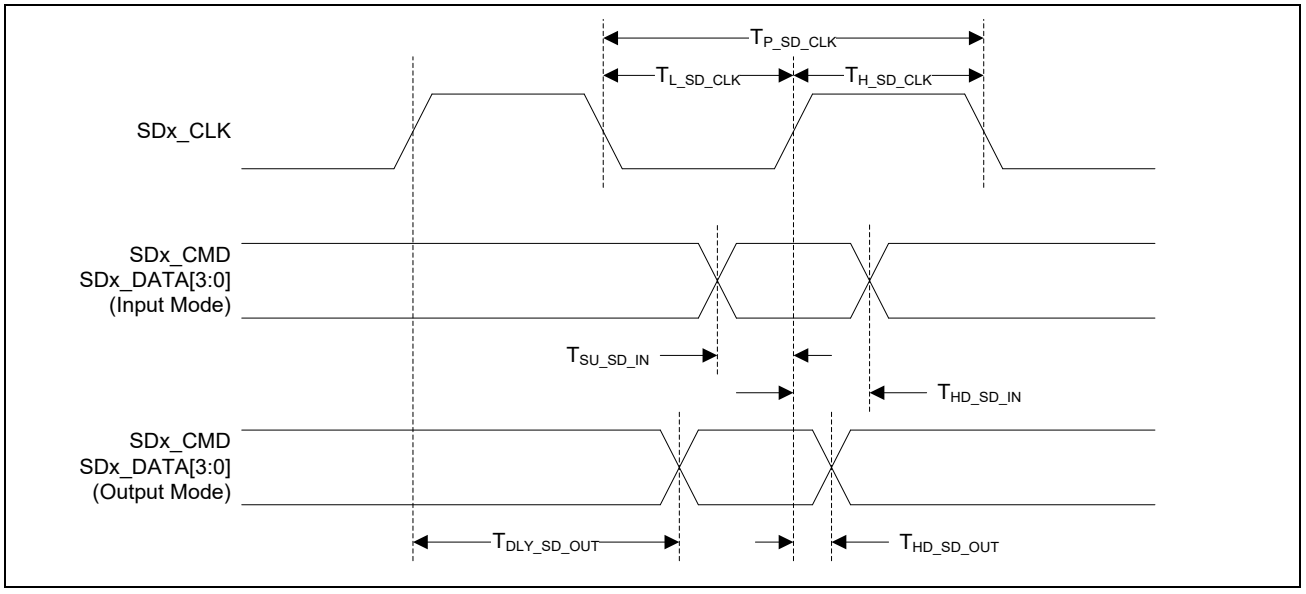


Figure 7.3-16 SD Interface High-Speed Mode Timing Diagram

7.3.14 Capture Sensor Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_VCAP_PCLK}$	VCAP_PCLK Period	20	-	-	ns	-
$T_{H_VCAP_PCLK}$	VCAP_PCLK High Time	-	10.0	-	ns	-
$T_{L_VCAP_PCLK}$	VCAP_PCLK Low Time	-	10.0	-	ns	-
$T_{SU_VCAP_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Setup Time to VCAP_PCLK Rising	4	-	-	ns	-
$T_{HD_VCAP_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Hold Time from VCAP_PCLK Rising	1	-	-	ns	-

Table 7.3-13 Capture Sensor Interface Characteristics

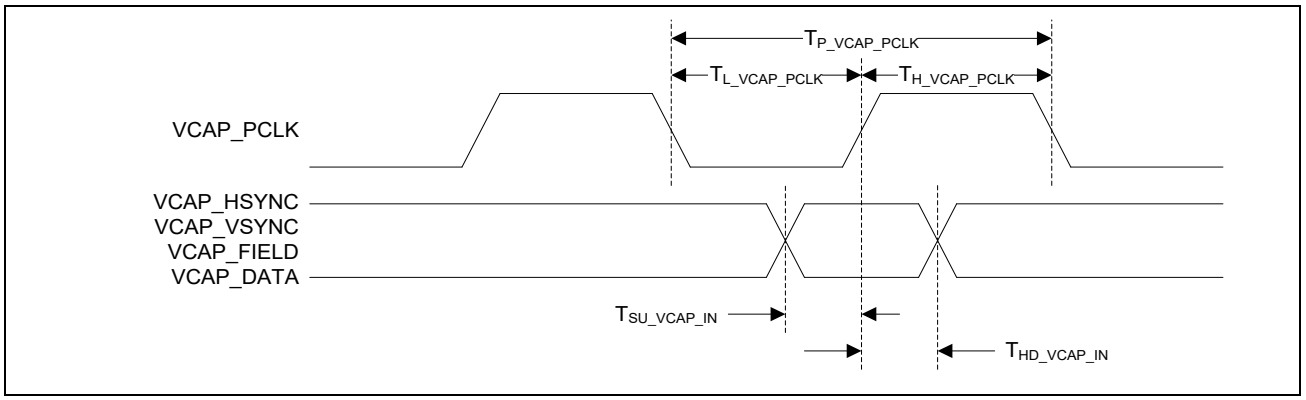


Figure 7.3-17 Capture Sensor Interface Timing Diagram

7.4 Analog Characteristics

7.4.1 12-bit SARADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{REF} is external AV_{ref} pin
INL	Integral Nonlinearity Error	-	-1.2	-	LSB	V_{REF} is external AV_{ref} pin
E_O	Offset Error	-	+3.7	-	LSB	V_{REF} is external AV_{ref} pin
E_G	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V_{REF} is external AV_{ref} pin
E_A	Absolute Error	-	4.2	-	LSB	V_{REF} is external AV_{ref} pin
-	Monotonic	Guaranteed				
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	
T_{ADC}	Conversion Time	-	20		Clock	
F_S	Sample Rate		-	200k	SPS	
AV_{DD33}	Supply Voltage	2.97	3.3	3.63	V	
I_{DDA1}	Supply Current (Avg.)	-	1.2		mA	ADC channel 1 high speed mode
I_{DDA2}	Supply Current (Avg.)	-	1.0		mA	ADC channel 1 low speed mode
I_{DDA3}	Supply Current (Avg.)	-	0.4		mA	
I_{LK}	Leakage Current	-	0.1	-	uA	
AV_{REF}	Reference Voltage	2	-	AV_{DD33}	V	
V_{IN}	Analog Input Voltage	0	-	AV_{ref}	V	
R_{IN}	Analog Input Impedance	-	-	2	MΩ	
C_{IN}	Capacitance	-	25.6		pF	
VBG	Band-gap 2.5V voltage output		2.5		V	VBG no trim for VREF output, the accuracy is 6% typically at 100ppm/℃

7.4.2 Low Voltage Detection (LVD) and Low Voltage Reset (LVR)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
AV_{DD33}	Operation Voltage	2.97	3.3	3.63	V	-
I_{LVDR}	Operating Current		21		uA	-
I_{LK}	Quiescent Current	-	0.1	0.5	uA	LVR_EN (SYS_LVRDCR[0]) = 0, LVD_EN (SYS_LVRDCR[8]) = 0
T_A	Temperature	-40	-	85	°C	-
V_{TH_LVD}	LVD Threshold Voltage	2.295	2.55	2.805	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		2.475	2.75	3.025	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{TH_LVR}	LVR Threshold Voltage	2.115	2.35	2.585	V	-
V_{HY_LVD}	LVD Hysteresis	0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{HY_LVR}	LVR Hysteresis	0.045	0.05	0.055	V	-

Note: Guaranteed by characterization results, not tested in production.

7.4.3 3.3V Power-On Reset (POR33)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	°C	-
V_{POR33}	Reset Voltage	-	1.83	-	V	AV_{DD33} rising from 0V to 3.3V
I_{POR33}	Quiescent current	-	5	-	nA	Vin > reset voltage

Note: Guaranteed by characterization results, not tested in production.

7.4.4 1.2V Power-On Reset (POR12)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	85	°C	-
V_{POR12}	Reset Voltage	-	0.76	-	V	V_{DD12} rising from 0V to 1.2V
I_{POR12}	Quiescent current	-	10	-	nA	Vin > reset voltage

Note: Guaranteed by characterization results, not tested in production.

7.4.5 USB 2.0 PHY

7.4.5.1 Low/Full-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OL}	Output Low (Driven)	-	-	0.3	V	1.5K RPU on DP to 3.6v
V_{OH}	Output High (Driven)	2.8	-	-	V	15K RPD on DP, DM to GND
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	$\lvert V_{USB0_DP}–V_{USB0_DM}\rvert$
V_{CM}	Differential Common-Mode Range	0.8	-	2.5	V	
V_{IL}	Single-Ended Input Low	-	-	0.8	V	-
V_{IH}	Single-Ended Input High	2.0	-	-	V	-
R_{PU}	Pull-Up Resistor	1.35	1.5	1.65	kΩ	
R_{PD_DP}	D+ Pull-Down Resistor	13.5	15	16.5	kΩ	
R_{PD_DM}	D- Pull-Down Resistor	13.5	15	16.5	kΩ	
Z_{DRV}	Driver Output Resistance	28	-	44	Ω	Steady state drive[1]
C_{IN}	Transceiver Low-Speed Donwstream Port Capacitance	200		600	pF	Pin to GND
C_{IN}	Transceiver Low-Speed Upstream Port Capacitance	50		150	pF	Pin to GND
C_{IN}	Transceiver Full-Speed Capacitance		50		pF	

Note:

1. Driver output resistance doesn't include series resistor resistance.
2. Guaranteed by characterization results, not tested in production.

7.4.5.2 High-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HSDI}	High Speed Differential Input Signal Level	150	-	-	mV	$\lvert V_{USB0_DP}–V_{USB0_DM}\rvert$
V_{HSQ}	High Speed Squelch Detection Threshold	100	125	150	mV	$\lvert V_{USB0_DP}–V_{USB0_DM}\rvert$
V_{HSCM}	High Speed Common Mode Voltage Range	-50	-	500	mV	
V_{HSOH}	High Speed Data Signaling High	300	400	440	mV	
V_{HSOL}	High Speed Data Signaling Low	-10	0	10	mV	
V_{CHIRPJ}	Chirp J Level	700	-	1100	mV	
V_{CHIRPK}	Chirp K Level	-900	-	-500	mV	
R_{HSDRV}	High Speed Driver Output Resistance	40.5	45	49.5	Ω	

Note: Guaranteed by characterization results, not tested in production.

7.4.5.3 USB Low-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{LRISE}	Rise Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
T_{LFALL}	Fall Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{LCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note: Guaranteed by characterization results, not tested in production.

7.4.5.4 USB Full-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FRISE}	Rise Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FFALL}	Fall Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Note: Guaranteed by characterization results, not tested in production.

7.4.5.5 USB High-Speed Driver AC Electrical Characteristics

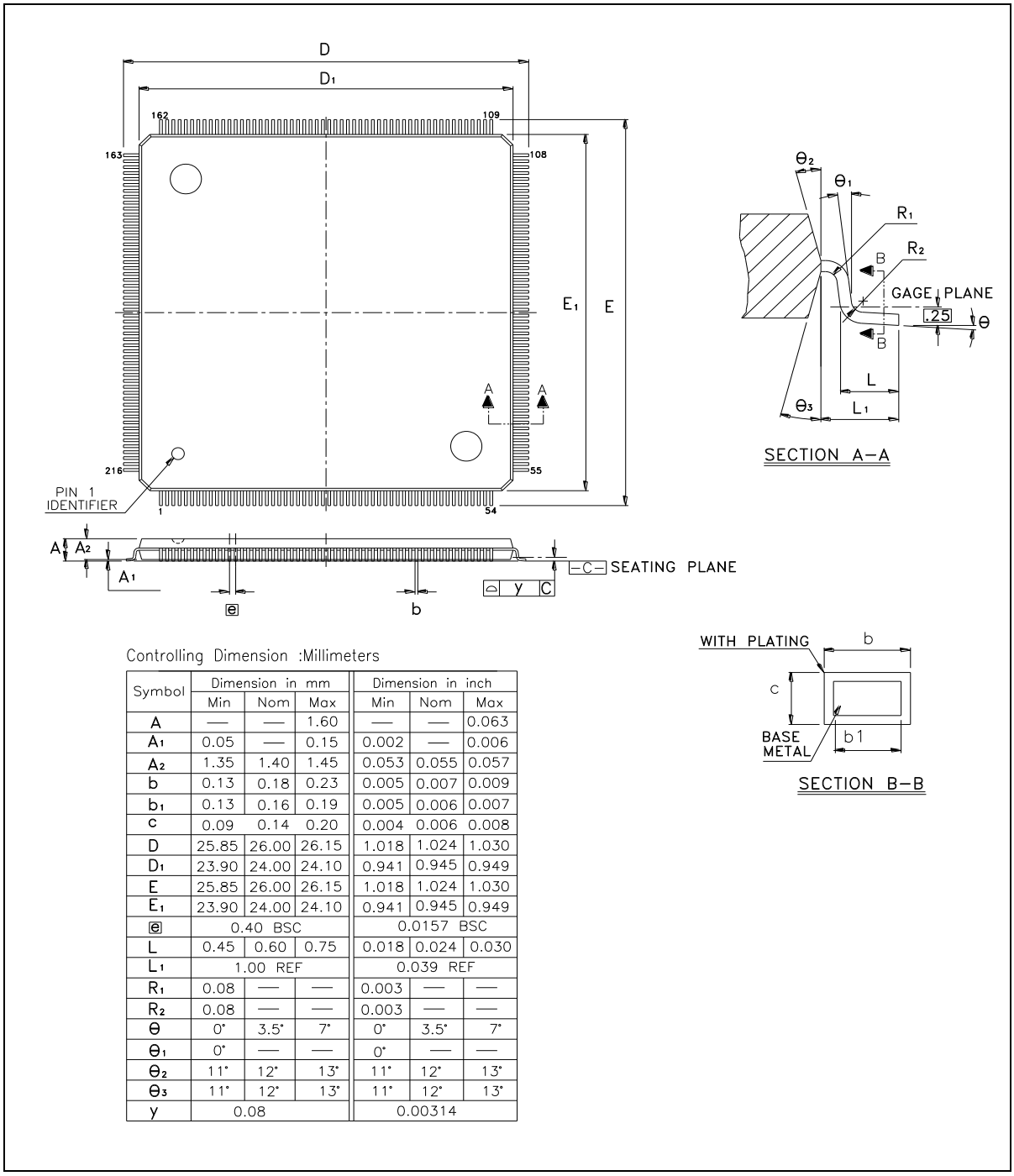
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRISE}	High Speed Driver Rise Time	500	-	900	ps	CL<10pF
V_{HFALL}	High Speed Driver Fall Time	500	-	900	ps	CL<10pF

Note: Guaranteed by characterization results, not tested in production.

8 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

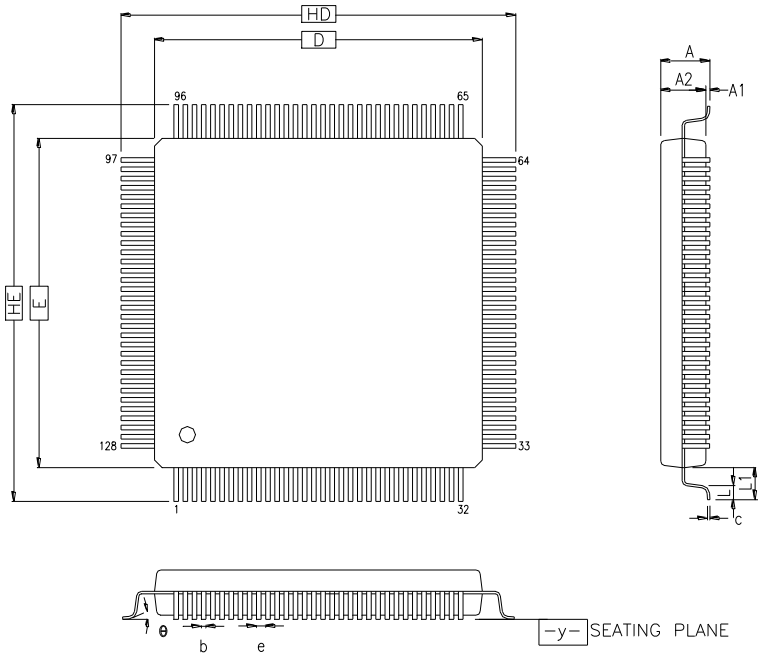
8.1 LQFP216 (24x24x1.4mm footprint 2.0mm)



Controlling Dimension :Millimeters

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	0.14	0.20	0.004	0.006	0.008
D	25.85	26.00	26.15	1.018	1.024	1.030
D1	23.90	24.00	24.10	0.941	0.945	0.949
E	25.85	26.00	26.15	1.018	1.024	1.030
E1	23.90	24.00	24.10	0.941	0.945	0.949
e	0.40 BSC			0.0157 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
y	0.08			0.00314		

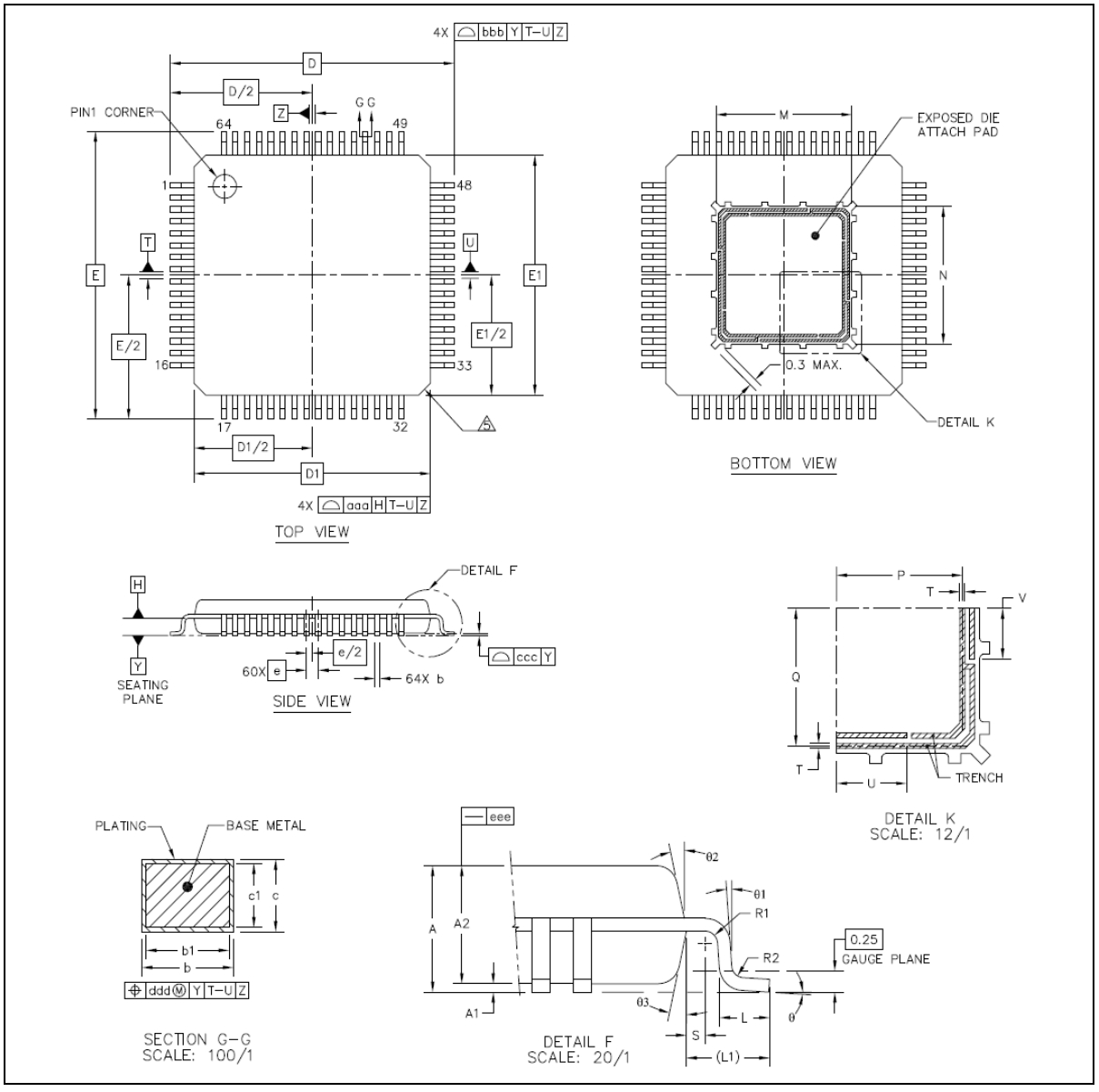
8.2 LQFP128 (14x14x1.4mm footprint 2.0mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

8.3 LQFP64-EP (10x10x1.4mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
	X	D	12 BSC		
	Y	E	12 BSC		
BODY SIZE	X	D1	10 BSC		
	Y	E1	10 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	5.64	5.74	5.84
	Y	N	5.64	5.74	5.84
		P	2.47	2.52	2.57
		Q	2.67	2.72	2.77
		T	0.05	---	0.15
		U	1.35	---	1.45
		V	0.95	---	1.05
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

⚠5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8.4 Thermal Characteristics

8.4.1 Thermal Performance of LQFP under Forced Convection

PKG Type	PCB condition	θ ja (℃/W)			θ jc (℃/W)	θ jb (℃/W)
		0 m/s	1 m/s	2m/s		
LQFP 216L 24mmx24mm	JEDEC 1S1P (2-layers)	42.5	35.9	33.8	9.2	35.16
	JEDEC 2S2P (4-layers)	39.8	33.5	31.7	9	32.08
LQFP64-EP 10x10mm	JEDEC 1S1P (2-layers)	35.9	29	27.2	16.5	22
	JEDEC 2S2P (4-layers)	28.5	22.5	21	14.3	15.56
LQFP 128L 14mmx14mm	JEDEC 1S1P (2-layers)	-	-	-	-	-
	JEDEC 2S2P (4-layers)	38.5	33.8	32	9.9	-

Table 8.4-1 Thermal Performance of LQFP

8.4.2 Thermal Performance Terminology

The major thermal dissipation paths can be illustrated as following

TJ: the maximum junction temperature;

TA: the ambient or environment temperature;

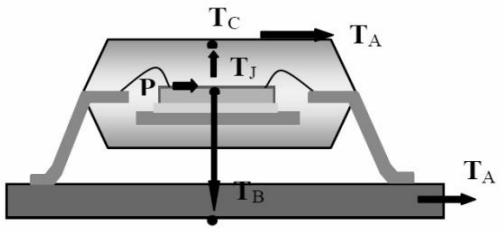
TC: the top center of compound surface temperature;

TB: the bottom center of PCB surface temperature;

P: total input power

1. Junction to ambient thermal resistance, θ_{JA}**, defined as:**

$$\theta_{JA} = \frac{T_J - T_A}{P} \; ; \qquad (1)$$



Thermal Dissipation of LQFP package

Figure 8.4-1 Junction to Ambient Thermal Resistance

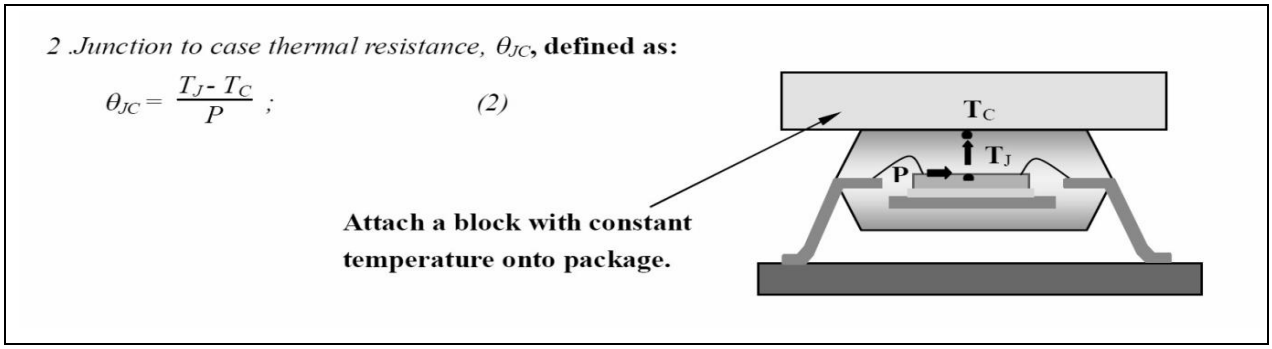


Figure 8.4-2 Junction to Case Thermal Resistance

8.4.3 Simulation Conditions

Input Power	Top Die: 0.6W Bottom die: 0.6 W
Test Board (PCB)	FR4 Cu=1-OZ PCB size = 3”x4.5” PCB thickness= 1.6mm
Control Condition	Air Flow = 0, 1, 2, 3 m/s

Table 8.4-2 Thermal Characteristics Simulation Conditions

8.5 PCB Reflow Profile Suggestion

8.5.1 Reflow Profile Suggestion for NUC980 series

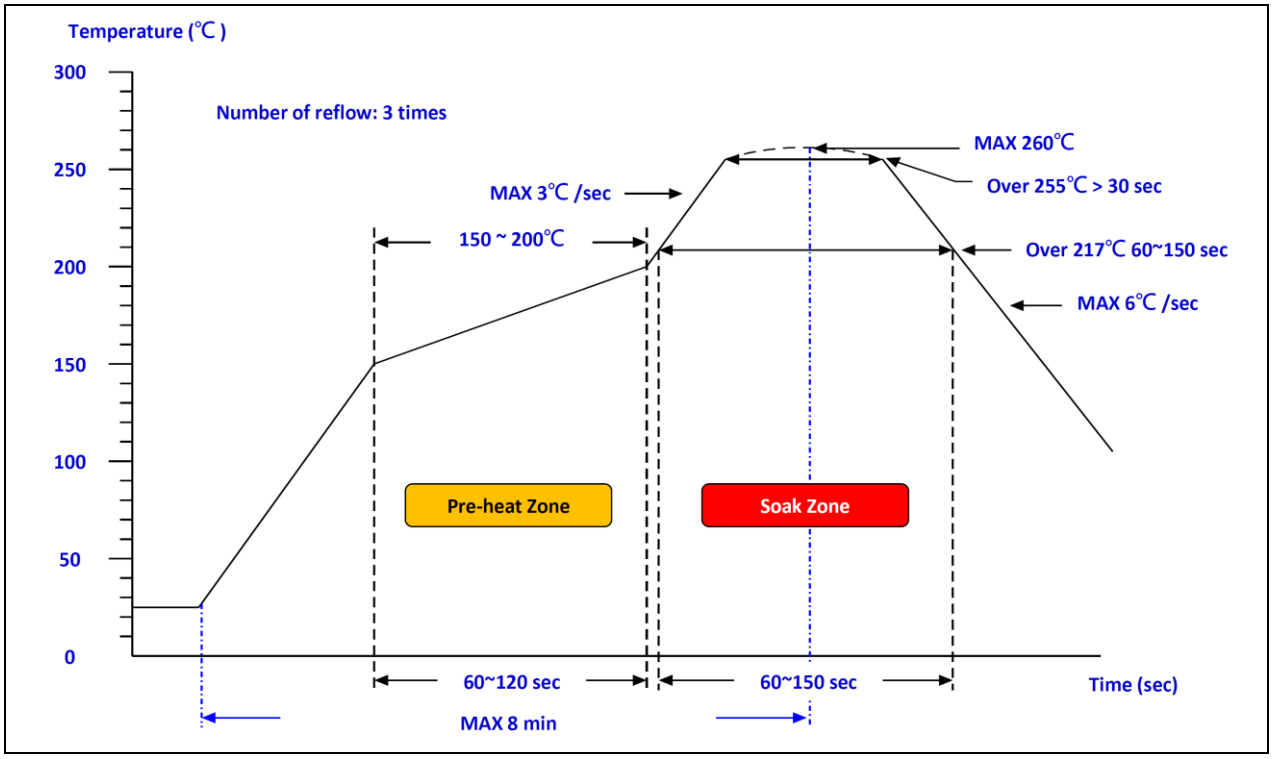


Figure 8.5-1 Profile Suggestion for NUC980 series

8.6 PKG Baking and Vacuumed

The moisture-sensitivity caution label (see Figure 8.6-1) is applied to the outside of the sealed moisture-barrier bag. This label contains detailed information specific to the device (moisture-sensitivity level, shelf life, etc.).

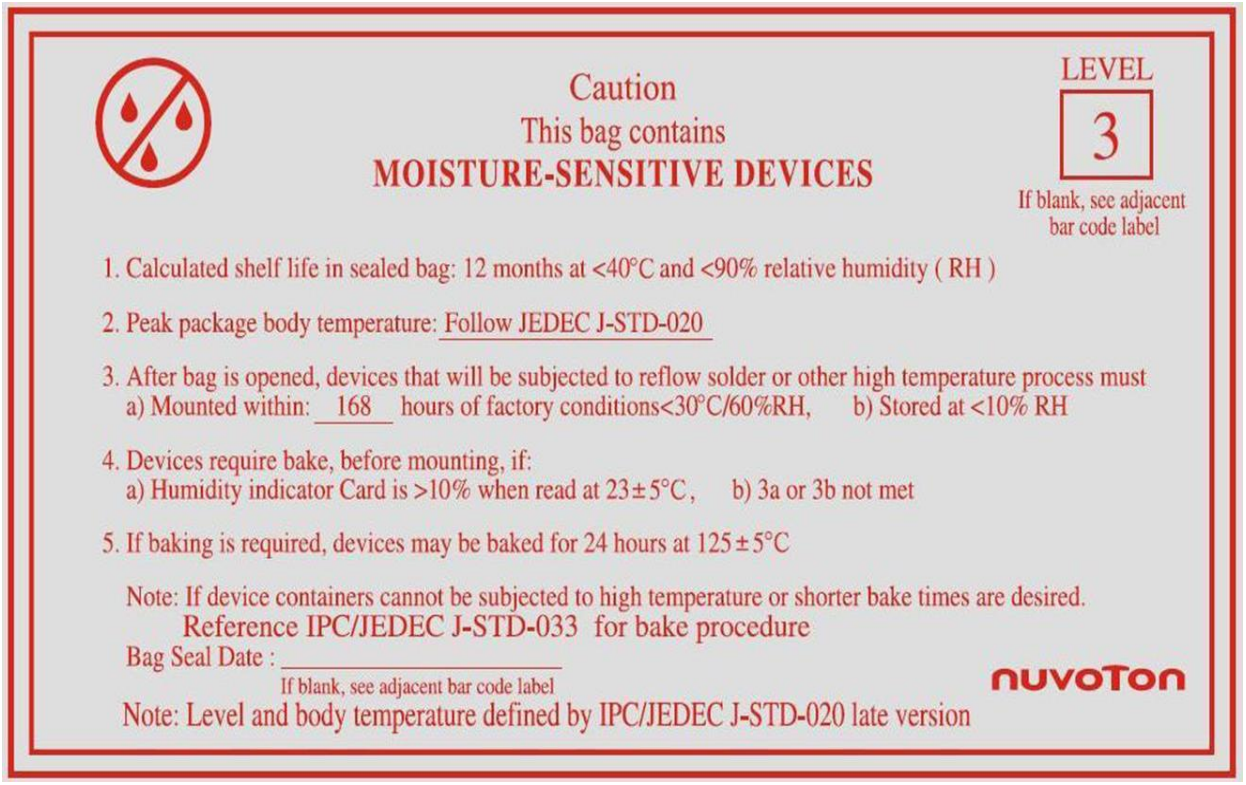


Figure 8.6-1 Cautions for PKG Baking

9 ABBREVIATIONS

Acronym	Description
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
AIC	Advanced Interrupt Controller
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
AMBA	Advanced Microprocessor Bus Architecture
BCH	Bose–Chaudhuri–Hocquenghem
BPS	Bit Per Second
CAN	Controller Area Network
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
DDR	Double Data Rate
DDR2	Double Data Rate 2
DMA	Direct Memory Access
EBI	External Bus Interface
ECC	Elliptic Curve Cryptography
ECC	Error Correcting code
EHCI	Enhance Host Controller Interface
EMAC	Ethernet MAC Controller
eMMC	Embedded Multimedia Card
ETU	Elementary time unit
FIFO	First In, First Out
FIQ	Fast Interrupt
FMI	Flash Memory Interface
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HMAC	keyed-Hash Message Authentication Code
HSUSBD	High Speed USB 2.0 Device Controller
HXT	12 MHz External High Speed Crystal Oscillator
I^2C	Inter-Integrated Circuit
I^2S	Inter-IC Sound
LIN	Local Interconnect Network
LPDDR	Low Power DDR
LSB	Least Significant Bit

LVD	Low Voltage Detect
LVR	Low Voltage Reset
LXT	32.748 kHz External Low Speed Crystal Oscillator
MLC	Multi-Level Cell NAND flash
MMU	Memory Management Unit
MSB	Most Significant Bit
OHCI	Open Host Controller Interface
PCLK	The Clock of Advanced Peripheral Bus
PCM	Pulse Code Modulation
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PMBus	Power Management Bus
PRNG	Pseudo Random Number Generator
PWM	Pulse Width Modulation
RMII	Reduced Media Independent Interface
RSA	Rivest、Shamir and Adleman Cryptography
RTC	Real Time Clock
SC	Smart Card
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIC	SDRAM Interface Controller
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SHA	Secure Hash Algorithm
SLC	Single Level Cell NAND flash
SMBus	System Management Bus
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 9-1 List of Abbreviations

10 REVISION HISTORY

Date	Revision	Description
2019. 01. 28	1.00	• Initial version.
2019. 08. 14	1.10	• Revised content and added NUC980DF71Y, NUC980DF61YC, NUC980DR61YC and NUC980DR41YC to section 3.2.
2019. 10. 02	1.11	• Added NUC980DK71Y and NUC980DK71YC to section 3.2.
2020. 11. 13	1.20	• Updated part number selection guide in section 3.2.
2021. 02. 09	1.21	• Updated SDRAM type in section 3.2 and section 3.3.
2021. 04. 09	1.22	• Added USB1.1 Host Lite function to all NUC980 series and updated part number selection guide in section 3.2.
2021. 05. 13	1.23	• Updated NUC980Dx63x series part numbers in section 3.2
2021. 09. 01	1.24	• Updated NUC980Dx63x series part numbers in section 3.2
2021. 11. 04	1.25	• Revised part number selection guide in section 3.2
2021. 11. 18	1.26	• Revised reflow profile in section 8.5
2023. 03. 23	1.27	• Added GPIO V_{OH} and V_{OL} parameters in section 7.2.2
2023. 08. 09	1.28	• Revised part number selection guide in section 3.2 and chapter 2 • Added “Package is Halogen-free, RoHS-compliant and TSCA-compliant.” in chapter 3 and 8
2025. 12.24	1.29	• Modified Pin Diagram in Figure 4.1-3 • Removed ADC from the supported trigger targets for time-out and capture interrupts in section 6.9.2

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