Smart Buzzer™

NSP2340BA24E Series

Data Sheet

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1. General Description

NSP2340BA24E Smart Buzzer™ series are advanced Voice IC with embedded Flash and Buzzer Driver to implement Voice Assistance on Piezo Buzzer applications. NSP2340BA24E series provide hardware I2C, UART and firmware Two-Wire interface to communicate with host MCU, and support In-System-Program (ISP) to update content with high data transition rate. NSP2340BA24E series contain an innovative piezo buzzer driver with voltage booster and class AB amplifier. The voltage booster can reach up to 24V, capable of driving buzzer playback voice or sound effects directly.
The NSP2340BA24E series include 3 part numbers with different durations, shown as below selection guide:

Part Number	NSP Duration	NM4 Duration		Package	Updated	Operating Voltage(V)	Operating Temperature	Boost Output Voltage	MCU Interface			
	16KHz	16kHz	24kHz						1-Wire	2-Wire	UART	I²C
NSP2080BA24E	72	18	16	TSSOP28	V	2.0 to 5.5	-40 to 85˚C	Piezo Buzzer V_{BUZ}: 10, 12, 18, 24V	-	V	V	V
NSP2170BA24E	133	33	29									
NSP2340BA24E	315	78	69									

2. Features

- Operating voltage: 2.0~5.5V
- Operating temperature: -40˚C ~ 85˚C
- Interface with MCU: UART, I2C (Slave), Two-Wire
- I2C Slave Address: can be assigned by 1 to 127 flexibly
- Provide ISP (In System Program) to update content from Host MCU
- Low Voltage Reset (LVR)
- Low Standby current: ≤ 3uA
- Adjustable gain by external R
- Automatic shutdown and wake-up
- Over temperature protection
- Over current protection
- Booster voltage output: 10V, 12V, 18V, 24V
- Package form: TSSOP28
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

3. PIN Description

NSP2080BA24E / NSP2170BA24E / NSP2340BA24E

PIN No.	Name	I/O	Description
28 27	BP00 BP01	I/O	● General input / output pins ● BP00, BP01 share with ICPCLK and ICPDATA ● Each pin can be set as I2C, UART, Two-Wire, interface
6	VDD	P	Positive power supply
5	REG	P	Internal regulator, 0.1uF capacitor is needed
4	VSS	P	Negative power supply
3	/RESET	I	IC reset input, low active
14	SW	P	Switch pin of voltage booster
13	VBUZ	P	Output of voltage booster
11	LDO5V	P	5V LDO output, 10uF capacitor is needed
8	VDDB	P	Positive power supply for buzzer driver
10, 15	VSSB x 2	P	Negative power supply for buzzer driver
16	BUZN	O	Buzzer negative signal amplified output
17	BUZP	O	Buzzer positive signal amplified output
18	RGAIN	O	Gain control pin
1	BP03	I/O	General input / output pin
2	BP04	I/O	General input / output pin
24	BP02	I/O	General input / output pin
25	BP07	I/O	General input / output pin
19~23, 26	NC	-	No connection pins
12	BOOT	O	Bootstrap pin of voltage booster, 0.1uF capacitor is needed.
7 9	SEL0 SEL1	I	Pin configuration for booster output options SEL0 / SEL1 / VBUZ 0 / 0 / 10V option 0 / 1 / 12V option 1 / 0 / 18V option 1 / 1 / 24V option

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rated Value	Unit
Input Voltage	VIN	All Inputs	VSS -0.3 to VDD +0.3	V
Storage Temp.	TSTG	-	-55 to +150	°C
Operating Temp.	TOPR	-	-40 to +85	°C

Noted: Exposure to conditions beyond those listed under the absolute Maximum ratings table may adversely affect the life and reliability of the device.

4.2 D.C. Characteristics

($V_{DD} - V_{SS}$ = 4.5V, L = 4.7uH, TA = 25° C, No Load unless otherwise specified)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		2.0	-	5.5	V
Operating Current	I_{OP1}	No load	-	20	-	mA
Standby Current (STOP)	I_{DD1}	No load	-	1.8	3	μA
Input Low Voltage	V_{IL}	All input pins	V_{SS}	-	0.3 V_{DD}	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Pull High resistor BP0x	RPH	VDD = 4.5V	105K	150K	195K	Ω
Booster Output Voltage	VBUZ	VBUZ = 10V option, VDD=2.0, No load	9.5	10	10.5	V
		VBUZ = 12V option, VDD=2.0, No load	11.4	12	12.6	V
		VBUZ = 18V option, VDD=2.0, No load	17.1	18	18.9	V
		VBUZ = 24V option, VDD=2.0, No load	22.8	24	25.2	V
Booster Output Driving Current	IBODC	VDD = 3.3V, VBUZ = 10V option, VBUZ > 0.9 * 10V	30			mA
		VDD = 3.3V, VBUZ = 12V option, VBUZ > 0.9 * 12V	30			mA
		VDD = 3.3V, VBUZ = 18V option, VBUZ > 0.9 * 18V	30			mA
		VDD = 3.3V, VBUZ = 24V option, VBUZ > 0.9 * 24V	30			mA

Output Current BP0x	I_{OL}	V_{DD} = 3V, Vout = 0.4V	8	-	-	mA
	I_{OH}	V_{DD} = 3V, Vout = 2.6V	-4	-	-	mA

4.3 A.C. Characteristics

(VDD = 4.5V, TA = 25°C, No Load unless otherwise specified)

Parameter	Sym	Conditions	Min	Typ	Max	Unit
Frequency Deviation by Voltage Drop	ΔF/F	(Fmax – Fmin)/Fmin @VDD: 2.0 ~ 5.5V	-	-	3	%

4.4 Rgain Resistor Selection Guide

The gain control resistor (Rgain) value should be selected based on the booster output voltage (VBUZ) and operating voltage (VDD) according to the following formula:

Rgain Calculation Formula:

$$R_{gain}(k\Omega) = \frac{V_{BUZ}}{V_{DD}} \times 25$$

Where:

- V_{BUZ}: Booster output voltage (10V, 12V, 18V, or 24V)
- V_{DD}: Operating voltage (2.0V ~ 5.5V)
- R_{gain}: Gain control resistor value in kΩ

Recommended Rgain Values for Common Operating Voltages:

The operating voltages of 3.3V and 5.0V are the most commonly used in typical applications. The recommended Rgain values are listed below:

Rgain Selection for VDD = 5.0V

VBUZ (Booster Output)	Rgain (kΩ)
10V	50
12V	60
18V	90
24V	120

Rgain Selection for VDD = 3.3V

VBUZ (Booster Output)	Rgain (kΩ)
10V	75
12V	90
18V	136
24V	181

Note: For other operating voltages within the range of 2.0V ~ 5.5V, please calculate the Rgain value using the formula provided above.

5. MCU Interface: I2C

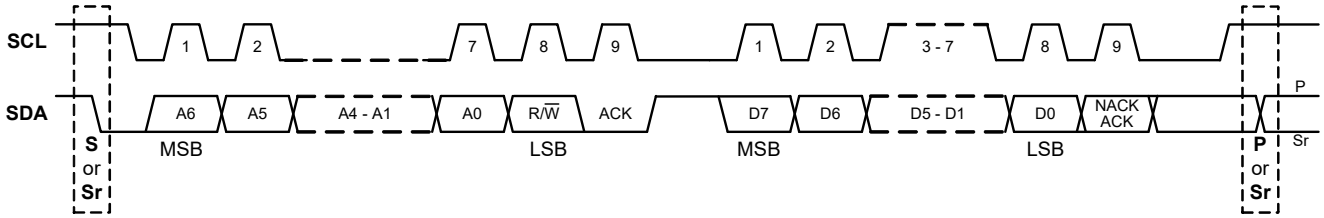
5.1 Interface

The I²C interface consists of two wires, SCL and SDA.

- SCL is connected to BP00.
- SDA is connected to BP01.

5.2 I2C Protocol

The NSP2340BA24E series support I²C serial interface to communicate with the microcontroller host. The relationship of I²C protocol is shown as below.



The I²C protocol is as follows, with four parts:

- START or Repeated START signal

When the bus is free/idle, meaning no master device is engaging the bus (both SCL and SDA lines are high), a master can initiate a transfer by sending a START signal. A START signal, usually referred to as the S-bit, is defined as a HIGH to LOW transition on the SDA line while SCL is HIGH. The START signal denotes the beginning of a new data transfer.

A Repeated START (Sr) is a START signal without first generating a STOP signal. The master uses this method to communicate with another slave or the same slave in a different transfer direction (e.g. from writing to a device to reading from a device) without releasing the bus.

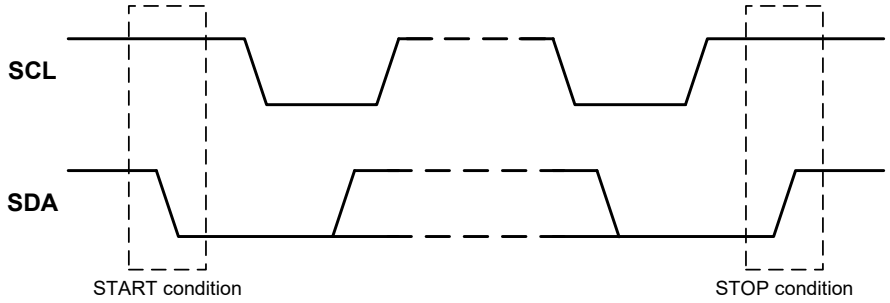


Figure 5.2-1: START and STOP condition

- Slave Address Transfer

The first byte of data transferred by the master immediately after the START signal is the slave address. This is a 7-bits calling address followed by a RW bit. The RW bit signals the slave the data transfer direction. No two slaves in the system can have the same address. Only the slave with an address that matches the one transmitted by the master will respond by returning an acknowledge bit by pulling the SDA low at the 9th SCL clock cycle.

- Data Transfer

Once successful slave addressing has been achieved, the data transfer can proceed on a byte-by-byte basis in the direction specified by the RW bit sent by the master. Each transferred byte is followed by an acknowledge bit on the 9th SCL clock cycle. If the slave signals a Not Acknowledge (NACK), the master can generate a STOP signal to abort the data transfer or generate a Repeated START signal and start a new transfer cycle.

If the master, as the receiving device, does Not Acknowledge (NACK) the slave, the slave releases the SDA line for the master to generate a STOP or Repeated START signal.

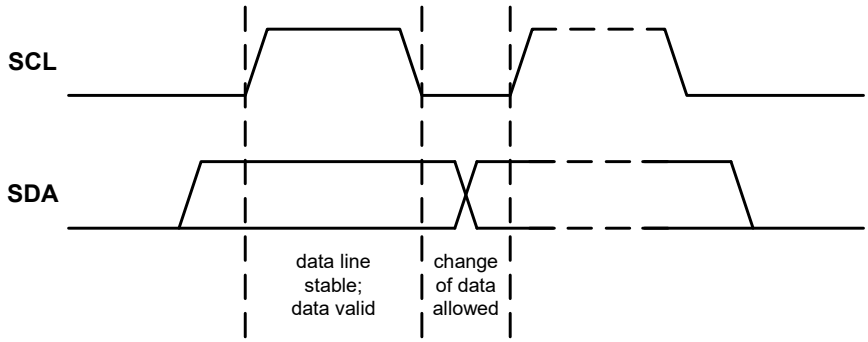


Figure 5.2-2: Bit Transfer on the I^{2}C bus

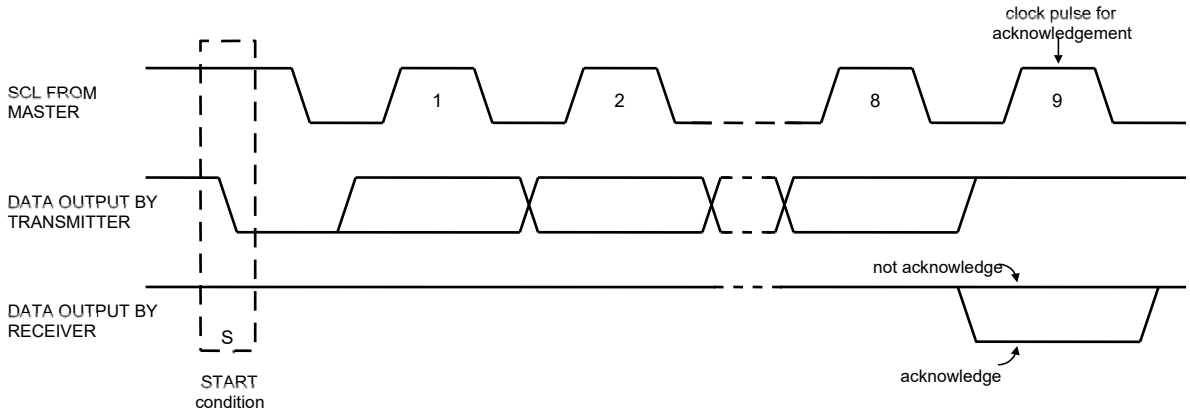


Figure 5.2-3: Acknowledge on the I^{2}C bus

- Stop signal (STOP)

The master can terminate the communication by generating a STOP signal. A STOP signal, usually referred to as the P-bit, is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH.

5.3 Timing

The timing parameters listed in below Tables and Charts are characterized for I2C Standard-mode operation. It is recommended that the maximum SCL clock frequency does not exceed 100 KHz to ensure bus stability and compliance with the specified timing constraints.

Symbol	Parameter	Min	Max	Unit
f_{SCL}	SCL clock frequency	-	100	KHz
t_{LOW}	SCL low period	4.7	-	uS
t_{HIGH}	SCL high period	4	-	uS
$t_{SU;STA}$	Repeated START condition setup time	4.7	-	uS
$t_{HD;STA}$	START condition hold time	4	-	uS
$t_{SU;STO}$	STOP condition setup time	4	-	uS
t_{BUF}	Bus free time	4.7	-	uS
$t_{SU;DAT}$	Data setup time	250	-	nS
$t_{HD;DAT}$	Data hold time	0	3.45	uS
t_r	SCL/SDA rise time	-	1,000	nS
t_f	SCL/SDA fall time	-	300	nS

Table 5.3-1: I2C Timing Spec.

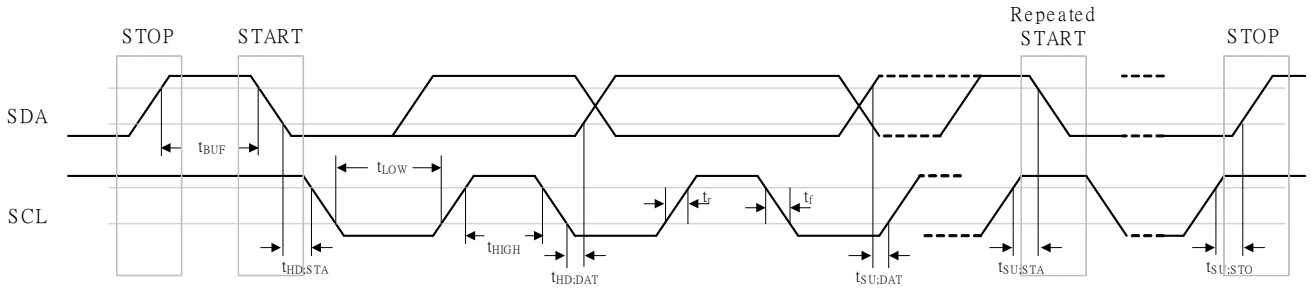


Figure 5.3-1: SCL (Serial Clock) and SDA (Serial Data I/O) Timing

Symbol	Parameter	Min	Typ	Max	Units
Twait1	Wait Time after PLAY Command		40		μs
Twait2	Wait Time after PLAY and STOP command		40		μs
Twait3	Wait Time after Other Command(Except STOP/ISP Command)		40		μs

Table 5.3-2: Twait Timing Parameter

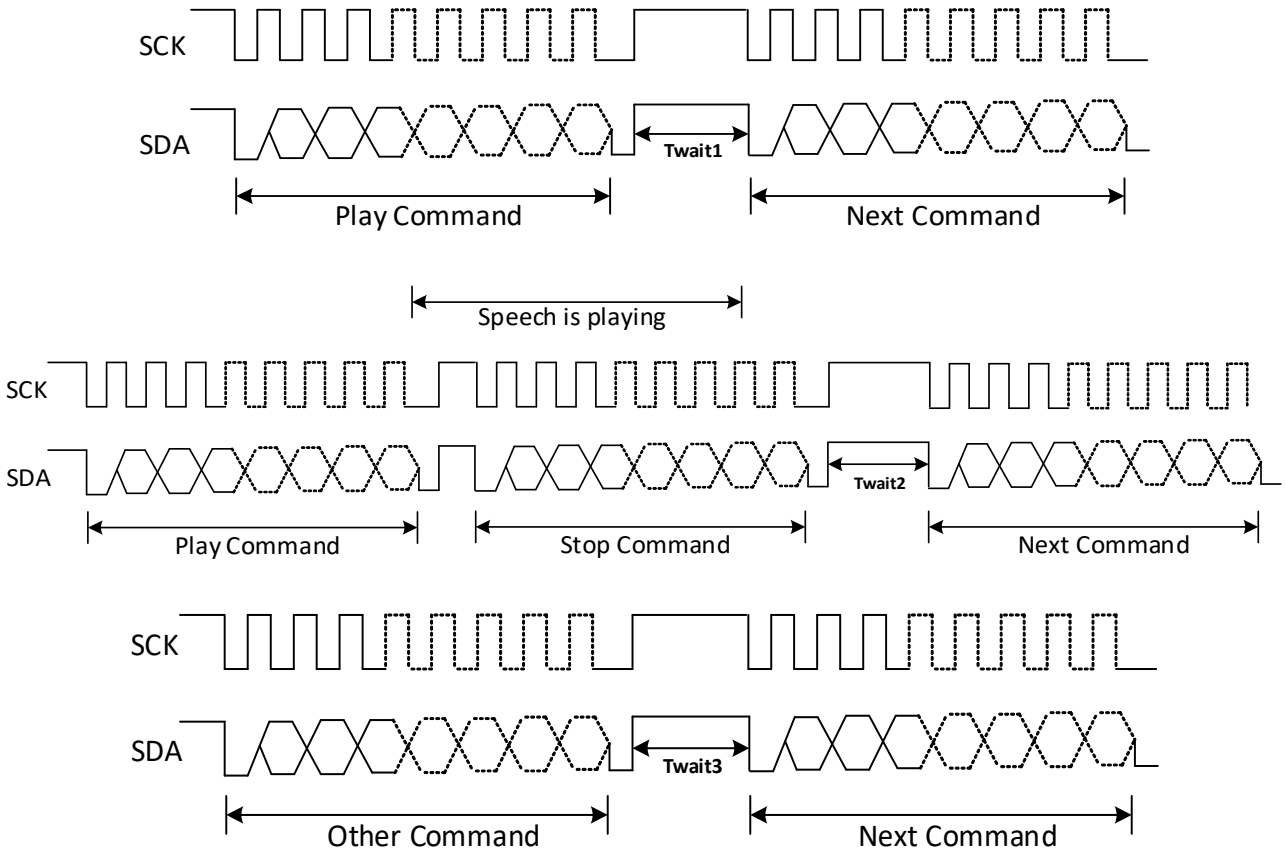


Figure 5.3-2: Twait Timing

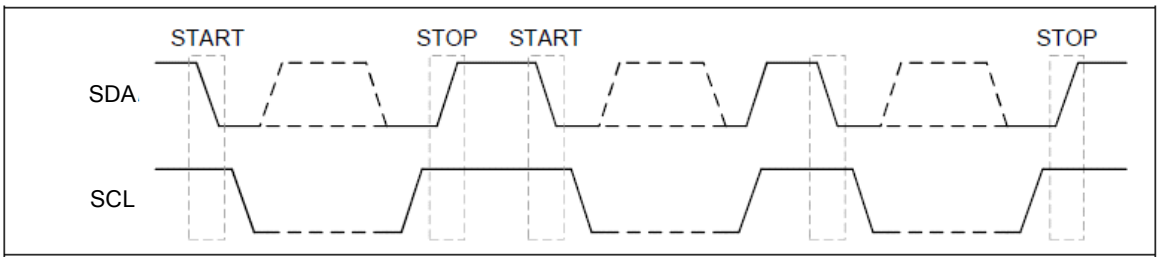


Figure 5.3-3: START and STOP Definition

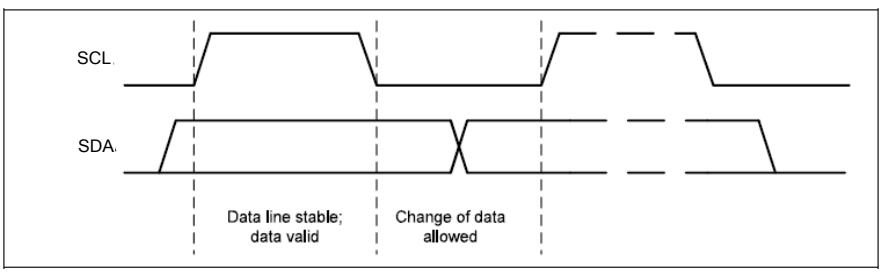
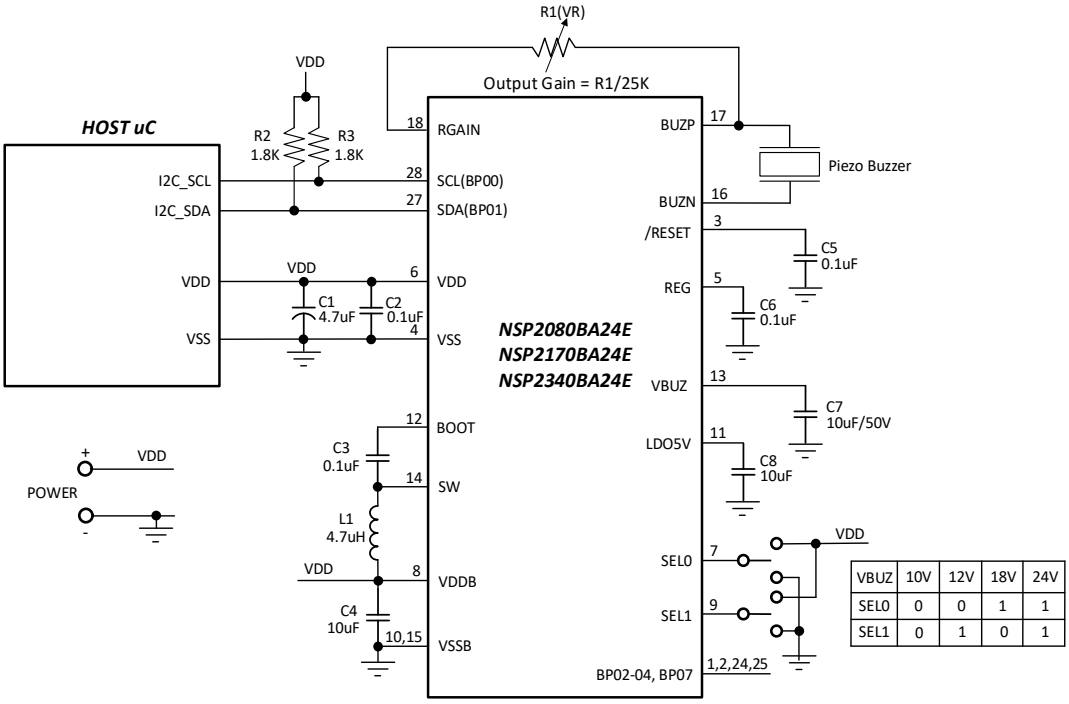


Figure 5.3-4: Data Validity

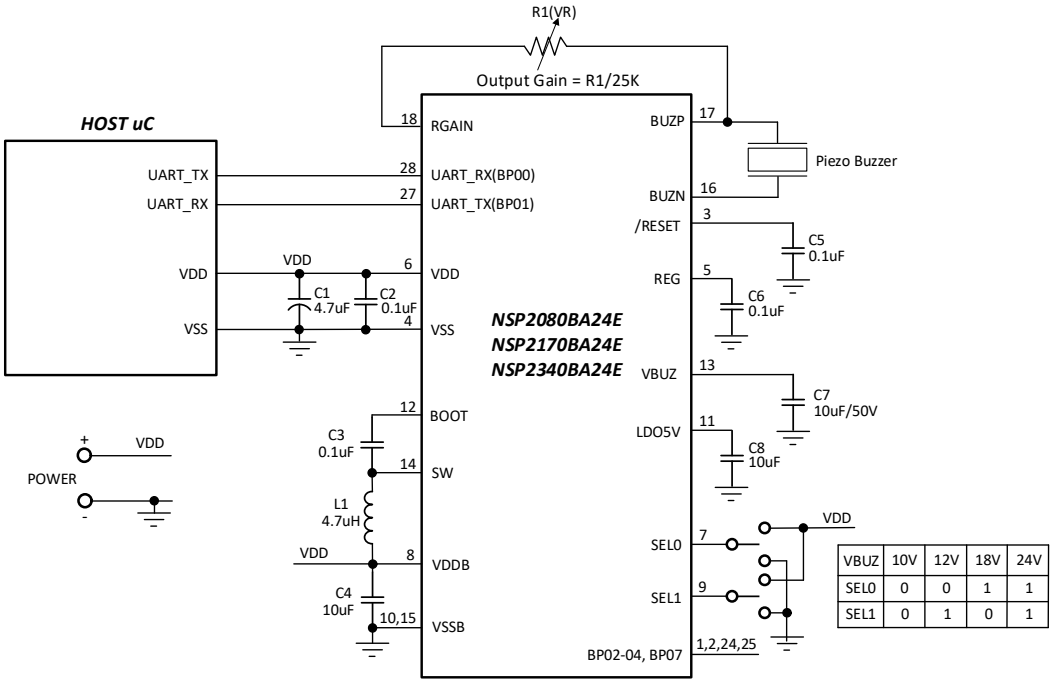
6. Typical Application Circuit

6.1 Connect to Host uC by I2C Interface



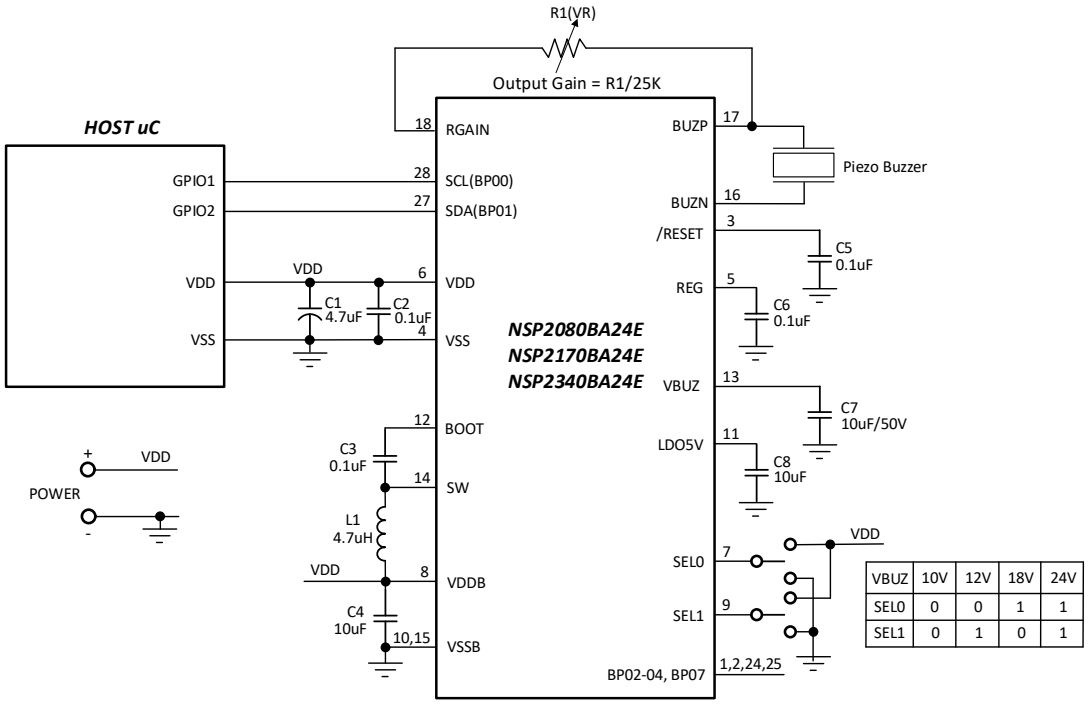
VBUZ	10V	12V	18V	24V
SEL0	0	0	1	1
SEL1	0	1	0	1

6.2 Connect to Host uC by UART Interface

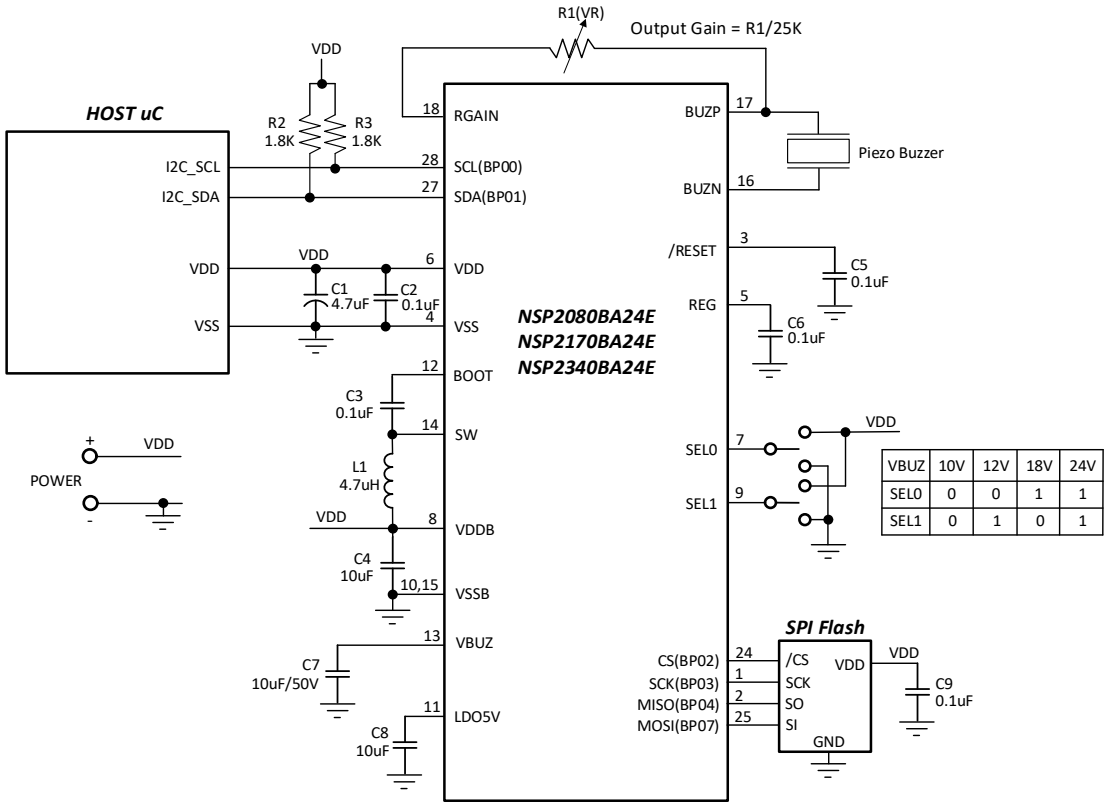


VBUZ	10V	12V	18V	24V
SEL0	0	0	1	1
SEL1	0	1	0	1

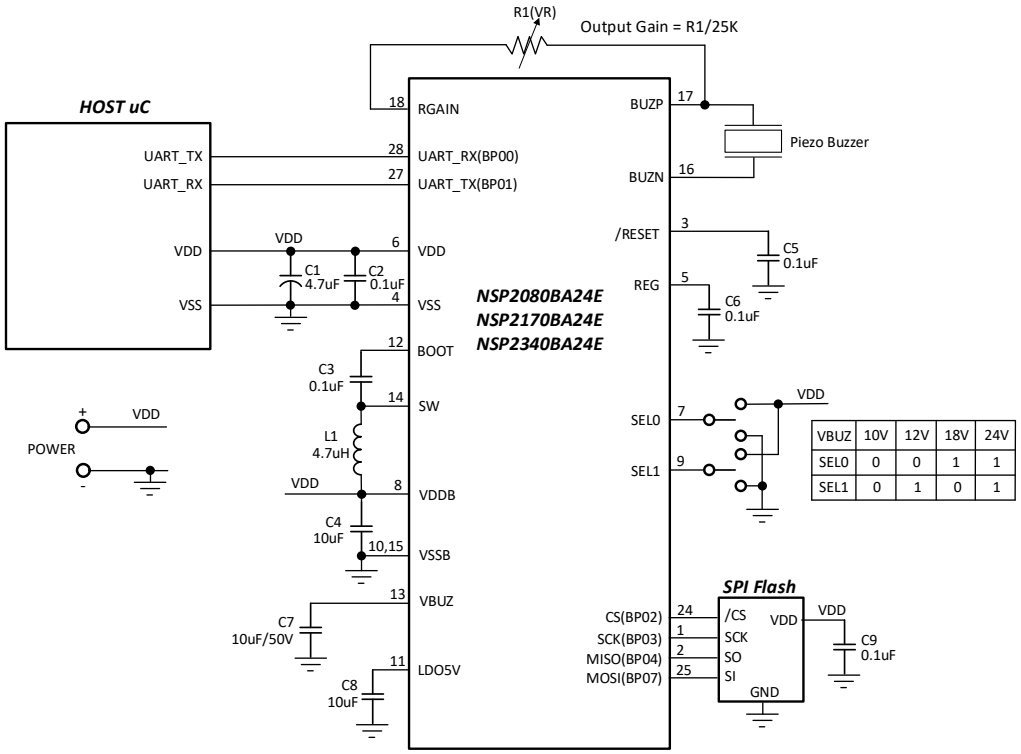
6.3 Connect to HOST uC by Two-Wire Interface



6.4 Connect to HOST uC by I2C Interface and apply with SPI Flash

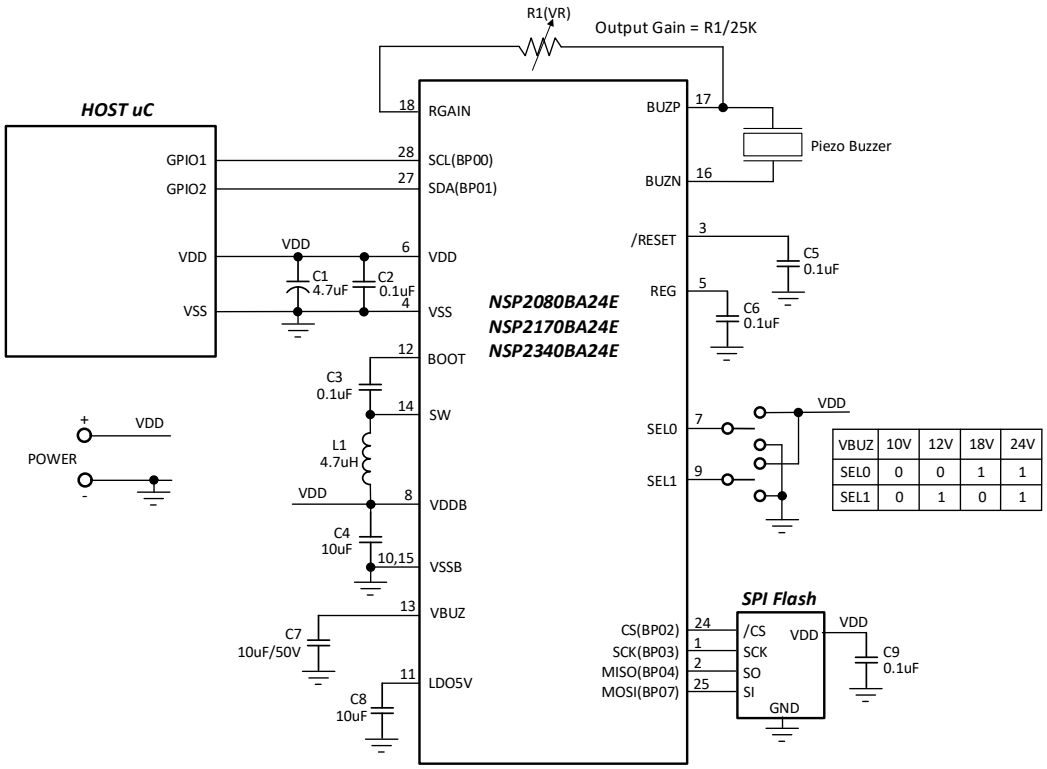


6.5 Connect to HOST uC by UART Interface and apply with SPI Flash



VBUZ	10V	12V	18V	24V
SEL0	0	0	1	1
SEL1	0	1	0	1

6.6 Connect to HOST uC by Two-Wire Interface and apply with SPI Flash



VBUZ	10V	12V	18V	24V
SEL0	0	0	1	1
SEL1	0	1	0	1

6.7 PCB Layout Notice

- **The C1、 C2、C4 and C5 connected to chip as near as possible.**

6.8 MCU Output Notice

- **Host MCU cannot output high level on the interface pins before chip is powered on.**

7. Package Information

7.1 Pin Assignment

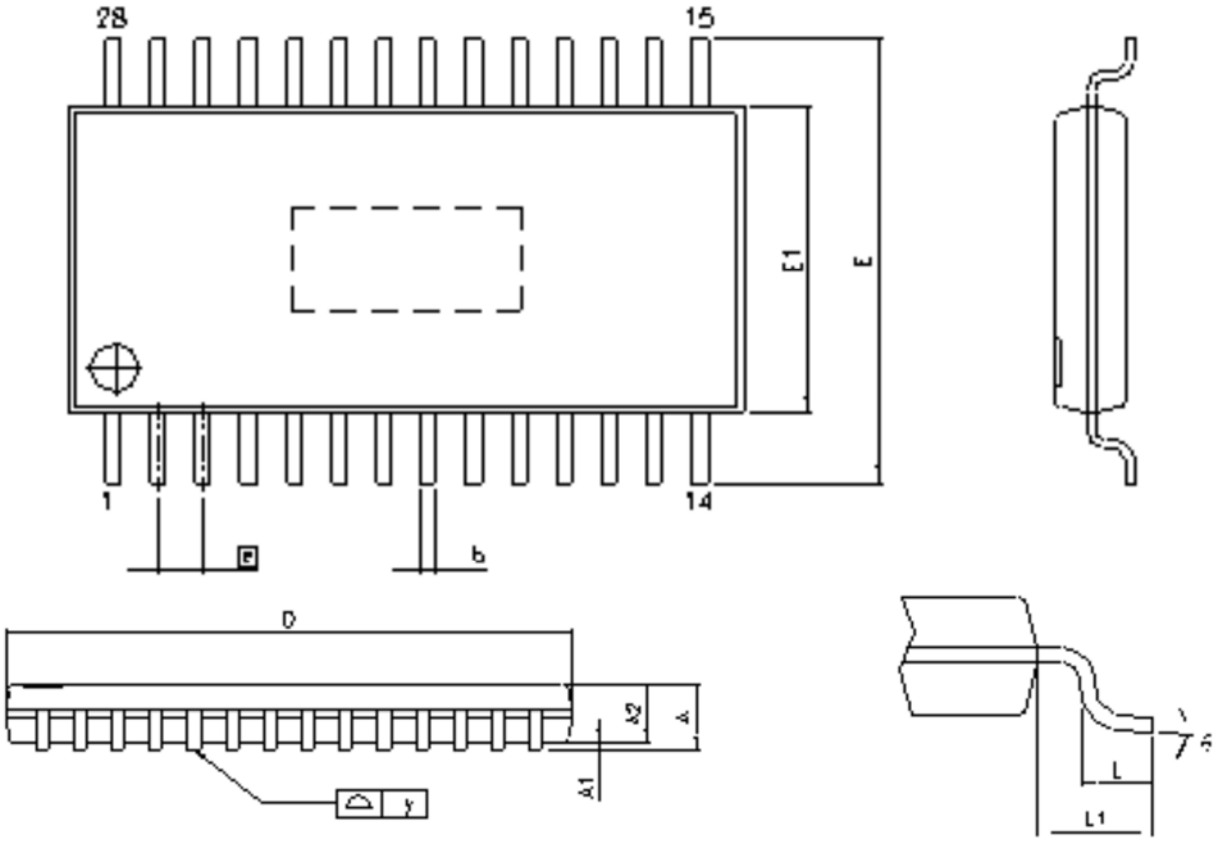
NSP2080BA24E, NSP2170BA24E, NSP2340BA24E

TSSOP28

BP03	1	28	BP00
BP04	2	27	BP01
/RESET	3	26	NC
VSS	4	25	BP07
REG	5	24	BP02
VDD	6	23	NC
SEL0	7	22	NC
VDDB	8	21	NC
SEL1	9	20	NC
VSSB	10	19	NC
LDO5V	11	18	RGAIN
BOOT	12	17	BUZP
VBUZ	13	16	BUZN
SW	14	15	VSSB

7.2 Package Dimension

TSSOP28 (4.4 x 9.7 mm^2)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E1	4.30	4.40	4.50	0.1692	0.1732	0.1771
E	6.40 BSC			0.2519 BSC		
D	9.60	9.70	9.80	0.3779	0.3818	0.3858
L	0.45	0.60	0.75	0.0177	0.0238	0.0295
L1	1.00 REF			0.0393 REF		
b	0.19	-	0.30	0.0074	-	0.0118
e	0.65 BSC			0.0255 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.05 BASIC			0.000196 BASIC		

8. Ordering Information

Part No.	Shape	Type	Remark
NSP2080BA24E NSP2170BA24E NSP2340BA24E	E: Tube T: Tape & Reel	Package: TSSOP28	Blank

9. Revision History

Version	Date	Substantial Changes	Page
1.0	Dec. 2025	First Release	All
1.1	Apr. 2026	Add MCU I2C Interface Protocol	7~11

Important Notice

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