NAU8502
24-bit Stereo Audio ADC with Differential Microphone Inputs

1. GENERAL DESCRIPTION

The NAU8502 is a low power, high quality audio input system for portable applications. In addition to precision 24-bit stereo ADCs, this device integrates a broad range of additional functions to simplify implementation of complete audio systems. The NAU8502 includes low-noise stereo differential high gain microphone inputs with wide range programmable amplifiers, separate line inputs, and an analog bypass/side tone line level stereo output.

Advanced on-chip digital signal processing includes a limiter/ALC (Automatic Level Control), 5-band equalizer, notch filter, and a high-pass filter for speech optimization and wind noise reduction. The digital interface can operate as either a master or a slave. Additionally, an internal Fractional-N PLL is available to accurately generate any audio sample rate clock for the ADCs derived using any available system clock from 8MHz through 33MHz.

The NAU8502 operates with analog supply voltages from 2.7V ~ 3.6V, while the digital core can operate as low as 1.71V to conserve power. Internal control registers enable flexible power conserving modes, shutting down or reducing power in sub-sections of the chip under software control.

The NAU8502 is specified for operation from -40°C ~ +85°C, and is available with full automotive AEC-Q100 and TS16949 compliant device is available upon request.

2. FEATURES

24-bit signal processing linear Audio ADC
- ADC: 90dB SNR and -80dB THD ("A" weighted)
- Supports any sample rates from 8KHz - 48kHz

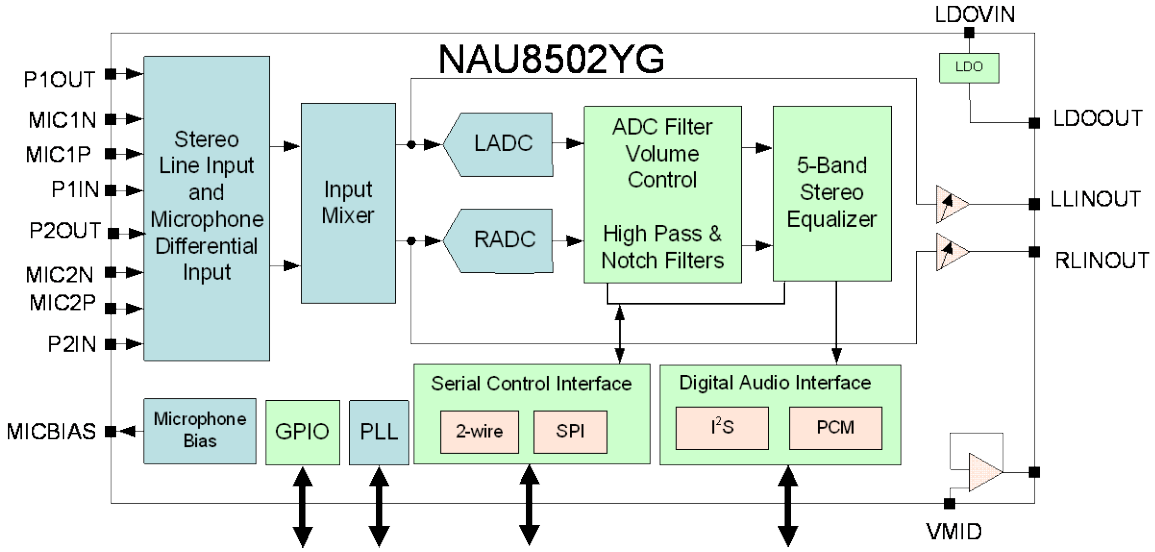
Analog I/O
- Very wide range programmable input amplifier
- Stereo line inputs with gain options and mixing
- Stereo differential input microphone amplifiers

Interfaces
- Standard audio interfaces: PCM and I^2S
- Serial control interfaces with read/write capability)

New Features
- Passive LINE OUT
- On-Chip LDO
- On-chip high resolution Fractional-N PLL

Additional features
- 5-band Graphic Equalizer
- Automatic level control / limiter
- Programmable Notch Filter
- High Pass Filter/ Wind Noise Reduction
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications
- Audio Recording Devices
- Security Systems
- Video and Still Cameras
- Enhanced Audio Inputs for SOC products
- Audio Input Accessory Products
- Gaming Systems



3. PIN CONFIGURATION

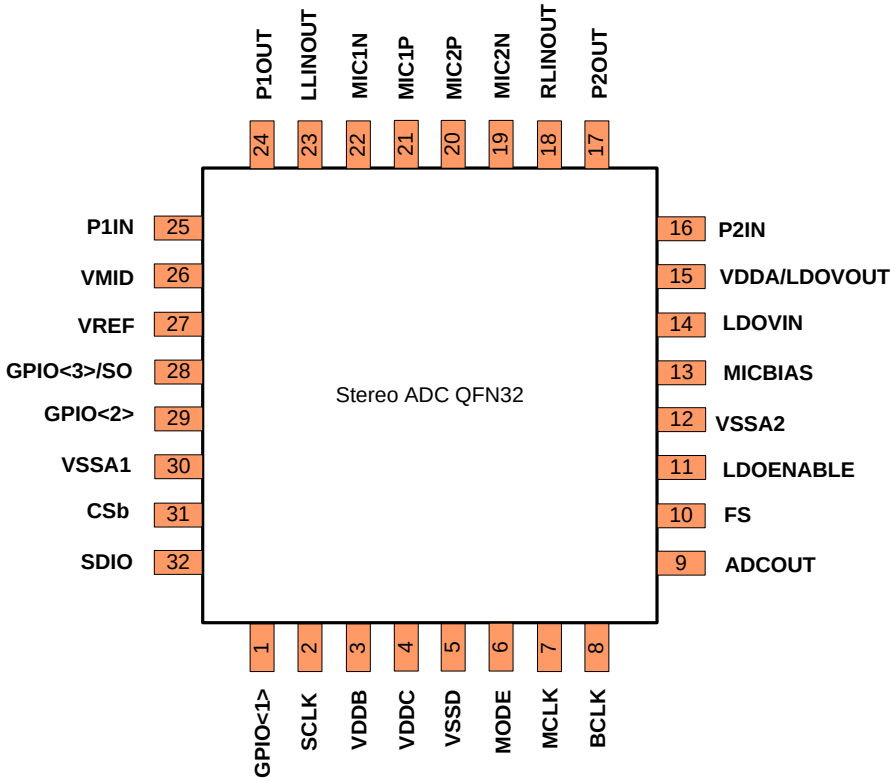


Figure 1: 32-Pin QFN Package

4. PIN DESCRIPTION

Pin Name	Pin No	Functionality	Pin Type
GPIO<1>	1	General Purpose IO Number One	I/O
SCLK	2	SPI or 2-Wire Serial Clock	I
VDDB	3	Digital Supply Buffer	PI
VDDC	4	Digital Supply Core	PI
VSSD	5	Digital Ground	PI
MODE	6	Interface Select (2-Wire:low or SPI:high)	I
MCLK	7	Master Clock	I
BCLK	8	Bit Clock	I/O
ADCOUT	9	Digital Audio Data Output	O
FS	10	Frame Sync	I/O
LDOENABLE	11	Enable Internal LDO, 5V Tolerant	I
VSSA2	12	Analog Ground	PI
MICBIAS	13	Microphone Bias	AO
LDOVIN	14	LDO Input Voltage (4.5V ~ 5.5V)	PI
VDDA /LDOVOUT	15	Analog Supply, LDOVOUT when LDOENABLE > 1.8V	PI /PO
P2IN	16	Right Channel Stage 2 Input	AI
P2OUT	17	Right Channel Stage 1 Output	AO
RLINOUT	18	Right Channel High Impedance Output	AO
MIC2N	19	Right Channel Microphone Negative Input	AI
MIC2P	20	Right Channel Microphone Positive Input	AI
MIC1P	21	Left Channel Microphone Positive Input/DM_IN	AI, I
MIC1N	22	Left Channel Microphone Negative Input/DM_CLK	AI, O
LLINOUT	23	Left Channel High Impedance Output	AO
P1OUT	24	Left Channel Stage 1 Output	AO
P1IN	25	Left Channel Stage 2 Input	AI
VMID	26	Decoupling internal analog mid supply reference	AO
VREF	27	Buffer Mid supply reference	AO
GPIO<3>/SO	28	General Purpose IO Number Three, 4 Wire SPI	I/O
GPIO<2>	29	General Purpose IO Number Two	I/O
VSSA1	30	Analog Ground	PI
CSb	31	SPI Chip Select	I
SDIO	32	SPI Data In or 2-Wire I/O	I/O

Table 1: Pin Description

TYPE PI: Power In, **PO**: Power Out, **AI**: Analog input, **AO**: Analog output, **I**: input, **O**: output, **I/O**: bi-directional.

1. **The QFN32 package includes a bulk ground connection pad on the underside of the chip. This bulk ground should be thermally tied to the PCB, and electrically tied to the analog ground.**
2. **Unused analog input pins should be left as no-connection.**
3. **Unused digital input pins should be tied to ground.**

5. BLOCK DIAGRAM

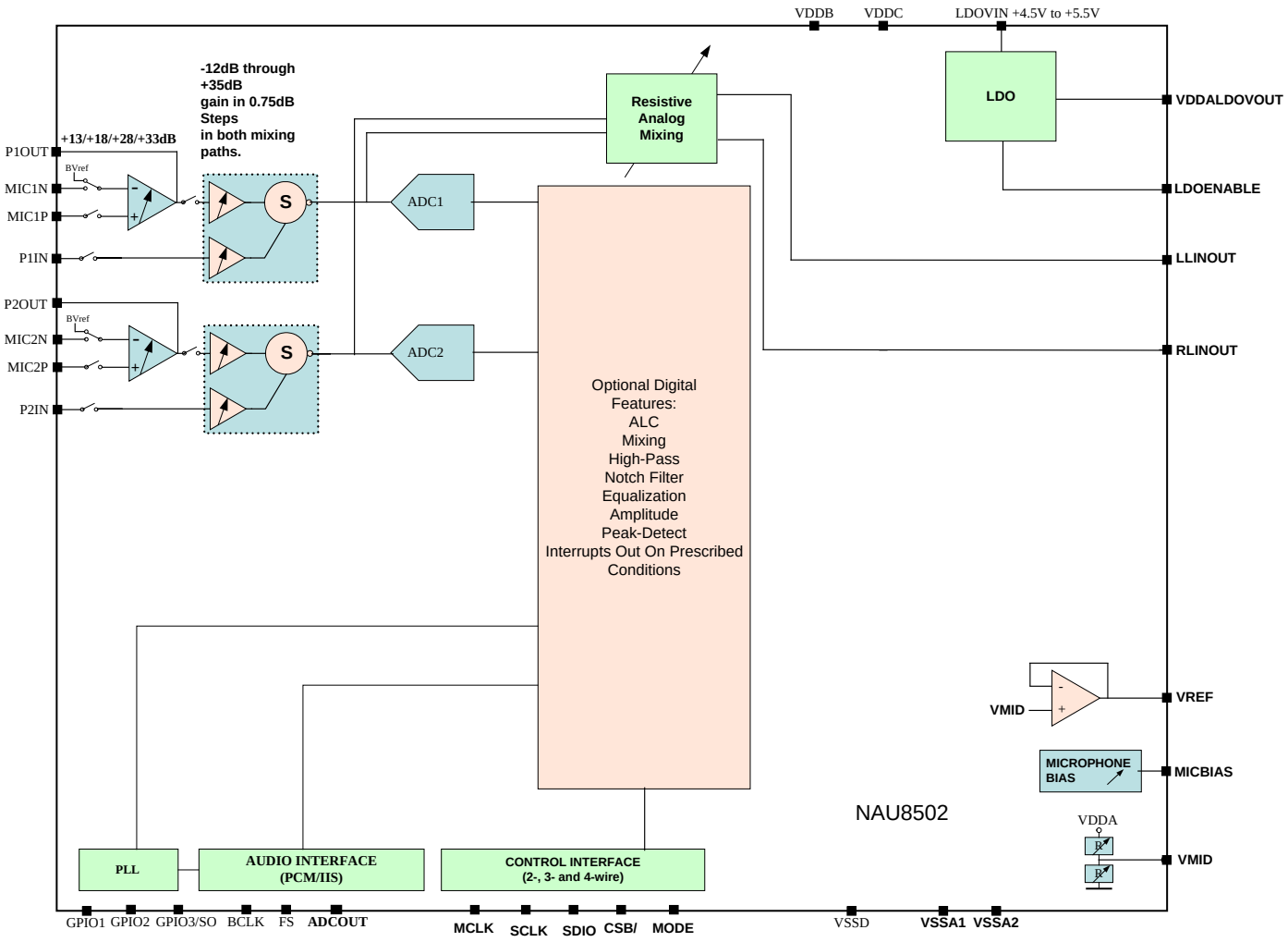


Figure 2: NAU8502 General Block Diagram

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9. ABSOLUTE MAXIMUM RATINGS

CONDITION	MIN	MAX	Units
VDDB, VDDC, VDDA supply voltages	-0.3	+3.61	V
LDOVIN	-0.3	+5.5	V
Core Digital Input Voltage range	VSSD – 0.3	VDDC + 0.30	V
Buffer Digital Input Voltage range	VSSD – 0.3	VDDB + 0.30	V
Analog Input Voltage range	VSSA – 0.3	VDDA + 0.30	V
Industrial operating temperature	-40	+85	°C
Storage temperature range	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended period of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty. These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

10. OPERATING CONDITIONS

Condition	Symbol	Min Value	Typical Value	Max Value	Units
Analogue supplies range	VDDA	2.70[1]		3.60	V
Digital supply range (Buffer)	VDDB	1.71[2]		3.60	V
Digital supply range (Core)	VDDC	1.71[2]		3.60	V
LDO supply range	LDOVIN	4.50		5.50	V
Ground	VSSD VSSA1 VSSA2		0		V

Note 1 : VDDA ≥ VDDB
Note 2 : VDDB ≥ VDDC
Note3: When Using PLL, VDDA ≥ 2.7V and VDDC ≥ 1.9V

ELECTRICAL CHARACTERISTICS

VDDC = +1.8V, VDDA = VDDB = 3.3V, LDOVIN = +5V, T_A = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
Analog to Digital Converter (ADC)						
Full scale input signal [1]	V_{INFS}	PGABST = 0dB PGAGAIN = 0dB		1.0 0		Vrms dBV
Signal-to-noise ratio	SNR	Gain = 0dB, A-weighted	tbd	90		dB
Total harmonic distortion [2]	THD+N	Input = -3dB FS input		-80	tbd	dB
Channel separation at 0dB gain		1kHz input signal		100		dB
Microphone Inputs (MIC1P, MIC1N, MIC2P, MIC2N, P1IN, P2IN) and Programmable Gain Amplifier (PGA)						
Programmable gain			-12		35.25	dB
Programmable gain step size		Guaranteed Monotonic		0.75		dB
Mute Attenuation				110		dB
PGA Input resistance in single ended mode (P1IN P2IN)		PGA Gain = 35.25dB PGA Gain = 0dB PGA Gain = -12dB		1.6 47 75		kΩ kΩ kΩ
Input capacitance				10		pF
PGA equivalent input noise		0 to 20kHz, Gain set to 35.25dB		120		µV
First Stage PGA Amplifier						
First stage PGA gain (single ended on MIC1P MIC2P)		Boost = 00 Boost = 01 Boost = 10 Boost = 11		13 18 28 33		dB dB dB dB
First stage PGA input resistance (single ended on MIC1P MIC2P)		LDC/RDC=1 LDC/RDC=0	5000	500		kΩ kΩ
First stage PGA Microphone Input resistance (differential mode MIC1/2P MIC1/2N)		PGA Gain=10.8dB Boost=00		5.4		kΩ
		PGA Gain=16.8dB Boost=01		3		kΩ
		PGA Gain=27.6dB Boost=10		955		Ω
		PGA Gain=32.8dB Boost=11		537		Ω
PGA1 equivalent input noise		Input referred Noise voltage at 1KHz +28db		7		nV / √Hz
		At 20~20Khz, 28db		2.2		uV rms

Parameter	Symbol	Comments/Conditions	Min	Typ	Max	Units
PGA1 Signal to Noise ratio (A-weighted)		At 20~20K, Vdda=2.7 28db		85		dB
		At 20~20K, Vdda=3.3 28db		94		dB
Total Harmonic Distortion		Gain=13db, Vdda=3.3		-80 0.01		dB %
Line Input to boost/mixer gain			-12		6	dB
Line Input step size to boost/mixer				3		dB
Microphone Bias						
Bias voltage	$V_{MICBIAS}$	See Table 8	0.50, 0.60,0.65, 0.70, 0.75, 0.85, or 0.90			VDDA VDDA
Bias current source	$I_{MICBIAS}$			3		mA
Output noise voltage	V_n	1kHz to 20kHz		14		nV/√Hz
Voltage regulator						
Output Voltage	V_{DDA} /LDOVOUT	LDOVIN=5V LDOENABLE>1.8V C=1uF ESR<0.2		3.3		V
Output current		LDOVIN=5V LDOENABLE>1.8V C=1uF ESR<0.2			40	mA

VDDC = +1.8V, VDDA = VDDB = 3.3V, LDOVIN = +5, T_A = +25ºC, 1kHz signal, fs = 48kHz, 24-bit audio data unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Automatic Level Control (ALC)/Limiter – ADC only						
Target Record Level			-28.5		-6	dB
Programmable Gain			-12		35.25	dB
Programmable Gain Step Size		Guaranteed Monotonic		0.75		dB
Gain Hold Time [4, 6]	tHOLD	MCLK=12.288MHz	0 / 2.67 / …/ 43691 (time doubles with each step)			ms
Gain Ramp-Up (Decay) Time [5, 6]	tDCY	ALC Mode ALCM=0 MCLK=12.288MHz	3.3 / 6.6 / 13.1 / … / 3360 (time doubles with each step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.73 / 1.45 / 2.91 / … / 744 (time doubles with each step)			ms
Gain Ramp-Down (Attack) Time [5, 6]	tATK	ALC Mode ALCM=0 MCLK=12.288MHz	0.83 / 1.66 / 3.33 / … / 852 (time doubles with each step)			ms
		Limiter Mode ALCM=1 MCLK=12.288MHz	0.18 / 0.36 / 0.73 / … / 186 (time doubles with each step)			ms
Digital Input / Output						
Input HIGH Level	V_{IH}		0.7 × VDDB			V
Input LOW Level	V_{IL}				0.3 × VDDB	V
Output HIGH Level	V_{OH}	I_{OL} = 1mA	0.9 × VDDB			V
Output LOW Level	V_{OL}	I_{OH} = -1mA			0.1 x VDDB	V

Notes

1. Full Scale is relative to VDDA (FS = VDDA/3.3.).
2. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full-scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
3. THD+N (dB) - THD+N are a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Hold Time is the length of time between a signal detected being too quiet and beginning to ramp up the gain. It does not apply to ramping down the gain when the signal is too loud, which happens without a delay.
5. Ramp-up and Ramp-Down times are defined as the time it takes to change the PGA gain by 6dB of its gain range.
6. All hold, ramp-up and ramp-down times scale proportionally with MCLK

11. FUNCTIONAL DESCRIPTION

The NAU8502 includes low-noise stereo differential high gain microphone inputs with wide range programmable amplifiers, separate line inputs, and an analog bypass/sidetone line level stereo output.

Advanced on-chip digital signal processing includes a limiter/ALC (Automatic Level Control), 5-band equalizer, notch filter, and a high-pass filter for speech optimization and wind noise reduction. The digital interface can operate as either a master or a slave. Additionally, an internal fractional-N PLL is available to accurately generate any audio sample rate clock for the ADCs derived using any available system clock from 8MHz through 33MHz.

11.1 SIGNAL PATH

The NAU8502 integrates two audio ADC. The input path is highly configurable with 2 programmable gain stages. The first gain stages outputs are connected to the pin P1OUT and P2OUT and can be used to ac couple the signal to the inputs of the second gain stages P1IN and P2IN.

All inputs are maintained at a DC bias at approximately half of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

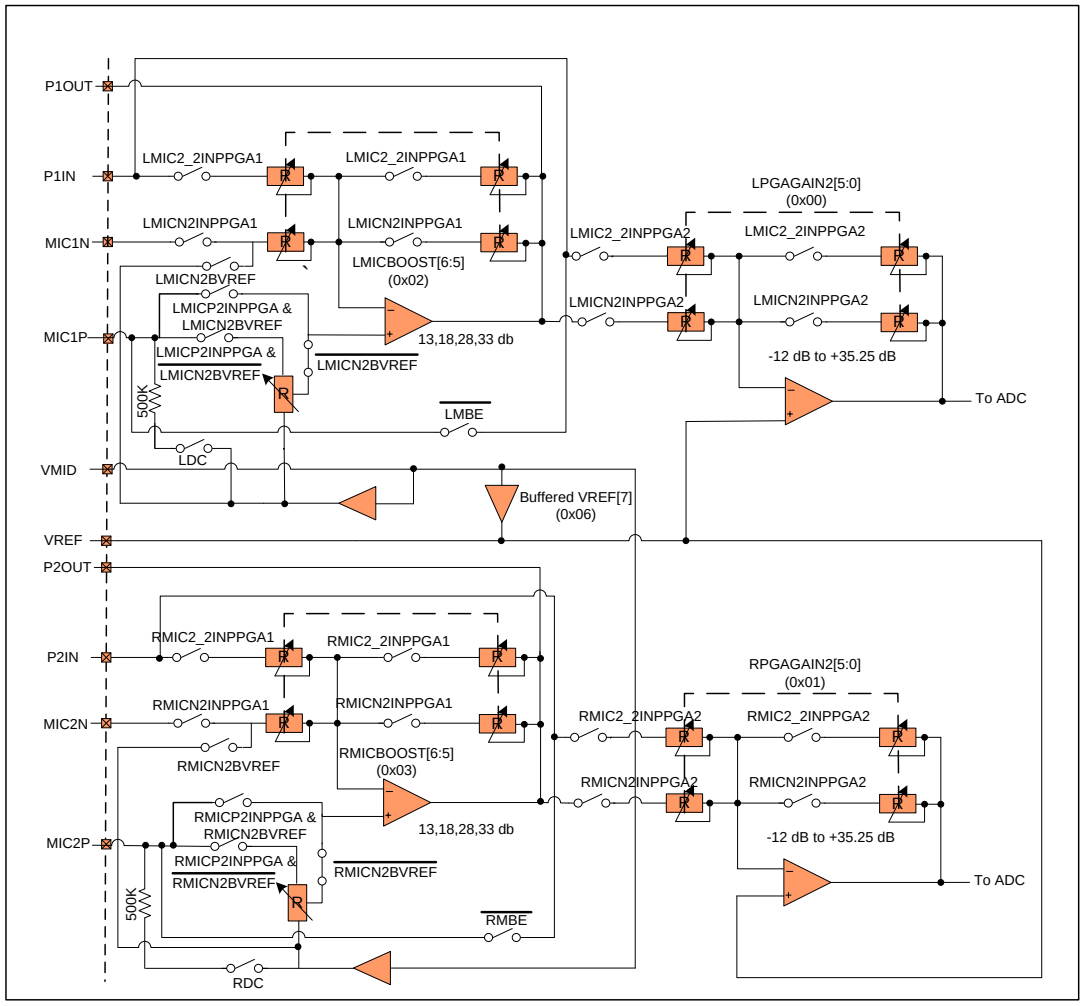


Figure 3 Input path description

Bit(s)	Addr	Parameter	Programmable Range
LMICP2INPPGA	0x4B[0]	Positive Microphone 1 to PGA stage 1	0 = Input PGA stage 1 Positive terminal to VREF 1 = Input PGA stage 1 Positive terminal to MIC1P
LMICN2INPPGA1	0x4B[1]	Negative Microphone 1 to PGA stage 1	0 = MIC1N not connected to input PGA stage 1 1 = MIC1N to input PGA stage 1 Negative terminal.
LMIC2_2INPPGA1	0x4B[2]	P1IN to PGA stage 1	0 = P1IN not connected to input PGA stage1 1 = P1IN to input PGA stage 1 Negative terminal.
LMICN2BVREF	0x22[1]	Buffer voltage to PGA stage 1	0 = Buffer VREF not connected to input PGA stage1 1 = Buffer VREF connected to input PGA stage1
LMIC2_2INPPGA2	0x4B[6]	P1IN to PGA stage 2	0 = P1IN not connected to input PGA stage2 1 = P1IN to input PGA stage 2 Negative terminal.
LMICN2INPPGA2	0x4B[5]	P1OUT to PGA stage 2	0 = not connected to input PGA stage 2 1 = to input PGA stage 2 Negative terminal.
RMICP2INPPGA	0x4C[0]	Positive Microphone 2 to PGA stage 1	0 = Input PGA stage 1 Positive terminal to VREF 1 = Input PGA stage 1 Positive terminal to MIC2P
RMICN2INPPGA1	0x4C[1]	Negative Microphone 2 to PGA stage 1	0 = MIC2N not connected to input PGA stage 1 1 = MIC2N to input PGA stage 1 Negative terminal.
RMIC2_2INPPGA1	0x4C[2]	P2IN to PGA stage 1	0 = P2IN not connected to input PGA stage1 1 = P2IN to input PGA stage 1 Negative terminal.
RMICN2BREF	0x22[0]	Buffer voltage to PGA stage 1	0 = Buffer VREF not connected to input PGA stage1 1 = Buffer VREF connected to input PGA stage1
RMIC2_2INPPGA2	0x4C[6]	P2IN to PGA stage 2	0 = P2IN not connected to input PGA stage2 1 = P2IN to input PGA stage 2 Negative terminal.
RMICN2INPPGA2	0x4C[5]	P2OUT to PGA stage 2	0 = not connected to input PGA stage 2 1 = to input PGA stage 2 Negative terminal.

Table 2: Register associated with Input PGA Control

11.1.1 Positive Microphone Inputs (MIC1P MIC2P)

The positive microphone inputs (MIC1P MIC2P) can be used as part of the differential input. They multiplex to the positive terminal of the first stage PGA gain amplifier by setting LMICP2INPPGA (0x4B[0]) or RMICP2INPPGA (0x4C[0]) to HIGH or can be connected to VREF by setting LMICP2INPPGA (0x4B[0]) and to RMICP2INPPGA (0x4C[0]) to LOW. MIC1P and MIC2P can be connected directly to the second stage of the PGA by setting LMBE (0x2[4]) and RMBE (0x3[4]) to LOW.

In single ended applications where MIC1P, MIC2P inputs are used without using MIC1N and MIC2N, the PGA gain is

$$Gain_{non-inverting-input} = 20.\log\left(1 + 10^{\frac{Gain_{inverting-input}}{20}}\right)$$

This gain is valid only if the MIC1N and MIC2N pins are terminated to a low impedance signal point. This can be done by setting LMICN2BVREF, RMICN2BREF, LMICP2INPPGA, RMICP2INPPGA, to HIGH and LMICN2INPPGA1(0x4B[1]), RMICN2INPPGA1(0x4C[1]) are set to LOW. This termination should normally be an AC coupled path to signal ground. This input impedance depends on the selection of register LDC(0xA[1]) and RDC(0xA[0]). The following table gives the nominal input impedance for this input.

MICP to non-inverting PGA input **Nominal Input Impedance**		
Gain (dB)	**Impedance (kΩ) if LDC and RDC are set to 1**	**Impedance (kΩ) if LDC and RDC are set to 0**
13	500	>5000
18	500	>5000
28	500	>5000
33	500	>5000

Table 3: Microphone Non-Inverting Input Impedances

When the associated control bit of LMICP2INPPGA, RMICP2INPPGA, LMICN2BVREF and RMICN2BVREF are set to logic = 0, the positive microphone input pins are connected to a resistor of approximately 40kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC+ pin close to VREF at all times.

11.1.2 Negative Microphone Inputs (MIC1N MIC2N)

The negative microphone inputs (MIC1N, MIC2N) have two distinctive configuration; differential input or single ended input. These inputs multiplex to the negative terminal of the PGA gain amplifier by setting LMICN2INPPGA1 (0x4B[1]) or RMICN2INPPGA1 (0x4C[1]) to HIGH. When the MIC1N, MIC2N are used as a single ended input, MIC1P MIC2P should be connected to VMID by setting LMICP2INPPGA, RMICP2INPPGA, LMICN2BVREF and RMICN2BVREF to LOW. The P1IN, P2IN input signals can also be mixed with the MIC1N MIC2N input signals by setting LMIC2_2INPPGA1 (0x4B[2]) and RMIC2_2INPPGA1 (0x4C[2]) to HIGH. By setting LMICN2INPPGA1 and RMICN2INPPGA1 to LOW, the pins of MIC1N and MIC2N internally connect to a resistor of approximately 30kΩ that's tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the MIC- pin close to VREF at all times. It is important for a system designer to know that the MIC1N and MIC2N input impedances vary as a function of the selected PGA gain. This is normal and expected for a difference amplifier type

topology. The above table gives the nominal resistive impedance values for this input over the possible gain range. Impedance for specific gain values not listed in this table can be estimated through interpolation between listed values. In a differential configuration LMICN2INPPGA1 (0x4B[1]) or RMICN2INPPGA1 (0x4C[1]) and LMICP2INPPGA (0x4B[0]) or RMICP2INPPGA (0x4C[0]) are set to HIGH. The gain, listed in Table 4, is less than in the MIC1P MIC2P single-ended configuration explained in chapter 12.1.1.

MICN to inverting PGA input MICN and MICP to inverting and non-inverting PGA inputs **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
10.8	5.373
16.83	3.021
27.65	0.955
32.8	0.537

Table 4: Microphone Inverting Input Impedances

11.1.3 The Single Ended Auxiliary Input (P1IN P2IN)

The single ended auxiliary inputs have two different paths.

- Directly connected to the first stage Programmable Gain amplifier
- Used in conjunction with P[1-2]OUT as AC coupled input to the second stage PGA

The second-stage PGA gain ranges from -12dB to +35.25 dB with 0.75db step.

The two paths above go through the ADC filters where the ALC loop may be used to control the amplitude of the input signal. The device also has an internal configurable biasing circuit for biasing the microphone, reducing external components.

When LMIC2_2INPPGA2 and RMIC2_2INPPGA2 are set to LOW, the single ended auxiliary input pins are connected to a resistor of approximately 30kΩ which is tied to VREF. The purpose of the tie to VREF is to reduce any pop or click sound by keeping the DC level of the P[1-2]IN pin close to VREF at all times.

MICN PIN to inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
-12	75
-9	69
-6	63
-3	55
0	47
3	39
6	31
9	25

MICN PIN to inverting PGA input **Nominal Input Impedance**	
Gain (dB)	**Impedance (kΩ)**
12	19
18	11
30	2.9
35.25	1.6

Table 5: Microphone Inverting Input Impedances

11.1.4 PGA Gain Control

The two stages of PGA amplification have independent gain settings.

The first stage PGA, also called mic pre-amp or boost, is enabled by LMBE and RMBE (0x02[4] 0x03[4]). The first stage PGA has four fixed gain settings +13dB, +18dB. +28dB, +33dB controlled by LMICBOOST (0x2[6:5]) and RMICBOOST (0x3[6:5]). The mute registers LMBMUTE and RMBMUTE are reserved and cannot be used.
When LMBE and RMBE are disabled, the first stage PGA is automatically bypassed and routed to the input of the second stage PGA.

The second stage PGA has a range of -12dB to +35.25dB in 0.75dB steps, controlled by INPPGALVOL (0x4D) INPPGARVOL (0x4E). Registers LINVOL 99i and RINVOL 0x01 may also be used to set the second stage PGA gain that are eventually mapped to INPPGALVOL and INPPGARVOL.
Second stage Input PGA gain will not take effect when ALC is enabled using register ALCEN (0xC[8:7]).

Zero crossing on the first stage PGA is enabled with LMZC (0x2[3]) and RMZC(0x3[3]).
Zero crossing on the second stage PGA is enabled with LPZC (0x2[2]) and RPZC (0x3[2]).

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x02	0		LMICBOOST		LMBE	LMZC	LPZC			0x007
0x03	0		RMICBOOST		RMBE	RMZC	RPZC			0x007
0x4D	0		LMBMUTE	INPPGALVOL						0x010
0x4E	0		RMBMUTE	INPPGARVOL						0x010

Table 6: Registers associated with Input PGA Gain Control

11.2 MICROPHONE BIASING

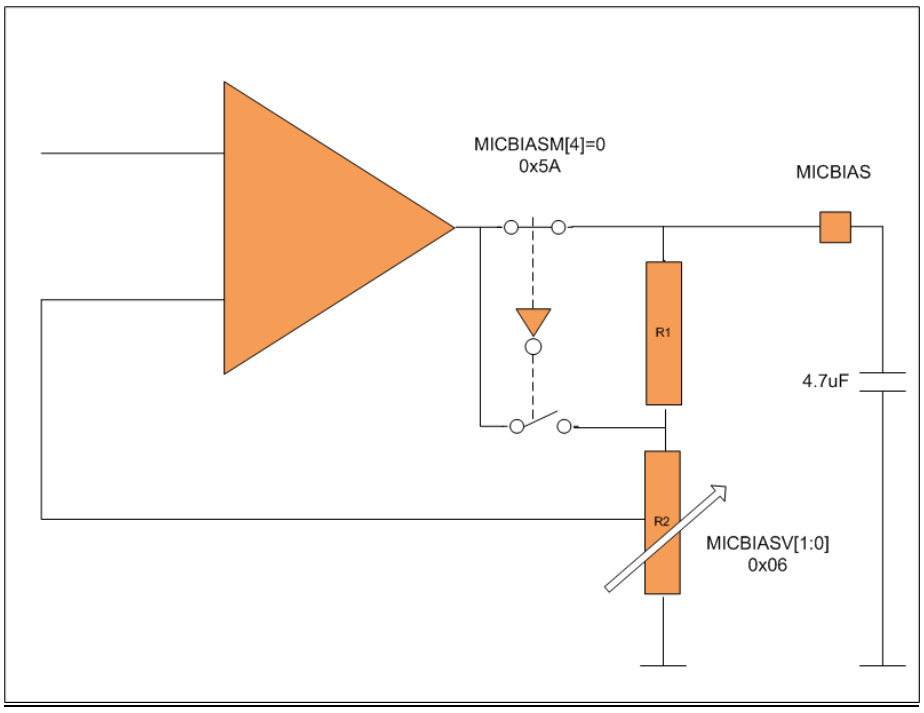


Figure 4: Microphone Bias Schematic

The MICBIAS pin is a low-noise microphone bias source for an external microphone, which can provide a maximum of 3mA of bias current. This DC bias voltage is suitable for powering either traditional ECM (electret) type microphones, or for MEMS types microphones with an independent power supply pin. Seven different bias voltages are available for optimum system performance, depending on the specific application. The microphone bias pin normally requires an external filtering capacitor as shown on the schematic in the Application section.

It has various voltage values selected by a combination of bits MICBIASM[4] address (0x5A) and MICBIASV[1:0] address (0x06).

When MICBIASM[4] is set to HIGH, low-noise is achieved by an internal resistor of approximately 200-ohms in series with the output pin. This creates a low pass filter in conjunction with the external microphone-bias filter capacitor, but without any additional external components.

Bit(s)	Addr	Parameter	Programmable Range
MICBIASM	0x05A[4]	Microphone bias mode selection	0=default larger cap on micbias 1=lower cap on micbias
MICBIASV	0x06[1:0]	Microphone bias voltage selection	00 off 01 0.75*VDDA 10 0.9*VDDA 11 0.5*VDDA

Table 7: Register associated with Microphone Bias

Below are the unloaded values when MICBIASM[4] is set to 1 and 0. When loaded, the series resistor will cause the voltage to drop, depending on the load current.

Microphone Bias Voltage Control			
MICBIASV[1:0]		MICBIASM[4] = 0	MICBIASM[4]= 1
0	0	off	off
0	1	0.75* VDDA	0.70* VDDA
1	0	0.9* VDDA	0.85* VDDA
1	1	0.50* VDDA	0.50* VDDA

Table 8: Microphone Bias Voltage Control

11.3 UNUSED ANALOG I/O AND VMID SELECTION

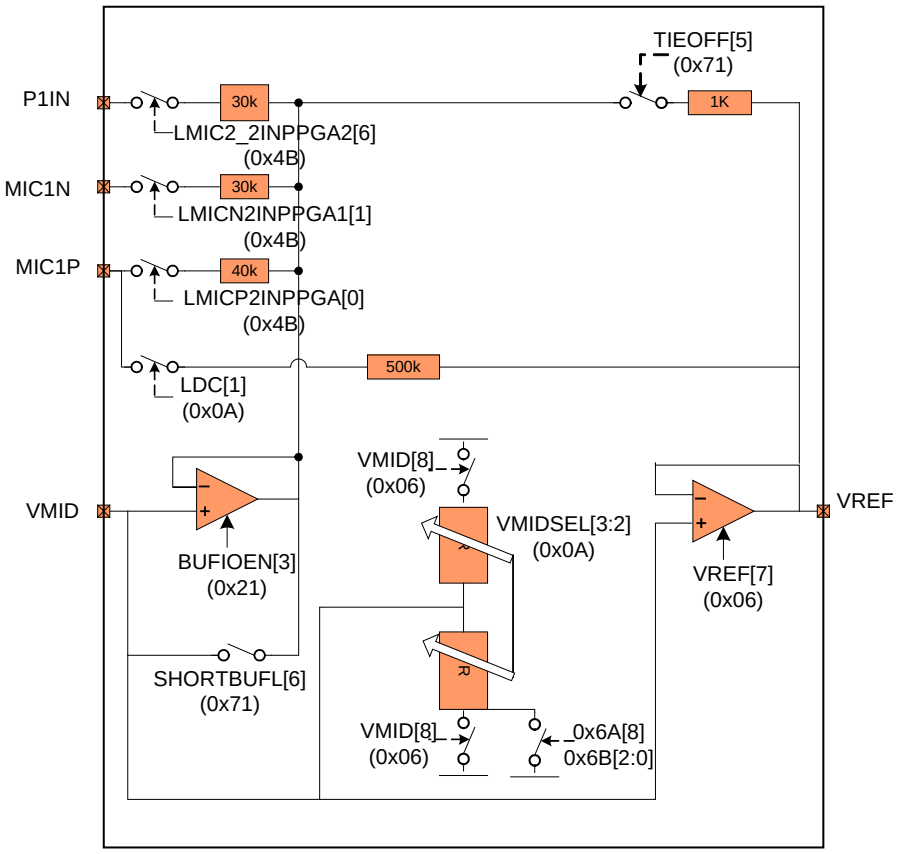


Figure 5 Tie-off Options

In audio and voice systems, any time there is a sudden change in voltage to an audio signal, an audible pop or click sound may be the result. Systems that change input and output configurations dynamically, or which are required to manage low power operation, need special attention to possible pop and click situations. The NAU8502 includes many features which may be used to greatly reduce or eliminate pop and click sounds. The most common cause of a pop or click signal is a sudden change to an input or output voltage. This may happen in either a DC coupled system, or in an AC coupled system.

The strategy to control pops and clicks is similar for either a DC coupled system, or an AC coupled system. The case of the AC coupled system is the most common and the more difficult situation, and therefore, the AC coupled case will be the focus for this information section. When an input or output pin is being used, the DC level of that pin will be very close to half of the VDDA voltage that is present on the VMID pin. In all cases, any input or output capacitors will become charged to the operating voltage of the used input or output pin. The goal to reduce pops and clicks is to insure that the charge voltage on these capacitors does not change suddenly at any time.

In order to use the tie-off on the VREF buffer REGENABLE[8] 0x71 must be set to 1.

When an input or output is in a not-used operating condition, it is desirable to keep the DC voltage on that pin at the same voltage level as the DC level of the used operating condition. This is accomplished using special internal DC

voltage sources that are at the required DC values. When an input or output is in the not-used condition, it is connected to the correct internal DC voltage as not to have a pop or click. This type of connection is known as a “tie-off” condition.

Outputs will automatically be tied to the VMID voltage value. The input pullups are connected to BUFIOEN[3] address (0x21) buffer with a voltage source (VMID). The output pullups can be connected to the same buffer.

Automatic internal logic determines whether an input or output pin is in the used or un-used condition. This logic function is always active. An output is determined to be in the un-used condition when it is in the disabled unpowered condition, as determined by the power management registers. An input is determined to be in the un-used condition when all internal switches connected to that input are in the “open” condition.

11.4 DIGITAL MICROPHONE

The digital microphone interface is enabled by setting register EN_DIG_MIC_L (0x68[4]) or EN_DIG_MIC_R (0x68[5]). NAU8502 can support up to two digital microphones through pin MIC1P. When pin MIC1N is configured as DM_CLK output, NAU8502 will generate a clock signal in the range of 1-4Mhz to support the digital microphone operation. Volume control for the digital microphone can be set in two ways. If ALCEN (0xC) is off, volume control for the digital microphone is provided by ADCVOLL (0x2f) and ADCVOLR(0x30). If ALCEN is on, volume control is set by the ALC registers in address 0xC.

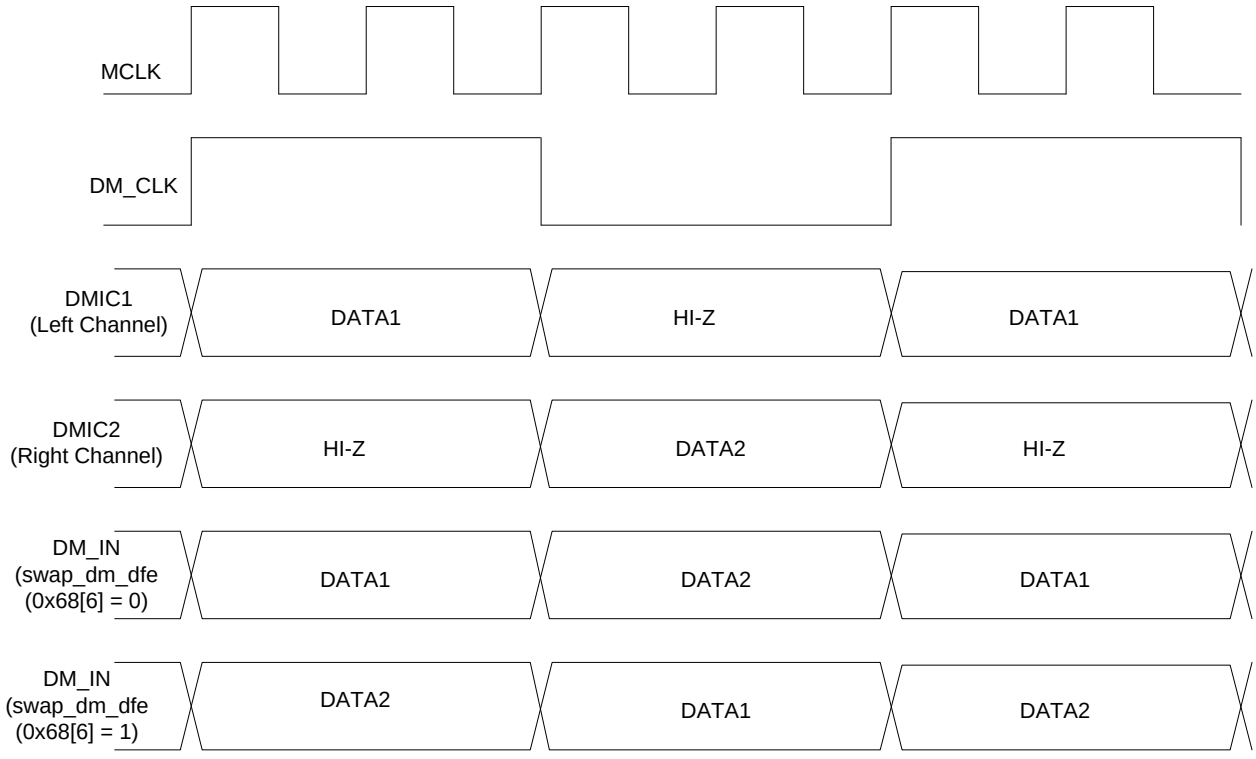


Figure 6 Digital Microphone Waveforms

11.5 ADC DIGITAL FILTER BLOCK

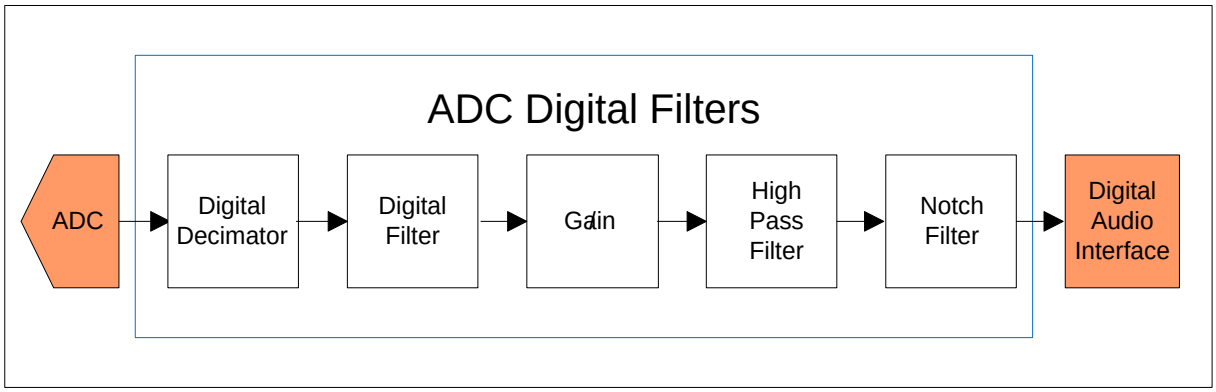


Figure 7: ADC Digital Filter Path Block Diagram

The ADC digital filter block performs a 24-bit signal processing. The block consists of an oversampled analog sigma-delta modulator, digital decimator, digital filter, high pass filter, and a notch filter. The oversampled analog sigma-delta modulator provides a bit stream to the decimation stages and filter. The ADC coding scheme is in twos-complement format and the full-scale input level is proportional to VDDA. With a 3.3V supply voltage, the full-scale level is $1.0V_{RMS}$ and any voltage greater than full scale may overload the ADC and cause distortion. The ADC is enabled by setting ADL[3] and ADR[2] in address (0x06) to HIGH. Polarity and oversampling rate of the ADC output signal can be changed by POLARITY[6:5] address (0x05) and ADCOSR[3] address (0x2E) respectively.

Bit(s)	Addr	Parameter	Programmable Range
POLARITY[6:5]	0x05	ADC Polarity	00 no inversion on ADC data 01 Left (1) inverted 10 Right (2) inverted 11 both inverted
ADCOSR[3]	0x2E	ADC Over Sample Rate	0=64x (Lowest power) 1=128x (best SNR at typical condition)
ADCHPD[0]	0x05	High Pass Filter Disable	0 = Enable 1 = Disable
HPFAPP[7]	0x2E	Audio or Application Mode	0 = Audio (1^{st} order, fc ~ 3.7 Hz) 1 = Application (2^{nd} order, fc = HPFCUT)
HPFCUT[6:4]	0x2E	High Pass Filter frequencies	82 Hz to 612 Hz dependant on the sample rate
ADL[3]	0x02	Enable Left Channel ADC	0 = Disable 1 = Enable
ADR[2]	0x02	Enable Right Channel ADC	0 = Disable 1 = Enable
SMPLR[3:1]	0x27	Sample rate	8k Hz to 48 kHz

Table 9: Register associated with ADC

11.5.1 Programmable High Pass Filter (HPF)

The high pass filter (HPF) has two different modes that it can operate in either Audio or Application mode HPFAPP[7] address (0x2E). In Audio Mode (HPFAPP=0) the filter is first order, with a cut-off frequency of 3.7kHz. In Application mode (HPFAPP=1) the filter is second order, with a cut-off frequency selectable via the HPFCUT[6:4] register bits. Cut-off frequency of the HPF depends on sample frequency selected by SMPLR[3:1] address (0x27). The HPF is enabled by setting ADCHPD[0] address (0x05) to LOW. Table below shows the cut-off frequencies with different sampling rate.

HPFCUT[6:4]	fs (kHz)								
	SMPLR=101/100			SMPLR=011/010			SMPLR=001/000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 10: High Pass Filter Cut-off Frequencies (HPFAM=1)

11.5.2 Programmable Notch Filter (NF)

Each ADC is optionally supported by a notch filter in the digital output path. Filter operation and settings are always the same for both left and right channels. A notch filter is useful to filter out a very narrow band of audio frequencies in a stop band around a given center frequency. The notch filter is enabled by setting NFCEN (0x3B[7]) to 1. The center frequency is programmed by setting registers 0x3B, 0x3C, 0x3D, and 0x3E, bits 0 to 6 (NFA0[13:7], NFA0[6:0], NFA1[13:7], NFA1[6:0]), with two's complement coefficient values calculated using Table 12.

Registers that affect operation of the notch filter are:

0x3B Notch filter enable/disable
0x3B Notch filter a0 coefficient high order bits and update bit
0x3C Notch filter a0 coefficient low order bits and update bit
0x3D Notch filter a1 coefficient high order bits and update bit
0x3E Notch filter a1 coefficient low order bits and update bit

Important: The register update bits are write-only bits. The update bit function is important so that all filter coefficients actively being used are changed simultaneously, even though these register values must be written sequentially. When there is a write operation to any of the filter coefficient settings, but the update bit is not set (value = 0), the value is

stored as pending for the future, but does not go into effect. When there is a write operation to any coefficient register, and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any pending coefficient value is put into effect at the same time.

Coefficient values are in the form of 2's-complement integer values, and must be calculated based upon the desired filter properties. The mathematical operations for calculating these coefficients are detailed in the following table.

Addr	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x3B	NFCU	NFCEN	NFCA0[13:7]							0x000
0x3C	NFCU	0	NFCA0[6:0]							0x000
0x3D	NFCU	0	NFCA1[13:7]							0x000
0x3E	NFCU	0	NFCA1[6:0]							0x000

Table 11: Registers associated with Notch Filter Function

	A_0	A_1	Notation	Register Value (DEC)
Coefficient	$\frac{1-\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}{1+\tan\left(\frac{2\ \pi\ f_b}{2\ f_s}\right)}$	$-\left(1+A_0\right)\ x\ \cos\left(\frac{2\ \pi\ f_c}{f_s}\right)$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) fs = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ (then convert to 2's complement)

Table 12: Equations to Calculate Notch Filter Coefficients

11.5.3 Digital ADC Gain Control

The digital ADC can be muted by setting "0000 0000" to ADCVOLL[7:0] address (0x2F) for the left channel or ADCVOLR[7:0] address (0x30) for the right channel. Any other combination digitally attenuates the ADC output signal in the range -127dB to 0dB in 0.5dB increments]. The gain setting takes effect only when the update bit in the MSB of the gain register is set.

Addr	Name	Bit 8	Bit 7	Bit 6	Bit5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
0x2F	**ADCG**	ADCVU	ADCVOLL								**0x0FF**
0x30	**ADCG**	ADCVU	ADCVOLR								**0x0FF**

Table 13: Register associated with ADC Gain

11.6 EQUALIZER

The NAU8502 includes a 5-band graphic equalizer with low distortion, low noise, and wide dynamic range. The equalizer is applied to both left and right channels. Registers that affect operation of the 5-Band Equalizer are:

0x32 Band 1 gain control and cut-off frequency

0x33 Band 2 gain control, center cut-off frequency, and bandwidth

0x34 Band 3 gain control, center cut-off frequency, and bandwidth

0x35 Band 4 gain control, center cut-off frequency, and bandwidth

0x36 Band 5 gain control and cut-off frequency

Each of the five equalizer bands is independently adjustable for maximum system flexibility, and each offers up to 12dB of boost and 12dB of cut with 1dB resolution. The high and the low bands are shelving filters (high-pass and low-pass, respectively), and the middle three bands are peaking filters. Details of the register value settings are described below. Response curve examples are provided in the Appendix of this document.

Register Value	Equalizer Band				
	1 (High Pass) Register 18 Bits 5 & 6 EQ1CF	2 (Band Pass) Register 19 Bits 5 & 6 EQ2CF	3 (Band Pass) Register 20 Bits 5 & 6 EQ3CF	4 (Band Pass) Register 21 Bits 5 & 6 EQ4CF	5 (Low Pass) Register 22 Bits 5 & 6 EQ5CF
00	80Hz	230Hz	650Hz	1.8kHz	5.3kHz
01	105Hz	300Hz	850Hz	2.4kHz	6.9kHz
10	135Hz	385Hz	1.1kHz	3.2kHz	9.0kHz
11	175Hz	500Hz	1.4kHz	4.1kHz	11.7kHz

Table 14: Equalizer Center/Cutoff Frequencies

Register Value		Gain	Registers
Binary	Hex		
00000	00h	+12db	Bits 0 to 4 in registers 18 (EQ1GC) 19 (EQ2GC) 20 (EQ3GC) 21 (EQ4GC) 22 (EQ5GC)
00001	01h	+11dB	
00010	02h	+10dB	
- - -	- -	Increments 1dB per step	
01100	0Ch	0dB	
01101	17h	-11dB	
- - -	- -	Increments 1dB per step	
11000	18h	-12dB	
11001 to 11111	19h to 1Fh	Reserved	

Table 15: Equalizer Gains

11.7 PROGRAMMABLE GAIN AMPLIFIER (PGA)

The NAU8502 has a programmable gain amplifier (PGA) which controls the gain such that the signal level of the PGA remains substantially constant as the input signal level varies within a specified dynamic range. The Automatic Level Control (ALC) can operate in either normal mode or limiter mode.

The Automatic Level Control (ALC) seeks to control the PGA gain in response to the amplitude of the input signal such that the PGA output maintains a constant envelope. A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x0C).

11.7.1 Automatic level control (ALC)

The ALC seeks to control the PGA gain such that the PGA output maintains a constant envelope. This helps to prevent clipping at the input of the sigma delta ADC while maximizing the full dynamic range of the ADC. The ALC monitors the output of the ADC, measured after the digital decimator has converted it to 1.23 fixed-point formats. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. Based on a comparison between the measured peak value and the target value, the ALC block adjusts the gain control, which is fed back to the PGA.

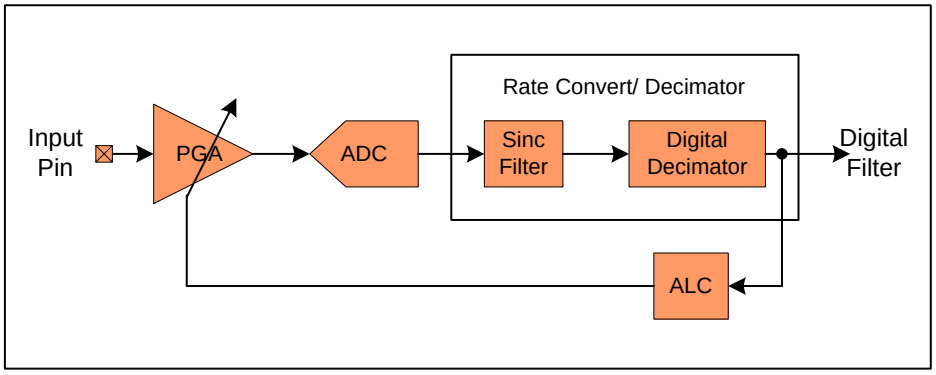


Figure 8: ALC Block Diagram

The ALC is enabled by setting ALCEN[8:7] address (0x0C) bit HIGH. The ALC has two functional modes, which is set by ALCMODE[5] address (0x0D).

- Normal mode (ALCMODE = LOW)
- Peak Limiter mode (ALCMODE = HIGH)

When the ALC is disabled, the input PGA remains at the last controlled value of the ALC. An input gain update must be made by writing to the PGAGAIN[5:0] address (0x4D). A digital peak detector monitors the input signal amplitude and compares it to a register defined threshold level ALCSL[3:0] address (0x0C).

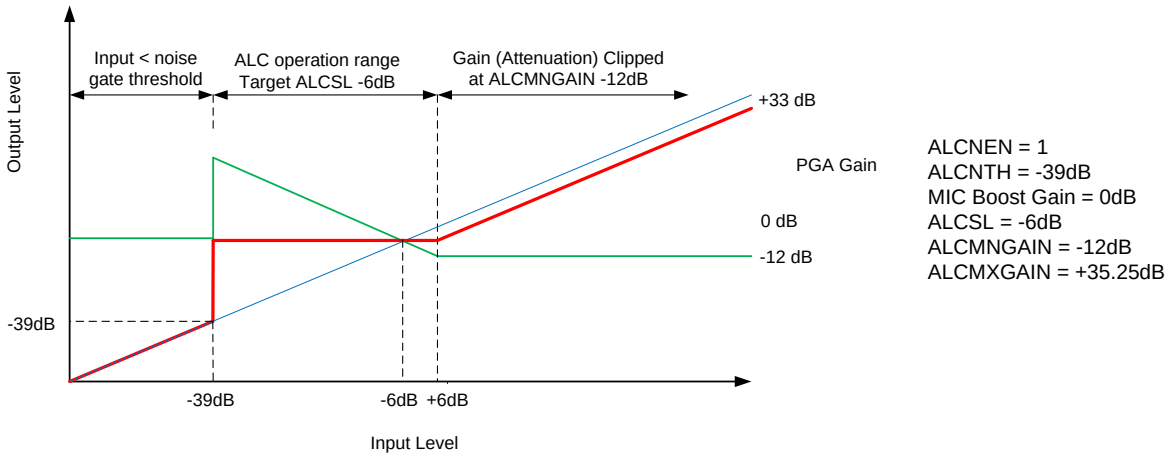


Figure 9: ALC Response Graph

The registers listed in the following section allow configuration of ALC operation with respect to:

- ALC target level
- Gain increment and decrement rates
- Minimum and maximum PGA gain values for ALC operating range
- Hold time before gain increments in response to input signal
- Inhibition of gain increment during noise inputs
- Limiter mode operation

Bit(s)	Addr	Parameter	Programmable Range
ALCMINGAIN[7:5]	0x0B	Minimum Gain of PGA	Range: -12dB to +30dB @ 6dB increment
ALCSL[3:0]	0x0C	ALC Target	Range: ALCTABLESEL = 0: -28.5dB to -6dB @ 1.5dB increment ALCTABLESEL = 1 -22.5dB to -1.5dB @ 1.5dB increment
ALCMAXGAIN[6:4]	0x0C	Maximum Gain of PGA	Range: -6.75dB to +35.25dB @ 6dB increment
ALCEN[8:7]	0x0C	Enable ALC function	00 = ALC disabled 01 = Right channel ALC enabled 10 = Left channel ALC enabled 11 = Both channels ALC enabled
ALCHLD[3:0]	0x0D	ALC Hold Time	Range: 0ms to 1s, time doubles with every step)
ALCZCE[4]	0x0D	ALC Zero Crossing	0 = Disable 1 = Enable
ALCMODE[5]	0x0D	ALC Select	0 = ALC mode 1 = Limiter mode
ALCATK[3:0]	0x0E	ALC Attack time	ALCMODE =0 - Range: 125us to 128ms =1 - Range: 31us to 32ms (time doubles with every step) Note: parameters refer to time to update one 0.75 dB step
ALCDCY[7:4]	0x0E	ALC Decay time	ALCMODE =0 - Range: 500us to 512ms =1 - Range: 125us to 128ms (Both ALC time doubles with every step) Note: parameters refer to time to update one 0.75 dB step
ALCTABLESEL[8]	0x66	ALCTABLESEL	0 = ALCSL range -28.5:-6dB 1 = ALCSL range -22.5:-1.5 dB

Table 16: Registers associated with ALC Control

The operating range of the ALC is set by ALCMAXGAIN[6:4] address (0x0C) and ALCMINGAIN[7:5] address (0x0B) bits such that the PGA gain generated by the ALC is between the programmed minimum and maximum levels. When the ALC is enabled, the PGA gain setting from INPPGAVOLL and INPPGAVOLR (0x4D and 0x4E) has no effect.

In Normal mode, the ALCMXGAIN bits set the maximum level for the PGA in the ALC mode but in the Limiter mode ALCMXGAIN has no effect because the maximum level is set by the initial PGA gain setting upon enabling of the ALC.

ALCMAXGAIN	Maximum Gain (dB)
111	35.25
110	29.25
ALC Max Gain Range 35.25dB to -6dB @ 6dB increments	
001	-0.75
000	-6.75

ALCMINGAIN	Minimum Gain (dB)
000	-12
001	-6
ALC Min Gain Range -12dB to 30dB @ 6dB increments	
110	24
111	30

Table 17: ALC Maximum and Minimum Gain Values

11.7.1.1 Normal Mode

Normal mode is selected when ALCMODE[5] address (0x0D) is set LOW and the ALC is enabled by setting either of the ALCEN[8:7] bits address (0x0C) HIGH. This block adjusts the PGA gain setting up and down in response to the input level. A peak detector circuit measures the envelope of the input signal and compares it to the target level set by ALCSL[3:0] address (0x0C). The ALC increases the gain when the measured envelope is less than (target – 1.5dB) and decreases the gain when the measured envelope is greater than the target. The following waveform illustrates the behavior of the ALC.

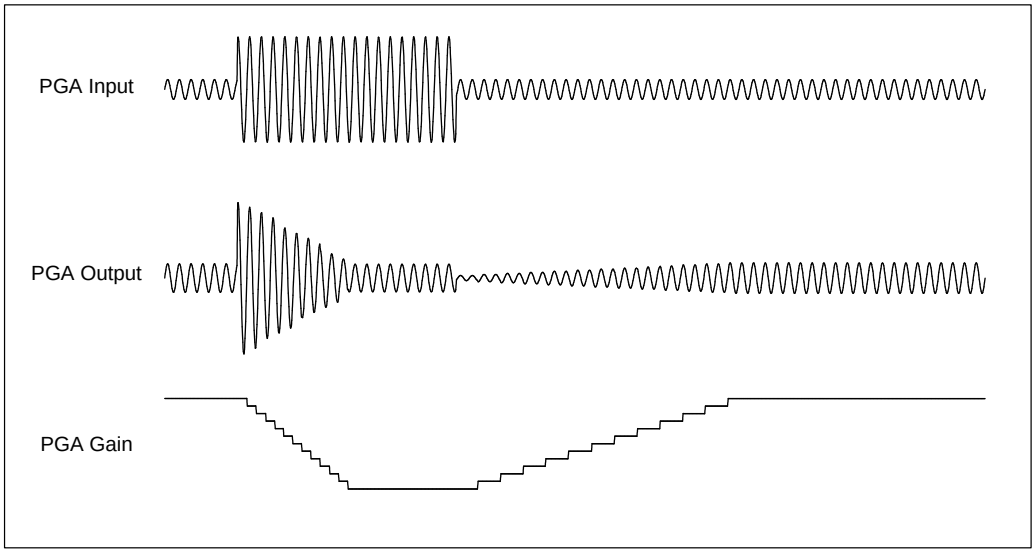


Figure 10: ALC Normal Mode Operation

11.7.1.2 ALC Hold Time (Normal mode Only)

The hold parameter ALCHT[3:0] address (0x0D) configures the time between detection of the input signal envelope being outside of the target range and the actual gain increase.

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimal performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings; having a shorter hold time, on the other hand, may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the ALCHT parameter.

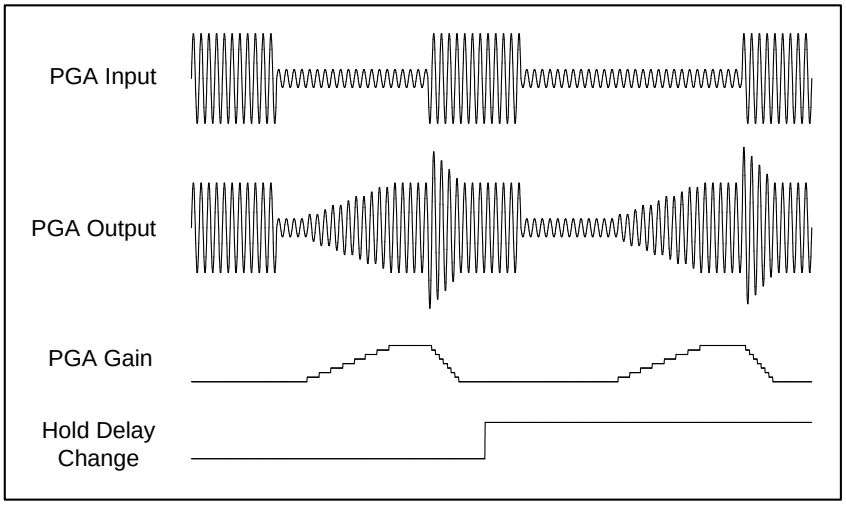


Figure 11: ALC Hold Time

11.7.1.3 Peak Limiter Mode

Peak Limiter mode is selected when ALCMODE[5] address (0x0D) is set to HIGH and the ALC is enabled by setting ALCEN[8:7] address (0x0C). In limiter mode, the PGA gain is constrained to be less than or equal to the gain setting at the time the limiter mode is enabled. In addition, attack and decay times are faster in limiter mode than in normal mode as indicated by the different lookup tables for these parameters for limiter mode. The following waveform illustrates the behavior of the ALC in Limiter mode in response to changes in various ALC parameters.

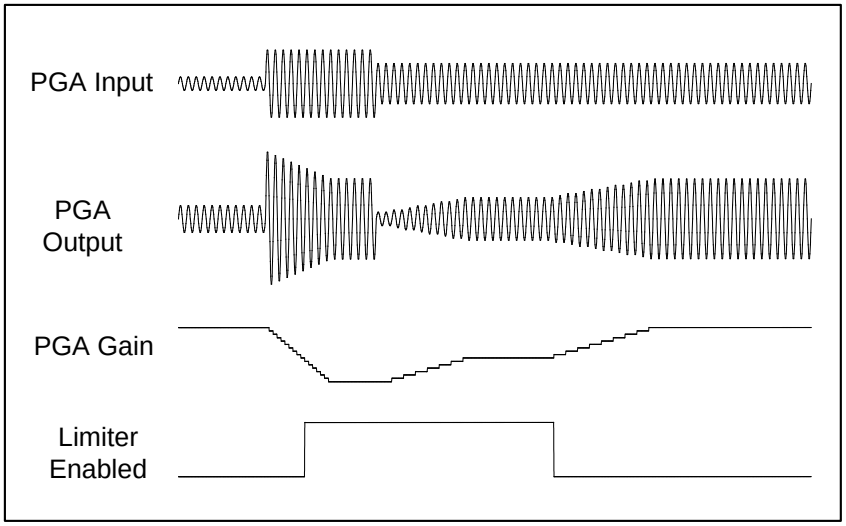


Figure 12: ALC Limiter Mode Operations

When the input signal exceeds 87.5% of full scale, the ALC block ramps down the PGA gain at the maximum attack rate (ALCATK=0000) regardless of the mode and attack rate settings until the ADC output level has been reduced below the threshold. This limits ADC clipping if there is a sudden increase in the input signal level.

11.7.1.4 Attack Time

When the absolute value of the ADC output exceeds the level set by the ALC threshold, ALCSL[3:0] address (0x0C), attack mode is initiated at a rate controlled by the attack rate register ALCATK[3:0] address (0x0E). The peak detector in the ALC block loads the ADC output value when the absolute value of the ADC output exceeds the current measured peak; otherwise, the peak decays towards zero, until a new peak has been identified. This sequence is continuously running. If the peak is ever below the target threshold, then there is no gain decrease at the next attack timer time; if it is ever above the target-1.5dB, then there is no gain increase at the next decay timer time.

11.7.1.5 Decay Times

The decay time ALCDCY[7:4] address (0x0E) is the time constant used when the gain is increasing. In limiter mode, the time constants are faster than in ALC mode.

11.7.1.6 Noise gate (normal mode only):

A noise gate is used when there is no input signal or the noise level is below the noise gate threshold. The noise gate is enabled by setting NGAT[0] address (0x0B) to HIGH. It does not remove noise from the signal. The noise gate threshold NGTH[4:2] address (0x0B) is set to a desired level so when there is no signal or a very quiet signal (pause), which is composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The noise gate only operates in conjunction with the ALC (ALCEN[8:7] 0x0C) and ONLY in Normal mode. The noise gate flag is asserted when

(Signal at ADC – PGA gain – MIC Boost gain) < ALCNTH (ALC Noise Gate Threshold) (dB)

Levels at the extremes of the range may cause inappropriate operation, so care should be taken when setting up the function.

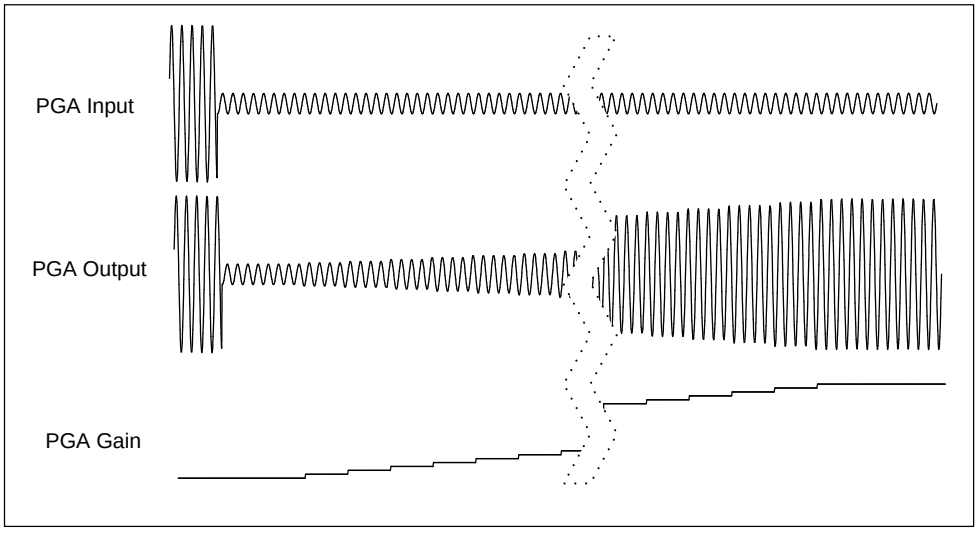


Figure 13: ALC Operation with Noise Gate disabled

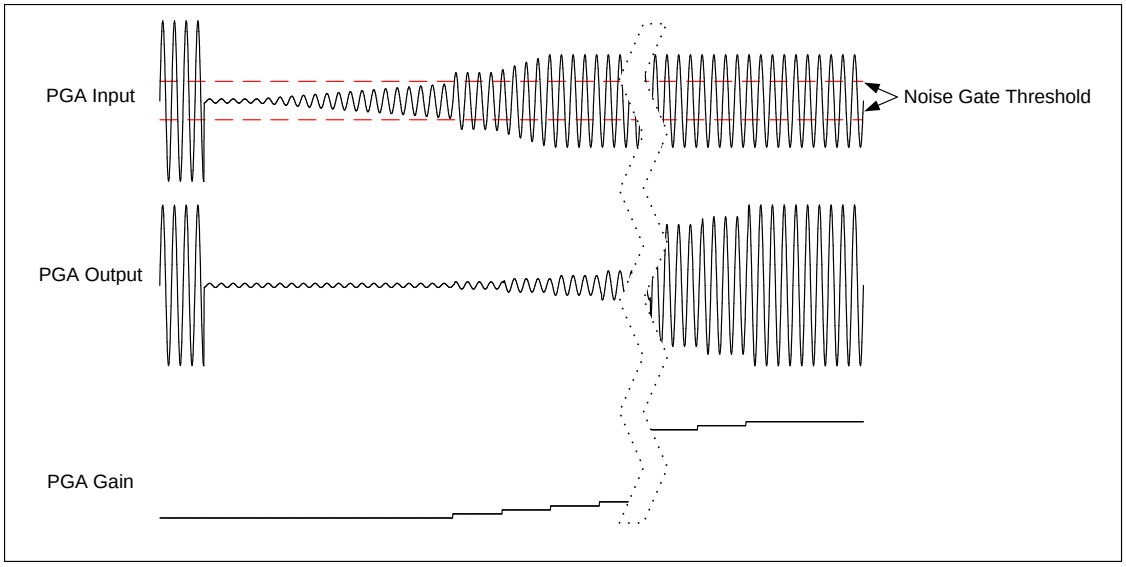


Figure 14: ALC Operation with Noise Gate Enabled

11.7.2 Zero Crossing

The PGA gain comes from either the ALC block when it is enabled or from the PGA gain register setting when the ALC is disabled. Zero crossing detection may be enabled to cause PGA gain changes to occur only at an input zero crossing. Enabling zero crossing detection limits clicks and pops that may occur if the gain changes while the input signal has a high volume.

There are two zero crossing detection enables:

- Register ALCZCE[8] address (0x0D) – is only relevant when the ALC is enabled.
- Register PGAZC[2] address (0x02, 0x03) – is only relevant when the ALC is disabled.

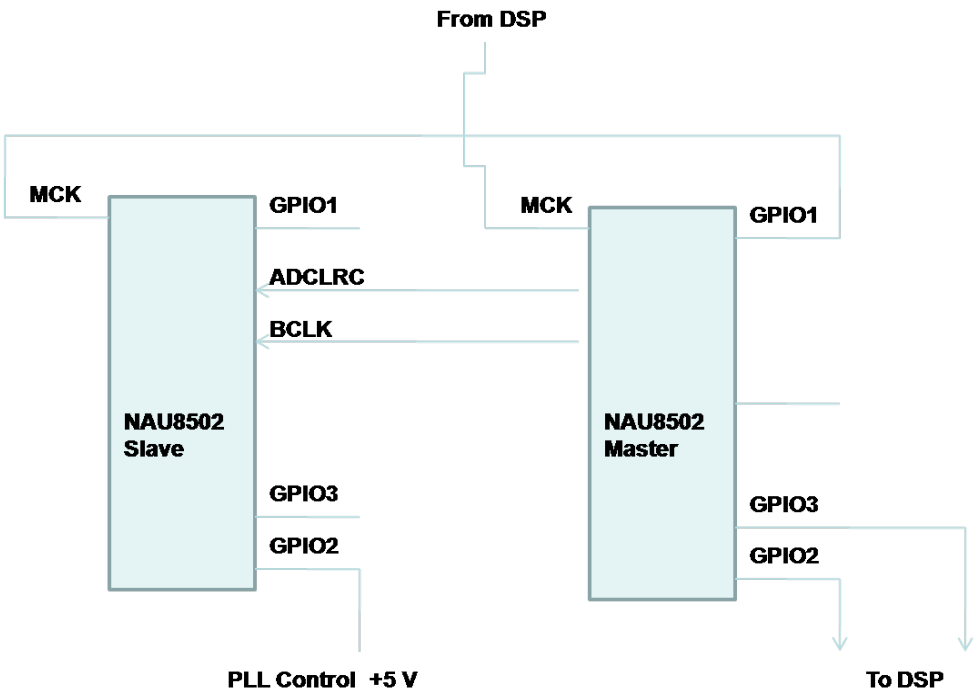
If the zero crossing function is enabled (using either register) and SLOWCLKEN[0] address (0x27) is asserted, the zero cross timeout function may take effect. If the zero crossing flag does not change polarity within 0.25 seconds of a PGA gain update (either via ALC update or PGA gain register update), then the gain will update. This backup system prevents the gain from locking up if the input signal has a small swing and a DC offset that prevents the zero crossing flag from toggling.

The slow clock timer at address 0x27[0] controls features that happen over a relatively long period of time. This enables the NAU8502 to implement long time-span features without any host/processor management or intervention. The Slow clock timer is initialized in the disabled state but is automatically asserted when zero crossing is enabled.

The slow clock timer rate is derived from MCLK using an integer divider that is compensated for the sample rate as indicated by the register address (0x08/0x27). If the sample rate register value precisely matches the actual sample rate, then the internal slow clock timer rate will be a constant value of 128ms. If the actual sample rate is, for example, 44.1kHz and the sample rate selected in register 0x27 is 48kHz, the rate of the slow clock timer will be approximately 10% slower in direct proportion of the actual vs. indicated sample rate. This scale of difference should not be important in relation to the dedicated end uses of the slow clock timer.

11.8 GPIO

There are three GPIO pins can be used for;



Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x29	GPIO_PS[2:0]			GPIO_PE[2:0]			GPIO_OE[2:0]			**0x000**
0x2A	GPIO3_OUT_SEL[2:0]			GPIO2_OUT_SEL[2:0]			GPIO1_OUT_SEL[2:0]			**0x000**
0x2B							GPIO3_IN	GPIO2_IN	GPIO1_IN	
0x2C		INT_POL			Clip2_INTE	Clip1_INTE	GPIO3_INTE	GPIO2_INTE	GPIO1_INTE	
0x2D					Clip2_INT	Clip1_INT	GPIO3_INT	GPIO2_INT	GPIO1_INT	**0x000**

Table 18: General Purpose Control

GPIO_OE[2:0] is used to configure the GPIO1, GPIO2, GPIO3 as input or output pins.

If GPIO_OE[2]=1 GPIO3 is configured as output pin.

If GPIO_OE[2]=0 GPIO3 is not configure as input or output pin. See register 0x5A[0] to configure as input pin.

If GPIO_OE[1]=1 GPIO2 is configured as output pin.

If GPIO_OE[1]=0 GPIO2 is configure as input pin.
If GPIO_OE[0]=1 GPIO1 is configured as output pin.
If GPIO_OE[0]=0 GPIO1 is configure as input pin.

GPIO_PE[2:0] is used for GPIO3, GPIO2, GPIO1 pull up/down enable. It is functional only when the GPIO is set to input pin.
GPIO_PS[2:0] is used for GPIO3, GPIO2, GPIO1 pull up/down select. If a GPIO's OE=0, PE=1, PS=1, it is weak pulled up. If a GPIO's OE=0, PE=1, PS=0, it is weak pulled down.

GPIOX_OUT_SEL[2:0] (where X=1,2,3 for GPIO1, GPIO2, GPIO3) is used as GPIO output function MUX select, when this GPIO is set as output pin.

GPIOX_OUT_SEL	GPIO Output function
000	Output 0
001	Output 1
010	Output PLL Clock
011	Output PLL Lock
100	Output MCLK_PIN
101	Output INT/INTB(note)
110	Output I2S Master FS
111	Output I2S Master BCLK

Table 19: General Purpose I/O Output Select

Note: when INT_POL=1, output INTB (low active interrupt), when INT_POL=0, output INT (high active interrupt)

GPIOX_INTE (where X=1,2,3 for GPIO1, GPIO2, GPIO3) is used as GPIO pin trigger interrupt enable.
GPIOX_INT (where X=1,2,3 for GPIO1, GPIO2, GPIO3) is used as GPIO trigger interrupt flag.

When GPIOX_INTE is 1 and GPIOX_OE=0, is a rising or falling edge happen, INT/INTB will be asserted (if one of GPIO out is set to select INT/INTB out), user should read REG0x2D (interrupt flags) to check which GPIO is generating Interrupt. Write 1 to corresponding interrupt flag bit will clear the interrupt. Then, the interrupt flag will be cleared and INT pin will be reset.

REG0x2B bit 2, bit 1, bit 0, can be read through I2C or SPI to check the status the GPIO3, GPIO2, GPIO1 input level.

11.9 Clock Generation Circuit

The PLL is fully programmable.

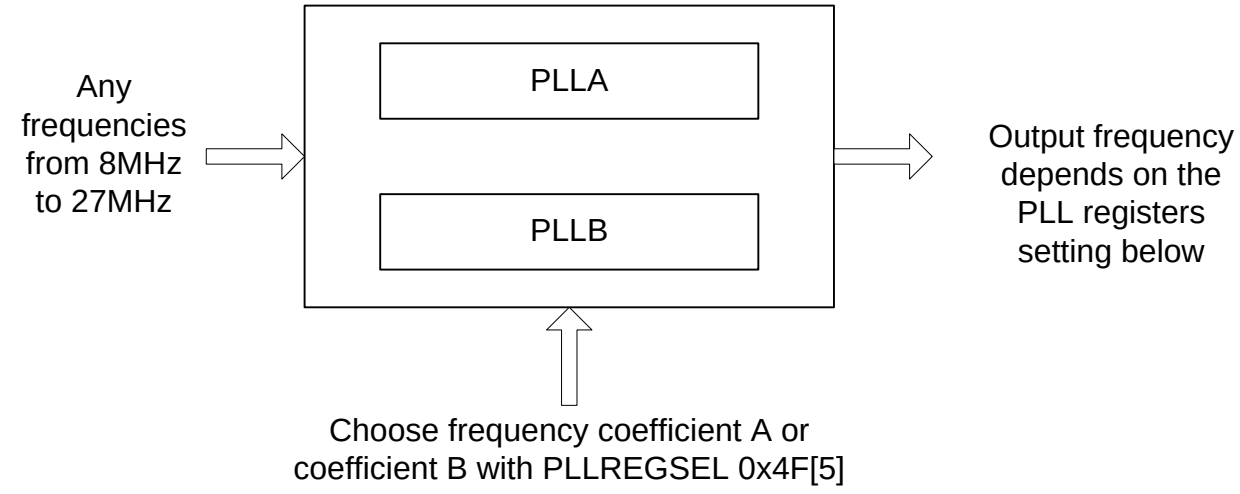
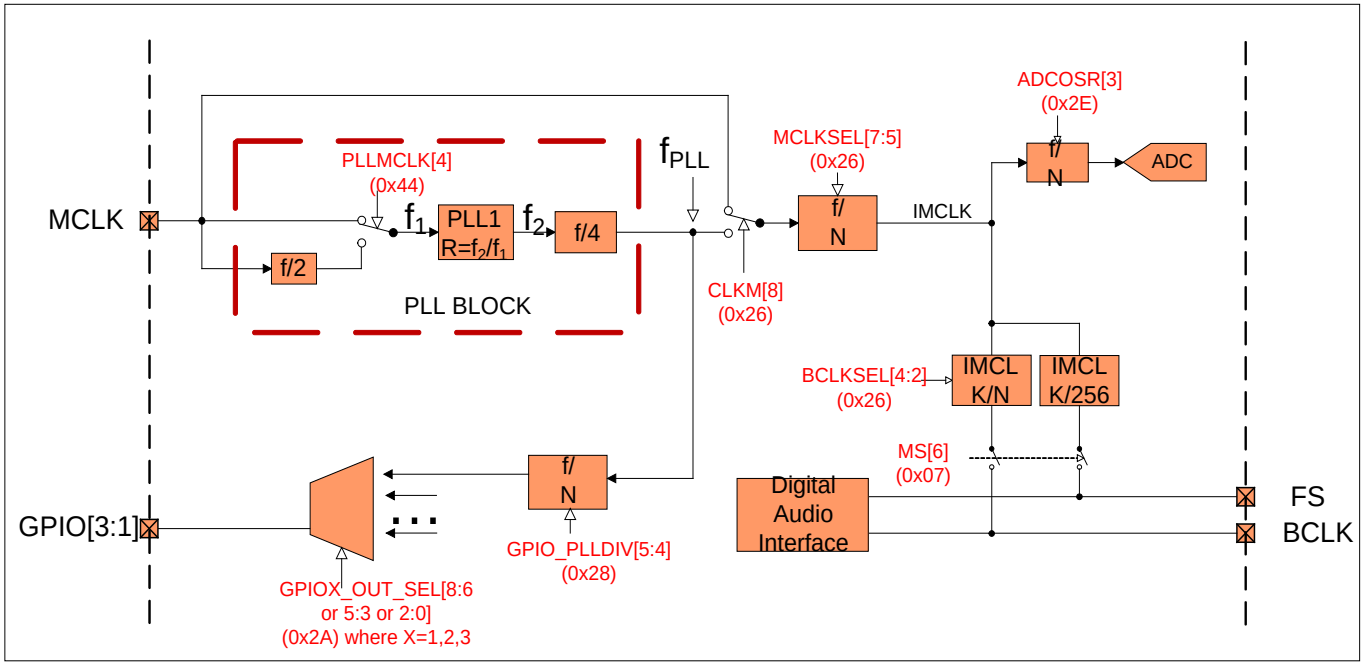


Figure 15: PLL and Clock Select Circuit



The 8502 has two clock modes that support the ADC converter. It can accept external clocks in the slave mode, or in the master mode, it can generate the required clocks from an external reference frequency using an internal PLL (Phase Locked Loop). The internal PLL is a fractional type scaling PLL, and therefore, a very wide range of external reference frequencies can be used to create accurate audio sample rates.

Separate from this ADC clock subsystem, audio data are clocked to and from the 8502 by means of the control logic described in the Digital Audio Interfaces section. The Frame Sync (FS) and Bit Clock (BCLK) pins in the Digital Audio Interface manage the audio bit rate and audio sample rate for this data flow.

It is important to understand that the Digital Audio Interface does not determine the sampling rate for the ADC data converters, and instead, this rate is derived exclusively from the Internal Master Clock (IMCLK). It is therefore a requirement that the Digital Audio Interface and data converters be operated synchronously, and that the FS, BCLK, and IMCLK signals are all derived from a common reference frequency. If these three clock signals are not synchronous, audio quality will be reduced.

The IMCLK is always exactly 256 times the sampling rate of the data converters. IMCLK is output from the Master Clock Prescaler. The prescaler reduces by an integer division factor the input frequency input clock. The source of this input frequency clock is either the external MCLK pin, or the output from the internal PLL Block.

In Master Mode, the IMCLK signal is used to generate FS and BCLK signals that are driven onto the FS and BCLK pins and input to the Digital Audio Interface. FS is always IMCLK/256 and the duty cycle of FS is automatically adjusted to be correct for the mode selected in the Digital Audio Interface. The frequency of BCLK may optionally be divided to optimize the bit clock rate for the application scenario.

In Slave Mode, there is no connection between IMCLK and the FS and BCLK pins. In this mode, FS and BCLK are strictly input pins, and it is the responsibility of the system designer to ensure that FS, BCLK, and IMCLK are synchronous and scaled appropriately for the application.

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x07		SDODIS	MS		FSP	WLEN		FORMAT		0A
0x26	CLKM	MCLKSEL[2:0]			BCLKSEL[2:0]			PLLEN		0x140
0x27						SMPLR[3:1]			SLOWCLKEN	0x000
0x44					PLLMCLK	PLLN_A[3:0]				0x008
0x45				PLLK_A[23:18]						0x00C
0x46	PLLK_A[17:9]									0x093
0x47	PLLK_A[8:0]									0x0E9
0x44				PLLREGSEL	PLLMCLK	PLLN_B[3:0]				0x008
0x45				PLLK_B[23:18]						0x00C
0x46	PLLK_B[17:9]									0x093
0x47	PLLK_B[8:0]									0x0E9

Table 20: Registers associated with PLL

11.9.1 Phase Locked Loop (PLL) General Description

The PLL may be optionally used to multiply an external input clock reference frequency by a high resolution fractional number. To enable the use of the widest possible range of external reference clocks, the PLL block includes an optional divide-by-two prescaler for the input clock, a fixed divide-by-four scaler on the PLL output, and an additional programmable integer divider that is the Master Clock Prescaler.

The high resolution fraction for the PLL is the ratio of the desired PLL oscillator frequency (f_2), and the reference frequency at the PLL input (f_1). This can be represented as $R = f_2/f_1$, with R in the form of a decimal number: xy.abcdefgh. To program the NAU8502, this value is separated into an integer portion ("xy"), and a fractional portion, "abcdefgh". The fractional portion of the multiplier is a value that when represented as a 24-bit binary number (stored in three 9-bit registers on the NAU8502), very closely matches the exact desired multiplier factor.

To keep the PLL within its optimal operating range, the integer portion of the decimal number ("xy"), must be any of the following decimal values: 6, 7, 8, 9, 10, 11, or 12. The input and output dividers outside of the PLL are often helpful to scale frequencies as needed to keep the "xy" value within the required range. Also, the optimum PLL oscillator frequency is in the range between 90MHz and 100MHz, and thus, it is best to keep f_2 within this range.

In summary, for any given design, choose:

Equations	Description	Notes
IMCLK = (256) * (desired codec sample rate)	IMCLK = desired Master Clock	
$f_2 = (4 * P * IMCLK)$	where P is the divider ratio in register MCLKSEL[7:5] optimal f_2: 90MHz< f_2 <100MHz	The integer values for D and P are chosen to keep the PLL in its optimal operating range. It may be best to assign initial values of 1 to both D and P, and then by inspection, determine if they should be a different value.
$f_1 = (MCLK / D)$	where D is the PLL Prescale factor of 1, or 2, and MCLK is the frequency at the MCLK pin	
$R = f_2 / f_1$	This is the fractional frequency multiplication factor for the PLL	
N = int(R)	Integer portion of the R value, and N is the integer element of [6, 7, 8, 9, 10, 11, 12]	
K = (2^24) * (R-N)	rounded to the nearest whole integer value and then converted to a 24-bit binary value	

Table 21: Registers associated with PLL

11.9.2 Phase Locked Loop (PLL) Design Example

In an example application, a desired sample rate for the ADC is known to be 48.000kHz. Therefore, it is also known that the IMCLK rate will be 256fs, or 12.288MHz. Because there is a fixed divide-by-four scaler on the PLL output, then the desired PLL oscillator output frequency will be 49.152MHz.

In this example system design, there is already an available 12.000MHz clock from the USB subystem. To reduce system cost, this clock will also be used for audio. Therefore, to use the 12MHz clock for audio, the desired fractional multiplier ratio would be R = 49.152/12.000 = 4.096. This value, however, does not meet the requirement that the "xy" whole number portion of the multiplier be in the inclusive range between 6 and 12. To meet the requirement, the Master

Clock Prescaler can be set for an additional divide-by-two factor. This now makes the PLL required oscillator frequency 98.304 MHz, and the improved multiplier value is now R = 98.304/12.000 = 8.192.

To complete this portion of the design example, the integer portion of the multiplier is truncated to the value 8 and the fractional portion is multiplied by 2^{24}, as to create the needed 24-bit binary fractional value. The calculation for this is: $(2^{24})(0.192) = 3221225.472$.

It is best to round this value to the nearest whole value of 3221225, or hexadecimal 0x3126E9.

Below are additional examples of results for this calculation applied to commonly available clock frequencies and desired IMCLK 256fs sample rates.

MCLK (MHz)	Desired Output (MHz)	Input Frequency (f_1)	f_2 (MHz)	MCLK Divider bits	R	N (Hex)	K (Hex)	Actual Register Setting		
								PLLK[23:18]	PLLK[17:9]	PLLK[8:0]
12.0	11.28960	MCLK/1	90.3168	$f_{PLL}/2$	7.526400	7	86C226	21	161	26
12.0	12.28800	MCLK/1	98.3040	$f_{PLL}/2$	8.192000	8	3126E9	0C	93	E9
14.4	11.28960	MCLK/1	90.3168	$f_{PLL}/2$	6.272000	6	45A1CA	11	D0	1CA
14.4	12.28800	MCLK/1	98.3040	$f_{PLL}/2$	6.826667	6	D3A06D	34	1D0	6D
19.2	11.28960	MCLK/2	90.3168	$f_{PLL}/2$	9.408000	9	6872B0	1A	39	B0
19.2	12.28800	MCLK/2	98.3040	$f_{PLL}/2$	10.240000	10	3D70A3	0F	B8	A3
19.8	11.28960	MCLK/2	90.3168	$f_{PLL}/2$	9.122909	9	1F76F8	07	1BB	F8
19.8	12.28800	MCLK/2	98.3040	$f_{PLL}/2$	9.929697	9	EE009E	3B	100	9E
24.0	11.28960	MCLK/2	90.3168	$f_{PLL}/2$	7.526400	7	86C226	21	161	26
24.0	12.28800	MCLK/2	98.3040	$f_{PLL}/2$	8.192000	8	3126E9	0C	93	E9
26.0	11.28960	MCLK/2	90.3168	$f_{PLL}/2$	6.947446	6	F28BD4	3C	145	1D4
26.0	12.28800	MCLK/2	98.3040	$f_{PLL}/2$	7.561846	7	8FD526	23	1EA	126

Table 22: PLL Frequency Examples

11.10 Serial Control Interface

The NAU8502 features two serial bus interfaces SPI and 2-Wire that provide access to the control registers. The MODE pin as shown in the following Table selects the interfaces. 2-Wire interface is compatible with other industry I^2C serial bus protocol using a bidirectional data signal (SDIO) and a clock signal (SCLK). SPI interface is also compatible with other industry interfaces allowing operation on a simple 3-wire or 4-wire bus. Table below describes the selection of the protocol modes.

REG0x69[8]	MODE Pin	Description
1	x	**SPI 4 Wire Mode (4 wire Write / Read)**
0	1	**SPI 3 Wire Mode (3 wire Write Only)**
0	0	**I2C Mode (2 wire Write / read)**

Table 23: Control Interface Selection

11.10.1 SPI Serial Control

The Serial Peripheral Interface (SPI) is one of the widely accepted communication interfaces implemented in Nuvoton's Audio CODEC portfolio. SPI is a software protocol allowing operation on a simple 3-wire or 4-wire bus where the data is transferred MSB first. NAU8502 has three different architectures a 16-bit write and a 24-bit write with 32-bit read and 16 Bit 4 wire Write/Read. The SPI interface consists of a clock (SCLK), chip select (CSb), serial data input (SDIO), and serial data output (SO Pin is ONLY on the 32-PIN QFN package) to configure all the internal register contents. SCLK is static, allowing the user to stop the clock and then start it again to resume operations where it left off.

The 24-bit write operation consists of 8-bits of device address, 7-bits of control register address, and 9-bits of data. The 32-bit read operation consists of 8-bits of device address, 8-bits of control register address, and 16-bits of data of which 9 LSB bits are actual data bits and the rest are 0's. The device address for a write operation is 00010000b = 10h and for a read is 00100000b = 20h. To set the SPI 24-bit Write and 32-bit read the Mode pin is set to "0" and FORCE_4W_SPI[8] address (0x69) is set to "1". SPI 32-bit read is only available on the QFN 32-Pin.

See below for the detail is the 16 Bit 4 wire Write and Read operation.

11.10.1.1 16-bit Write Operation (SPI 3 Wire Write)

The default control interface architecture is SPI 16-bit. This interface architecture consists of 7-bits of control register address, and 9-bits of control register data. The MODE Pin selects the SPI 16-bit. In this mode, the user can only do write operation. The write operation requires a valid control register address, then a valid 9-bit Data Byte and the finally to complete the transaction the CSb has to transition from LOW to HIGH to latch the last 9-bits (data).

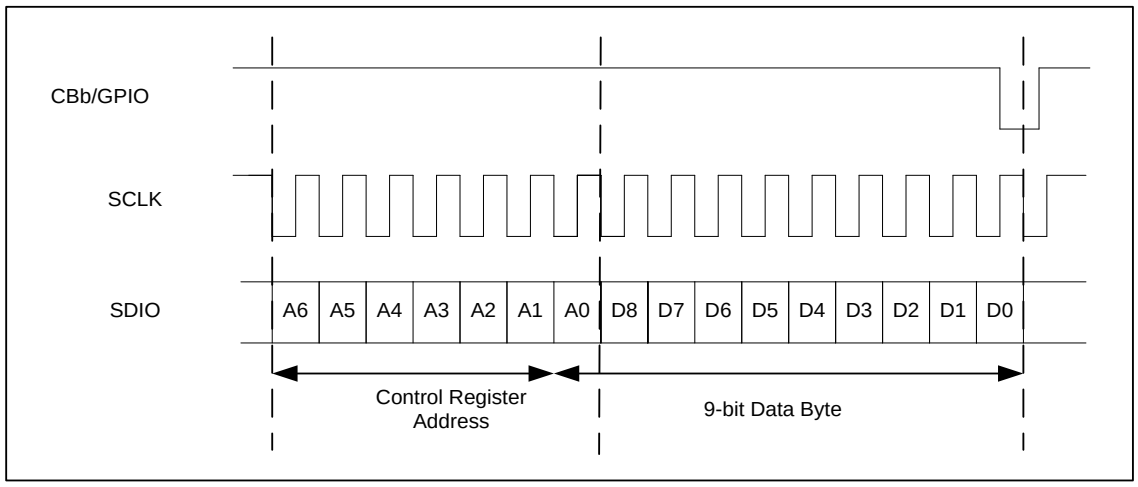


Figure 16: Register write operation using a 16-bit SPI Interface

11.10.1.2 24-bit Write Operation (SPI 4 Wire Write)

The 24-bit write operation is a three-byte operation. To start the operation the host controller transitions the CSb from HIGH to LOW. The host micro-controller sends valid device address, then a valid control register address following Data Byte. Finally the interface is terminated by toggling CSb pin from LOW to HIGH. The write operation will accept multiple 9-bit DATA blocks, which will be written in to sequential addresses beginning with the address, specified in the control register address.

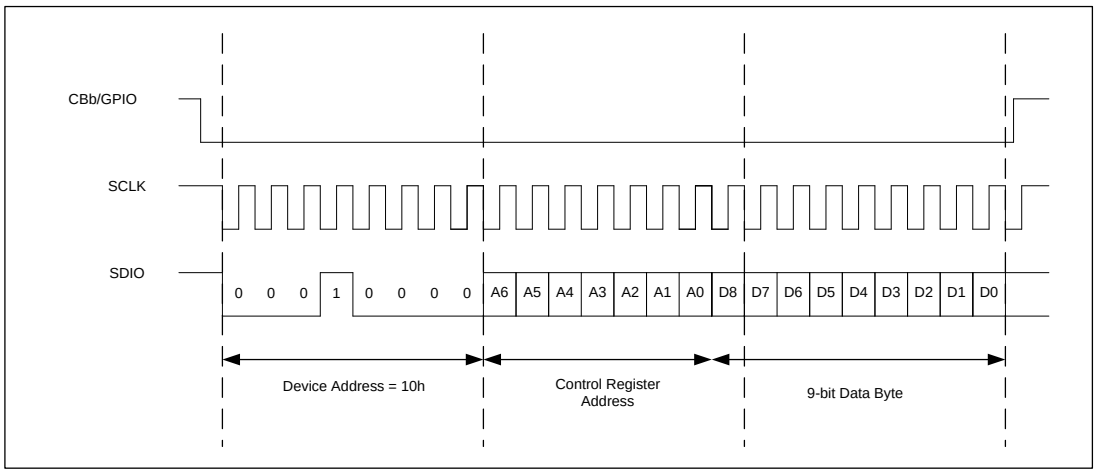


Figure 17: Register Write operation using a 24-bit SPI Interface

11.10.1.3 32-bit Read Operation (SPI 4 Wire Read)

The 32-bit read operation is a four-byte operation with 2-bytes of data. The transmission starts with the falling edge of the CSb line and ends with the rising edge of the CSb. The host micro-controller sends device address, control register address byte following 2 bytes of data. The device can receive more than one byte of data by continuously

clocking. Note after reaching the maximum address the internal pointer “rolls over” to address 0x00 (hex). The device will output a dummy byte [0x00] when locations without register assignments are within the sequence.

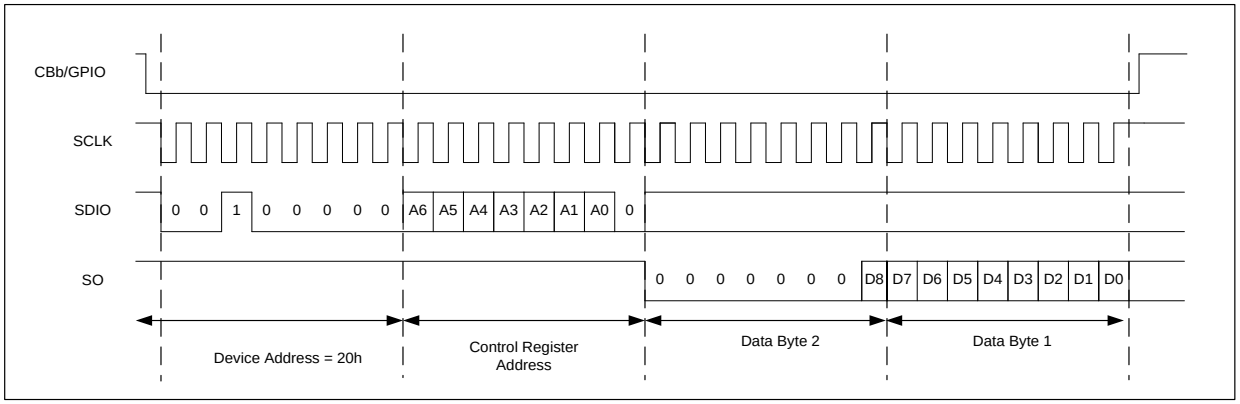


Figure 18: Register Read operation through a 32-bit SPI Interface

11.10.2 2-Wire Serial Control Mode (I2C style Interface)

The NAU8502 supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. Therefore, the 2-Wire operates as slave interface. All communication over the 2-Wire interface is conducted by sending the MSB of each byte of data first.

11.10.2.1 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH to LOW transition of SDIO while SCLK is HIGH. All 2-Wire and all interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a or write operation places the device in standby mode. An acknowledge (ACK), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

NAU8502 has two available device addresses. When CSB=0 at initial power up stage, the7 bit device address is “0011010”. When CSB=1 at initial power up stage, the7 bit device address is “1011010”.

Following a START condition, the master must output a device address byte. The 7-MSB bits are the device address. The LSB of the device address byte is the R/W bit and defines a read (R/W = 0) or write (R/W = 1) operation. When this, R/W, bit is a “1”, then a read operation is selected and when “0” the device selects a write operation. The device outputs an acknowledge LOW for a correct device address and HIGH for an incorrect device address on the SDIO pin.

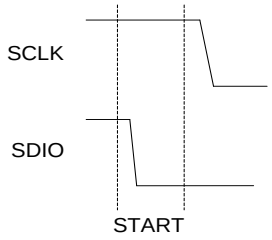


Figure 19: Valid START Condition

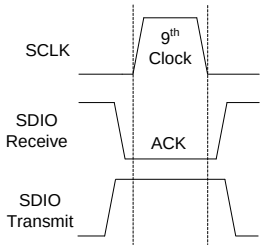


Figure 20: Valid Acknowledge

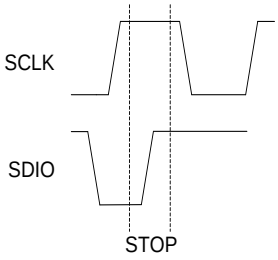


Figure 21: Valid STOP Condition

0	0	1	1	0	1	0	R/W	Device Address Byte
A6	A5	A4	A3	A2	A1	A0	Write - D8 Read - 0	Control Address Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte

Figure 22: Slave Address Byte, Control Address Byte, and Data Byte

11.10.2.2 2-WIRE Write Operation

A Write operation consists of a two-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid 7 bit device ID byte + (R/W bit=0), a valid 7 bit register address byte "REGISTER ADDRESS[6:0]" + 1 bit data for bit 8 data, data byte for bit 7 to bit 0, and a STOP condition. After each three bytes sequence, the NAU8502 responds with an ACK. If the host doesn't issue a STOP after the 9 bit register data write, the next two bytes write (first 7 bit is dummy data, only remaining 9 bit will be written to the 9 bit register), the register at "REGISTER ADDRESS[6:0] + 1" will be programmed. This is called Burst Register Write. If Burst write keep going, after reaching the memory location 7Fh the register address "rolls over" to 00h.

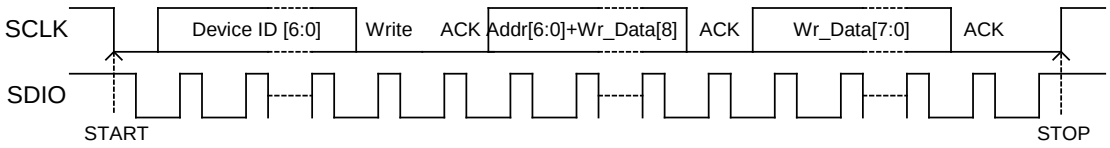


Figure 23: Write Sequence(writing 1 register)

11.10.2.3 2-WIRE Read Operation

A Read operation consists of a three-byte instruction followed by one or more Data Bytes. The master initiates the operation issuing the following sequence: a START condition, 7 bit device ID byte plus the R/W bit set to "0", a

register address byte with 7 bit register address + 1 dummy bit, a second START condition, and a second 7 bit device ID with the R/W bit set to “1”.

After each of the first three bytes, the NAU8502 responds with an ACK. Then the NAU8502 transmits Data Bytes as long as the master responds with an ACK during the SCLK cycle following the ninth bit of each byte. For the first 2 bytes read, it read the 9 bit register data at the “REGISTER ADDRESS” set at the “register address byte”, the master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte. If the master doesn’t issue STOP right after the first 2 bytes read, the next 2 bytes read will be the register data at the “REGISTER ADDRESS” + 1. This is called “Burst Register read”, the burst register read will keep going until the “STOP” condition.

If Burst read keep going, after reaching the memory location 7Fh the pointer “rolls over” to 00h, and the device continues to output data for each ACK received.

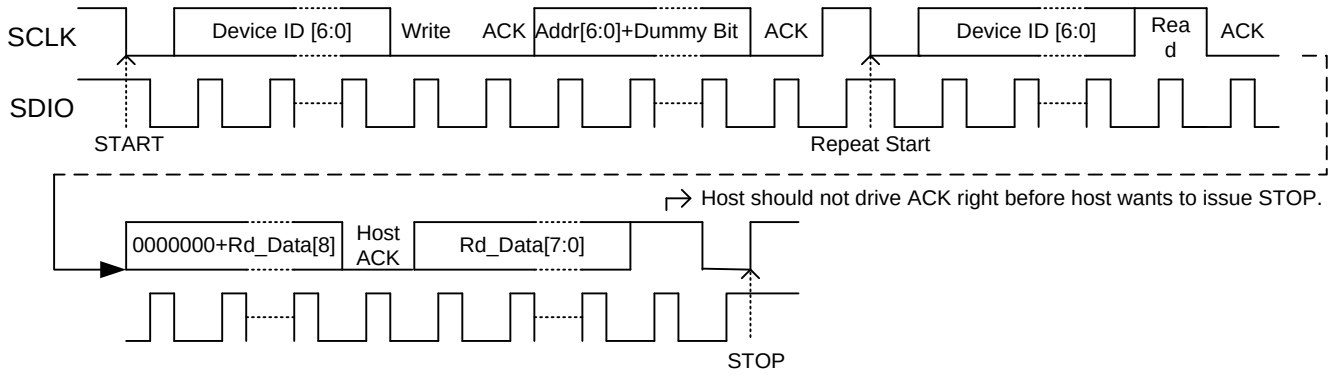


Figure 24: Read Sequence (reading 1 register)

11.11 DIGITAL AUDIO INTERFACES

NAU8502 only uses the Left and right channel to transfer data in normal mode. It supports an independent digital interface for voice and audio. The digital interface is used to output digital data from the ADC. The digital interface can be configured to Master mode or Slave mode.

Master mode is configured by setting MS[6] address (0x07) bit to HIGH. The main clock (MCLK) of the digital interface is provided from an external clock either from a crystal oscillator or from a microcontroller. With an appropriate MCLK, the device generates bit clock (BCLK) and frame sync (FS) internally in the master mode. By generating the bit clock and frame sync internally, the 8502 has full control of the data transfer.

In Master Mode, 8502 drive FS and BCLK, default Frame Sync length of 256 bit clock, it can be set to 128 / 64 / 32 bit clock per Frame Sync. 8502 also can be set to drive Frame Sync length of 192 bit clock in 16KHz sampling rate with an external Master Clock rate of 12.288MHz

Slave mode is configured by setting MS[6] address (0x07) bit to LOW. In this mode, an external controller has to supply the bit clock and the frame sync. The 8502 uses ADCOUT, FS, and BCLK pins to control the digital interface. Care needs to be exercised when designing a system to operate the 8502 in this mode as the relationship between the sample rate, bit clock, and frame sync needs to be controlled by other controller. In both modes of operation, the internal MCLK and MCLK prescalers determine the sample rate for the ADC.

The output state of the ADCOUT pin by default is Hi-Z. Depending on the application, the output can be configured to be Hi-Z, pull-low, pull-high, Low or High. See the table below.

ADCDAT_OEN_SEL Ox5C[2]	SDODIS 0x07[7]	AI 0x06[6]	ADCDAT_OEN 0x5C[5]	ADCDAT_PE 0x5C[4]	ADCDAT_PS 0x5C[3]	ADCOUT pin behavior
0	1	X	X	0	X	Hi-Z
0	1	X	X	1	1	Pull Up
0	1	X	X	1	0	Pull Down
0	0	0	X	0	X	Hi-Z
0	0	0	X	1	1	Pull Up
0	0	0	X	1	0	Pull Down
0	0	1	X	X	X	Output
1	X	X	0	0	X	Output when data transfer, Hi-Z when data transfer done
1	X	X	0	1	1	Output when data transfer, pull up when data transfer done
1	X	X	0	1	0	Output when data transfer, pull down when data transfer done
1	X	X	1	X	X	Output

Table 24: ADCOUT pin behavior selections

Six different audio formats are supported by 8502 with most significant bit first and they are as follows.

FORMAT[1] 0x07	FORMAT[0] 0x07	PCMTSEN[8] 0x5C	FSP[4] 0x07	PCM Mode
0	0	Don't care	Don't care	Right Justified
0	1	Don't care	Don't care	Left Justified
1	0	Don't care	Don't care	I^2S
1	1	0	0	PCM (DSP A)
			1	PCM (DSP B)
1	1	1	Don't care	PCM Time Slot

Table 25: Standard Interface modes

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x07		SDO DIS	MS		FSP	WLEN[3:2]		FORMAT[1:0]		0x020
0x25	BCLKP				ADC_R_MUX_SEL	ADC_L_MUX_SEL		ADCLRSWAP	MONO	0x000
0x25							ADC_COMP		U_OFFSET	0x000
0x26	CLKM	MCLKSEL[2:0]			BCLKSEL[2:0]			PLLEN		0x008
0x27						SMPLR [3:1]			SLOWCLKGEN	0x001
0x5B	TSLOTL[8:0]									0x000
0x5C	PCMTSEN	TRI	PCM8BIT	ADCDAT_OEN	ADCDAT_PE	ADCDAT_PS	ADCDAT_OEN_M	TSLOTL[9]	TSLOTR[9]	0x020
0x5D	TSLOTR[8:0]									0x020

Table 26: Audio Interface Control Registers

11.11.1 Right Justified audio data

In right justified mode, the left channel serial audio data is synchronized with the frame sync falling edge, the left channel serial audio data is synchronized with the frame sync rising edge. Left channel data is transferred during the HIGH frame sync. Right Channel data is transferred during the LOW frame sync. The MSB data is sampled first. The LSB is aligned with the falling edge of the frame sync signal (FS). Right justified format is selected by setting FORMAT[1:0] address (0x07) to “00” binary.

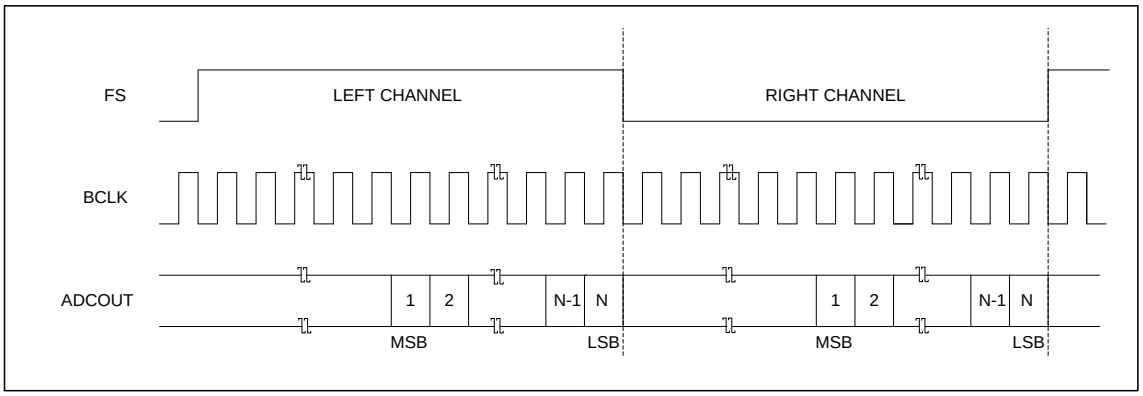


Figure 25: Right Justified Audio Interface

11.11.2 Left Justified audio data

In Left justified mode, the left channel serial audio data is synchronized with the frame sync rising edge, the right channel serial audio data is synchronized with the frame sync falling edge. Left channel data is transferred during the HIGH frame sync. Right channel data is transferred during the LOW frame sync. The MSB data is sampled first. The MSB data is latched on the first rising edge of BCLK following a frame sync transition (FS). Left justified format is selected by setting FORMAT[1:0] address (0x07) to “01” binary.

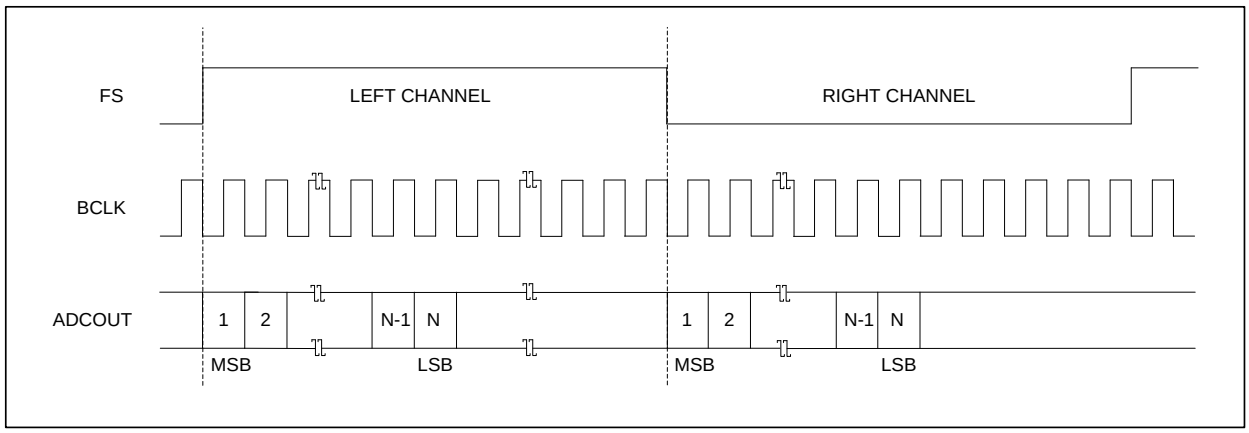


Figure 26: Left Justified Audio Interface

11.11.3 I²S audio data

In I²S mode, the left and right channel serial audio data is synchronized with the frame sync. Left channel data is transferred during the LOW frame sync. Left channel data is transferred during the HIGH frame sync. The MSB data is sampled first. The MSB data is latched on the second rising edge of BCLK following a frame sync transition (FS). I²S format is selected by setting FORMAT[1:0] address (0x07) to "10" binary.

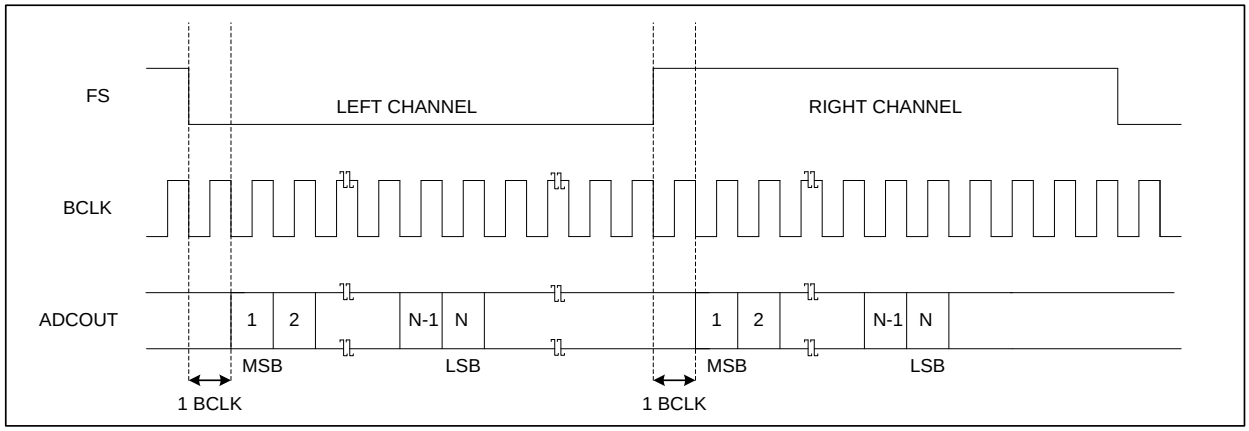


Figure 27: I2S Audio Interface

11.11.4 PCM audio data

In PCM mode, the left channel serial audio data is synchronized with the frame sync. The Left Channel MSB data is sampled first. The Left Channel MSB data is latched on the first (DSP mode B) or second (DSP mode A) rising edge of BCLK following a frame sync (FS) rising edge. PCM format is selected by setting FORMAT[1:0] address (0x07) to "11" binary in conjunction with PCMTSEN[8] address (0x5C) set to LOW. If FSP (address 0x07 bit 4)=0, this is DSP mode A, if FSP (address 0x07 bit 4)=1, this is DSP mode B

The starting point of the right phase data depends on the word length WLEN[3:2] address (0x07) after the frame sync (FS) rising edge.

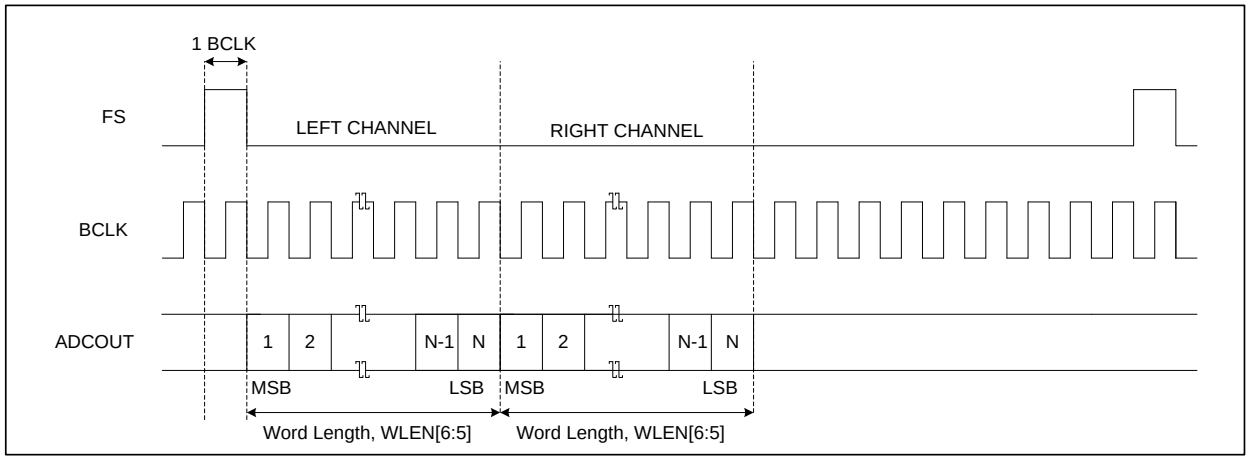


Figure 28: PCM Mode Audio Interface (Special mode)

11.11.5 PCM Time Slot audio data

PCM Time-Slot format is enabled by setting FORMAT[1:0] address (0x07) to “11” binary in conjunction with PCMTSEN[8] address (0x5C) set to HIGH.

The BCLK 0 is defined as the 1st BCLK rising edge after the rising edge FS, so the next rising edge BCLK is the BCLK 1, the Xth rising edge after the BCLK count 0 is defined as BCLK “X”

The Left Channel MSB starts from the BCLK “X” set by Registers TSLOTL[9:0]. The Right Channel MSB starts from the BCLK “Y” set by Registers TSLOTR[9:0] (Register 0x5B, 0x5C and 0x5D).

If ADCOUT will return to the bus condition either on the negative edge of BCLK during the LSB, or on the positive edge of BCLK following the LSB depending on the setting of TRI[7] address (0x5C) (ADCOUT_OE_SEl(0x5C[2]) must be 1). Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots without the risk of driver contention.

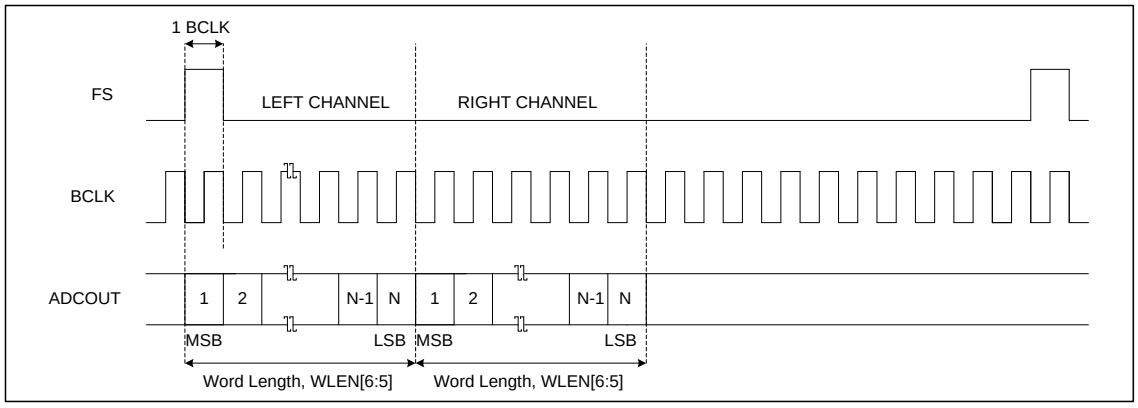


Figure 29: PCM Time Slot Mode (Time slot = 0) (Special mode)

11.11.6 Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, and make use of non-linear algorithms. NAU8502 supports two different types of companding A-law and µ-law on both transmit and receive sides. A-law algorithm is used in European communication systems and µ-law algorithm is used by North America, Japan, and Australia. This feature is enabled by setting ADC_COMP[2:1] address (0x25) register bits. Companding converts 13 bits (µ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The companded signal is an 8-bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits). As recommended by the G.711 standard (all 8-bits are inverted for µ-law, all even data bits are inverted for A-law).

Setting PCM8BIT[5] address 0x5C to 1 will cause the PCM interface to use 8-bit word length for data transfer, overriding the word length configuration setting in WLEN[3:2] address 0x07.

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x25							ADC_COMP[2:1]		U_OFFSET	**0x000**

Table 27: Companding Control

The following equations for data compression (as set out by ITU-T G.711 standard):

µ-law (where µ=255 for the U.S. and Japan):

$F(x) = \ln(1 + \mu|x|) / \ln(1 + \mu)$ $\quad -1 \le x \le 1$

A-law (where A=87.6 for Europe):

$F(x) = A|x| / (1 + \ln A)$ □□□□□□ for $x \le 1/A$

$F(x) = (1 + \ln A|x|) / (1 + \ln A)$ □□ for $1/A \le x \le 1$

11.12 POWER SUPPLY

This device has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. There are no special requirements for the sequence or rate at which the various power supply pins change. Any supply can rise or fall at any time without harm to the device. However, pops and clicks may result from some sequences. Optimum handling of hardware and software power-on and power-off sequencing is described in more detail in the Power Up/Down Sequencing section of this document.

11.12.1 Power-On Reset

The NAU8502 does not have an external reset pin. The device reset function is automatically generated internally when power supplies are too low for reliable operation. The internal reset is generated any time that either VDDA or VDDC is lower than is required for reliable maintenance of internal logic conditions. The threshold voltage for VDDA is approximately ~1.52Vdc and the threshold voltage for VDDC is approximately ~0.67Vdc. Note that these are much lower voltages than are required for normal operation of the chip. These values are mentioned here as general guidance as to overall system design.

If either VDDA or VDDC is below its respective threshold voltage, an internal reset condition may be asserted. During this time, all registers and controls are set to the hardware determined initial conditions. Software access during this time will be ignored, and any expected actions from software activity will be invalid.

When both VDDA and VDDC reach a value above their respective thresholds, an internal reset pulse is generated which extends the reset condition for an additional time. The duration of this extended reset time is approximately 50 microseconds, but not longer than 100 microseconds. The reset condition remains asserted during this time. If either VDDA or VDDC at any time becomes lower than its respective threshold voltage, a new reset condition will result. The reset condition will continue until both VDDA and VDDC again higher than their respective thresholds. After VDDA and VDDC are again both greater than their respective threshold voltage, a new reset pulse will be generated, which again will extend the reset condition for not longer than an additional 100 microseconds.

11.12.2 Power Related Software Considerations

There is no direct way for software to determine that the device is actively held in a reset condition. If there is a possibility that software could be accessing the device sooner than 100 microseconds after the VDDA and VDDC supplies are valid, the reset condition can be determined indirectly. This is accomplished by writing a value to any register other than register 0x00, with that value being different than the power-on reset initial values. The optimum choice of register for this purpose may be dependent on the system design, and it is recommended that the system engineer choose the register test bit for this purpose. After writing a value to register, a read back can be performed on the same register. When the register test bit returns the new value, instead of the power-on reset initial value, software can reliably determine that the reset condition has ended.

Although it is not required, it is strongly recommended that a Software Reset command should be issued after power-on and after the power-on-reset condition is ended. This will help ensure reliable operation under every power sequencing condition that could occur.

11.12.3 Software Reset

The control registers can be reset to default conditions by writing 0x000 (TBC) to SoftwareReset[8:0] address (0x0F), using any of the control interface modes. Writing valid data to any other register disables the reset, but all registers will need to be initiated again appropriate to the operation. See the applications section on powering NAU8502 up for information on avoiding pops and clicks after a software reset.

11.12.4 Power Up/Down Sequencing

Most audio products have issues during power up and power down in the form of pop and click noise. To avoid such issues the NAU8502 provides three different power supplies VDDA, VDDB and VDDC with separated grounds VSSA1 VSSA2, VSSD. The audio CODEC circuitry, the input amplifiers, output amplifiers and drivers, the audio ADC converter, the PLL, and so on, can be powered up and down individually by software control via 2-Wire or SPI interface. The zero cross function should be used when changing the volume in the PGAs to avoid any audible pops or clicks. The recommended power-up and power-down sequences for both the modes are outlined as following.

	Power Up
Name	VDDSPK - 3.3V operation
Power supplies	Analog – VDDA
	Buffer - VDDB
	Digital – VDDC
Power Management	VMID[8] and VMIDSEL[3:2] as required (value of the REFIMP bits based on the startup time which is a combination of the reference impedance and the decoupling capacitor on VREF)
	BIASEN[3] = 1 (enables the internal device bias for all analog blocks)
	BUFIOEN[2] = 1 (enables the internal device bias buffer)
Clock divider	MS[6] if required
	BCLKSEL[4:2] if required
	MCLKSEL[7:5] if required
PLL	PLLEN[5] if required
PGA 1st stage Left	LMBE[4] = 1
PGA 1st stage Right	RMBE[4] = 1
PGA 2nd stage Left	PGL[5] = 1

	Power Up
Name	VDDSPK - 3.3V operation
PGA 2nd stage Right	PGR[4] = 1
ADC Left	ADL[3] = 1
ADC Right	ADR[2] = 1

Table 28: Power up sequence

Name	Power Down Both Cases
Power Management	0x02[4] = 0x000 0x03[4] = 0x000 0x06 = 0x080 0x0A = 0x000 0x21 = 0x000 0x26[1] = 0x000
Power supplies	Analog – VDDA
	Buffer - VDDB
	Digital – VDDC

Table 29: Power down Sequence

11.12.5 Reference Impedance (REFIMP) and Analog Bias

Before the device is functional or any of the individual analog blocks are enabled VMID[8] address (0x06), VMIDSEL[3:2] address (0x0A) and BIASEN[3] address (0x21) must be set. The VMIDSEL[3:2] bits control the resistor values (“R” in Figure 5) that generates the mid supply reference, VMID. VMIDSEL[3:2] bits control the power up ramp rate in conjunction with the external decoupling capacitor. A small value of “R” allows fast ramp up of the mid supply reference and a large value of “R” provides higher PSRR of the mid supply reference.

The master analog biasing of the device is enabled by setting BIASEN[3] address (0x21). This bit has to be set before for the device to function. The VMID reference block must be enabled by setting VMID[8] address (0x06).

11.12.6 Power Saving

Saving power is one of the critical features in a semiconductor device specially ones used in the Bluetooth headsets and handheld device. NAU8502 has two oversampling rates 64x and 128x. The default mode of operation for the ADC is in 128x oversampling mode which is set by programming ADCOSR[3] address (0x2E) respectively to HIGH. Power is saved by choosing 64x oversampling rate compared to 128x oversampling rate but slightly degrades the noise performance. To reach lowest power possible after the device is functioning set BIASEN[3] address (0x21) bit to LOW.

The ADC current can be further reduced by setting HALF_BIAS_ADC_buffer[7] address (0x5A) to high. This setting is not recommended at high sample rates.
Also the device master bias can be scaled using MBCTRL[1:0] address (0x09).

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x09								MBCTRL		0x000
0x21						BIASEN	BUFIOEN			0x000
0x2E		HPFAPP	HPFCUT			ADCOSR				0x000
0x5A	PGA_stage2_bias	HALF_BIAS_ADC_buffer				TRIM_REGULATOR_SV				0x000

Table 30: Registers associated with Power Saving

11.12.7 Estimated Supply Currents

NAU8502 can be programmed to enable or disable various analog blocks individually. The table below shows the amount of current consumed by certain analog blocks. Sample rate settings will vary current consumption of the VDDC supply. VDDC consumes approximately 4mA with VDDC = 1.8V and fs = 48kHz. Lower sampling rates will draw lower current.

BIT	Address	VDDA CURRENT
VMID[8]	0x06	5.6K => 600 uA 161k/595k < 100 uA
VMIDSEL[1:0]	0x0A	5.6K => 600 uA 161k/595k < 100 uA
BUFIOEN[2]	0x21	100 uA
BIASEN[3]	0x21	300 uA
MICBIAS[1:0]	0x06	500 uA
PLLEN[5]	0x26	1.4 mA Clocks Applied
ADL[3]	0x06	x64 --- 2.6mA ADCOSR= 0 =>lower current x128--- 4.9mA ADCOSR= 1 =>higher curren
ADR[2]	0x06	x64---2,6mA ADCOSR= 0 =>lower current x128---4.9mA ADCOSR= 1 =>higher curren
PGL[5]	0x06	200 uA
PGR[4]	0x06	200 uA
LMBE[4]	0x02	200 uA
RMBE[4]	0x03	200 uA

Table 31: VDDA 3.3V Supply Current

12 REGISTER DESCRIPTION

There are two dedicated register spaces:

- 8737 space 0x00 to 0x0F and 0x1C
- NAU8502 space from 0x21 and on

The NAU8502 register map have a reserved space from register 0x00 to register 0x0F and 0x1C that mimic the 8737 registers.. Programming in this address space [0x00-0x0F:0x1C] will trigger the appropriate functions in the NAU8502 via mapping.

Register Address		Register Bits									Default
DEC	HEX	D8	D7	D6	D5	D4	D3	D2	D1	D0	
		PGA volume									
0	0	LVU	LINVOL								C3
1	1	RVU	RINVOL								C3
		Audio path									
2	2			LMICBOOST		LMBE	LMZC	LPZC			07
3	3			RMICBOOST		RMBE	RMZC	RPZC			07
		3D									
4	4										00
		ADC control									
5	5			POLARITY			0	LP		ADC HPD	00
		Power Management									
6	6	VMID	VREF	AI	PGL	PGR	ADL	ADR	MICBIAS		80
		Audio Format and clocking									
7	7		SDODIS	MS		FSP	WLEN		FORMAT		0A
8	8			CLKDIV2	SR						00
		Mic pre-amp and bias									
9	9								MBCTRL		0F
10	A						VMIDSEL		LIN DC EN	RIN DC EN	03
		Noise gate and ALC									
11	B		ALCMINGAIN			NGTH				NGAT	00
12	C	ALCEN		ALCMAXGAIN			ALCSL				7C
13	D				ALCMODE	ALCZCE	HLD				00
14	E		DCY				ATK				32
		Reset									
15	F	Software Reset									00
16	10										
17	11										
18	12										
19	13										
20	14										
21	15										
22	16										
23	17										
24	18										
25	19										
26	1A										
27	1B										
28	1C										4
29	1D										
30	1E										
31	1F										
32	20										
		Power management									
33	21						BIASEN	BUFIOEN			00
		Audio path selection									
34	22	LLINOUTEN	RLINOUTEN	SLEEP	VINSEL				LMICN2BVREF	RMICN2BVREF	00
Register Address		Register Bits									Default
DEC	HEX	D8	D7	D6	D5	D4	D3	D2	D1	D0	
35	23						LINEOUTSELL		LINEOUTSELR		00
		Audio format and clocking									
36	24	BCLKP				ADC_R_MUX_SEL	ADC_L_MUX_SEL		ADCLRSWAP	MONO	00
37	25							ADC_COMP		U_OFFSET	
38	26	CLKM	MCLKSEL			BCLKSEL			PLLEN		08
39	27						SMPLR			SLOWCLKEN	01
		GPIO									

40	28	RAM_TEST_START	RAM_TEST_FINISH	RAM_TEST_FAIL	GPIO_PLLDIV						**00**
41	29	GPIO_PS			GPIO_PE			GPIO_OE			**00**
42	2A	GPIO3_OUT_SEL			GPIO2_OUT_SEL			GPIO1_OUT_SEL			**00**
		GPIO interrupt									
43	2B							GPIO3_IN	GPIO2_IN	GPIO1_IN	RO
44	2C		POL			clip2_INTE	clip1_INTE	GPIO3_INTE	GPIO2_INTE	GPIO1_INTE	180
45	2D					clip2_INT	clip1_INT	GPIO3_INT	GPIO2_INT	GPIO1_INT	00
		ADC additional control									
46	2E		HPFAPP	HPFCUT			ADCOSR				**08**
47	2F	ADCVU	ADCVOLL								**ff**
48	30	ADCVU	ADCVOLR								**ff**
49	31										
		Equalizer									
50	32		EQ1BW	EQ1C	EQ1G						12C
51	33	EQ2BW		EQ2C	EQ2G						2C
52	34	EQ3BW		EQ3C	EQ3G						2C
53	35	EQ4BW		EQ4C	EQ4G						2C
54	36	EQ5BW		EQ5C	EQ5G						2C
		Analog test mode									
55	37	ANA_TEST									**00**
56	38										
57	39										
58	3A										
		Notch filter									
59	3B	NFU	NFEN	NFA0[13:7]							**00**
60	3C	NFU		NFA0[6:0]							**00**
61	3D	NFU		NFA1[13:7]							**00**
62	3E	NFU		NFA1[6:0]							**00**
63	3F										
64	40										
65	41										
66	42										
67	43										
		PLL registerA									
68	44					PLLMCLK	PLLN_A				**08**
69	45				PLLK_A[23:18]						**0C**
70	46	PLLK_A[17:9]									**93**
71	47	PLLK_A[8:0]									**E9**
72	48										
73	49										
74	4A										
		Audio path selection									
75	4B			LMIC2_2INPPGA2	LMICN2INPPGA2			LMIC2_2INPPGA1	LMICN2INPPGA1	LMICP2INPPGA	**00**
76	4C			RMIC2_2INPPGA2	RMICN2INPPGA2			RMIC2_2INPPGA1	RMICN2INPPGA1	RMICP2INPPGA	**00**
77	4D			LMBMUTE	INPPGALVOL						**00**
78	4E			RMBMUTE	INPPGARVOL						**00**
		PLL registerB									
79	4F				PLLREGSEL	PLLMCLK	PLLN_B				**08**
80	50				PLLK_B[23:18]						**0C**
81	51	PLLK_B[17:9]									**93**
Register Address		**Register Bits**									**Default**
DEC	**HEX**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	
82	52	PLLK_B[8:0]									**E9**
83	53										
84	54										
85	55										
86	56										
87	57										

88	58										
		ADC mixer									
89	59				MixerMap_ADC2				MixerMap_ADC1		**21**
		Power management and additional GPIO3 control input enable									
90	5A	PGA_stage2_bias	HALF_BIAS_ADC_buffer	HALF_BIAS_SPARES		MCBSMODE	TRIM_REGULATOR_SV			GPIO3_IE	**00**
		PCM and time slot									
91	5B	TSLOTL[8:0]									**00**
92	5C	PCMTSEN	TRI	PCM8BIT	ADCDAT_OEN	ADCDAT_PE	ADCDAT_PS	ADCDAT_OEN_SEL	TSLOTR[9]	TSLOTL[9]	**20**
93	5D	TSLOTR[8:0]									**20**
		ID register									
94	5E		REG_SI_REV								**FD**
95	5F			I2C_DEVID							**1B/1A**
96	60		Additional nuvoton ID								**CA**
97	61										
98	62										
99	63										
100	64										
101	65										
		ALC interrupt features									
102	66	ALCTABLESEL	ALCPKSEL	ALCNGSEL	ALCGAIN_L						**10**
103	67	ALCPKLIMENn	PK_DET_CLR	PK_DET_HOLD	ALCGAIN_R						**10**
		Additional ADC equalizer registers									
104	68	LATCH_DLY		SWAP_DM_DFE	EN_DIG_MIC_R	EN_DIG_MIC_L	DM_DS	ALCGRP	EQON_TEST	SKIP_DLY	**06**
		Additional register SPI and notch filter									
105	69	FORCE_4W_SPI		FLUSH_ON_ERR	IDSEL_MODE	NOTCH_DLY_DIS		PLLOCK_BP			**00**
		Tie-Off control VMID									
106	6A	MANU_IN_CTRL									**00**
107	6B							MANU_VMID_CTRL			**00**
		AGC readout									
108	6C	P2P_OUT_L									**RO**
109	6D	P2P_OUT_R									**RO**
110	6E	PEAK_OUT_L									**RO**
111	6F	PEAK_OUT_R									**RO**
112	70				NOISE_OUT_R	NOISE_OUT_L			FAST_DEC_L	FAST_DEC_R	**RO**
		Tie-Off control buffer VMID									
113	71	REGENABLE		SHORTBUFL	Tie-off buffered VREF						**00**

12.1 REGISTERS 0X00 0X01 2ND STAGE PGA GAIN

The registers set the gain of the PGA stage 2. The settings are mapped to the register 0x4D and 0x4E for a complete range: -12dB to +35.25dB in 0.75dB gain steps.

Bit(s)	Addr	Parameter	Function
[8]	0x00	LVU	Volume update, setting this bit to one will update the gain
[8]	0x01	LVU	Volume update, setting this bit to one will update the gain
[7:0] map to 0x4D[5:0]	0x00	LINVOL	Set the gain from -12dB to 35.25dB
[7:0] map to 0x4E[5:0]	0x01	RINVOL	Set the gain from -12dB to 35.25dB

Note: The register settings in LINVOL and RINVOL will take effect only when the MCLK is present

The table below describes the mapping between registers 0x00/0x01 and 0x4D/0x4E. It shows that the NAU8502 can adjust the gain on the second stage PGA from -12dB to +35.25dB if the register 0x4D and 0x4E are programmed.

However for dedicated gain setting like MUTE, +4dB and +29.5dB the user can program the register 0x00 and 0x01 the same it is done on the 8737 and the gain will mapped within 0.5dB.

0x00[7:0] 0x01[7:0]		**0x4D[5:0] 0x4E[5:0]**	
Settings (decimal)	8737 Gain [dB]	Settings (decimal)	Effective Gain [dB]
0	MUTE	Assert INPPGAMUTE	--
1 to 171	-97 to -12	0	-12
172	-11.5	1	-11.25
173	-11	2	-10.5
…	…	…	…
194	-0.5	16	0
…	…	…	…
203	4	22	4.5
…	…	…	…
254	29.5	56	30

12.2 REGISTERS 0X02 0X03 AUDIO PATH

The registers set the gain, enable the first stage PGA and enable/disable the zero crossing functions.

Bit(s)	Addr	Parameter	Function
[6:5]	0x02	LMICBOOST	Set the gain 00 = +13dB 01 = +18dB 10 = +28dB 11 = +33dB
[4]	0x02	LMBE	Left (channel 1) 0: Disable PGA 1st stage 1: Enable PGA 1st stage
[6:5]	0x03	RMICBOOST	Set the gain 00 = +13dB 01 = +18dB 10 = +28dB 11 = +33dB
[4]	0x03	RMBE	Right (channel 2) 0: Disable PGA 1st stage 1: Enable PGA 1st stage

12.3 REGISTER 0X04

Not supported.

12.4 REGISTER 0X05 ADC

Bit(s)	Addr	Parameter	Function
[6:5]	0x05	POLARITY	00 no inversion on ADC data 01 Left (1) inverted 10 Right (2) inverted 11 both inverted
[2]	0x05	LP	1 reduces ADC current by half 0 nominal ADC current
[0]	0x05	ADCHPD	1 disable ADC high pass filter 0 enable

12.5 REGISTER 0X06 POWER MANAGEMENT

Bit(s)	Addr	Parameter	Function
[8]	0x06	VMID	0 VMID reference turned off 1 VMID reference turned on
[7]	0x06	VREF	0 VREF buffer turned on 1 VREF buffer turned off
[6]	0x06	AI	0 audio interface off 1 audio interface on
[5]	0x06	PGL	0 pga 2nd stage off 1 pga 2nd stage on
[4]	0x06	PGR	0 pga 2nd stage off 1 pga 2nd stage on

[3]	0x06	ADL	0 ADC off 1 ADC on
[2]	0x06	ADR	0 ADC off 1 ADC on
[1:0]	0x06	MICBIAS (if MICBMODE = 0)	00 off 01 0.75*VDDA 10 0.9*VDDA 11 0.5*VDDA

Note: The register setting in ADL and ADR will take effect only when the MCLK is present

ADL/ADR mapping

When the ADCs are enabled by setting ADL or ADR high, a corresponding set of registers in the NAU8502 space are simultaneously and automatically configured. These registers may be overwritten at their locations in the NAU8502 space, and the most recent configuration will take effect. The mapped register values from ADL/ADR to NAU8502 space may be read from the NAU8502 space, but the mapping is uni-directional; writes in the NAU8502 space will not be reflected or mapped back to any overwrites of the 8737 space.

When either ADL or ADR are set high, the following register changes are made in NAU8502 space:

- BIASEN (0x21[3]) is enabled high
- BUFIOEN (0x21[2]) is enabled high
- L/RMICP2INPPGA (0x4B[0], 0x4C[0] are enabled high (corresponding to left and/or right channel ADL/ADR)
- L/RMICN2BVREF (0x22[1:0]) are enabled high (corresponding to left and/or right channel ADL/ADR)
- L/RMIC2_2INPPGA2 (0x4B[6], 0x4C[6]) are enabled high (corresponding to left and/or right channel ADL/ADR)
- L/RMICN2INPPGA1 (0x4B[1], 0x4C[1]) are disabled low
- L/RMIC2_2INPPGA1 (0x4B[2], 0x4C[2]) are disabled low
- L/RMICN2INPPGA2 (0x4B[5], 0x4C[5]) are disabled low

When ADL or ADR are subsequently cleared, L/RMICN2BVREF and L/RMIC2_2INPPGA2 are cleared along with other path selection bits, and BIASEN/BUFIOEN are set to the value at address 0x21.

12.6 REGISTER 0X07 AUDIO FORMAT AND CLOCKING

Bit(s)	Addr	Parameter	Function
[7]	0x07	ADCOUTDIS	Controls ADCOUT enable 0 ADCOUT enable 1 ADCOUT disable ADCDAT_OE_SEL 0x5C[2] must be set to 0 first
[6]	0x07	MS	0 Slave PCM bus 1 Master PCM bus
[4]	0x07	FSP	0 frame sync clock non inverted 1 frame sync clock inverted (this bit is not applicable to FORMAT=11)
[3:2]	0x07	WLEN	00 16 bits 01 20 bits 10 24 bits 11 32 bits (set to 24 bit if FORMAT=00 Right Justified)
[1:0]	0x07	FORMAT	00 Right justified 01 Left justified 10 I2S mode 11 DSP mode A when FSP (0x07[4]) = 0, DSP mode B when FSP (0x07[4]) = 1

12.7 REGISTER 0X08 AUDIO FORMAT AND CLOCKING

Bit(s)	Addr	Parameter	Function
[6]	0x08	CLKDIV2	0 Master clock not divided by 2 1 Master clock divided by 2
[5:1] mapped to 0x27[3:1]	0x08	SR	Sample rates supported are: MCLK=12.288MHz 00100 8KHz 01000 12KHz 01010 16KHZ 11100 24KHZ 01100 32KHZ 00000 48KHZ MCLK=11.2896MHz 11000 11.025KHz 11010 22.05KHz 10000 44.1KHz

Sample Rate register mapping

The SR (0x08[5:1]) and CLKDIV2 (0x08[6]) register bits map to the MCLKSEL (0x26[7:5]), BCLKSEL (0x26[4:2]), and SMPLR (0x27[3:1]) registers in NAU8502 space as in the following table:

MCLK		SR	MCLKSEL	BCLKSEL	SMPLR
CLKDIV2=0	CLKDIV2=1				
12.288 MHz	24.576 MHz	00100	101 (6)	010 (4)	101 (8k)
		01000	100 (4)	010 (4)	100 (12k)
		01010	011 (3)	110 (192 BCLK per FS)	011 (16k)
		11100	010 (2)	010 (4)	010 (24k)
		01100	001 (1.5)	010 (4)	001 (32k)
		00000	000 (1)	010 (4)	000 (48k)

12.8 REGISTER 0X09 ANALOG POWER CONTROL

Bit(s)	Addr	Parameter	Function
[1:0]	0x09	MBCTRL	Master bias current setting 00 125% 01 85% 10 75% 11 nominal 100%

12.9 REGISTER 0X0A VMID IMPEDANCE AND INPUT IMPEDANCE SELECTION

Bit(s)	Addr	Parameter	Function
[3:2]	0x0A	VMIDSEL	VMID impedance selection 00 80K 01 300K 10 2.5K 11 reserved
[1]	0x0A	LDC	0 500K disconnected from MIC1P 1 500K connected from MIC1P
[0]	0x0A	RDC	0 500K disconnected from MIC2P 1 500K connected from MIC2P

12.10 REGISTER 0X0B NOISE GATE AND ALC

Bit(s)	Addr	Parameter	Function
[7:5]	0x0B	ALCMINGAIN	Minimum level for ALC operation 0 = -12dB 1 = -6dB 2 = 0dB 3 = +6dB … 7 = +30dB
[4:2]	0x0B	NGATH	Noise gate threshold 000 = -78dB 001 = -72dB 010 = -66dB 011 = -60dB 100 = -54dB 101 = -48dB 110 = -42dB 111 = -30dB
[0]	0x0B	NGAT	0 Noise gate disabled 1 Noise gate enabled

12.11 REGISTER 0X0C ALC

Bit(s)	Addr	Parameter	Function
[8:7]	0x0C	ALCEN	00 = ALC disabled 01 = Right channel ALC enabled 10 = Left channel ALC enabled 11 = Both channels ALC enabled
[6:4]	0x0C	ALCMAXGAIN	Maximum level for ALC operation 0 = -6.75 dB 1 = -.75 dB 2 = +5.25 dB 3 = +11.25 dB … 7 = +35.25 dB
[3:0]	0x0C	ALCSL	ALC target level ALCTABLESEL (0x66.8) = 0 0 = -28.5 dB 1 = -27 dB 2 = -25.5 dB

			… 14 = -7.5 dB 15 = -6 dB ALCTABLESEL (0x66.8) = 1 0 = -22.5 dB 1 = -21 dB 2 = -19.5 dB … 13 = -3 dB 14 = -1.5 dB 15 = -1.5 dB

12.12 REGISTER 0X0D ALC

Bit(s)	Addr	Parameter	Function
[5]	0x0D	ALCMODE	0 = ALC normal operation mode 1 = ALC limiter mode.
[4]	0x0D	ALCZCE	ALC zero cross enable 0 = zero crossing disabled 1 = zero crossing enabled
[3:0]	0x0D	HLD	Range: 0ms to 1s, time doubles with every step)

12.13 REGISTER 0X0E ALC

Bit(s)	Addr	Parameter	Function
[7:4]	0x0E	DCY	ALC decay time ALCMODE=0 Range: 500us to 512ms ALCMODE=1 Range: 125us to 128ms (Both ALC time doubles with every step) Note: parameters refer to time to update one 0.75 dB step
[3:0]	0x0E	ATK	ALC attack time ALCMODE=0 Range: 125us to 128ms ALCMODE=1 Range: 31us to 32ms (time doubles with every step) Note: parameters refer to time to update one 0.75 dB step

12.14 REGISTER 0X0F RESET

Bit(s)	Addr	Parameter	Function
[8:0]	0x0F	Software Reset	Program 0x000 to reset the registers

12.15 REGISTER 0X1C

Natively supported, the maximum ADC code is 0x7FFFFF

12.16 Register 0x21 Additional power management registers (note: write-only)

Bit(s)	Addr	Parameter	Function
[3]	0x21	BIASEN	Register turning on the remaining of the analog circuitry like band gap and references 0 disable 1 enable
[2]	0x21	BUFIOEN	Buffer enable for tie-off connections 0 disable 1 enable

12.17 Register 0x22 Additional audio path registers

Bit(s)	Addr	Parameter	Function
[8]	0x22	LLINOUTEN	Not used
[7]	0x22	RLINOUTEN	Not used
[6]	0x22	SLEEP	Stops the clock, same as PLLEN 0x26[2]
[5]	0x22	VINSEL	Not used
[1]	0x22	LMICN2BVREF	Connect MIC1N to reference for single ended operation
[0]	0x22	RMICN2BVREF	Connect MIC2N to reference for single ended operation

12.18 Register 0x23 Additional audio path registers

Bit(s)	Addr	Parameter	Function
[3:2]	0x23	LINOUTSELL	Mix the ADC input signal to LLINOUT pin 00 none 01 ADC signal left only 10 ADC signal right only 11 both ADC signal
[1:0]	0x23	LINOUTSELR	Mix the ADC input signal to RLINOUT pin 00 none 01 ADC signal left only 10 ADC signal right only 11 both ADC signal

12.19 Register 0x24 Left and Right channel select for ADCOUT

Bit(s)	Addr	Parameter	Function
[8]	0x24	BCLKP	BCLK polarity 0 = non-inverted BCLK 1 = inverted BCLK
[4]	0x24	ADC_R_MUX_SEL	0 = output Right Channel Data on Right Channel ADCOUT 1 = output Left Channel Data on Right Channel ADCOUT
[3]	0x24	ADC_L_MUX_SEL	0 = output Left Channel Data on Left Channel ADCOUT

			1 = output Right Channel Data on Left Channel ADCOUT
[1]	0x24	ADCLRSWAP	0 = no swap between the Left and Right Channel ADCOUT 1 = swap the Left and Right Channel ADCOUT
[0]	0x24	MONO	Select audio data on one channel only 0 = both channel ADCOUT 1 = only Left channel ADCOUT if ADCLRSWAP=0 or only Right channel ADCOUT if ADCLRSWAP=1

12.20 REGISTER 0X25 AUDIO FORMAT AND CLOCKING

Bit(s)	Addr	Parameter	Function
[2:1]	0x25	ADC_COMP	ADC Companding Select 00 linear 01 reserved 10 Mu-law 11 A-law
[0]	0x25	U_OFFSET	Mu-law 0 = input offset by 32 1 = input offset by 33

12.21 REGISTER 0X26 CLOCK SOURCE AND DIVISION SELECT AND PLL ENABLE

Bit(s)	Addr	Parameter	Function
[8]	0x26	CLKM	0 PLL is bypassed 1 PLL is used for MCLK
[7:5]	0x26	MCLKSEL	Scale the MCLK or PLL ouput clock 000 = divide by 1 001 = divide by 1.5 010 = divide by 2.0 011 = divide by 3 100 = divide by 4 101 = divide by 6 110 = divide by 8 111 = divide by 12
[4:2]	0x26	BCLKSEL	Scale the bclk output frequency when used as master. 000 = divide by 1 001 = divide by 2 010 = divide by 4 011 = divide by 8 100 = divide by 16 101 = divide by 32 110 = reserved 111 = reserved
[1]	0x26	PLLEN	0 PLL off 1 PLL on

12.22 REGISTER 0X27 AUDIO FORMAT AND CLOCKING

Bit(s)	Addr	Parameter	Function
[3:1]	0x27	SMPLR	Direct sample rate selection 000 = 48 kHz 001 = 32 kHz 010 = 24 kHz 011 = 16 kHz 100 = 12 kHz

			101 = 8 kHz 110 = reserved 111 = reserved
[0]	0x27	SLOWCLKGEN	0 = Slow clock disabled 1 = Slow clock enabled. Slow clock needs to be enabled when zero crossing is enabled. When zero crossing is enabled in the 8737 address space, this register is automatically set.

12.23 REGISTER 0X28 RAM

Bit(s)	Addr	Parameter	Function
[8]	0x28	RAM_TEST_START	RAM test start control
[7]	0x28	RAM_TEST_FINISH	RAM test finished status flag
[6]	0x28	RAM_TEST_FAIL	RAM test failed status flag
[5:4]	0x28	GPIO_PLLDIV	Scaled PLL output clock 00 = divide by 1 01 = divide by 2 10 = divide by 3 11 = divide by 4

12.24 REGISTER 0X29 GPIO

Bit(s)	Addr	Parameter	Function
[8:6]	0x29	GPIO_PS	GPIO pull select enable 000 pull low 111 pull high
[5:3]	0x29	GPIO_PE	GPIO pull enable 000 tri-stated input 111 pull enabled
[2:0]	0x29	GPIO_OE	GPIO output enable x00 disabled 111 enabled

If GPIO_OE[2]=0 GPIO3 is not configure as input or output pin. See register 0x5A[0] to configure as input pin.

12.25 REGISTER 0X2A GPIO

Bit(s)	Addr	Parameter	Function
[8:6]	0x2A	GPIO3_OUT_SEL	GPIO output selection 000 = 0 001 = 1 010 = PLL clock 011 = PLL lock 100 = MCLK_PIN 101 = Interrupt 110 = Master FS 111 = Master BCLK
[5:3]	0x2A	GPIO2_OUT_SEL	GPIO output selection Same as above
[2:0]	0x2A	GPIO1_OUT_SEL	GPIO output selection Same as above

Register 0x2B GPIO

Bit(s)	Addr	Parameter	Function
[2]	0x2B	GPIO3_IN	GPIO3 input read out
[1]	0x2B	GPIO2_IN	GPIO2 input read out
[0]	0x2B	GPIO1_IN	GPIO1 input read out

12.26 REGISTER 0X2C GPIO

Bit(s)	Addr	Parameter	Function
[7]	0x2C	POL	0 interrupt polarity, output will be 1 active high 1 interrupt polarity, output will be 0 active low
[4]	0x2C	Clip2_IE	Clip interrupt enable number 2
[3]	0x2C	Clip1_IE	Clip interrupt enable number 1
[2]	0x2C	GPIO3_IE	GPIO3 interrupt enable
[1]	0x2C	GPIO2_IE	GPIO2 interrupt enable
[0]	0x2C	GPIO1_IE	GPIO1 interrupt enable

12.27 REGISTER 0X2D GPIO

Bit(s)	Addr	Parameter	Function
[4]	0x2D	Clip2_INT	Clip1 interrupt read status
[3]	0x2D	Clip1_INT	Clip1 interrupt read status
[2]	0x2D	GPIO3_INT	GPIO3 interrupt read status
[1]	0x2D	GPIO2_INT	GPIO2 interrupt read status
[0]	0x2D	GPIO1_INT	GPIO1 interrupt read status

12.28 REGISTER 0X2E ADC CONTROLS

Bit(s)	Addr	Parameter	Function
[7]	0x2E	HPFAPP	High pass filter application mode 0 audio 1st order fc=3.7Hz 1 2nd order, cutoff set by HPFCUT
[6:4]	0x2E	HPFCUT	High pass filter cutoff frequency
[3]	0x2E	ADCOSR	0 ADC OSR64 better operation at low V 1 ADC OSR128 lower noise

12.29 REGISTER 0X2F ADC CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	0x2F	ADCVU	ADC volume update bit
[7:0]	0x2F	ADCVOLL	Set the ADC volume left channel 0 = digital mute 1 = -127 dB 2 = -126.5 dB … 0.5 dB steps 255 = 0 dB

12.30 REGISTER 0X30 ADC CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	030	ADCVU	ADC volume update bit
[7:0]	0x30	ADCVOLR	Set the ADC volume right channel 0 = digital mute 1 = -127 dB 2 = -126.5 dB … 0.5 dB steps 255 = 0 dB

12.31 REGISTER 0X32 EQUALIZER CONTROLS

Bit(s)	Addr	Parameter	Function
[7]	0x32	EQ1BW	Bandwidth control 0 Narrow bandwidth 1 Wide bandwidth
[6:5]	0x32	EQ1CF	Cut-off frequencies 00 80Hz 01 105Hz 10 135Hz 11 175Hz
[4:0]	0x32	EQ1GF	Equalizer gain 00000 +12dB 11000 -12dB 11001 to 11111 reserved

12.32 REGISTER 0X33 EQUALIZER CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	0x33	EQ2BW	Bandwidth control 0 Narrow bandwidth 1 Wide bandwidth
[6:5]	0x33	EQ2CF	Center frequencies 00 230Hz 01 300Hz 10 385Hz 11 500Hz
[4:0]	0x33	EQ2GF	Equalizer gain 00000 +12dB 11000 -12dB 11001 to 11111 reserved

12.33 REGISTER 0X34 EQUALIZER CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	0x34	EQ3BW	Bandwidth control 0 Narrow bandwidth 1 Wide bandwidth
[6:5]	0x34	EQ3CF	Center frequencies 00 650Hz 01 850Hz 10 1100Hz 11 1400Hz
[4:0]	0x34	EQ3GF	Equalizer gain 00000 +12dB 11000 -12dB 11001 to 11111 reserved

12.34 REGISTER 0X35 EQUALIZER CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	0x35	EQ4BW	Bandwidth control 0 Narrow bandwidth 1 Wide bandwidth
[6:5]	0x35	EQ4CF	Center frequencies 00 1.8KHz 01 2.4KHz 10 3.2KHz 11 4.1KHz
[4:0]	0x35	EQ4GF	Equalizer gain 00000 +12dB 11000 -12dB 11001 to 11111 reserved

12.35 REGISTER 0X36 EQUALIZER CONTROLS

Bit(s)	Addr	Parameter	Function
[8]	0x36	EQ5BW	Bandwidth control 0 Narrow bandwidth 1 Wide bandwidth
[6:5]	0x36	EQ5CF	Cut-off frequencies 00 5.3KHz 01 6.9KHz 10 9.0KHz 11 11.7KHz
[4:0]	0x36	EQ5GF	Equalizer gain 00000 +12dB 11000 -12dB 11001 to 11111 reserved

12.36 REGISTER 0X37 ANALOG TEST MODES

Bit(s)	Addr	Parameter	Function
[8:0]	0x37	ANA_TEST	000000100 2nd stage PGA bypassed 000010000 1.8V logic supply to POUT pin 000100000 1.8V logic supply to VREF pin

12.37 REGISTER 0X3B-0X3E NOTCH FILTERS CONTROLS

Addr	D8	D7	D6	D5	D4	D3	D2	D1	D0	Default
0x3B	NFCU	NFCEN	NFCA0[13:7]							**0x000**
0x3C	NFCU	0	NFCA0[6:0]							**0x000**
0x3D	NFCU	0	NFCA1[13:7]							**0x000**
0x3E	NFCU	0	NFCA1[6:0]							**0x000**

The Notch Filter is enabled by setting NFCEN[7] address (0x3B) bit to HIGH. The coefficients, A_0 and A_1, should be converted to 2's complement numbers to determine the register values. A_0 and A_1 are represented by the register bits NFCA0[13:0] and NFCA1[13:0]. Since there are four register of coefficients, a Notch Filter Update bit is provided so that the coefficients can be updated simultaneously. NFCU[8] is provided in all registers of the Notch Filter coefficients but only one bit needs to be toggled for LOW - HIGH - LOW for an update. If any of the NFCU[8] bits are left HIGH then the Notch Filter coefficients will continuously update. An example of how to calculate is provided in the Notch Filter section.

12.38 REGISTER 0X44 PLL REGISTER A

Bit(s)	Addr	Parameter	Function
[4]	0x44	PLLMCLK	0=MCLK input not divided 1=MCLK input is divided by 2
[3:0]	0x44	PLLN_A	PLL coefficient N

12.39 REGISTER 0X45 PLL REGISTER A

Bit(s)	Addr	Parameter	Function
[5:0]	0x45	PLLK_A[23:18]	PLL coefficient K, upper bits

12.40 REGISTER 0X46 PLL REGISTER A

Bit(s)	Addr	Parameter	Function
[8:0]	0x46	PLLK_A[17:9]	PLL coefficient K, mid bits

12.41 REGISTER 0X47 PLL REGISTER A

Bit(s)	Addr	Parameter	Function
[8:0]	0x47	PLLK_A[8:0]	PLL coefficient K, lower bits

12.42 REGISTER 0X4B ADDITIONAL AUDIO PATH REGISTERS

Bit(s)	Addr	Parameter	Function
[6]	0x4B	LMIC2_2INPPGA2	0 = P1IN not connected to input PGA stage2 1 = P1IN to input PGA stage 2 Negative terminal.
[5]	0x4B	LMICN2INPPGA2	0 = not connected to input PGA stage 2 1 = to input PGA stage 2 Negative terminal.
[2]	0x4B	LMIC2_2INPPGA1	0 = P1IN not connected to input PGA stage1 1 = P1IN to input PGA stage 1 Negative terminal.
[1]	0x4B	LMICN2INPPGA1	0 = MIC1N not connected to input PGA stage 1 1 = MIC1N to input PGA stage 1 Negative terminal.
[0]	0x4B	LMICP2INPPGA	0 = Input PGA stage 1 Positive terminal to VREF 1 = Input PGA stage 1 Positive terminal to MIC1P

12.43 REGISTER 0X4C ADDITIONAL AUDIO PATH REGISTERS

Bit(s)	Addr	Parameter	Function
[6]	0x4C	RMIC2_2INPPGA2	0 = P2IN not connected to input PGA stage2 1 = P2IN to input PGA stage 2 Negative terminal.
[5]	0x4C	RMICN2INPPGA2	0 = not connected to input PGA stage 2 1 = to input PGA stage 2 Negative terminal.
[2]	0x4C	RMIC2_2INPPGA1	0 = P2IN not connected to input PGA stage1 1 = P2IN to input PGA stage 1 Negative terminal.
[1]	0x4C	RMICN2INPPGA1	0 = MIC2N not connected to input PGA stage 1 1 = MIC2N to input PGA stage 1 Negative terminal.
[0]	0x4C	RMICP2INPPGA	0 = Input PGA stage 1 Positive terminal to VREF 1 = Input PGA stage 1 Positive terminal to MIC2P

12.44 REGISTER 0X4D ADDITIONAL AUDIO PATH REGISTERS

Bit(s)	Addr	Parameter	Function
[6]	0x4D	LMBMUTE	Reserved/unused
[5:0]	0x4D	INPPGALVOL	Left channel PGA stage 2 gain

12.45 REGISTER 0X4E ADDITIONAL AUDIO PATH REGISTERS

Bit(s)	Addr	Parameter	Function
[6]	0x4E	RMBMUTE	Reserved/unused
[5:0]	0x4E	INPPGARVOL	Right channel PGA stage 2 gain

12.46 REGISTER 0X4F PLL REGISTER B

Bit(s)	Addr	Parameter	Function
[5]	0x4F	PLLREGSEL	0 select PLL coefficients register A 1 select PLL coefficients register B
[4]	0x4F	PLLMCLK	0=MCLK input not divided 1=MCLK input is divided by 2
[3:0]	0x4F	PLLN_B	PLL coefficient N

12.47 REGISTER 0X50 PLL REGISTER B

Bit(s)	Addr	Parameter	Function
[5:0]	0x50	PLLK_B[23:18]	PLL coefficient K, upper bits

12.48 REGISTER 0X51 PLL REGISTER B

Bit(s)	Addr	Parameter	Function
[8:0]	0x51	PLLK_B[17:9]	PLL coefficient K, mid bits

12.49 REGISTER 0X52 PLL REGISTER B

Bit(s)	Addr	Parameter	Function
[8:0]	0x52	PLLK_B[8:0]	PLL coefficient K, lower bits

12.50 REGISTER 0X59 ADC MIXER

Bit(s)	Addr	Parameter	Function
[5:4]	0x59	MixerMap_ADC2	ADC right channel digital mixer map Configure outputs routed out on to ADC right channel 00: zero 01: left channel input 10: right channel input (default) 11: left + right channel input
[1:0]	0x59	MixerMap_ADC1	ADC left channel digital mixer map Configure outputs routed out on to ADC left channel 00: zero 01: left channel input (default) 10: right channel input 11: left + right channel input

12.51 REGISTER 0X5A POWER MANAGEMENT EXTRA

Bit(s)	Addr	Parameter	Function
[8]	0x5A	PGA_stage2_bias	0 PGA stage 2 uses nominal bias 1 PGA stage 2 uses half current bias
[7]	0x5A	HALF_BIAS_ADC_buffer	0 ADC uses nominal bias 1 ADC uses half current bias
[6]	0x5A	HALF_BIAS_SPARES (no used)	0 ADC uses nominal bias 1 ADC uses half current bias
[4]	0x5A	MCBSMODE	0 nominal mode requires large cap 1 lower noise mode requires small cap
[3:2]	0x5A	TRIM_REGULATOR_SV	00 nominal logic supply 1.8V 01 1.71V 10 1.6V 11 1.4V
[0]	0x5A	GPIO3_IE	0 Input disabled on GPIO3 1 Input enabled on GPIO3

12.52 REGISTER 0X5B LEFT CHANNEL PCM TIME SLOT START COUNT

Bit(s)	Addr	Parameter	Function
[8:0]	0x5B	TSLOTL[8:0]	Left Channel PCM Time Slot Start Count [8:0]

12.53 REGISTER 0X5C PCM AND TIME SLOT CONTROL

Bit(s)	Addr	Parameter	Function
[8]	0x5C	PCMTSEN	0 = Only DSP MODE A or MODE B can be used when 1 = PCM Time Slot Mode is enabled when FORMT=11
[7]	0x5C	TRI	0 = not enabled 1 = when ADCDAT_OEN_SEL (0x5C[2])=1 and ADCDAT_OEN(0x5C[5])]=0, 2nd half of LSB will be Tri-State or pull up / down
[6]	0x5C	PCM8BIT	0 = use WLEN to select the Word Length 1 = Word Length is 8 bit
[5]	0x5C	ADCDAT_OEN	This bit is only effective when ADCDAT_OEN_SEL(0x5c[2]) = 0 0 = ADCOUT is tri-state or pull up/down before MSB and after LSB 1 = ADCOUT is always driven 1 or 0 by NAU8502
[4]	0x5C	ADCDAT_PE	0 = no internal weak pull up / down on ADCOUT 1 = internal weak pull up / down on ADCOUT
[3]	0x5C	ADCDAT_PS	0 = internal weak pull down on ADCOUT when ADCDAT_PE=1 1 = internal weak pull up on ADCOUT when ADCDAT_PE=1
[2]	0x5C	ADCDAT_OEN_SEL	0 = use ADCOUTDIS(0x07[7]) to enable or disable ADCOUT 1 = use ADCDAT_OEN(0x5C[5]) to control ADCOUT driver
[1]	0x5C	TSLOTR[9]	Right Channel PCM Time Slot Start Count [9]
[0]	0x5C	TSLOTL[9]	Left Channel PCM Time Slot Start Count [9]

12.54 REGISTER 0X5D RIGHT CHANNEL PCM TIME SLOT START COUNT

Bit(s)	Addr	Parameter	Function
[8:0]	0x5D	TSLOTR[8:0]	Right Channel PCM Time Slot Start Count [8:0]

12.55 REGISTER 0X5E ID REGISTERS

Bit(s)	Addr	Parameter	Function
[8:0]	0x5E	REG_SI_REV	Silicon revision set to 0xFE

12.56 REGISTER 0X5F ID REGISTERS

Bit(s)	Addr	Parameter	Function

[8:0]	0x5F	I2C_DEVID	I2C device is set to 0x1A when CSB=0 I2C device is set to 0x1B when CSB=1

12.57 REGISTER 0X60 ID REGISTERS

Bit(s)	Addr	Parameter	Function
[8:0]	0x60	NTCA	Custom register is set to 0xCA

12.58 REGISTER 0X66 ALC INTERRUPTS FEATURES REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x66	ALCTABLESEL	0 = ALCSL range -28.5:-6dB 1 = ALCSL range -22.5:-1.5 dB
[7]	0x66	ALCPKSEL	0 = use absolute peak value for ALC training 1 = use peak-to-peak value for ALC training
[6]	0x66	ALCNGSEL	0 = use peak-to-peak value for noise gate threshold determination 1 = use absolute peak value for noise gate threshold determination
[5:0]	0x66	ALCGAIN_L	Left channel ALC gain status

12.59 REGISTER 0X67 ALC INTERRUPTS FEATURES REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x67	ALCPKLIMENn	0 = enable fast decrement when signal exceeds 87.5% of full scale 1 = disable fast decrement when signal exceeds 87.5% of full scale
[7]	0x67	PK_DET_CLR	When PK_DET_HOLD is asserted HIGH, writing a 1 to this bit clears the stored peak value
[6]	0x67	PK_DET_HOLD	0 = Normal peak detection 1 = Hold peak value until PK_DET_CLR is written. This should only be used for signal level diagnostics and not for normal ALC operation
[5:0]	0x67	ALCGAIN_R	Right channel ALC gain status

12.60 REGISTER 0X68 ADC AND EQUALIZER ADDITIONAL REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x68	LATCH_DLY[1]	(test mode only) 0 = ADC data sampled on rising edge 1 = ADC data sampled on falling edge
[7]	0x68	LATCH_DLY[0]	(test mode only) 0 = Normal phase for ADC clock 1 = Inverted phase for ADC clock
[6]	0x68	SWAP_DM_DFE	0: ch1=left dmic, ch2=right dmic 1: ch1=right dmic, ch2=left dmic
[5]	0x68	EN_DIG_MIC_R	0=disable right digital mic 1=enable right digital mic

[4]	0x68	EN_DIG_MIC_L	0=disable left digital mic 1=enable left digital mic
[3]	0x68	DM_DS	0=slower slew-rate for DM_CLK 1=faster slew-rate for DM_CLK
[2]	0x68	ALCGRP	0 = Left and right channel ALCs train independently with separate gain settings for each channel 1 = Left and right channel ALCs train together with a single gain setting for both channels when both enabled (default)
[1]	0x68	EQON_TEST	0 = Bypass equalizer 1 = Enable equalizer (default)
[0]	0x68	SKIP_DLY	0 = Align L/R sinc outputs with delay 1 = Bypass right channel sinc alignment delay

12.61 REGISTER 0X69 ADC AND EQUALIZER ADDITIONAL REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x69	FORCE_4W_SPI	0 = only I2C or SPI 3 wire mode can be used 1 = use SPI 4 wire mode no matter the MODE pin is 1 or 0
[5]	0x69	FLUSH_ON_ERR	0 = Normal operation 1 = Flush digital filter memory when internal clocking error detected
[4]	0x69	IDSEL_MODE	0 = I2C Device ID selected by CSB on every transaction 1 = I2C Device ID selected by CSB state at reset
[3]	0x69	NOTCH_DLY_DIS	0 = Normal operation – notch filter output is delayed until stabilized 1 = Notch delay disabled – notch filter output is available immediately upon enabling
[1]	0x69	PLLOCK_BP	0 = PLL lock circuit normal operation 1 = PLL lock forced high

12.62 REGISTER 0X6A TIE-OFF REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x6A	MANU_IN_CTRL	0 nominal control of the VMID tie off 1 manual control of the VMID tie off

12.63 REGISTER 0X6B TIE-OFF REGISTERS

Bit(s)	Addr	Parameter	Function
[2:0]	0x6B	MANU_VMID_CTRL	Require to have 0x6A[8] set to 1 001 5.6K Ohm pull down resistor 010 161K Ohm pull down resistor 100 595K Ohm pull down resistor

12.64 REGISTER 0X6C AGC READOUT REGISTERS

Bit(s)	Addr	Parameter	Function

[8:0]	0x6C	P2P_OUT_L	Left channel peak-to-peak value

12.65 REGISTER 0X6D AGC READOUT REGISTERS

Bit(s)	Addr	Parameter	Function
[8:0]	0x6D	P2P_OUT_R	Right channel peak-to-peak value

12.66 REGISTER 0X6E AGC READOUT REGISTERS

Bit(s)	Addr	Parameter	Function
[8:0]	0x6E	PEAK_OUT_L	Left channel absolute peak value

12.67 REGISTER 0X6F AGC READOUT REGISTERS

Bit(s)	Addr	Parameter	Function
[8:0]	0x6F	PEAK_OUT_R	Right channel absolute peak value

12.68 REGISTER 0X70 NOISE GATE READOUT REGISTERS

Bit(s)	Addr	Parameter	Function
[5]	0x70	NOISE_OUT_R	Right channel noise gate flag 0 = signal above noise gate threshold 1 = signal below noise gate threshold
[4]	0x70	NOISE_OUT_L	Left channel noise gate flag 0 = signal above noise gate threshold 1 = signal below noise gate threshold
[1]	0x70	FAST_DEC_L	Left channel fast decrement flag 0 = signal below 87.5% of full scale 1 = signal above 87.5% of full scale
[0]	0x70	FAST_DEC_R	Right channel fast decrement flag 0 = signal below 87.5% of full scale 1 = signal above 87.5% of full scale

12.69 REGISTER 0X71 MANUAL TIE-OFF REGISTERS

Bit(s)	Addr	Parameter	Function
[8]	0x71	REGENABLE	0 disabled 1 enable direct control on buffer tie off
[6]	0x71	SHORTBUFL	0 tie off buffer is used 1 bypass tie off buffer
[5]	0x71	Tie-off buffered VREF	0 disabled 1 enabled tie off voltage to VMID buffer when buffer is off

13 CONTROL INTERFACE TIMING DIAGRAM

13.1 SPI WRITE TIMING DIAGRAM

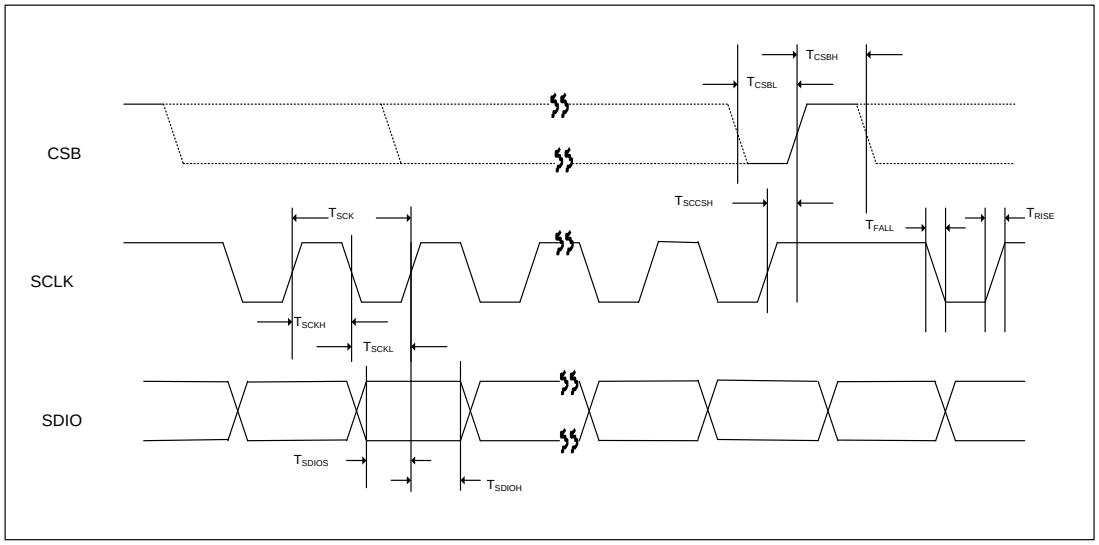


Figure 30: SPI Write Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{SCK}	SCLK Cycle Time	80	---	---	ns
T_{SCKH}	SCLK High Pulse Width	35	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	35	---	---	ns
T_{RISE}	Rise Time for all SPI Signals	---	---	10	ns
T_{FALL}	Fall Time for all SPI Signals	---	---	10	ns
T_{CSSCS}	CSb Falling Edge to 1st SCLK Falling Edge Setup Time (4 wire SPI only)	30	---	---	ns
T_{SCCSH}	Last SCLK Rising Edge to CSb Rising Edge Hold Time	30	---	---	ns
T_{CSBL}	CSb Low Time	30	---	---	ns
T_{CSBH}	CSb High Time between CSb Lows	30	---	---	ns
T_{SDIOS}	SDIO to SCLK Rising Edge Setup Time	20	---	---	ns
T_{SDIOH}	SCLK Rising Edge to SDIO Hold Time	20	---	---	ns

Table 32: SPI Timing Parameters

13.2 2-WIRE TIMING DIAGRAM

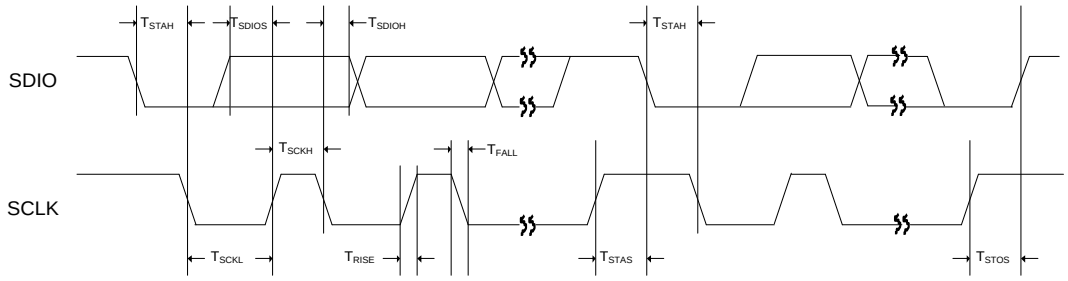


Figure 31: 2-Wire Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{STAH}	START / Repeat START condition, SCLK falling edge to SDIO falling edge hold timing	600	---	---	ns
T_{STAS}	Repeat START condition, SDIO rising edge to SCLK falling edge setup timing	600	---	---	ns
T_{STOS}	STOP condition, SDIO rising edge to SCLK rising edge setup timing	600	---	---	ns
T_{SCKH}	SCLK High Pulse Width	600	---	---	ns
T_{SCKL}	SCLK Low Pulse Width	1.3	---	---	us
T_{RISE}	Rise Time for all 2-Wire Signals	---	---	300	ns
T_{FALL}	Fall Time for all 2-Wire Signals	---	---	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	400	---	---	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	---	600	ns

Table 33: 2-WireTiming Parameters

14 AUDIO INTERFACE TIMING DIAGRAM

14.1 AUDIO INTERFACE IN SLAVE MODE

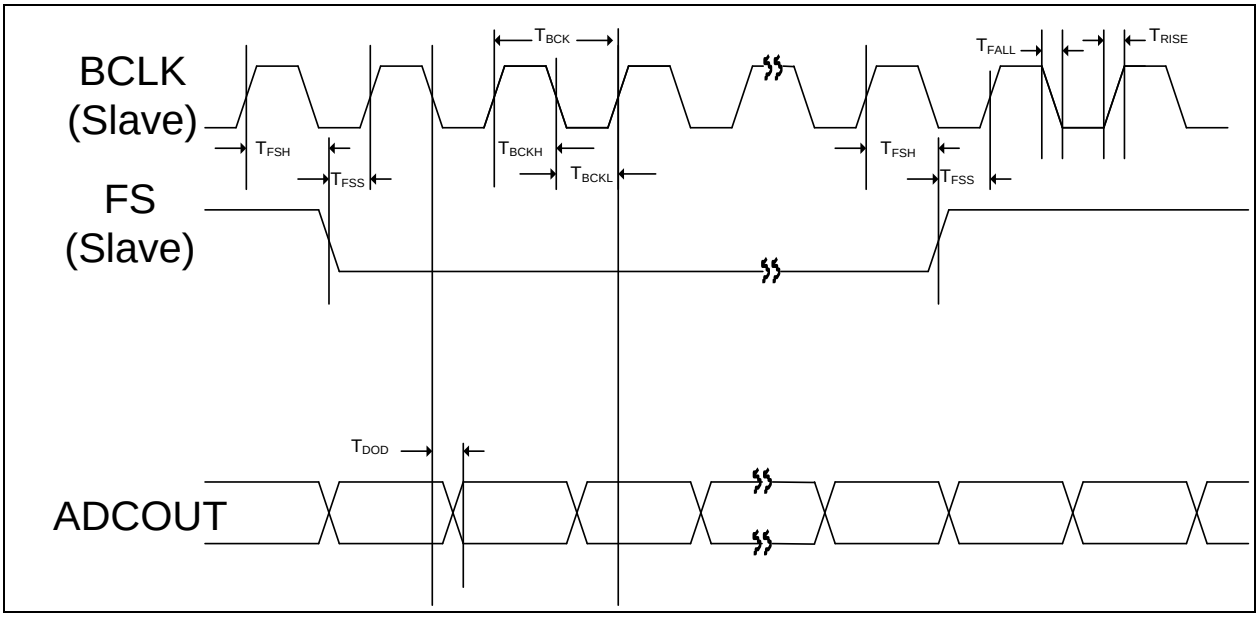


Figure 32: Audio Interface Slave Mode Timing Diagram

14.2 AUDIO INTERFACE IN MASTER MODE

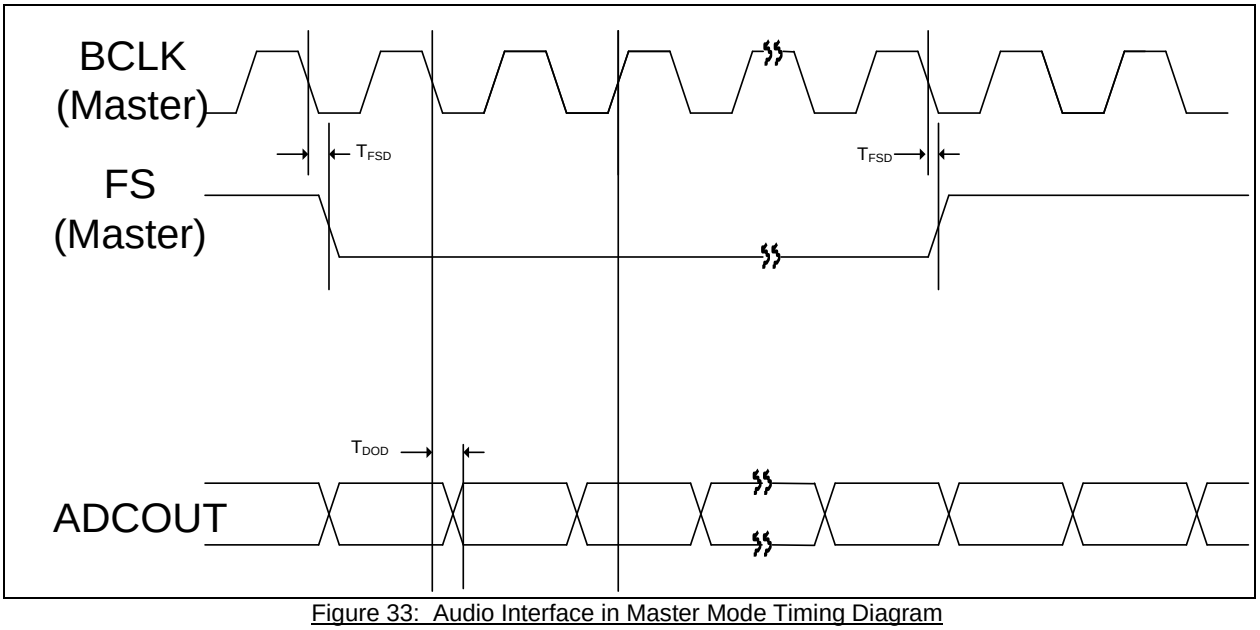


Figure 33: Audio Interface in Master Mode Timing Diagram

14.3 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Audo Data)

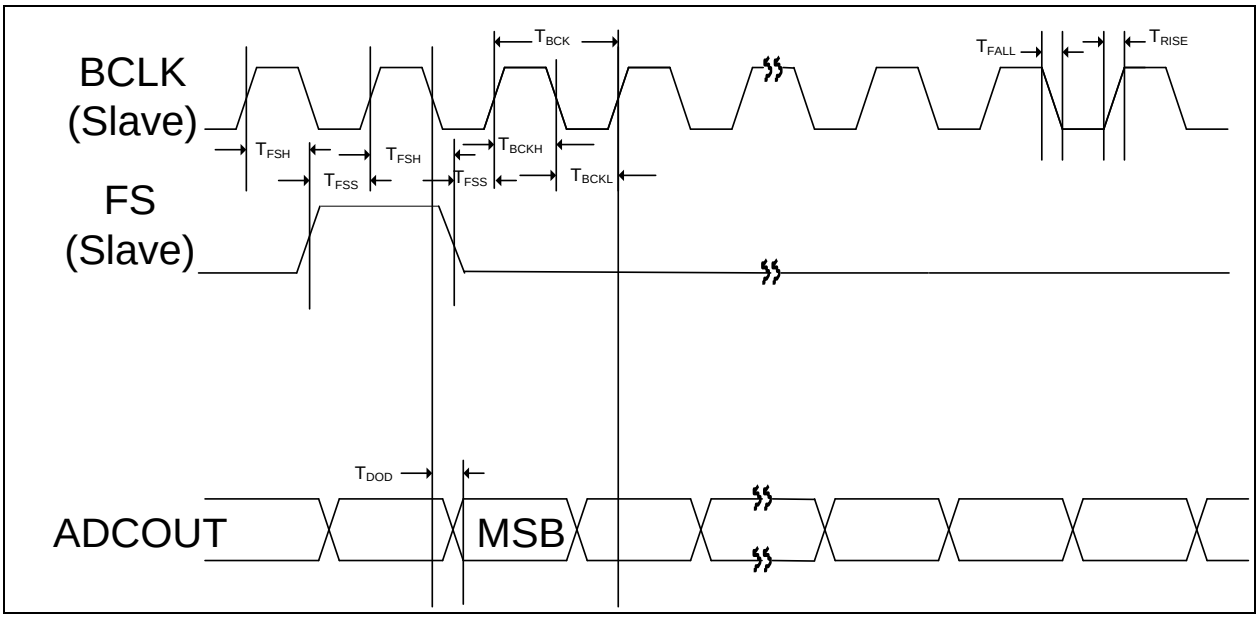


Figure 34: PCM Audio Interface Slave Mode Timing Diagram

14.4 PCM AUDIO INTERFACE IN MASTER MODE (PCM Audo Data)

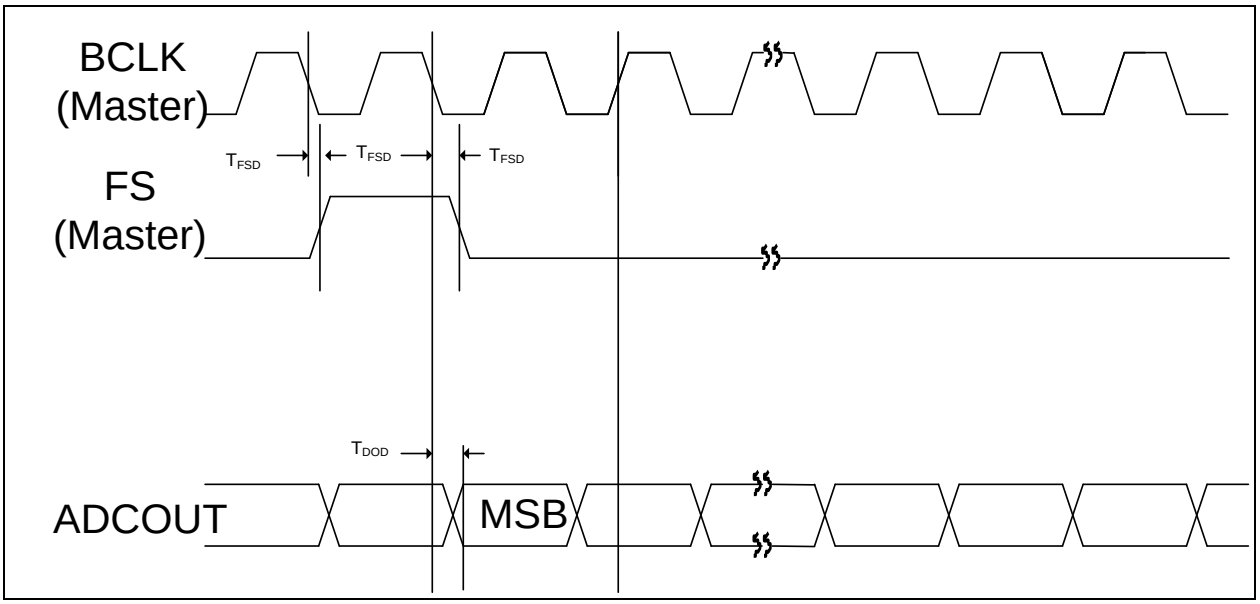


Figure 35: PCM Audio Interface Slave Mode Timing Diagram

14.5 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Time Slot Mode)

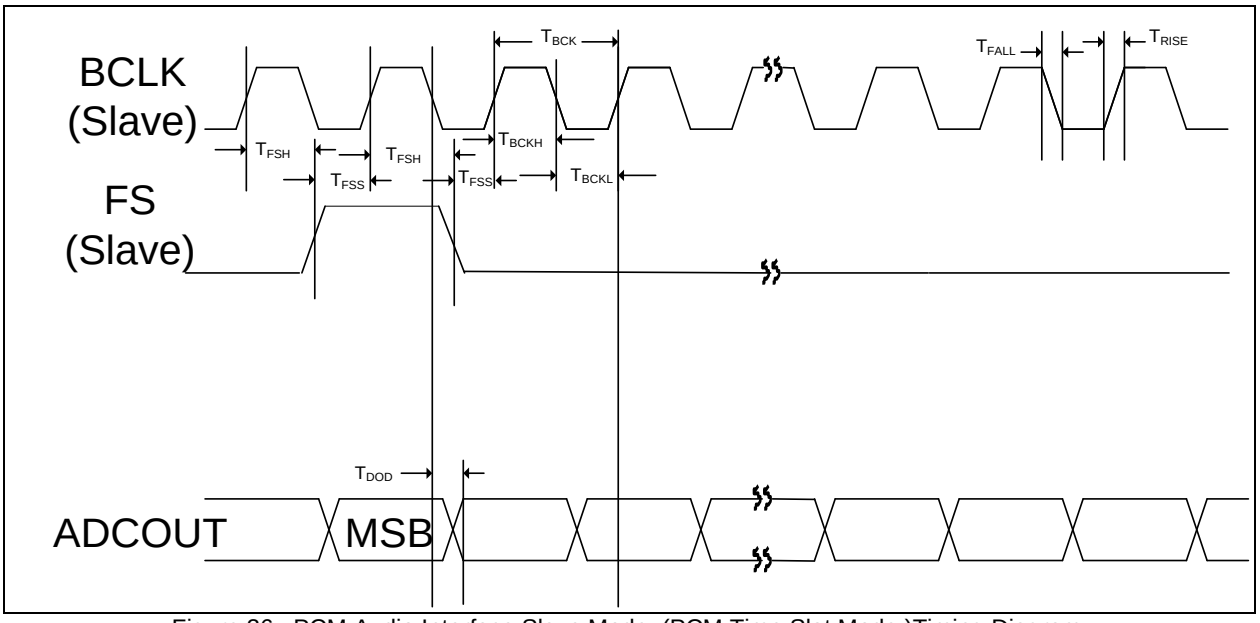


Figure 36: PCM Audio Interface Slave Mode (PCM Time Slot Mode)Timing Diagram

14.6 PCM AUDIO INTERFACE IN MASTER MODE (PCM Time Slot Mode)

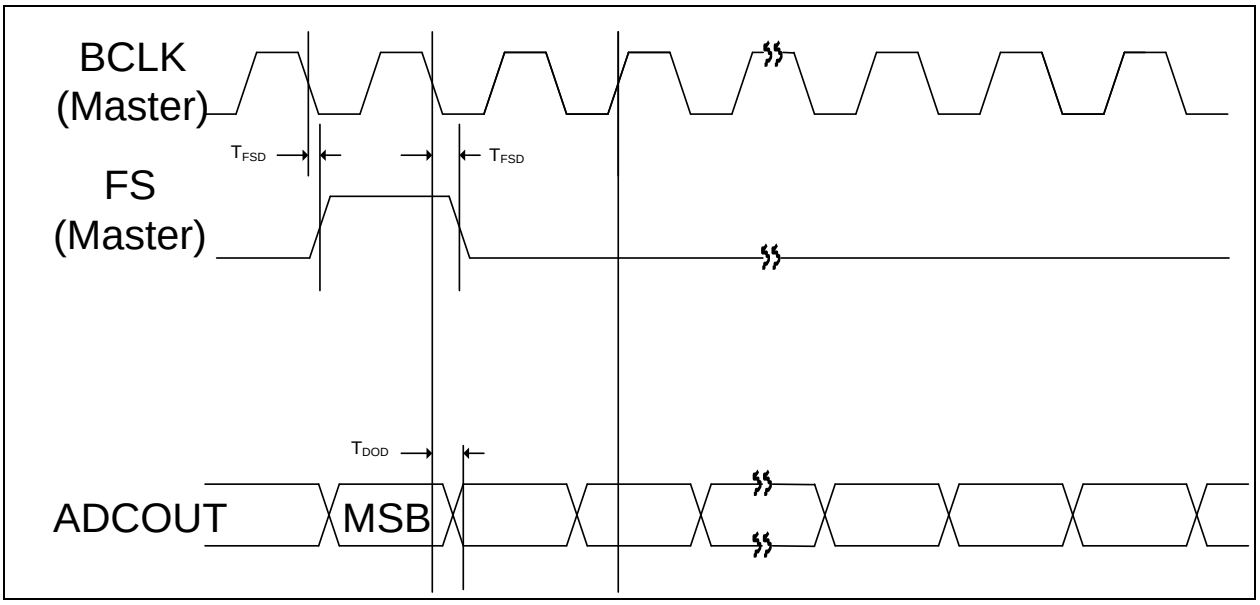


Figure 37: PCM Audio Interface Master Mode (PCM Time Slot Mode)Timing Diagram

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{BCK}	BSCK Cycle Time (Slave Mode)	50	---	---	ns
T_{BCKH}	BSCK High Pulse Width (Slave Mode)	20	---	---	ns
T_{BCKL}	BSCK Low Pulse Width (Slave Mode)	20	---	---	ns
T_{FSS}	fs to SCK Rising Edge Setup Time (Slave Mode)	20	---	---	ns
T_{FSH}	SCK Rising Edge to fs Hold Time (Slave Mode)	20	---	---	ns
T_{FSD}	fs to SCK falling to fs transition (Master Mode)	---	---	10	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{DIS}	ADCIN to SCK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	SCK Rising Edge to ADCIN Hold Time	15	---	---	ns

Table 34: Audio Interface Timing Parameters

14.7 System Clock (MCLK) Timing Diagram

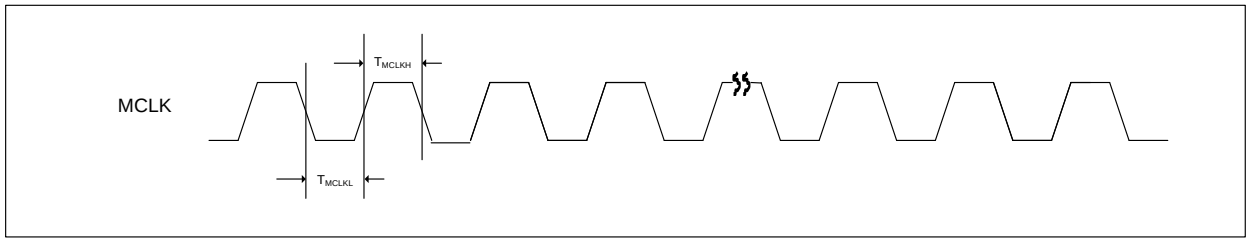


Figure 38: MCLK Timing Diagram

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCLK Duty Cycle	T_{MCLKDC}		60:40		40:60	
MCLK High Pulse Width	T_{MCLKH}		20	---	---	ns
MCLK Low Pulse Width	T_{MCLKL}		20	---	---	ns

Table 35: MCLK Timing Parameter

14.8 μ-LAW ENCODE DECODE CHARACTERISTICS

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
8159									
	1	0	0	0	0	0	0	0	8031
7903 : 4319	:	:	:	:	:	:	:	:	:
	1	0	0	0	1	1	1	1	4191
4063 : 2143	:	:	:	:	:	:	:	:	:
	1	0	0	1	1	1	1	1	2079
2015 : 1055	:	:	:	:	:	:	:	:	:
	1	0	1	0	1	1	1	1	1023
991 : 511	:	:	:	:	:	:	:	:	:
	1	0	1	1	1	1	1	1	495
479 : 239	:	:	:	:	:	:	:	:	:
	1	1	0	0	1	1	1	1	231
223 : 103	:	:	:	:	:	:	:	:	:
	1	1	0	1	1	1	1	1	99
95 : 35	:	:	:	:	:	:	:	:	:
	1	1	1	0	1	1	1	1	33
31 : 3	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	0	2
1	:	:	:	:	:	:	:	:	:
	1	1	1	1	1	1	1	1	0
0									

Notes:
Sign bit = 0 for negative values, sign bit = 1 for positive values

14.9 A-LAW ENCODE DECODE CHARACTERISTICS

Normalized Encode Decision Levels	Digital Code								Normalized Decode Levels
	D7	D6	D5	D4	D3	D2	D1	D0	
	Sign	Chord	Chord	Chord	Step	Step	Step	Step	
4096									
	1	0	1	0	1	0	1	0	4032
3968 : 2176	:	:	:	:	:	:	:	:	:
	1	0	1	0	0	1	0	1	2112
2048 : 1088	:	:	:	:	:	:	:	:	:
	1	0	1	1	0	1	0	1	1056
1024 : 544	:	:	:	:	:	:	:	:	:
	1	0	0	0	0	1	0	1	528
512 : 272	:	:	:	:	:	:	:	:	:
	1	0	0	1	0	1	0	1	264
256 : 136	:	:	:	:	:	:	:	:	:
	1	1	1	0	0	1	0	1	132
128 : 68	:	:	:	:	:	:	:	:	:
	1	1	1	0	0	1	0	1	66
64 : 2	:	:	:	:	:	:	:	:	:
	1	1	0	1	0	1	0	1	1
0									

Notes:
1. Sign bit = 0 for negative values, sign bit = 1 for positive values
2. Digital code includes inversion of all even number bits

14.10 μ-LAW / A-LAW CODES FOR ZERO AND FULL SCALE

Level	μ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
+ Full Scale	1	000	0000	1	010	1010
+ Zero	1	111	1111	1	101	0101
- Zero	0	111	1111	0	101	0101
- Full Scale	0	000	0000	0	010	1010

14.11 μ-LAW / A-LAW OUTPUT CODES (DIGITAL MW)

Sample	μ-Law			A-Law		
	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)	Sign bit (D7)	Chord bits (D6,D5,D4)	Step bits (D3,D2,D1,D0)
1	0	001	1110	0	011	0100
2	0	000	1011	0	010	0001
3	0	000	1011	0	010	0001
4	0	001	1110	0	011	0100
5	1	001	1110	1	011	0100
6	1	000	1011	1	010	0001
7	1	000	1011	1	010	0001
8	1	001	1110	1	011	0100

15 DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	+/- 0.025dB	0		0.454*fs	
	-6dB		0.5*fs		
Passband Ripple				+/-0.025	dB
Stopband		0.546*fs			
Stopband Attenuation	f > 0.546*fs	-60			dB
Group Delay			21/fs		
ADC High Pass Filter					
High Pass Filter Corner Frequency	-3dB		3.7		Hz
	-0.5dB		10.4		
	-0.1dB		21.6		

Table 57 Digital Filter Characteristics

TERMINOLOGY

1. Stop Band Attenuation (dB) – the degree to which the frequency spectrum is attenuated (outside audio band)
2. Pass-band Ripple – any variation of the frequency response in the pass-band region
3. Note that this delay applies only to the filters and does not include

16 TYPICAL APPLICATION

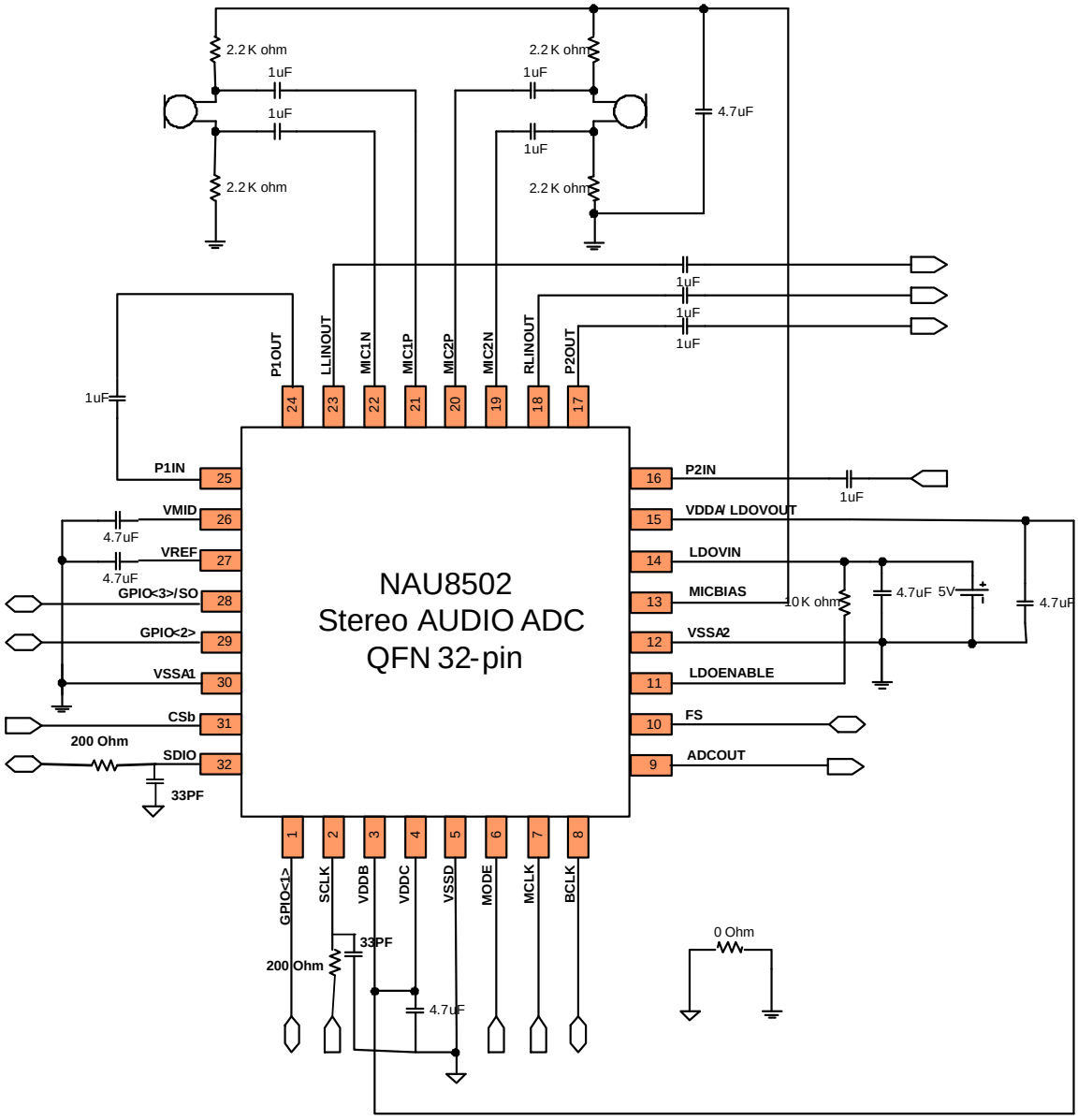


Figure 39: Application Diagram for 32-Pin QFN

Note 1: All non-polar capacitors are assumed to be low ESR type parts, such as with MLC construction or similar. If capacitors are not low ESR, additional 0.1uF and/or 0.01uF capacitors may be necessary in parallel with the bulk 4.7uF capacitors on the supply rails.

Note 2: Load resistors to ground on outputs may be helpful in some applications to insure a DC path for the output capacitors to charge/discharge to the desired levels. If the output load is always present and the output load provides a suitable DC path to ground, then the additional load resistors may not be necessary. If needed, such load resistors are typically a high value, but a value dependent upon the application requirements.

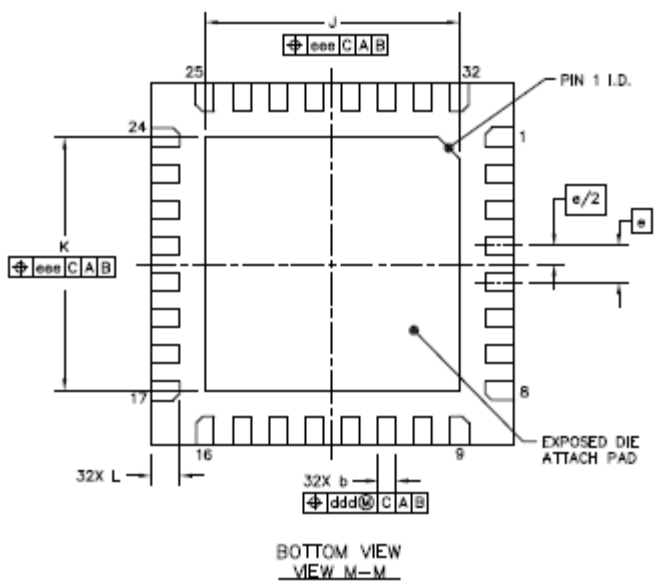
Note 3: To minimize pops and clicks, large polarized output capacitors should be a low leakage type.

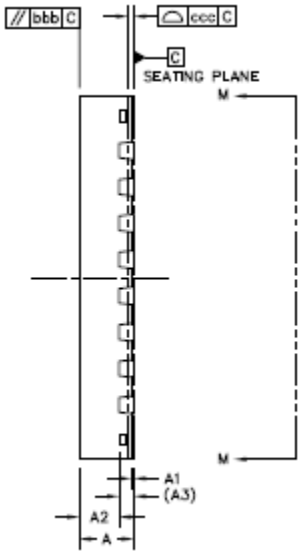
Note 4: Depending on the microphone device and PGA gain settings, common mode rejection can be improved by choosing the resistors on each node of the microphone such that the impedance presented to any noise on either microphone wire is equal.

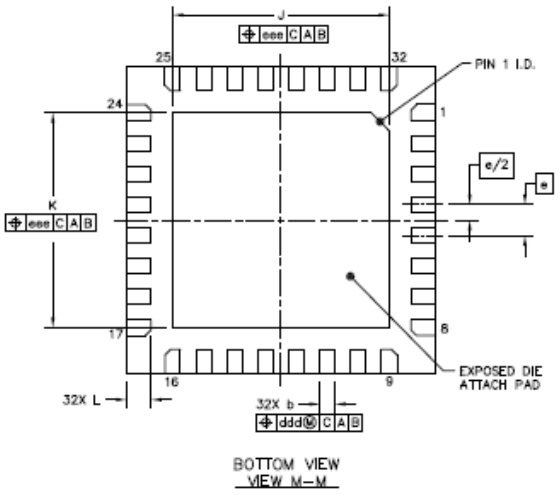
Note 5; SCLK and SDIO can use low pass filters to filter out glitch. The low pass filter corner frequency range is from 8MHz to 33MHz depending on PCB parasitic.

PACKAGE SPECIFICATION

32-lead plastic QFN 32L; 5X5mm^2, 0.8mm thickness, 0.5mm lead pitch







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

QFN32 Package

17 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU8502YG	5x5 mm	QFN-32	Green

NAU8502 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-32

18 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Jan, 2012	Changed the package reference to 32 QFN from 24 Pin QFN
2.0	Sep, 2012	Corrected the 32QFN package diagram
2.1	Oct, 2013	Corrected 2 wire interface timing diagram
2.2	Mar, 2014	Corrected rising/fall time specification of I2S Modified application circuit
2.3	Nov, 2014	I2C Isdios setup time
2.4	Jan, 2015	Updated AECQ100 description
2.5	Aug, 2018	Low pass filters are added for I2C
2.6	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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