NAU8315/NAU83U15
DataSheet

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1 FEATURE

- Pin Selectable Gain Setting
- Pin Selectable I2S Left or Right Channel Selection
- Pin Selectable PCM Time Slot
- Low Output Noise: 12 µVRMS
- 80dB PSRR @217Hz
- Low Current Shutdown and Standby Modes
- Click-and Pop Suppression: 26 µVRMS
- Sampling rate from 8K to 96 KHz
- Powerful Mono Class-D Amplifier
  3.2W (4Ω @ 5V, 10% THD+N)
  1.76W (4Ω @ 4.2V, 1% THD+N)
  1.8W (8Ω @ 5V, 10% THD+N)
  1.0W (8Ω @ 4.2V, 1% THD+N)
- Package: 9 ball WLCSP / 12 ball WLCSP / 20-pin QFN
- Package is Halogen-free, RoHS-compliant and TSCA-compliant

Applications

- Gaming Controllers
- Wireless (VR) Headset
- Smart Remote Controller
- Notebooks / Tablet PCs
- Personal Media Players
- Ultrasonic speakers

2 GENERAL DESCRIPTION

NAU8315/NAU83U15 is a mono high efficiency filter-free Class-D audio amplifier, which is capable of driving a 4Ω load with up to 3.2W output power. This device provides Enable control and I2S audio input with low standby current and fast start-up time.

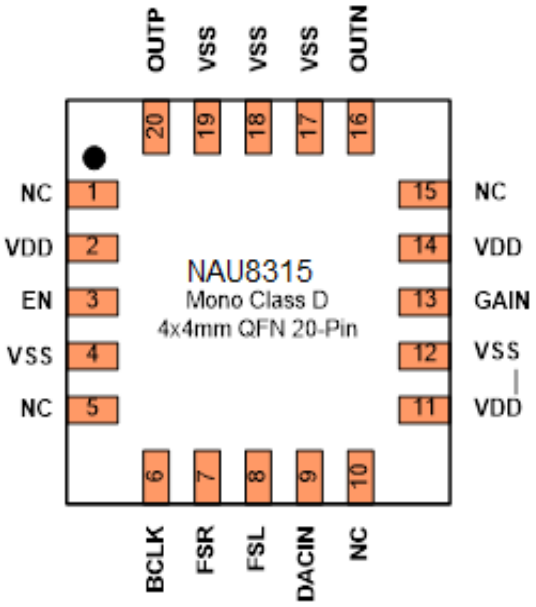
NAU8315/NAU83U15 is ideal for the portable applications, as it has advanced features like 80dB PSRR, 91% efficiency, ultra-low quiescent current and superior EMI performance.

NAU8315 is specified for operation from -40℃ ~ +85℃ with WLCSP-9 / WLCSP-12 / QFN-20 package.

NAU83U15 is specified for operation from -40℃ ~ +105℃ with QFN-20 package.

NAU83U15 is available for Automotive Grade AEC-Q100 qualification & TS16949 compliant.

3 PART INFORMATION



QFN exposed thermal pad must be connected to VSS

Figure 1 QFN-20 Configuration of NAU8315/NAU83U15

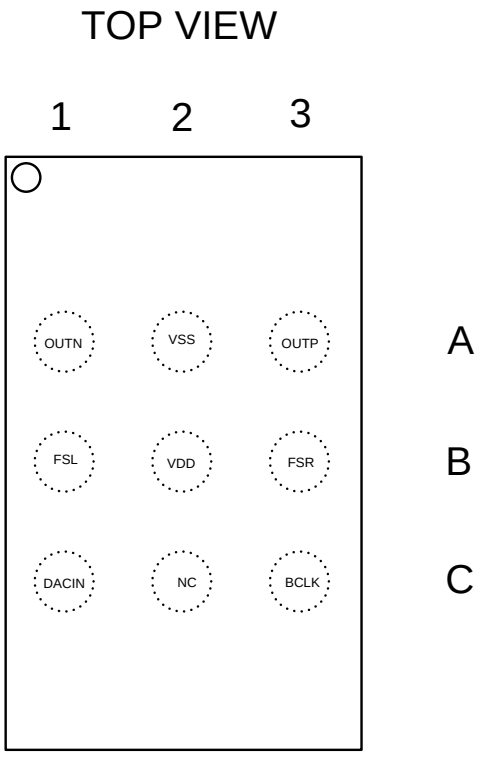


Figure 2 WLCSP-9 Configuration of NAU8315 (TOP VIEW)

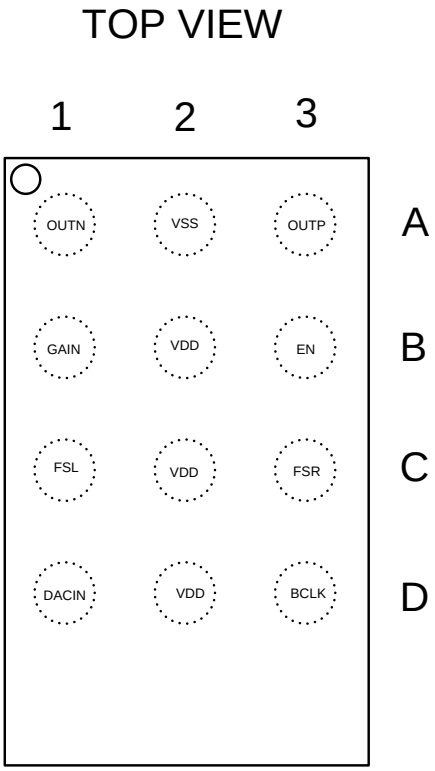


Figure 3 WLCSP-12 Configuration of NAU8315 (TOP VIEW)

Table 1 Pin Descriptions for the NAU8315/NAU83U15

12 Ball WLCSP#	9 Ball WLCSP#	20-pin QFN #	Name	Type	Description
D1	C1	9	DACIN	Digital Input	I2S I/F DAC digital audio data
C1	B1	8	FSL	Digital Input	I2S I/F Left Channel Frame clock
B1	-	13	GAIN	Analog IO	Gain Selection
A1	A1	16	OUTN	Analog Output	Speaker negative output
B2	B2	2	VDD	Supply	Power Supply
C2	-	11	VDD	Supply	Power Supply
D2	-	14	VDD	Supply	Power Supply
A2	A2	4,12,17, 18,19	VSS	Supply	Ground
D3	C3	6	BCLK	Digital Input	I2S I/F bit clock
C3	B3	7	FSR	Digital Input	I2S I/F Right Channel Frame clock
B3	-	3	EN	Digital Input	Device Enable Input
A3	A3	20	OUTP	Analog Output	Speaker positive output
-	C2**	1,5, 10,15*	NC	No Connection	No Connection

**Note: For WLCSP9 the NC ball C2 can be tied to VDD for convenient PCB layout.

*Note: For 20 pin QFN the NC pins can be tied to VSS for convenient PCB layout.

4 BLOCK DIAGRAM

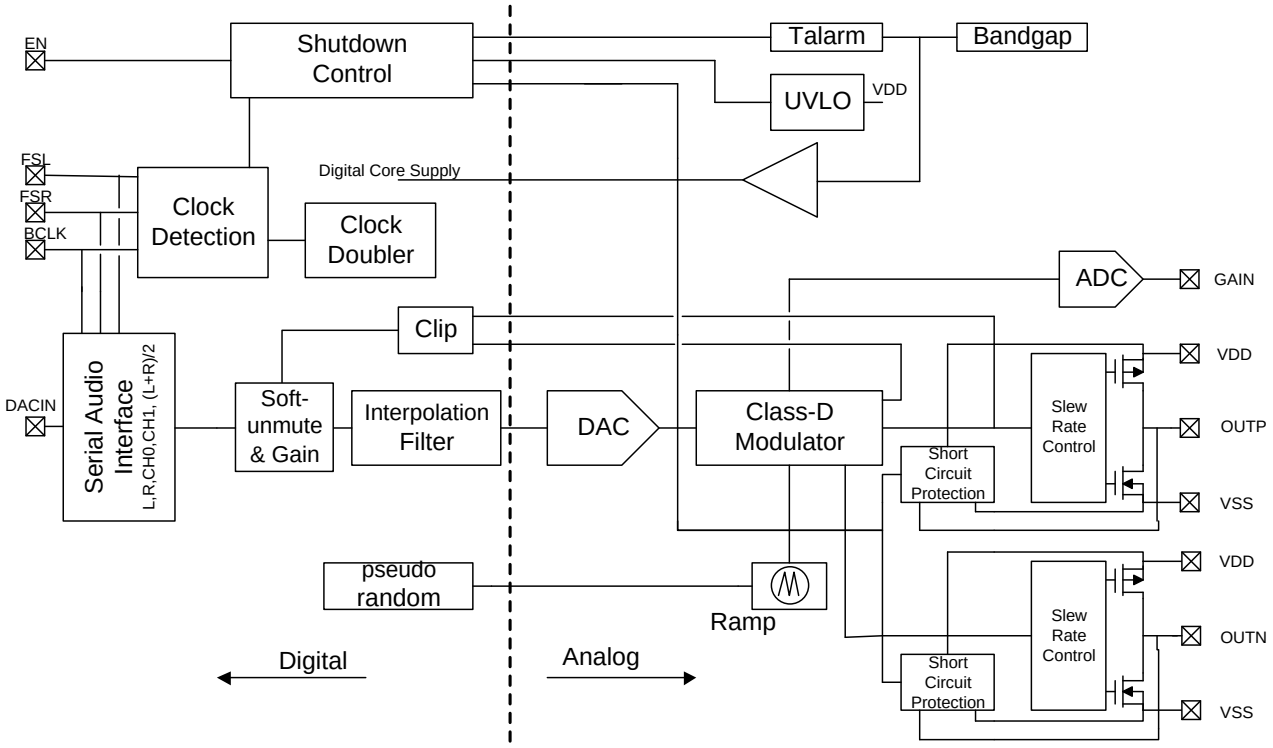


Figure 4 NAU8315/NAU83U15 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
VDD Battery Supply Range	-0.3	6.0	V
Voltage Input I/O Range	VSS - 0.3	VDD + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

5.2 Operating Conditions

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Battery Supply Range	VDD	2.50	4.2	5.25	V
Digital IO Range		1.8		VDD	
Ground	VSS		0		V
Industrial Operating Temperature		-40		+85	°C

5.3 Electrical Parameters

Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, gain=12dB, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units
ISD	Shutdown Supply Current	VDD, all clocks off	0.3	16	µA
ISB	Standby Mode Supply Current	VDD, clocks off, EN=VDD	0.3		µA
IDD	Operating Mode Supply Current	VDD, idle Channel	4.0		mA
Class-D Channel					
P_O	Output Power	VDD=4.2V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **QFN-20**	0.98		W
		VDD=4.2V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **WLCSP-12**	1.0		W
		VDD=5V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **QFN-20**	1.73		W
		VDD=5V RL = 8 Ohm + 33 µH and Total Harmonic Distortion+Noise	1.8		W

Symbol	Parameter	Conditions	Typical	Limit	Units
		(THD+N) = 10%, Gain=12dB, **WLCSP-12**			
		VDD=4.2V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **QFN-20**	1.69		W
		VDD=4.2V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 1%, Gain=12dB, **WLCSP-12**	1.76		W
		VDD=5V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **QFN-20**	3.03		W
		VDD=5V RL = 4 Ohm + 33 µH and Total Harmonic Distortion+Noise (THD+N) = 10%, Gain=12dB, **WLCSP-12**	3.2		W
THD+N	Total Harmonic Distortion + Noise	R_L = 8 Ω + 33 µH, f=1kHz, P_O = 0.15 W, Gain=12dB	0.017		%
e_{OS}	Output Noise	A-Weighted, 20Hz-20kHz, no DAC input signal	11.8		µVrms
PSRR	Power Supply Rejection Ratio (Note 1)	DC, VDD = 3.2V – 4.2V, amplifier voltage GAIN = 6dB	85		dB
		f_{RIPPLE} = 1020Hz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	82	60	dB
		f_{RIPPLE} = 4kHz, V_{RIPPLE} = 100mV_{P_P} amplifier voltage GAIN = 6dB	77		dB
Fres	Frequency Response	F = 20Hz ~ 20KHz, 1Watt, R_L = 8 Ω + 33 µH	+0.06/ -0.06		dB
V_{OS}	Output Offset Voltage	Idle Channel, Gain= 6dB	±1	±5	mV
Kpop	Pop and Click Noise	A-weighted, Idle DAC input, toggling clocks on/off, Gain= 6dB	0.026		mVrms
		A-weighted, Idle DAC input, toggling EN pin with clocks running, Gain= 6dB	0.019		mVrms
Fsw	Switching Frequency	Average	300	400	kHz
Class-D					
Neff	Power Efficiency	Output Power = 1.48W, VDD = 4.2 V	91		%

***Note 1** : PSRR = 20 x LOG10(GAIN x ΔVDD/Δ(SPKP-SPKN)) dB*

5.4 Digital Input Parameters

Digital Inputs FS, BCLK, DACIN & EN.

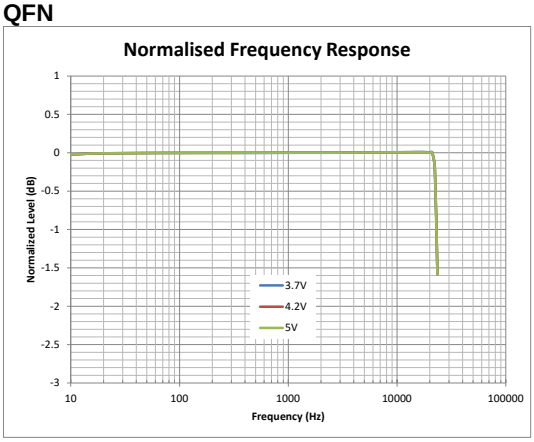
Parameter	Symbol	Comments/Conditions	Min	Max	Units
Input LOW level	V_{IL}	VDD = 2.5V – 5.25V		0.4	V
Input HIGH level	V_{IH}	VDD = 2.5V – 5.25V	1.4*		V
Input Leakage Current	I_{IL}	VDD = 2.5V – 5.25V	-0.001	+0.001	mA

Note: I2S signals can be 1.8V

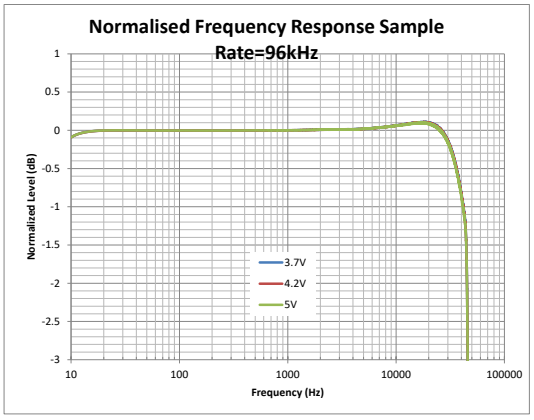
5.5 Typical Operating Plots

Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified.

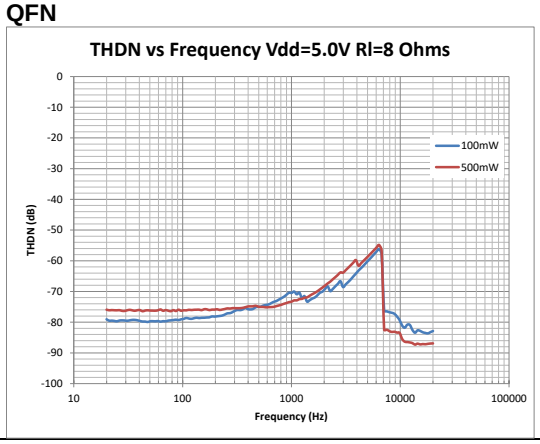
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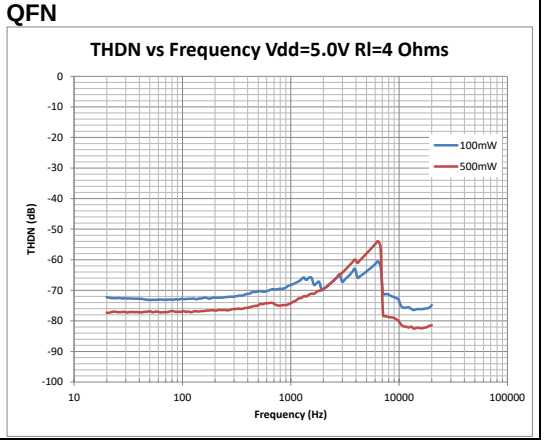
WLCSP



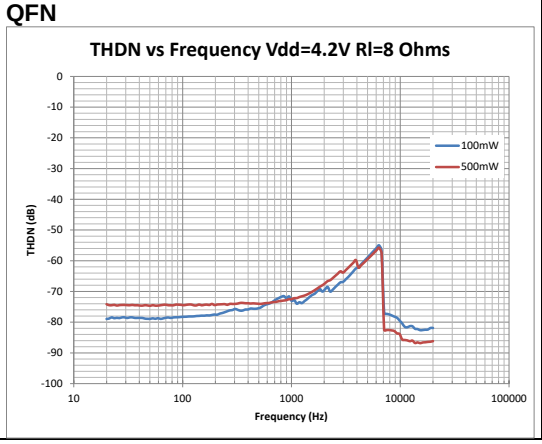
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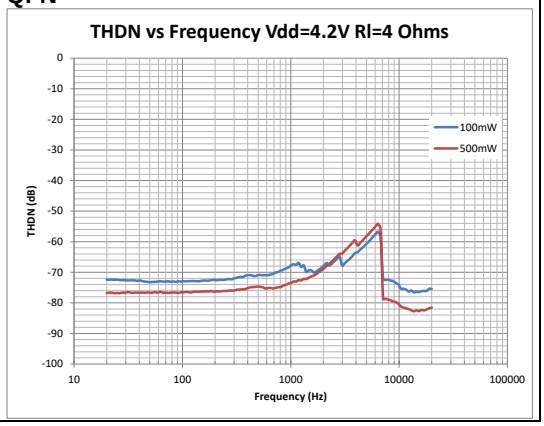
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QFN

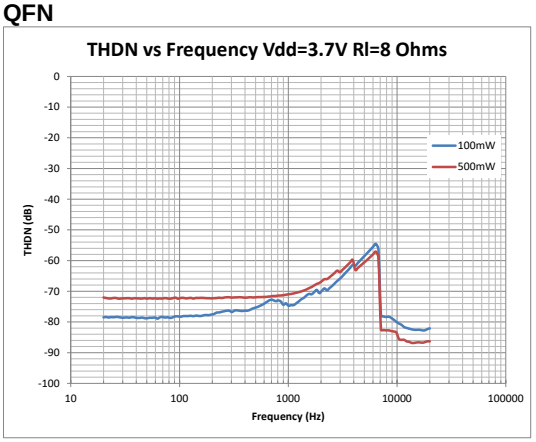


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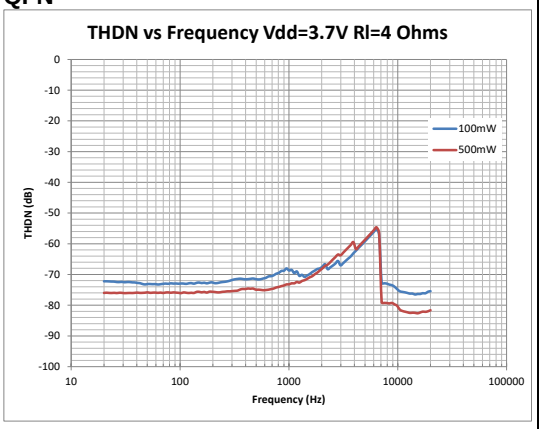


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified**.**

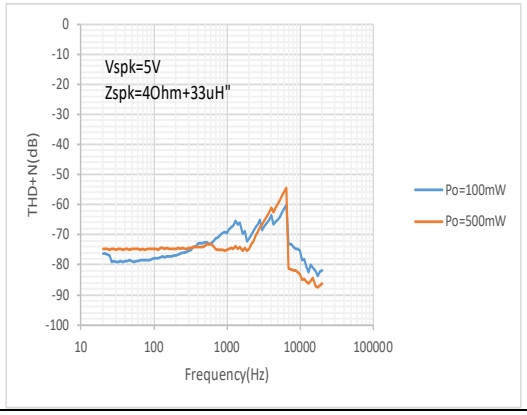
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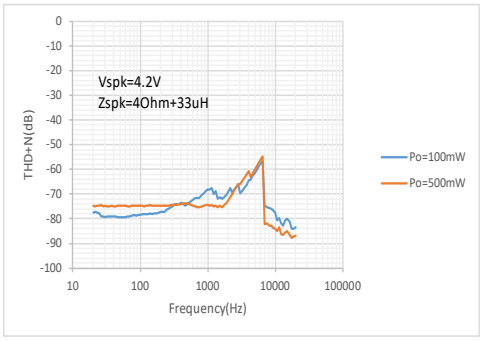
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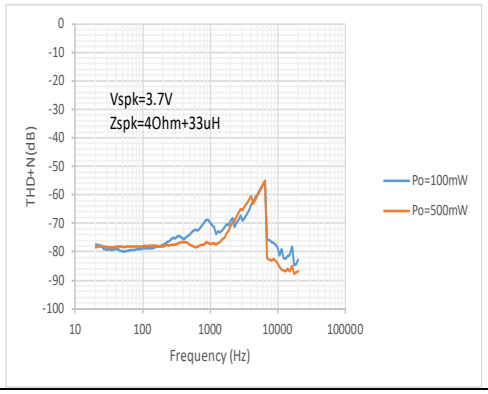
WLCSP



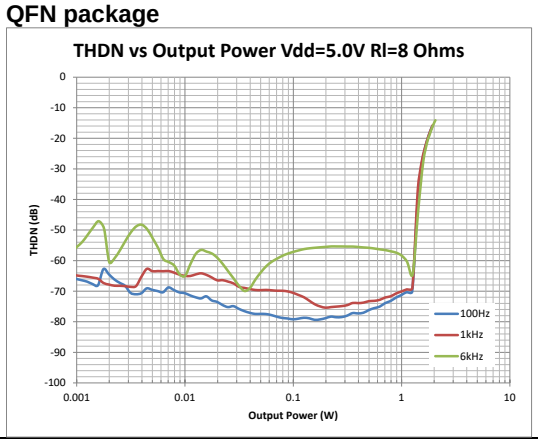
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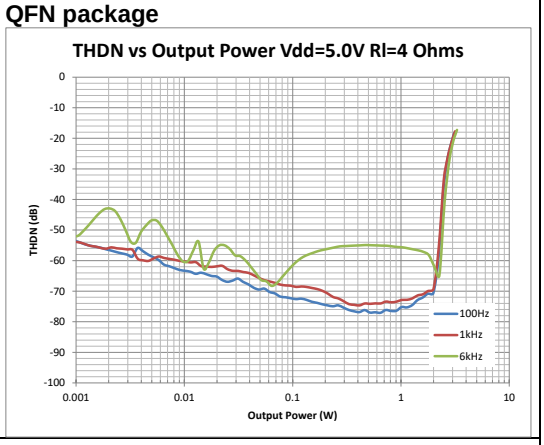
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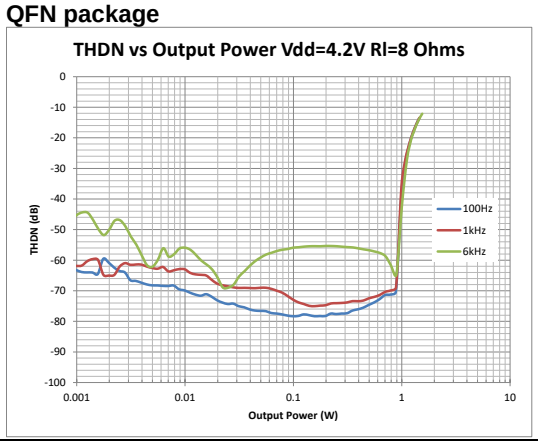
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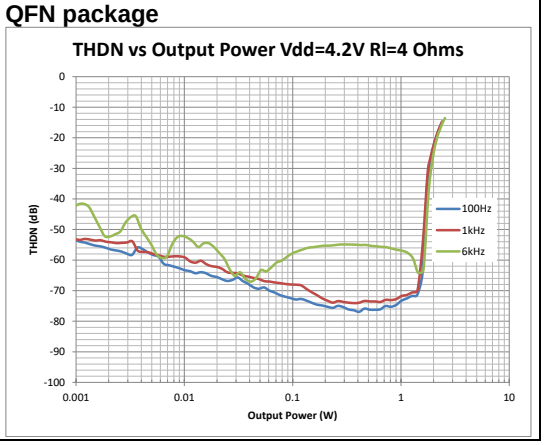
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QFN package

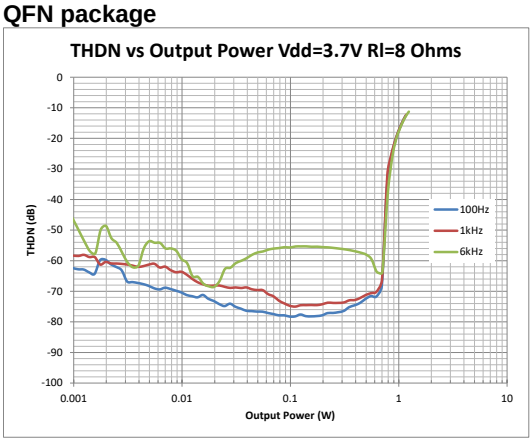


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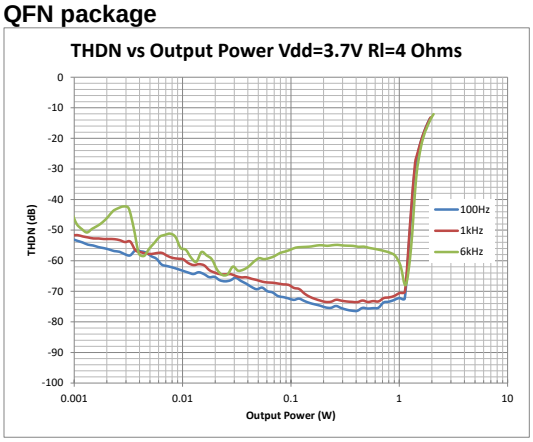


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified.

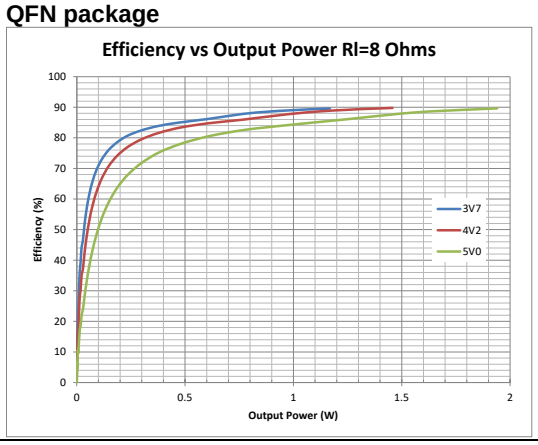
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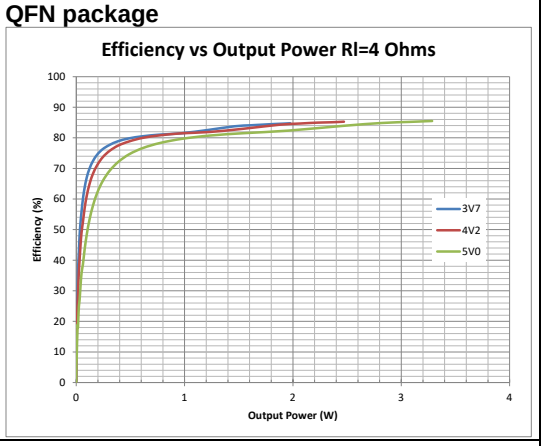
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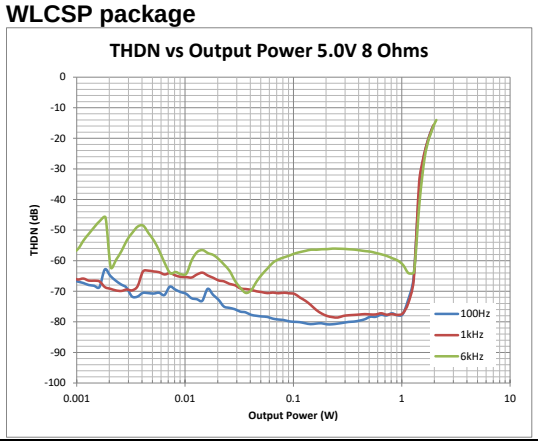
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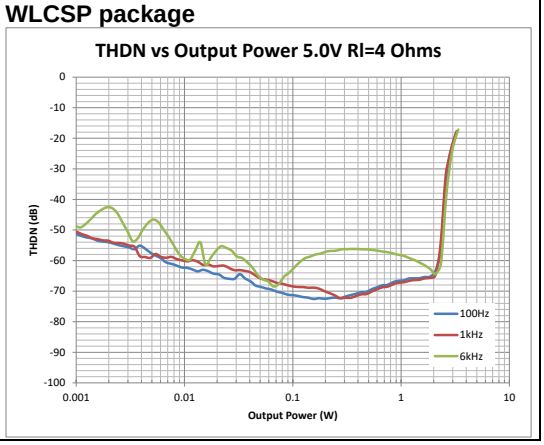
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WLCSP package

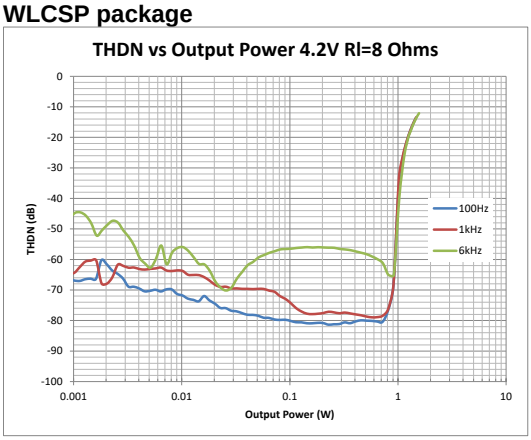


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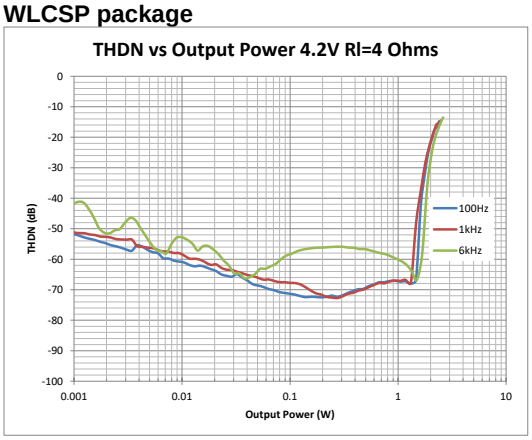


Conditions: VDD= 4.2V. R_L = 8 Ω + 33 µH, f = 1kHz, 48kHz sample rate, BCLK=12.288MHz, T_A = 25°C, gain=12dB, unless otherwise specified.

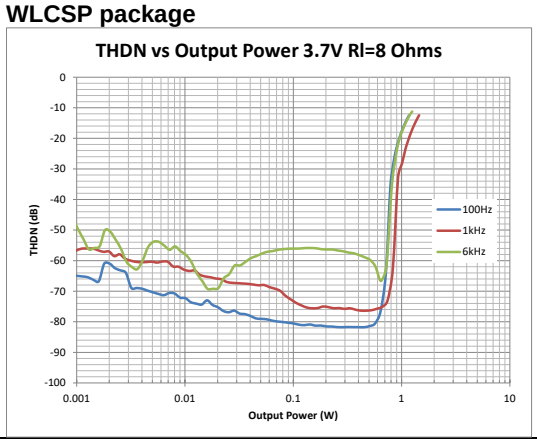
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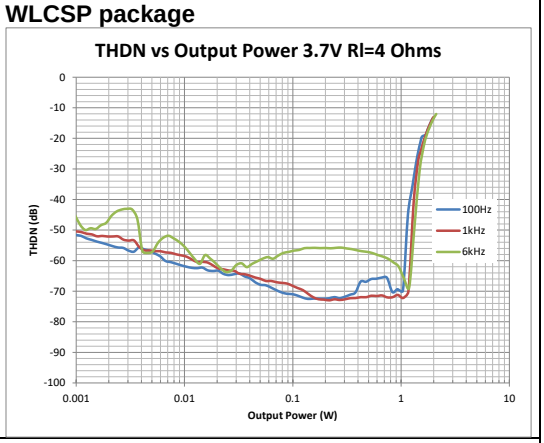
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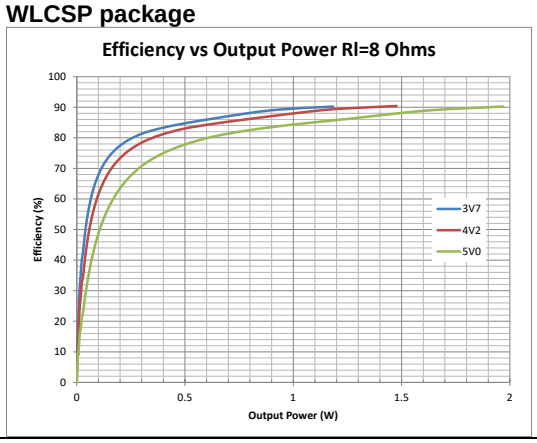
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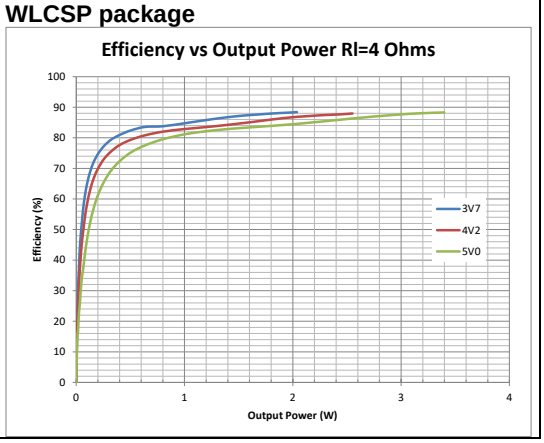
WLCSP package



WLCSP package



WLCSP package



6 FUNCTIONAL DESCRIPTION

This chapter provides detailed descriptions of the major functions of the NAU8315/NAU83U15 Amplifier.

6.1 Inputs

The NAU8315/NAU83U15 provides digital inputs to acquire and process audio signals with high fidelity and flexibility. The audio input path is from an I2S/PCM Interface, using the FSL, FSR, BCLK & DACIN pins.

The device is enabled by setting the EN pin high and disabled by setting EN to 0V. The EN, FSL, FSR, BCLK & DACIN pins all have a low input threshold voltage to allow for operation from a host with low IO supply voltage.

The GAIN input pin is a special input pin which essentially is an ADC input. The ADC tied to this pin has 5 decision levels and can therefore select 5 modes of operation each.

The GAIN input pin can be configured as shown in the table below. The GAIN set represents the signal voltage gain of the differential DAC outputs to the differential modulator outputs or speaker outputs. The differential DAC full scale reference is 1.8Vpk. Note that on the 9-Ball WLCSP package the gain is set to 12dB fixed.

Table 2 GAIN Configurations for the NAU8315/NAU83U15

Gain Mode #	GAIN (dB) MODE	-6dBFs Output (Vpk)	Min Reference Tolerance VDD = 2.5V (Vpk)	Max Reference Tolerance VDD = 5.25V (Vpk)	GAIN Pin Configuration
1	9	2.535	2.515	2.535	GAIN pin tied to VSS
2	3	1.265	1.268	1.293	GAIN pin tied to VSS through 100 KOhm +/- 5% resistor
3	12	3.595	2.231 (clipping)	3.678	GAIN pin tied to VDD
4	Max. 12 CLIP ALC	3.595 (no clipping)	2.231 (clipping)	3.678	GAIN pin tied to VDD through 100 KOhm +/- 5% resistor
5	6	1.795	1.793	1.836	GAIN pin floating

The GAIN input ADC converts the input levels set by the external pin configuration and internal voltage dividers into a digital representation that sets the internal GAIN mode. There are a total of 5 modes having different gains as shown above. Gain mode 4 also enables the CLIP detection ALC, which then allows the gain to be reduced automatically as the supply voltage decreases.

The FSR & FSL input pins are used to set the I2S and PCM interface modes. The table below shows the modes supported.

Table 3 Audio Interface Configurations for the NAU8315/NAU83U15

Interface Mode #	Interface MODE	FSL Pin Configuration	FSR Pin Configuration
1	Power Down or Standby	tied to VDD or VSS	tied to VDD or VSS
2	Left Channel I2S	Toggling with valid BCLK/FSL ratio and FSL is high for more than 2 BCLK rising edges	tied to VDD or VSS
3	Right Channel I2S	tied to VDD or VSS	Toggling with valid BCLK/FSR ratio and FSR is high for more than 2 BCLK rising edges
4	I2S (L+R)/2	Toggling with valid BCLK/FSL ratio and FSL is high for more than 2 BCLK rising edges. FSL & FSR signals are the same.	Toggling with valid BCLK/FSR ratio and FSR is high for more than 2 BCLK rising edges. FSL & FSR signals are the same.
5	16 bit PCM Timeslot 0	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VSS
6	16 bit PCM Timeslot 1	tied to VSS	Toggling with valid BCLK/FSR ratio and FSR is high for less than 2 BCLK rising edges
7	16 bit PCM Timeslot 2	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges	tied to VDD
8	16 bit PCM Timeslot 3	tied to VDD	Toggling with valid BCLK/FSR ratio and FSR is high for less than 2 BCLK rising edges
9	16 bit PCM (Timeslot0+Timeslot1)/2	Toggling with valid BCLK/FSL ratio and FSL is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.	Toggling with valid BCLK/FSR ratio and FSR is high for less than 2 BCLK rising edges. FSL & FSR signals are the same.

I2S data is 24-bit by default. For the PCM Timeslot interface modes the host can also sent 24 bit or 32 bit data. However, only the 16 MSB bits will be used to process the audio in this mode.

Internal mask options can be used to select other timeslots or 24-bit data or 32-bit PCM data upon special request.

6.2 Outputs

The NAU8315/NAU83U15 Mono Class-D PWM Amplifier has a gain range from 3dB to 12dB, and is powered by a separate power supply VDD, which can go up to 5V. This amplifier is capable of delivering up to 3.2W into a 4Ω load with a 5V supply.

6.3 Digital Interfaces

Audio data is passed to the device through a serial data interface compatible with industry standard I2S and PCM devices, using the FSL, FSR, BCLK & DACIN pins. The NAU8315/NAU83U15 has no serial interface for control input. Operating modes are defined by the external pin configurations.

6.4 Power Supply

This NAU8315/NAU83U15 has been designed to operate reliably under a wide range of power supply conditions and Power-On/Power-Off sequences. However, the Electro Static Detection (ESD) protection diodes between the supplies and the IO pins impact the application of the supplies.

6.5 Power-On-and-Off Reset

The NAU8315/NAU83U15 includes a Power-On-and-Off Reset circuit on-chip. The circuit resets the internal logic control at VDD supply power-up and this reset function is automatically generated internally when power supply is too low for reliable operation. Typical reset thresholds are **1.88** V for VDD during a power-on ramp, and **1.61** V for VDD during a power-down ramp. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held ON while the power level for VDD is below the threshold. Once the power level rises above the threshold, the reset is released. Once the reset is released, the device will respond to control from external inputs.

An additional internal RC filter-based circuit is added which helps the circuit to respond for fast ramp rates (~3 µsec) and to generate the desired reset period width (~3 µsec at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50 nsec.

In addition, setting the enable pin ‘EN’ low will reset the internal logic.

6.6 Power Up & Down Sequence

A diagram of the typical power up sequence is shown in the figure below. At first, the power supply is ramped up.

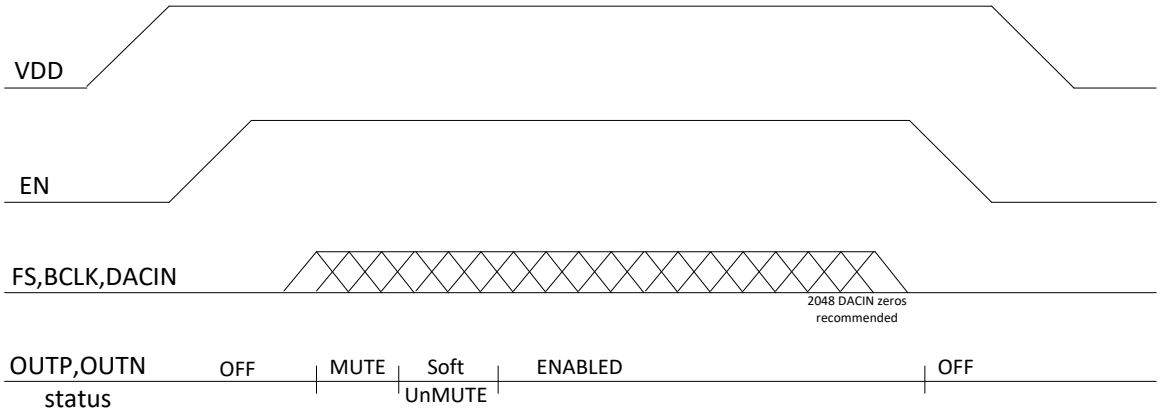


Figure 5 NAU8315/NAU83U15 Power Up & Down Sequence

Once the supply is powered up, the enable pin 'EN' can be set high in order to set the device in standby state. Note that the 'EN' pin can also ramp up the same time as the supply voltage. During the standby state the outputs OUTN & OUTP are still off. After enabling VDD & EN, the BCLK detection circuit is activated. External clocks and data can be applied right away if needed. Once the FS & BCLK are applied the clock detection module will validate the BCLK/FS ratio and set the internal clock dividers. When a valid BCLK/FS ratio is detected and the clock dividers are set, a 4-millisecond mute period is enabled during which all circuits are powered up and the DAC digital volume control is in the muted state. The mute period is followed by a soft-unmute, which gradually increases the DAC digital volume to full scale. After this event the signal path is fully active, and the outputs are fully enabled. At the end of playback, it is recommended to add 2048 zero samples to the DACIN input for a pop-less shutdown. When either one or both FS & BCLK clocks is stopped the clock detection circuit will power down the device. The detection time depends on the clock frequency used but is approximately 50usec. Once detected, the output drivers will shut down.

6.7 Clocking and Sample Rates

The internal clocks for the NAU8315/NAU83U15 are derived from the external BCLK clock source. This master system clock can set directly by the BCLK input, or it can be generated from a clock multiplier using the BCLK as a reference.

6.7.1 Clock Control and Detection

The NAU8315/NAU83U15 includes a Clock Detection circuit that is used to enable and disable the audio paths. The actual power up/down is gated by the clock detection circuit. The block diagram of the clock detection circuit is shown in **Figure 6**.

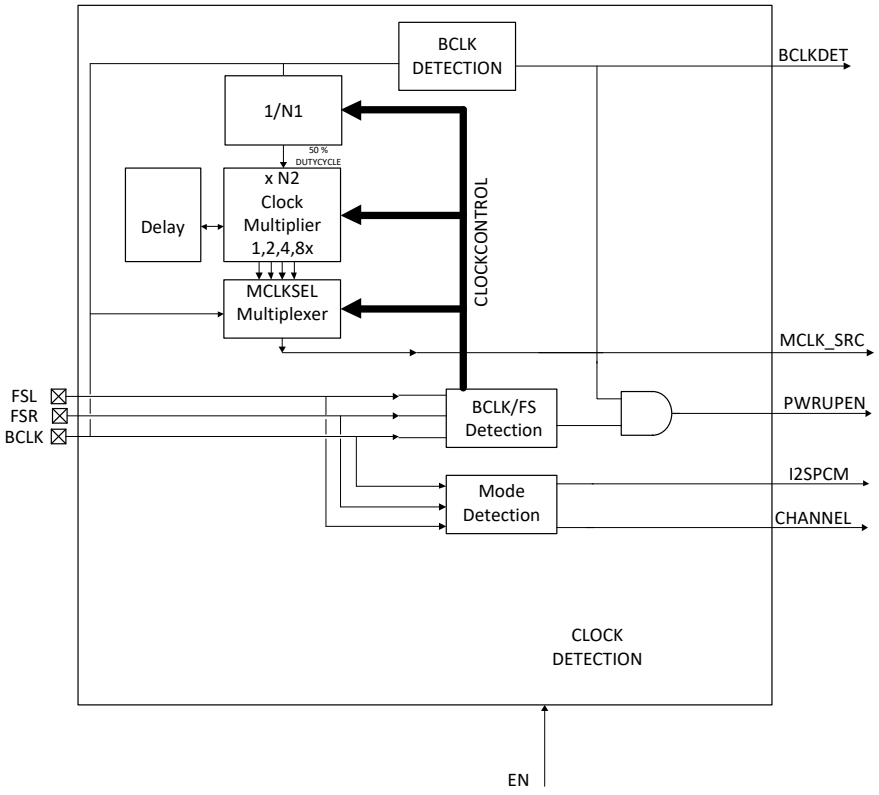


Figure 6 NAU8315/NAU83U15 Clock Detection Circuit

Clock Detection by the NAU8315/NAU83U15 uses the BCLK FSL, FSR and EN to control the internal PWRUPEN signal and set the clock divider ratios.

6.7.2 Automatic Power Control and Mute

Clock detection and automatic power control in the NAU8315/NAU83U15 is enabled by meeting two conditions, depending on the configuration. If all conditions are met, the PWRUPEN signal will be asserted to 1. If any of the conditions are not met, the PWRUPEN signal is set to 0.

The conditions for generating the PWRUPEN signal are:

1) The NAU8315/NAU83U15 has custom logic clock detection circuits that detect if BCLK is present. Upon BCLK detection, the detector output BCLKDET goes to 1. When the BCLK disappears, BCLKDET goes back to 0. Up to 1 µsec is required to detect BCLK and the BCLK release time is about 50 µsec.
2) The clock detection logic also needs to detect the ratio BCLK /FS of 32, 50, 64, 100, 125, 128, 200, 250, 256, 400, 500.

The PWRUPEN signal is capable of controlling all the analog power consuming blocks.

A Mode Detection circuit also determines one of the I2S/PCM operating mode and channel (as shown in Table 3) once a valid BCLK/FS ratio is detected.

When PWRUPEN goes high an internal sequence is triggered to bring up analog functions. This includes an analog MUTE to allow stabilization of internal analog blocks, followed by a soft unmute of the DAC. The analog MUTE time is 4ms. The soft unmute then ramps the gain 512 MCLK_SRC periods per gain step. For the 512 setting, the soft unmute takes 256 * 512 * Tmclk_src seconds to reach 0dB (10ms for 12.288MHz MCLK_SRC). This ensures pop free startup of the amplifier. An example of this startup is shown in figure below.

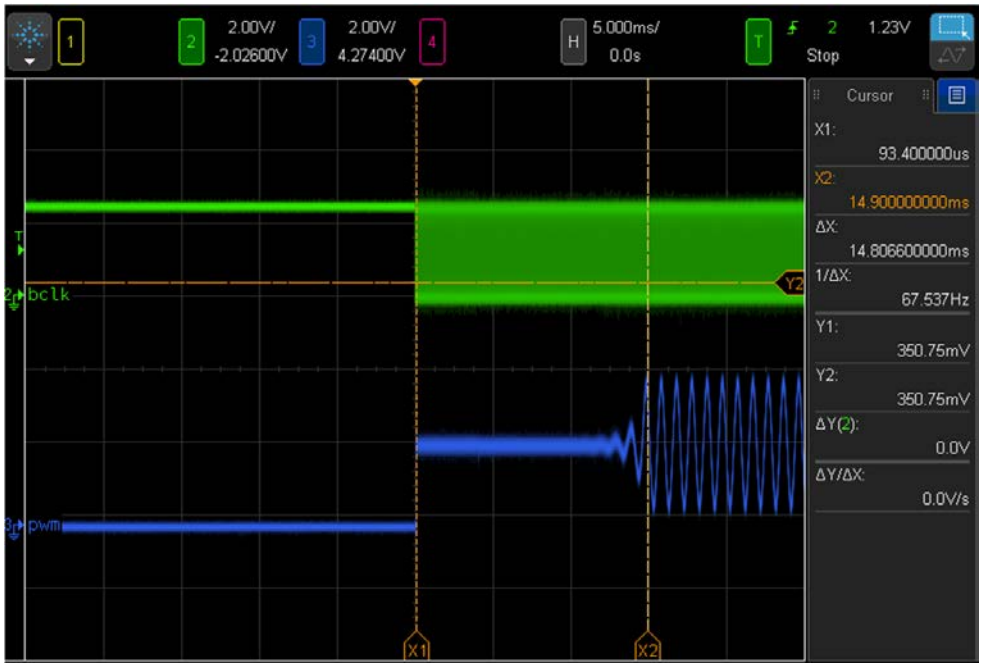


Figure 7 PWRUPEN startup sequence.

Before reaching the DAC the incoming PCM signal is processed by a digital signal path. To ensure complete flushing and transient free audio of this path it is recommended that 2048 zero samples are sent to the device before stopping clocks. The DAC soft unmute function is also beneficial for eliminating any audio transients from audio path.

6.7.3 Input Clock Rates

The range of the input clocks is shown in **Table 4**.

Table 4 Range of Input Clocks

Signal	Min	Max
Frame Synch (FS) (kHz)	8	96
Bit Clock BCLK (MHz)	1.4112	24.576

6.7.4 Sample and Over Sampling Rates

Table 5 BCLK/FS ratios and Over Sampling Rates

	Lower	Upper				
BCLK/FS	**Decision**	**Decision**	**N1**	**N2**	**MCLK_SRC/FS**	**OSR**
ratio	Threshold	Threshold				
32	31	33	1	8	256	64
50	49	51	1	8	400	100
64	63	65	2	8	256	64
100	99	101	2	8	400	100
125	124	126	2	8	500	100
128	127	129	2	4	256	64
200	199	201	2	4	400	100
250	249	251	2	4	500	100
256	255	257	1	1	256	64
400	399	401	1	1	400	100
500	499	501	1	1	500	100

Table 6 Ranges of Sampling Frequencies and BCLK Rates

BCLK/FS Ratio	FS (kHz)		BCLK (MHz)	
	Min	Max	Min	Max
32	44.1	96	1.4112	3.072
50	32	48	1.600	2.400
64	44.1	96	2.8224	6.144
100	32	48	3.200	4.800
125	24	48	3.000	6.000
128	24	96	3.072	12.288
200	16	48	3.200	9.600
250	12	48	3.000	12.000
256	8	96	2.048	24.576
400	8	48	3.200	19.200
500	8	48	4.000	24.000

The MCLK_SRC frequency is defined as:

F_MCLK_SRC = N2 x F_BCLK / N1

For BCLK/FS ratios of 32 & 50 a low jitter BCLK source with accurate duty cycle must be used.

6.8 Automatic Level Control

The digital Automatic Level Control (ALC) function supports the DAC digital audio path of the NAU8315/NAU83U15. It can be enabled as by setting the GAIN pin to 12dB gain with ALC. This function can be used to manage the gain to optimize the signal level at the output of the Class-D Amplifier by automatically amplifying input signals that are too small or automatically decreasing the amplitude signals that are too loud. The ALC is designed such that it adjusts the output level in order to prevent clipping. This may be use-full in battery operated applications, where the battery supply voltage decreases as the battery discharges. At lower supply voltages the outputs will more likely clip at higher output levels. In such case, the ALC would decrease the output level just below the clipping level and maintain high quality sound as well as decreasing the peak power drain from the battery.

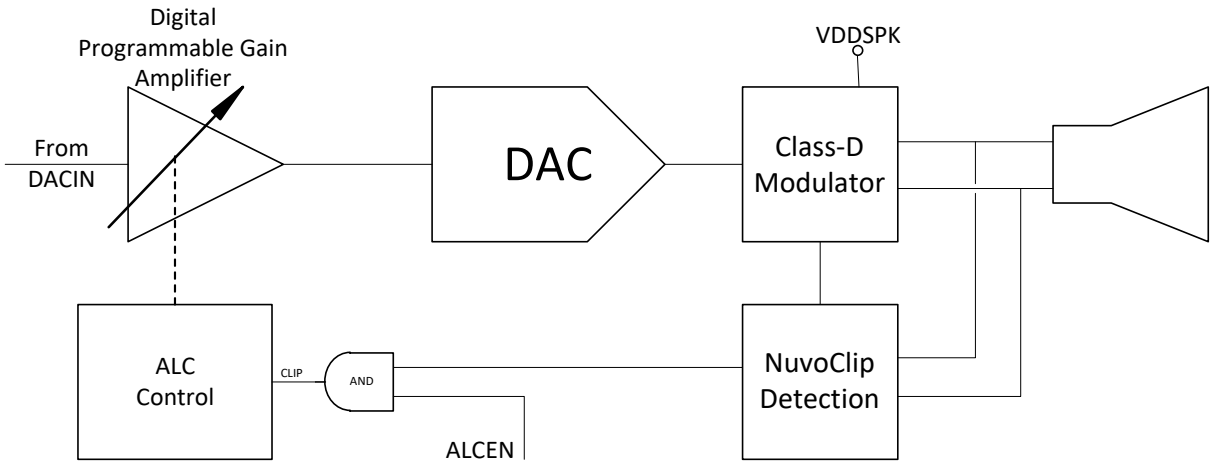


Figure 8 ALC Control Loop Block Diagram

6.8.1 ALC Operation

A clip detection signal is provided by the clip detection circuit as soon as the input signal is clipping at its peak levels. The ALC block then ramps down the gain at the pre-programmed ALC Attack Time rate. This continues until the clipping detection no longer detects a clipping signal or until the maximum gain decrement per clipping event is reached. When the clipping is no longer occurring, the ALC gain is held for the hold time. The ALC gain is then ramped up to the target following the pre-programmed ALC Release Time rate.

6.8.2 ALC Parameter Definitions

ALC Minimum Gain (ALCMIN): This sets the minimum allowed gain during all modes of ALC operation. This is useful to keep the ALC operating range close to the desired range for a given application scenario.

ALC Attack Time (ALCATK): Attack time refers to how quickly a system responds to a clipping event. Typically, attack time is much faster than decay time.

ALC Decay Time (ALCDCY): Decay time refers to how quickly a system responds after the hold time. Typically, decay time is much slower than attack time. When no more clipping events occur, the gain will increase at a rate determined by this parameter.

ALC Hold Time (ALCHLD): Hold time refers to the duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU8315/NAU83U15, the hold time value is the duration from the last clipping event before there is an actual gain increase during the decay time.

CLIP_GAINADJUST sets the maximum gain decrease per clipping event. During a clipping even the gain decreases by 0.250dB (1-1/64) per attack time step until the clipping event no longer occurs or the maximum gain reduction limit set in CLIP_GAINADJUST has been reached or the ALC Minimum Gain is reached.

6.9 Device Protection

The NAU8315/NAU83U15 includes the following types of device protection:

- Over Current Protection (OCP)
- Under Voltage Lock Out (UVLO)
- Over Temperature Protection (OTP)
- Clock Termination Protection (CTP)

Over Current Protection is provided in the NAU8315/NAU83U15. If a short circuit is detected on any of the pull-up or pull-down devices on the output drivers for at least 14µs, the output drivers will be disabled for 100ms. The output drivers will then be re-enabled and checked for a short circuit again. If the short circuit is still present for another 14µs, the cycle will repeat until the short circuit has been fixed. The short circuit threshold is set at 2.1A.

Under Voltage Lock Out (UVLO) provides Supply Under Voltage Protection in the NAU8315/NAU83U15 If the VDD drops under 2.1V, the output drivers are disabled, however, the NAU8315/NAU83U15 control circuitry will still operate. This is useful to help avoid the battery supply voltage dropping before the host processor can safely shutdown the devices on the system. If the VDD drops below 1.61V, the internal power-on-reset will activate and put the class-D driver in power down state.

Over Temperature Protection (OTP) is provided in the event of thermal overload. When the device internal junction temperature reaches 143°C, the NAU8315/NAU83U15 will disable the output drivers. Once the device cools down to a safe operating temperature (123°C) for at least 100us, the output drivers will be re-enabled.

Clock Termination Protection (CTP) is provided in the NAU8315/NAU83U15. If the FS and/or BCLK clock stops running, the NAU8315/NAU83U15 automatically shuts down the Class-D driver and therefore prevents DC voltages to remain at the outputs.

6.10 Power-up and Power-Down Control

When the supply voltage ramps up, the internal power on reset circuit is triggered. At this time, all internal circuits will be set to the power-down state. The device can be enabled by setting EN to VDD and starting the clocks. Upon starting the clocks, the device will go through an internal power-up sequence in order to minimize ‘pops’ on the speaker output. The complete power-up sequence requires about 14 msec. The device will typically power down in about 22 µsec, when the clocks are stopped.

NOTE: It is important to keep the input signal at zero amplitude or enable the mute condition in order to minimize ‘pops’ when the clocks are stopped.

6.11 Bypass Capacitors

Bypass capacitors are required to remove the AC ripple on the VDD pins. The value of these capacitors depends on the length of the VDD trace. In most cases, 2 x 4.7 µF and 0.1 µF are sufficient to achieve good performance.

6.12 Filters

The NAU8315/NAU83U15 is designed for use without any filter on the output line. However, the NAU8315/NAU83U15 may be used with or without various types of filters, depending on the needs of the application.

6.12.1 Class D without Filters

The NAU8315/NAU83U15 is designed for use without any filter on the output line. That means the outputs can be directly connected to the speaker in the simplest configuration. This type of filter-less design is suitable for portable applications where the speaker is very close to the amplifier. In other

words, this is preferable in applications where the length of the traces between the speaker and amplifier is short. **Figure 9** illustrates this simple configuration.

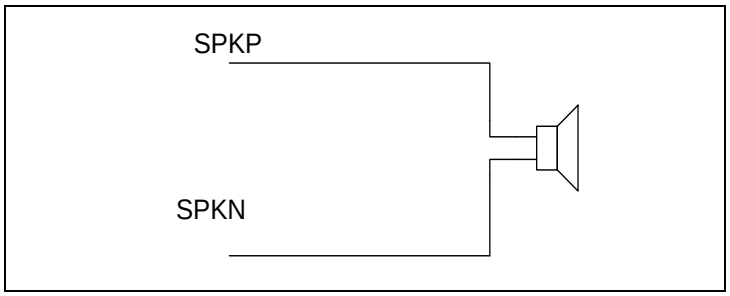


Figure 9 NAU8315/NAU83U15 Speaker Connections without Filter

6.12.2 Class D with Filters

In some applications, shorter trace lengths are not possible because of speaker size limitations and other layout reasons. In these applications, long traces will cause EMI issues. Several types of filter circuits are available to reduce the EMI effects. These are Ferrite Bead Filters, LC filters, Low-Pass LCR Filters, and High-Pass Filters.

Ferrite Bead Filters are used to reduce high-frequency emissions. The characteristic of a Ferrite Bead Filter is such that it offers higher impedance at high frequencies. For better EMI performance, select a Ferrite Bead Filter which offers the highest impedance at high frequencies, so that it will attenuate the signals at higher frequencies. The typical circuit diagram using a Ferrite Bead Filter for each output to the speaker is shown **Figure 10**.

NOTE: Usually, the ferrite beads have low impedance in the audio range, so they will act as pass-through filters in the audio frequency range.

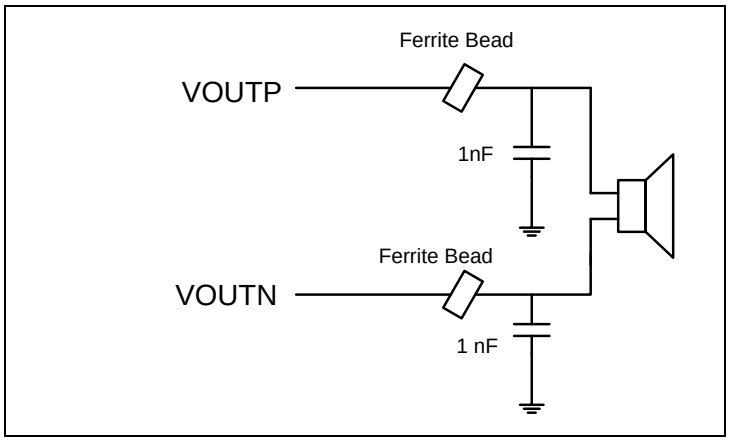


Figure 10 NAU8315/NAU83U15 Speaker Connections with Ferrite Bead Filters

LC Filters is used to suppress low-frequency emissions. The diagram in **Figure 11** shows the NAU8315/NAU83U15 outputs connected to the speaker with an LC Filter circuit. R_L is the resistance of the speaker coil.

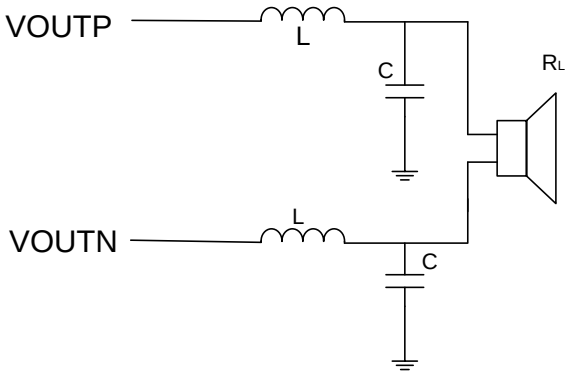


Figure 11 NAU8315/NAU83U15 Speaker Connections with LC Filters

Low-Pass LCR Filters may also be useful in some applications where long traces or wires to the speakers are used. **Figure 12** shows the speaker connections using standard Low-Pass LCR Filters.

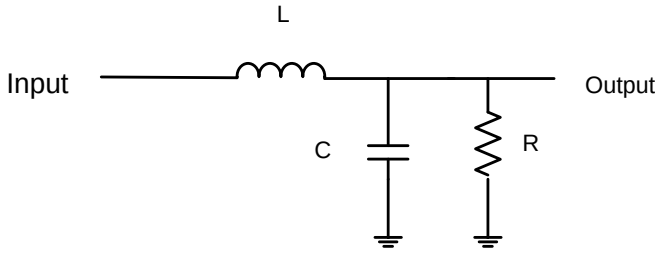


Figure 12 NAU8315/NAU83U15 Speaker Connections with Low-Pass Filters

The following equations apply for critically damped (ζ = 0.707) standard Low-Pass LCR Filters:

$$2\pi fc = \frac{1}{\sqrt{(LC)}} \qquad fc \text{ is the cut-off frequency}$$

$$\zeta = 0.707 = \frac{1}{2R} * \sqrt{\frac{L}{C}}$$

NOTE: The L and C values for differential configuration can be calculated by duplicating the single-ended configuration values and substituting RL = 2R.

6.13 Control

NAU8315/NAU83U15 Audio Interface is set to default I2S and PCM time slot modes as described in the FSL & FSR operating mode table. Other modes may be feasible through metal mask option changes upon special request.

6.13.1 Digital Audio Interface

NAU8315/NAU83U15 is an I2S or PCM Timeslot slave device. In I2S Slave Mode, an external controller supplies BCLK (bit clock) and the frame synchronization or FS signal. Data is latched on the rising edge of BCLK.

NAU8315/NAU83U15 reads 24-bit I2S data on DACIN. For the BCLK/FS rate of 32, only the 16 MSB bits are read.

6.13.1.1 I2S Audio Data

In I2S Mode, the MSB is clocked on the second BCLK rising edge after the FS transitions. When FS is LOW, Left Channel data is received; when FS is HIGH, Right Channel data is received. This can be seen in **Figure 13.**

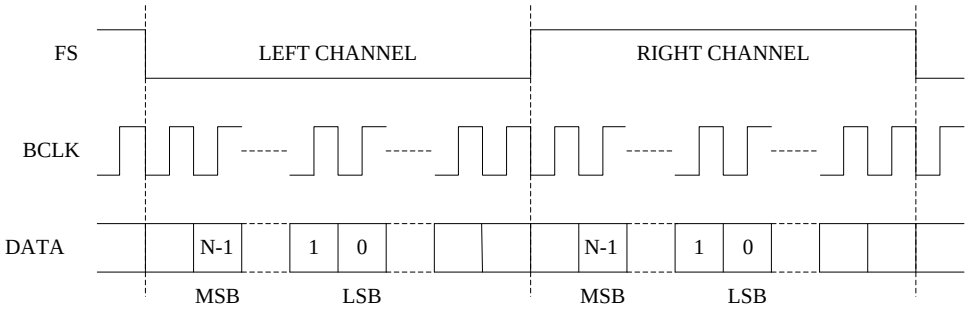


Figure 13 I2S Audio Data

6.13.1.2 PCM Time Slot Audio Data

PCM Time Slot Mode is used to delay the time at which the DAC data is clocked into the device. This can be useful when multiple NAU8315/NAU83U15 chips or other devices share the same audio bus. This will allow the audio from the chips to be delayed around each other without interference.

Normally, the DAC data is clocked immediately after the Frame Sync (FS); however, in PCM Time Slot Mode, the audio data can be delayed. These delays can be seen before the MSB in **Figure 14**.

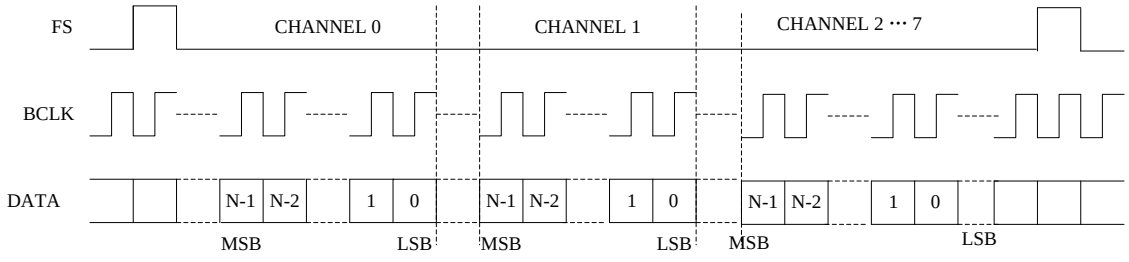


Figure 14 PCM Time Slot Audio Data

6.13.2 Digital Audio Interface Timing Diagrams

6.13.2.1 I2S Audio Interface

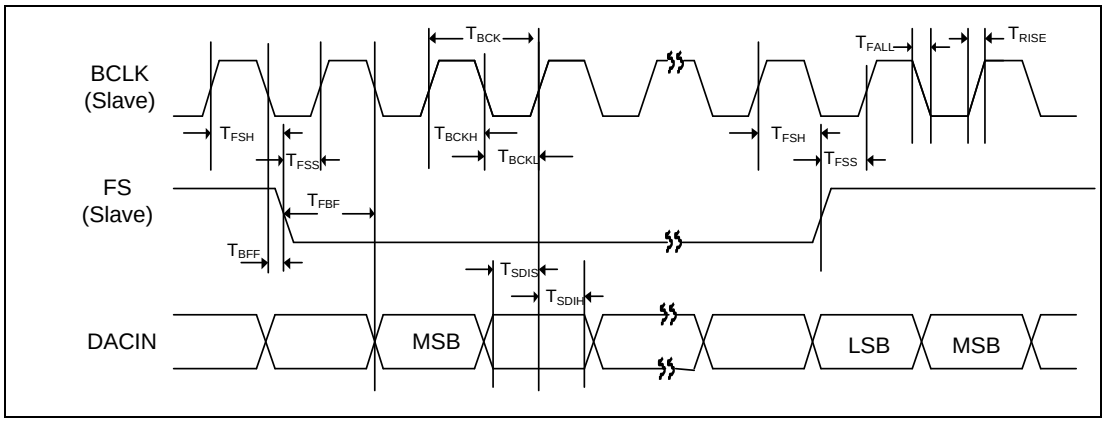


Figure 15 I2S Audio Interface

6.13.2.2 PCM Audio

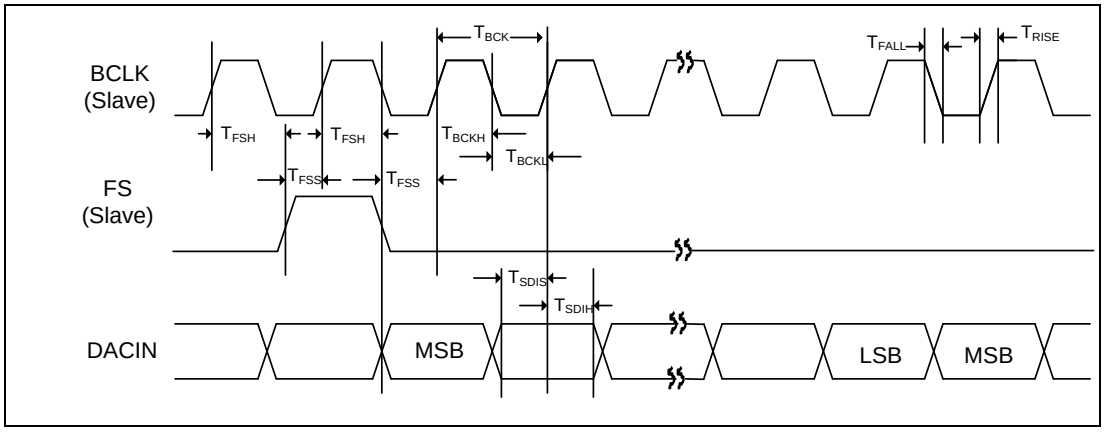


Figure 16 PCM Audio Interface

BCLK=3.072MHz, Fs=48KHz, 64Bit, VDD 2.5 - 5.25V, Room Temperature

Description	Symbol	Min	Typ	Max	Unit
BCLK High Pulse Width	T_{BCKH}	20	---	---	ns
BCLK Low Pulse Width	T_{BCKL}	50	---	---	ns
Fs to BCLK Rising Edge Setup Time	T_{FSS}	20	---	---	ns
BCLK Rising Edge to FS Hold Time	T_{FSH}	10	---	---	ns
Rise Time for All Audio Interface Signals	T_{RISE}	---	---	$0.135T_{BCK}$	ns
Fall Time for All Audio Interface Signals	T_{FALL}	---	---	$0.135T_{BCK}$	ns
DACIN to BCLK Rising Edge Setup Time	T_{DIS}	15	---	---	ns
BCLK Rising Edge to DACIN Hold Time	T_{DIH}	15	---	---	ns
BCLK falling edge to FS falling edge	T_{BFF}	0	---	---	ns
FS falling edge to BCLK falling edge	T_{FBF}	20	---	---	ns

Table 7 Digital Audio Interface Timing Parameter

7 APPLICATION CIRCUIT

7.1 Block Diagram

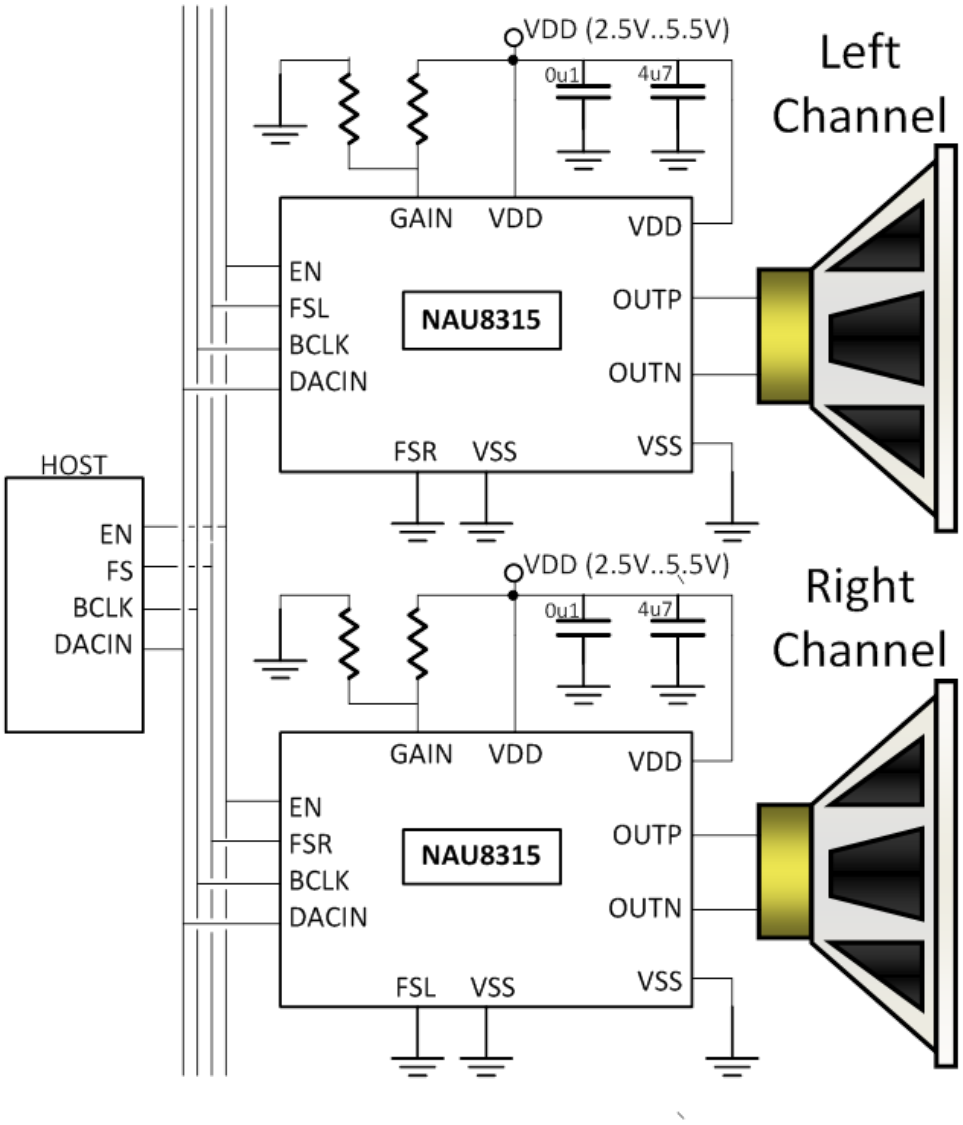


Figure 17 NAU8315/NAU83U15 Simplified System Diagram

7.2 Printed Circuit Board Layout Considerations

Good Printed Circuit Board (PCB) layout and grounding techniques are essential to achieve good audio performance. It is better to use low-resistance traces as these devices are driving low impedance loads. The resistance of the traces has a significant effect on the output power delivered to the load. In order to dissipate more heat, use wide traces for the power and ground lines.

7.2.1 PCB Layout Notes

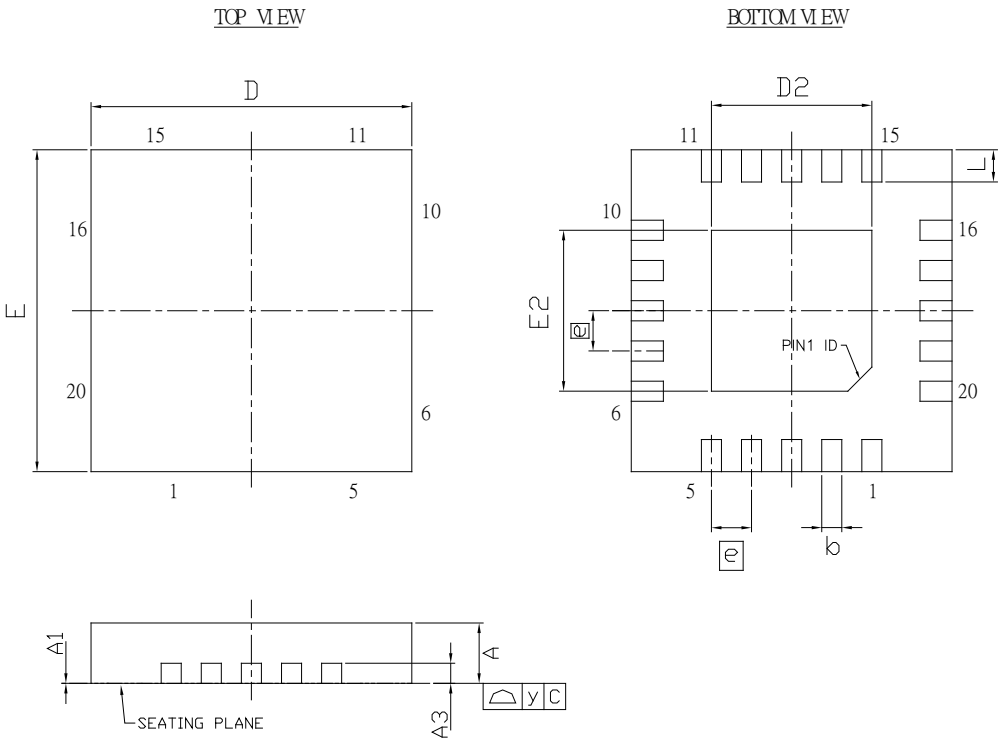
The Class-D Amplifier is a high-power switching circuits that can cause Electro Magnetic Interference (EMI) when poorly connected. Therefore, care must be taken to design the PCB eliminate Electro Magnetic Interference (EMI), reduce IR drops, and maximize heat dissipation.

The following notes are provided to assist product design and enhance product performance:

- Use a VSS plane, preferably on both sides, to shield clocks and reduce EMI
- Maximize the copper to the VSS pins and have solid connections to the plane
- Planes on VDD are optional
- The VDD connection needs to be a solid piece of copper
- Use thick copper options on the supply layers if cost permits
- Keep the speaker connections short and thick. Do not use VIAs
- Use a small speaker connector like a wire terminal block (Phoenix Contact)
- For better heat dissipation, use VIAs to conduct heat to the other side of the PCB
- Do not use VIA's to connect OUTP & OUTN. Use a direct top layer copper connection to the pins. Thick copper is preferred.
- Use large or multiple parallel VIAs to decoupling capacitors when connecting to a ground plane
- The digital IO lines can be shielded between power planes

8 PACKAGE DIMENSION

NAU8315/NAU83U15 Mono Class-D Amplifier is available in a small, 20 pin QFN package, using 0.5 mm pitch, as shown below.



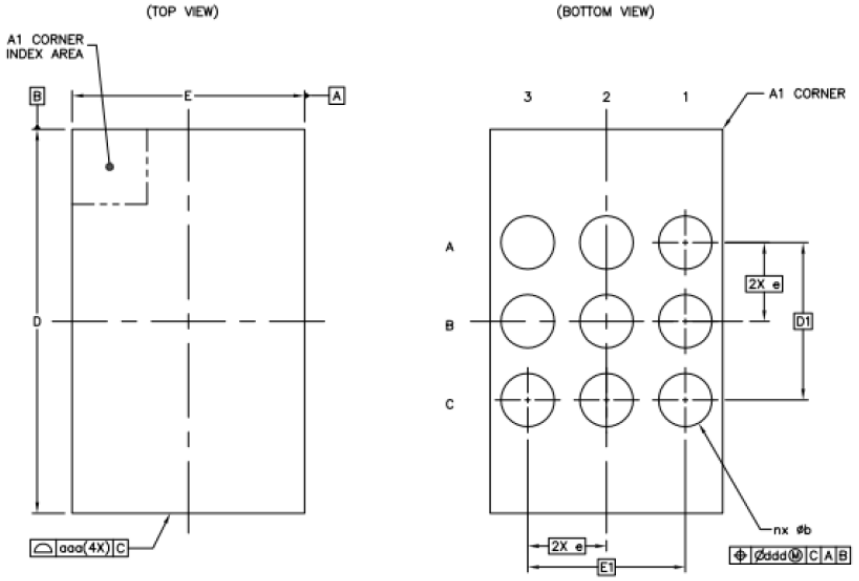
Controlling Dimension :Millimeters

SYMBOL	DIMENSION (MM)			DIMENSION (Inch)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.02756	0.02953	0.03150
A1	0	0.02	0.05	0	0.0079	0.00197
A3	0.203 REF			0.0079 REF		
b	0.18	0.25	0.30	0.00709	0.00984	0.01181
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
D2	1.90	2.00	2.10	0.0748	0.0787	0.0827
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
E2	1.90	2.00	2.10	0.0748	0.0787	0.0827
e	0.50 BSC			0.01969 BSC		
L	0.30	0.40	0.50	0.01181	0.01574	0.01969
y	0.08			0.00315		

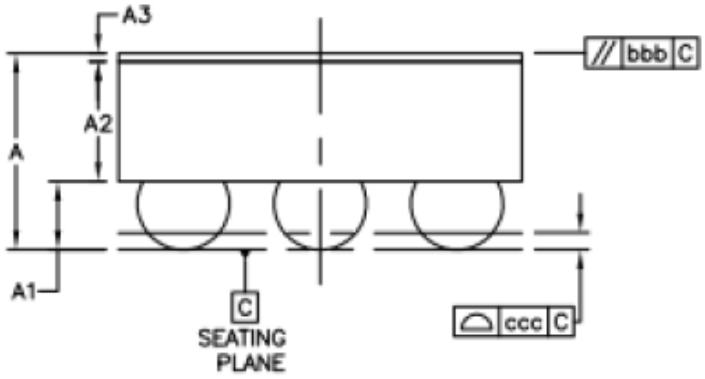
Note:D2,E2 by die size difference .

NAU8315/NAU83U15 QFN-20 Package

The NAU8315 Mono Class-D Amplifier is also available in a small, 9 Ball WLCSP package, using 0.4 mm pitch, as shown below.

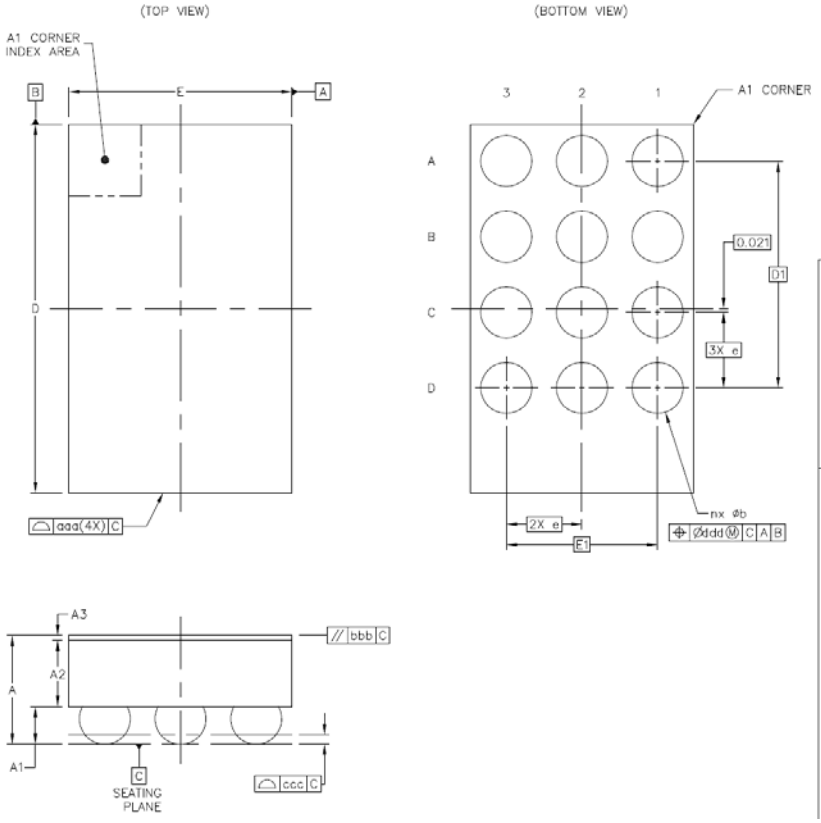


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.517	0.575	0.633
STAND OFF		A1	0.17	---	0.23
WAFER THICKNESS		A2	0.325	0.35	0.375
FILM THICKNESS		A3	0.022	0.025	0.028
BODY SIZE	X	E		1.18	
	Y	D		1.95	
BALL/BUMP PITCH	X	SE		---	BSC
	Y	SD		---	BSC
EDGE BALL CENTER TO CENTER	X	E1		0.8	BSC
	Y	D1		0.8	BSC
PITCH		e		0.4	BSC
BALL DIAMETER (SIZE)				0.25	
BALL/BUMP WIDTH		b	0.24	---	0.3
BALL/BUMP COUNT		n		9	
PACKAGE EDGE TOLERANCE		aaa		0.03	
WAFER FLATNESS		bbb		0.06	
COPLANARITY		ccc		0.05	
BALL/BUMP OFFSET (PACKAGE)		ddd		0.015	



NAU8315 WLCSP-9 Package

NAU8315 Mono Class-D Amplifier is also available in a small, 12 Ball WLCSP package, using 0.4 mm pitch, as shown below.



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.517	0.575	0.633
STAND OFF		A1	0.17	---	0.23
WAFER THICKNESS		A2	0.325	0.35	0.375
FILM THICKNESS		A3	0.022	0.025	0.028
BODY SIZE	X	E		1.18	
	Y	D		1.95	
BALL/BUMP PITCH	X	SE		---	BSC
	Y	SD		---	BSC
EDGE BALL CENTER TO CENTER	X	E1		0.8	BSC
	Y	D1		1.2	BSC
PITCH		e		0.4	BSC
BALL DIAMETER (SIZE)				0.25	
BALL/BUMP WIDTH		b	0.24	---	0.3
BALL/BUMP COUNT		n		12	
PACKAGE EDGE TOLERANCE		aaa		0.03	
WAFER FLATNESS		bbb		0.06	
COPLANARITY		ccc		0.05	
BALL/BUMP OFFSET (PACKAGE)		ddd		0.015	

NAU8315 WLCSP-12 Package

9 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU8315YG	4mm x 4mm	QFN-20	Green
NAU8315A31VG	1.95mm x 1.18mm	WLCSP-9	Green
NAU8315B31VG	1.95mm x 1.18mm	WLCSP-12	Green
NAU83U15YG (Under Development)	4mm x 4mm	QFN-20	Green

NAU83_15 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-20

A31V = WLCSP-9

B31V = WLCSP-12

Package Grade:

Blank = Commercial & Industrial Grade

U = Automotive Grade AEC-Q100 qualification & TS16949 compliant

10 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Sep 23, 2019	Initial Release
1.1	Sep 23, 2019	Updated WLCSP 9 pinout and package drawing
1.2	Oct 25, 2019	Updated VIL & VIH conditions. Add WLCSP & QFN20 charts and WLCSP parameters
1.3	Jan 29, 200	Updated electrical characteristic section
1.4	Feb 18,2020	Updated Part number Added more information for I2S
1.5	Mar 30, 2020	Added Section 9.2
1.6	Jun 23, 2021	WLCSP 9 Ball C2 pin description Table 3, changed FSL to FSR
1.7	May 19, 2022	Updated Figure 16, Figure 17, Table 7
1.8	Feb 1, 2023	Updated Halogen-free, RoHS-compliant and TSCA-compliant description
1.9	Sep 10, 2024	Updated Format
2.0	Jan 15, 2025	Updated Digital Audio Interface (Add T_{DIS})
2.1	Jan 22, 2025	Updated Ordering Information
2.2	Mar 21, 2025	Updated Digital Audio Interface Timing Descriptions
2.3	Oct 17, 2025	Updated Digital Audio Interface Timing Parameter

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