NuMicro® Family

ARM926EJ-S™-based Microprocessor

N9H26 Series
Datasheet

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1 GENERAL DESCRIPTION

The N9H26 series is built on the ARM926EJ-S CPU core and integrated with USB2.0 HS Host/Device, NAND/eMMC/SD/SDIO/SPI host controller, video codec (H.264), JPEG codec, 32-channel SPU (Sound Processing Unit), ADC, DAC and AAC accelerator for saving the BOM cost in various kinds of application needs to be the best choice.

The N9H26 series can also be ported under Linux OS to leverage the driver availability of emerging functionalities such as Wi-Fi, etc., maximum resolutions for N9H26 is1024x768 @ TFT LCD panel. On the other hand, the open source code environment provides the product development more flexibility and Nuvoton's continuous optimizations in Linux provide customers with a cost-effective solution. Moreover, the 3rd parties USB and SDIO Wi-Fi modules are introduced to best utilize Wi-Fi streaming application.

To reduce system complexity while cutting the BOM cost, the N9H26 series provides MCP (Multi-Chip Package) to ensure higher performance and to minimize the system design efforts.Total BOM cost can be cut by employing 2-layer PCB along with the elimination of external parts, EMI prevention components and saving board space.

1.1 Applications

- HMI
- Home Appliance
- Advertisement

2 FEATURES

- **CPU**
  - ARM926EJ-S 32-bit RISC CPU up to 240MHz with 8KB I-Cache & 8KB D-Cache
  - JTAG interface supported for development and debugging

- **Internal SRAM & ROM**
  - 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory Card
      - SD card
      - SD-to-NAND flash bridge
    - NAND Interface
      - Raw NAND Flash
    - SPI Flash
    - USB Mass Storage

- **SDRAM MCP**
  - 32Mbx16 DDR2 MCP for N9H26K63N

- **EDMA (Enhanced DMA)**
  - Totally 11 DMA channels supported
    - 8 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - 3 dedicated channels for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format: RGB555, RGB565 and YCbCr422
    - Destination color format: RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- **JPEG Codec**
  - Baseline sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
  - Planar Format
  - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Support to decode YCbCr 4:2:2 transpose format
  - Support arbitrary width and height image encode and decode
  - Support three programmable quantization-tables
  - Support standard default Huffman-table and programmable Huffman-table for decode
  - Support arbitrarily 1X~8X image up-scaling function for encode mode
  - Support down-scaling function for encode and decode modes
  - Support specified window decode mode
  - Support quantization-table adjustment for bit-rate and quality control in encode mode
  - Support rotate function in encode mode
  - Packet Format
  - Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format

- Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
- Support decoded output image RGB555, RGB565 and RGB888 formats.
- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode

- **H.264 Codec**
  - Supports ITU-T Recommendation H.264|ISO/IEC 14496-10 Advance Video Coding(AVC) Standard (MPEG-4 part 10) baseline profile Level 3.1 standard
  - Supports up to the 720p @25fps video resolution
  - Supports YUV 4:2:0 video input format (MB base)
  - Hardware block-base rate-control (CBR/VBR)
  - Pure hardware engine

- **Video Data Processor(VPE)**
  - Video Data Processor
    - Image/Video data format conversion
      - Source
        - Planar: YUV/YCbCr 444/422/420
        - Packet: YUV 422
      - Destination
        - Packet: YUV 422, RGB 555/565/888
    - Image/video 2-D rotation and coordinate transforming
      - Left/Right with 90/180 degrees, mirror, up-side-down, and flip/flop.
    - Arbitrary scaling up/down with the bilinear filter
    - Supports MMU DMA

- **CRC Generator/Checking Hardware Engine**
  - CRC16: x^16+x^15+x^2+1 or x^16+x^15+x^5+1 (CRC-CCITT)
  - CRC32: x^32+x^26+x^23+x^22+x^16+x^12+x^11+x^10+x^8+x^7+x^5+x^4+x^2+x+1

- **VPOST**
  - 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
  - Color format supported:
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
  - SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
    - The maximum resolution is up to 1024x768 for TFT LCD panel
  - Display scaling to fit different size of LCD panels
    - Horizontal: At most 4.0x scale
    - Vertical: At most 3.0x scale
  - For SYNC type LCD:
    - For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported
      - CCIR656 interface supported
      - RGB Through mode supported
    - For 16/18/24-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock)

- Color format transform supported:
  - Color format transform between YCbCr422 and RGB565
  - Color format transform from YCbCr422 to RGB888
- Support OSD functions to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- **SPU (Sound Processing Unit)**
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels
  - 10-band equalizer supported
  - Special code supported for loop playing and event detection

- **AAC accelerator**
  - MDCT/IMDCT engine

- **I^2S Controller**
  - I^2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported

- **Storage Interface Controller**
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC24 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD

- **USB Device Controller**
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- **USB Host Controllers**
  - One USB 1.1 Host port (lite)
  - One USB 2.0 Host port
  - Over Current detection required
  - Fully compliant with USB Revision 1.1 and 2.0 specifications
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - High-speed (480Mbps), Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported
  - Control, Bulk, Interrupt and Isochronous transfers supported

- **Ethernet MAC Controller**
  - Supports IEEE Std. 802.3 CSMA/CD protocol.
  - Supports both half and full duplex for 10M/100M bps operation.
  - Supports RMII interface.
  - Supports MII Management function.
  - Supports pause and remote pause function for flow control.
  - Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception.

- Supports 16 entries CAM function for Ethernet MAC address recognition.
- Supports internal loop back mode for diagnostic.
- Supports 256 bytes embedded transmit and receive FIFO.
- Supports DMA function.

- **Timer & Watch-Dog Timer**
  - Four 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- **PWM**
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported

- **UART**
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 2 signals TX and RX supported only
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only
- **SPI**
  - Two SPI interfaces are supported
    - Both master and slave mode are supported in SPI interface 0 and 1
    - Byte transfer with configurable stop interval supported
  - Supports 1/2/4 bit SPI NOR Flash interface timing specification

- **I^2C**
  - One I^2C channel supported
  - Compatible with Philips's I^2C standard and only master mode supported
  - Multi-master operation supported

- **Advanced Interrupt Controller**
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Low priority interrupt automatic masking supported for interrupt nesting

- **Internal SRAM**
  - 8KB embedded SRAM
  - Co-work with Fast Booting (<3 seconds) for reducing system power consumption.

- **RTC**
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Build-in 32KHz RC oscillator
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported

- Alarm supported (second, minute, hour, day, month and year)
- 12/24-hour mode and Leap year supported
- Alarm to wake chip up from Standby mode or from Power-down mode supported
- Wake chip up from Power-down mode by input pin supported
- Power-off chip by register setting supported
- Power-on timeout is supported for low battery protection

- **GPIO**
  - 80 programmable general purpose I/Os supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- **Audio DAC**
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- **Audio ADC**
  - 16-bit Sigma-Delta ADC supported

- **General-Purpose ADC (SAR ADC)**
  - Multi-channel, 12-bit ADC supported
    - 4 channels dedicated for 4-wire resistive touch sensor inputs
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
    - 5-wire resistive touch sensor interface is also supported
    - Input voltage range from 0V ~ 3.3V supported
  - Maximum 16MHz input clock supported
  - Maximum 200K/s conversion rate supported
  - One high-speed channel for 1M SPS sampling rate
  - LVR (Low Voltage Reset) supported

- **Power Management**
  - Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
    - Normal Operating Mode
      - Core power is 1.2V and chip is in normal operation
    - CPU Standby Mode
      - Core power is 1.2V and only ARM CPU clock is turned OFF
    - Deep Standby Mode
      - Core power is 1.2V and all IP clocks are turned OFF
    - Power Down Mode
      - Only the RTC power is ON. Other 3.3V and 1.2V power are OFF

- **Operating Voltage**
  - I/O: 3.3V
  - Core: 1.2V
  - DDR2: 1.8V

- **Package**
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.
  - LQFP-128

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 N9H26 Series Part Number Naming Guide

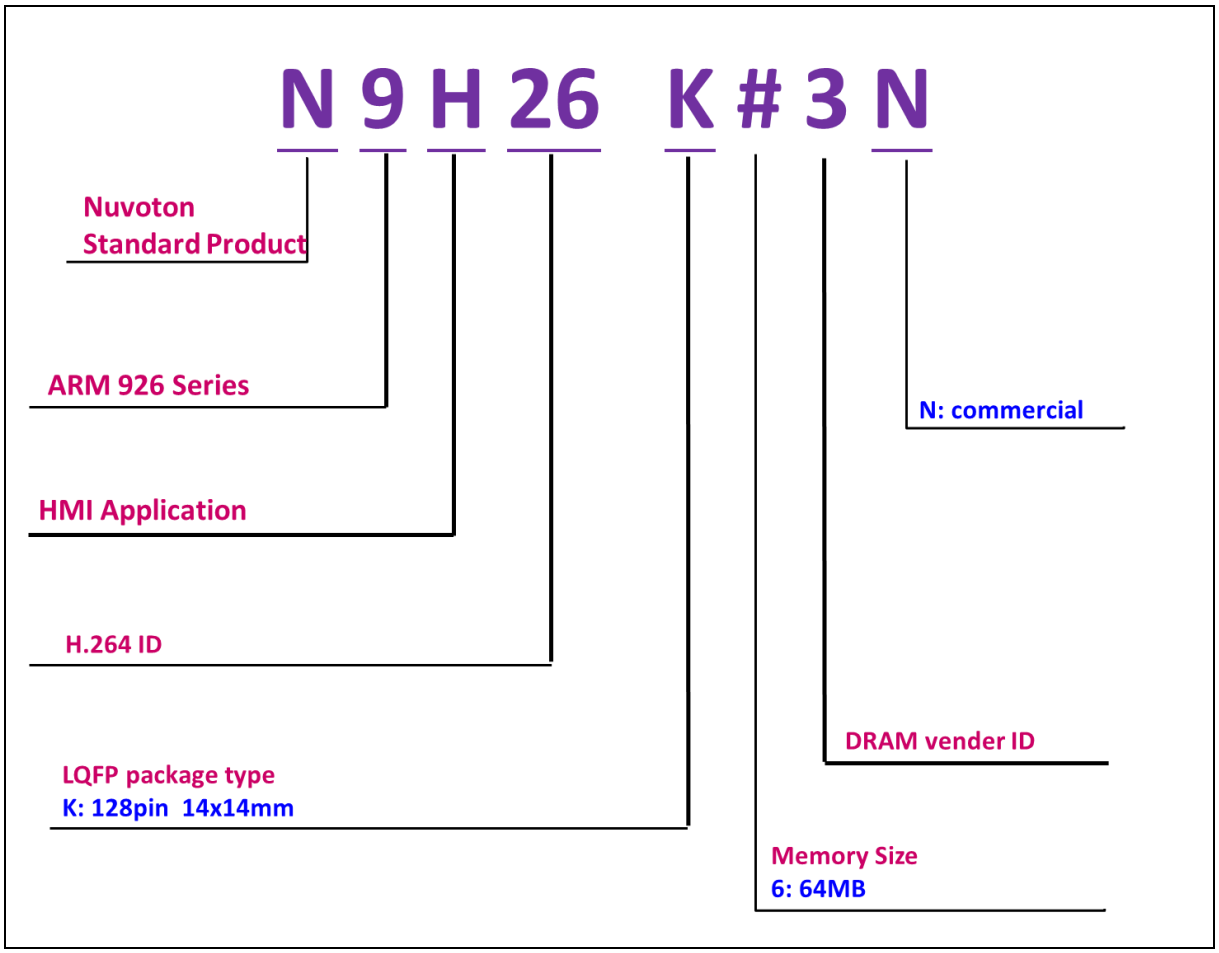


Figure 3.1-1 N9H26 Series Part Number Naming Guide

3.2 N9H26 Series Part Selection Guide

N9H26 Series																																				
Part No.	Core				Memory/Flash					MAC	USB			Accelerator			LCD		Analog					Peripheral								Power			Operating Temp.	PKG
Spec.	Max Speed(MHz)	ARM CPU	I cache(KB)	D cache(KB)	SRAM(KB)	Stacked DRAM	SPI NOR (1/4 bit) booting	NAND booting	eMMC/SD/SDIO booting	Ethernet 10/100 MAC	FS 1.1 Host(12Mbps)	HS 2.0 Host(480Mbps)	HS 2.0 Device(480Mbps) booting	2D BitBLT GFX	JPEG Codec	H.264 Video codec	RGB color (bits)	Max. Resolution[1]	12-bit SAR ADC	Audio 16-bit ΣΔ ADC MIC	Digital MIC I/F	4/5-wire TP ADC	Audio 16-bit stereo DAC	JTAG	GPIO(Max)	UART	I^2C	SPI	RTC	PWM	I^2S	Core Voltage (V)	DRAM Voltage (V)	I/O Voltage (V)	°C	Type
N9H26K63N	240	926	8	8	8	64MB	√	√	3	2	1	1	1	√	√	√	24	XGA	√	√	√	√	√	√	80	2	1	2	√	4	√	1.2	1.8	3.3	-20~ +85	LQFP 128

* Resolution: XGA(1024x768).

3.3 Pin Configuration

3.3.1 N9H26 Series Pin Diagram

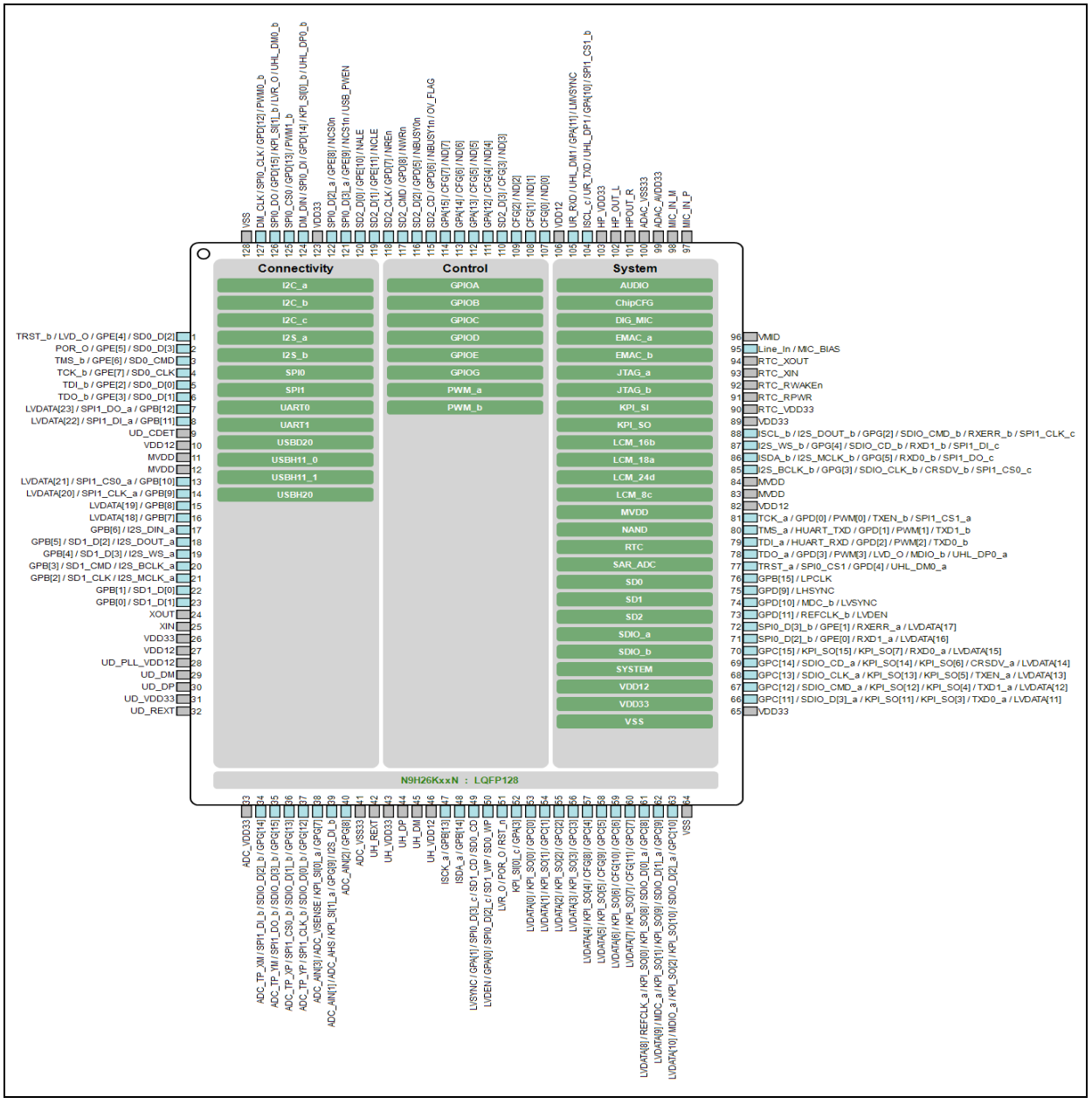


Figure 3.3-1 N9H26KxxN LQFP 128 Pin Diagram

3.4 Pin Description

Pin No	Name	Type	Group	Description
1	SD0_D[2]	I/O	SD0	SD Interface Port 0 Data Bit 2.
	TRST_b	O	JTAG	Alternative JTAG Interface Test Reset, low active.
	GPE[4]	I/O	GPIOE	GPIO Port E Bit 4.
	LVD_O	O	SYSTEM	Low Voltage Detect Indicator, low active.
2	SD0_D[3]	I/O	SD0	SD Interface Port 0 Data Bit 3.
	GPE[5]	I/O	GPIOE	GPIO Port E Bit 5.
	POR_O	O	SYSTEM	Power On Reset, low active.
3	SD0_CMD	I/O	SD0	SD Interface Port 0 Command.
	TMS_b	O	JTAG	Alternative JTAG Interface Test Mode Select.
	GPE[6]	I/O	GPIOE	GPIO Port E Bit 6.
4	SD0_CLK	I/O	SD0	SD Interface Port 0 Clock.
	TCK_b	O	JTAG	Alternative JTAG Interface Test Clock.
	GPE[7]	I/O	GPIOE	GPIO Port E Bit 7.
5	SD0_D[0]	I/O	SD0	SD Interface Port 0 Data Bit 0.
	TDI_b	I	JTAG	Alternative JTAG Interface Test Data In.
	GPE[2]	I/O	GPIOE	GPIO Port E Bit 2.
6	SD0_D[1]	I/O	SD0	SD Interface Port 0 Data Bit 1.
	TDO_b	O	JTAG	Alternative JTAG Interface Test Data Out.
	GPE[3]	I/O	GPIOE	GPIO Port E Bit 3.
7	SPI1_DO_a	O	SPI1	Alternative SPI Interface Port 1 Data Out.
	LVDATA[23]	O	LCM	LCD Interface Data Bit 23.
	GPB[12]	I/O	GPIOB	GPIO Port B Bit 12.
8	SPI1_DI_a	I	SPI1	Alternative SPI Interface Port 1 Data In.
	LVDATA[22]	O	LCM	LCD Interface Data Bit 22.
	GPB[11]	I/O	GPIOB	GPIO Port B Bit 11.
9	UD_CDET	I	USBD20	USB Device Connect Detect, high active.
10	VDD12	P	VDD12	Core Logic Power.
11	MVDD	P	MVDD	SDRAM I/F Power.
12	MVDD	P	MVDD	SDRAM I/F Power.
13	SPI1_CS0_a	O	SPI1	Alternative SPI Interface Port 1 Device Select 0, low active.

	LVDATA[21]	O	LCM	LCD Interface Data Bit 21.
	GPB[10]	I/O	GPIOB	GPIO Port B Bit 10.
14	SPI1_CLK_a	O	SPI1	Alternative SPI Interface Port 1 Clock.
	LVDATA[20]	O	LCM	LCD Interface Data Bit 20.
	GPB[9]	I/O	GPIOB	GPIO Port B Bit 9.
15	LVDATA[19]	O	LCM	LCD Interface Data Bit 19.
	GPB[8]	I/O	GPIOB	GPIO Port B Bit 8.
16	LVDATA[18]	O	LCM	LCD Interface Data Bit 18.
	GPB[7]	I/O	GPIOB	GPIO Port B Bit 7.
17	I2S_DIN_a	I	I2S	Alternative I^2S Interface Data Input.
	GPB[6]	I/O	GPIOB	GPIO Port B Bit 6.
18	I2S_DOUT_a	O	I2S	Alternative I^2S Interface Data Output.
	SD1_D[2]	I/O	SD1	SD Interface Port 1 Data Bit 2.
	GPB[5]	I/O	GPIOB	GPIO Port B Bit 5.
19	I2S_WS_a	O	I2S	Alternative I^2S Interface Left/Right Channel Clock.
	SD1_D[3]	I/O	SD1	SD Interface Port 1 Data Bit 3.
	GPB[4]	I/O	GPIOB	GPIO Port B Bit 4.
20	I2S_BCLK_a	O	I2S	Alternative I^2S Interface Bit Clock.
	SD1_CMD	I/O	SD1	SD Interface Port 1 Command.
	GPB[3]	I/O	GPIOB	GPIO Port B Bit 3.
21	I2S_MCLK_a	O	I2S	Alternative I^2S Interface Master Clock.
	SD1_CLK	I/O	SD1	SD Interface Port 1 Clock.
	GPB[2]	I/O	GPIOB	GPIO Port B Bit 2.
22	SD1_D[0]	I/O	SD1	SD Interface Port 1 Data Bit 0.
	GPB[1]	I/O	GPIOB	GPIO Port B Bit 1.
23	SD1_D[1]	I/O	SD1	SD Interface Port 1 Data Bit 1.
	GPB[0]	I/O	GPIOB	GPIO Port B Bit 0.
24	XOUT	O	SYSTEM	12MHz Crystal Output.
25	XIN	I	SYSTEM	12MHz Crystal In.
26	VDD33	P	VDD33	I/O Power.
27	VDD12	P	VDD12	Core Logic Power.
28	UD_PLL_VDD12	P	SYSTEM	PLL and USB Core Power.

29	UD_DM	I/O	USBD20	USB 2.0 Device D-.
30	UD_DP	I/O	USBD20	USB 2.0 Device D+.
31	UD_VDD33	P	USBD20	USB 2.0 PHY Power.
32	UD_REXT	I	USBD20	External Resister 12.1K Resistor Connected to Ground.
33	ADC_VDD33	AP	SAR_ADC	SAR-ADC Power.
34	ADC_TP_XM	AI	SAR_ADC	Touch Panel XM.
	SPI1_DI_b	I	SPI1	Alternative SPI Interface Port 1 Data In.
	SDIO_D[2]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 2.
	GPG[14]	I/O	GPIOG	GPIO Port G Bit 14.
35	ADC_TP_YM	AI	SAR_ADC	Touch Panel YM.
	SPI1_DO_b	O	SPI1	Alternative SPI Interface Port 1 Data Out.
	SDIO_D[3]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 3.
	GPG[15]	I/O	GPIOG	GPIO Port G Bit 15.
36	ADC_TP_XP	AI	SAR_ADC	Touch Panel XP.
	SPI1_CS0_b	O	SPI1	Alternative SPI Interface Port 1 Device Select 0, low active.
	SDIO_D[1]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 1.
	GPG[13]	I/O	GPIOG	GPIO Port G Bit 13.
37	ADC_TP_YP	AI	SAR_ADC	Touch Panel YP.
	SPI1_CLK_b	O	SPI1	Alternative SPI Interface Port 1 Clock.
	SDIO_D[0]_b	I/O	SDIO	Alternative SDIO Interface Data Bit 0.
	GPG[12]	I/O	GPIOG	GPIO Port G Bit 12.
38	ADC_VSENSE	AI	SAR_ADC	5W Touch Panel Input Detection.
	ADC_AIN[3]	AI	SAR_ADC	ADC Analog Input Channel 3.
	KPI_SI[0]_a	I	KPI_SI	Alternative KPI Scan In Bit 0.
	GPG[7]	I/O	GPIOG	GPIO Port G Bit 7.
39	ADC_AHS	AI	SAR_ADC	ADC Analog High Speed Input Channel.
	ADC_AIN[1]	AI	SAR_ADC	ADC Analog Input Channel 1.
	I2S_DI_b	I	I2S	Alternative I^2S Interface Data Input.
	KPI_SI[1]_a	I	KPI_SI	Alternative KPI Scan In Bit 1.
	GPG[9]	I/O	GPIOG	GPIO Port G Bit 9.
40	ADC_AIN[2]	AI	SAR_ADC	ADC Analog Input Channel 2.
	GPG[8]	I/O	GPIOG	GPIO Port G Bit 8.

41	ADC_VSS33	AP	SAR_ADC	SAR-ADC Ground.
42	UH_REXT	I	USBH20	External Resistor12.1K Resistor connected to Ground For USB 2.0 Host PHY.
43	UH_VDD33	AP	USBH20	USB 2.0 Host PHY Power.
44	UH_DP	I/O	USBH20	USB 2.0 Host D+.
45	UH_DM	I/O	USBH20	USB 2.0 Host D-.
46	UH_VDD12	AP	USBH20	USB 2.0 Host Core Logic Power.
47	ISCK_a	O	I2C	Alternative I^2C Interface Clock.
	GPB[13]	I/O	GPIOB	GPIO Port B Bit 13.
48	ISDA_a	I/O	I2C	Alternative I^2C Interface Data.
	GPB[14]	I/O	GPIOB	GPIO Port B Bit 14.
49	SPI0_D[3]_c	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	LVSYNC	O	LCM	LCD Interface Vertical Sync, high active.
	SD0_CD_	I	SD0	SD Interface Card 0 Insert Detect, low active.
	GPA[1]	I/O	GPIOA	GPIO Port A Bit 1.
	SD1_CD_	I	SD1	SD Interface Crad 1 Insert Detect, low active.
50	SPI0_D[2]_c	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	LVDEN	O	LCM	LCD Interface Data Enable, high active.
	SD0_WP_	I	SD0	SD Interface 0 Write Protect Indicator, low active.
	GPA[0]	I/O	GPIOA	GPIO Port A Bit 0.
	SD1_WP_	I/O	SD1	SD Interface 1 Write Protect Indicator, low active.
51	RST_	I	SYSTEM	System Reset, low active.
	POR_O	O	SYSTEM	Power On Reset, low active.
	LVR_O	O	SYSTEM	Low Voltage Reset Indicator, low active.
52	KPI_SI[0]_c	I	KPI_SI	Alternative KPI Scan In Bit 0.
	GPA[3]	I/O	GPIOA	GPIO Port A Bit 3.
53	LVDATA[0]	O	LCM	LCD Interface Data Bit 0.
	GPC[0]	I/O	GPIOC	GPIO Port C Bit 0.
	KPI_SO[0]	O	KPI_SO	KPI Scan Out Bit 0.
54	LVDATA[1]	O	LCM	LCD Interface Data Bit 1.
	GPC[1]	I/O	GPIOC	GPIO Port C Bit 1.
	KPI_SO[1]	O	KPI_SO	KPI Scan Out Bit 1.

55	LVDATA[2]	O	LCM	LCD Interface Data Bit 2.
	GPC[2]	I/O	GPIOC	GPIO Port C Bit 2.
	KPI_SO[2]	O	KPI_SO	KPI Scan Out Bit 2.
56	LVDATA[3]	O	LCM	LCD Interface Data Bit 3.
	GPC[3]	I/O	GPIOC	GPIO Port C Bit 3.
	KPI_SO[3]	O	KPI_SO	KPI Scan Out Bit 3.
57	LVDATA[4]	O	LCM	LCD Interface Data Bit 4.
	GPC[4]	I/O	GPIOC	GPIO Port C Bit 4.
	CHIPCFG[8]	I	ChipCFG	Chip Power On Configuration Data Bit 8.
	KPI_SO[4]	O	KPI_SO	KPI Scan Out Bit 4.
58	LVDATA[5]	O	LCM	LCD Interface Data Bit 5.
	GPC[5]	I/O	GPIOC	GPIO Port C Bit 5.
	CHIPCFG[9]	I	ChipCFG	Chip Power On Configuration Data Bit 9.
	KPI_SO[5]	O	KPI_SO	KPI Scan Out Bit 5.
59	LVDATA[6]	O	LCM	LCD Interface Data Bit 6.
	GPC[6]	I/O	GPIOC	GPIO Port C Bit 6.
	CHIPCFG[10]	I	ChipCFG	Chip Power On Configuration Data Bit 10.
	KPI_SO[6]	O	KPI_SO	KPI Scan Out Bit 6.
60	LVDATA[7]	O	LCM	LCD Interface Data Bit 7.
	GPC[7]	I/O	GPIOC	GPIO Port C Bit 7.
	CHIPCFG[11]	I	ChipCFG	Chip Power On Configuration Data Bit 11.
	KPI_SO[7]	O	KPI_SO	KPI Scan Out Bit 7.
61	LVDATA[8]	O	LCM	LCD Interface Data Bit 8.
	SDIO_D[0]_a	I/O	SDIO	Alternative SDIO Interface Data Bit 0.
	REFCLK_a	I	EMAC	Alternative LAN RMII Interface, REFCLK input.
	GPC[8]	I/O	GPIOC	GPIO Port C Bit 8.
	KPI_SO[8]	O	KPI_SO	KPI Scan Out Bit 8.
	KPI_SO[0]	O	KPI_SO	KPI Scan Out Bit 0.
62	LVDATA[9]	O	LCM	LCD Interface Data Bit 9.
	SDIO_D[1]_a	I/O	SDIO	Alternative SDIO Interface Data Bit 1.
	MDC_a	O	EMAC	Alternative LAN RMII Interface, MDC.
	GPC[9]	I/O	GPIOC	GPIO Port C Bit 9.

	KPI_SO[9]	O	KPI_SO	KPI Scan Out Bit 9.
	KPI_SO[1]	O	KPI_SO	KPI Scan Out Bit 1.
63	LVDATA[10]	O	LCM	LCD Interface Data Bit 10.
	SDIO_D[2]_a	I/O	SDIO	Alternative SDIO Interface Data Bit 2.
	MDIO_a	I/O	EMAC	Alternative LAN RMII Interface, MDIO.
	GPC[10]	I/O	GPIOC	GPIO Port C Bit 10.
	KPI_SO[10]	O	KPI_SO	KPI Scan Out Bit 10.
	KPI_SO[2]	O	KPI_SO	KPI Scan Out Bit 2.
64	VSS	P	VSS	Ground
65	VDD33	P	VDD33	I/O Power.
66	LVDATA[11]	O	LCM	LCD Interface Data Bit 11.
	SDIO_D[3]_a	I/O	SDIO	Alternative SDIO Interface Data Bit 3.
	TXD0_a	O	EMAC	Alternative LAN RMII Interface TXD0.
	GPC[11]	I/O	GPIOC	GPIO Port C Bit 11.
	KPI_SO[11]	O	KPI_SO	KPI Scan Out Bit 11.
	KPI_SO[3]	O	KPI_SO	KPI Scan Out Bit 3.
67	LVDATA[12]	O	LCM	LCD Interface Data Bit 12.
	SDIO_CMD_a	I/O	SDIO	Alternative SDIO Interface Command.
	TXD1_a	I/O	EMAC	Alternative LAN RMII Interface TXD1.
	GPC[12]	I/O	GPIOC	GPIO Port C Bit 12.
	KPI_SO[12]	O	KPI_SO	KPI Scan Out Bit 12.
	KPI_SO[4]	O	KPI_SO	KPI Scan Out Bit 4.
68	LVDATA[13]	O	LCM	LCD Interface Data Bit 13.
	SDIO_CLK_a	O	SDIO	Alternative SDIO Interface Clock.
	TXEN_a	O	EMAC	Alternative LAN RMII Interface, TXEN.
	GPC[13]	I/O	GPIOC	GPIO Port C Bit 13.
	KPI_SO[13]	O	KPI_SO	KPI Scan Out Bit 13.
	KPI_SO[5]	O	KPI_SO	KPI Scan Out Bit 5.
69	LVDATA[14]	O	LCM	LCD Interface Data Bit 14.
	SDIO_CD_a	I	SDIO	Alternative SDIO Interface Card Detect Indicator, low active.
	CRSDV_a	I/O	EMAC	Alternative LAN RMII Interface, carrier sense / receive data valid

	GPC[14]	I/O	GPIOC	GPIO Port C Bit 14.
	KPI_SO[14]	O	KPI_SO	KPI Scan Out Bit 14.
	KPI_SO[6]	O	KPI_SO	KPI Scan Out Bit 6.
70	LVDATA[15]	O	LCM	LCD Interface Data Bit 15.
	RXD0_a	I	EMAC	Alternative LAN RMII Interface, RXD0.
	GPC[15]	I/O	GPIOC	GPIO Port C Bit 15.
	KPI_SO[15]	O	KPI_SO	KPI Scan Out Bit 15.
	KPI_SO[7]	O	KPI_SO	KPI Scan Out Bit 7.
71	LVDATA[16]	O	LCM	LCD Interface Data Bit 16.
	SPI0_D[2]_b	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	RXD1_a	I	EMAC	Alternative LAN RMII Interface, RXD1.
	GPE[0]	I/O	GPIOE	GPIO Port E Bit 0.
72	LVDATA[17]	O	LCM	LCD Interface Data Bit 17.
	SPI0_D[3]_b	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	RXERR_a	I	EMAC	Alternative LAN RMII Interface, RXERR.
	GPE[1]	I/O	GPIOE	GPIO Port E Bit 1.
73	LVDEN	O	LCM	LCD Interface Data Enable, high active.
	REFCLK_b	I	EMAC	Alternative LAN RMII Interface, REFCLK.
	GPD[11]	I/O	GPIOD	GPIO Port D Bit 11.
74	LVSYNC	O	LCM	LCD Interface Vertical Sync., high active.
	MDC_b	O	EMAC	Alternative LAN RMII Interface, MDC.
	GPD[10]	I/O	GPIOD	GPIO Port D Bit 10.
75	LHSYNC	O	LCM	LCD Interface Horizontal Sync, high active.
	GPD[9]	I/O	GPIOD	GPIO Port D Bit 9.
76	LPCLK	O	LCM	LCD Interface Pixel Clock.
	GPB[15]	I/O	GPIOB	GPIO Port B Bit 15.
77	TRST_a	O	JTAG	Alternative JTAG Interface Test Reset, low active.
	SPI0_CS1_	O	SPI0	SPI Interface Port 0 Device Select 1.
	UHL0_DM_a	I/O	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D-.
	GPD[4]	I/O	GPIOD	GPIO Port D Bit 4.
78	TDO_a	O	JTAG	Alternative JTAG Interface Test Data Out.
	PWM3	O	PWM	PWM Output Channel 3.

	UHL0_DP_a	I/O	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D+.
	LVD_O	O	SYSTEM	Low Voltage Detect Output, low active.
	MDIO_b	I/O	EMAC	Alternative LAN RMII Interface, MDIO.
	GPD3	I/O	GPIOD	GPIO Port D Bit 3.
79	TDI_a	I	JTAG	Alternative JTAG Interface Test Data In.
	HUR_RXD	I	HUART	High Speed UART RX Data.
	PWM2	O	PWM	PWM Output Channel 2.
	TXD0_b	O	EMAC	Alternative LAN RMII Interface, TXD0.
	GPD[2]	I/O	GPIOD	GPIO Port D Bit 2.
80	TMS_a	O	JTAG	Alternative JTAG Interface Test Mode Select.
	HUR_TXD	O	HUART	High Speed UART TX Data.
	PWM1_a	O	PWM	Alternative PWM Output Channel 1.
	TXD1_b	O	EMAC	Alternative LAN RMII Interface, TXD1.
	GPD[1]	I/O	GPIOD	GPIO Port D Bit 1.
81	TCK_a	O	JTAG	Alternative JTAG Interface Test Clock.
	SPI1_CS1_a	O	SPI1	Alternative SPI Interface Port 1 Device Select 1, low active.
	PWM0_a	O	PWM	Alternative PWM Output Channel 0.
	TXEN_b	O	EMAC	Alternative LAN RMII Interface, TXEN.
	GPD[0]	I/O	GPIOD	GPIO Port D Bit 0.
82	VDD12	P	VDD12	Core Logic Power.
83	MVDD	P	MVDD	SDRAM I/F Power.
84	MVDD	P	MVDD	SDRAM I/F Power.
85	I2S_BCLK_b	O	I2S	Alternative I^2S Interface Bit Clock.
	SPI1_CS0_c	O	SPI1	Alternative SPI Interface Port 1 Device Select 0, low active.
	SDIO_CLK_b	O	SDIO	Alternative SDIO Interface Clock.
	CRSDV_b	I	EMAC	Alternative LAN RMII Interface, carrier sense / receive data valid.
	GPG[3]	I/O	GPIOG	GPIO Port G Bit 3.
86	I2S_MCLK_b	O	I2S	Alternative I^2S Interface Master Clock.
	ISDA_b	I/O	I2C	Alternative I^2C Interface Data.
	SPI1_DO_c	O	SPI1	Alternative SPI Interface Port 1 Data Out.
	RXD0_b	I	EMAC	Alternative LAN RMII Interface, RXD0.

	GPG[5]	I/O	GPIOG	GPIO Port G Bit 5.
87	I2S_WS_b	O	I2S	Alternative I²S Interface Left/Right Channel Clock.
	SPI1_DI_c	I	SPI1	Alternative SPI Interface Port 1 Data In.
	SDIO_CD_b	I	SDIO	Alternative SDIO Interface Card Detect Indicator, low active.
	RXD1_b	I	EMAC	Alternative LAN RMII Interface, RXD1.
	GPG[4]	I/O	GPIOG	GPIO Port G Bit 4.
88	I2S_DOUT_b	O	I2S	Alternative I²S Interface Data Output.
	ISCK_b	O	I2C	Alternative I²C Interface Clock.
	SPI1_CLK_c	O	SPI1	Alternative SPI Interface Port 1 Clock.
	SDIO_CMD_b	I/O	SDIO	Alternative SDIO Interface Command.
	RXERR_b	I	EMAC	Alternative LAN RMII Interface, RXERR.
	GPG[2]	I/O	GPIOG	GPIO Port G Bit 2.
89	VDD33	P	VDD33	I/O Power.
90	RTC_VDD	P	RTC	RTC Power.(3.3V)
91	RTC_RPWR	O	RTC	Power Enable, high active.
92	RTC_RWAKE_	I	RTC	Wakeup Enable, low active.
93	RTC_XIN	I	RTC	32.768KHZ Crystal Input.
94	RTC_XOUT	O	RTC	32.768KHZ Crystal Output.
95	MIC_BIAS	AP	AUDIO	Microphone Bias Power Supply output. (MIC_BIAS=0.75 * ADAC_AVDD33)
	Line_In	AI	AUDIO	Analog Audio Input.
96	VMID	I	AUDIO	Mid-Rail Reference, connect 1uF to ADAC_VSS33. (1/2 * ADAC_VDD33).
97	MIC_IN_P	AI	AUDIO	Microphone Positive Input.
98	MIC_IN_M	AI	AUDIO	Microphone Negative Input.
99	ADAC_AVDD33	AP	AUDIO	Audio DAC Analog Power.
100	ADAC_HPVSS33	AP	AUDIO	Audio DAC and Headphone Analog Ground.
101	ADAC_HPOUT_R	O	AUDIO	Headphone Right Output Channel.
102	ADAC_HPOUT_L	O	AUDIO	Headphone Left Output Channel.
103	ADAC_HPVDD33	AP	AUDIO	Headphone Analog Power.
104	UR_TXD	O	UART	UART TX Data.
	UHL1_DP	I/O	USBH11_1	USB 1.1 Host Lite Port 1 D+.
	ISCK_c	O	I2C	Alternative I²C Interface Clock.

	SPI1_CS1_b	O	SPI1	Alternative SPI Interface Port 1 Device Select 1, low active.
	GPA[10]	I/O	GPIOA	GPIO Port A Bit 10.
105	UR_RXD	I	UART	UART RX Data.
	UHL1_DM	I/O	USBH11_1	USB 1.1 Host Lite Port 1 D-.
	ISDA_c	I/O	I2C	Alternative I^2C Interface Data.
	LMVSYNC	I/O	LCM	LCD Interface MPU Mode Vertical Sync., high active.
	GPA[11]	I/O	GPIOA	GPIO Port A Bit 11.
106	VDD12	P	VDD12	Core Logic Power.
107	ND[0]	I/O	NAND	NAND Interface Data Bit 0.
	CHIPCFG[0]	I	ChipCFG	Chip Power On Configuration Data Bit 0.
108	ND[1]	I/O	NAND	NAND Interface Data Bit 1.
	CHIPCFG[1]	I	ChipCFG	Chip Power On Configuration Data Bit 1.
109	ND[2]	I/O	NAND	NAND Interface Data Bit 2.
	CHIPCFG[2]	I	ChipCFG	Chip Power On Configuration Data Bit 2.
110	ND[3]	I/O	NAND	NAND Interface Data Bit 3.
	SD2_D[3]	I/O	SD2	SD Interface Port 2 Data Bit 3.
	CHIPCFG[3]	I	ChipCFG	Chip Power On Configuration Data Bit 3.
111	ND[4]	I/O	NAND	NAND Interface Data Bit 4.
	GPA[12]	I/O	GPIOA	GPIO Port A Bit 12.
	CHIPCFG[4]	I	ChipCFG	Chip Power On Configuration Data Bit 4.
112	ND[5]	I/O	NAND	NAND Interface Data Bit 5.
	GPA[13]	I/O	GPIOA	GPIO Port A Bit 13.
	CHIPCFG[5]	I	ChipCFG	Chip Power On Configuration Data Bit 5.
113	ND[6]	I/O	NAND	NAND Interface Data Bit 6.
	GPA[14]	I/O	GPIOA	GPIO Port A Bit 14.
	CHIPCFG[6]	I	ChipCFG	Chip Power On Configuration Data Bit 6.
114	ND[7]	I/O	NAND	NAND Interface Data Bit 7.
	GPA[15]	I/O	GPIOA	GPIO Port A Bit 15.
	CHIPCFG[7]	I	ChipCFG	Chip Power On Configuration Data Bit 7.
115	NBUSY1_	I	NAND	NAND Interface Busy Indicator 1, low active.
	SD2_CD_	I	SD2	SD Interface Port 2, Card Insert Detect, low active.
	OV_FLAG	I	USBH20	USB HOS Power Over Current Occurrence Flag.

	GPD[6]	I/O	GPIOD	GPIO Port D Bit 6.
116	NBUSY0_	I	NAND	NAND Interface Busy Indicator 0, low active.
	SD2_D[2]	I/O	SD2	SD Interface Port 2 Data Bit 2.
	GPD[5]	I/O	GPIOD	GPIO Port D Bit 5.
117	NWR_	O	NAND	NAND Interface Write Enable, low active.
	SD2_CMD	I/O	SD2	SD Interface Port 2 Command.
	GPD[8]	I/O	GPIOD	GPIO Port D Bit 8.
118	NRE_	O	NAND	NAND Interface Read Enable, low active
	SD2_CLK	O	SD2	SD Interface Port 2 Clock.
	GPD[7]	I/O	GPIOD	GPIO Port D Bit 7.
119	NCLE	O	NAND	NAND Interface Command Latch Enable, low active
	SD2_D[1]	I/O	SD2	SD Interface Port 2 Data Bit 1.
	GPE[11]	I/O	GPIOE	GPIO Port E Bit 11.
120	NALE	O	NAND	NAND Interface Address Latch Enable, low active
	SD2_D[0]	I/O	SD2	SD Interface Port 2 Data Bit 0.
	GPE[10]	I/O	GPIOE	GPIO Port E Bit 10.
121	NCS1_	O	NAND	NAND Interface Device Select 1, low active.
	SPI0_D[3]_a	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 3.
	USB_PWEN	O	USBH20	USB HOST Power Output Control.
	GPE[9]	I/O	GPIOE	GPIO Port E Bit 9.
122	NCS0_	O	NAND	NAND Interface Device Select 0, low active
	SPI0_D[2]_a	I/O	SPI0	Alternative SPI Interface Port 0 Data Bit 2.
	GPE[8]	I/O	GPIOE	GPIO Port E Bit 8.
123	VDD33	P	VDD33	I/O Power.
124	SPI0_DI	I	SPI0	SPI Interface Port 0 Data In.
	UHL0_DP_b	I/O	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D+.
	KPI_SI[0]_b	I	KPI_SI	Alternative KPI Scan In Bit 0.
	DM_DIN	I	DIG_MIC	Digital Microphone Data Input.
	GPD[14]	I/O	GPIOD	GPIO Port D Bit 14.
125	SPI0_CS0_	O	SPI0	SPI Interface Port 0 Device Select 0.
	PWM1_b	O	PWM	Alternative PWM Output Channel 1.
	GPD[13]	I/O	GPIOD	GPIO Port D Bit 13.

126	SPI0_DO	O	SPI0	SPI Interface Port 0 Data Out.
	UHL0_DM_b	I/O	USBH11_0	Alternative USB 1.1 Host Lite Port 0 D-.
	KPI_SI[1]_b	I	KPI_SI	Alternative KPI Scan In Bit 1.
	LVR_O	O	SYSTEM	Low Voltage Reset Indicator, low active.
	GPD[15]	I/O	GPIOD	GPIO Port D Bit 15.
127	SPI0_CLK	O	SPI0	SPI Interface Port 0 Clock.
	PWM0_b	O	PWM	Alternative PWM Output Channel 0.
	DM_CLK	O	DIG_MIC	Digital Microphone Clock.
	GPD[12]	I/O	GPIOD	GPIO Port D Bit 12.
128	VSS	P	VSS	Ground

Note:

TYPE	DESCRIPTION
I	Input
O	Output
I/O	Input / Output
P	Digital Power or Digital GND
AP	Analog Power or Analog GND
AI	Analog Input

4 BLOCK DIAGRAM

4.1 N9H26 Series Block Diagram

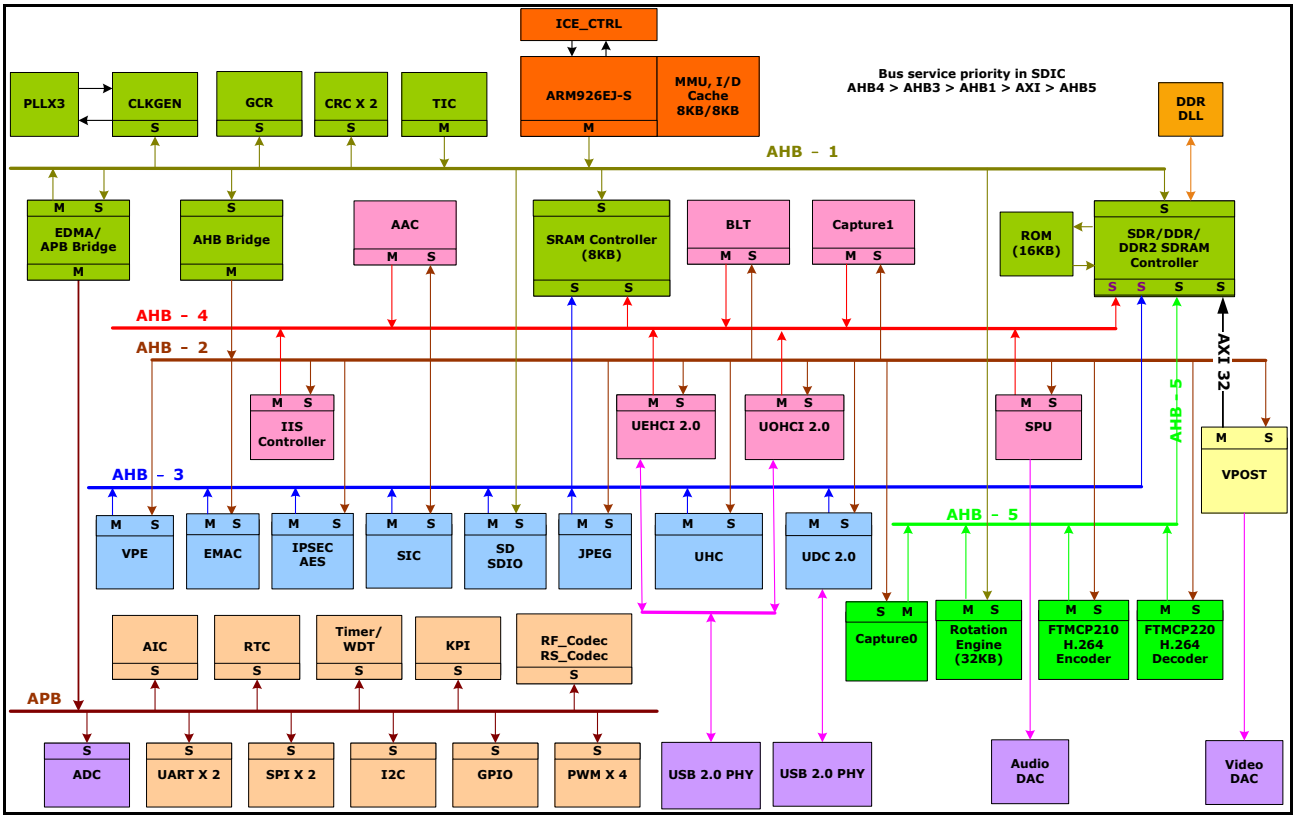


Figure 4.1-1 N9H26 Series Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 ARM926EJ-S CPU Core

The ARM926EJ-S CPU core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S CPU core is targeted at multi-tasking applications where full memory management, high performance, low die size, and low power are all important. The ARM926EJ-S CPU core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to trade off between high performance and high code density. The ARM926EJ-S CPU core includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead. The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core
- A Memory Management Unit (MMU)
- Separate instruction and data AMBA AHB bus interfaces

5.2 System Manager

5.2.1 Overview

The following functions are included in System Manager section: The system management describes following information and functions.

- System Memory Map
- Power-On Setting
- Bus Arbitration Mode
- Power Management
- IBR (Internal Boot ROM) Sequence
- System management registers for product ID, functional reset and multi-function pin control.

5.3 Clock Controller (CLK_CTL)

5.3.1 Overview

The clock controller generates the clocks for the whole chip, it include all of IPs on AHB, APB and engine clock like USB, UART and so on. There are three PLLs in this chip, and the PLL clock source is from the external crystal input. It also implements the power control function, include the individually clock on or off control register, clock source selector and divider. These functions minimize the extra power consumption and the chip run on the only just condition. On the power down mode the controller turn off the crystal oscillator to minimize the chip power consumption.

5.4 SDRAM Interface Controller (SDIC)

5.4.1 Overview

The SDRAM Controller support Low-Power DDR and DDR2 type SDRAM. The memory device size type can be from 64M bit and up to 512M bits. Only 16-bit data bus width is supported. The total system memory size can be from 8M-byte and up to 64M-byte for different SDRAM configuration.

5.5 2D Blitting Accelerator

5.5.1 Overview

The 2D blitting accelerator features are built on top of the FlashLite Bitmap rendering feature. It improves rendering performance of bitmap objects (source image) onto the frame buffer (destination image).

5.6 VPE Video Data Processing Engine

5.6.1 Overview

Video Data Processing Engine (VPE) contains the acceleration engines for still images and video movies.

The first function is for the image/video data format conversion and the second function is for the image/video 2D rotation or the coordinate transformation.

5.7 JPEG Codec

5.7.1 Overview

The JPEG Codec supports Baseline Sequential Mode JPEG still image compression and decompression that is fully compliant with ISO/IEC International Standard 10918-1 (T.81).

5.8 H.264 Video Codec

5.8.1 H.264 DECODER Overview

H.264 DEC is a video decoder, which supports the H.264 standard baseline profile. H.264 DEC is compliant with the ITU-T Recommendation H.264|ISO/IEC 14496-10 Advanced Video Coding Standard (MPEG 4 Part 10). This decoder is capable of decoding the video streams with a resolution of up to 720 x 480 at a frame rate of up to 60 frames per second or decoding the video streams with a resolution of up to 2048 x 1024 at a frame rate of up to 10 frames per second.

5.9 CAPTURE Engine

5.9.1 Overview

CAPTURE engine is designed to capture image data from sensor or TV decoder. After capturing or fetching image data, capture engine processes the image data, and then FIFO output them into frame buffer.

5.10 LCD Display Interface Controller (VPOST)

5.10.1 Overview

The main purpose of Display Controller is used to display the video/image data to LCD device or connect with external TV-encoder. The video/image data source may come from the H.264 video codec, JPEG decoder and the OSD pattern which have been stored in system memory (SDRAM). The input data format of the display controller can be packet YUV422, packet YUV444, packet RGB444, packet RGB565, packet RGB666, and packet RGB888. The OSD (On Screen Display) function supports packet YUV422 and 8/16/24-bit direct-color mode. The LCD controller supports both sync-type and MPU-type LCDM. This LCD Controller is a bus master and can transfer display data from system memory (SDRAM) without CPU intervention.

5.11 Sound Processing Unit (SPU)

5.11.1 Overview

The SPU performs 32 channels audio input and 16-bit stereo output to DAC and I^2S. SPU support 3 data-types (E-MDPCM (4bit), PCM16, LP8) with event and raw PCM16 mono/stereo and Tone.

5.12 I^2S Controller (I^2S)

5.12.1 Overview

The audio controller consists of I^2S protocols to interface with external audio CODEC. The I^2S interface

supports 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

5.13 Storage Interface Controller

5.13.1 Overview

The Storage Interface Controller (SIC) has DMAC unit and FMI unit. The DMAC unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory and shared buffer (128 bytes). The FMI control the interface of SD/SDHC/SDIO/MMC or NAND/SM. The storage interface controller can support SD/SDHC/SDIO/MMC card and NAND-type flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

5.14 USB 2.0 Device Controller (USBD)

5.14.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains four configurable endpoints in addition to control endpoint.These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

5.15 USB Host Controller (USBH)

5.15.1 Overview

The Universal Serial Bus (USB) is a fast, bi-directional, isochronous, low-cost, dynamically attachable serial interface standard intended for modem, scanners, PDAs, keyboards, mice, and digital imaging devices. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and a network of peripheral devices. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

5.16 Enhanced DMA Controller

5.16.1 Overview

The N9H26 contains an enhanced direct memory access (EDMA) controller that transfers data to and from memory or transfer data to and from APB. The EDMA controller has 6-channel DMA that include 2 channel VDMA (Video-DMA, Memory-to-Memory) and four channels PDMA (Peripheral-to-Memory or Memory-to-Peripheral). For channel0/5 VDMA mode, it also support color format transform and stripe mode transfer. For PDMA channel (EDMA CH1~CH4), it can transfer data between the Peripherals APB IP (ex: UART, SPI, ADC….) and Memory.

5.17 Advanced Interrupt Controller (AIC)

5.17.1 Overview

An interrupt temporarily changes the execution sequence of a program to react to a particular event such as power failure, watchdog timer timeout, engine complete, system events, external event trigger and so on. The ARM9 processor provides two modes of interrupts, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general purpose. The IRQ exception is occurred when the nIRQ input is asserted. Similarly, the FIQ exception is occurred when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F-bit and I-bit in the current program status register (CPSR).

5.18 General Purpose I/O (GPIO)

5.18.1 Overview

80 pins of General Purpose I/O are shared with special feature functions.

Supported Features of these I/O are: input or output facilities, pull-up resistors.

All these general purpose I/O functions are achieved by software programming setting and I/O cells selected from SMIC universal standard I/O Cell Library. And the following figures illustrate the control mechanism to achieve the GPIO functions.

5.19 Timer Controller (TMR)

5.19.1 Overview

The timer module includes four channels, TIMER0~TIMER3, which allow you to easily implement a counting scheme for use. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer possesses features such as adjustable resolution, programmable counting period, and detailed information. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

5.20 Watchdog Timer (WDT)

5.20.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

5.21 Real Time Clock (RTC)

5.21.1 Overview

Real Time Clock (RTC) block can be operated by independent power supply while the system power is off. The RTC uses a 32.768 KHz external crystal or internal oscillator. It can transmit data to CPU with BCD values. The data includes the time by (second, minute and hour), the day by (day, month and year). In addition, to achieve better frequency accuracy, the RTC counter can be adjusted by software.

5.22 I²C Synchronous Serial Interface Controller (I²C)

5.22.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

5.23 Pulse Width Modulation (PWM)

5.23.1 Overview

There are 4 PWM-Timers. The 4 PWM-Timers has 2 Pre-scale, 2 clock divider, 4 clock selectors, 4 16-bit counters, 4 16-bit comparators, 2 Dead-Zone generators. They are all driven by Crystal or system clock. Each can be used as a timer and issues interrupt independently.

5.24 UART Interface Controller (UART)

5.24.1 Overview

The N9H26 provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1 perform Normal Speed UART.

5.25 SPI Serial Interface Controller (SPI Master/Slave)

5.25.1 Overview

The MICROWIRE/SPI Synchronous Serial Interface performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from CPU. This interface can drive up to 2 external peripherals and is seen as the master or can be driven as the slave.

5.26 Analog to Digital Converter (ADC)

5.26.1 Overview

The N9H26 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with eight input channels. The A/D converter supports two operation modes: 4-wire or 5-wire mode. The ADC is especially suitable to act as touch screen controller. Battery voltage detection could be easily accomplished by the SAR ADC. It has keypad interrupt signal generator.

5.27 Keypad Interface (KPI)

5.27.1 Overview

The Keypad Interface (KPI) is an APB slave with configurable minimum 2-row up to 16-row scan output and minimum 1-column up to 4-column scan input. Any keys in the array pressed or released are de-bounced and generate an interrupt.

5.28 Ethernet MAC Controller

5.28.1 Overview

The N9H26 provides a Ethernet MAC Controller (EMC) for WAN/LAN application. This EMC has its DMA controller, transmit FIFO, and receive FIFO.

The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for Ethernet MAC address recognition, Transmit-FIFO, Receive-FIFO, TX/RX state machine controller and status controller. The EMC only supports RMII (Reduced MII) interface to connect with PHY operating on 50MHz REF_CLK.

5.29 Audio Record Control

5.29.1 Overview

The Audio Record control block has two parts. One is the analog IP (sigma-delta ADC), and the other is digital audio record control. The analog IP interface is I^2C and I^2S. I^2C is for command, and I^2S is for audio data. Digital part includes three blocks, AGC and NG block, I^2C wrapper, and Register. The Register block is to handshake with APB bus. AGC and NG are to control the gain automatically. I^2C wrapper is for transferring the command to the ADC.

5.30 AAC IMDCT/MDCT Engine

5.30.1 Overview

AAC IMDCT/MDCT engine is designed to calculate the data for the AAC decoder or encoder.

5.31 Secure-Digital Input / Output Controller

5.31.1 Overview

The Secure-Digital Input / Output Controller (SDIO) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit control the interface of SD/SDHC/SDIO/MMC. The SDIO controller can support SD/SDHC/SDIO/MMC card and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

6 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the N9H26 electrical characteristics.

6.1 Absolute Maximum Ratings

Parameters	Values
Ambient Temperature	-20 °C ~ 85 °C
Storage Temperature	-40 °C ~ 125 °C
Voltage On Any Pin	-0.3V ~ 3.6V
Power Supply Voltage (Core Logic)	-0.5V ~ 1.5V
Power Supply Voltage (I/O Buffer)	-0.5V ~ 4.6V
Injection Current (Latch-Up Testing)	100mA
Crystal Frequency	12MHz

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

6.2 DC Electrical Characteristics

6.2.1 N9H26 Series DC Electrical Characteristics

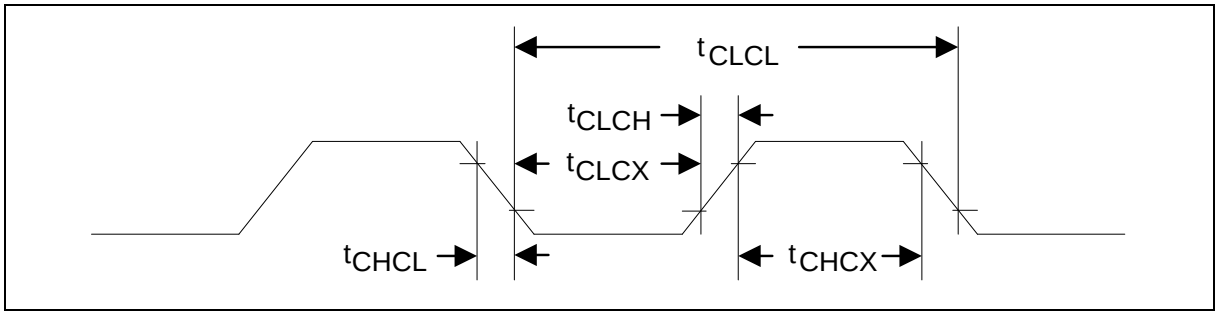
(V_{DD}-V_{SS}=3.3 V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VDD33	I/O Buffer Post-Driver Voltage		2.97	3.30	3.63	V
VDD12	Core Logic Voltage	For N9H26K63N	1.15	1.20	1.25	V
MVDD	SDRAM Voltage	For N9H26K63N	1.75	1.80	1.85	V
RTC_VDD	RTC Power Supply		2.0		3.6	V
I_{RTC_VDD}	RTC Supply Current			10		uA
V_{IH}	Input High Voltage		2.0		VDD33 +0.3	V
V_{IL}	Input Low Voltage				0.8	V
V_T	Threshold Point			1.65		V
V_{T+}	Schmitt Trigger Low to High Threshold Point		1.7		1.96	V
V_{T-}	Schmitt Trigger High to Low Threshold Point		0.87		1.11	V
I_{CC1}	Supply Current 1 (Core@1.2V)	CPU@240MHz_MPLL_CLK@360MHz for H.264 ENC/DEC running (all Engines ON)		300		mA
I_{CC2}	Supply Current 2 (Core@1.2V)	CPU@240MHz_MPLL_CLK@360MHz for memory R/W test		182		mA
IMVDD	DRAM Supply Current	CPU@240MHz_MPLL_CLK@360MHz for memory R/W test		40		mA
I_L	Input Leakage Current		-10		10	uA
I_{OZ}	Tri-State Output Leakage Current		-10		10	uA
R_{PU}	Pull-Up Resistor		53	66	120	kohm
R_{PD}	Pull-Down Resistor		37	50	120	kohm
V_{OL}	Output Low Voltage				0.4	V

V_{OH}	Output High Voltage			2.4			V
I_{OL}	Low Level Output Current	4mA I/O	V_{OL} = 0.4V	4.2	6.5	8	mA
		8mA I/O	V_{OL} = 0.4V	8.4	13	16	mA
I_{OH}	High Level Output Current	4mA I/O	V_{OH} = 2.4V	4.7	9.6	14.9	mA
		8mA I/O	V_{OH} = 2.4V	9.4	19.2	29.8	mA

6.3 AC Electrical Characteristics

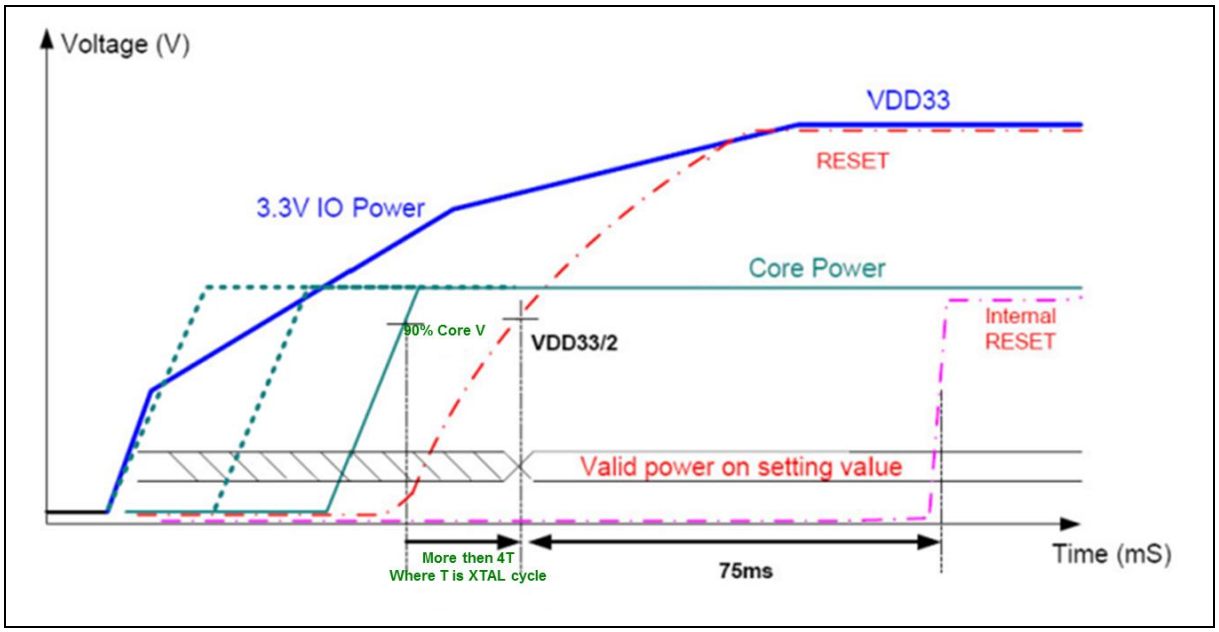
6.3.1 External 12 MHz Crystal



Note: Duty cycle is 50%.

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITION
Clock High Time	t_{CHCX}	20	-	125	nS	
Clock Low Time	t_{CLCX}	20	-	125	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

6.3.2 Power-on Sequence & RESET



6.3.2.1 Power up Sequence

- Higher Voltage (3.3V) First
- Sequence: T33 ≥ T18 ≥ T12, (The time of delay gap between < 500uS is prefer)

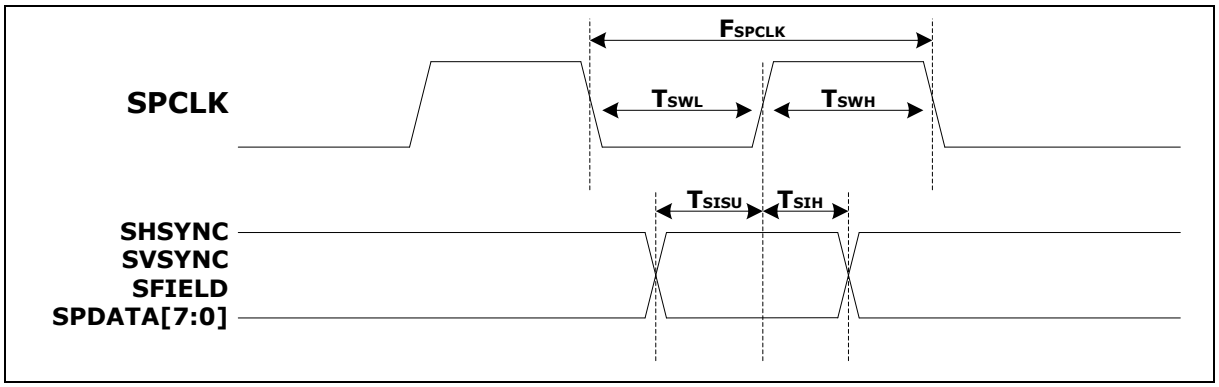
6.3.2.2 Power down Sequence

- The lower voltage (1.2V) should be powered down first
- Sequence: T12 ≥ T18 ≥ T33

Note:

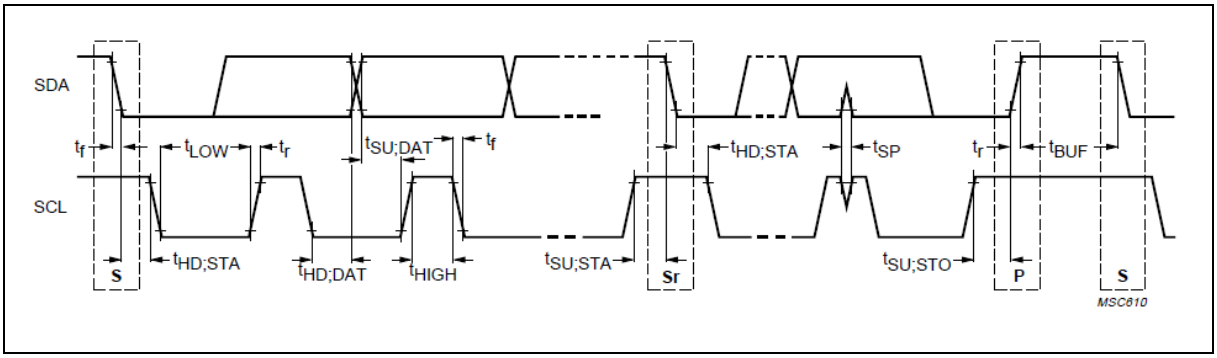
- T12 represents 1.2V powered time for Core power
- T18 represents 1.8V powered time for MVDD power
- T33 represents 3.3V powered time for I/O power

6.3.3 Sensor/Video-In Interface



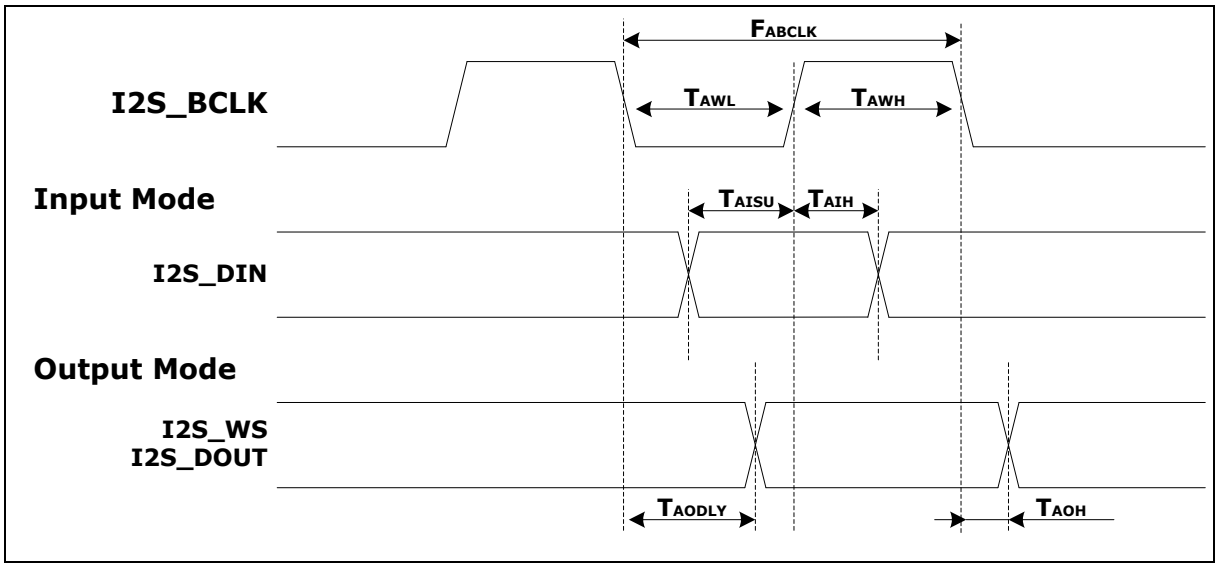
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPCLK Clock Frequency		-	-	72M	MHz
T_{SWL}	SPCLK Clock Low Time		10	-	-	ns
T_{SWH}	SPCLK Clock High Time		10	-	-	ns
T_{SISU}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Setup Time		1.0	-	-	ns
T_{SIH}	SHSYNC, SVSYNC, SFIELD, SPDATA[7:0] Hold Time		1.0	-	-	ns

6.3.4 I²C Interface



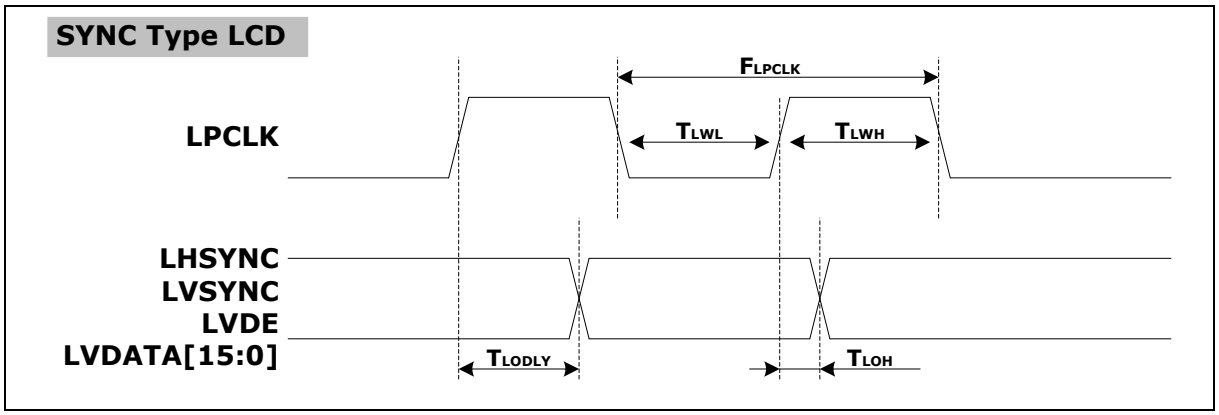
PARAMETER	SYMBOL	STANDARD-MODE		FAST-MODE		UNIT
		MIN.	MAX.	MIN.	MAX.	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	µs
LOW period of the SCL clock	t_{LOW}	4.7	–	1.3	–	µs
HIGH period of the SCL clock	t_{HIGH}	4.0	–	0.6	–	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	µs
Data hold time: for CBUS compatible masters (see NOTE, Section 10.1.3) for I²C-bus devices	$t_{HD;DAT}$	 5.0 0(2)	 – 3.45(3)	 – 0(2)	 – 0.9(3)	 µs µs
Data set-up time	$t_{SU;DAT}$	250	–	100(4)	–	ns
Rise time of both SDA and SCL signals	t_r	–	1000	20 + 0.1C_b(5)	300	ns
Fall time of both SDA and SCL signals	t_f	–	300	20 + 0.1C_b(5)	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0	–	0.6	–	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	–	1.3	–	µs
Capacitive load for each bus line	C_b	–	400	–	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1V_{DD}	–	0.1V_{DD}	–	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2V_{DD}	–	0.2V_{DD}	–	V

6.3.5 I²S Interface

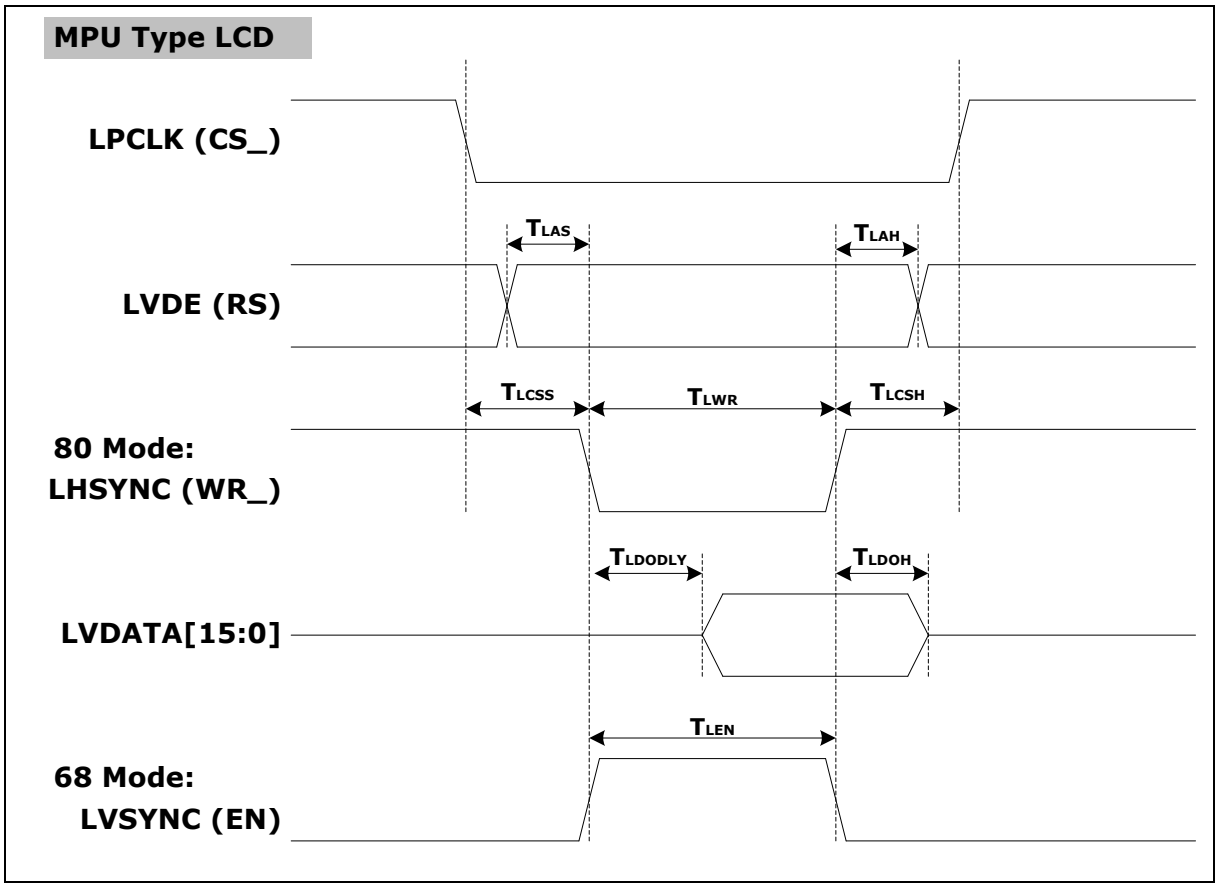


Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{ABCLK}	I2S_BCLK Clock Frequency		-	-	16	MHz
T_{AWL}	I2S_BCLK Clock Low Time		31.25	-	-	ns
T_{AWH}	I2S_BCLK Clock High Time		31.25	-	-	ns
T_{AISU}	I2S_DIN Setup Time		10	-	-	ns
T_{AIH}	I2S_DIN Hold Time		10	-	-	ns
T_{AODLY}	I2S_DOUT Output Delay Time		-	-	0.5	ns
T_{AOH}	I2S_DOUT Output Hold Time		0.1	-	-	ns

6.3.6 LCD/Display Interface



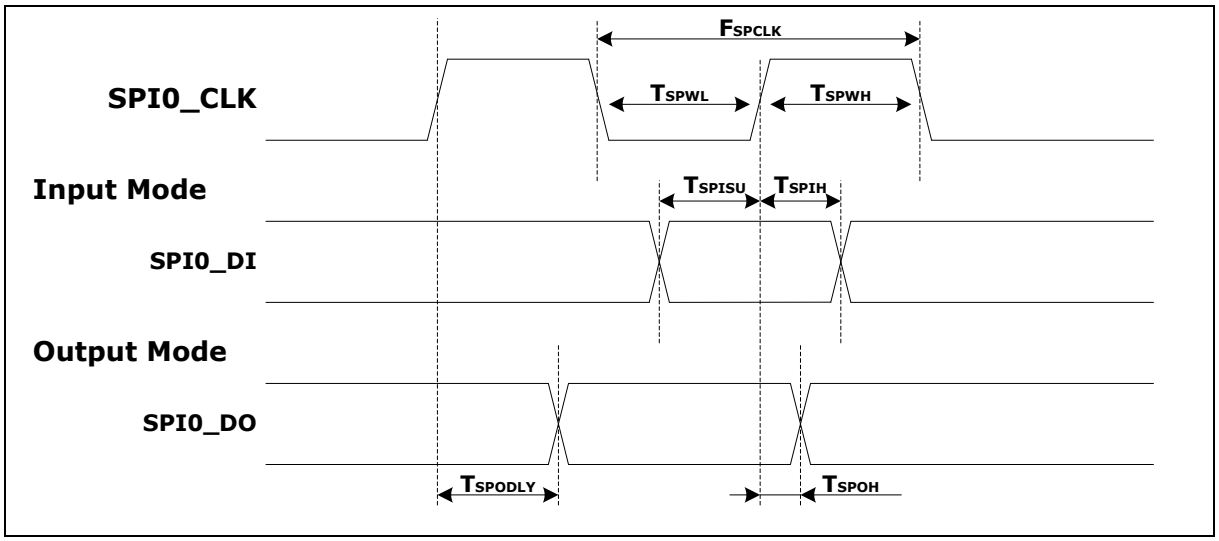
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{LPCLK}	LPCLK Clock Frequency		-	-	120	MHz
T_{LWL}	LPCLK Clock Low Time		18.5	-	-	ns
T_{LWH}	LPCLK Clock High Time		18.5	-	-	ns
T_{LODLY}	LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time		-	-	1.3	ns
T_{LOH}	LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time		0.67	-	-	ns



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{LCSS}	CS_ to WR_ Setup Time		2	-	-	PCLK
T_{LCSH}	CS_ to WR_ Hold Time		1	-	-	PCLK
T_{LAS}	RS to WR_ Setup Time		1	-	-	PCLK
T_{LAH}	RS to WR_ Hold Time		1	-	-	PCLK
T_{LDODLY}	LVDATA Output Delay Time		-	-	1	PCLK
T_{LDOH}	LVDATA Output Hold Time		1	-	-	PCLK
T_{LWR}	WR_ Pulse Width	80 Mode	1	-	-	PCLK
T_{LEN}	EN Pulse Width	68 Mode	1	-	-	PCLK

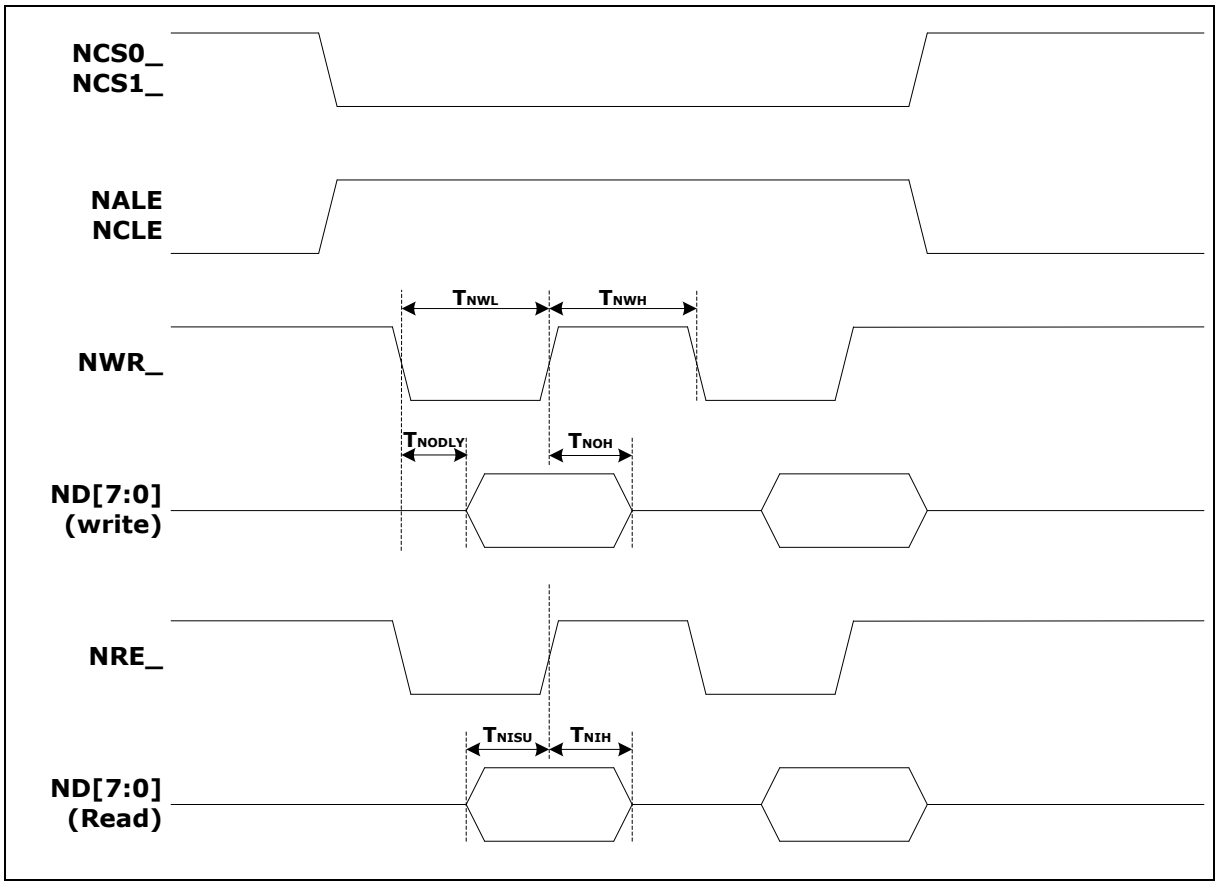
Note: Where PCLK is APB bus clock.

6.3.7 SPI Interface



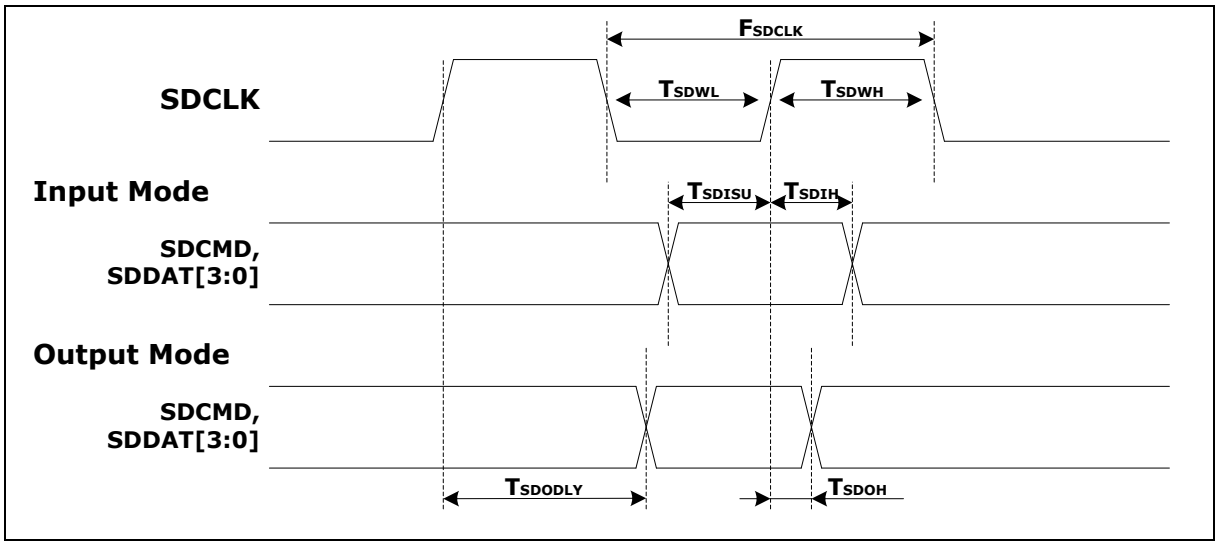
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
F_{SPCLK}	SPI0_CLK Clock Frequency		-	-	25	MHz
T_{SPWL}	SPI0_CLK Clock Low Time		20	-	-	ns
T_{SPWH}	SPI0_CLK Clock High Time		20	-	-	ns
T_{SPISU}	SPI0_DI Setup Time		10	-	-	ns
T_{SPIH}	SPI0_DI Hold Time		10	-	-	ns
T_{SPODLY}	SPI0_DO Output Delay Time		-	-	1	ns
T_{SPOH}	SPI0_DO Output Hold Time		0.2	-	-	ns

6.3.8 NAND Interface



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T_{NWL}	Write Pulse Low Width		10	-	-	ns
T_{NWH}	NWR_ High Hold Time		10	-	-	ns
T_{NODLY}	ND[7:0] Output Delay Time		-	-	2.5	ns
T_{NOH}	ND[7:0] Output Hold Time		10	-	-	ns
T_{NISU}	ND[7:0] Data in Setup Time		3.2	-	-	ns
T_{NIH}	ND[7:0] Data in hold time		1	-	-	ns

6.3.9 SD Card Interface



Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Clock SDCLK						
F_{SDCLK}	Clock Frequency in Data Transfer Mode		-	-	50	MHz
F_{SDCLK}	Clock Frequency in Identification Mode		100	-	400	KHz
T_{SDWL}	Clock Low Time		10	-	-	ns
T_{SDWH}	Clock High Time		10	-	-	ns
Input SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDISU}	Input Setup Time		6	-	-	ns
T_{SDIH}	Input Hold Time		2	-	-	ns
Output SDCMD, SDDAT[3:0] (referenced to SDCLK)						
T_{SDODLY}	Output Delay Time		-	-	14	ns
T_{SDOH}	Output Hold Time		2.5	-	-	ns

6.3.10 USB PHY Specifications

6.3.10.1 USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input high (driven)		2.0	-	-	V
V_{IL}	Input low		-	-	0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2	-	-	V
V_{CM}	Differential common-mode range	Includes VDI range	0.8	-	2.5	V
V_{SE}	Single-ended receiver threshold		0.8	-	2.0	V
	Receiver hysteresis		-	400	-	mV
V_{OL}	Output low (driven)		0	-	0.3	V
V_{OH}	Output high (driven)		2.8	-	3.6	V
V_{CRS}	Output signal cross voltage		1.3	-	2.0	V
R_{PU}	Pull-up resistor		1.425	-	1.575	kΩ
V_{TRM}	Pull-down resistor		14.25	-	15.75	kΩ
Z_{DRV}	Termination Voltage for upstream port pull up (RPU)		3.0	-	3.6	V
C_{IN}	Driver output resistance	Steady state drive*	28	-	49.5	Ω
V_{IH}	Transceiver capacitance	Pin to V_{SS}	-	-	20	pF

Note: Driver output resistance does not include series resistor resistance.

6.3.10.2 USB Full-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{FR}	Rising time	CL = 50p	4	-	20	ns
T_{FF}	Falling time	CL = 50p	4	-	20	ns

6.3.10.3 USB High-Speed Driver Electrical Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T_{FR}	Rising time	CL = 5p	500			ns
T_{FF}	Falling time	CL = 5p	500			ns

6.3.11 Ethernet Interface Timing

6.3.11.1 RMII Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
$T_{P_RMII_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H_RMII_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L_RMII_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY_RMII_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	10	ns	-
$T_{SU_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

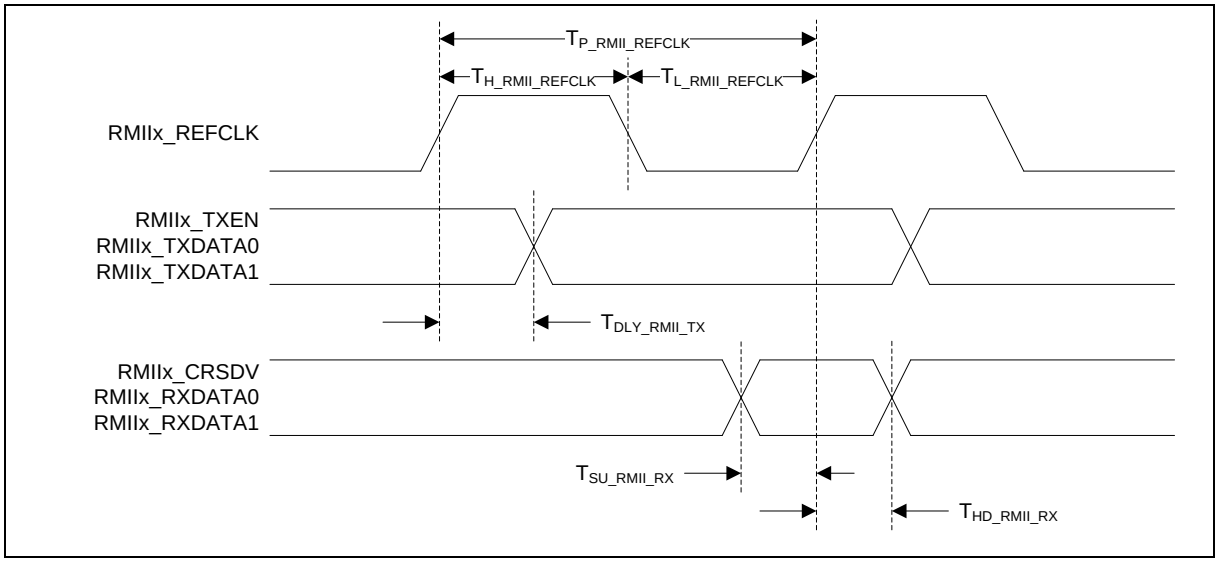


Figure 6.3-1 RMII Interface Timing Diagram

6.3.11.2 Ethernet PHY Management Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
$T_{P_RMII_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H_RMII_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L_RMII_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY_RMII_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU_RMII_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD_RMII_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

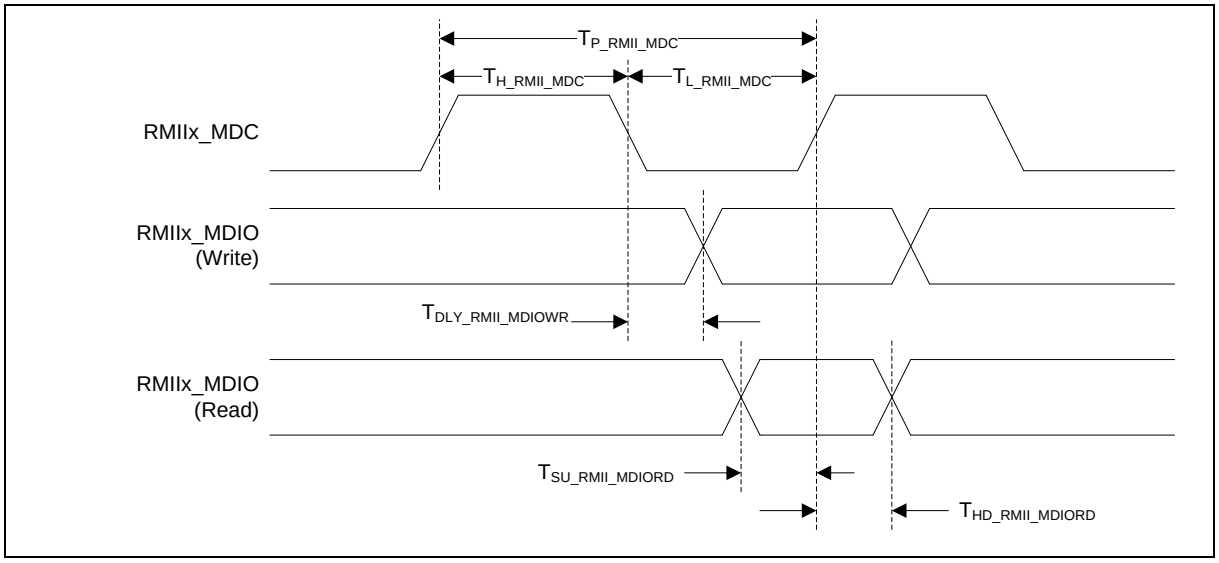


Figure 6.3-2 Ethernet PHY Management Interface Timing Diagram

6.3.12 Specifications of 12-bit SARADC

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		Min.	Typ.	Max.	UNIT	
Operating Voltage	A_{VDD_ADC}	2.7	3.3	3.6	V	
Resolution	R_{ADC}	-	12	-	bit	
Reference Voltage	V_{REF}	2	-	A_{VDD}	V	
ADC input Voltage	V_{IN}	0	-	V_{REF}	V	
Sampling Rate	F_{SPS}	-	-	1M	Hz	ADC Clock = 16MHz Free Running Conversion
Integral Non-linearity Error (INL)	INL	-	±3	-	LSB	
Differential Non-linearity Error (DNL)	DNL	-1	-	+1.5	LSB	
Offset Error	E_{OFFSET}		±1	±3	LSB	
SNR		-	62		dB	

Note: The performance measurement is in ADC only condition (all other IPs are in reset statue).

6.3.13 Specifications of 24-bit Delta-Sigma CODEC

Parameter	Sym	Specifications				Test Conditions
		Min.	Typ.	Max.	Unit	
Reference						
VMID		-	0.5*A_{VDD_CODEC}	-	V	
Microphone Bias						
Bias Voltage		-	0.75*A_{VDD_CODEC}	-	V	
Maximum Output Current		-	-	3	mA	
Capacitive Load		-	-	50	pF	
Line Input						
Resolution		-	24	-	Bit	
Total Harmonic Distortion	THD	-	-80	-70	dB	
Dynamic Range	DR	80	90	-	dB	-60dB input, A-Weighted
S/N	SNR	80	90	-	dB	
Channel Separation		-	100	-	dB	
Channel Matching		-	0.2	-	dB	
Full Scale Output Voltage	VFS	-	0.93* A_{VDD_CODEC}/3.3	-	dB	
Input Impedance		10	-	-	kΩ	
Input Capacitor		-	10	-	pF	
Headphone Output						
Total Harmonic Distortion	THD	-	-80	-	dB	RL = 0 Ohm, Po = 10mW
Total Harmonic Distortion	THD	-	-60	-	dB	RL = 32Ohm, Po = 10mW
S/N	SNR	90	93	-	dB	A-Weighted
Power Supply Current (No PLL, No Loading)						
A_{VDD_CODEC}		-	8	-	mA	
A_{VDD_HP}		-	4	-	mA	

Note: The performance measurement is in CODEC only condition (All other IPs are in reset statue).

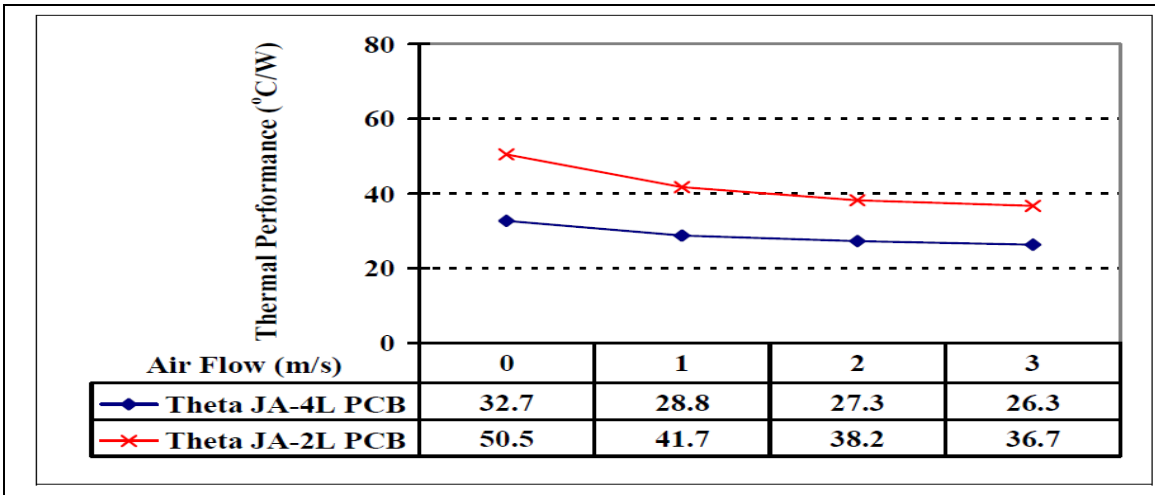
6.3.14 Specification of Low Voltage Reset

Parameter	Conditions	Min.	Typ.	Max.	Unit
Operation voltage	-20℃ ~ 85℃	2	3.3	3.6	V
LVD Detect Levels	LVD_SEL = 0 VDD rises	2.34	2.6	2.86	V
	LVD_SEL = 0 VDD falls	2.295	2.55	2.805	V
	LVD_SEL = 1 VDD rises	2.52	2.8	3.08	V
	LVD_SEL = 1 VDD falls	2.475	2.75	3.025	V
LVR Detect Levels	VDD rises	2.16	2.4	2.64	V
	VDD falls	2.115	2.35	2.585	V

6.3.15 Specifications of Power-on Reset (3.3V)

Parameter	Min.	Typ.	Max.	Unit
Temperature	-20	25	85	℃
Reset voltage	1.05	1.57	1.99	V

6.4 Thermal Characteristics of N9H26 Package

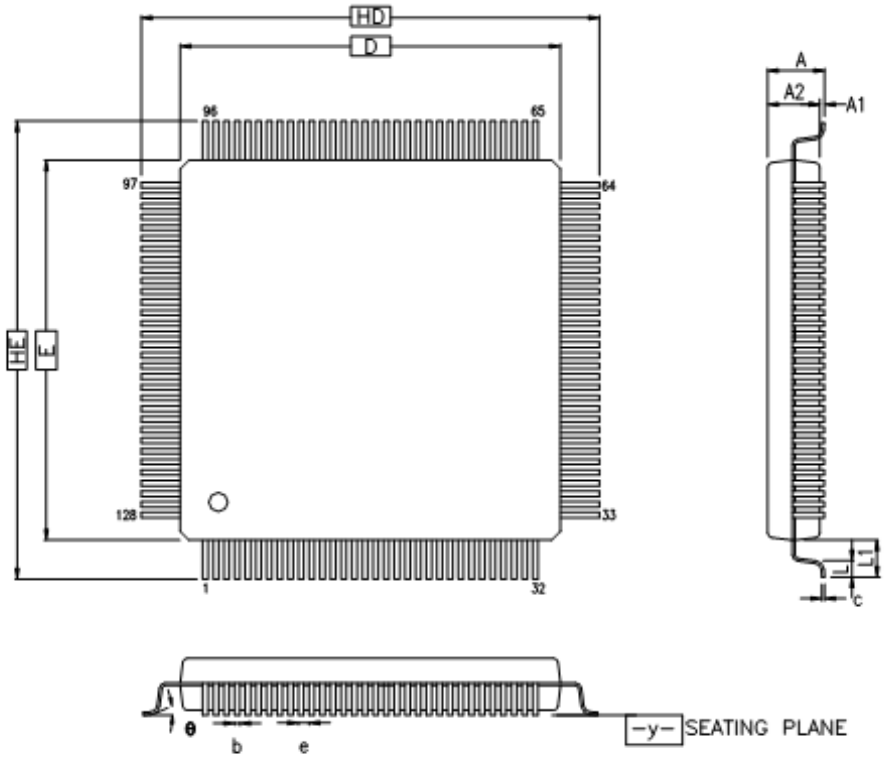


Thermal Performance of SLQFP under Forced Convection

7 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

7.1 LQFP 128L (14x14x1.4mm footprint 2.0mm)

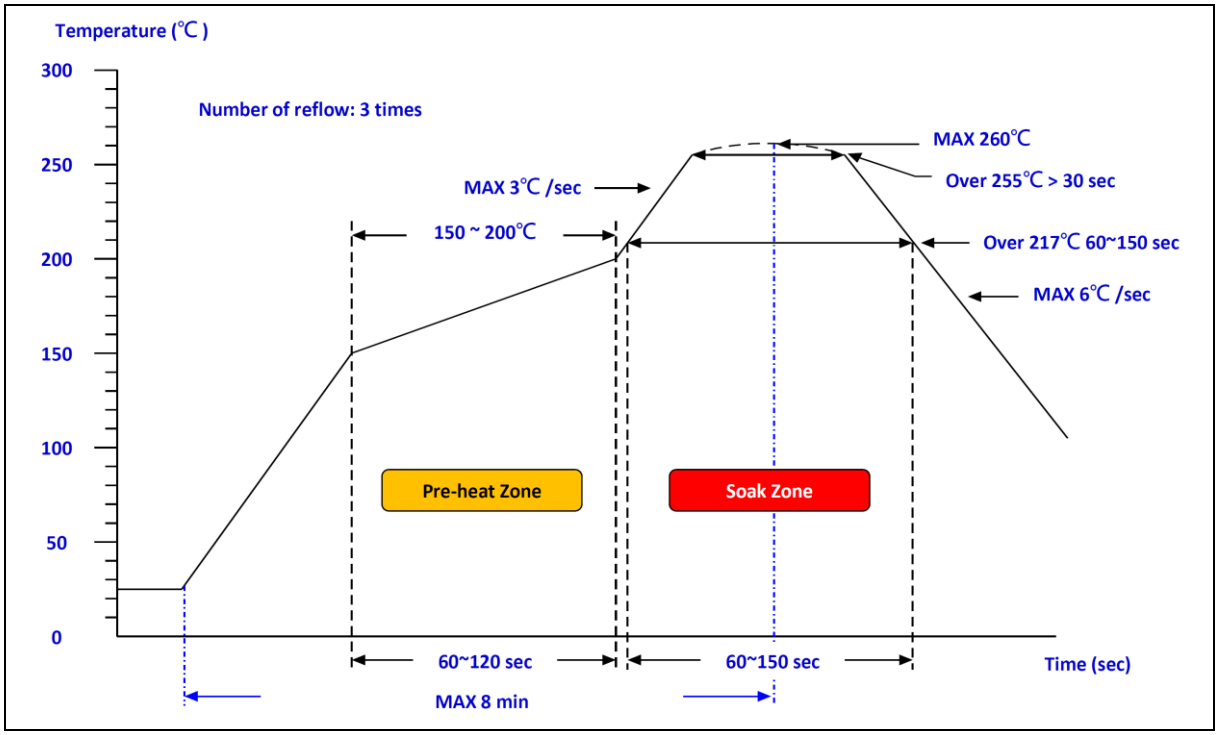


COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A_1	0.05	—	0.15	0.002	—	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

7.2 PCB Reflow Profile

7.2.1 Reflow Profile Suggestion for N9H26 Series



8 REVISION HISTORY

Date	Revision	Description
2018.04.19	1.00	• Initial version.
2018.09.10	1.01	• Added notice for CPU@264MHz limitation in chapter 2. • Added CPU@240MHz DC specification in section 6.2.
2019.10.16	1.10	• Supported CMOS Image Sensor and EMAC functions for N9H26 series in chapter 2.
2019.12.05	1.20	• Added new part No, N9H26K61N in section 3.2.
2020.01.22	1.21	• Revised feature, SPI 0 and 1 can support master/slave mode in chapter 2.
2020.04.16	1.22	• Removed UART0 flow control function in chapter 2 and 3.
2020.11.13	1.23	• Updated selection guide part number, N9H26K61N in section 3.2.
2021.05.13	1.24	• Updated selection guide part number, N9H26K63N in section 3.2. • Removed CPU@264 MHz solution.
2021.11.10	1.25	• Revised selection guide in section 3.2.
2021.11.18	1.26	• Revised reflow profile in section 7.2.
2022.08.01	1.27	• Revised N9H26K63N DC characteristics in section 6.2.
2024.05.28	1.28	• Added “Package is Halogen-free, RoHS-compliant and TSCA-compliant.” In chapter 2 and 7. • Added EMAC function pin in section 3.3.1, 3.2 and 3.4. • Revised feature in chapter 2.

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