## NuMicro® Family

## ARM926EJ-S™-based 32-bit Microprocessor

# N9H20 Series
# Datasheet

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# 1 GENERAL DESCRIPTION

The N9H20 series is built on the ARM926EJ-S, synchronous DRAM, 2D BitBLT accelerator, LCD panel interface, USB 1.1 Host & USB2.0 HS Device core and integrated with JPEG codec, 32-channel SPU (Sound Processing Unit), ADC, DAC, for meeting various kinds of application needs for saving the BOM cost and makes the best choice for LCD application of cost/performance products.

Maximum resolution is XVGA (1,024x768)@TFT LCD panel. The 2D BitBLT accelerator accelerates the graphic computation to make the rendering smooth and off-load CPU to save power consumption.

The open source code environment provides the product development more flexibility. For reducing system complexity while cutting the BOM cost, the N9H20 series provides MCP (Multi-Chip Package) to ensure higher performance and to minimize the system design efforts. Total BOM cost could be cut by employing 2-layer PCB along with the elimination of external parts, EMI prevention components and saving board design space.

## 1.1 Applications

- HMI
- Home Appliance
- Advertisement

# 2 FEATURES

- CPU
  - ARM926EJ-S 32-bit RISC CPU with 8KB I-Cache & 8KB D-Cache
  - Frequency up to 200MHz@1.8V or 240MHz@2.0V core power operation voltage
  - JTAG interface supported for development and debugging

- Internal SRAM & ROM
  - 8KB internal SRAM and 16KB IBR internal booting ROM supported
  - IBR booting messages displayed by UART console for debugging supported
  - Different system booting modes supported:
    - Memory card
      - SD card or eMMC Flash device
      - SD-to-NAND flash bridge
    - Raw NAND Flash
    - SPI Flash
    - USB

- EDMA (Enhanced DMA)
  - Totally 5 DMA channels supported
    - 4 peripheral DMA channels for transfer between memory and on-chip peripherals, such as ADC, UART and SPI
    - One dedicated channel for memory-to-memory transfer
  - Byte, half-word and word data width types supported
  - Single and burst transfer modes supported
  - Block transfer supported in memory-to-memory transfer channel
  - Color format transformation supported in memory-to-memory transfer channel
    - Source color format could be RGB555, RGB565 and YCbCr422
    - Destination color format could be RGB555, RGB565 and YCbCr422
  - Auto reload supported for continuous data transfer
  - Interrupt generation supported in the half-of-transfer or end-of-transfer

- JPEG Codec
  - Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard supported.
  - Planar Format
    - Support to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
    - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
    - Support to decode YCbCr 4:2:2 transpose format
    - Support arbitrary width and height image encode and decode
    - Support three programmable quantization-tables
    - Support standard default Huffman-table and programmable Huffman-table for decode
    - Support arbitrarily 1X~8X image up-scaling function for encode mode
    - Support down-scaling function for encode and decode modes
    - Support specified window decode mode
    - Support quantization-table adjustment for bit-rate and quality control in encode mode
    - Support rotate function in encode mode
  - Packet Format
    - Support to encode interleaved YUYV format input image, output bit stream 4:2:2 and 4:2:0 format
    - Support to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
    - Support decoded output image RGB555, RGB565 and RGB888 formats.

- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode

- 2D Accelerator
  - BitBLT operation
    - 2x2 transform matrix with effects:
      - Scale
      - Translate
      - Rotate
      - Shear
    - Alpha blending and color transformation supported
    - Source format for operations: supported color format of source bitmap
  - Fill
    - Rectangle Fill with single color – ARGB8888
    - Fill with blending effect supported
  - Supported color formats
    - Source
      - 16 bits/pixel – RGB565
      - 32 bits/pixel – ARGB8888
      - 1 bit/pixel, 2 bits/pixel, 4 bits/pixel, 8 bits/pixel with RGB color palette
    - Destination
      - 16 bits/pixel – RGB565
      - 32 bits/pixel – ARGB8888

- VPOST
  - 8/16/18/24-bit SYNC type and 8/9/16/18/24-bit MPU type TFT LCD supported
  - Color format supported:
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data in
    - YCbCr422, RGB565, RGB555, and RGB888 color formats supported for data out
  - XGA (1024x768), SVGA (800x600), WVGA (800x480), D1 (720X480), VGA (640x480), WQVGA (480x272), QVGA (320x240) and HVGA (640x240) resolution supported
    - The maximum resolution is up to 1024X768 for TFT LCD panel for still image displaying
    - The maximum resolution is up to 480x272 for TFT LCD panel for MJPEG video displaying up to 25fps.
  - Display scaler – to fit different size of LCD panels
    - Horizontal: At most 4.0x scale
    - Vertical: At most 3.0x scale
  - For SYNC type LCD:
    - For 8-bit bus
      - CCIR601 YCbCr422 packet mode (NTSC/PAL) supported
      - CCIR601 RGB Dummy mode (NTSC/PAL) supported
      - CCIR656 interface supported
      - RGB Through mode supported
    - For 16/18/24-bit bus
      - Parallel pixel data output mode (1-pixel/1-clock)

- NTSC/PAL interlace & non-interlace output supported
- Color format transform supported:
  - Color format transform between YCbCr422 and RGB565
  - Color format transform from YCbCr422 to RGB888
- Support OSD function to overlap system information like battery life, brightness tuning, volume tuning or muting, etc.

- Frame Switch Controller
  - Frame relation controlled between VPOST and Capture supported
  - 2 modes supported to switch Frame Buffer Base
    - Frame Ratio Mode (16 selectable ratio)
    - Frame sync mode
  - Double/triple buffers supported

- SPU (Sound Processing Unit)
  - 32 stereo channels supported
  - PCM8/PCM16/4-bit MDPCM/TONE source format supported
  - 7-bit volume control supported for each of 32 channels
  - 5-bit pan control supported for each L/R of 32 channels
  - 10-band equalizer supported
  - Special code supported for loop playing and event detection

- Audio DAC
  - 16-bit stereo DAC supported with headphone driver output
  - H/W volume control supported

- I2S Controller
  - I2S interface supported to connect external audio codec
  - 16/18/20/24-bit data format supported

- Storage Interface Controller
  - Interface to NAND Flash:
    - 8-bit data bus width supported
    - SLC and MLC type NAND Flash supported
    - 512B, 2KB, 4KB, and 8KB page size NAND Flash supported
    - ECC4, ECC8, ECC12 and ECC15 algorithm supported for ECC generation, error detection and error correction
    - PBA-NAND flash supported
  - Interface to SD/MMC/SDIO/SDHC/micro-SD cards/ eMMC Flash device supported
    - SD-to-NAND flash bridge supported
  - DMA function supported to accelerate the data transfer between system memory and NAND Flash or SD/MMC/SDIO/SDHC/micro-SD/eMMC Flash device

- USB Device Controller
  - USB2.0 HS (High-Speed) x 1 port
  - 6 configurable endpoints supported
  - Control, Bulk, Interrupt and Isochronous transfers supported
  - Suspend and remote wakeup supported

- USB Host Controller
  - USB1.1 Host one H/W Engine, two pin locations.
  - Fully compliant with USB Revision 1.1 specification
  - Open Host Controller Interface (OHCI) Revision 1.0 compatible
  - Full-speed (12Mbps) and low-speed (1.5Mbps) USB devices supported

- Control, Bulk, Interrupt and Isochronous transfers supported

- Timer & Watch-Dog Timer
  - Two 32-bit with 8-bit pre-scalar timers supported
  - One programmable 24-bit Watch-Dog Timer supported

- PWM
  - 4 PWM channel outputs supported
  - 16-bit counter supported for each PWM channel
  - Two 8-bit pre-scalars supported and each pre-scalar shared by two PWM channels
  - Two clock-dividers supported and each divider shared by two PWM channels
  - Two Dead-Zone generators supported and each generator shared by two PWM channels
  - Auto reloaded mode and one-shot pulse mode supported
  - Capture function supported

- UART
  - A high speed UART supported:
    - Baud rate is up to 1M bps
    - 2 signals TX and RX supported only
  - A normal UART supported:
    - Baud rate is up to 115.2K bps
    - 2 signals TX and RX supported only

- SPI
  - Two SPI controller is supported
    - Both master and slave mode are supported in SPI interface
    - Two chip selection signals for two SPI devices

- I2C
  - One I2C channel supported
  - Compatible with Philips's $I^2C$ standard and only master mode supported
  - Multi-master operation supported

- Advanced Interrupt Controller
  - Total 32 interrupt source supported
  - Configurable interrupt type:
    - Low-active level triggered interrupt
    - High-active level triggered interrupt
    - Low-active edge (falling edge) triggered interrupt
    - High-active edge (rising edge) triggered interrupt
  - Individual interrupt mask bit for each interrupt source
  - 8 different priority levels supported
  - Daisy-chain priority mechanism supported for interrupts with same priority level
  - Low priority interrupt automatic masking supported for interrupt nesting

- RTC
  - Independent power plane supported
  - 32.768 KHz crystal oscillation circuit supported
  - Time counter (second, minute, hour) and Calendar counter (day, month, year) supported
  - Alarm supported (second, minute, hour, day, month and year)
  - 12/24-hour mode and Leap year supported
  - Alarm to wake chip up from Standby mode or from Power-down mode supported
  - Wake chip up from Power-down mode by input pin supported
  - Power-off chip by register setting supported

- Power-on timeout is supported for low battery protection

- GPIO
  - 70 programmable general purpose I/O supported and separated into 5 groups
  - Individual configuration supported for each I/O signal
  - Configurable interrupt control functions supported
  - Configurable de-bounce circuit supported for interrupt function

- ADC
  - Multi-channel, 10-bit ADC supported
    - 2 channels dedicated for 4-wire resistive touch sensor inputs
    - 2 channels dedicated for Audio ADC with Microphone pre-Amp & AGC
    - 3 channels reserved for various purposes, like LVD (Low Voltage Detection), keypad input, and light sensor
    - Input voltage range from 0V ~ 3.3V supported
  - Maximum 25MHz input clock supported
  - Maximum 400K/s conversion rate supported
  - LVR (Low Voltage Reset) supported

- Power Management
  - Advanced power management including Power Down, Deep Standby, CPU Standby, and Normal Operating modes
    - Normal Operating Mode
      - Core power is 1.8V and chip is in normal operation
    - CPU Standby Mode
      - Core power is 1.8V and only ARM CPU clock is turned OFF
    - Deep Standby Mode
      - Core power is 1.8V and all IP clocks are turned OFF
    - Power Down Mode
      - Only the RTC power is ON. Other 3.3V and 1.8V power are OFF

- Operating Voltage
  - I/O: 3.3V
  - Core: 1.8V

- Package
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.
  - LQFP-128 MCP
  - TQFP-64 MCP

# 3 PARTS INFORMATION LIST AND PIN CONFIGURATION

## 3.1 N9H20 Series Part Number Naming Guide

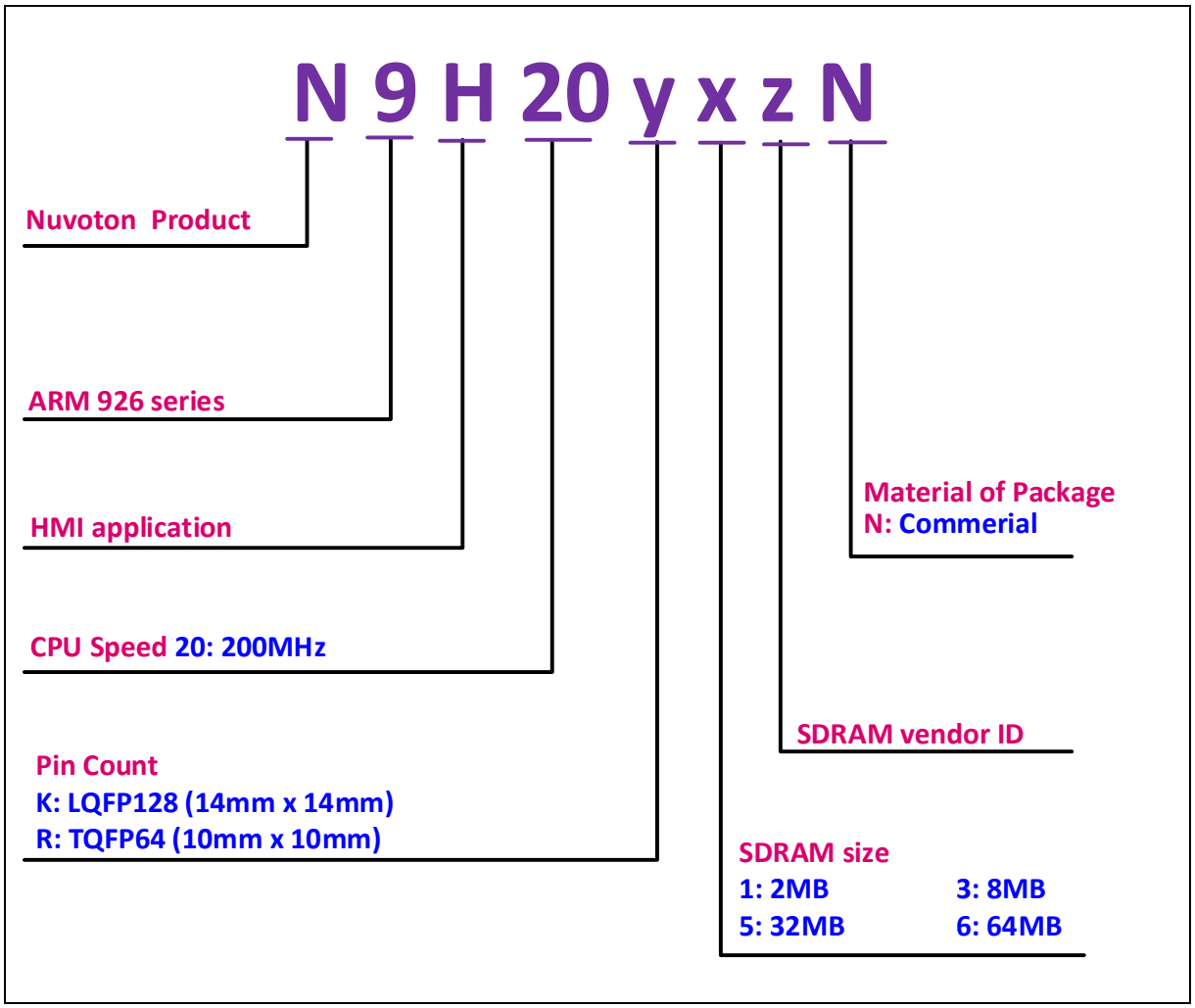



Figure 3-1 N9H20 Series Part Number Naming Guide

## 3.2 N9H20 Series Part Selection Guide

| N9H20 series | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Part No. | Core | | | | Memory | | | | | USB | | H/W Accelerator | | | LCD | | Analog | | | Peripheral | | | | | | | | | | Power | | | PKG | |
| | Max Speed(MHz) | ARM CPU | I cache(KB) | D cache(KB) | SRAM(KB) | Stacked DRAM | SPI Flash I/F | Raw NAND I/F, ECC bits | eMMC/SD/SDIO | 1.1 Host(12Mbps) | Device(FS/HS) | 2D BitBLT GFX | JPEG Codec | Video codec | RGB color (bits) | Max. Resolution[1] | 10/12-bit SAR ADC | 4/5-wire TP ADC | Audio Stereo DAC | JTAG | GPIO(Max) | UART | I²C | SPI booting | SPI | RTC | PWM | I²S | Core Voltage (V) | DRAM Voltage (V) | I/O Voltage (V) | Package | Status[2] |
| N9H20R11N | 200 | 926 | 8 | 8 | 8 | 2MB SDRAM | √ | - | 1 | 1 | HS | √ | √ | JPEG | 16 | QVGA | - | - | - | √ | 44 | 2 | 1 | √ | 1 | - | 4 | - | 1.8 | 3.3 | 3.3 | TQFP-64 | MP |
| N9H20K63N | 200 | 926 | 8 | 8 | 8 | 64MB DDR2 | √ | 15 | 3 | 1 | HS | √ | √ | JPEG | 24 | XGA[3] | 7 | 4W | √ | √ | 70 | 2 | 1 | √ | 2 | √ | 4 | √ | 1.8 | 1.8 | 3.3 | LQFP-128 | MP |
| N9H20K51N | 200 | 926 | 8 | 8 | 8 | 32MB DDR2 | √ | 15 | 3 | 1 | HS | √ | √ | JPEG | 24 | XGA[3] | 7 | 4W | √ | √ | 70 | 2 | 1 | √ | 2 | √ | 4 | √ | 1.8 | 1.8 | 3.3 | LQFP-128 | MP |
| N9H20K31N | 200 | 926 | 8 | 8 | 8 | 8MB DDR | √ | 15 | 3 | 1 | HS | √ | √ | JPEG | 24 | XGA[3] | 7 | 4W | √ | √ | 70 | 2 | 1 | √ | 2 | √ | 4 | √ | 1.8 | 1.8 | 3.3 | LQFP-128 | MP |
| N9H20K11N | 200 | 926 | 8 | 8 | 8 | 2MB SDRAM | √ | 15 | 3 | 1 | HS | √ | √ | JPEG | 24 | QVGA | 7 | 4W | √ | √ | 70 | 2 | 1 | √ | 2 | √ | 4 | √ | 1.8 | 3.3 | 3.3 | LQFP-128 | MP |

[1] Resolution: QVGA(320x240), VGA(640x480), SVGA(800x600), XGA(1024x768).
[2] Status: MP- Mass Production, ES- Engineering Sample, UD- Under Development.
[3] XGA is for still image only.

## 3.3 Pin Configuration

### 3.3.1 N9H20K series Pin Diagram

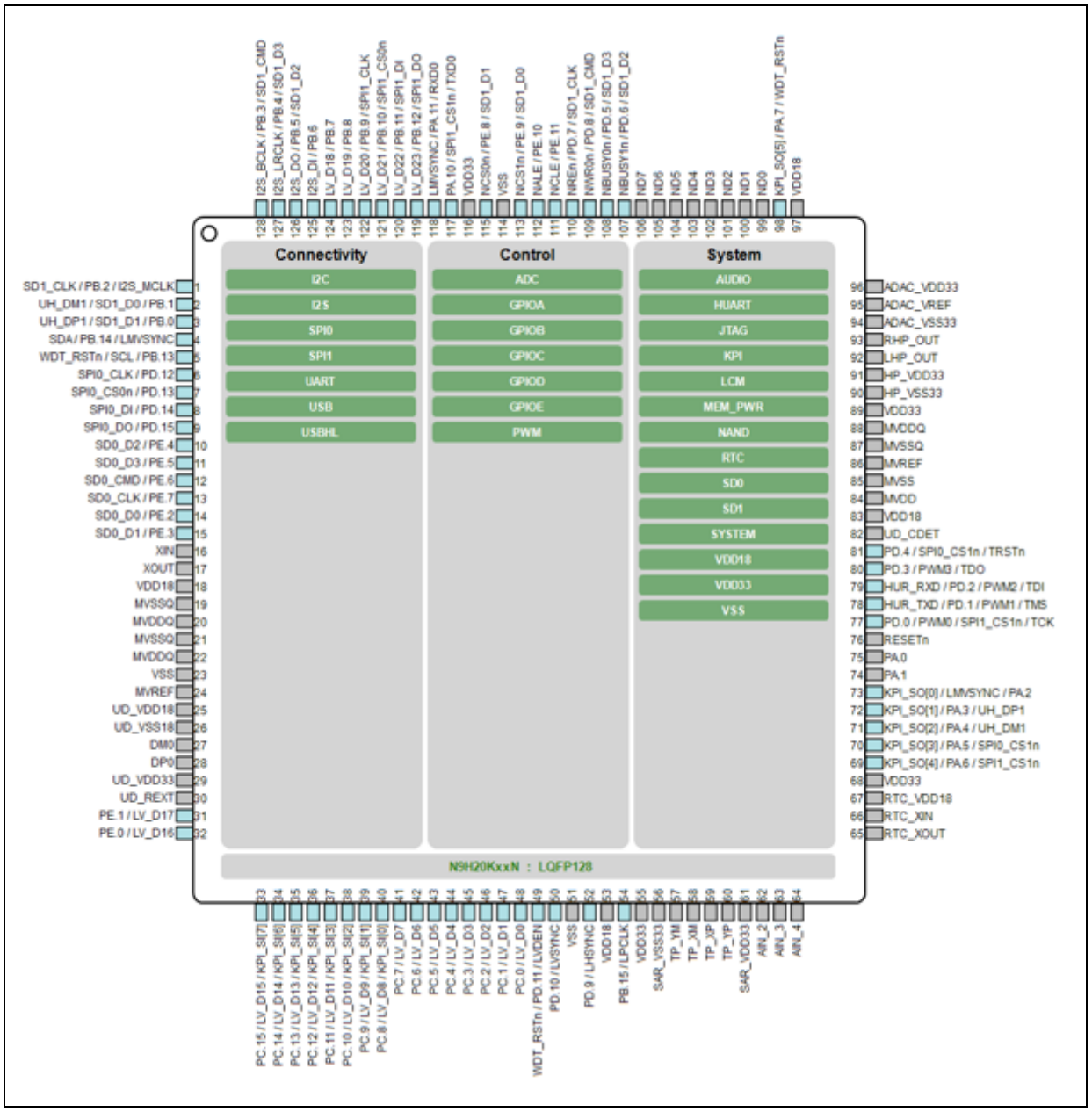



Figure 3.3-1 N9H20K Series LQFP 128 Pin Diagram

### 3.3.2 N9H20R11N Pin Diagram

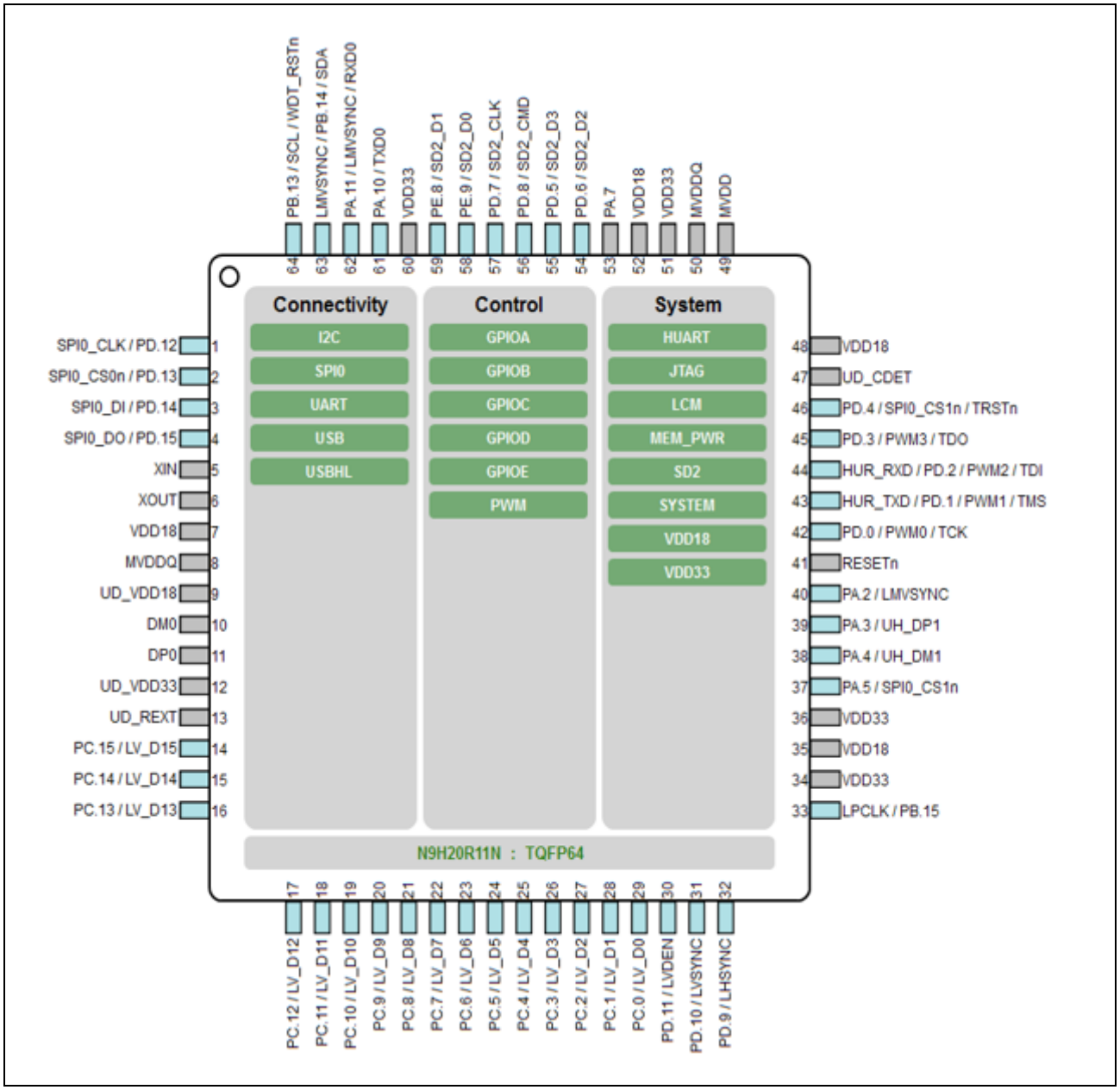



Figure 3.3-2 N9H20R11N TQFP 64 Pin Diagram

## 3.4 Pin Description

### 3.4.1 N9H20K series LQFP128 pin list

| Pin No | Name | Type | Group | Description |
|---|---|---|---|---|
| 1 | GPB[2] | IOU | GPIOB | GPIO Port B Bit 2 |
| | I2S_MCLK | OU | I²S | Clock to I2S Codec, Output |
| | SD1_CLK | OU | SD1 | SD Port 1 Clock, Output |
| 2 | GPB[1] | IOU | GPIOB | GPIO Port B Bit 1 |
| | SD1_DAT[0] | IOU | SD1 | SD Port 1 Data Bit 0 |
| | UHL_DM1 | IOU | USB | USB Host 1.0 Lite Port 1, D-E154 |
| 3 | GPB[0] | IOU | JTAG | GPIO Port B Bit 0 |
| | SD1_DAT[1] | IOU | SD1 | SD Port 1 Data Bit 1 |
| | UHL_DP1 | IOU | USB | USB Host 1.0 Lite Port 1, D+ |
| 4 | ISDA | IOU | I2C | I2C Interface Data |
| | GPB[14] | IOU | GPIOB | GPIO Port B Bit 14 |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| | LMVSYNC | OU | LCD | MPU LCD Interface Mode VSYNC, Output |
| 5 | ISCK | OU | I2C | I2C Interface Clock, Output |
| | GPB[13] | IOU | GPIOB | GPIO Port B Bit 13 |
| 6 | SPI0_CLK | IOU | SPI0 | SPI Port 0 Clock,<br>Output in Master Mode<br>Input in Slave Mode |
| | GPD[12] | IOU | GPIOD | GPIO Port D Bit 12 |
| 7 | SPI0_CS0_ | IOU | SPI0 | SPI Port 0 Device Select 0 (low active),<br>Output in Master Mode<br>Input in Slave Mode |
| | GPD[13] | IOU | GPIOD | GPIO Port D Bit 13 |
| 8 | SPI0_DI | IU | SPI0 | SPI Port 0 Data Input |
| | GPD[14] | IOU | GPIOD | GPIO Port D Bit 14 |
| 9 | SPI0_DO | OU | SPI0 | SPI Port 0 Data Output |
| | GPD[15] | IOU | GPIOD | GPIO Port D Bit 15 |
| 10 | SD0_DAT[2] | IOU | SD0 | SD Port 0 Data Bit 2 |
| | GPE[4] | IOU | GPIOE | GPIO Port E Bit 4 |
| 11 | SD0_DAT[3] | IOU | SD0 | SD Port 0 Data Bit 3 |
| | GPE[5] | IOU | GPIOE | GPIO Port E Bit 5 |
| 12 | SD0_CMD | IOU | SD0 | SD Port 0 Command/Response |
| | GPE[6] | IOU | GPIOE | GPIO Port E Bit 6 |

| | | | | |
|---|---|---|---|---|
| 13 | SD0_CLK | OU | SD0 | SD Port 0 Clock, Output |
| | GPE[7] | IOU | GPIOE | GPIO Port E Bit 7 |
| 14 | SD0_DAT[0] | IOU | SD0 | SD Port 0 Data Bit 0 |
| | GPE[2] | IOU | GPIOE | GPIO Port E Bit 2 |
| 15 | SD0_DAT[1] | IOU | SD0 | SD Port 0 Data Bit 1 |
| | GPE[3] | IOU | GPIOE | GPIO Port E Bit 3 |
| 16 | XIN | I | XTAL | 12MHz Crystal Input |
| 17 | XOUT | O | XTAL | 12MHz Crystal Output |
| 18 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 19 | VSSQ | G | MVDD | SDRAM I/F Ground (0V) |
| 20 | VDDQ | P | MVDD | SDRAM I/F Power |
| 21 | VSSQ | G | MVDD | SDRAM Ground (0V) |
| 22 | MVDD | P | MVDD | SDRAM Power |
| 23 | VSS | G | GND | Ground (0V) |
| 24 | NC | | NC | NC, when N9H20R11N or N9H20K11N is installation |
| | MVREF | P | MVDD | 1/2 MVDD (0.9V) for DDR_VREF, when N9H20K31N or N9H20K51N or N9H20K63N is installation |
| 25 | PLL_UD_VDD18 | P | PLL & USB | PLL & USB2.0 Device Core Power (1.8V) |
| 26 | UD_VSS | G | USB | USB2.0 Device Ground (0V) |
| 27 | UD_DM | I/O | USB | USB 2.0 Device D-. |
| 28 | UD_DP | I/O | USB | USB 2.0 Device D+. |
| 29 | UD_VDD33 | P | USB | USB 2.0 Device PHY 3.3V |
| 30 | UD_REXT | O | USB | External Resistor 12.1K resistor connected to ground |
| 31 | LVDATA[17] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 17 |
| | GPE[1] | IOU | GPIOE | GPIO Port E Bit 1 |
| 32 | LVDATA[16] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 16 |
| | GPE[0] | IOU | GPIOE | GPIO Port E Bit 0 |
| 33 | LVDATA[15] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 15 |
| | GPC[15] | IOU | GPIOC | GPIO Port C Bit 15 |
| | KPI_SI[7] | IU | KPI | KPI Scan In Bit 7 |
| 34 | LVDATA[14] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 14 |
| | GPC[14] | IOU | GPIOC | GPIO Port C Bit 14 |
| | KPI_SI[6] | IU | KPI | KPI Scan In Bit 6 |
| 35 | LVDATA[13] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 13 |
| | GPC[13] | IOU | GPIOC | GPIO Port C Bit 13 |
| | KPI_SI[5] | IU | KPI | KPI Scan In Bit 5 |

| | | | | |
|---|---|---|---|---|
| 36 | LVDATA[12] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 12 |
| | GPC[12] | IOU | GPIOC | GPIO Port C Bit 12 |
| | KPI_SI[4] | IU | KPI | KPI Scan In Bit 4 |
| 37 | LVDATA[11] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 11 |
| | GPC[11] | IOU | GPIOC | GPIO Port C Bit 11 |
| | KPI_SI[3] | IU | KPI | KPI Scan In Bit 3 |
| 38 | LVDATA[10] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 10 |
| | GPC[10] | IOU | GPIOC | GPIO Port C Bit 10 |
| | KPI_SI[2] | IU | KPI | KPI Scan In Bit 2 |
| 39 | LVDATA[9] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 9 |
| | GPC[9] | IOU | GPIOC | GPIO Port C Bit 9 |
| | KPI_SI[1] | IU | KPI | KPI Scan In Bit 1 |
| 40 | LVDATA[8] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 8 |
| | GPC[8] | IOU | GPIOC | GPIO Port C Bit 8 |
| | KPI_SI[0] | IU | KPI | KPI Scan In Bit 0 |
| 41 | LVDATA[7] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 7 |
| | GPC[7] | IOU | GPIOC | GPIO Port C Bit 7 |
| 42 | LVDATA[6] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 6 |
| | GPC[6] | IOU | GPIOC | GPIO Port C Bit 6 |
| | CFG[10] | IU | SYSTEM | Chip Power-On Configuration Bit [10], Input |
| 43 | LVDATA[5] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 5 |
| | GPC[5] | IOU | GPIOC | GPIO Port C Bit 5 |
| | CFG[9] | IU | SYSTEM | Chip Power-On Configuration Bit [9], Input |
| 44 | LVDATA[4] | IOU | LCD | GPIO Port C Bit 4 |
| | GPC[4] | IOU | GPIOC | GPIO Port C Bit 4 |
| | CFG[8] | IU | SYSTEM | Chip Power-On Configuration Bit [8], Input |
| 45 | LVDATA[3] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 3 |
| | GPC[3] | IOU | GPIOC | GPIO Port C Bit 3 |
| 46 | LVDATA[2] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 2 |
| | GPC[2] | IOU | GPIOC | GPIO Port C Bit 2 |
| 47 | LVDATA[1] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 1 |
| | GPC[1] | IOU | GPIOC | GPIO Port C Bit 1 |
| 48 | LVDATA[0] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 0 |
| | GPC[0] | IOU | GPIOC | GPIO Port C Bit 0 |
| 49 | LVDE | OU | LCD | SYNC LCD Interface Data Enable, Output, High Active |
| | LRS | OU | LCD | MPU LCD Interface Register Select |

| | | | | |
|---|---|---|---|---|
| | GPD[11] | IOU | GPIOD | GPIO Port D Bit 11<br>Note. By design limitation, GPD[11] function will be disable when SPI1 is used. |
| 50 | LVSYNC | OU | LCD | SYNC LCD Interface VSYNC, Output, High Active |
| | LRD | OU | LCD | MPU I80 mode LCD Interface Read, active low |
| | LEN | OU | LCD | MPU M68 mode LCD Interface Read Write Enable/Disable , High Enable |
| | GPD[10] | IOU | GPIOD | LCD Interface Data Enable, High Active. |
| 51 | VSS | G | GND | Ground (0V) |
| 52 | LHSYNC | OU | LCD | SYNC LCD Interface HSYNC, Output, High Active |
| | LWR | OU | LCD | MPU I80 mode LCD Interface Write, active low |
| | LR/W | OU | LCD | MPU M68 mode LCD interface R/W, High is read command and Low is write instruction |
| | GPD[9] | IOU | GPIOD | GPIO Port D Bit 9 |
| 53 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 54 | LPCLK | OU | LCD | SYNC LCD Interface Pixel Clock, Output |
| | LCS | OU | LCD | MPU LCD Interface Chip Enable, active low |
| | GPB[15] | IOU | GPIOB | GPIO Port B Bit 15 |
| 55 | VDD33 | P | I/O | I/O Power (3.3V) |
| 56 | ADC_VSS33 | G | ADC | ADC Ground (0V) |
| 57 | ADC_TP_YM | I | ADC | Touch Panel YM |
| 58 | ADC_TP_XM | I | ADC | Touch Panel XM |
| 59 | ADC_TP_XP | I | ADC | Touch Panel XP |
| 60 | ADC_TP_YP | I | ADC | Touch Panel YP |
| 61 | ADC_VDD33 | P | ADC | ADC Power (3.3V) |
| 62 | ADC_AIN[2] | I | ADC | ADC Analog Input Channel 2 |
| 63 | ADC_AIN[3] | I | ADC | ADC Analog Input Channel 3 |
| 64 | ADC_AIN[4] | I | ADC | ADC Analog Input Channel 4 |
| 65 | RTC_XOUT | O | RTC | 32768Hz Crystal Output |
| 66 | RTC_XIN | I | RTC | 32768Hz Crystal Input |
| 67 | RTC_VDD1.8V | P | RTC | RTC Power (1.8V) |
| 68 | VDD33 | P | I/O | I/O Power (3.3V) |
| 69 | GPA[6] | IOU | GPIOA | GPIO Port A Bit 6 |
| | SPI1_CS1_ | OU | SPI1 | SPI Port 1 Device Select 1, Output, Low Active |
| | KPI_SO[4] | OU | KPI | KPI Scan Out Bit 4 |
| 70 | GPA[5] | IOU | GPIOA | GPIO Port A Bit 5 |

| | | | | |
|---|---|---|---|---|
| | SPI0_CS1_ | OU | SPI0 | SPI Port 0 Device Select 1, Output, Low Active |
| | KPI_SO[3] | OU | KPI | KPI Scan Out Bit 3 |
| 71 | GPA[4] | IOU | GPIOA | GPIO Port A Bit 4 |
| | UHL_DM1 | IOU | USB | USB Host 1.0 Lite Port 1, D- |
| | KPI_SO[2] | OU | KPI | KPI Scan Out Bit 2 |
| 72 | GPA[3] | IOU | GPIOA | GPIO Port A Bit 3 |
| | UHL_DP1 | IOU | USB | USB Host 1.0 Lite Port 1, D+ |
| | KPI_SO[1] | OU | KPI | KPI Scan Out Bit 1 |
| 73 | GPA[2] | IOU | GPIOA | GPIO Port A Bit 2 |
| | LMVSYNC | OU | LCD | MPU LCD Interface VSYNC, Output |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| | KPI_SO[0] | OU | KPI | KPI Scan Out Bit 0 |
| 74 | GPA[1] | IOU | GPIOA | GPIO Port A Bit 1 |
| | SD_CD_ | IU | SD | SD Card Detect, Input, Low Active |
| 75 | GPA[0] | IOU | GPIOA | GPIO Port A Bit 0 |
| 76 | RST_ | IU | SYSTEM | System Reset, Input, Low Active |
| | WDT_RST_ | OU | SYSTEM | Watch-Dog Reset, Output, Low Active |
| 77 | TCK | ID | JTAG | JTAG Interface Test Clock, Input |
| | GPD[0] | IOD | GPIOD | GPIO Port D Bit 0 |
| | SPI1_CS1_ | OD | SPI1 | SPI Port 1 Device Select 1, Output, Low Active |
| | PWM0 | OD | PWM | PWM Channel 0 |
| 78 | TMS | IU | JTAG | JTAG Interface Test Mode Select, Input |
| | GPD[1] | IOU | GPIOD | GPIO Port D Bit 1 |
| | HUR_TXD | OU | UART | High-Speed UART TX Data, Output |
| | PWM1 | OU | PWM | PWM Channel 1 |
| 79 | TDI | IU | JTAG | JTAG Interface Test Data In, Input |
| | GPD[2] | IOU | GPIOD | GPIO Port D Bit 2 |
| | HUR_RXD | IU | UART | High-Speed UART RX Data, Input |
| | PWM2 | OU | PWM | PWM Channel 2 |
| 80 | TDO | OU | JTAG | JTAG Interface Test Data Out, Output |
| | GPD[3] | IOU | GPIOD | GPIO Port D Bit 3 |
| | PWM3 | OU | PWM | PWM Channel 3 |
| 81 | TRST_ | IU | JTAG | JTAG Interface Test Reset, Input, Low Active |
| | GPD[4] | IOU | GPIOD | GPIO Port D Bit 4 |
| | SPI0_CS1_ | OU | SPI0 | SPI Port 0 Device Select 1, Output, Low Active |
| 82 | UD_CDET | I | USB | USB Device Connect Detect, Input, High Active |

| | | | | |
|---|---|---|---|---|
| 83 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 84 | MVDD | P | MVDD | SDRAM I/O Power |
| 85 | MVSS | G | MVDD | SDRAM I/F Ground (0V) |
| 86 | MVREF | P | MVDD | 1/2 MVDD (0.9V) for DDR_VREF, when N9H20K31N or N9H20K51N or N9H20K63N is installation |
| | NC | | NC | NC, when N9H20R11N or N9H20K11N is installation |
| 87 | VSSQ | G | MVDD | SDRAM Ground (0V) |
| 88 | VDDQ | P | MVDD | SDRAM Power |
| 89 | VDD33 | P | I/O | I/O Power (3.3V) |
| 90 | ADAC_HPVSS33 | G | AUDIO | Audio DAC Headphone Driver Ground (0V) |
| 91 | ADAC_HPVDD33 | P | AUDIO | Audio DAC Headphone Driver Power (3.3V) |
| 92 | ADAC_HPOUT_L | O | AUDIO | Audio Headphone Left Channel Output |
| 93 | ADAC_HPOUT_R | O | AUDIO | Audio Headphone Right Channel Output |
| 94 | ADAC_AVSS33 | G | AUDIO | Audio DAC Ground (0V) |
| 95 | ADAC_VREF | O | AUDIO | Audio DAC Reference Voltage Output, please connect 1uF capacitor to DAC ground |
| 96 | ADAC_AVDD33 | P | AUDIO | Audio DAC Power (3.3V) |
| 97 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 98 | GPA[7] | IOU | GPIOA | GPIO Port A Bit 7 |
| | KPI_SO[5] | OU | KPI | KPI Scan Out Bit 5 |
| 99 | ND[0] | IOU | NAND | NAND Interface Data Bit [0] |
| | CFG[0] | IU | SYSTEM | Chip Power-On Configuration Bit [0], Input |
| 100 | ND[1] | IOU | NAND | NAND Interface Data Bit [1] |
| | CFG[1] | IU | SYSTEM | Chip Power-On Configuration Bit [1], Input |
| 101 | ND[2] | IOU | NAND | NAND Interface Data Bit [2] |
| | CFG[2] | IU | SYSTEM | Chip Power-On Configuration Bit [2], Input |
| 102 | ND[3] | IOU | NAND | NAND Interface Data Bit [3] |
| | CFG[3] | IU | SYSTEM | Chip Power-On Configuration Bit [3], Input |
| 103 | ND[4] | IOU | NAND | NAND Interface Data Bit [4] |
| | CFG[4] | IU | SYSTEM | Chip Power-On Configuration Bit [4], Input |
| 104 | ND[5] | IOU | NAND | NAND Interface Data Bit [5] |
| | CFG[5] | IU | SYSTEM | Chip Power-On Configuration Bit [5], Input |
| 105 | ND[6] | IOU | NAND | NAND Interface Data Bit [6] |
| | CFG[6] | IU | SYSTEM | Chip Power-On Configuration Bit [6], Input |
| 106 | ND[7] | IOU | NAND | NAND Interface Data Bit [7] |
| | CFG[7] | IU | SYSTEM | Chip Power-On Configuration Bit [7], Input |

| | | | | |
|---|---|---|---|---|
| 107 | NBUSY1_ | IU | NAND | NAND Interface Busy 1, Input, Low Active |
| | GPD[6] | IOU | GPIOD | GPIO Port D Bit 6 |
| | SD2_DAT[2] | IOU | SD2 | SD Port 2 Data Bit 2 |
| 108 | NBUSY0_ | IU | NAND | NAND Interface Busy 0, Input, Low Active |
| | GPD[5] | IOU | GPIOD | GPIO Port D Bit 5 |
| | SD2_DAT[3] | IOU | SD2 | SD Port 2 Data Bit 3 |
| 109 | NWR_ | OU | NAND | NAND Interface Write Enable, Output, Low Active |
| | GPD[8] | IOU | GPIOD | GPIO Port D Bit 8 |
| | SD2_CMD | IOU | SD2 | SD Port 2 Command/Response |
| 110 | NRE_ | OU | NAND | NAND Interface Read Enable, Output, Low Active |
| | GPD[7] | IOU | GPIOD | GPIO Port D Bit 7 |
| | SD2_CLK | OU | SD2 | SD Port 2 Clock, Output |
| 111 | NCLE | OU | NAND | NAND Interface Command-Latch-Enable, Output, High Active |
| | GPE[11] | IOU | GPIOE | GPIO Port E Bit 11 |
| 112 | NALE | OU | NAND | NAND Interface Address-Latch-Enable, Output, High Active |
| | GPE[10] | IOU | GPIOE | GPIO Port E Bit 10 |
| 113 | NCS1_ | OU | NAND | NAND Interface Chip Select 1, Output, Low Active |
| | GPE[9] | IOU | GPIOE | GPIO Port E Bit 9 |
| | SD2_DAT[0] | IOU | SD2 | SD Port 2 Data Bit 0 |
| 114 | VSS | G | GND | Ground (0V) |
| 115 | NCS0_ | IU | NAND | NAND Interface Chip Select 0, Output, Low Active |
| | GPE[8] | IOU | GPIOE | GPIO Port E Bit 8 |
| | SD2_DAT[1] | IOU | SD2 | SD Port 2 Data Bit 1 |
| 116 | VDD33 | P | I/O | I/O Power (3.3V) |
| 117 | URTXD | OU | UART | UART TX Data, Output |
| | GPA[10] | IOU | GPIOA | GPIO Port A Bit 10 |
| | SPI1_CS1_ | OU | SPI1 | SPI Port 1 Device Select 1, Output, Low Active |
| 118 | URRXD | IU | UART | UART RX Data, Input |
| | GPA[11] | IOU | GPIOA | GPIO Port A Bit 11 |
| | LMVSYNC | OU | LCD | MPU LCD Interface VSYNC, Output |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| 119 | GPB[12] | IOU | GPIOB | GPIO Port B Bit 12 |
| | SPI1_DO | OU | SPI1 | SPI Port 1 Data Output |
| | LVDATA[23] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 23 |
| 120 | GPB[11] | IOU | GPIOB | GPIO Port B Bit 11 |

| | | | | |
|---|---|---|---|---|
| | SPI1_DI | IU | SPI1 | SPI Port 1 Data Input |
| | LVDATA[22] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 22 |
| 121 | GPB[10] | IOU | GPIOB | GPIO Port B Bit 10 |
| | SPI1_CS0_ | IOU | SPI1 | SPI Port 1 Device Select 0 (low active),<br>Output in Master Mode<br>Input in Slave Mode |
| | LVDATA[21] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 21 |
| 122 | GPB[9] | IOU | GPIOB | GPIO Port B Bit 9 |
| | SPI1_CLK | IOU | SPI1 | SPI Port 1 Clock,<br>Output in Master Mode<br>Input in Slave Mode |
| | LVDATA[20] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 20 |
| 123 | GPB[8] | IOU | GPIOB | GPIO Port B Bit 8 |
| | LVDATA[19] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 19 |
| 124 | GPB[7] | IOU | GPIOB | GPIO Port B Bit 7 |
| | LVDATA[18] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 18 |
| 125 | GPB[6] | IOU | GPIOB | GPIO Port B Bit 6 |
| | I2S_DIN | IU | I²S | I2S Interface Data Input |
| 126 | GPB[5] | IOU | GPIOB | GPIO Port B Bit 5 |
| | I2S_DOUT | OU | I2S | I2S Interface Data Output |
| | SD1_DAT[2] | IOU | SD1 | SD Port 1 Data Bit 2 |
| 127 | GPB[4] | IOU | GPIOB | GPIO Port B Bit 4 |
| | I2S_WS | OU | I²S | I2S Interface Word Select, Output |
| | SD1_DAT[3] | IOU | SD1 | SD Port 1 Data Bit 3 |
| 128 | GPB[3] | IOU | GPIOB | GPIO Port B Bit 3 |
| | I2S_BCLK | IU | I²S | I2S Interface Clock, Input |
| | SD1_CMD | IOU | SD1 | SD Port 1 Command/Response |

### 3.4.2 N9H20R11N TQFP64 pin list

| Pin No | Name | Type | Group | Description |
|---|---|---|---|---|
| 1 | SPI0_CLK | IOU | SPI0 | SPI Port 0 Clock,<br>Output in Master Mode<br>Input in Slave Mode |
| | GPD[12] | IOU | GPIOD | GPIO Port D Bit 12 |
| 2 | SPI0_CS0_ | IOU | SPI0 | SPI Port 0 Device Select 0 (low active)<br>Output in Master Mode<br>Input in Slave Mode |
| | GPD[13] | IOU | GPIOD | GPIO Port D Bit 13 |
| 3 | SPI0_DI | IU | SPI0 | SPI Port 0 Data Input |
| | GPD[14] | IOU | GPIOD | GPIO Port D Bit 14 |
| 4 | SPI0_DO | OU | SPI0 | SPI Port 0 Data Output |
| | GPD[15] | IOU | GPIOD | GPIO Port D Bit 15 |
| 5 | XIN | I | XTAL | 12MHz Crystal Input |
| 6 | XOUT | O | XTAL | 12MHz Crystal Output |
| 7 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 8 | MVDD33 | P | MVDD | SDRAM Power (3.3V) |
| 9 | PLL_UD_VDD18 | P | PLL & USB | PLL & USB2.0 Device Core Power (1.8V) |
| 10 | UD_DM | I/O | USB | USB 2.0 Device D-. |
| 11 | UD_DP | I/O | USB | USB 2.0 Device D+. |
| 12 | UD_VDD33 | P | USB | USB 2.0 Device PHY 3.3V |
| 13 | UD_REXT | O | USB | External Resistor 12.1K resistor connected to ground |
| 14 | LVDATA[15] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 15 |
| | GPC[15] | IOU | GPIOC | GPIO Port C Bit 15 |
| 15 | LVDATA[14] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 14 |
| | GPC[14] | IOU | GPIOC | GPIO Port C Bit 14 |
| 16 | LVDATA[13] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 13 |
| | GPC[13] | IOU | GPIOC | GPIO Port C Bit 13 |
| 17 | LVDATA[12] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 12 |
| | GPC[12] | IOU | GPIOC | GPIO Port C Bit 12 |
| 18 | LVDATA[11] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 11 |
| | GPC[11] | IOU | GPIOC | GPIO Port C Bit 11 |
| 19 | LVDATA[10] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 10 |
| | GPC[10] | IOU | GPIOC | GPIO Port C Bit 10 |
| 20 | LVDATA[9] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 9 |

| | | | | |
|---|---|---|---|---|
| | GPC[9] | IOU | GPIOC | GPIO Port C Bit 9 |
| 21 | LVDATA[8] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 8 |
| | GPC[8] | IOU | GPIOC | GPIO Port C Bit 8 |
| 22 | LVDATA[7] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 7 |
| | GPC[7] | IOU | GPIOC | GPIO Port C Bit 7 |
| 23 | LVDATA[6] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 6 |
| | GPC[6] | IOU | GPIOC | GPIO Port C Bit 6 |
| 24 | LVDATA[5] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 5 |
| | GPC[5] | IOU | GPIOC | GPIO Port C Bit 5 |
| 25 | LVDATA[4] | IOU | LCD | GPIO Port C Bit 4 |
| | GPC[4] | IOU | GPIOC | GPIO Port C Bit 4 |
| 26 | LVDATA[3] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 3 |
| | GPC[3] | IOU | GPIOC | GPIO Port C Bit 3 |
| 27 | LVDATA[2] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 2 |
| | GPC[2] | IOU | GPIOC | GPIO Port C Bit 2 |
| 28 | LVDATA[1] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 1 |
| | GPC[1] | IOU | GPIOC | GPIO Port C Bit 1 |
| 29 | LVDATA[0] | IOU | LCD | SYNC/MPU LCD Interface Data Bit 0 |
| | GPC[0] | IOU | GPIOC | GPIO Port C Bit 0 |
| 30 | LVDE | OU | LCD | SYNC LCD Interface Data Enable, Output, High Active |
| | LRS | OU | LCD | MPU LCD Interface, Register Select |
| | GPD[11] | IOU | GPIOD | GPIO Port D Bit 11 |
| 31 | LVSYNC | OU | LCD | SYNC LCD Interface VSYNC, Output, High Active |
| | LRD | OU | LCD | MPU I80 mode LCD Interface Read, active low |
| | GPD[10] | IOU | GPIOD | LCD Interface Data Enable, High Active. |
| 32 | LHSYNC | OU | LCD | SYNC LCD Interface HSYNC, Output, High Active |
| | LWR | OU | LCD | MPU I80 mode LCD Interface Write, active low |
| | GPD[9] | IOU | GPIOD | GPIO Port D Bit 9 |
| 33 | LPCLK | OU | LCD | SYNC LCD Interface Pixel Clock, Output |
| | LCS | OU | LCD | MPU LCD Interface Chip Enable, active low |
| | GPB[15] | IOU | GPIOB | GPIO Port B Bit 15 |
| 34 | ADC_VDD33 | P | ADC | ADC Power (3.3V) |
| 35 | RTC_VDD1.8V | P | RTC | RTC Power (1.8V) |
| 36 | VDD33 | P | I/O | I/O Power (3.3V) |
| 37 | GPA[5] | IOU | GPIOA | GPIO Port A Bit 5 |
| | SPI0_CS1_ | OU | SPI0 | SPI Port 0 Device Select 1, Output, Low Active |

| | | | | |
|---|---|---|---|---|
| 38 | GPA[4] | IOU | GPIOA | GPIO Port A Bit 4 |
| | UHL_DM1 | IOU | USB | USB Host 1.0 Lite Port 1, D- |
| 39 | GPA[3] | IOU | GPIOA | GPIO Port A Bit 3 |
| | UHL_DP1 | IOU | USB | USB Host 1.0 Lite Port 1, D+ |
| 40 | GPA[2] | IOU | GPIOA | GPIO Port A Bit 2 |
| | LMVSYNC | OU | LCD | MPU LCD Interface VSYNC, Output |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| 41 | RST_ | IU | SYSTEM | System Reset, Input, Low Active |
| | WDT_RST_ | OU | SYSTEM | Watch-Dog Reset, Output, Low Active |
| 42 | TCK | ID | JTAG | JTAG Interface Test Clock, Input |
| | GPD[0] | IOD | GPIOD | GPIO Port D Bit 0 |
| | SPI1_CS1_ | OD | SPI1 | SPI Port 1 Device Select 1, Output, Low Active |
| | PWM0 | OD | PWM | PWM Channel 0 |
| 43 | TMS | IU | JTAG | JTAG Interface Test Mode Select, Input |
| | GPD[1] | IOU | GPIOD | GPIO Port D Bit 1 |
| | HUR_TXD | OU | UART | High-Speed UART TX Data, Output |
| | PWM1 | OU | PWM | PWM Channel 1 |
| 44 | TDI | IU | JTAG | JTAG Interface Test Data In, Input |
| | GPD[2] | IOU | GPIOD | GPIO Port D Bit 2 |
| | HUR_RXD | IU | UART | High-Speed UART RX Data, Input |
| | PWM2 | OU | PWM | PWM Channel 2 |
| 45 | TDO | OU | JTAG | JTAG Interface Test Data Out, Output |
| | GPD[3] | IOU | GPIOD | GPIO Port D Bit 3 |
| | PWM3 | OU | PWM | PWM Channel 3 |
| 46 | TRST_ | IU | JTAG | JTAG Interface Test Reset, Input, Low Active |
| | GPD[4] | IOU | GPIOD | GPIO Port D Bit 4 |
| | SPI0_CS1_ | OU | SPI0 | SPI Port 0 Device Select 1, Output, Low Active |
| 47 | UD_CDET | I | USB | USB Device Connect Detect, Input, High Active |
| 48 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 49 | MVDD33 | P | MVDD | SDRAM Power (3.3V) |
| 50 | MVDD33 | P | MVDD | SDRAM Power (3.3V) |
| 51 | AVDD33 | P | AUDIO | Audio DAC Power (3.3V) |
| 52 | VDD18 | P | Core | Core Logic Power (1.8V) |
| 53 | GPA[7] | IOU | GPIOA | GPIO Port A Bit 7 |
| | CFG[0] | IU | SYSTEM | Chip Power-On Configuration Bit [0], Input |
| 54 | GPD[6] | IOU | GPIOD | GPIO Port D Bit 6 |

| | | | | |
|---|---|---|---|---|
| | SD2_DAT[2] | IOU | SD2 | SD Port 2 Data Bit 2 |
| 55 | GPD[5] | IOU | GPIOD | GPIO Port D Bit 5 |
| | SD2_DAT[3] | IOU | SD2 | SD Port 2 Data Bit 3 |
| 56 | GPD[8] | IOU | GPIOD | GPIO Port D Bit 8 |
| | SD2_CMD | IOU | SD2 | SD Port 2 Command/Response |
| 57 | GPD[7] | IOU | GPIOD | GPIO Port D Bit 7 |
| | SD2_CLK | OU | SD2 | SD Port 2 Clock, Output |
| 58 | GPE[9] | IOU | GPIOE | GPIO Port E Bit 9 |
| | SD2_DAT[0] | IOU | SD2 | SD Port 2 Data Bit 0 |
| 59 | GPE[8] | IOU | GPIOE | GPIO Port E Bit 8 |
| | SD2_DAT[1] | IOU | SD2 | SD Port 2 Data Bit 1 |
| 60 | VDD33 | P | I/O | I/O Power (3.3V) |
| 61 | URTXD | OU | UART | UART TX Data, Output |
| | GPA[10] | IOU | GPIOA | GPIO Port A Bit 10 |
| | SPI1_CS1_ | OU | SPI1 | SPI Port 1 Device Select 1, Output, Low Active |
| 62 | URRXD | IU | UART | UART RX Data, Input |
| | GPA[11] | IOU | GPIOA | GPIO Port A Bit 11 |
| | LMVSYNC | OU | LCD | MPU LCD Interface VSYNC, Output |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| 63 | ISDA | IOU | I2C | I2C Interface Data |
| | GPB[14] | IOU | GPIOB | GPIO Port B Bit 14 |
| | LFMARK | IU | LCD | MPU LCD Interface Frame Mark, Input |
| | LMVSYNC | OU | LCD | MPU LCD Interface Mode VSYNC, Output |
| 64 | ISCK | OU | I2C | I2C Interface Clock, Output |
| | GPB[13] | IOU | GPIOB | GPIO Port B Bit 13 |
| EPAD | VSS | P | GND | Ground (0V) |

Note:

| TYPE | DESCRIPTION |
|---|---|
| I | Input |
| O | Output |
| I/O | Input / Output |
| IU | Input with internal pull high (50K) |
| OU | Output with internal pull high (50K) |
| IOU | Bi-direction with internal pull high (50K) |
| ID | Input with internal pull low (50K) |
| OD | Output with internal pull low (50K) |
| IOD | Bi-direction with internal pull low (50K) |
| P | Analog Power or Digital Power |
| G | Analog GND or Digital GND |

# 4 BLOCK DIAGRAM

## 4.1 N9H20 Series Block Diagram

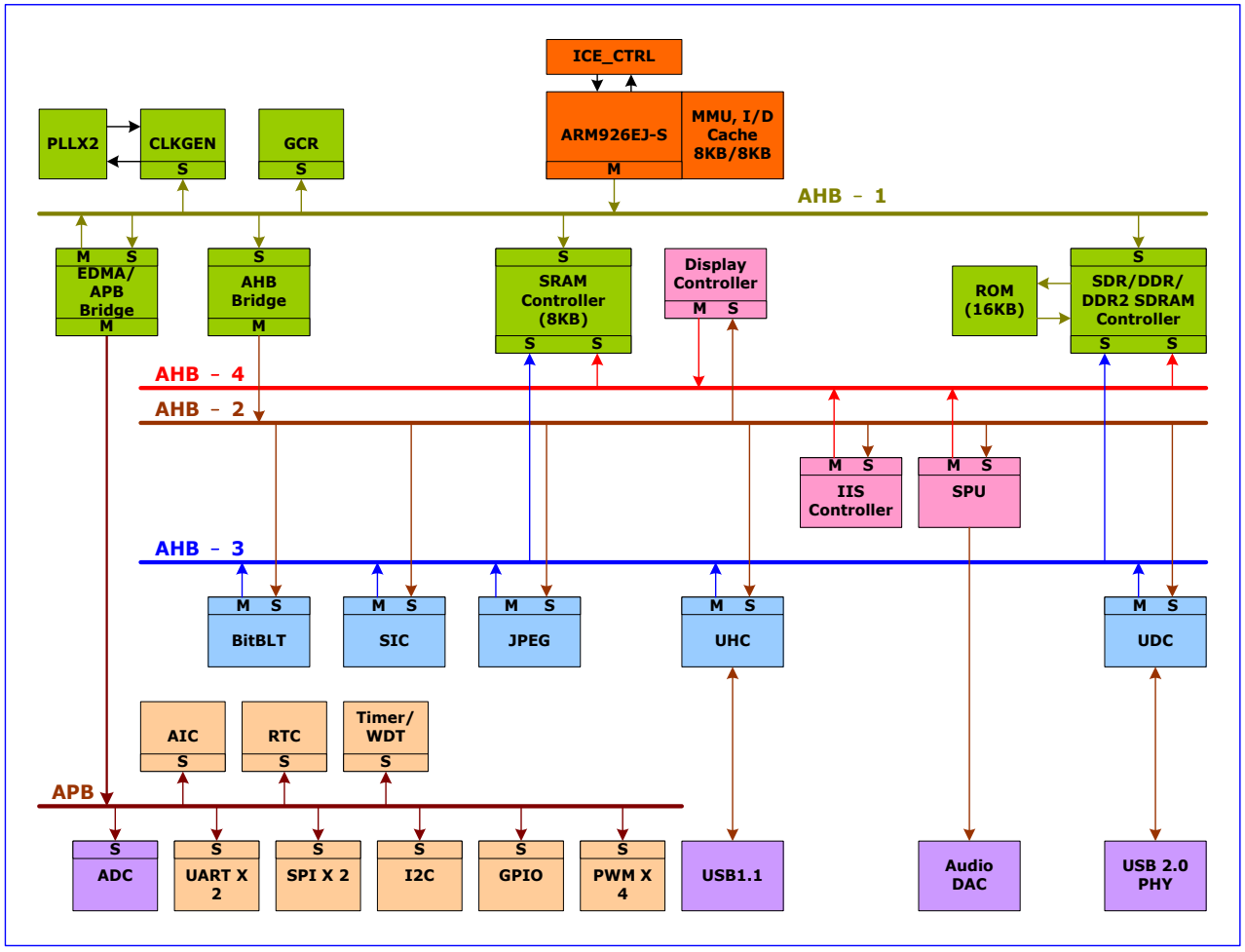



Figure 4.1 N9H20 Series Block Diagram

# 5 FUNCTIONAL DESCRIPTION

## 5.1 ARM® ARM926EJ-S CPU Core

### 5.1.1 Overview

The ARM926EJ-S CPU core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S CPU core is targeted at multi-tasking applications where full memory management, high performance, and low power are all important.

The ARM926EJ-S CPU core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to choose between high performance and high code density.

The ARM926EJ-S processor provides support for external coprocessor enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S CPU core implements ARM architecture version 5TEJ.

The ARM926EJ-S processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core.
- A Memory Management Unit (MMU).
- Separate instruction and data cache.
- Separate instruction and data AMBA AHB bus interfaces.

## 5.2 System Manager

### 5.2.1 Overview

The system management describes following information and functions.

- System Memory Map
- Power-On Setting
- Bus Arbitration Mode
- Power Management
- IBR (Internal Boot ROM) Sequence
- System management registers for product ID, functional reset and multi-function pin control.

## 5.3 Clock Controller (CLK_CTL)

### 5.3.1 Overview

The clock controller generates the clocks for the whole chip, it include all of IPs on AHB, APB and engine clock like USB, UART and so on. There are a PLL in this chip, and the PLL clock source is from the external crystal input. It also implements the power control function, include the individually clock on or off control register, clock source selector and divider. These functions minimize the extra power consumption and the chip run on the only just condition. On the power down mode the controller turn off the crystal oscillator to minimize the chip power consumption.

## 5.4 SDRAM Interface Controller (SDIC)

### 5.4.1 Overview

The SDRAM Controller support SDR, DDR, Low-Power DDR and DDR2 type SDRAM. The memory device size type can be from 16M bit and up to 1G bits. Only 16-bit data bus width is supported. The total system memory size can be from 2M-byte and up to 64M-byte for different SDRAM configuration.

## 5.5 2D Blitting Accelerator

### 5.5.1 Overview

The 2D accelerator feature built on top of the FlashLite Bitmap rendering feature. It improves rendering performance of bitmap objects (source image) onto the frame buffer (destination image).

There are two functions support. First is BitBLT function with effects of Scale, Rotate, Shear and Reflect. The second is Fill function to fill a rectangle in the frame buffer.

## 5.6 JPEG Codec (JPEG)

### 5.6.1 Overview

The JPEG Codec supports Baseline Sequential Mode JPEG still image compression and decompression that is fully compliant with ISO/IEC International Standard 10918-1 (T.81).

## 5.7 LCD Display Interface Controller (VPOST)

### 5.7.1 Overview

The main purpose of Display Controller is used to display the video/image data to LCD device or connect with external TV-encoder. The video/image data source may come from the JPEG decoder and the OSD pattern which have been stored in system memory (SDRAM). The input data format of the display controller can be packet YUV422, packet YUV444, packet RGB444, packet RGB565, packet RGB666, and packet RGB888. The OSD (On Screen Display) function supports packet YUV422 and 8/16/24-bit direct-color mode. The LCD controller supports both sync-type and MPU-type LCDM. This LCD Controller is a bus master and can transfer display data from system memory (SDRAM) without CPU intervention.

## 5.8 Sound Processing Unit (SPU)

### 5.8.1 Overview

The SPU performs 32 channels audio input and 16-bit stereo output to DAC and I2S. SPU support 3 data-types (E-MDPCM (4bit), PCM16, LP8) with event and raw PCM16 mono/stereo and Tone.

## 5.9 I²S Controller (I²S)

### 5.9.1 Overview

The audio controller consists of I2S protocols to interface with external audio CODEC. The I2S interface supports 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

## 5.10 Storage Interface Controller

### 5.10.1 Overview

The Storage Interface Controller (SIC) has SIC_DMA unit and SIC_FMI unit. The SIC_DMAC unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (ex. SDRAM) and shared buffer (128 bytes), and the SIC_FMI unit control the interface of SD/SDHC/SDIO/MMC or NAND/SM. The serial interface controller can support SD/SDHC/SDIO/MMC card and NAND-type flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

## 5.11 USB 2.0 Device Controller (USBD)

### 5.11.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains four configurable endpoints in addition to control endpoint. These endpoints could be configured BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

## 5.12 USB Host Controller (USBH)

### 5.12.1 Overview

The Universal Serial Bus (USB) is a low-cost, low-to mid-speed peripheral interface standard intended for modem, scanners, PDAs, keyboards, mice, and other devices that do not require a high-bandwidth parallel interface. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and a network of peripheral devices. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

## 5.13 Enhanced DMA Controller

### 5.13.1 Overview

The N9H20 contains an enhanced direct memory access (EDMA) controller that transfers data to and from memory or transfer data to and from APB. The EDMA controller has five-channel DMA that include a one channel VDMA (Video-DMA, Memory-to-Memory) and four channels PDMA (Peripheral-to-Memory or Memory-to-Peripheral). For channel0 VDMA mode, it also support color format transform and stripe mode transfer. For PDMA channel (EDMA CH1~CH4), it can transfer data between the Peripherals APB IP (ex: UART, SPI, ADC⋯.) and Memory.

The N9H20 also support hardware scatter-gather function, software can set CSRx [SG_EN] to enable scatter-gather function.

## 5.14 Advanced Interrupt Controller (AIC)

### 5.14.1 Overview

An interrupt temporarily changes the execution sequence of a program to react to a particular event such as power failure, watchdog timer timeout, and engine complete, system events, external event trigger and so on. The ARM9 processor provides two modes of interrupts, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general purpose. The IRQ exception mode is occurred when the NIRQ input is asserted. Similarly, the FIQ exception mode is occurred when the NFIQ input is asserted. The FIQ mode has privilege over the IRQ mode and can preempt an ongoing IRQ mode. It is possible to ignore the NFIQ and the NIRQ by setting the F-bit and I-bit in the current program status register (CPSR).

## 5.15 General Purpose I/O (GPIO)

### 5.15.1 Overview

General Purpose I/O are shared with special feature functions.

Supported Features of these I/O are: input or output facilities, pull-up resistors.

All these general purpose I/O functions are achieved by software programming setting and I/O cells selected from SMIC universal standard I/O Cell Library. And the following figures illustrate the control mechanism to achieve the GPIO functions.

## 5.16 Timer Controller (TMR)

### 5.16.1 Overview

The timer module includes two channels, TIMER0 and TIMER1, which allow easily implement a counting scheme for use. The timer can perform functions like frequency measurement, event counting, interval measurement, clock generation, delay timing, and so on. The timer possesses features such as adjustable resolution, programmable counting period, and detailed information. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

## 5.17 Watchdog Timer (WDT)

### 5.17.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

## 5.18 Real Time Clock (RTC)

### 5.18.1 Overview

Real Time Clock (RTC) block can be operated by independent power supply while the system power is off. The RTC uses a 32.768 KHz external crystal. It can transmit data to CPU with BCD values. The data includes the time by (second, minute and hour), the day by (day, month and year). In addition, to achieve better frequency accuracy, the RTC counter can be adjusted by software.

The built in RTC is designed to generate the alarm interrupt and periodic interrupt signals. The period interrupt can be 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second. The alarm interrupt indicates that time counter and calendar counter have counted to a specified time recorded in TAR and CAR.

## 5.19 I²C Synchronous Serial Interface Controller (I²C)

### 5.19.1 Overview

I2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I2C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Serial, 8-bit oriented bi-directional data transfers can be made up to100 Kbit/s in Standard-mode, and 400 Kbit/s in the Fast-Mode. or up to 3.4 Mbit/s in the High-speed mode. Only 100kbps and 400kbps mode supported directly. For High-speed mode special IOs are needed. If these IOs are available and used, then High-speed mode is also supported.

## 5.20 Pulse Width Modulation (PWM)

### 5.20.1 Overview

There are 4 PWM-Timers. The 4 PWM-Timers has 2 Pre-scale, 2 clock divider, 4 clock selectors, 4 16-bit counters, 4 16-bit comparators, 2 Dead-Zone generators. They are all driven by system clock. Each can be used as a timer and issues interrupt independently.

## 5.21 UART Interface Controller (UART)

### 5.21.1 Overview

The N9H20K provides two channels of Universal Asynchronous Receiver/Transmitters (UART). UART0 supports High Speed UART and UART1 perform Normal Speed UART.

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from the CPU. Each UART channel supports six types of interrupts including transmitter FIFO empty interrupt (Int_THRE), receiver threshold level reaching interrupt (Int_RDA), line status interrupt (overrun error or parity error or framing error or break interrupt) (Int_RLS) , time out interrupt (Int_Tout), MODEM status interrupt (Int_Modem) and Wake up status interrupt (Int_WakeUp).

## 5.22 SPI Interface Controller (SPI Master/Slaver)

### 5.22.1 Overview

The MICROWIRE/SPI Synchronous Serial Interface performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from CPU. This interface can drive up to 2 external peripherals and is seen as the master or can be driven as the slave.

It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral it's connected. Writing a divisor into DIVIDER register can program the frequency of serial clock output when it is as the master. This master/slave core contains four 32-bit transmit/receive buffers, and can provide burst mode operation. The maximum bits can be transmitted/received is 32 bits, and can transmit/receive data up to four times successively.

There is EDMA mode for transmit or received data access by enable the EDMA bit in SPI_EDMA[0]

## 5.23 Analog to Digital Converter (ADC)

### 5.23.1 Overview

The 10-bit analog to digital converter (ADC) in this chip is a successive approximation type ADC with 3-channel inputs. It needs 34 cycles to convert one sample, the maximum conversion rate is 500K/sec, so the maximum input clock to ADC is 17MHz, so and the operating voltage range is 3.3V +/- 10%. The power down mode is supported in the ADC.

The touch screen interfaces are supported in this chip, it contains 4-wire resistive touch screen. The four switches to bias XP, XM, YP, YM are embedded in this chip. The CPU could access the ADC control register by APB bus, and the ADC output an interrupt signal to AIC to represent the completion of conversion.

## 5.24 Keypad Interface (KPI)

### 5.24.1 Overview

The KPI supports release multiple keys, press multiple keys scan interrupt and specified INT_3KEYs interrupt for chip reset. If the 3 pressed keys matches with the 3 keys defined in KPI3KCONF, it will generate an interrupt and chip reset (ENRST must setting) depend on the ENRST setting. The interrupt is generated whenever it detects any key in the keypad pressing or releasing or waking up from IDLE or three-key reset. User can know the interrupt source by querying KPISTATUS register.

# 6 ELECTRICAL CHARACTERISTICS

## 6.1 Absolute Maximum Ratings

| Parameters | Values |
|---|---|
| Ambient Temperature | -20 °C ~ 85 °C |
| Storage Temperature | -40 °C ~ 125 °C |
| Voltage On Any Pin | -0.3V ~ 3.6V |
| Power Supply Voltage (Core Logic) | -0.5V ~ 2.5V |
| Power Supply Voltage (I/O Buffer) | -0.5V ~ 4.6V |
| Injection Current (Latch-Up Testing) | 100mA |
| Crystal Frequency | 1MHz ~ 27MHz |

**Note:** Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

## 6.2 DC Electrical Characteristics

### 6.2.1 N9H20 Series DC Electrical Characteristics

(VDD-VSS=3.3 V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| VDD33 | I/O Buffer Post-Driver Voltage | | 3.0 | 3.3 | 3.6 | V |
| MVDD33 | SDRAM Operation Voltage (for N9H20K11N or N9H20R11N) | SDRAM_CLK=96MHz | 3.0 | 3.3 | 3.6 | V |
| MVDD18 | DDR Operation Voltage (for N9H20K31N or N9H20K51N or N9H20K63N) | DDR_CLK=96MHz | 1.7 | 1.8 | 1.9 | V |
| | | DDR_CLK=120MHz | 1.95 | 2.0 | 2.05 | V |
| VDD18 | Core Logic and I/O Buffer Pre-Driver Voltage | CPU_CLK=192MHz | 1.7 | 1.8 | 1.9 | V |
| | | CPU_CLK=240MHz | 1.95 | 2.0 | 2.05 | V |
| RTC_VDD | RTC Power Supply | | 1.2 | - | 1.8 | V |
| $I_{RTC_VDD}$ | RTC Supply Current | RTC_VDD≦1.8V | - | 6 | - | uA |
| $V_{IH}$ | Input High Voltage | | 2.0 | - | 5.5 | V |
| $V_{IL}$ | Input Low Voltage | | -0.3 | - | 0.8 | V |
| $V_T$ | Threshold Point | | 1.45 | 1.58 | 1.74 | V |
| $V_{T+}$ | Schmitt Trigger Low to High Threshold Point | | 1.44 | 1.50 | 1.56 | V |
| $V_{T-}$ | Schmitt Trigger High to Low Threshold Point | | 0.89 | 0.94 | 0.99 | V |
| $I_{CC}$ | Core Power Supply Current | $F_{CPU}$ = 192MHz, MCLK = 96Hz, VDD18 = 1.8V | - | 140 | - | mA |
| | | FCPU = 240MHz, MCLK = 120Hz, VDD18 = 2.0V | | 180 | | mA |
| $I_L$ | Input Leakage Current | | -10 | - | 10 | uA |
| $I_{OZ}$ | Tri-State Output Leakage Current | | -10 | - | 10 | uA |
| $R_{PU}$ | Pull-Up Resistor | | 39 | 65 | 116 | kΩ |
| $R_{PD}$ | Pull-Down Resistor | | 40 | 56 | 108 | kΩ |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $V_{OL}$ | Output Low Voltage | | | - | - | 0.4 | V |
| $V_{OH}$ | Output High Voltage | | | 2.4 | - | - | V |
| $I_{OL}$ | Low Level Output Current | 4mA I/O | $V_{OL}$ = 0.4V | - | 4.0 | - | mA |
| $I_{OH}$ | High Level Output Current | 4mA I/O | $V_{OH}$ = 2.4V | - | 5.9 | - | mA |

### 6.2.2 ADC Characteristics

| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| SAR ADC Input Voltage Range | 3.0 | - | 3.6 | V |
| Resolution of ADC | - | - | 10 | bit |
| Signal-to-Noise Plus Distortion of ADC from Line In | - | TBD | - | dB |
| Integral Non-Linearity of ADC | - | ±2.0 | - | LSB |
| Differential Non-Linearity of ADC | - | ±0.8 | - | LSB |
| No Missing Code | - | 10 | - | bit |
| AD Conversion Rate=ADCCLK/16 | - | - | 400 | KHz |

### 6.2.3 Audio DAC Characteristics

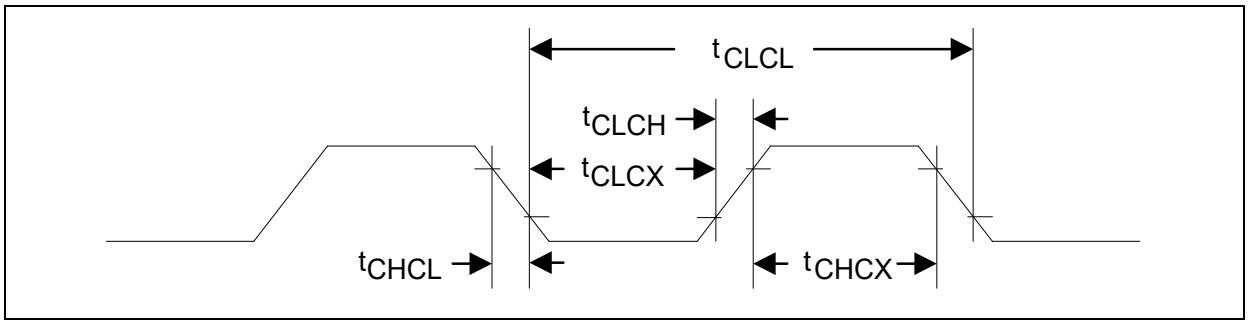
| Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Operating Voltage | 3.0 | 3.3 | 3.6 | V |
| Reference Voltage | - | DAC_VDD/2 | - | V |
| Reference Capacitor | - | 0.1 | - | uF |
| Full Scale output voltage | - | 0.74 | - | Vrms |
| Full Scale output voltage | - | 2.08 | - | Vpp |
| Maximum Output Power | - | - | 52 | mW |
| Maximum Output Power @ 32ohm load | - | - | 46 | mW |
| Maximum Output Power @ 16ohm load | - | - | 41 | mW |
| L-Channel SNR | - | 86 | - | dBV |
| R-Channel SNR | - | 85 | - | dBV |
| L-Channel THD+N | - | -64 | - | dB |
| R-Channel THD+N | - | -64 | - | dB |

| | | | | |
|---|---|---|---|---|
| L-Channel THD+N @ 32ohm load | - | -63 | - | dB |
| R-Channel THD+N @ 32ohm load | - | -63 | - | dB |
| L-Channel THD+N @ 16ohm load | - | -62 | - | dB |
| R-Channel THD+N @ 16ohm load | - | -62 | - | dB |

Test conditions: RL = 10K / 50pF, BW = 20Hz ~ 20KHz, Freq.= 1KHz, Sample Rate = 48KHz.

## 6.3 AC Electrical Characteristics

### 6.3.1 External 12 MHz Crystal

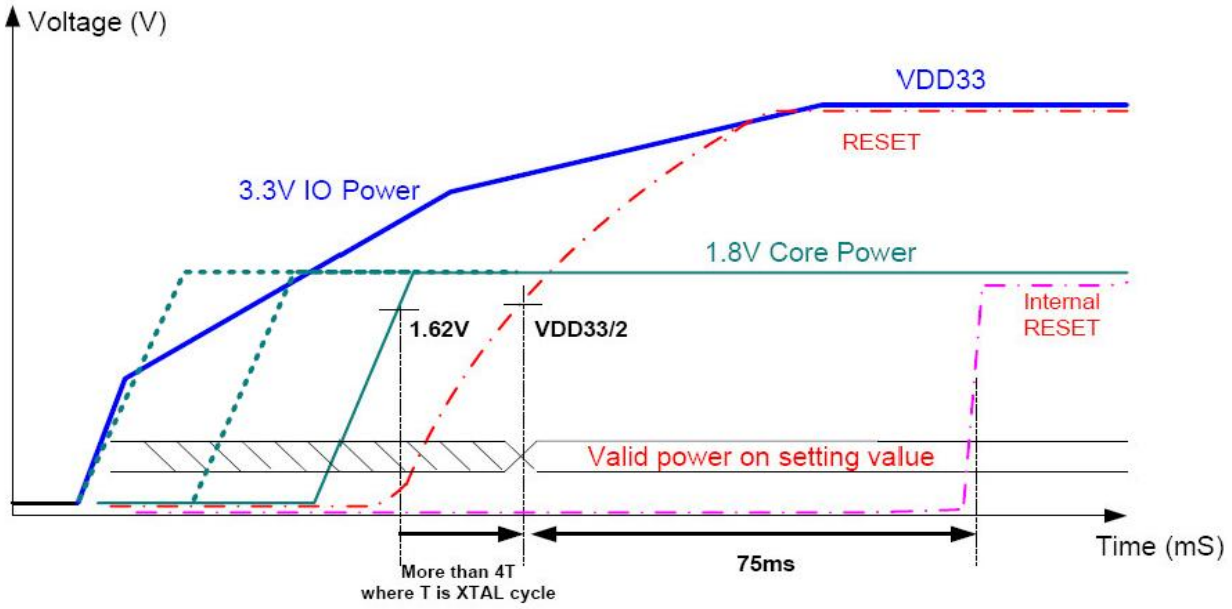



**Note:** Duty cycle is 50%.

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS | CONDITION |
|---|---|---|---|---|---|---|
| Clock High Time | $t_{CHCX}$ | 20 | - | 125 | nS | |
| Clock Low Time | $t_{CLCX}$ | 20 | - | 125 | nS | |
| Clock Rise Time | $t_{CLCH}$ | - | - | 10 | nS | |
| Clock Fall Time | $t_{CHCL}$ | - | - | 10 | nS | |

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{XIN}$ | Clock Input Frequency | - | 12 | - | MHz |
| $XIN_{DUTY}$ | Clock Input Duty Cycle | 45 | 50 | 55 | % |

### 6.3.2 Power-on Sequence & RESET




#### *6.3.2.1 Power up sequence*

- Higher Voltage IO (3.3V) First
- Sequence: T33 ≥ T18 (The time of delay gap between < 500uS is prefer)

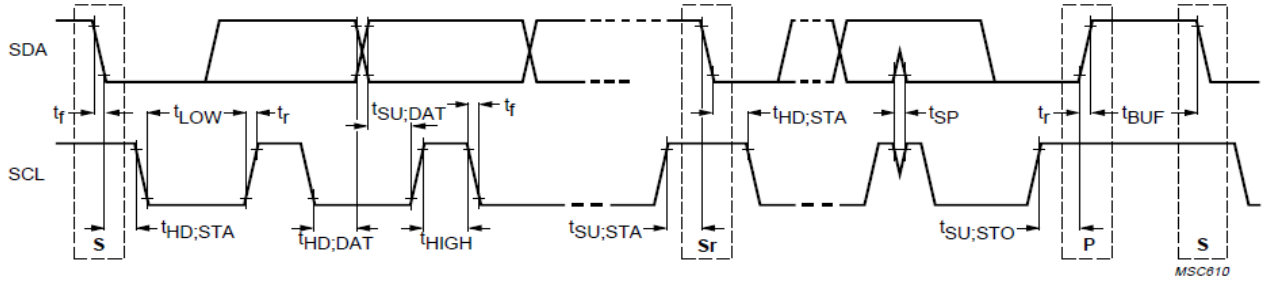
#### *6.3.2.2 Power down Sequence*

- The lower voltage (1.8V) should be powered down first
- Sequence: T18 ≥ T33

Note.

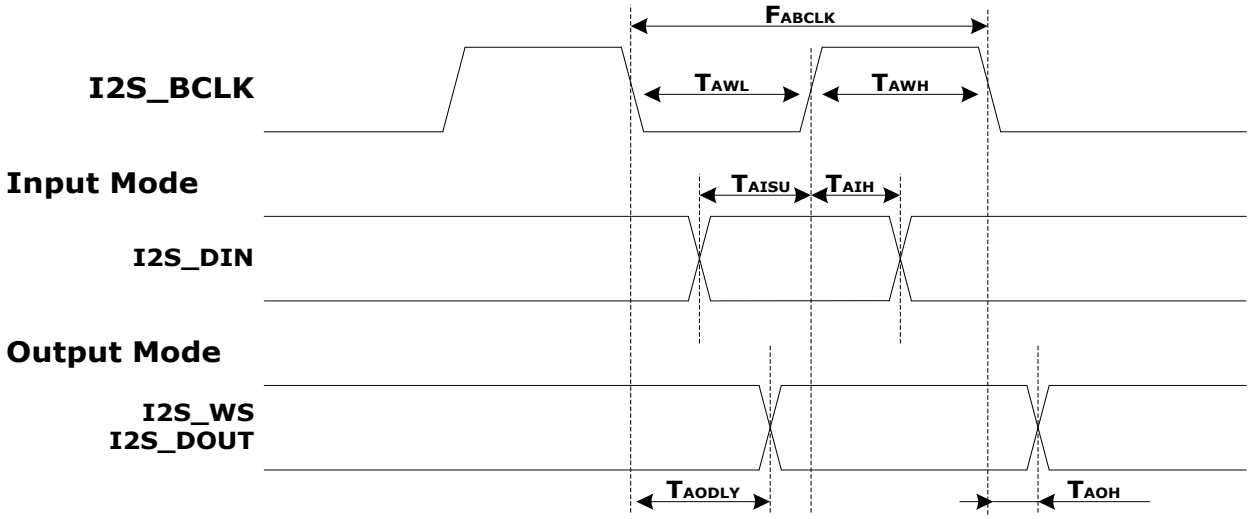
- T18 represents 1.8V powered time for Core power
- T33 represents 3.3V powered time for I/O power

### 6.3.3 I2C Interface




| PARAMETER | SYMBOL | STANDARD-MODE | | FAST-MODE | | UNIT |
|---|---|---|---|---|---|---|
| | | MIN. | MAX. | MIN. | MAX. | |
| SCL clock frequency | $f_{SCL}$ | 0 | 100 | 0 | 400 | kHz |
| Hold time (repeated) START condition. After this period, the first clock pulse is generated | $t_{HD;STA}$ | 4.0 | – | 0.6 | – | µs |
| LOW period of the SCL clock | $t_{LOW}$ | 4.7 | – | 1.3 | – | µs |
| HIGH period of the SCL clock | $t_{HIGH}$ | 4.0 | – | 0.6 | – | µs |
| Set-up time for a repeated START condition | $t_{SU;STA}$ | 4.7 | – | 0.6 | – | µs |
| Data hold time:<br>for CBUS compatible masters (see NOTE, Section 10.1.3)<br>for I²C-bus devices | $t_{HD;DAT}$ | <br>5.0<br>0(2) | <br>–<br>3.45(3) | <br>–<br>0(2) | <br>–<br>0.9(3) | <br>µs<br>µs |
| Data set-up time | $t_{SU;DAT}$ | 250 | – | 100(4) | – | ns |
| Rise time of both SDA and SCL signals | $t_r$ | – | 1000 | 20 + 0.1$C_b$(5) | 300 | ns |
| Fall time of both SDA and SCL signals | $t_f$ | – | 300 | 20 + 0.1$C_b$(5) | 300 | ns |
| Set-up time for STOP condition | $t_{SU;STO}$ | 4.0 | – | 0.6 | – | µs |
| Bus free time between a STOP and START condition | $t_{BUF}$ | 4.7 | – | 1.3 | – | µs |
| Capacitive load for each bus line | $C_b$ | – | 400 | – | 400 | pF |
| Noise margin at the LOW level for each connected device (including hysteresis) | $V_{nL}$ | 0.1$V_{DD}$ | – | 0.1$V_{DD}$ | – | V |
| Noise margin at the HIGH level for each connected device (including hysteresis) | $V_{nH}$ | 0.2$V_{DD}$ | – | 0.2$V_{DD}$ | – | V |

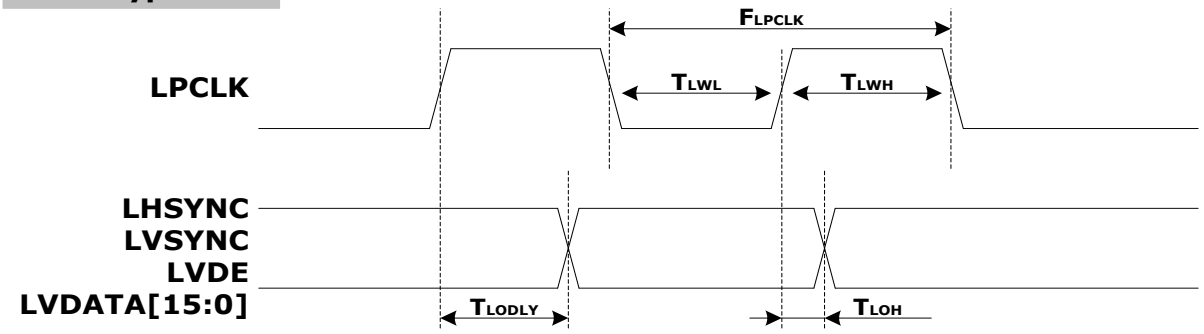
### 6.3.4 I2S Interface




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{ABCLK}$ | I2S_BCLK Clock Frequency | - | - | 16 | MHz |
| $T_{AWL}$ | I2S_BCLK Clock Low Time | 31.25 | - | - | ns |
| $T_{AWH}$ | I2S_BCLK Clock High Time | 31.25 | - | - | ns |
| $T_{AISU}$ | I2S_DIN Setup Time | 10 | - | - | ns |
| $T_{AIH}$ | I2S_DIN Hold Time | 10 | - | - | ns |
| $T_{AODLY}$ | I2S_DOUT Output Delay Time | - | - | 0.5 | ns |
| $T_{AOH}$ | I2S_DOUT Output Hold Time | 0.1 | - | - | ns |

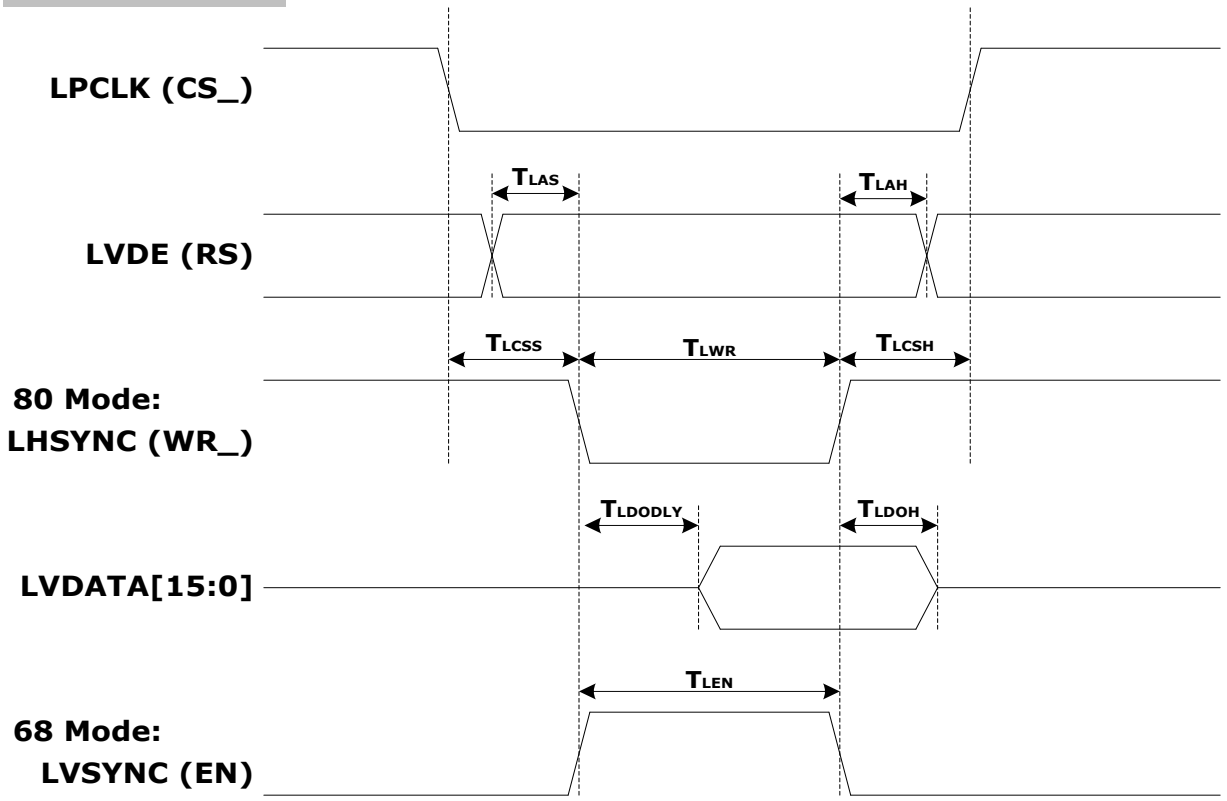
### 6.3.5 LCD/ Display Interface

**SYNC Type LCD**




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{LPCLK}$ | LPCLK Clock Frequency | - | - | 45 | MHz |
| $T_{LWL}$ | LPCLK Clock Low Time | 11.1 | - | - | ns |
| $T_{LWH}$ | LPCLK Clock High Time | 11.1 | - | - | ns |
| $T_{LODLY}$ | LHSYNC, LVSYNC, LVDE and LVDATA Output Delay Time | - | - | 0.78 | ns |
| $T_{LOH}$ | LHSYNC, LVSYNC, LVDE and LVDATA Output Hold Time | 0.4 | - | - | ns |

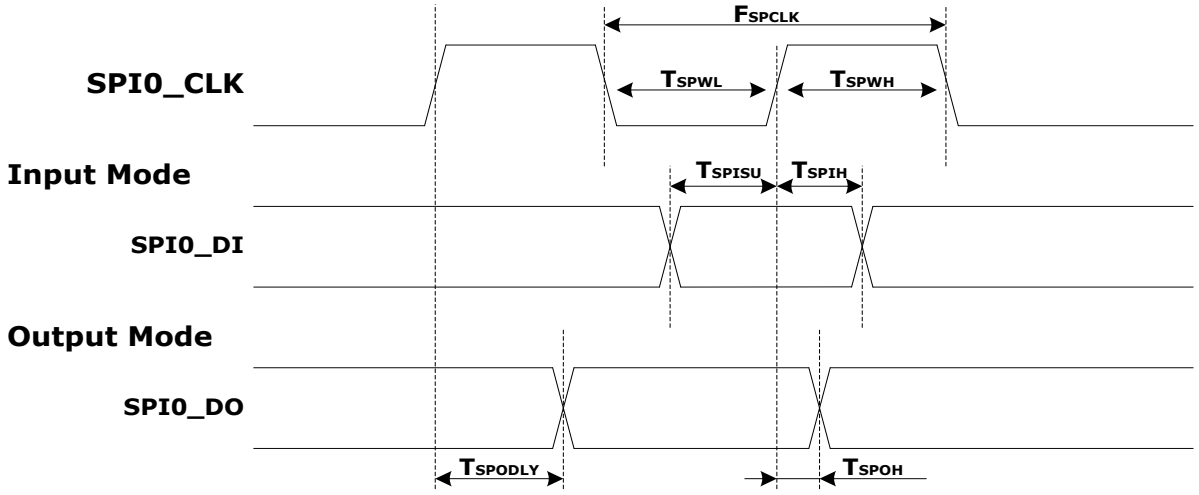
**MPU Type LCD**




| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{LCSS}$ | CS_ to WR_ Setup Time | | 2 | - | - | PCLK |
| $T_{LCSH}$ | CS_ to WR_ Hold Time | | 1 | - | - | PCLK |
| $T_{LAS}$ | RS to WR_ Setup Time | | 1 | - | - | PCLK |
| $T_{LAH}$ | RS to WR_ Hold Time | | 1 | - | - | PCLK |
| $T_{LDODLY}$ | LVDATA Output Delay Time | | - | - | 1 | PCLK |
| $T_{LDOH}$ | LVDATA Output Hold Time | | 1 | - | - | PCLK |
| $T_{LWR}$ | WR_ Pulse Width | 80 Mode | 1 | - | - | PCLK |
| $T_{LEN}$ | EN Pulse Width | 68 Mode | 1 | - | - | PCLK |

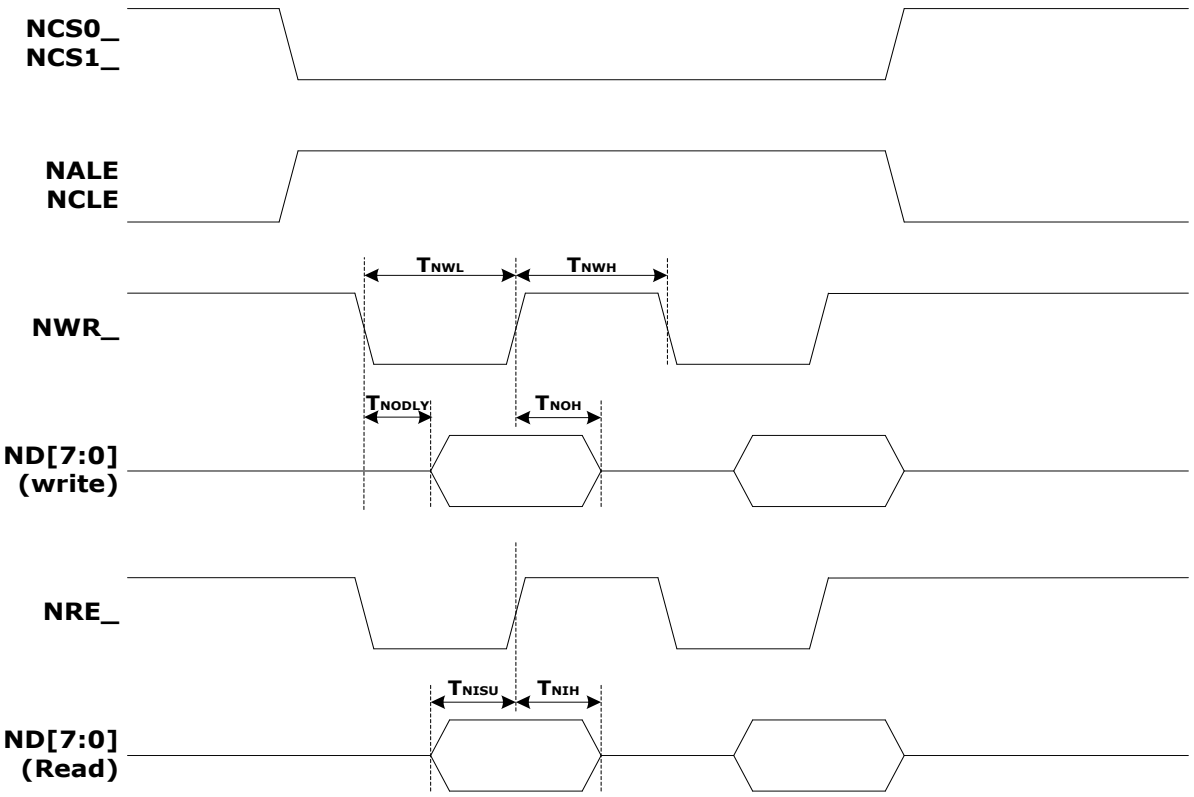
Note: Where PCLK is APB bus clock.

### 6.3.6 SPI Interface



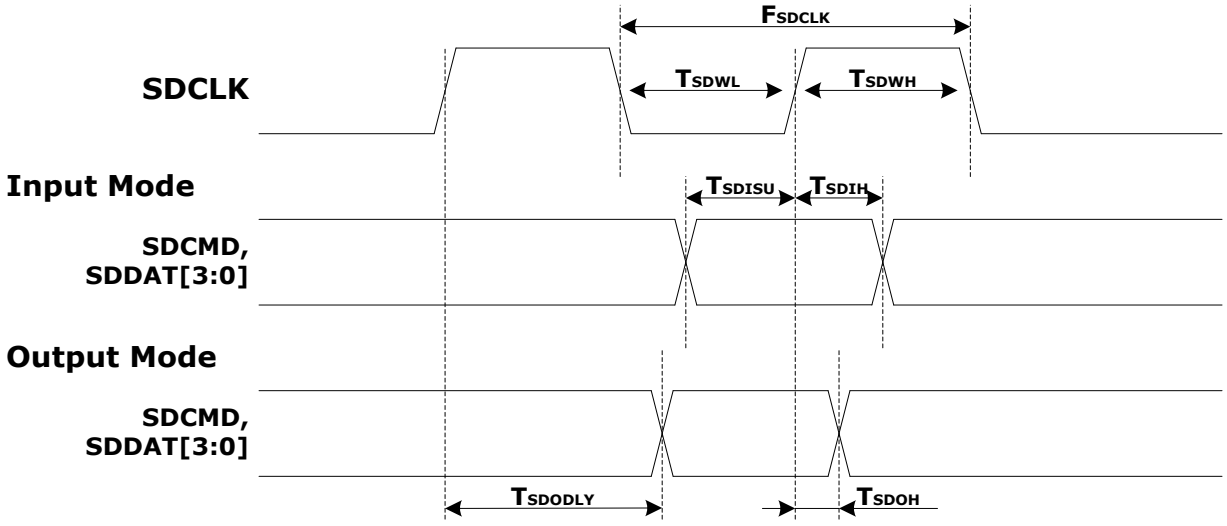

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $F_{SPCLK}$ | SPI0_CLK Clock Frequency | - | - | 25 | MHz |
| $T_{SPWL}$ | SPI0_CLK Clock Low Time | 20 | - | - | ns |
| $T_{SPWH}$ | SPI0_CLK Clock High Time | 20 | - | - | ns |
| $T_{SPISU}$ | SPI0_DI Setup Time | 10 | - | - | ns |
| $T_{SPIH}$ | SPI0_DI Hold Time | 10 | - | - | ns |
| $T_{SPODLY}$ | SPI0_DO Output Delay Time | - | - | 1 | ns |
| $T_{SPOH}$ | SPI0_DO Output Hold Time | 0.2 | - | - | ns |

### 6.3.7 NAND Interface




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $T_{NWL}$ | Write Pulse Low Width | 10 | - | - | ns |
| $T_{NWH}$ | NWR_ High Hold Time | 10 | - | - | ns |
| $T_{NODLY}$ | ND[7:0] Output Delay Time | - | - | 2.5 | ns |
| $T_{NOH}$ | ND[7:0] Output Hold Time | 10 | - | - | ns |
| $T_{NISU}$ | ND[7:0] Data in Setup Time | 3.2 | - | - | ns |
| $T_{NIH}$ | ND[7:0] Data in hold time | 1 | - | - | ns |

### 6.3.8 SD Card Interface




| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| **Clock SDCLK** | | | | | |
| $F_{SDCLK}$ | Clock Frequency in Data Transfer Mode | - | - | 24 | MHz |
| $F_{SDCLK}$ | Clock Frequency in Identification Mode | 100 | - | 400 | KHz |
| $T_{SDWL}$ | Clock Low Time | 10 | - | - | ns |
| $T_{SDWH}$ | Clock High Time | 10 | - | - | ns |
| **Input SDCMD, SDDAT[3:0] (referenced to SDCLK)** | | | | | |
| $T_{SDISU}$ | Input Setup Time | 6 | - | - | ns |
| $T_{SDIH}$ | Input Hold Time | 2 | - | - | ns |
| **Output SDCMD, SDDAT[3:0] (referenced to SDCLK)** | | | | | |
| $T_{SDODLY}$ | Output Delay Time | - | - | 14 | ns |
| $T_{SDOH}$ | Output Hold Time | 2.5 | - | - | ns |

### 6.3.9 USB PHY Specifications

#### *6.3.9.1 USB DC Electrical Characteristics*

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input high (driven) | | 2.0 | - | - | V |
| $V_{IL}$ | Input low | | - | - | 0.8 | V |
| $V_{DI}$ | Differential input sensitivity | \|PADP-PADM\| | 0.2 | - | - | V |
| $V_{CM}$ | Differential common-mode range | Includes VDI range | 0.8 | - | 2.5 | V |
| $V_{SE}$ | Single-ended receiver threshold | | 0.8 | - | 2.0 | V |
| | Receiver hysteresis | | - | 400 | - | mV |
| $V_{OL}$ | Output low (driven) | | 0 | - | 0.3 | V |
| $V_{OH}$ | Output high (driven) | | 2.8 | - | 3.6 | V |
| $V_{CRS}$ | Output signal cross voltage | | 1.3 | - | 2.0 | V |
| $R_{PU}$ | Pull-up resistor | | 1.425 | - | 1.575 | kΩ |
| $V_{TRM}$ | Pull-down resistor | | 14.25 | - | 15.75 | kΩ |
| $Z_{DRV}$ | Termination Voltage for upstream port pull up (RPU) | | 3.0 | - | 3.6 | V |
| $C_{IN}$ | Driver output resistance | Steady state drive* | 28 | - | 49.5 | Ω |
| $V_{IH}$ | Transceiver capacitance | Pin to $V_{SS}$ | - | - | 20 | pF |

Note: Driver output resistance does not include series resistor resistance.

#### *6.3.9.2 USB Full-Speed Driver Electrical Characteristics*

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{FR}$ | Rising time | CL = 50p | 4 | - | 20 | ns |
| $T_{FF}$ | Falling time | CL = 50p | 4 | - | 20 | ns |

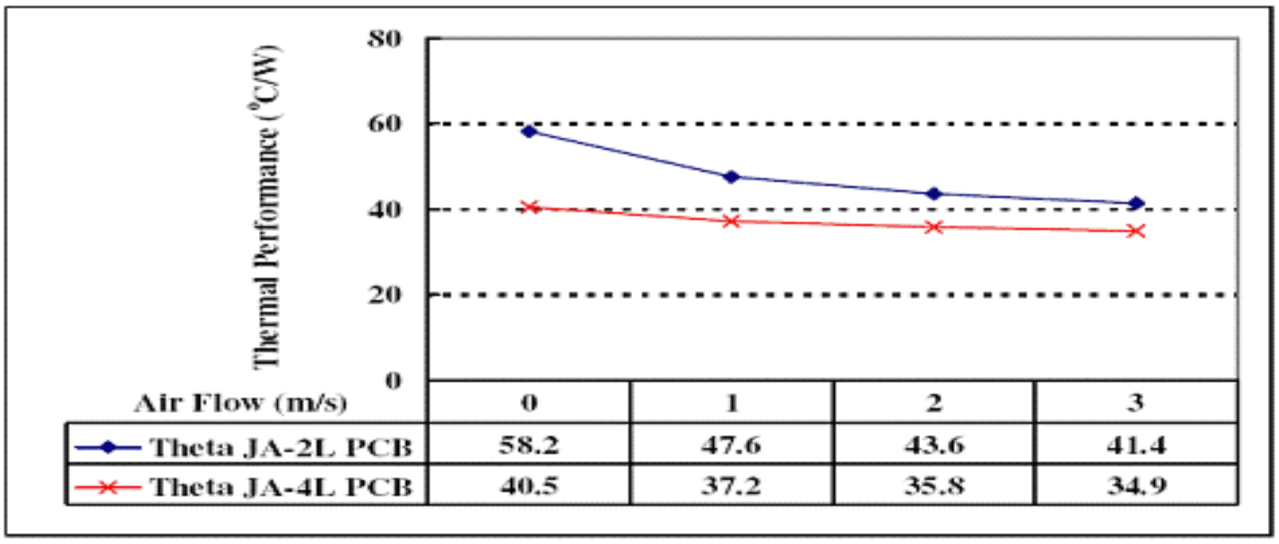
#### *6.3.9.3 USB High-Speed Driver Electrical Characteristics*

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{FR}$ | Rising time | CL = 5p | 500 | | | ps |
| $T_{FF}$ | Falling time | CL = 5p | 500 | | | ps |

### 6.3.10 Specification of Low Voltage Reset

| Parameter | Conditions | Min. | Typ | Max. | Unit |
|---|---|---|---|---|---|
| Operation voltage | -20℃ ~ +85℃ | 2 | 3.3 | 3.6 | V |
| LVR Detect Levels | VDD rises | 2.16 | 2.4 | 2.64 | V |
| | VDD falls | 2.115 | 2.35 | 2.585 | V |

## 6.4 Thermal Characteristics of N9H20



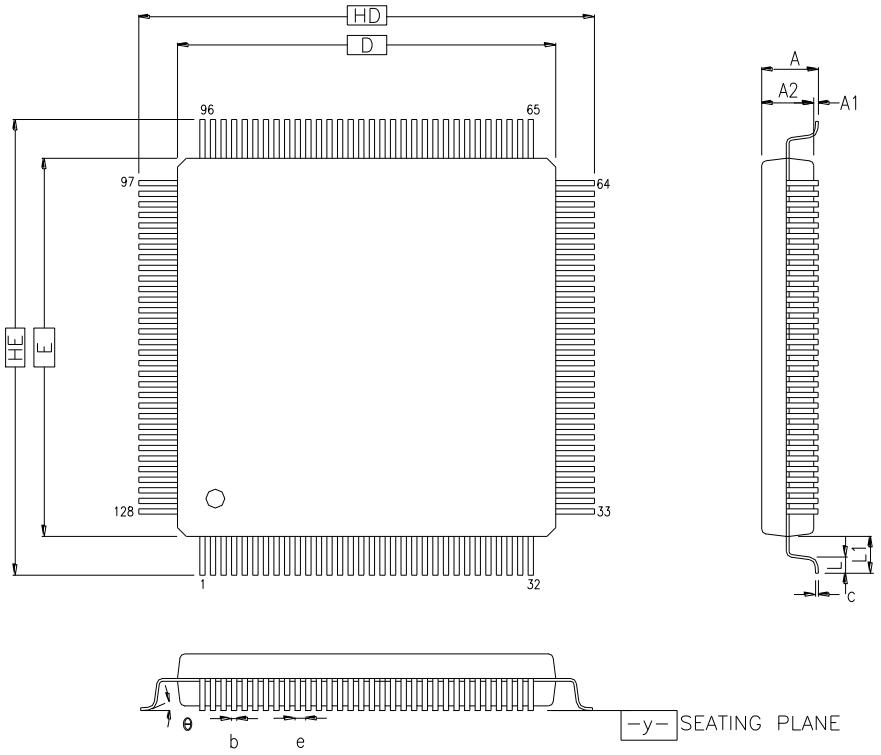

| Air Flow (m/s) | 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| Theta JA-2L PCB | 58.2 | 47.6 | 43.6 | 41.4 |
| Theta JA-4L PCB | 40.5 | 37.2 | 35.8 | 34.9 |

**Thermal Performance of LQFP-128 under Forced Convection**

# 7 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

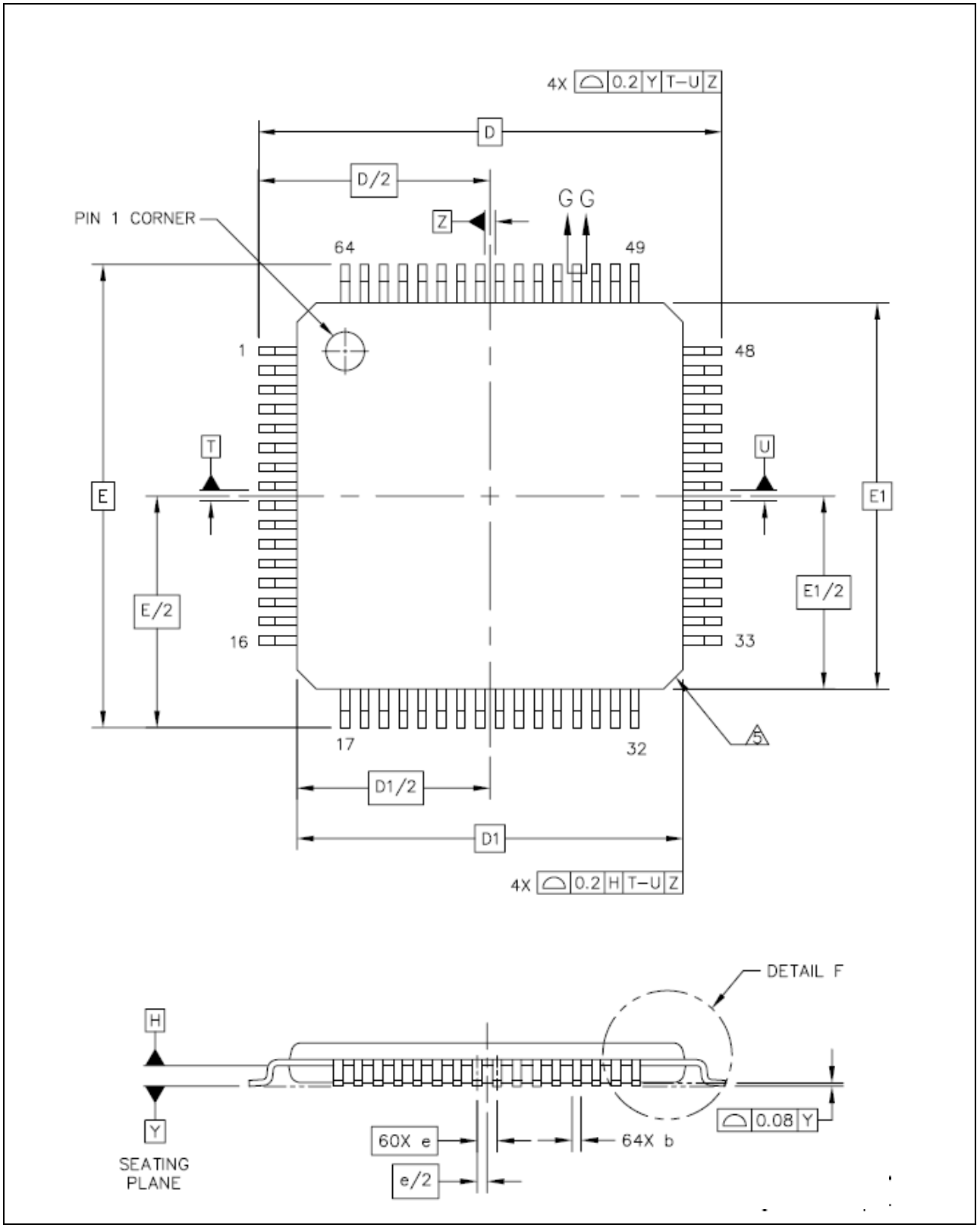
## 7.1 128L LQFP (14x14x1.4mm footprint)

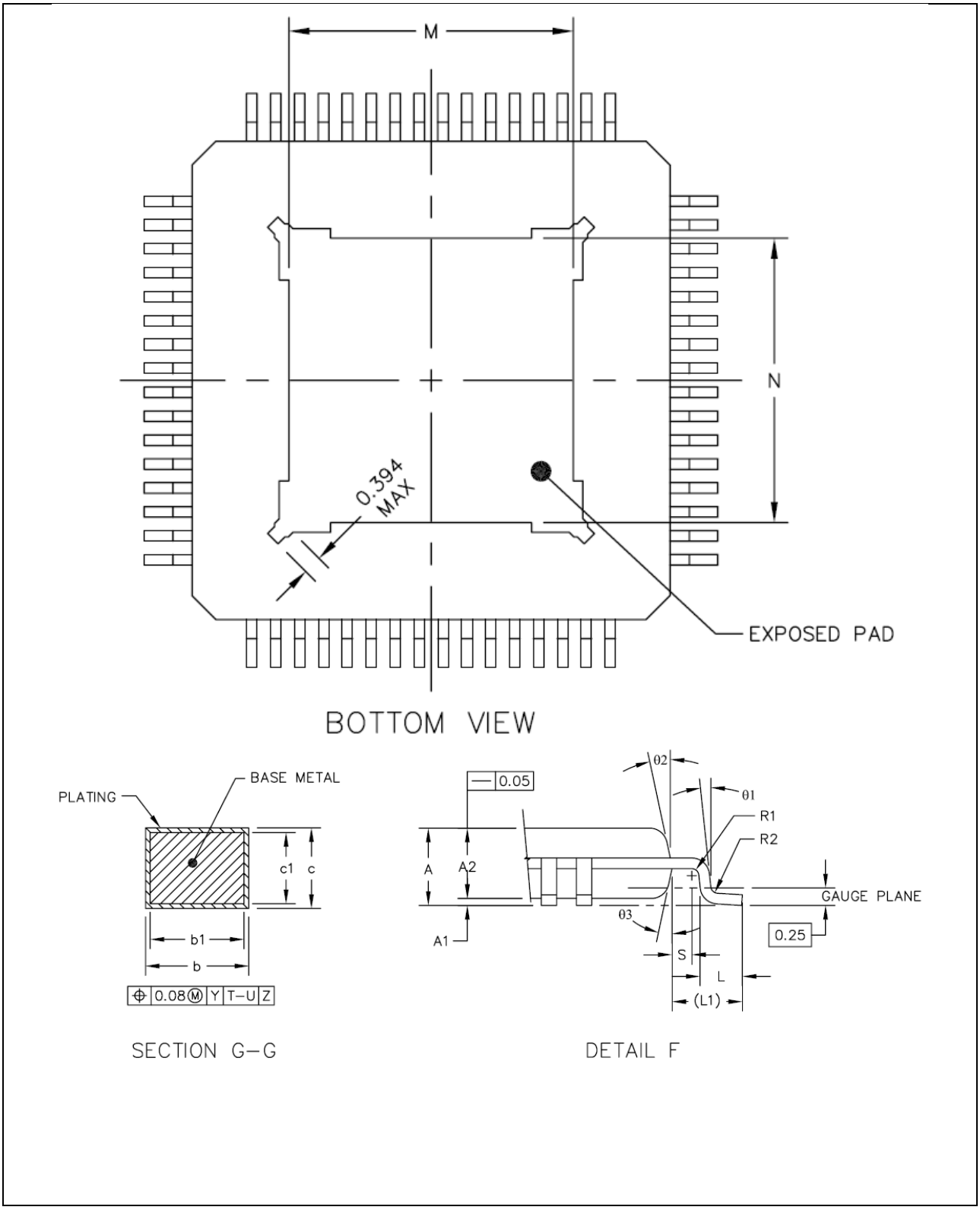



COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | | INCH | | |
|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | — | — | 1.60 | — | — | 0.063 |
| A1 | 0.05 | — | 0.15 | 0.002 | — | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| HD | 16.00 BSC. | | | 0.630 BSC. | | |
| D | 14.00 BSC. | | | 0.551 BSC. | | |
| HE | 16.00 BSC. | | | 0.630 BSC. | | |
| E | 14.00 BSC. | | | 0.551 BSC. | | |
| b | 0.13 | 0.16 | 0.23 | 0.005 | 0.006 | 0.009 |
| e | 0.40 BSC. | | | 0.016 BSC. | | |
| θ | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 | 0.004 | — | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| $L_1$ | 1.00 REF | | | 0.039 REF | | |
| y | – | – | 0.1 | – | – | 0.004 |

## 7.2 TQFP-64 EPAD (10X10X1.0mm footprint, 0.5mm pitch)




M
N
0.394
MAX
EXPOSED PAD
BOTTOM VIEW
PLATING
BASE METAL
c1
c
b1
b
0.08 M Y T-U Z
SECTION G–G
0.05
θ2
θ1
R1
R2
A
A2
A1
θ3
GAUGE PLANE
0.25
S
L
(L1)
DETAIL F

| DIM | MIN | | MAX |
|---|---|---|---|
| A | --- | | 1.2 |
| A1 | 0.05 | | 0.15 |
| A2 | 0.95 | 1 | 1.05 |
| b | 0.17 | 0.22 | 0.27 |
| b1 | 0.17 | 0.2 | 0.23 |
| c | 0.09 | | 0.2 |
| c1 | 0.09 | | 0.16 |
| D | | 12 BSC | |
| D1 | | 10 BSC | |
| e | | 0.5 BSC | |
| E | | 12 BSC | |
| E1 | | 10 BSC | |
| L | 0.45 | 0.6 | 0.75 |

| DIM | MIN | | MAX |
|---|---|---|---|
| L1 | | 1 REF | |
| R1 | 0.08 | | --- |
| R2 | 0.08 | | 0.2 |
| S | 0.2 | | --- |
| θ | 0° | 3.5° | 7° |
| θ1 | 0° | | --- |
| θ2 | 11° | 12° | 13° |
| θ3 | 11° | 12° | 13° |
| M | 5.85 | | 6.05 |
| N | 5.85 | | 6.05 |

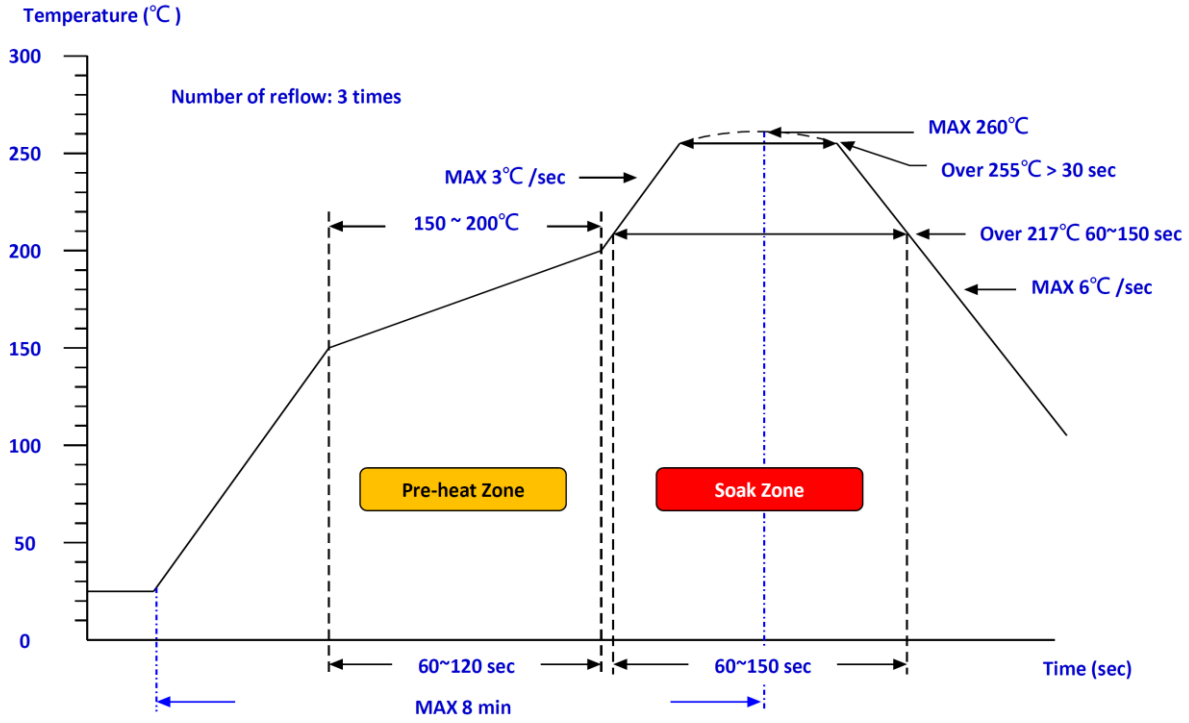
**UNIT: mm**

COTROL DIMENSIONS ARE IN MILLIMETERS.

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | — | — | 1.60 |
| $A_1$ | 0.05 | — | 0.15 |
| $A_2$ | 1.35 | 1.40 | 1.45 |
| HD | | 16.00 BSC. | |
| D | | 14.00 BSC. | |
| HE | | 16.00 BSC. | |
| E | | 14.00 BSC. | |
| b | 0.13 | 0.16 | 0.23 |
| e | | 0.40 BSC. | |
| θ | 0° | 3.5° | 7° |
| c | 0.09 | — | 0.20 |
| L | 0.45 | 0.60 | 0.75 |
| $L_1$ | | 1.00 REF | |
| y | – | – | 0.1 |

## 7.3 PCB Reflow Profile

### 7.3.1 Reflow Profile Suggestion for N9H20 series (Pb Free & Halogen Free)



# 8 REVISION HISTORY

| Date | Revision | Description |
|---|---|---|
| 2018, 05, 16 | 1.00 | • Preliminary version. |
| 2018, 10, 11 | 1.10 | • Added part no., N9H20R11N at section 3.2 |
| 2020, 03, 24 | 1.20 | • Removed UART0_CTS and UART0_RTS flow control function in the chapter 2 and the chapter 3. |
| 2020, 06, 29 | 1.21 | • Added CPU_CLK@240MHz condition at section 6.2.1. |
| 2020, 11, 11 | 1.22 | • Revised Timer channel amount at section 5.16. |
| 2021, 04, 12 | 1.23 | • Added DRAM type information at section 3.2. |
| 2021, 08, 26 | 1.24 | • Revised LPCLK max. frequency value at section 6.3.5 |
| 2021, 11, 18 | 1.25 | • Revised PCB relflow profile at section 7.3 |
| 2022, 03, 14 | 1.26 | • Revised CFG[0] I/O type at section 3.4. |
| 2024, 08, 12 | 1.27 | • Revised ADC number in section 3.2<br>• Added “Package is Halogen-free, RoHS-compliant and TSCA-compliant.” In Chapter 2 and 7. |
| 2026, 08, 06 | 1.28 | • Added part no., N9H20K63N at section 3.2 |
| 2026, 09, 10 | 1.29 | • Revised pin diagram in section 3.3.1 and 3.3.2 |

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