NuMicro® Family

Arm® Cortex®-M55-based Microcontroller

M55M1 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro M55M1 series is a new generation AI microcontroller, which delivers up to 110 GOPS of AI computing power, specifically designed for Endpoint AI such as data recognition and intelligent audio. The M55M1 is a 32-bit microcontroller based on a 220 MHz Arm Cortex-M55 core, featuring an Arm Ethos™-U55 Neural Processing Unit (NPU) as a coprocessor to accelerate neural network operations. In addition to its outstanding AI performance, the M55M1 also includes DSP extensions, vector extensions (Helium), double-precision FPU, two 16-ch PDMA controllers and one 2-ch GDMA controller, making it an ideal choice for embedded applications—especially those requiring intensive computation such as audio processing, communications, digital signal processing, machine learning and sensor fusion.

Flexible Memory & Expansion Options

The M55M1 series is equipped with up to 1.5 MB of on-chip RAM and 2 MB of Flash memory, and features OctoSPI and HyperBus interfaces to support the expansion of RAM and Flash memory capacity. The M55M1 supports a low supply voltage range from 1.71V to 3.6V and operates within a temperature range of -40°C to +105°C.

Energy-Saving Design & Robust Security

For power consumption and security, the M55M1 offers five low-power modes and supports a variety of peripherals, including CCAP, DMIC, I²C, SPI, Timer, UART, ADC, and GPIO that can continue to operate in low-power mode. In addition, the M55M1 features multi-level security mechanisms, including secure boot, TrustZone, TRNG, key storage, crypto accelerators, tamper detection, and PSA Level 2 compliance, providing reliable protection for IoT and embedded applications.

Rich High-Speed Communication Interfaces

The M55M1 series also offers a rich set of communication and peripheral interfaces, including 10/100 Ethernet MAC with RMII, 1 set of USB High-Speed OTG with PD (Power Delivery) function and supporting USB Type-C connector, 1 set of USB Full-Speed OTG, 2 sets of CAN FD, 1 set of I3C, 4 sets of I²C, 2 sets of QSPI, 4 sets of SPI/I²S, 2 sets of I²S, 10 sets of UART, 2 sets of SDIO, 8-bit camera capture interface (CCAP), and digital microphone input (DMIC).

Comprehensive Analog and Precision Control

In terms of analog and control features, the M55M1 series implements 2 sets of 12-bit 5 Msps SAR ADCs, 2 sets of 12-bit 1 Msps buffered DACs, 4 sets of analog comparators, up to 24-channel 200 MHz PWM outputs, 4 sets of QEI, and 4 sets of input capture units.

Flexible IDE Compatibility and Debugging Tools

For development tool support, Nuvoton provides the NuMaker-X-M55M1D evaluation board and the Nu-Link debugger tool. In addition, it supports commonly used development environments such as Keil MDK, IAR EWARM, and Eclipse IDE with GNU GCC.

Line	UART	I²C	I3C	SPI	QSPI	USCI	I²S	PWM	ADC	DAC	ACMP
M55M1	10 + 5	4 + 2	1	4 + 2	2	1	2 + 4	24-ch	48-ch	2	4
	CAN FD	FS USB	HS USB	Ethernet	PSIO	SDIO	Smart Card	DMIC	CCAP	QEI	PDMA
	2	1	1	1	8-ch	2	3	4-ch	1	4	32-ch

Table 2.1-1 M55M1 Series Key Features Support Table

The M55M1 series microcontroller benefits design of a wide range of applications such as:

- Human presence detection
- Robotics
- Smart toys

- Sensor Hub
- Smart appliances
- PC Accessories
- AIoT

2 FEATURES

2.1 M55M1 Series Features

Core and System	
Arm Cortex-M55	• Arm Cortex-M55 processor, running up to 220 MHz • Supports Arm TrustZone Technology • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Built-in Embedded Trace Macrocell (ETM) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions • Supports L1 cache – 16KB I-cache and 16KB D-cache • Supports TCM – 64KB I-TCM and 128KB D-TCM • Supports 10-cycle sine/consine calculation custom instruction
Arm Ethos®-U55 (NPU)	• Arm Ethos®-U55 micro-neural processing unit, running up to 220 MHz • Supports 8-bit and 16-bit integer operation – Activations: 16-bit signed integers – Weights: 8-bit signed integers • Implements 256 MACs • Supports Performance Monitoring Unit • Support neural network model protection
Secure Configuration Unit (SCU)	• Configures SRAM's security and privilege attribution block by block • Configures GPIOs'security and privilege attribution port by port • Configures peripherals" security and privilege attribution • Generates secure violation interrupt • Equipped with a 24-bit timer as a non-secure state monitor • Monotonic firmware version counter • Debug protection mechanism • Product life-cycle management
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option

Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Boot Loader	• Factory pre-loaded mask ROM for secure boot procedure and ISP procedure • Use SHA-256 and ECDSA-P256/RSA-2048/RSA-3072/Ed25519 to validate signed image data in APROM and LDROM • NuTool-Boot Loader ISP Tool for firmware upgrade via UART, CAN, SPI, I^2C and high speed USB device
Flash Memory	• Up to 2048 Kbytes on-chip Application ROM (APROM) • Supports dual bank for Over-The-Air (OTA) upgrade • Four eXecute-Only-Memory (XOM) regions for code protection • 8 Kbytes on-chip Flash for user-defined loader (LDROM) • 3 Kbytes One Time Programmable (OTP) ROM for data security • All on-chip Flash support 8 Kbytes page erase • Fast Flash programming verification with CRC32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• On-chip SRAM includes: – 512 Kbytes SRAM bank0 – 512 Kbytes SRAM bank1 – 320 Kbytes SRAM bank2 – 8 Kbytes SRAM bank3 – 8 Kbytes SRAM in low power domain – 64 Kbytes ITCM – 128 Kbytes DTCM • Supports byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports 8-bits, 16-bits and 32-bits configurable polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials included • Programmable initial value

	• Supports order reverse setting and one's complement setting for input data and CRC checksum • Supports 8-bit, 16-bit, and 32-bit data width • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Up to 16 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Supports Fixed-priority and Round-robin priority modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Graphic DMA (GDMA)	• 2 parallel DMA channels each with 16 depth FIFO • 1D memory copy including increments • Interrupt capability for each channel and global events • Flexible command linking capability • Extended memory copy capabilities: 2D/wrap/template (support in Channel 0) • Presence of Security Extension for TrustZone support
Clocks	
External Clock Source	• 4~32 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC48M) • 1~8 MHz High-speed Internal RC oscillator (MIRC) • 12 MHz High-speed Internal RC oscillator (HIRC) trimmed to 2% accuracy that can optionally be used as a system clock • 32 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Two programmable APLL output clock frequency (APLLFOUT), APLL source can be selected from external 4~24 MHz external high speed crystal (HXT), external 24~32 MHz external high speed crystal divide 2 (HXT/2), 12 MHz internal high speed oscillator (HIRC) or 48 MHz internal high speed oscillator divide 4 (HIRC48M/4)
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain and independent V_{BAT} pin

	• Supports 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports frequency compensation of RTC clock source • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Tick Timer Controller (TTMR)	• Two sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic and Continuous Counting operation modes • Supports time-out interrupt signal to trigger LPADC, DAC0, LPI2C, LPSPI, LPUART, CCAP Motion detector and LPPDMA function
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels

	• Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Trigger EADC/LPADC/DAC to start conversion immediately • Supports External Pin Trigger Function
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 20-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection) and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One set of 12-bit, 24-ch 5 Msps SAR EADC with up to 24 single-ended input channels or 12 differential input pairs; 10-bit accuracy is guaranteed • Four internal channels for $AV_{DD}/4$, $V_{BAT}/4$, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage • Supports Power-down mode • Supports calibration capability • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse or EPWM/BPWM • Configurable EADC sampling time • Up to 28 sample modules

	• Double data buffers for sample module 0~3 • PDMA operation • Supports Averageing mode and Oversampling mode, where Oversampling mode provides up to 16-bit precision
Digital-to-Analog Converter (DAC)	• Up to two sets of 12-bit, 1 Msps voltage type DAC with 12- or 8-bit mode • Maximum output voltage AV_{DD} -0.2V in buffer mode • Conversion can be triggered by software, Timer0~3, EPWM, external pin • Supports group mode for synchronized data update of two DACs • PDMA operation
Analog Comparator (ACMP)	• Up to four rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, DAC, and 64-level Voltage divider from AV_{DD} at negative input • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for EPWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 20mV and 40mV • Supports offset calibration
Communication Interfaces	
UART	• Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports PDMA operation • Supports Single-wire function mode

Smart Card Interface	Up to three sets of Smart Card interfaces • ISO-7816-3 compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 267 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I²C	• Up to four sets of I²C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation • Supports pin swap function • Supports setup/hold time programmable • Supports two level buffer mode
I3C Serial Interface Controller (I3C)	• Supports Master and Slave mode • Static or Dynamic Slave Device support • Built-in Hardware Dynamic Address Allocation support (ENTDAA/SETDASA) • Built-in CCC transfer handler • Auto Hot-Join request generation support • In-Band Interrupt request generation support • Adaptive mode of operation between I2C and I3C depending on I3C bus traffic • Built-in S0-S5 Error Handling • Supports Power-down wake-up function • Supports PDMA mode for data transfer • Supports SDR mode, data rates up to 12.5 Mbps • Supports HDR-DDR mode, data rates up to 25 Mbps
SPI Flash/HyperBus	• Supports SPI Flash with maximum 32 Mbytes size

Controller (SPIM)	• Support 8 Kbytes cache memory • Supports HyperBus device with maximum 32 Mbytes size • Supports SPI master mode and HyperBus host mode • Supports Direct Memory Mapping Mode, Normal I/O Mode, DMA Read Mode, and DMA Write mode • Supports transaction with data width 8/16/24/32 bits for Normal I/O mode • Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer • Supports standard (1-bit), dual (2-bit), quad (4-bit), and octal (8-bit) I/O transfer mode • Supports Single Transfer Rate (STR) mode and Double Transfer Rate (DTR) mode • Supports AES OTFC (On-The-Fly Cipher) encryption/decryption • One slave/device select line for storage component of SPI Flash and HyperBus device • Supports read DQS data strobe from SPI Flash and HyperBus device to sample RX data from SPI Flash and HyperBus device
Quad SPI	• Up to two sets of Quad SPI with Master/Slave mode • Master mode up to 100 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7V~3.6V) • Supports Dual and Quad I/O Transfer mode • Supports one data channel half-duplex transfer • Supports double data rate mode (Master TX DIR Mode Only) • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation
SPI/I²S	• Up to four sets of SPI/I²S controllers with Master/Slave mode • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Master mode up to 100 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7~3.6V) • Configurable bit length of a transfer word from 4 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function

	• Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
I²S	• Up to two sets of I²S interfaces with Master/Slave mode • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Digital Microphone Inputs (DMIC)	• Provides one 32-level FIFO data buffers for receiving • Generates interrupt requests when buffer levels cross a programmable boundary • Supports LPPDMA transfer • Supports up to four channel digital microphones • Four digital PDM microphone inputs can be used simultaneously • Supports High Pass Filter (HPF) to removed DC offset from digital microphone • Supports volume gain (+36dB~-128dB) 0.125dB step setting with zero cross gain change • Supports microphone operates at clock frequency between 1 MHz and 6 MHz • VAD (Voice Active Detection) generates interrupt requests when voice detected • Supports Power-down mode VAD wake-up function
Universal Serial Control Interface (USCI)	• Configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and programmable

	flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports wake-up function • PDMA operation **SPI** • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function: input slave select transition • Supports one data channel half-duplex transfer • PDMA operation **I²C** • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data payload • Communication in standard mode (100 kbps) and fast mode (up to 400 kbps) • Supports 10-bit mode • Supports 10-bit bus time out capability • Supports bus monitor mode • Supports Power down wake-up by START signal or address match • Supports multiple address recognition • Programmable setup/hold time
Controller Area Network with Feasibility Data Rate (CAN FD)	• Up to two sets of CAN FD controllers • Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015 • Compliant with CAN FD version 1.0 with up to 64 data bytes supported • Supports CAN Error logging, AUTOSAR and SAE J1938 • Built-in Message SRAM for each CAN FD controller
Secure Digital Host Controller (SDHC)	• Compliant with SD Memory Card Specification Version 2.0 • Supports 50 MHz to achieve 200 Mbps at 3.3V operation • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC card

External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter • Supports dedicated external chip select pin with polarity control and up to 1 Mbytes addressing space for each bank • 8-/16-bit data width • Supports byte write in 16-bit data width mode • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode • Supports LCD interface i80 mode • PDMA operation
Programmable Serial I/O (PSIO)	• Supports up to 8 PSIO pins • Supports 7 clock sources with clock divider • Supports 4 slot controllers for timing sequence control • Supports 8 check points to connect with slots in each pin • Supports 8 check point actions in each check point • Supports four I/O modes, input, output, open-drain, and quasi • Supports switch I/O mode in different check points • Supports four kinds of Interrupt trigger conditions • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O (Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PC.9 ~ 13; PD.10 ~ 12; PE.15; PF.2 ~ 5; PI.0 ~ 5; All USB High Speed PIN and nRESET PIN.)
KeyPad Interface (KPI)	• Matrix keypad interface with up to 6x8 array • Programmable de-bounce time • Generates interrupt and update press/release status of all keys once key press or release detected
Low Power peripheral	
Low Power General Purpose I/O (LPGPIO)	• Supports function operating in NPD0/1/3 • Two I/O modes:

	– Push-Pull Output mode – Input only with high impendence mode • Supports pin output data individual bit set/reset
Low Power LPPDMA Controller (LPPDMA)	• Supports 4 independently configurable channels • Supports selectable 2 level of priority (fixed priority or round-robin priority) • Supports transfer data width of 8, 16, and 32 bits • Supports source and destination address increment size can be byte, half-word, word or no increment • Supports software and LPUART, LPSPI, LPI2C, LPTMR, TTMR, DMIC and LPADC request • Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table • Supports single and burst transfer type
Low Power Timer Controller (LPTMR)	**TIMER** • Two sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Supports 16-bit PWM counters with 8-bit clock prescale • Up PWM counter type • Supports tri-state output for each PWM channel
Low-power UART	• Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit

	FIFO overflow detection function • Supports LPPDMA operation
Low Power Serial Peripheral Interface (LPSPI)	• Master mode up to 100 MHz (V_{DD} = 2.7V ~ 3.6V) • Master/Slave mode up to 50/25 MHz (when chip works at V_{DD} = 2.7~3.6V) • Configurable bit length of a transfer word from 4 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode
Low Power I^2C Serial Interface Controller (LPI2C)	• One set of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) when clock source is over 20 MHz • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports multi-address power-down wake-up function • LPPDMA operation • Supports pin swap function • Supports setup/hold time programmable
Low Power Analog-to-Digital Converter (LPADC)	• One set of 12-bit, 24-ch 2 Msps SAR ADC with up to 24 single-ended input channels or 12 differential input pairs; 10-bit accuracy is guaranteed • Four internal channels for AV_{DD}/4, V_{BAT}/4, band-gap VBG input and Temperature sensor input • Four operation modes: single mode, bust mode, single-cycle scan mode and continuous scan mode • Supports external V_{REF} pin or internal reference voltage • Supports Power-down mode • Supports calibration capability • Conversion can be triggered by software, external pin or EPWM/BPWM • Supports auto-operation mode with A/D conversion can be started by Low power Timer 0/1, Low power Tick Timer 0/1, Wakeup I/O and ACMP interrupt event • Supports extend sample time function (0~16383 LPADC clock) • LPPDMA operation • Supports Floating Detect Function
Awake Filter (AWF)	• Present as memory in system • Supports configurable threshold conditions(high threshold and low

	threshold) • Supports 8-word buffer
Control Interfaces	
Enhanced Quadrature Encoder Interface (EQEI)	• Two EQEI phase inputs (EQEI_A, EQEI_B) and one Index input (EQEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode • Supports swap function for input signals (EQEI_A, EQEI_B) • Supports for detecting the occurrence of phase error • Supports one times index signal reset function
Enhanced Capture (ECAP)	• Up to four sets of enhanced input capture units • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 2.0 Full Speed Host Controller** • Compliant with USB Revision 2.0 Full-speed Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Supports port power control and port overcurrent detection • Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Full-Speed Specification

	• Supports suspend function when no bus activity exists for 3 ms • 25 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1.5 Kbytes configurable RAM for endpoint buffer • Remote wake-up capability • Start of Frame (SOF) locked clock pulse generation for crystal-less feature • USB 2.0 link power management • Supports double buffer function
USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed OTG (On-The-Go)** • On-chip USB 2.0 high speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0 • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Built-in DMA **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports 18 configurable endpoints in addition to Control Endpoint • Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction • Maximum packet size up to 1024 bytes • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode • Suspend, resume and remote wake-up capability • Built-in DMA • Supports Battery Charging 1.2 (BC1.2)
USB Type C Power Delivery Controller (UTCPD)	• Compliant with USB Type-C Cable and Connector Specification Rev1.2 (TYPE-C) • Supports UFP, DFP and DRD data roles • Supports Sink, Source and DRP power roles • Dual-Role Power functionality with Autonomous DRP toggle

	• Supports CC1 and CC2 signals • Compliant with USB Power Delivery Specification Rev3.0, V1.2 (PD) • Supports Power Delivery PHY Layer • Supports Power Delivery Protocol Layer
Ethernet MAC	• Compliant with IEEE Std 802.3-2008 for Ethernet MAC • Compliant with IEEE Std 1588-2008 for precision networked clock synchronization. • Compliant with RMII specification version 1.2 from RMII consortium • Full-duplex operation – IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion – Forwarding of received Pause frames to the user application • Half-duplex operation – CSMA/CD Protocol support – Flow control using backpressure support • Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size • IEEE 802.1Q VLAN tag detection for reception frames • Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1) • Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2) • CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control • Serial management interface (MDC/MDIO) master mode for PHY device configuration and management
Digital Camera Interface	
Camera Capture Interface (CCAP)	• Supports CCIR601, CCIR656 and 8-bit/4-bit interfaces for CMOS sensor • Color format for data input supports YUV4:2:2 and RGB565 and RGB888 • Color format for data output supports YUV4:2:2, RGB565, RGB555, RGB888, ARGB8888 and Y-only • Supports 1-bit Y(luminance) output with 8-bit threshold setting for 2-level image thresholding • Supports the CROP function to crop input image to the required size for digital application • Supports image scaling-down • Supports motion detection engine with 320x240 image data in Power-down mode

	• Supports chip wake-up from Power-down mode if a motion detection interrupt signal is generated.
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports 163-bit ~ 571-bit key length • Supports both prime field GF(p) and binary field GF(2m) • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p) • Supports Curve25519 • Improved side-channel attack protection
Rivest–Shamir–Adleman Cryptography (RSA)	• Supports both encryption and decryption with up to 4096 bits • CRT decryption with up to 4096 bits • Improved side-channel attack protection ability
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197 • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum • Supports CCM mode, GCM mode and GMAC function • Improved side-channel attack protection ability
Secure Hash Algorithm (SHA)	• Hardware SHA accelerator • Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and and SHA-512/t • Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256 • Compliant with FIPS 180/180-2
keyed-Hash Message Authentication Code (HMAC)	• Hardware HMAC accelerator • Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512 • Supports HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512 • Compliant with FIPS 180/180-2

Pseudo Random Number Generator (PRNG)	• Hardware PRNG accelerator • Supports take seed from TRNG
True Random Number Generator (TRNG)	• Up to 10Mbit/s data rate for entropy source • Pass NIST SP800-22A standard • Includes NIST SP800-90A known answer test for DRBG and NIST SP800-90B health test for entropy source (Start-up test, Repetition count test, Adaptive proportion test). • Provides the true random number seed for PRNG
Keystore	• Supports programming interface for key management • Supports multiple key size from 128 bits to 4096 bits • Supports 32 SRAM keys, 32 Flash keys and 16 OTP keys at most • Supports crypto engine access key in keystore directly • Supports ECDH operation with ECC and PRNG engine • Supports to store middle data for RSA CRT and SCAP mode • Supports revoke operation for each key • Supports auto verify function • Supports lock function for OTP keys • Supports data remanence prevention at SRAM
Key Derivation Function (KDF)	• Supports IETF Protocols RFC 5869 • Supports NIST SP 800-108 feedback mode • Supports 65280-bit output key at most • KDF output size is 256 bits; supports up to 255 expansions to reach 65280-bit output key • Supports output key stored in KeyStore • Supports input keying material from NVM • Supports key information and salt from random value
On-The-Fly Cipher (OTFC)	• Supports both on-the-fly encryption and on-the-fly decryption for external memory controller • Supports four 128-bit alignment protection regions in external memory • Supports address cipher function • Supports AES encryption with 128-bits key • Supports AES 128-bits key from key store • Supports one technique to improve side-channel attack protection (SCAP) ability • Supports two techniques to improve differential fault analysis protection (DFAP) ability

3 PARTS INFORMATION

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1 M55M1 Series Package Type

Part No.	LQFP64 (10x10mm)	LQFP128 (14x14mm)	LQFP176 (24x24mm)
M55M1	M55M1R2LJAE	M55M1K2LJAE	M55M1H2LJAE

3.2 M55M1 Series Naming Rule

M55	M1	H2	L	J	A	E
Core	**Line**	**Package**	**Flash Memory**	**SRAM**	**Reserve**	**Temperature**
Cortex-M55	M1: Machine Learning	H2: LQFP176 (24 mm x 24 mm) K2: LQFP128 (14 mm x 14 mm) R2: LQFP64 (10 mm x 10 mm)	L: 2 MB	J: 1.5 MB N: 9.5 MB	A: Reserved	E: -40˚C to +105˚C

3.3 M55M1 Series Selection Guide

Part Number		M55M1H2LJAE	M55M1K2LJAE	M55M1R2LJAE
System Frequency (MHz)		220	220	220
Ethos-U55 Neural Processing Unit		√	√	√
APROM Flash (KB)		2,048	2,048	2,048
RAM (KB)		1,552	1,552	1,552
LDROM (KB)		8	8	8
PDMA (up to 32-ch)		2	2	2
GDMA (2-ch)		1	1	1
LPPDMA (4-ch)		1	1	1
Secure Boot		√	√	√
Crypto Accelerator		Up to AES-256, ECC-571, RSA-4096, SHA-512, and HMAC-512, PRNG	Up to AES-256, ECC-571, RSA-4096, SHA-512, and HMAC-512, PRNG	Up to AES-256, ECC-571, RSA-4096, SHA-512, and HMAC-512, PRNG
Key Store		√	√	√
Key Derivation Function		√	√	√
XOM		√	√	√
TRNG		√	√	√
Timer (32-bit)		4	4	4
Watchdog Timer		2	2	2
Window Watchdog Timer		2	2	2
Connectivity	CCAP	1	1	1
	DMIC (4-ch)	1	1	1
	USCI	1	1	1
	PSIO (8-ch)	1	1	1
	UART	10	10	9
	SPI/I^2S	4	4	4
	QSPI	2	2	1
	I^2S	2	2	2
	I^2C	4	4	3
	I3C	1	1	1
	USB FS	1	1	-
	USB HS	1	1	1

	CAN FD	2	2	2
	SDIO	2	2	2
	ISO-7816-3	3	3	3
	LPUART	1	1	1
	LPI2C	1	1	1
	LPSPI	1	1	1
	Ethernet 10/100 MAC	1	1	1
SPIM		1	1	-
EBI		1	-	-
EPWM (up to 12-ch)		2	2	2
BPWM (up to 12-ch)		2	2	2
EQEI		4	4	4
ECAP		4	2	1
12-bit EADC		1 (up to 24-ch)	1 (up to 24-ch)	1 (up to 18-ch)
12-bit LPADC		1 (up to 24-ch)	1 (up to 24-ch)	1 (up to 18-ch)
12-bit DAC		2	2	2
Analog Comparator (ACMP)		4	4	4
RTC (V_{BAT})		1	1	1
GPIO		142	97	39
Package		LQFP176	LQFP128	LQFP64

4 PIN CONFIGURATION

Users can find pin configuration information in the M55M1 Series Pin Diagram Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M55M1 Series Pin Diagram

4.1.1.1 LQFP64-Pin Diagram

Corresponding Part Number: M55M1R2LJAE

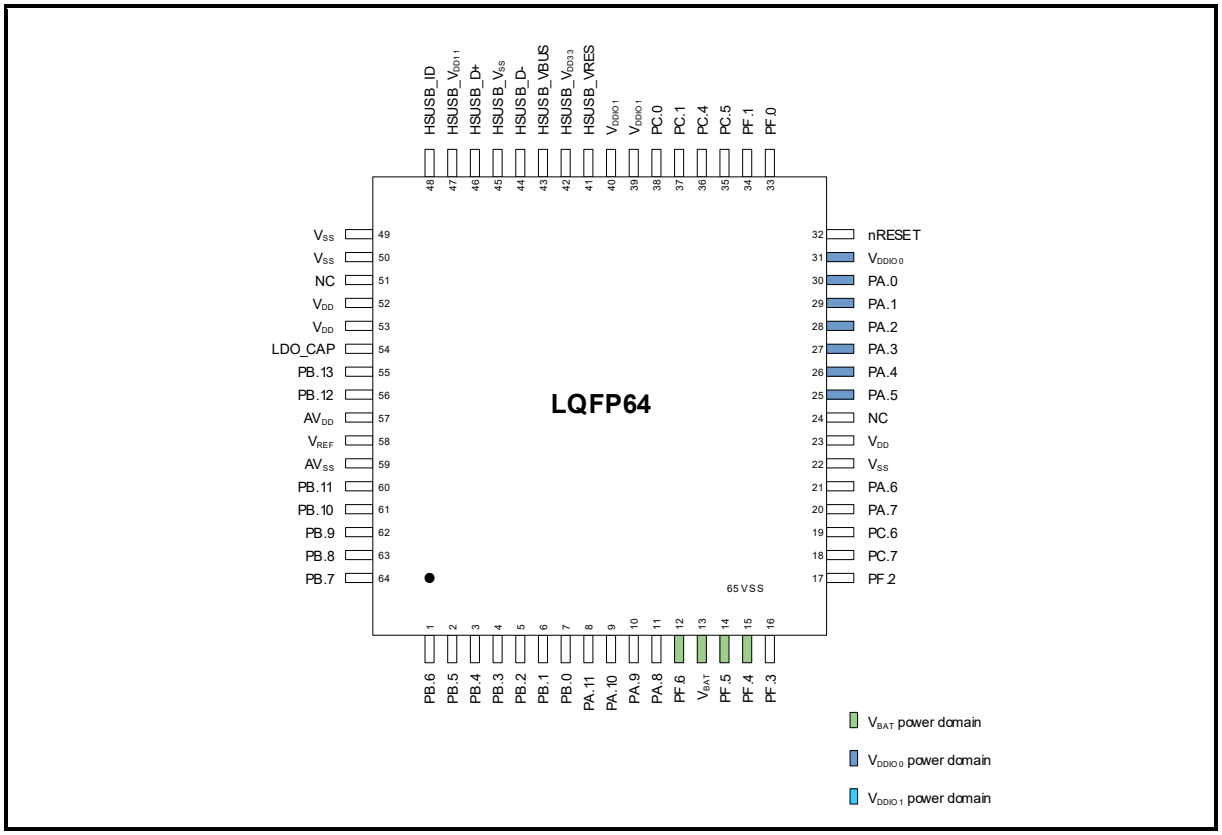


Figure 4.1-1 LQFP64-Pin Diagram

4.1.1.2 LQFP128-Pin Diagram

Corresponding Part Number: M55M1K2LJAE

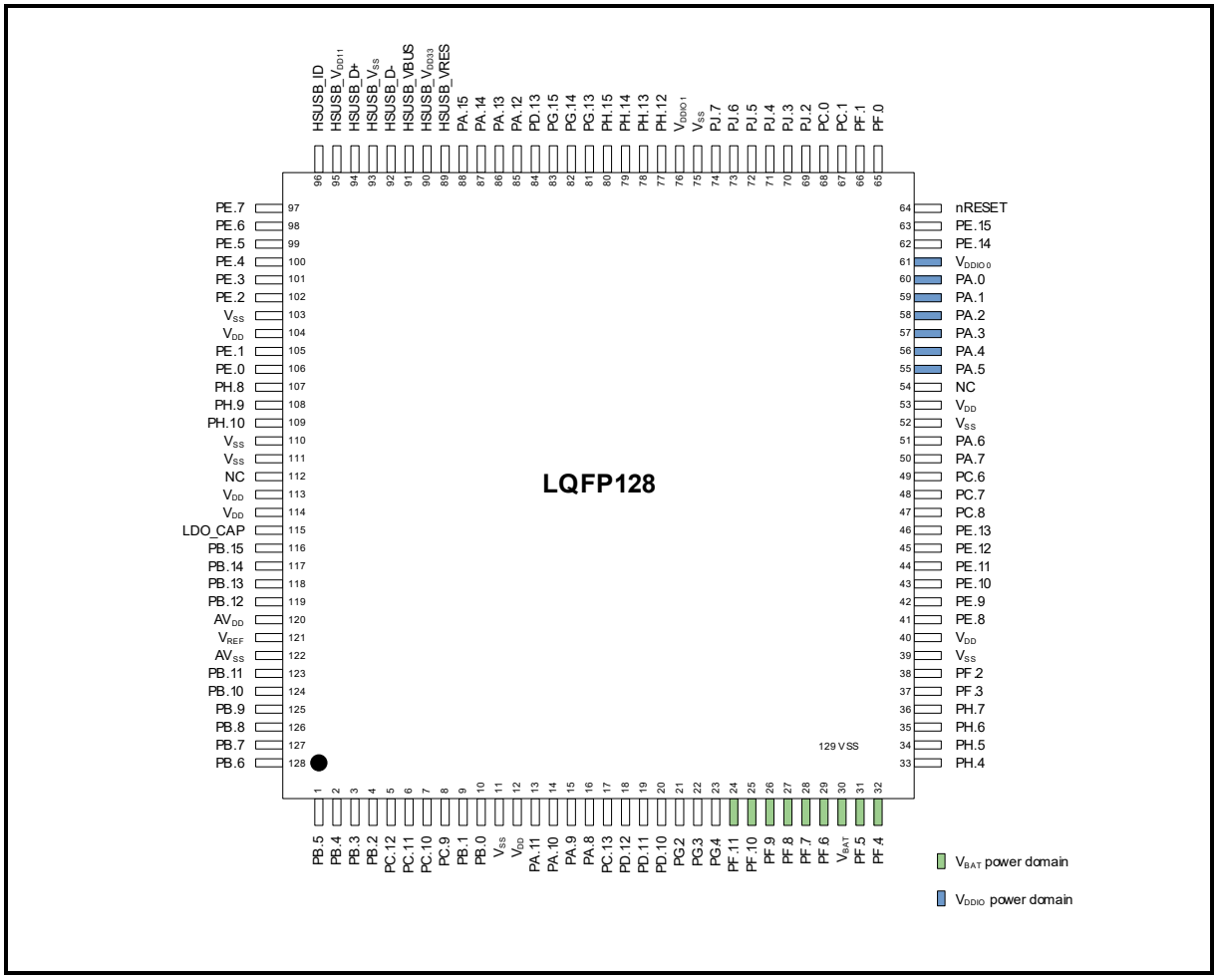


Figure 4.1-2 M55M1K2LJAE LQFP128-Pin Diagram

4.1.1.3 LQFP176-Pin Diagram

Corresponding Part Number: M55M1H2LJAE

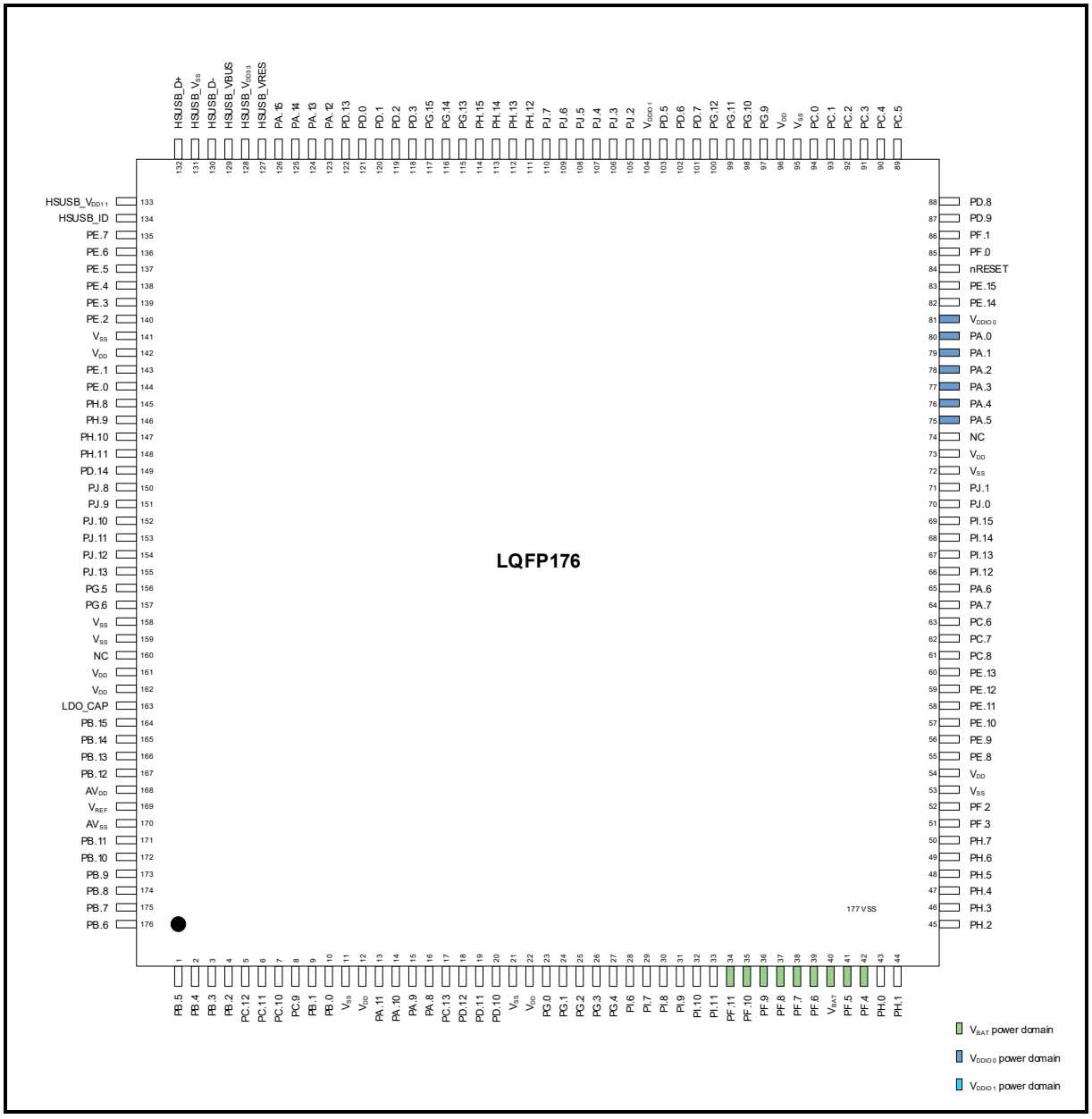


Figure 4.1-3 M55M1H2LJAE LQFP176-Pin Diagram

4.1.2 M55M1 Series Multi-function Pin Diagram

4.1.2.1 LQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M55M1R2LJAE

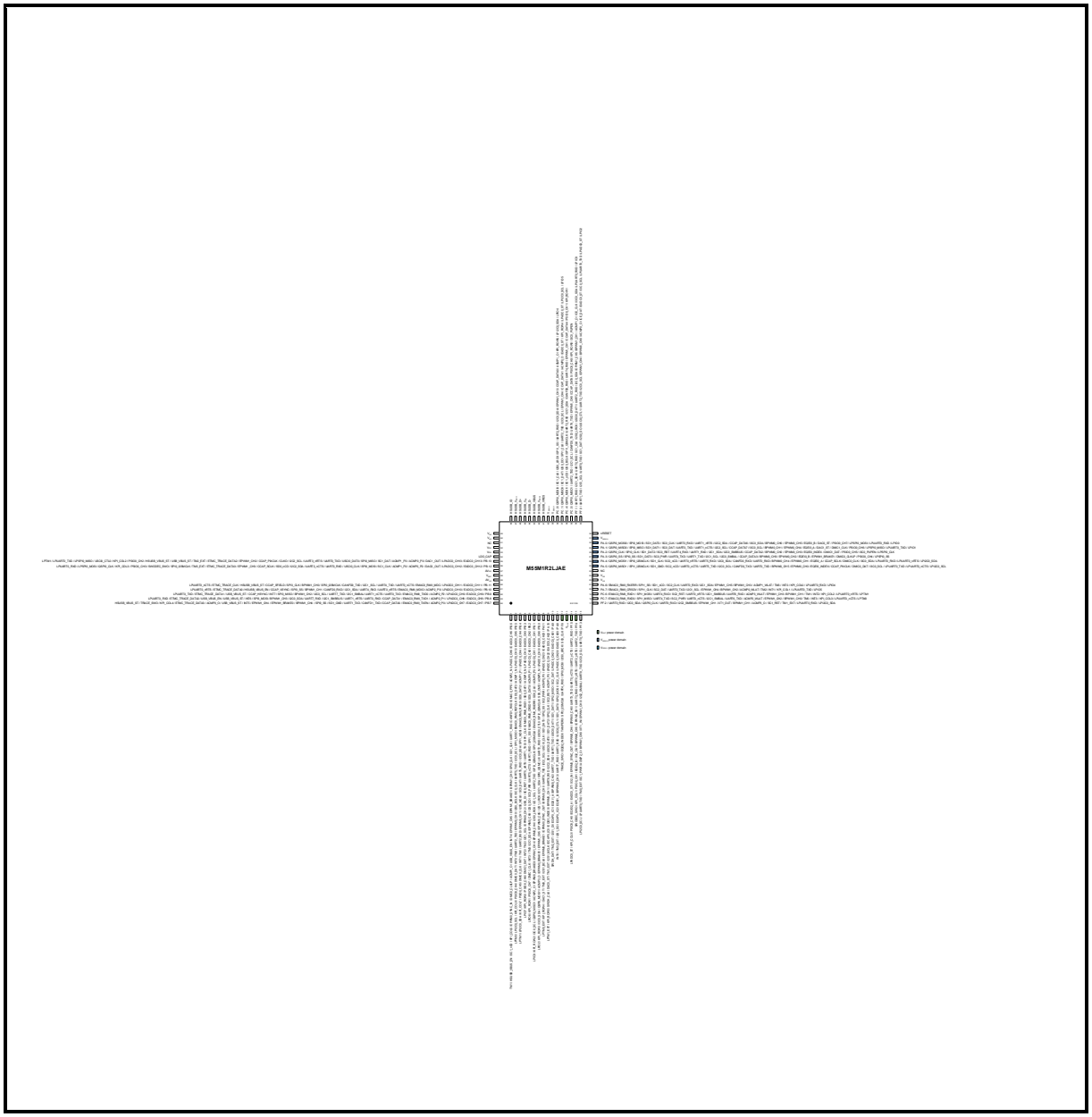


Figure 4.1-4 M55M1R2LJAE Multi-function Pin Diagram

Pin	Type	M55M1R2LJAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_N / EMAC0_PPS / CANFD1_RXD / UART1_RXD / SD1_CLK / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / DMIC0_CLKLP / EPWM0_SYNC_IN / KPI_COL5 / SC1_nCD / HSUSB_VBUS_EN / TM1
2	I/O	PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / DMIC0_DAT / PSIO0_CH4 / KPI_COL6 / LPI2C0_SCL / LPTM0

3	I/O	PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / DMIC0_CLK / PSIO0_CH5 / KPI_COL7 / LPI2C0_SDA / LPTM1
4	I/O	PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / DMIC1_DAT / PSIO0_CH6 / KPI_ROW0 / LPIO7
5	I/O	PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / DMIC1_CLK / PSIO0_CH7 / KPI_ROW1 / LPIO6
6	I/O	PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP3_P0 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / I3C0_SCL / KPI_ROW2 / LPIO3
7	I/O	PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP3_N / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / I3C0_SDA / KPI_ROW3 / LPIO2
8	I/O	PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4 / LPTM0_EXT
9	I/O	PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5 / LPTM1_EXT
10	I/O	PA.9 / EADC0_CH21 / LPADC0_CH21 / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
11	I/O	PA.8 / EADC0_CH20 / LPADC0_CH20 / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
12	I/O	PF.6 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
13	P	VBAT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / EQEI2_A / PSIO0_CH0 / KPI_COL0 / LPADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EQEI2_B / PSIO0_CH1 / KPI_COL1 / SWODEC_SWO
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / ACMP2_O / SC1_PWR / TM0_EXT / LPUART0_TXD / LPI2C0_SCL
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / ACMP3_O / SC1_RST / TM1_EXT / LPUART0_RXD / LPI2C0_SDA
18	I/O	PC.7 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / KPI_COL3 / LPUART0_nCTS / LPTM0
19	I/O	PC.6 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / KPI_COL2 / LPUART0_nRTS / LPTM1
20	I/O	PA.7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1 / LPUART0_TXD / LPIO5
21	I/O	PA.6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0 / LPUART0_RXD / LPIO4
22	P	VSS
23	P	V_{DD}

24	-	NC
25	I/O	PA.5 / EBI_AD0 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / CCAP_PIXCLK / DMIC0_DAT / I3C0_SCL / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL
26	I/O	PA.4 / EBI_AD1 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / CCAP_SCLK / DMIC0_CLK / I3C0_SDA / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / CCAP_DATA3 / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / DMIC0_CLKLP / PSIO0_CH4 / LPSPI0_SS
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / CCAP_DATA2 / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / DMIC1_DAT / PSIO0_CH5 / I3C0_PUPEN / LPSPI0_CLK
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / DMIC1_CLK / PSIO0_CH6 / LPSPI0_MISO / LPUART0_TXD / LPIO1
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7 / LPSPI0_MOSI / LPUART0_RXD / LPIO0
31	P	VDDIO0
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / I3C0_SCL / LPUART0_TXD / LPADC0_ST / LPIO2
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / I3C0_SDA / LPUART0_RXD / LPIO3
35	I/O	PC.5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / PSIO0_CH0 / KPI_ROW0 / I3C0_PUPEN
36	I/O	PC.4 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / PSIO0_CH1 / KPI_ROW1
37	I/O	PC.1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / KPI_ROW4 / LPADC0_ST / LPI2C0_SCL / LPIO5
38	I/O	PC.0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / KPI_ROW5 / LPI2C0_SDA / LPIO4
39	P	VDDIO1
40	P	VDDIO1
41	A	HSUSB_VRES
42	P	HSUSB_VDD33
43	I/O	HSUSB_VBUS
44	A	HSUSB_D-
45	P	HSUSB_VSS
46	A	HSUSB_D+
47		HSUSB_VDD11
48	I	HSUSB_ID

49	P	V_{SS}
50	P	V_{SS}
51	-	NC
52	P	V_{DD}
53	P	V_{DD}
54	A	LDO_CAP
55	I/O	PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / USB_VBUS_ST / HSUSB_VBUS_ST / PSIO0_CH2 / KPI_COL2 / USCI0_CTL0 / LPSPI0_MISO / LPUART0_TXD / LPTM1
56	I/O	PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / SPI0_I2SMCLK / SWODEC_SWO / PSIO0_CH3 / KPI_COL3 / QSPI0_CLK / LPSPI0_MOSI / LPUART0_RXD
57	P	AV_{DD}
58	A	VREF
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / LPADC0_CH11 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST / ETMC_TRACE_CLK / LPUART0_nCTS
61	I/O	PB.10 / EADC0_CH10 / LPADC0_CH10 / ACMP2_P3 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN / ETMC_TRACE_DATA0 / LPUART0_nRTS
62	I/O	PB.9 / EADC0_CH9 / LPADC0_CH9 / ACMP2_P2 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7 / CCAP_HSYNC / USB_VBUS_ST / ETMC_TRACE_DATA1 / LPUART0_TXD
63	I/O	PB.8 / EADC0_CH8 / LPADC0_CH8 / ACMP2_P1 / EMAC0_RMII_TXD1 / CCAP_DATA1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6 / USB_VBUS_ST / USB_VBUS_EN / ETMC_TRACE_DATA2 / LPUART0_RXD
64	I/O	PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P0 / EMAC0_RMII_TXEN / CCAP_DATA0 / CANFD1_TXD / UART1_TXD / SD1_CMD / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / ETMC_TRACE_DATA3 / KPI_COL4 / TRACE_SWO / HSUSB_VBUS_ST
65	P	V_{SS}

Table 4.1-1 M55M1R2LJAE Multi-function Pin Table

4.1.2.2 LQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M55M1K2LJAE

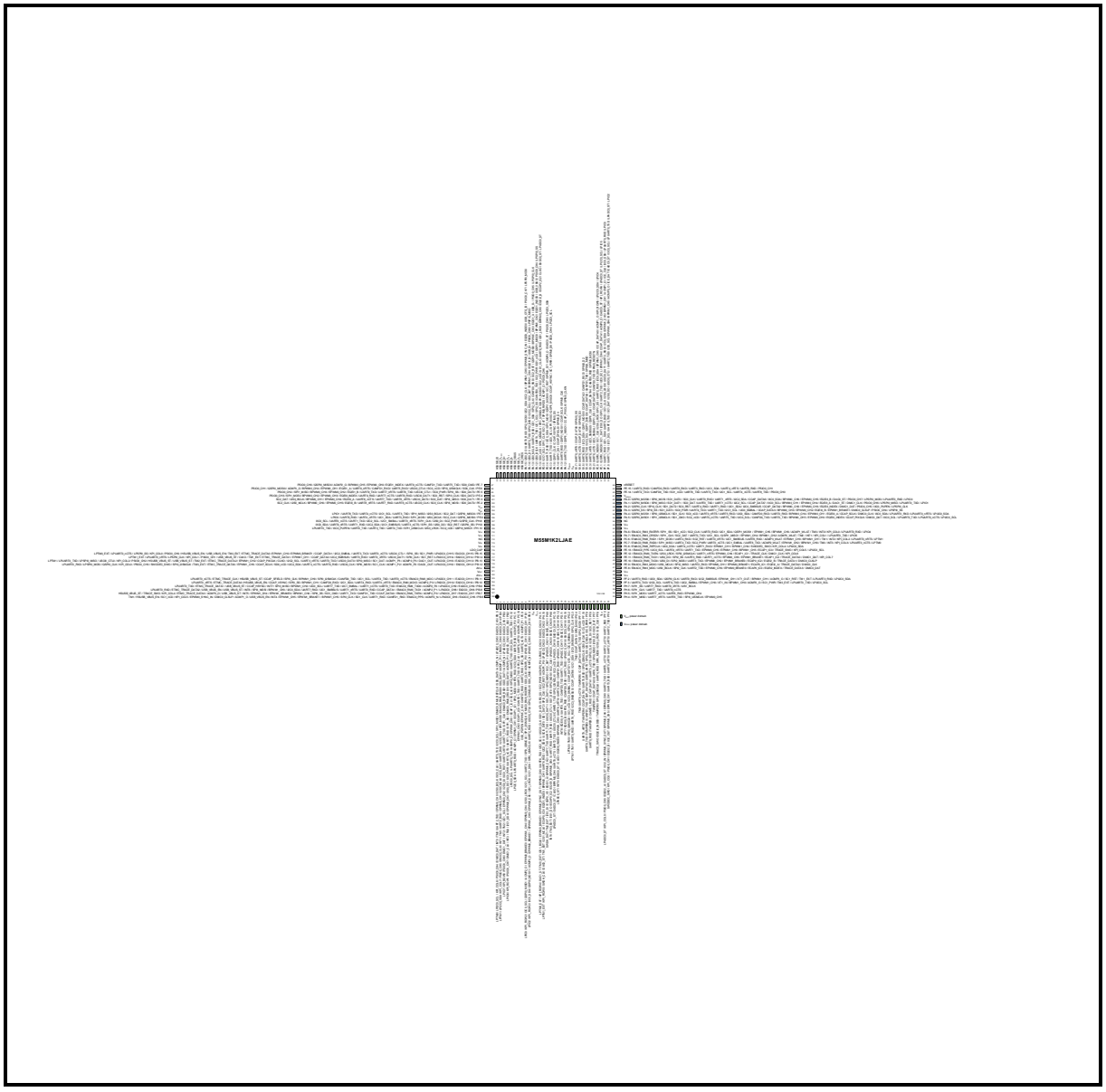


Figure 4.1-5 M55M1K2LJAE Multi-function Pin Diagram

Pin	Type	M55M1K2LJAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / DMIC0_DAT / PSIO0_CH4 / KPI_COL6 / LPI2C0_SCL / LPTM0
2	I/O	PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / DMIC0_CLK / PSIO0_CH5 / KPI_COL7 / LPI2C0_SDA / LPTM1
3	I/O	PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / DMIC1_DAT / PSIO0_CH6 / KPI_ROW0 / LPIO7

4	I/O	PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / DMIC1_CLK / PSIO0_CH7 / KPI_ROW1 / LPIO6
5	I/O	PC.12 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O / LPUART0_TXD / LPI2C0_SCL
6	I/O	PC.11 / ACMP3_P3 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O / LPUART0_RXD / LPI2C0_SDA
7	I/O	PC.10 / ACMP3_P2 / UART6_nRTS / SPI3_CLK / UART3_TXD / CANFD1_TXD / ECAP1_IC0 / EPWM1_CH2
8	I/O	PC.9 / ACMP3_P1 / UART6_nCTS / SPI3_SS / UART3_RXD / CANFD1_RXD / EPWM1_CH3 / I3C0_PUPEN
9	I/O	PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP3_P0 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / I3C0_SCL / KPI_ROW2 / LPIO3
10	I/O	PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP3_N / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / I3C0_SDA / KPI_ROW3 / LPIO2
11	P	VSS
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4 / LPTM0_EXT
14	I/O	PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5 / LPTM1_EXT
15	I/O	PA.9 / EADC0_CH21 / LPADC0_CH21 / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
16	I/O	PA.8 / EADC0_CH20 / LPADC0_CH20 / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
17	I/O	PC.13 / EADC0_CH19 / LPADC0_CH19 / SC2_nCD / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / UART8_nCTS / BPWM0_CH4 / CLKO / EADC0_ST / LPADC0_ST
18	I/O	PD.12 / EADC0_CH18 / LPADC0_CH18 / CANFD1_RXD / UART2_RXD / UART8_nRTS / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5 / LPADC0_ST
19	I/O	PD.11 / EADC0_CH17 / LPADC0_CH17 / UART1_TXD / CANFD0_TXD / UART8_TXD / EQEI0_A / INT6
20	I/O	PD.10 / EADC0_CH16 / LPADC0_CH16 / UART1_RXD / CANFD0_RXD / UART8_RXD / EQEI0_B / INT7
21	I/O	PG.2 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / CCAP_DATA7 / I2C3_SMBAL / SC1_nCD / SPI0_I2SMCLK / TM0 / LPTM0
22	I/O	PG.3 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / CCAP_DATA6 / I2C3_SMBSUS / UART4_RXD / UART0_RXD / TM1 / LPTM1
23	I/O	PG.4 / SPI2_MISO / CCAP_DATA5 / TM2
24	I/O	PF.11 / SPI2_MOSI / UART5_TXD / CCAP_DATA4 / TAMPER5 / UART9_nCTS / TM3
25	I/O	PF.10 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / CCAP_DATA3 / TAMPER4 / UART9_nRTS
26	I/O	PF.9 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / CCAP_DATA2 / CANFD1_TXD / TAMPER3 / UART9_TXD

27	I/O	PF.8 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / CCAP_DATA1 / CANFD1_RXD / TAMPER2 / UART9_RXD
28	I/O	PF.7 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / CCAP_DATA0 / TAMPER1
29	I/O	PF.6 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
30	P	VBAT
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / EQEI2_A / PSIO0_CH0 / KPI_COL0 / LPADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EQEI2_B / PSIO0_CH1 / KPI_COL1 / SWODEC_SWO
33	I/O	PH.4 / SPI1_MISO / UART7_nRTS / UART6_TXD / SPI3_I2SMCLK / EPWM0_CH5
34	I/O	PH.5 / SPI1_MOSI / UART7_nCTS / UART6_RXD / EPWM0_CH4
35	I/O	PH.6 / SPI1_CLK / UART7_TXD / UART9_nCTS
36	I/O	PH.7 / SPI1_SS / UART7_RXD / UART9_nRTS / I2S1_BCLK
37	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / ACMP2_O / SC1_PWR / TM0_EXT / LPUART0_TXD / LPI2C0_SCL
38	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / ACMP3_O / SC1_RST / TM1_EXT / LPUART0_RXD / LPI2C0_SDA
39	P	VSS
40	P	V_{DD}
41	I/O	PE.8 / EMAC0_RMII_MDC / I2S0_BCLK / SPI2_CLK / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / EQEI2_INDEX / TRACE_DATA3 / DMIC0_DAT
42	I/O	PE.9 / EMAC0_RMII_MDIO / I2S0_MCLK / SPI2_MISO / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / EQEI2_A / TRACE_DATA2 / DMIC0_CLK
43	I/O	PE.10 / EMAC0_RMII_TXD0 / I2S0_DI / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / EQEI2_B / TRACE_DATA1 / DMIC0_CLKLP
44	I/O	PE.11 / EMAC0_RMII_TXD1 / I2S0_DO / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / DMIC1_DAT / KPI_COL7
45	I/O	PE.12 / EMAC0_RMII_TXEN / I2S0_LRCK / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / DMIC1_CLK / KPI_COL6
46	I/O	PE.13 / EMAC0_PPS / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5 / LPI2C0_SCL
47	I/O	PC.8 / EMAC0_RMII_REFCLK / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / SWODEC_SWO / KPI_COL4 / LPI2C0_SDA
48	I/O	PC.7 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / KPI_COL3 / LPUART0_nCTS / LPTM0
49	I/O	PC.6 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / KPI_COL2 / LPUART0_nRTS / LPTM1
50	I/O	PA.7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1 / LPUART0_TXD / LPIO5
51	I/O	PA.6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0 / LPUART0_RXD / LPIO4
52	P	VSS

53	P	V_{DD}
54	-	NC
55	I/O	PA.5 / EBI_AD0 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / CCAP_PIXCLK / DMIC0_DAT / I3C0_SCL / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL
56	I/O	PA.4 / EBI_AD1 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / CCAP_SCLK / DMIC0_CLK / I3C0_SDA / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / CCAP_DATA3 / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / DMIC0_CLKLP / PSIO0_CH4 / LPSPI0_SS
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / CCAP_DATA2 / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / DMIC1_DAT / PSIO0_CH5 / I3C0_PUPEN / LPSPI0_CLK
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / DMIC1_CLK / PSIO0_CH6 / LPSPI0_MISO / LPUART0_TXD / LPIO1
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7 / LPSPI0_MOSI / LPUART0_RXD / LPIO0
61	P	VDDIO0
62	I/O	PE.14 / UART2_TXD / CANFD0_TXD / SD1_nCD / UART6_TXD / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD / PSIO0_CH0
63	I/O	PE.15 / UART2_RXD / CANFD0_RXD / UART6_RXD / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD / PSIO0_CH1
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / I3C0_SCL / LPUART0_TXD / LPADC0_ST / LPIO2
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / I3C0_SDA / LPUART0_RXD / LPIO3
67	I/O	PC.1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / KPI_ROW4 / LPADC0_ST / LPI2C0_SCL / LPIO5
68	I/O	PC.0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / KPI_ROW5 / LPI2C0_SDA / LPIO4
69	I/O	PJ.2 / UART8_nCTS / I2C3_SMBAL / QSPI1_SS / CCAP_DATA5 / CANFD0_TXD / SPIM0_RESETN
70	I/O	PJ.3 / UART8_nRTS / I2C3_SMBSUS / QSPI1_CLK / CCAP_DATA4 / CANFD0_RXD / SPIM0_MOSI
71	I/O	PJ.4 / UART8_TXD / I2C3_SCL / QSPI1_MISO0 / CCAP_DATA3 / CANFD1_TXD / SPIM0_MISO
72	I/O	PJ.5 / UART8_RXD / I2C3_SDA / QSPI1_MOSI0 / CCAP_DATA2 / CANFD1_RXD / SPIM0_D2
73	I/O	PJ.6 / UART9_nCTS / CCAP_DATA1 / SPIM0_D3
74	I/O	PJ.7 / UART9_nRTS / CCAP_DATA0 / SPIM0_SS
75	P	VSS

76	P	VDDIO1
77	I/O	PH.12 / UART9_TXD / QSPI1_MISO1 / CCAP_PIXCLK / SPIM0_CLKN
78	I/O	PH.13 / UART9_RXD / QSPI1_MOSI1 / CCAP_SCLK / SPIM0_CLK
79	I/O	PH.14 / QSPI1_SS / CCAP_SFIELD / SPIM0_D4
80	I/O	PH.15 / QSPI1_CLK / CCAP_VSYNC / SPIM0_D5
81	I/O	PG.13 / UART1_TXD / I2C0_SCL / SPI1_MISO / QSPI1_MISO0 / CCAP_HSYNC / SC1_PWR / SPIM0_D6 / PSIO0_CH4 / LPI2C0_SCL
82	I/O	PG.14 / UART1_RXD / I2C0_SDA / SPI1_MOSI / QSPI1_MOSI0 / SC1_RST / SPIM0_D7 / ACMP0_O / EADC0_ST / PSIO0_CH5 / LPI2C0_SDA
83	I/O	PG.15 / I2C1_SCL / SPI1_CLK / SC1_DAT / SPIM0_RWDS / ACMP1_O / PSIO0_CH6
84	I/O	PD.13 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / SC2_nCD / SD1_CLK / UART6_RXD / I2S1_LRCK / BPWM0_CH0 / EQEI2_B / ECAP2_IC2 / CLKO / EADC0_ST / LPADC0_ST
85	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / USB_VBUS / PSIO0_CH4 / LPSPI0_SS
86	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / USB_D- / PSIO0_CH5 / LPSPI0_CLK
87	I/O	PA.14 / I2S0_DI / UART0_TXD / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / USB_D+ / PSIO0_CH6 / LPSPI0_MISO
88	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7 / LPSPI0_MOSI
89	A	HSUSB_VRES
90	P	HSUSB_VDD33
91	I/O	HSUSB_VBUS
92	A	HSUSB_D-
93	P	HSUSB_VSS
94	A	HSUSB_D+
95		HSUSB_VDD11
96	I	HSUSB_ID
97	I/O	PE.7 / SD0_CMD / UART5_TXD / CANFD1_TXD / UART9_nCTS / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / ACMP2_O / QSPI0_MISO0 / PSIO0_CH0
98	I/O	PE.6 / SD0_CLK / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / UART9_nRTS / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / ACMP3_O / QSPI0_MOSI0 / PSIO0_CH1
99	I/O	PE.5 / SD0_DAT3 / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / UART9_TXD / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / SPI1_MISO / PSIO0_CH2
100	I/O	PE.4 / SD0_DAT2 / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / UART9_RXD / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / SPI1_MOSI / PSIO0_CH3
101	I/O	PE.3 / SD0_DAT1 / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / UART8_nCTS / EQEI0_A / EPWM0_CH4 / BPWM0_CH1 / I2S0_BCLK / SC2_DAT
102	I/O	PE.2 / SD0_DAT0 / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / UART8_nRTS / EQEI0_B / EPWM0_CH5 / BPWM0_CH0 / I2S0_MCLK / SC2_CLK
103	P	V_{SS}

104	P	V_{DD}
105	I/O	PE.1 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD / LPIO1
106	I/O	PE.0 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD / LPIO0
107	I/O	PH.8 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / UART9_nCTS / I3C0_SCL
108	I/O	PH.9 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / UART9_nRTS / I3C0_SDA
109	I/O	PH.10 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / UART9_TXD / I3C0_PUPEN / LPUART0_TXD
110	P	VSS
111	P	VSS
112	-	NC
113	P	V_{DD}
114	P	V_{DD}
115	A	LDO_CAP
116	I/O	PB.15 / EADC0_CH15 / LPADC0_CH15 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 / ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0 / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT
117	I/O	PB.14 / EADC0_CH14 / LPADC0_CH14 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1 / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT
118	I/O	PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / USB_VBUS_ST / HSUSB_VBUS_ST / PSIO0_CH2 / KPI_COL2 / USCI0_CTL0 / LPSPI0_MISO / LPUART0_TXD / LPTM1
119	I/O	PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / SPI0_I2SMCLK / SWODEC_SWO / PSIO0_CH3 / KPI_COL3 / QSPI0_CLK / LPSPI0_MOSI / LPUART0_RXD
120	P	AV_{DD}
121	A	VREF
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / LPADC0_CH11 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST / ETMC_TRACE_CLK / LPUART0_nCTS
124	I/O	PB.10 / EADC0_CH10 / LPADC0_CH10 / ACMP2_P3 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN / ETMC_TRACE_DATA0 / LPUART0_nRTS
125	I/O	PB.9 / EADC0_CH9 / LPADC0_CH9 / ACMP2_P2 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7 / CCAP_HSYNC / USB_VBUS_ST / ETMC_TRACE_DATA1 / LPUART0_TXD
126	I/O	PB.8 / EADC0_CH8 / LPADC0_CH8 / ACMP2_P1 / EMAC0_RMII_TXD1 / CCAP_DATA1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6 / USB_VBUS_ST / USB_VBUS_EN / ETMC_TRACE_DATA2 / LPUART0_RXD

127	I/O	PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P0 / EMAC0_RMII_TXEN / CCAP_DATA0 / CANFD1_TXD / UART1_TXD / SD1_CMD / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / ETMC_TRACE_DATA3 / KPI_COL4 / TRACE_SWO / HSUSB_VBUS_ST
128	I/O	PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_N / EMAC0_PPS / CANFD1_RXD / UART1_RXD / SD1_CLK / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / DMIC0_CLKLP / EPWM0_SYNC_IN / KPI_COL5 / SC1_nCD / HSUSB_VBUS_EN / TM1
129	P	VSS

Table 4.1-2 M55M1K2LJAE Multi-function Pin Table

4.1.2.3 LQFP176-Pin Multi-function Pin Diagram

Corresponding Part Number: M55M1H2LJAE

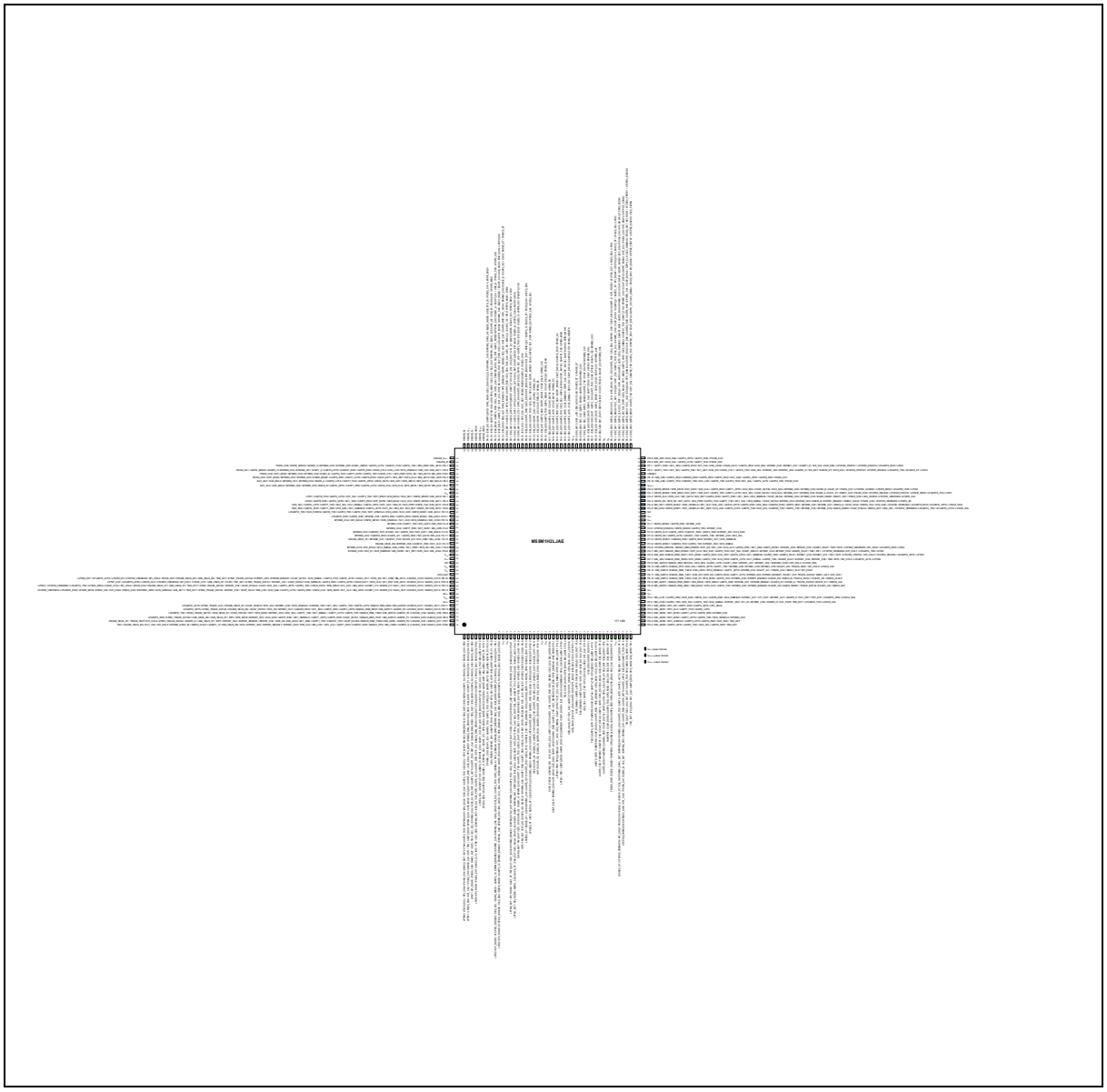


Figure 4.1-6 M55M1H2LJAE Multi-function Pin Diagram

Pin	Type	M55M1H2LJAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / DMIC0_DAT / PSIO0_CH4 / KPI_COL6 / LPI2C0_SCL / LPTM0
2	I/O	PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / DMIC0_CLK / PSIO0_CH5 / KPI_COL7 / LPI2C0_SDA / LPTM1
3	I/O	PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / DMIC1_DAT / PSIO0_CH6 / KPI_ROW0 / LPIO7

4	I/O	PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / DMIC1_CLK / PSIO0_CH7 / KPI_ROW1 / LPIO6
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O / LPUART0_TXD / LPI2C0_SCL
6	I/O	PC.11 / ACMP3_P3 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O / LPUART0_RXD / LPI2C0_SDA
7	I/O	PC.10 / ACMP3_P2 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CANFD1_TXD / ECAP1_IC0 / EPWM1_CH2
8	I/O	PC.9 / ACMP3_P1 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CANFD1_RXD / EPWM1_CH3 / I3C0_PUPEN
9	I/O	PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP3_P0 / EBI_ADR8 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / I3C0_SCL / UTCPD0_VBDCHG / KPI_ROW2 / LPIO3
10	I/O	PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP3_N / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / I3C0_SDA / UTCPD0_VCNEN2 / KPI_ROW3 / LPIO2
11	P	VSS
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4 / LPTM0_EXT
14	I/O	PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5 / LPTM1_EXT
15	I/O	PA.9 / EADC0_CH21 / LPADC0_CH21 / EBI_MCLK / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
16	I/O	PA.8 / EADC0_CH20 / LPADC0_CH20 / EBI_ALE / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
17	I/O	PC.13 / EADC0_CH19 / LPADC0_CH19 / EBI_ADR10 / SC2_nCD / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / UART8_nCTS / BPWM0_CH4 / CLKO / EADC0_ST / LPADC0_ST
18	I/O	PD.12 / EADC0_CH18 / LPADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / UART8_nRTS / BPWM0_CH5 / EQEI0_INDEX / ECAP3_IC0 / CLKO / EADC0_ST / INT5 / LPADC0_ST
19	I/O	PD.11 / EADC0_CH17 / LPADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / UART8_TXD / EQEI0_A / ECAP3_IC1 / INT6
20	I/O	PD.10 / EADC0_CH16 / LPADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / UART8_RXD / EQEI0_B / ECAP3_IC2 / INT7
21	P	V_{SS}
22	P	V_{DD}
23	I/O	PG.0 / EBI_ADR8 / I2C0_SCL / I2C1_SMBAL / UART2_RXD / CANFD1_TXD / UART1_TXD / I2C3_SCL / I2S1_DO / EPWM0_CH1 / CCAP_PIXCLK
24	I/O	PG.1 / EBI_ADR9 / SPI2_I2SMCLK / I2C0_SDA / I2C1_SMBSUS / UART2_TXD / CANFD1_RXD / UART1_RXD / I2C3_SDA / I2S1_LRCK / EPWM0_CH0 / CCAP_SCLK
25	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / CCAP_DATA7 / I2C3_SMBAL / SC1_nCD / SPI0_I2SMCLK / TM0 / LPTM0

26	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / CCAP_DATA6 / I2C3_SMBSUS / UART4_RXD / UART0_RXD / TM1 / LPTM1
27	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / CCAP_DATA5 / TM2
28	I/O	PI.6 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_TXD / I2C1_SCL / USB_VBUS_ST
29	I/O	PI.7 / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_RXD / I2C1_SDA / USB_VBUS_EN
30	I/O	PI.8 / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nRTS / I2C0_SMBAL
31	I/O	PI.9 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_nCTS / I2C0_SMBSUS
32	I/O	PI.10 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_TXD / I2C0_SCL
33	I/O	PI.11 / UART2_RXD / I2C0_SDA
34	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / CCAP_DATA4 / TAMPER5 / UART9_nCTS / TM3
35	I/O	PF.10 / EBI_ADR15 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / CCAP_DATA3 / TAMPER4 / UART9_nRTS
36	I/O	PF.9 / EBI_ADR16 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / CCAP_DATA2 / CANFD1_TXD / TAMPER3 / UART9_TXD
37	I/O	PF.8 / EBI_ADR17 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / CCAP_DATA1 / CANFD1_RXD / TAMPER2 / UART9_RXD
38	I/O	PF.7 / EBI_ADR18 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / CCAP_DATA0 / TAMPER1
39	I/O	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
40	P	VBAT
41	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / EQEI2_A / PSIO0_CH0 / KPI_COL0 / UTCPD0_VBSNKEN / LPADC0_ST
42	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EQEI2_B / PSIO0_CH1 / KPI_COL1 / SWODEC_SWO / UTCPD0_VBSRCEN
43	I/O	PH.0 / EBI_ADR7 / SPI3_MISO / UART5_TXD / SC1_DAT / I2C3_SCL / TM0_EXT
44	I/O	PH.1 / EBI_ADR6 / SPI3_MOSI / UART5_RXD / SC1_CLK / I2C3_SDA / TM1_EXT
45	I/O	PH.2 / EBI_ADR5 / UART5_nRTS / UART4_TXD / I2C0_SCL / UART9_RXD / TM2_EXT
46	I/O	PH.3 / EBI_ADR4 / SPI1_I2SMCLK / UART5_nCTS / UART4_RXD / I2C0_SDA / TM3_EXT
47	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD / SPI3_I2SMCLK / EPWM0_CH5
48	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD / EPWM0_CH4
49	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD / UART9_nCTS
50	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD / UART9_nRTS / I2S1_BCLK
51	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / ACMP2_O / SC1_PWR / TM0_EXT / LPUART0_TXD / LPI2C0_SCL
52	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / ACMP3_O / SC1_RST / TM1_EXT / LPUART0_RXD / LPI2C0_SDA
53	P	V_{SS}
54	P	V_{DD}
55	I/O	PE.8 / EBI_ADR10 / EMAC0_RMII_MDC / I2S0_BCLK / SPI2_CLK / UART2_TXD / EPWM0_CH0 /

		EPWM0_BRAKE0 / ECAP0_IC0 / EQEI2_INDEX / TRACE_DATA3 / ECAP3_IC0 / DMIC0_DAT
56	I/O	PE.9 / EBI_ADR11 / EMAC0_RMII_MDIO / I2S0_MCLK / SPI2_MISO / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / EQEI2_A / TRACE_DATA2 / ECAP3_IC1 / DMIC0_CLK
57	I/O	PE.10 / EBI_ADR12 / EMAC0_RMII_TXD0 / I2S0_DI / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / EQEI2_B / TRACE_DATA1 / ECAP3_IC2 / DMIC0_CLKLP
58	I/O	PE.11 / EBI_ADR13 / EMAC0_RMII_TXD1 / I2S0_DO / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / DMIC1_DAT / KPI_COL7
59	I/O	PE.12 / EBI_ADR14 / EMAC0_RMII_TXEN / I2S0_LRCK / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / DMIC1_CLK / KPI_COL6
60	I/O	PE.13 / EBI_ADR15 / EMAC0_PPS / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5 / LPI2C0_SCL
61	I/O	PC.8 / EBI_ADR16 / EMAC0_RMII_REFCLK / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / SWODEC_SWO / KPI_COL4 / LPI2C0_SDA
62	I/O	PC.7 / EBI_AD9 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / KPI_COL3 / LPUART0_nCTS / LPTM0
63	I/O	PC.6 / EBI_AD8 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / UTCPD0_FRSTX2 / KPI_COL2 / UTCPD0_DISCHG / LPUART0_nRTS / LPTM1
64	I/O	PA.7 / EBI_AD7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / KPI_COL1 / LPUART0_TXD / LPIO5
65	I/O	PA.6 / UTCPD0_DISCHG / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / KPI_COL0 / LPUART0_RXD / LPIO4
66	I/O	PI.12 / QSPI0_MISO1 / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL
67	I/O	PI.13 / QSPI0_MOSI1 / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS
68	I/O	PI.14 / QSPI0_SS / UART8_nCTS / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / I2C3_SCL
69	I/O	PI.15 / QSPI0_CLK / UART8_nRTS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / I2C3_SDA
70	I/O	PJ.0 / UTCPD0_DISCHG / QSPI0_MISO0 / UART8_TXD / EPWM1_CH4
71	I/O	PJ.1 / QSPI0_MOSI0 / UART8_RXD / EPWM1_CH5
72	P	V_{SS}
73	P	V_{DD}
74	-	NC
75	I/O	PA.5 / EBI_AD0 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / CCAP_PIXCLK / DMIC0_DAT / I3C0_SCL / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL
76	I/O	PA.4 / EBI_AD1 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / CCAP_SCLK / DMIC0_CLK / I3C0_SDA / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA
77	I/O	PA.3 / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / CCAP_DATA3 / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / DMIC0_CLKLP / PSIO0_CH4 / UTCPD0_VBSNKEN / LPSPI0_SS
78	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / CCAP_DATA2 / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / DMIC1_DAT / PSIO0_CH5 / I3C0_PUPEN / UTCPD0_VBSRCEN / LPSPI0_CLK

79	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / DMIC1_CLK / PSIO0_CH6 / UTCPD0_DISCHG / UTCPD0_FRSTX1 / LPSPI0_MISO / LPUART0_TXD / LPIO1
80	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0
81	P	VDDIO0
82	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / SD1_nCD / UART6_TXD / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD / PSIO0_CH0
83	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD / PSIO0_CH1
84	I	nRESET
85	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / I3C0_SCL / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPADC0_ST / LPIO2
86	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / I3C0_SDA / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3
87	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD / PSIO0_CH2
88	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD / PSIO0_CH3
89	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / QSPI1_SS / I2C3_SMBAL / PSIO0_CH0 / KPI_ROW0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG / I3C0_PUPEN
90	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / QSPI1_CLK / I2C3_SMBSUS / PSIO0_CH1 / KPI_ROW1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG
91	I/O	PC.3 / EBI_AD3 / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / CCAP_DATA3 / QSPI1_MISO0 / I2C3_SCL / PSIO0_CH2 / KPI_ROW2 / UTCPD0_CCDB1
92	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / CCAP_DATA2 / QSPI1_MOSI0 / I2C3_SDA / PSIO0_CH3 / KPI_ROW3 / UTCPD0_CCDB2
93	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / KPI_ROW4 / UTCPD0_CC2 / LPADC0_ST / LPI2C0_SCL / LPIO5
94	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / KPI_ROW5 / UTCPD0_CC1 / LPI2C0_SDA / LPIO4
95	P	V_{SS}
96	P	V_{DD}
97	I/O	PG.9 / EBI_AD0 / SD1_DAT3 / QSPI1_MISO1 / CCAP_PIXCLK / ECAP2_IC0 / BPWM0_CH5
98	I/O	PG.10 / EBI_AD1 / SD1_DAT2 / QSPI1_MOSI1 / CCAP_SCLK / ECAP2_IC1 / BPWM0_CH4
99	I/O	PG.11 / EBI_AD2 / SD1_DAT1 / QSPI1_SS / UART7_TXD / CCAP_SFIELD / ECAP2_IC2 / BPWM0_CH3
100	I/O	PG.12 / EBI_AD3 / SD1_DAT0 / QSPI1_CLK / UART7_RXD / CCAP_VSYNC / BPWM0_CH2
101	I/O	PD.7 / EBI_AD4 / SD1_CMD / QSPI1_MISO0 / UART6_TXD / CCAP_HSYNC / BPWM0_CH1
102	I/O	PD.6 / EBI_AD5 / SD1_CLK / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0

103	I/O	PD.5 / EBI_AD15 / SD1_nCD / EBI_nCS0 / CLKO / EADC0_ST / LPADC0_ST
104	P	VDDIO1
105	I/O	PJ.2 / EBI_AD5 / UART8_nCTS / I2C3_SMBAL / QSPI1_SS / CCAP_DATA5 / CANFD0_TXD / SPIM0_RESETN
106	I/O	PJ.3 / EBI_AD4 / UART8_nRTS / I2C3_SMBSUS / QSPI1_CLK / CCAP_DATA4 / CANFD0_RXD / SPIM0_MOSI
107	I/O	PJ.4 / EBI_AD3 / UART8_TXD / I2C3_SCL / QSPI1_MISO0 / CCAP_DATA3 / CANFD1_TXD / SPIM0_MISO
108	I/O	PJ.5 / EBI_AD2 / UART8_RXD / I2C3_SDA / QSPI1_MOSI0 / CCAP_DATA2 / CANFD1_RXD / SPIM0_D2
109	I/O	PJ.6 / EBI_AD1 / UART9_nCTS / CCAP_DATA1 / SPIM0_D3
110	I/O	PJ.7 / EBI_AD0 / UART9_nRTS / CCAP_DATA0 / SPIM0_SS
111	I/O	PH.12 / EBI_AD0 / UART9_TXD / QSPI1_MISO1 / CCAP_PIXCLK / SPIM0_CLKN
112	I/O	PH.13 / EBI_AD1 / UART9_RXD / QSPI1_MOSI1 / CCAP_SCLK / SPIM0_CLK
113	I/O	PH.14 / EBI_AD2 / QSPI1_SS / CCAP_SFIELD / SPIM0_D4
114	I/O	PH.15 / EBI_AD3 / QSPI1_CLK / CCAP_VSYNC / SPIM0_D5
115	I/O	PG.13 / EBI_AD4 / UART1_TXD / I2C0_SCL / SPI1_MISO / QSPI1_MISO0 / CCAP_HSYNC / SC1_PWR / SPIM0_D6 / PSIO0_CH4 / LPI2C0_SCL
116	I/O	PG.14 / EBI_AD5 / UART1_RXD / I2C0_SDA / SPI1_MOSI / QSPI1_MOSI0 / SC1_RST / SPIM0_D7 / ACMP0_O / EADC0_ST / PSIO0_CH5 / LPI2C0_SDA
117	I/O	PG.15 / I2C1_SCL / SPI1_CLK / SC1_DAT / SPIM0_RWDS / ACMP1_O / PSIO0_CH6
118	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / SC2_PWR / SC1_nCD / UART0_TXD / I2S1_BCLK / EQEI3_A / LPSPI0_SS / LPUART0_TXD
119	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / SC2_RST / UART0_RXD / I2S1_MCLK / EQEI3_B / LPSPI0_CLK / LPUART0_RXD
120	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL / SC2_DAT / I2S1_DI / EQEI2_INDEX / ECAP2_IC0 / LPSPI0_MISO / LPIO7
121	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / SC2_CLK / I2S1_DO / EQEI2_A / ECAP2_IC1 / TM2 / LPSPI0_MOSI / LPIO6
122	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / SC2_nCD / SD1_CLK / UART6_RXD / I2S1_LRCK / BPWM0_CH0 / EQEI2_B / ECAP2_IC2 / CLKO / EADC0_ST / LPADC0_ST
123	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / ECAP3_IC0 / USB_VBUS / PSIO0_CH4 / LPSPI0_SS
124	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / ECAP3_IC1 / USB_D- / PSIO0_CH5 / LPSPI0_CLK
125	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / ECAP3_IC2 / USB_D+ / PSIO0_CH6 / LPSPI0_MISO
126	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7 / LPSPI0_MOSI
127	A	HSUSB_VRES
128	P	HSUSB_VDD33
129	I/O	HSUSB_VBUS

130	A	HSUSB_D-
131	P	HSUSB_VSS
132	A	HSUSB_D+
133	P	HSUSB_VDD11
134	I	HSUSB_ID
135	I/O	PE.7 / EBI_AD10 / SD0_CMD / UART5_TXD / CANFD1_TXD / UART9_nCTS / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / ACMP2_O / QSPI0_MISO0 / PSIO0_CH0
136	I/O	PE.6 / EBI_AD11 / SD0_CLK / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / UART9_nRTS / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / ACMP3_O / QSPI0_MOSI0 / PSIO0_CH1
137	I/O	PE.5 / EBI_nRD / SD0_DAT3 / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / UART9_TXD / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / SPI1_MISO / PSIO0_CH2
138	I/O	PE.4 / EBI_nWR / SD0_DAT2 / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / UART9_RXD / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / SPI1_MOSI / PSIO0_CH3
139	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / UART8_nCTS / EQEI0_A / EPWM0_CH4 / BPWM0_CH1 / I2S0_BCLK / SC2_DAT
140	I/O	PE.2 / EBI_ALE / SD0_DAT0 / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / UART8_nRTS / EQEI0_B / EPWM0_CH5 / BPWM0_CH0 / I2S0_MCLK / SC2_CLK
141	P	V_{SS}
142	P	V_{DD}
143	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD / LPIO1
144	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD / LPIO0
145	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / UART9_nCTS / I3C0_SCL
146	I/O	PH.9 / EBI_AD13 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / UART9_nRTS / I3C0_SDA
147	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / UART9_TXD / I3C0_PUPEN / LPUART0_TXD
148	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / UART9_RXD / LPUART0_RXD
149	I/O	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SC1_nCD / SPI0_I2SMCLK / QSPI0_MOSI1 / I2S1_BCLK / EPWM0_CH4
150	I/O	PJ.8 / EBI_nRD / SD1_DAT3 / UART7_TXD / BPWM0_CH5
151	I/O	PJ.9 / EBI_nWR / SD1_DAT2 / UART7_RXD / BPWM0_CH4
152	I/O	PJ.10 / EBI_MCLK / SD1_DAT1 / UART6_TXD / ECAP2_IC0 / CANFD0_TXD / BPWM0_CH3
153	I/O	PJ.11 / EBI_ALE / SD1_DAT0 / UART6_RXD / ECAP2_IC1 / CANFD0_RXD / BPWM0_CH2
154	I/O	PJ.12 / EBI_nCS0 / SD1_CMD / ECAP2_IC2 / CANFD1_TXD / BPWM0_CH1 / HSUSB_VBUS_ST
155	I/O	PJ.13 / SD1_CLK / CANFD1_RXD / BPWM0_CH0 / HSUSB_VBUS_EN
156	I/O	PG.5 / EBI_nCS1 / SPI3_SS / SC1_PWR / EBI_nWRL / I2C3_SMBAL / I2S1_MCLK / EPWM0_CH3
157	I/O	PG.6 / EBI_nCS2 / SPI3_CLK / SC1_RST / EBI_nWRH / I2C3_SMBSUS / I2S1_DI / EPWM0_CH2
158	P	VSS

159	P	V_{SS}
160	-	NC
161	P	V_{DD}
162	P	V_{DD}
163	A	LDO_CAP
164	I/O	PB.15 / EADC0_CH15 / LPADC0_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 / ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0 / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT
165	I/O	PB.14 / EADC0_CH14 / LPADC0_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1 / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT
166	I/O	PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / USB_VBUS_ST / HSUSB_VBUS_ST / PSIO0_CH2 / KPI_COL2 / USCI0_CTL0 / LPSPI0_MISO / LPUART0_TXD / UTCPD0_VBSNKEN / LPTM1
167	I/O	PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / SWODEC_SWO / PSIO0_CH3 / KPI_COL3 / QSPI0_CLK / LPSPI0_MOSI / LPUART0_RXD / UTCPD0_VBSRCEN
168	P	AV_{DD}
169	A	VREF
170	P	AV_{SS}
171	I/O	PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST / ETMC_TRACE_CLK / LPUART0_nCTS
172	I/O	PB.10 / EADC0_CH10 / LPADC0_CH10 / ACMP2_P3 / EBI_ADR17 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN / ETMC_TRACE_DATA0 / LPUART0_nRTS
173	I/O	PB.9 / EADC0_CH9 / LPADC0_CH9 / ACMP2_P2 / EBI_ADR18 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7 / CCAP_HSYNC / USB_VBUS_ST / ETMC_TRACE_DATA1 / LPUART0_TXD
174	I/O	PB.8 / EADC0_CH8 / LPADC0_CH8 / ACMP2_P1 / EBI_ADR19 / EMAC0_RMII_TXD1 / CCAP_DATA1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6 / USB_VBUS_ST / USB_VBUS_EN / ETMC_TRACE_DATA2 / LPUART0_RXD
175	I/O	PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P0 / EBI_nWRL / EMAC0_RMII_TXEN / CCAP_DATA0 / CANFD1_TXD / UART1_TXD / SD1_CMD / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / ETMC_TRACE_DATA3 / KPI_COL4 / TRACE_SWO / HSUSB_VBUS_ST
176	I/O	PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_N / EBI_nWRH / EMAC0_PPS / CANFD1_RXD / UART1_RXD / SD1_CLK / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / DMIC0_CLKLP / EPWM0_SYNC_IN / KPI_COL5 / SC1_nCD / HSUSB_VBUS_EN / TM1
177	P	VSS

Table 4.1-3 M55M1H2LJAE Multi-function Pin Table

4.2 Pin Mapping Table

4.2.1 M55M1 Series Pin Mapping Table

	M55M1		
Pin Name	**64 Pin**	**128 Pin**	**176 Pin**
PB.5	2	1	1
PB.4	3	2	2
PB.3	4	3	3
PB.2	5	4	4
PC.12		5	5
PC.11		6	6
PC.10		7	7
PC.9		8	8
PB.1	6	9	9
PB.0	7	10	10
V_{SS}		11	11
V_{DD}		12	12
PA.11	8	13	13
PA.10	9	14	14
PA.9	10	15	15
PA.8	11	16	16
PC.13		17	17
PD.12		18	18
PD.11		19	19
PD.10		20	20
V_{SS}			21
V_{DD}			22
PG.0			23
PG.1			24
PG.2		21	25
PG.3		22	26
PG.4		23	27
PI.6			28
PI.7			29
PI.8			30

PI.9			31
PI.10			32
PI.11			33
PF.11		24	34
PF.10		25	35
PF.9		26	36
PF.8		27	37
PF.7		28	38
PF.6	12	29	39
V_{BAT}	13	30	40
PF.5	14	31	41
PF.4	15	32	42
PH.0			43
PH.1			44
PH.2			45
PH.3			46
PH.4		33	47
PH.5		34	48
PH.6		35	49
PH.7		36	50
PF.3	16	37	51
PF.2	17	38	52
V_{SS}		39	53
V_{DD}		40	54
PE.8		41	55
PE.9		42	56
PE.10		43	57
PE.11		44	58
PE.12		45	59
PE.13		46	60
PC.8		47	61
PC.7	18	48	62
PC.6	19	49	63
PA.7	20	50	64
PA.6	21	51	65

PI.12			66
PI.13			67
PI.14			68
PI.15			69
PJ.0			70
PJ.1			71
V_{SS}	22	52	72
V_{DD}	23	53	73
NC	24	54	74
PA.5	25	55	75
PA.4	26	56	76
PA.3	27	57	77
PA.2	28	58	78
PA.1	29	59	79
PA.0	30	60	80
V_{DDIO0}	31	61	81
PE.14		62	82
PE.15		63	83
nRESET	32	64	84
PF.0	33	65	85
PF.1	34	66	86
PD.9			87
PD.8			88
PC.5	35		89
PC.4	36		90
PC.3			91
PC.2			92
PC.1	37	67	93
PC.0	38	68	94
V_{SS}			95
V_{DD}			96
PG.9			97
PG.10			98
PG.11			99
PG.12			100

PD.7			101
PD.6			102
PD.5			103
V_{DDIO1}	39		104
PJ.2		69	105
PJ.3		70	106
PJ.4		71	107
PJ.5		72	108
PJ.6		73	109
PJ.7		74	110
PH.12		77	111
PH.13		78	112
V_{SS}		75	
V_{DDIO1}	40	76	
PH.14		79	113
PH.15		80	114
PG.13		81	115
PG.14		82	116
PG.15		83	117
NC			
NC			
NC			
NC			
NC			
NC			
NC			
NC			
NC			
NC			
NC			
NC			
PD.4			
PD.3			118
PD.2			119
PD.1			120
PD.0			121

PD.13		84	122
PA.12		85	123
PA.13		86	124
PA.14		87	125
PA.15		88	126
HSUSB_VRES	41	89	127
HSUSB_VDD33	42	90	128
HSUSB_VBUS	43	91	129
HSUSB_D-	44	92	130
HSUSB_V_{SS}	45	93	131
HSUSB_D+	46	94	132
HSUSB_VDD11	47	95	133
HSUSB_ID	48	96	134
PE.7		97	135
PE.6		98	136
PE.5		99	137
PE.4		100	138
PE.3		101	139
PE.2		102	140
V_{SS}	49	103	141
V_{DD}		104	142
PE.1		105	143
PE.0		106	144
PH.8		107	145
PH.9		108	146
PH.10		109	147
PH.11			148
PD.14			149
PJ.8			150
PJ.9			151
PJ.10			152
PJ.11			153
PJ.12			154
PJ.13			155
PG.5			156

PG.6			157
V_{SS}		110	158
V_{SS}	50		
V_{SS}		111	159
NC	51	112	160
V_{DD}	52	113	161
V_{DD}	53	114	162
LDO_CAP	54	115	163
PB.15		116	164
PB.14		117	165
PB.13	55	118	166
PB.12	56	119	167
AV_{DD}	57	120	168
V_{REF}	58	121	169
AV_{SS}	59	122	170
PB.11	60	123	171
PB.10	61	124	172
PB.9	62	125	173
PB.8	63	126	174
PB.7	64	127	175
PB.6	1	128	176
V_{SS}	65	129	177

4.3 Pin Functional Description

4.3.1 M55M1 Series Summary Function Pin Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
ACMP2	ACMP2_N	A	Analog comparator 2 negative input pin.
	ACMP2_O	O	Analog comparator 2 output pin.
	ACMP2_P0	A	Analog comparator 2 positive input 0 pin.
	ACMP2_P1	A	Analog comparator 2 positive input 1 pin.
	ACMP2_P2	A	Analog comparator 2 positive input 2 pin.
	ACMP2_P3	A	Analog comparator 2 positive input 3 pin.
	ACMP2_WLAT	I	Analog comparator 2 window latch input pin
ACMP3	ACMP3_N	A	Analog comparator 3 negative input pin.
	ACMP3_O	O	Analog comparator 3 output pin.
	ACMP3_P0	A	Analog comparator 3 positive input 0 pin.
	ACMP3_P1	A	Analog comparator 3 positive input 1 pin.
	ACMP3_P2	A	Analog comparator 3 positive input 2 pin.
	ACMP3_P3	A	Analog comparator 3 positive input 3 pin.
	ACMP3_WLAT	I	Analog comparator 3 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.

Group	Pin Name	Type	Description
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CANFD0	CANFD0_RXD	I	CANFD0 bus receiver input.
	CANFD0_TXD	O	CANFD0 bus transmitter output.
CANFD1	CANFD1_RXD	I	CANFD1 bus receiver input.
	CANFD1_TXD	O	CANFD1 bus transmitter output.
CCAP	CCAP_DATA0	I	Camera capture data input bus bit 0.
	CCAP_DATA1	I	Camera capture data input bus bit 1.
	CCAP_DATA2	I	Camera capture data input bus bit 2.
	CCAP_DATA3	I	Camera capture data input bus bit 3.
	CCAP_DATA4	I	Camera capture data input bus bit 4.
	CCAP_DATA5	I	Camera capture data input bus bit 5.
	CCAP_DATA6	I	Camera capture data input bus bit 6.
	CCAP_DATA7	I	Camera capture data input bus bit 7.
	CCAP_HSYNC	I	Camera capture interface hsync input pin.
	CCAP_PIXCLK	I	Camera capture interface pix clock input pin.
	CCAP_SCLK	O	Camera capture interface sensor clock pin.
	CCAP_SFIELD	I	Camera capture interface SFIELD input pin.
	CCAP_VSYNC	I	Camera capture interface vsync input pin.
CLKO	CLKO	O	Clock Out.
DAC0	DAC0_OUT	A	DAC0 channel analog output.
	DAC0_ST	I	DAC0 external trigger input.
DAC1	DAC1_OUT	A	DAC1 channel analog output.
	DAC1_ST	I	DAC1 external trigger input.
DMIC0	DMIC0_CLK	O	Clock of channel 1 output pin.
	DMIC0_CLKLP	O	Clock of channel 0 output pin.
	DMIC0_DAT	I	PDM data of channel 0 and channel 1 input.

Group	Pin Name	Type	Description
DMIC1	DMIC1_CLK	O	Clock of channel 2 and channel 3 output pin.
	DMIC1_DAT	I	PDM data of channel 2 and channel 3 input.
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_CH16	A	EADC0 channel 16 analog input.
	EADC0_CH17	A	EADC0 channel 17 analog input.
	EADC0_CH18	A	EADC0 channel 18 analog input.
	EADC0_CH19	A	EADC0 channel 19 analog input.
	EADC0_CH20	A	EADC0 channel 20 analog input.
	EADC0_CH21	A	EADC0 channel 21 analog input.
	EADC0_CH22	A	EADC0 channel 22 analog input.
	EADC0_CH23	A	EADC0 channel 23 analog input.
	EADC0_ST	I	EADC0 external trigger input.
EBI	EBI_AD0	I/O	EBI address/data bus bit 0.
	EBI_AD1	I/O	EBI address/data bus bit 1.
	EBI_AD2	I/O	EBI address/data bus bit 2.
	EBI_AD3	I/O	EBI address/data bus bit 3.
	EBI_AD4	I/O	EBI address/data bus bit 4.
	EBI_AD5	I/O	EBI address/data bus bit 5.
	EBI_AD6	I/O	EBI address/data bus bit 6.

Group	Pin Name	Type	Description
	EBI_AD7	I/O	EBI address/data bus bit 7.
	EBI_AD8	I/O	EBI address/data bus bit 8.
	EBI_AD9	I/O	EBI address/data bus bit 9.
	EBI_AD10	I/O	EBI address/data bus bit 10.
	EBI_AD11	I/O	EBI address/data bus bit 11.
	EBI_AD12	I/O	EBI address/data bus bit 12.
	EBI_AD13	I/O	EBI address/data bus bit 13.
	EBI_AD14	I/O	EBI address/data bus bit 14.
	EBI_AD15	I/O	EBI address/data bus bit 15.
	EBI_ADR0	O	EBI address bus bit 0.
	EBI_ADR1	O	EBI address bus bit 1.
	EBI_ADR2	O	EBI address bus bit 2.
	EBI_ADR3	O	EBI address bus bit 3.
	EBI_ADR4	O	EBI address bus bit 4.
	EBI_ADR5	O	EBI address bus bit 5.
	EBI_ADR6	O	EBI address bus bit 6.
	EBI_ADR7	O	EBI address bus bit 7.
	EBI_ADR8	O	EBI address bus bit 8.
	EBI_ADR9	O	EBI address bus bit 9.
	EBI_ADR10	O	EBI address bus bit 10.
	EBI_ADR11	O	EBI address bus bit 11.
	EBI_ADR12	O	EBI address bus bit 12.
	EBI_ADR13	O	EBI address bus bit 13.
	EBI_ADR14	O	EBI address bus bit 14.
	EBI_ADR15	O	EBI address bus bit 15.
	EBI_ADR16	O	EBI address bus bit 16.
	EBI_ADR17	O	EBI address bus bit 17.
	EBI_ADR18	O	EBI address bus bit 18.
	EBI_ADR19	O	EBI address bus bit 19.
	EBI_ALE	O	EBI address latch enable output pin.
	EBI_MCLK	O	EBI external clock output pin.
	EBI_nCS0	O	EBI chip select 0 output pin.
	EBI_nCS1	O	EBI chip select 1 output pin.
	EBI_nCS2	O	EBI chip select 2 output pin.

Group	Pin Name	Type	Description
	EBI_nRD	O	EBI read enable output pin.
	EBI_nWR	O	EBI write enable output pin.
	EBI_nWRH	O	EBI high byte write enable output pin
	EBI_nWRL	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
ECAP1	ECAP1_IC0	I	Enhanced capture unit 1 input 0 pin.
	ECAP1_IC1	I	Enhanced capture unit 1 input 1 pin.
	ECAP1_IC2	I	Enhanced capture unit 1 input 2 pin.
ECAP2	ECAP2_IC0	I	Enhanced capture unit 2 input 0 pin.
	ECAP2_IC1	I	Enhanced capture unit 2 input 1 pin.
	ECAP2_IC2	I	Enhanced capture unit 2 input 2 pin.
ECAP3	ECAP3_IC0	I	Enhanced capture unit 3 input 0 pin.
	ECAP3_IC1	I	Enhanced capture unit 3 input 1 pin.
	ECAP3_IC2	I	Enhanced capture unit 3 input 2 pin.
EMAC0	EMAC0_PPS	O	EMAC0 Pulse Per Second output pin.
	EMAC0_RMII_CRSDV	I	EMAC0 RMII Carrier Sense/Receive Data input pin.
	EMAC0_RMII_MDC	O	EMAC0 RMII PHY Management Clock output pin.
	EMAC0_RMII_MDIO	I/O	EMAC0 RMII PHY Management Data pin.
	EMAC0_RMII_REFCLK	I	EMAC0 RMII reference clock input pin.
	EMAC0_RMII_RXD0	I	EMAC0 RMII Receive Data bus bit 0.
	EMAC0_RMII_RXD1	I	EMAC0 RMII Receive Data bus bit 1.
	EMAC0_RMII_RXERR	I	EMAC0 RMII Receive Data Error input pin.
	EMAC0_RMII_TXD0	O	EMAC0 RMII Transmit Data bus bit 0.
	EMAC0_RMII_TXD1	O	EMAC0 RMII Transmit Data bus bit 1.
	EMAC0_RMII_TXEN	O	EMAC0 RMII Transmit Enable output pin.
EPWM0	EPWM0_BRAKE0	I	EPWM0 Brake 0 input pin.
	EPWM0_BRAKE1	I	EPWM0 Brake 1 input pin.
	EPWM0_CH0	I/O	EPWM0 channel 0 output/capture input.
	EPWM0_CH1	I/O	EPWM0 channel 1 output/capture input.

Group	Pin Name	Type	Description
	EPWM0_CH2	I/O	EPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	EPWM0 channel 3 output/capture input.
	EPWM0_CH4	I/O	EPWM0 channel 4 output/capture input.
	EPWM0_CH5	I/O	EPWM0 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	O	EPWM0 counter synchronous trigger output pin.
EPWM1	EPWM1_BRAKE0	I	EPWM1 Brake 0 input pin.
	EPWM1_BRAKE1	I	EPWM1 Brake 1 input pin.
	EPWM1_CH0	I/O	EPWM1 channel 0 output/capture input.
	EPWM1_CH1	I/O	EPWM1 channel 1 output/capture input.
	EPWM1_CH2	I/O	EPWM1 channel 2 output/capture input.
	EPWM1_CH3	I/O	EPWM1 channel 3 output/capture input.
	EPWM1_CH4	I/O	EPWM1 channel 4 output/capture input.
	EPWM1_CH5	I/O	EPWM1 channel 5 output/capture input.
EQEI0	EQEI0_A	I	EQEI0 phase A input.
	EQEI0_B	I	EQEI0 phase B input.
	EQEI0_INDEX	I	EQEI0 index input.
EQEI1	EQEI1_A	I	EQEI1 phase A input.
	EQEI1_B	I	EQEI1 phase B input.
	EQEI1_INDEX	I	EQEI1 index input.
EQEI2	EQEI2_A	I	EQEI2 phase A input.
	EQEI2_B	I	EQEI2 phase B input.
	EQEI2_INDEX	I	EQEI2 index input.
EQEI3	EQEI3_A	I	EQEI3 phase A input.
	EQEI3_B	I	EQEI3 phase B input.
	EQEI3_INDEX	I	EQEI3 index input.
ETMC	ETMC_TRACE_CLK	I	ETM receiver Trace Clock input pin.
	ETMC_TRACE_DATA0	I	ETM receiver Trace Data 0 input pin.
	ETMC_TRACE_DATA1	I	ETM receiver Trace Data 1 input pin.
	ETMC_TRACE_DATA2	I	ETM receiver Trace Data 2 input pin.
	ETMC_TRACE_DATA3	I	ETM receiver Trace Data 3 input pin.

Group	Pin Name	Type	Description
HSUSB	HSUSB_VBUS_EN	O	HSUSB external VBUS regulator enable pin.
	HSUSB_VBUS_ST	I	HSUSB external VBUS regulator status pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin.
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin.
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
	I2C2_SMBAL	O	I2C2 SMBus SMBALTER pin.
	I2C2_SMBSUS	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C3	I2C3_SCL	I/O	I2C3 clock pin.
	I2C3_SDA	I/O	I2C3 data input/output pin.
	I2C3_SMBAL	O	I2C3 SMBus SMBALTER pin.
	I2C3_SMBSUS	O	I2C3 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	O	I2S0 bit clock output pin.
	I2S0_DI	I	I2S0 data input pin.
	I2S0_DO	O	I2S0 data output pin.
	I2S0_LRCK	O	I2S0 left right channel clock output pin.
	I2S0_MCLK	O	I2S0 master clock output pin.
I2S1	I2S1_BCLK	O	I2S1 bit clock output pin.
	I2S1_DI	I	I2S1 data input pin.
	I2S1_DO	O	I2S1 data output pin.
	I2S1_LRCK	O	I2S1 left right channel clock output pin.
	I2S1_MCLK	O	I2S1 master clock output pin.
I3C0	I3C0_PUPEN	O	I3C0 pull-up resistor enable pin.
	I3C0_SCL	I/O	I3C0 serial clock pin.
	I3C0_SDA	I/O	I3C0 serial data pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin.

Group	Pin Name	Type	Description
			Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
INT6	INT6	I	External interrupt 6 input pin.
INT7	INT7	I	External interrupt 7 input pin.
KPI	KPI_COL0	I	Keypad Interface Column 0 input pin.
	KPI_COL1	I	Keypad Interface Column 1 input pin.
	KPI_COL2	I	Keypad Interface Column 2 input pin.
	KPI_COL3	I	Keypad Interface Column 3 input pin.
	KPI_COL4	I	Keypad Interface Column 4 input pin.
	KPI_COL5	I	Keypad Interface Column 5 input pin.
	KPI_COL6	I	Keypad Interface Column 6 input pin.
	KPI_COL7	I	Keypad Interface Column 7 input pin.
	KPI_ROW0	O	Keypad Interface Row 0 output pin.
	KPI_ROW1	O	Keypad Interface Row 1 output pin.
	KPI_ROW2	O	Keypad Interface Row 2 output pin.
	KPI_ROW3	O	Keypad Interface Row 3 output pin.
	KPI_ROW4	O	Keypad Interface Row 4 output pin.
	KPI_ROW5	O	Keypad Interface Row 5 output pin.
LPADC0	LPADC0_CH0	A	Low Power ADC0 channel 0 analog input.
	LPADC0_CH1	A	Low Power ADC0 channel 1 analog input.
	LPADC0_CH2	A	Low Power ADC0 channel 2 analog input.
	LPADC0_CH3	A	Low Power ADC0 channel 3 analog input.
	LPADC0_CH4	A	Low Power ADC0 channel 4 analog input.
	LPADC0_CH5	A	Low Power ADC0 channel 5 analog input.
	LPADC0_CH6	A	Low Power ADC0 channel 6 analog input.
	LPADC0_CH7	A	Low Power ADC0 channel 7 analog input.
	LPADC0_CH8	A	Low Power ADC0 channel 8 analog input.
	LPADC0_CH9	A	Low Power ADC0 channel 9 analog input.
	LPADC0_CH10	A	Low Power ADC0 channel 10 analog input.

Group	Pin Name	Type	Description
	LPADC0_CH11	A	Low Power ADC0 channel 11 analog input.
	LPADC0_CH12	A	Low Power ADC0 channel 12 analog input.
	LPADC0_CH13	A	Low Power ADC0 channel 13 analog input.
	LPADC0_CH14	A	Low Power ADC0 channel 14 analog input.
	LPADC0_CH15	A	Low Power ADC0 channel 15 analog input.
	LPADC0_CH16	A	Low Power ADC0 channel 16 analog input.
	LPADC0_CH17	A	Low Power ADC0 channel 17 analog input.
	LPADC0_CH18	A	Low Power ADC0 channel 18 analog input.
	LPADC0_CH19	A	Low Power ADC0 channel 19 analog input.
	LPADC0_CH20	A	Low Power ADC0 channel 20 analog input.
	LPADC0_CH21	A	Low Power ADC0 channel 21 analog input.
	LPADC0_CH22	A	Low Power ADC0 channel 22 analog input.
	LPADC0_CH23	A	Low Power ADC0 channel 23 analog input.
	LPADC0_ST	I	Low Power ADC0 external trigger input pin.
LPI2C0	LPI2C0_SCL	I/O	Low Power I2C0 clock pin.
	LPI2C0_SDA	I/O	Low Power I2C0 data input/output pin.
LPIO0	LPIO0	I	Low Power I/O 0 input pin.
LPIO1	LPIO1	I	Low Power I/O 1 input pin.
LPIO2	LPIO2	I	Low Power I/O 2 input pin.
LPIO3	LPIO3	I	Low Power I/O 3 input pin.
LPIO4	LPIO4	I	Low Power I/O 4 input pin.
LPIO5	LPIO5	I	Low Power I/O 5 input pin.
LPIO6	LPIO6	I	Low Power I/O 6 input pin.
LPIO7	LPIO7	I	Low Power I/O 7 input pin.
LPSPI0	LPSPI0_CLK	I/O	Low Power SPI0 serial clock pin.
	LPSPI0_MISO	I/O	Low Power SPI0 MISO (Master In, Slave Out) pin.
	LPSPI0_MOSI	I/O	Low Power SPI0 MOSI (Master Out, Slave In) pin.
	LPSPI0_SS	I/O	Low Power SPI0 slave select pin.
LPTM0	LPTM0	I/O	Low Power Timer0 event counter input/toggle output pin.
	LPTM0_EXT	I/O	Low Power Timer0 external capture input/toggle output pin.
LPTM1	LPTM1	I/O	Low Power Timer1 event counter input/toggle output pin.
	LPTM1_EXT	I/O	Low Power Timer1 external capture input/toggle output pin.
LPUART0	LPUART0_RXD	I	Low Power UART0 data receiver input pin.
	LPUART0_TXD	O	Low Power UART0 data transmitter output pin.

Group	Pin Name	Type	Description
	LPUART0_nCTS	I	Low Power UART0 clear to Send input pin.
	LPUART0_nRTS	O	Low Power UART0 request to Send output pin.
PSIO0	PSIO0_CH0	I/O	PSIO 0 channel 0 input/output pin.
	PSIO0_CH1	I/O	PSIO 0 channel 1 input/output pin.
	PSIO0_CH2	I/O	PSIO 0 channel 2 input/output pin.
	PSIO0_CH3	I/O	PSIO 0 channel 3 input/output pin.
	PSIO0_CH4	I/O	PSIO 0 channel 4 input/output pin.
	PSIO0_CH5	I/O	PSIO 0 channel 5 input/output pin.
	PSIO0_CH6	I/O	PSIO 0 channel 6 input/output pin.
	PSIO0_CH7	I/O	PSIO 0 channel 7 input/output pin.
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
QSPI1	QSPI1_CLK	I/O	Quad SPI1 serial clock pin.
	QSPI1_MISO0	I/O	Quad SPI1 MISO0 (Master In, Slave Out) pin.
	QSPI1_MISO1	I/O	Quad SPI1 MISO1 (Master In, Slave Out) pin.
	QSPI1_MOSI0	I/O	Quad SPI1 MOSI0 (Master Out, Slave In) pin.
	QSPI1_MOSI1	I/O	Quad SPI1 MOSI1 (Master Out, Slave In) pin.
	QSPI1_SS	I/O	Quad SPI1 slave select pin.
SC0	SC0_CLK	O	Smart Card 0 clock pin.
	SC0_DAT	I/O	Smart Card 0 data pin.
	SC0_PWR	O	Smart Card 0 power pin.
	SC0_RST	O	Smart Card 0 reset pin.
	SC0_nCD	I	Smart Card 0 card detect pin.
SC1	SC1_CLK	O	Smart Card 1 clock pin.
	SC1_DAT	I/O	Smart Card 1 data pin.
	SC1_PWR	O	Smart Card 1 power pin.
	SC1_RST	O	Smart Card 1 reset pin.
	SC1_nCD	I	Smart Card 1 card detect pin.
SC2	SC2_CLK	O	Smart Card 2 clock pin.
	SC2_DAT	I/O	Smart Card 2 data pin.

Group	Pin Name	Type	Description
	SC2_PWR	O	Smart Card 2 power pin.
	SC2_RST	O	Smart Card 2 reset pin.
	SC2_nCD	I	Smart Card 2 card detect pin.
SD0	SD0_CLK	O	SD/SDIO0 clock output pin
	SD0_CMD	I/O	SD/SDIO0 command/response pin
	SD0_DAT0	I/O	SD/SDIO0 data line bit 0.
	SD0_DAT1	I/O	SD/SDIO0 data line bit 1.
	SD0_DAT2	I/O	SD/SDIO0 data line bit 2.
	SD0_DAT3	I/O	SD/SDIO0 data line bit 3.
	SD0_nCD	I	SD/SDIO0 card detect input pin
SD1	SD1_CLK	O	SD/SDIO1 clock output pin
	SD1_CMD	I/O	SD/SDIO1 command/response pin
	SD1_DAT0	I/O	SD/SDIO1 data line bit 0.
	SD1_DAT1	I/O	SD/SDIO1 data line bit 1.
	SD1_DAT2	I/O	SD/SDIO1 data line bit 2.
	SD1_DAT3	I/O	SD/SDIO1 data line bit 3.
	SD1_nCD	I	SD/SDIO1 card detect input pin
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
SPI2	SPI2_CLK	I/O	SPI2 serial clock pin.
	SPI2_I2SMCLK	I/O	SPI2 I2S master clock output pin
	SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin.
	SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin.
	SPI2_SS	I/O	SPI2 slave select pin.
SPI3	SPI3_CLK	I/O	SPI3 serial clock pin.
	SPI3_I2SMCLK	I/O	SPI3 I2S master clock output pin

Group	Pin Name	Type	Description
	SPI3_MISO	I/O	SPI3 MISO (Master In, Slave Out) pin.
	SPI3_MOSI	I/O	SPI3 MOSI (Master Out, Slave In) pin.
	SPI3_SS	I/O	SPI3 slave select pin.
SPIM0	SPIM0_CLK	I/O	SPIM serial clock pin.
	SPIM0_CLKN	O	SPIM0 serial clock # pin.
	SPIM0_D2	I/O	SPIM0 data 2 pin for Quad Mode I/O.
	SPIM0_D3	I/O	SPIM0 data 3 pin for Quad Mode I/O.
	SPIM0_D4	I/O	SPIM0 data 4 pin for Quad Mode I/O.
	SPIM0_D5	I/O	SPIM0 data 5 pin for Quad Mode I/O.
	SPIM0_D6	I/O	SPIM0 data 6 pin for Quad Mode I/O.
	SPIM0_D7	I/O	SPIM0 data 7 pin for Quad Mode I/O.
	SPIM0_MISO	I/O	SPIM MISOO (Master In, Slave Out) pin.
	SPIM0_MOSI	I/O	SPIM MOSII (Master Out, Slave In) pin.
	SPIM0_RESETN	O	SPIM0 reset # output pin.
	SPIM0_RWDS	I/O	SPIM0 Read Write Data Strobe pin.
	SPIM0_SS	I/O	SPIM slave select S pin.
SWDH	SWDH_CLK	O	Serial Wire Debug Host Clock output.
	SWDH_DAT	I/O	Serial Wire Debug Host Data input/output pin.
SWODEC	SWODEC_SWO	I	SWODEC Data input pin.
TAMPER0	TAMPER0	I/O	TAMPER detector loop pin 0.
TAMPER1	TAMPER1	I/O	TAMPER detector loop pin 1.
TAMPER2	TAMPER2	I/O	TAMPER detector loop pin 2.
TAMPER3	TAMPER3	I/O	TAMPER detector loop pin 3.
TAMPER4	TAMPER4	I/O	TAMPER detector loop pin 4.
TAMPER5	TAMPER5	I/O	TAMPER detector loop pin 5.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TRACE	TRACE_CLK	O	ETM Trace Clock output pin.

Group	Pin Name	Type	Description
	TRACE_DATA0	O	ETM Trace Data 0 output pin.
	TRACE_DATA1	O	ETM Trace Data 1 output pin.
	TRACE_DATA2	O	ETM Trace Data 2 output pin.
	TRACE_DATA3	O	ETM Trace Data 3 output pin.
	TRACE_SWO	O	Trace Single Wire output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
UART4	UART4_RXD	I	UART4 data receiver input pin.
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
UART5	UART5_RXD	I	UART5 data receiver input pin.
	UART5_TXD	O	UART5 data transmitter output pin.
	UART5_nCTS	I	UART5 clear to Send input pin.
	UART5_nRTS	O	UART5 request to Send output pin.
UART6	UART6_RXD	I	UART6 data receiver input pin.
	UART6_TXD	O	UART6 data transmitter output pin.
	UART6_nCTS	I	UART6 clear to Send input pin.
	UART6_nRTS	O	UART6 request to Send output pin.
UART7	UART7_RXD	I	UART7 data receiver input pin.

Group	Pin Name	Type	Description
	UART7_TXD	O	UART7 data transmitter output pin.
	UART7_nCTS	I	UART7 clear to Send input pin.
	UART7_nRTS	O	UART7 request to Send output pin.
UART8	UART8_RXD	I	UART8 data receiver input pin.
	UART8_TXD	O	UART8 data transmitter output pin.
	UART8_nCTS	I	UART8 clear to Send input pin.
	UART8_nRTS	O	UART8 request to Send output pin.
UART9	UART9_RXD	I	UART9 data receiver input pin.
	UART9_TXD	O	UART9 data transmitter output pin.
	UART9_nCTS	I	UART9 clear to Send input pin.
	UART9_nRTS	O	UART9 request to Send output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_OTG_ID	I	USB_ identification.
	USB_VBUS	P	Power supply from USB host or HUB.
	USB_VBUS_EN	O	USB external VBUS regulator enable pin.
	USB_VBUS_ST	I	USB external VBUS regulator status pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
UTCPD0	UTCPD0_CC1	A	UTCPD0 USB Type-C Configuration Channel pin 1.
	UTCPD0_CC2	A	UTCPD0 USB Type-C Configuration Channel pin 2.
	UTCPD0_CCDB1	A	UTCPD0 USB Type-C Dead Battery pin 1.
	UTCPD0_CCDB2	A	UTCPD0 USB Type-C Dead Battery pin 2.
	UTCPD0_DISCHG	O	UTCPD0 VCONN Discharge Enable output pin.
	UTCPD0_FRSTX1	O	UTCPD0 CC1 Fast Role Swap Transmit output pin.
	UTCPD0_FRSTX2	O	UTCPD0 CC2 Fast Role Swap Transmit output pin.
	UTCPD0_VBDCHG	O	UTCPD0 VBUS Discharge Enable output pin.
	UTCPD0_VBSNKEN	O	UTCPD0 VBUS Sink Enable output pin.
	UTCPD0_VBSRCEN	O	UTCPD0 VBUS Source Enable output pin.
	UTCPD0_VCNEN1	O	UTCPD0 CC1 VCONN Enable output pin.

Group	Pin Name	Type	Description
	UTCPD0_VCNEN2	O	UTCPD0 CC2 VCONN Enable output pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
USB	HSUSB_D+	A	HSUSB differential signal D+.
	HSUSB_D-	A	HSUSB differential signal D-.
	HSUSB_ID	I	HSUSB identification.
	HSUSB_VBUS	I/O	HSUSB Power supply from USB host or HUB.
	HSUSB_VDD11	P	Power supply for HSUSB VDD11.
	HSUSB_VDD33	P	Power supply for HSUSB VDD33.
	HSUSB_VRES	A	HSUSB module reference resister.
	HSUSB_VSS	P	Ground pin for HSUSB.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. **Note:** This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	NC	-	No connect pin, leave floating.
	V_{BAT}	P	Power supply by batteries for RTC.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{DDIO0}	P	Power supply for I/O group 0.
	V_{DDIO1}	P	Power supply for I/O group 1.
	V_{REF}	A	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	V_{SW}	P	Inductor for DC-DC Buck Converter. **Note:** This pin needs to be connected with a inductor whose value can be found in General operating conditions table in Datasheet.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

5 BLOCK DIAGRAM

5.1 M55M1 Series Block Diagram

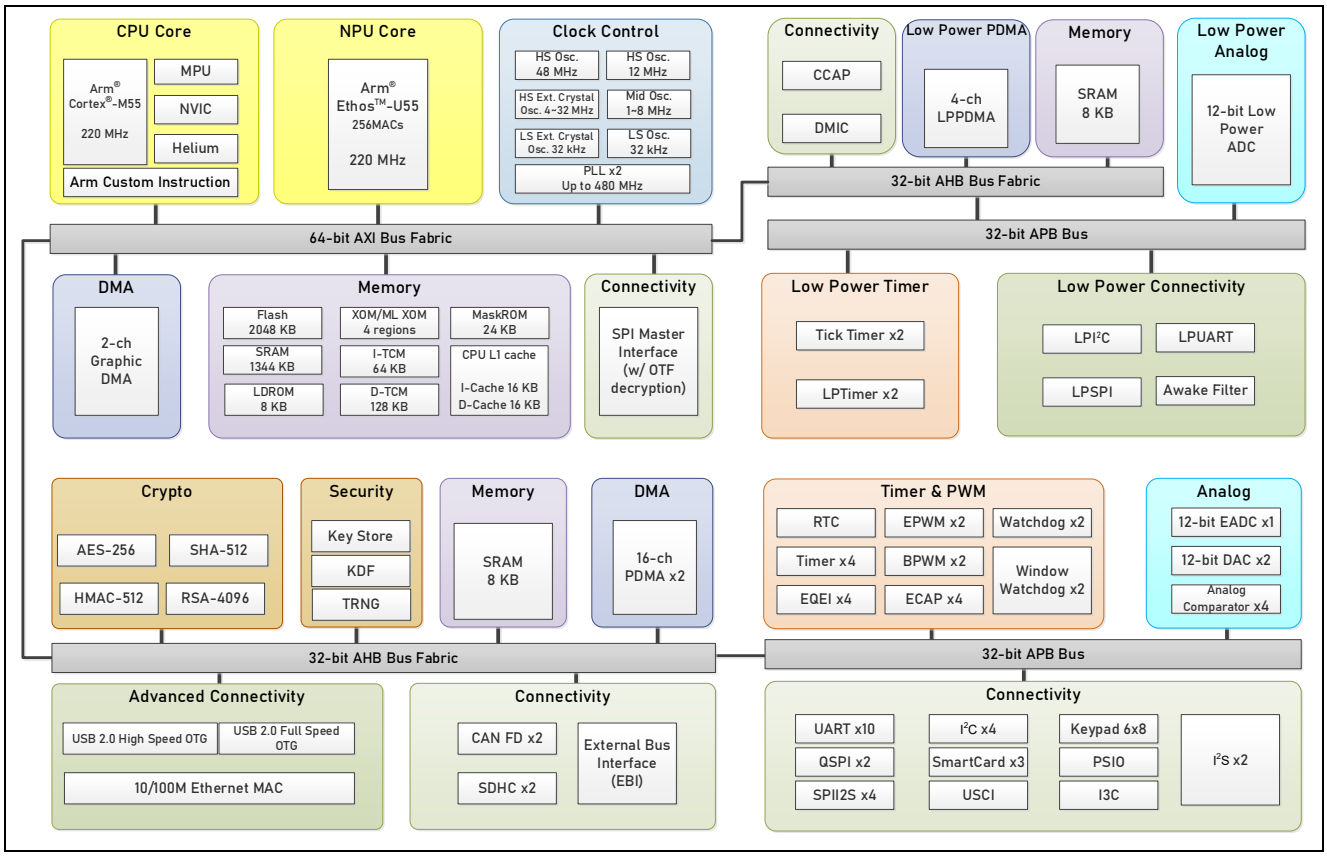


Figure 5.1-1 M55M1 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M55 Core

The M55M1 series contains the Cortex-M55 processor that implements the Armv8.1-M Mainline architecture. It features the M-class Vector Extension (MVE, which is also referred to as Arm Helium technology) that supports compute applications, such as Digital Signal Procession (DSP) and Machine Learning. MVE adds over 150 new scalar and vector instructions and eight 128-bit vector registers. Each MVE operation can handle four 32-bit data (integer or single precision floating-point data) or eight 16-bit data (integer or half precision floating-point data) or sixteen 8-bit data (integer). Another caracheristic is TrustZone Security Extension, which supports Secure and Non-secure states on all memory interfaces. Memory and peripherals in the system can be marked as Secure, making them accessible only to code that is running in the Secure state. The Security Extension adds security through code and data protection features. This processor also supports previous Armv8-M architectural features. Figure 6.1-1 shows the functional controller of the processor. For more detail of Cortex-M55, please see the Arm® Cortex®-M55 Processor Technical Reference Manual.

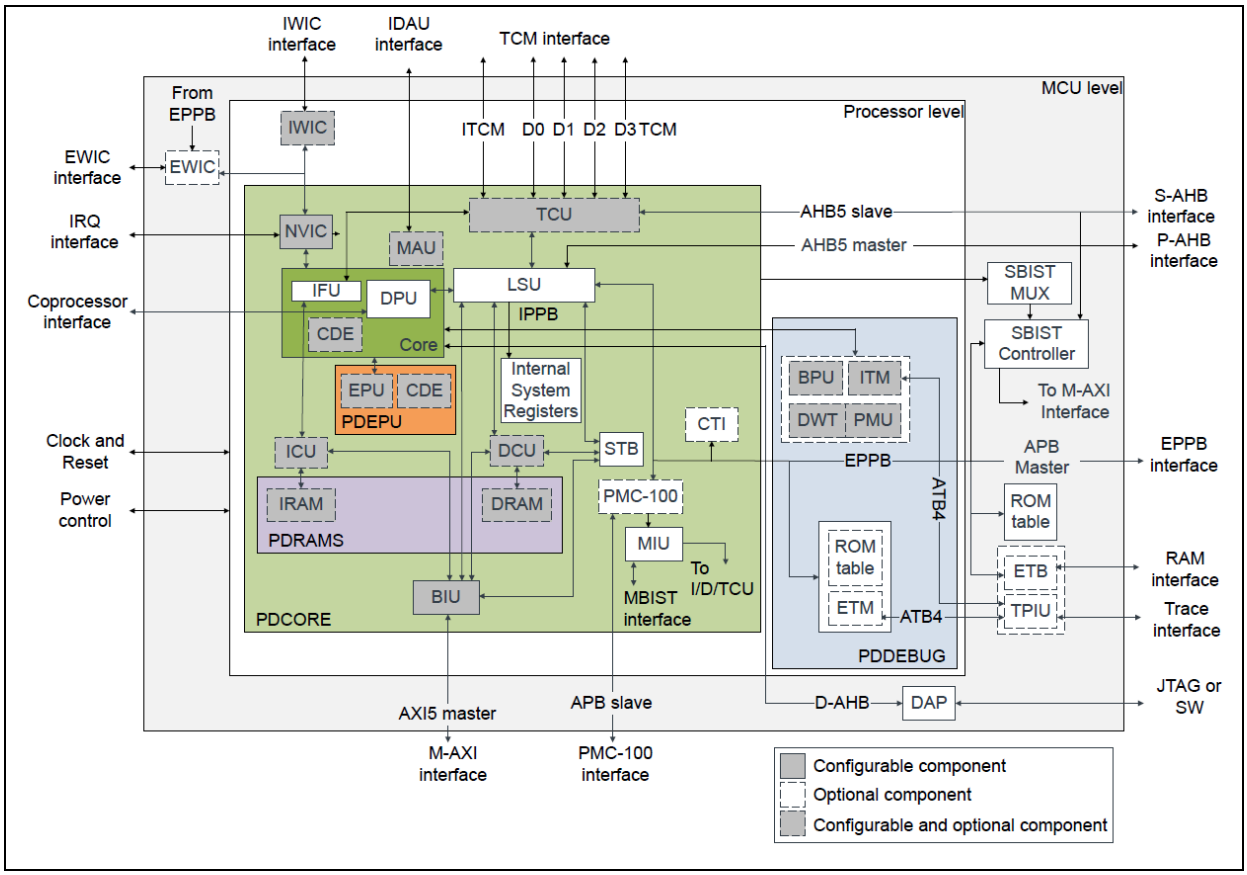


Figure 6.1-1 Cortex-M55 Block Diagram

With the help of Arm Custom Instructions (ACIs) Extension, the Cortex-M55 processor in the M55M1 series also supports 10-cycle sine/cosine calculation instruction. For more information of how to use the ACI, please refer to the sample code provided in our Board Support Package (BSP).

Here is a quick summary of the key characteristics of the Cortex-M55 processor in the M55M1.

- Armv8.1-M architecture with support for:
  - Helium vector processing
  - Floating-point Unit (FPU) with support for multiple floating-point formats
- TrustZone security extension

- Advanced memory system features including caches (16KB I/D-cache) and tightly coupled memory (64KB I-TCM and 128KB D-TCM) support
- Secure and Non-secure Memory Protection Units (MPU) with 8 MPU regions for each of them
- Up to 480 interrupts and non-maskable interrupt (NMI), with 16 levels of programmable priority levels
- Arm Custom Instructions (sine/cosine calculation)
- Various debug feature enhancements including new Performance Monitoring Unit (PMU)

6.2 Arm® TrustZone®

The Arm® TrustZone® can be considered as a physical partition that divides the microcontroller into **Secure** (Trusted) and **Non-secure** (Non-trusted) worlds according to memory address. The secure world is an isolated execution environment, where code and data inside are protected and cannot be accessed from Non-secure world. Code running at secure world is called secure code that can access both secure and non-secure memories and peripherals; while code running at non-secure world is called non-secure code that can only access non-secure memories and peripherals.

Figure 6.2-1 shows an example of a system divided into the secure world and non-secure world. Green blocks indicate secure components, Red blocks indicate non-secure components and white ones are both/either secure and/or non-secure accessible. When the core processor is in secure state (left side of the figure), it belongs to secure world, which has its own MSP, PSP and VTOR registers and can access the green, red, white blocks. Contrarily, when the core processor is in non-secure state (right side of the figure), it belongs to non-secure world, which also has its own MSP, PSP and VTOR registers, but, it can only access red and white blocks so that non-secure world components are not able to impact secure world.

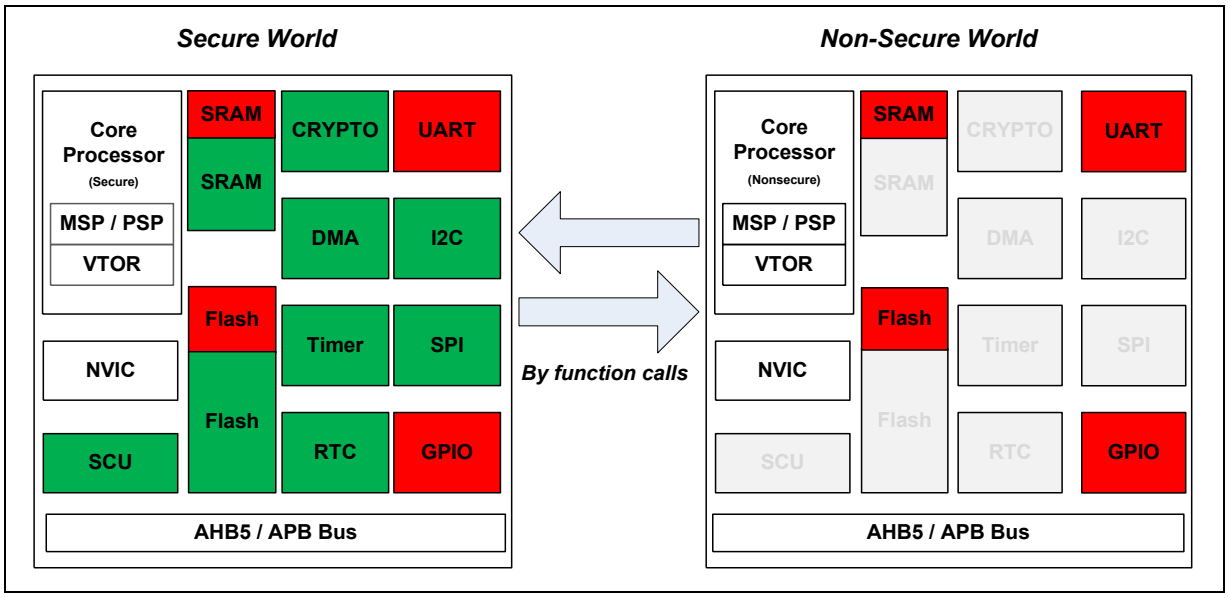


Figure 6.2-1 Secure World View and Non-secure World View on a Chip

To support Arm® TrustZone®, there are two parts should be considered: one is the address space partition of a master/processor view; the other is the security attribute of a slave/peripheral.

The address space is the space that a master/processor view a system. It should be partitioned to targeted world (Secure or Non-secure) with correct attribute (NS, S, NSC). The “Address Space Partition” section will give detailed description of the partitioning.

Each slave/peripheral has its own security attribute, indicating which world the slave/peripheral belongs to. The “6.2.2.4 Address Space Security Check of Processor” section will give detailed description of setting the security attribute of the slave.

To make the Trustzone correct, correct address space partitioning and correct security attribute configuration are essential, the secure software should take charge of the correctness of these settings.

Whenever being cold reset, the whole system of the chip is in secure state, that is, the core processor, RAM and peripherals are all in secure state. Therefore, the system boots in secure state. The boot code is responsible to set up TrustZone® related control units to partition address space and assign non-secure resources for non-secure world.

6.2.1 Address Space Partition

Arm Cortex-M® Trustzone® defines three types of security attributes. Each memory address is assigned with one of the security attributes. These security attributes are listed below.

- Non-secure (NS)
  Addresses used for non-secure memory or non-secure peripheral's registers.
- Secure (S)
  Addresses used for secure memory or secure peripheral's registers.
- Non-secure Callable (NSC)
  A special type of secure memory region which can contain SG instructions. The SG instruction allows a non-secure function calls to a secure function.

The address space partitioning, a process to assign the security attributes of a region of address space, is completed by Implementation Define Attribution Unit (IDAU) and Security Attribution Unit (SAU) together.

The IDAU is non-programmable, and defines static partitions and their security attribute of address space. i.e. IDAU specifies the default security attribute of all regions of address space.

In contrast with IDAU, the SAU is programmable and provides dynamic partitions of address space, which is set by software programmer. SAU is for software programmer to overwrite the default security attribute of regions defined by IDAU to a new one, depending on the demend.

For setting IDAU and SAU, refer to sections “Implementation Define Attribution Unit (IDAU)” and “Security Attribution Unit (SAU)” for more details.

Each memory region defined by the SAU and IDAU has a region number generated by the SAU and by the IDAU. Region number is used for determining a group of memory share the same security attribute. Overlapping region numbers are not allowed. To test the security attribute and region number of a given address, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine that the memory range is located entirely in same space. Refer to the Arm®v8-M Architecture Reference Manual for more details.

6.2.2 Implementation Define Attribution Unit (IDAU)

6.2.2.1 IDAU Block Diagram

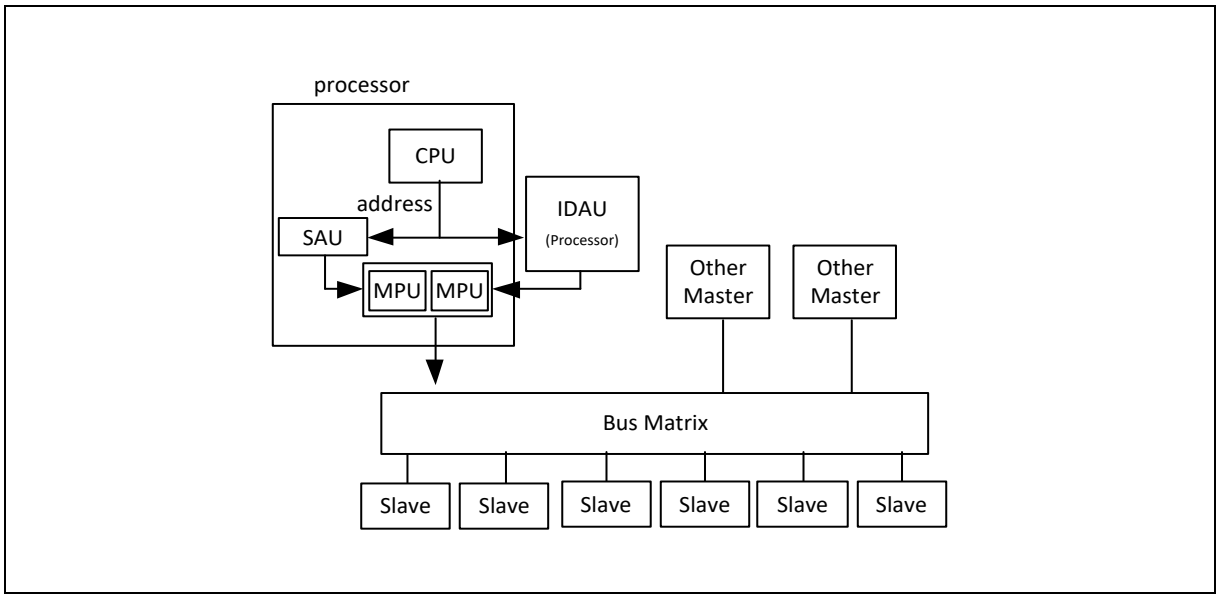


Figure 6.2-2 IDAU Block Diagram of CPU

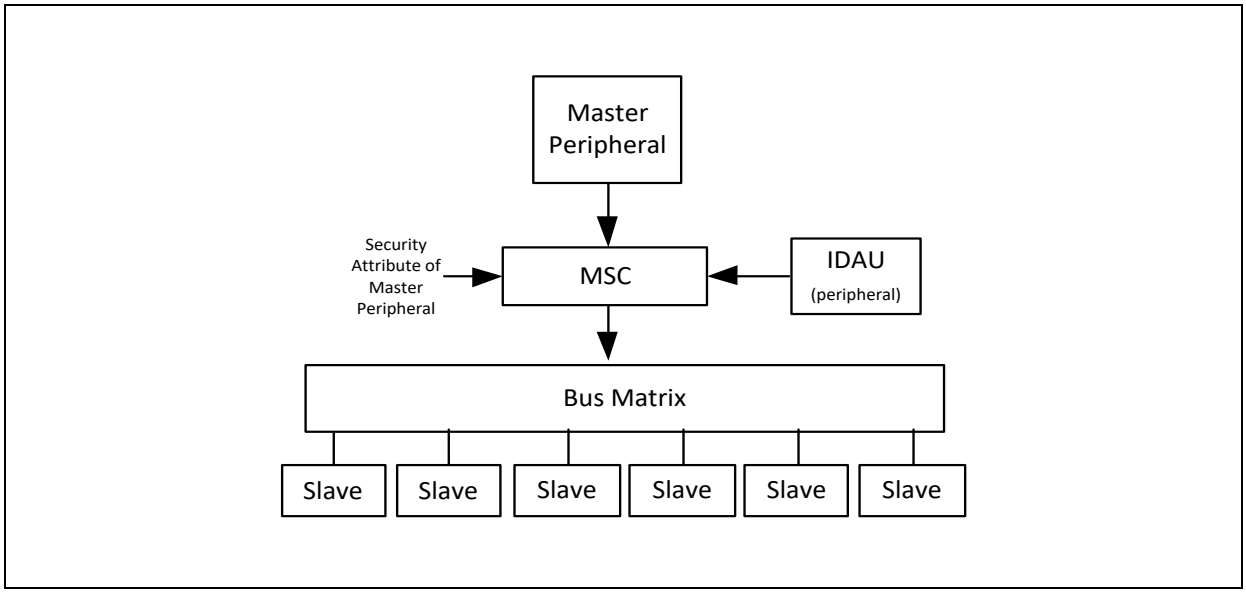


Figure 6.2-3 IDAU Block Diagram of Master Peripheral

The IDAU block diagram of processor is shown in Figure 6.4-11. IDAU is a security attribute unit connected to the processor and provides the attribute of the address the processor is going to access.

The IDAU block diagram of master peripheral is shown in Figure 6.2-3. This chip utilizes AHB5 TrustZone master security controller (MSC) module connected to a master peripheral to do the security check of the address the master peripheral is going to access. IDAU of master peripheral is the module connected to MSC to provide the attribute of the address.

6.2.2.2 Functional Description

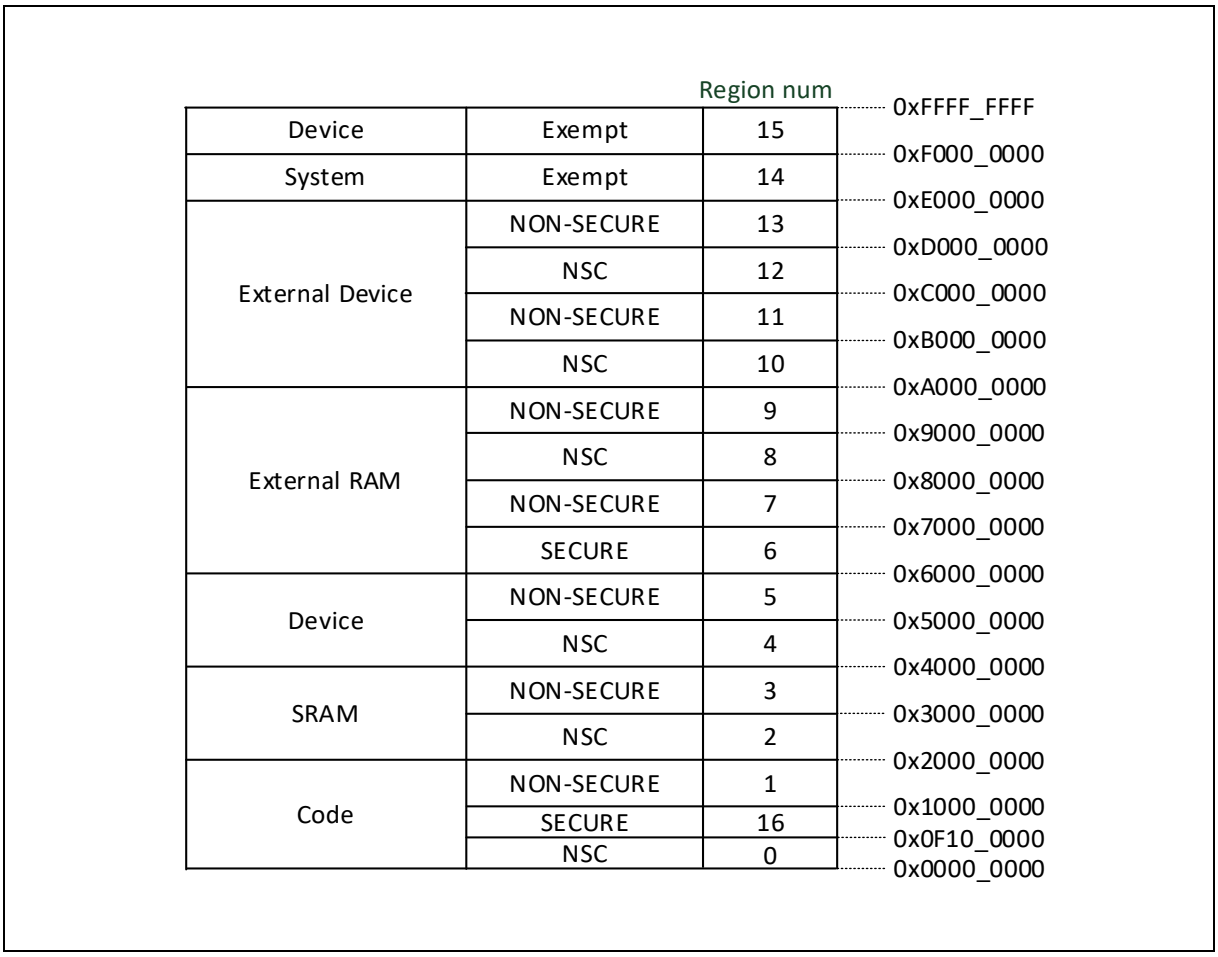


Figure 6.2-4 The Address Space of Processor Partitioned by IDAU

The IDAU uses address bit 28 to distinguish between secure and non-secure world. The bit 28 of a secure address is always 0, and the bit 28 of a non-secure address is always 1, except regions above 0xE000_0000 which is defined as exempt region.

The partition of the processor 4GB address space is shown as Figure 6.2-4. Each region consists of a **S** (bit 28 is 0) and a **NS** (bit 28 is 1) sub-regions, the size of a sub-region is 256 Mbytes. In order to store entry functions for non-secure code, the security attribute of secure SRAM region is assigned as **NSC**. Similarly, the secure “Code” region is assigned as **NSC** except the first 2 KB area. This first 2 KB area (0x0000_0000~0x0000_0800) is defined as **S** to avoid accidental **SG** instruction after power on.

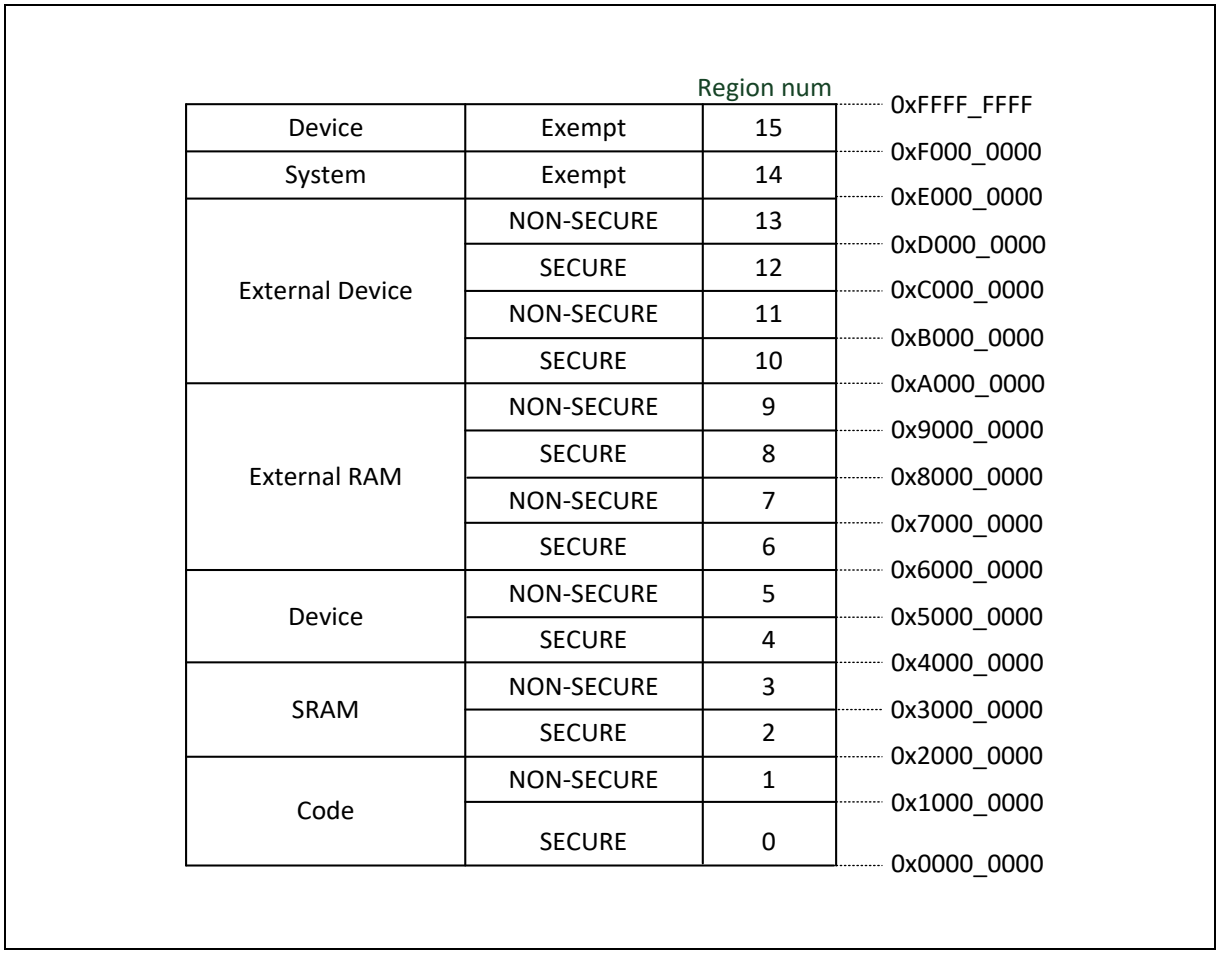


Figure 6.2-5 The Address Space of Master Peripheral Partitioned by IDAU

Apart from the processor, the master peripherals also need IDAU to partition their address space. Unlike the process which can execute instruction, the master peripheral, in general, can only access data in its address space. Thus, the partitions of address space of a peripheral master don't need **NSC** region but only needs **S** and **NS** regions. As shown in Figure 6.2-5, the address space of a peripheral master is purely partitioned to **S** region and **NS** region by address bit 28.

6.2.2.3 Security Attribution Unit (SAU)

The SAU is a MPU-like function unit inside the Cortex-M processor. Up to 8 memory regions can be defined by programming SAU control registers.

Memory regions are enabled individually by programming SAU_RNR, SAU_RBAR and SAU_RLAR. The memory region is enabled once RENABLE (SAU_RLAR[0]) is set to 1, and the security attribute is defined by NSC (SAU_RLAR[1]):

- NSC = 0, the memory region is Non-secure (NS).
- NSC = 1, the memory region is Secure and Non-secure callable (NSC).

The security attribute of each memory region defined by SAU is either NS or NSC. Those memory addresses not defined by SAU regions are treated as Secure. After all memory regions are set, SAU_CTRL[0] should be set to 1 to enable SAU.

Both IDAU and SAU define the security attribute of a memory address. If the definitions are different, the more secure attribute will be used for the memory address. The priority of the security attribute from high to low is Secure > NSC > NS.

When the core processor attempts to access a target, e.g. a memory or peripheral register, the security attribute of the target is decided by checking IDAU and SAU. If the core processor is non-secure but the target is secure, a HardFault exception will be generated. Because non-specified memory addresses are treated as secure, non-secure memory regions need to be defined for the core processor to access non-secure memory and non-secure peripheral registers. Besides, whole secure code and SRAM regions are defined as NSC by IDAU. The size of NSC regions can be changed according to the NSC entry functions included in application code. The example usage of SAU regions is shown as Figure 6.2-6.

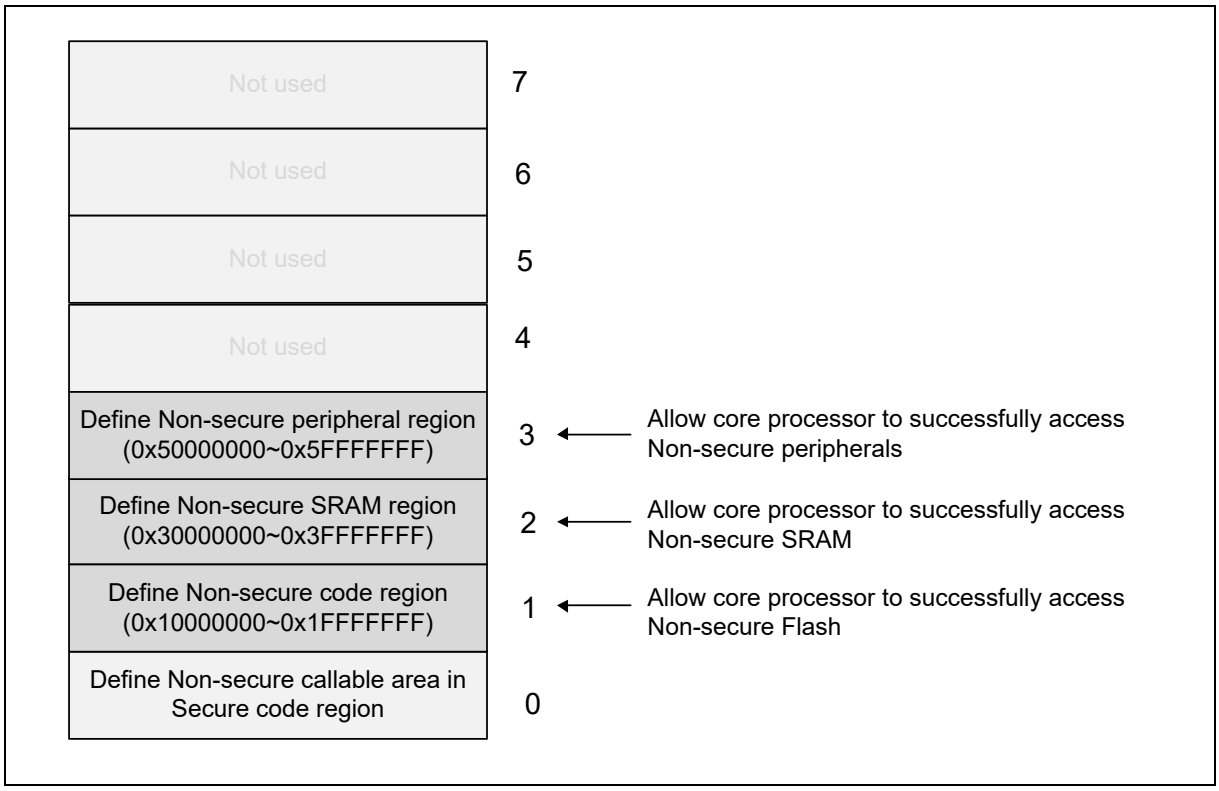


Figure 6.2-6 Typical Setting of SAU

6.2.2.4 *Address Space Security Check of Processor*

Each time the processor issues an access, including instruction access and data access, the targeted address of the access is sent to IDAU and SAU. The IDAU will return the security attribute of the targeted address to the processor, which is one of S, NSC, NS and Exempt. Combined the IDAU and SAU, the logic in the processor will do the security check. The policy of the security check is listed below:

- For instruction fetch, if the processor is in secure state, the security check is fail when the targeted address is **NS**.
- For instruction fetch, if the processor is in non-secure state, the security check is fail when the targeted address is **S**.
- For data access, if the processor is in secure state, the security check is pass for all kinds of targeted address.
- For data access If the processor is in non-secure state, the security check is pass only when the targeted address

Summary of the policy is listed in Table 6.2-1.

CPU state and access type	**Security Attribute of Target Address**		
	Secure (S)	**NSC**	**Non-secure (NS)**
Secure state instruction fetch	Pass	Pass	Fail
Secure state data access	Pass	Pass	Pass
Non-secure state instruction fetch	Fail	Pass	Pass
Non-secure state data access	Fail	Fail	Pass

Table 6.2-1 Summary of Processor Address Space Security Check

This address space security check is part of the whole security check, refer to section “Valid Access vs. Invalid Access” for more details.

6.2.2.5 *Address Space Security Check of Master Peripheral*

The address space security check of master peripheral is done by Arm MSC. Each time the peripheral sends an access, the MSC will forward the targeted address of the access to IDAU, and judge whether the access is valid or not based on the security attribute of targeted address from IDAU and the security attribute of this master.

The policy of master peripheral security check is shown as Table 6.2-2. In general, MSC will block the access only when the master is non-secure but the targeted address is **S**. Otherwise, the access will be transfer to the target slave. Another security check will be execute on the slave side, refer to “Valid Access vs. Invalid Access” for more details.

Master Peripheral Security Attribute	**Security Attribute of Target Address**		
	Secure (S)	**Non-secure (NS)**	**Exempt**
Secure	Pass	Pass	Pass
Non-secure	Fail	Pass	Pass

Table 6.2-2 Summary of Master Peripheral Address Space Security Check

6.2.3 Security Attribute Configuration

The previous section describes how to divide the address space of core processor view into secure world and non-secure world. In this chip, the memory and peripherals can be assigned to either secure or non-secure world during system initialization.

This chip is designed to start execution in secure state after reset. In other words, core processor and all system resources including SRAM and peripherals are secure after reset. Then, the system initialization code may change some parts of the system resources to be non-secure.

6.2.3.1 Security Attribute Configuration of Flash

The Flash memory is split into a number of different regions such as LDROM, APROM and others. Most of the Flash regions are always secure and cannot be changed. The only one can be changed is the APROM region. Non-secure APROM region is set by programming a special control register, NSCBA (Non-secure base address). The NSCBA[23:0] indicates the starting address of non-secure APROM and its value should be aligned with a Flash page size. The secure APROM region starts from address 0x0 and ends at NSCBA[23:0] – 1, while the non-secure APROM region ranges from NSCBA[23:0] to the end of APROM. For setting NSCBA, refer to FMC section for more details.

6.2.3.2 Security Attribute Configuration of SRAM and Peripherals

The security attribute of SRAM blocks and all peripherals can be configured by Security Configuration Unit (SCU), which contains a set of control registers used to assign the security attribute. Besides, the SCU monitors bus transfers to detect unsecure access. The unsecure access is one of the following conditions.

- Non-secure master peripheral tries to access a secure address (address bit 28 = 0).
- Secure code or secure master peripheral uses non-secure address (address bit 28 = 1) to access secure SRAM or peripheral.

When an unsecure access is detected, SCU blocks the access operation and generates a secure alarm interrupt.

For more details, refer to the Security Configuration Unit (SCU) chapter.

6.2.4 System Address Map and Access Scheme

The Trustzone architecture of this chip allows the Flash, SRAM and most peripherals to be assigned to Secure or Non-secure, but most of them can be accessed through either Secure address or Non-secure address depending on its security attribute configuration. Core processor and master peripherals should use correct address to access resources, i.e. the secure resource should be accessed via secure address. Similarly, the non-secure resource should be accessed via non-secure address.

6.2.4.1 Secure Address vs. Non-secure Address

A memory or a peripheral register may have secure and non-secure address in system address map, but the memory or register only responds to the address that is consistent with its security attribute. The different access modes of secure and non-secure target are illustrated in Figure 6.2-7.

Suppose that SRAM block 0, 2, and 4 are set to secure, they will respond to an access when address bit 28 is 0 (secure address), but will not respond to an access with address bit 28 is 1 (non-secure address). In this example, SRAM block 1 and 3 are in non-secure state. Hence, these blocks will only respond to an access when the address bit 28 is 1.

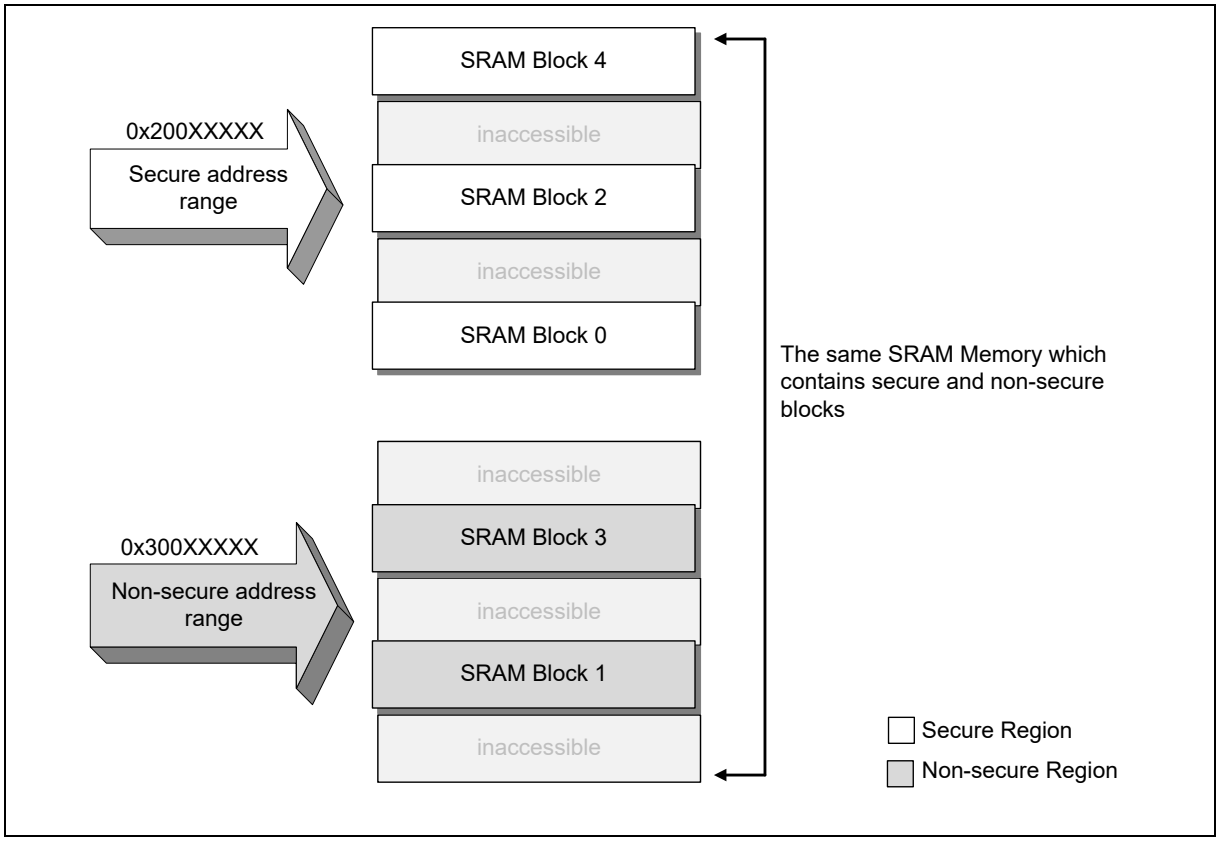


Figure 6.2-7 Example of SRAM Divided Into Secure Block and Non-secure Block

6.2.4.2 Valid Access vs. Invalid Access

When core processor or a master peripheral is trying to access (read or write) a memory or register, the result depends on the following conditions.

- Non-secure code or master peripheral is not allowed to access a secure memory or register.
- A memory or register only responds to the related address which is consistent with its security attribute.

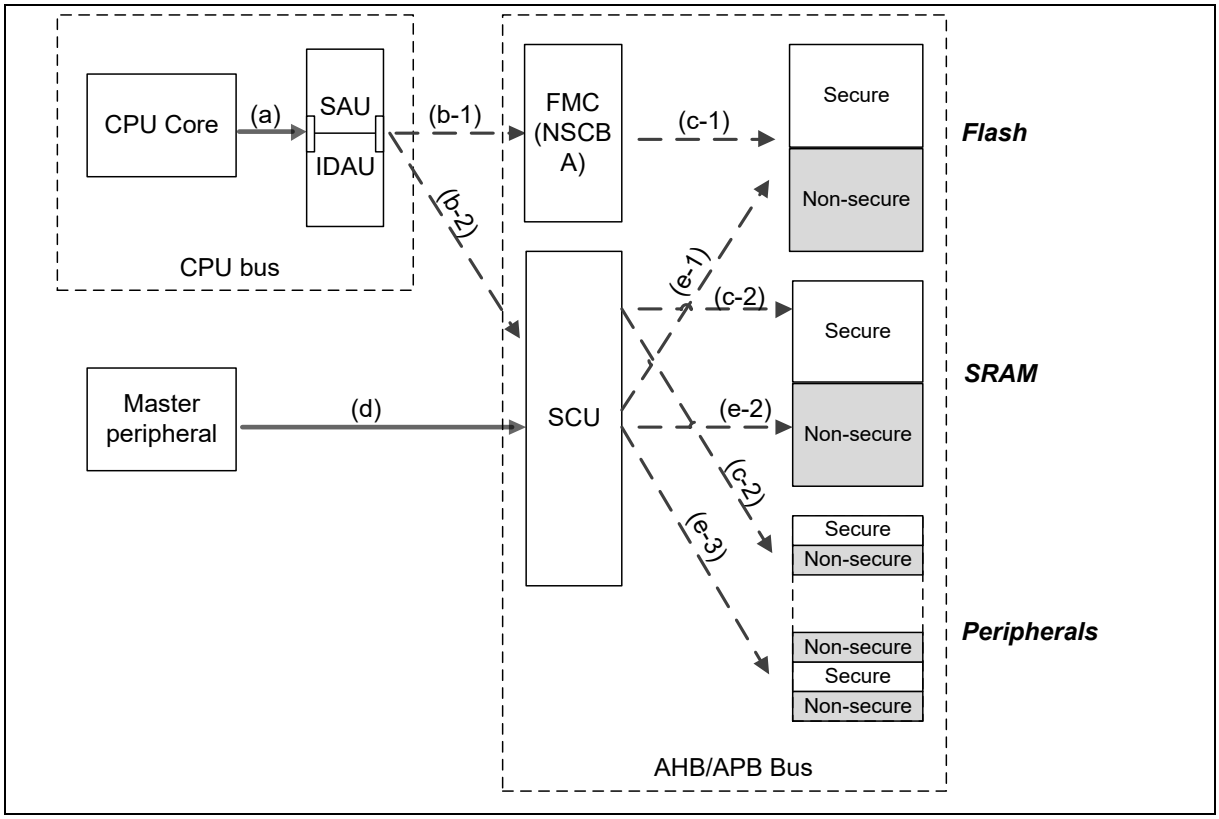


Figure 6.2-8 Checking Point of Accesses

Figure 6.2-8 illustrates how the above conditions are checked by TrustZone® related control units.

When the core processor tries to fetch instructions or access data, the security attribute of the core processor and target address are verified by SAU and IDAU (refer to (a)). If the core processor is in non-secure state and target address is secure, a hard fault exception will be generated. The other cases will go to next checkpoints (refer to (b-1) and (b-2)). If the non-secure code tries to read/write a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure code uses non-secure address to access a secure memory or register, the operation has no effect. (refer to (c-1) and (c-2))

When a master peripheral tries to read/write a memory or register, the SCU will verify the access (refer to (d)). When a non-secure master peripheral wants to access a secure memory or register, the access will be blocked and a secure violation interrupt (SCU interrupt) can be generated. If a secure master peripheral uses non-secure address to read/write a secure memory or register, the operation has no effect.

The responses of the accesses from the core processor and master peripherals follow the rule called memory access policy, which is described in the “Memory Access Policy (MAP)” section of “Security Configuration Unit (SCU)” chapter.

6.3 Power Manager

6.3.1 Overview

Power management includes the following sections:

- Wake-up Source
- Power Domain Distribution
- Power Manager Control register

6.3.2 Power Level and Wake-up Sources

This chip has a power manager unit to support several power level for saving power. Table 6.3-1 lists all power levels in the chip.

Mode	LDO_CAP (V)	Performance Domain Max Speed(MHz)	Base Domain Max Speed (MHz)	Low Power Domain Max Speed (MHz)
Power level 0	1.15	220 MHz	220 MHz	110 MHz
Power level 1	1.1	200 MHz	200 MHz	100 MHz

Table 6.3-1 Power Level Table

Each power mode has different entry setting and leaving condition. Table 6.3-2 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]) and execute WFI instruction. System tick interrupt TICKINT(SYS_CTRL[1]) has to be disabled before entering to Power-down mode, to avoid system tick interrupt may influence system not entering power-down mode and keep operation.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	CPU Run WFI Instruction
Normal mode	0	NO
Idle mode	0	YES
Power-down mode	1	YES

Table 6.3-2 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.3-3 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	1. CPU is in sleep state. 2. All clocks stop except LXT and LIRC. 3. MIRC and HIRC stop control by AOCKPDEN (PMC_PWRCTL[8]). 4. Regulator output drop, control by VDROPEN(PMC_PWRCTL[10]). 5. Power domain gating, control by DxPGEN(PMC_PWRCTL[3:0])
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.

Wake-up Sources	N/A	All interrupts	ACMP, AWF, BOD, CCAP, CLKD, DMIC, EMAC, EINT, GPIO, GPA Trigger Wake-up pin, GPB Trigger Wake-up pin, GPC Trigger Wake-up pin, GPD Trigger Wake-up pin, HSOTG, HSUSBD, I²C, I3C, ICE, LPADC, LPI2C, LPPDMA, LPSPI, LPTMR, LPUART, LVR, OTG, Pin0(PC.0) Wake-up pin, Pin1(PB.0) Wake-up pin, Pin2(PB.2) Wake-up pin, Pin3(PB.12) Wake-up pin, Pin4(PF.6) Wake-up pin, Pin5(PA.12) Wake-up pin, POR, RTC, SDH, Standby Timer, Timer, Tick Timer, UART, USBD, USBH, USCI, UTCPD and WDT.
Available Clocks	All	All except CPU clock	HIRC, MIRC, LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.3-3 Power Mode Difference Table

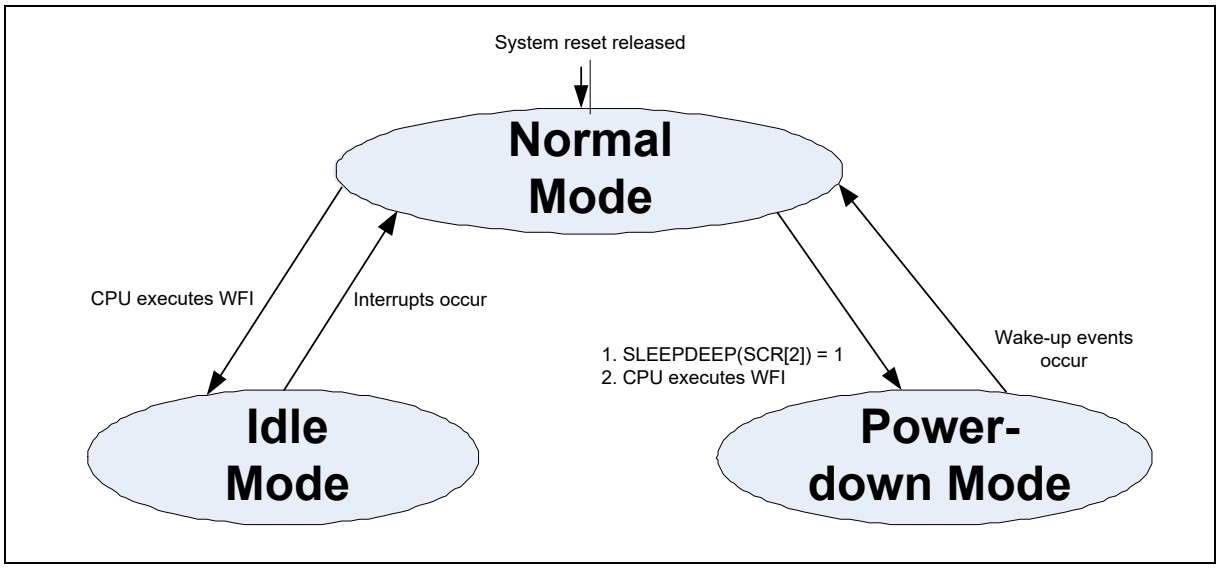


Figure 6.3-1 Power Mode State Machine

	Normal Mode	Idle Mode	Power-Down Mode
HXT	ON	ON	Halt
HIRC	ON	ON	ON/OFF[4]
HIRC48M	ON	ON	Halt
MIRC	ON	ON	ON/OFF[3]
LXT	ON	ON	ON/OFF[1]
LIRC	ON	ON	ON/OFF[2,25]
APLLx	ON	ON	Halt
CPU	ON	Halt	Halt
SCLK	ON	ON	ON/OFF[26]
ACLK	ON	ON	OFF
HCLK0/HCLK1	ON	ON	OFF
PCLK0/PCLK1/PCLK2/PCLK3	ON	ON	OFF
HCLK2	ON	ON	ON/OFF[27]
PCLK4	ON	ON	ON/OFF[28]
SRAM	NOR/RET/PSD[5]	NOR/RET/PSD[5]	NOR/RET/PSD[5]
FLASH	ON	ON	Halt
TIMER	ON	ON	ON/OFF[6]
WDT	ON	ON	ON/OFF[7]
RTC	ON	ON	ON/OFF[8]
UART	ON	ON	ON/OFF[9]
SDH	ON	ON	ON/OFF[10]
SPI	ON	ON	ON/OFF[11]
SC	ON	ON	ON/OFF[12]
CANFD	ON	ON	ON/OFF[13]
I^2S	ON	ON	ON/OFF[14]
QSPI	ON	ON	ON/OFF[15]
CCAP	ON	ON	ON/OFF[16]
TTMR	ON	ON	ON/OFF[17]
LPTMR	ON	ON	ON/OFF[18]
LPUART	ON	ON	ON/OFF[19]
LPSPI	ON	ON	ON/OFF[20]
DMIC	ON	ON	ON/OFF[21]
LPADC	ON	ON	ON/OFF[22]

PSIO	ON	ON	ON/OFF[23]
KPI	ON	ON	ON/OFF[24]
Others	ON	ON	Halt

Table 6.3-4 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on software setting in normal mode.
2. LIRC ON or OFF depends on software setting in normal mode.
3. MIRC ON or OFF depends on software setting in normal mode.
4. HIRC ON or OFF depends on software setting in normal mode.
5. SRAM power mode depends on software setting in normal mode.
6. If TIMER clock source is selected as LIRC/LXT/HIRC and LIRC/LXT/HIRC is on.
7. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
8. If RTC clock source is selected as LXT and LXT is on.
9. If UART clock source is selected as LXT/HIRC and LXT/HIRC is on.
10. If SDH clock source is selected as HIRC and HIRC is on.
11. If SPI clock source is selected as HIRC and HIRC is on.
12. If SC clock source is selected as HIRC and HIRC is on.
13. If CANFD clock source is selected as HIRC and HIRC is on.
14. If I^2S clock source is selected as HIRC and HIRC is on.
15. If QSPI clock source is selected as HIRC and HIRC is on.
16. If CCAP clock source is selected as MIRC/HIRC and MIRC/HIRC is on.
17. If TTMR clock source is selected as LIRC/LXT/MIRC/HIRC and LIRC/LXT/MIRC/HIRC is on.
18. If LPTMR clock source is selected as LIRC/LXT/MIRC/HIRC and LIRC/LXT/MIRC/HIRC is on.
19. If LPUART clock source is selected as LXT/MIRC/HIRC and LXT/MIRC/HIRC is on.
20. If LPSPI clock source is selected as MIRC/HIRC and MIRC/HIRC is on.
21. If DMIC clock source is selected as MIRC/HIRC and MIRC/HIRC is on.
22. If LPADC clock source is selected as LXT/MIRC/HIRC and LXT/MIRC/HIRC is on.
23. If PSIO clock source is selected as LIRC/LXT/HIRC and LIRC/LXT/HIRC is on.
24. If KPI clock source is selected as LIRC/HIRC and LIRC/ HIRC is on.
25. If timer wake up function is enabled, LIRC will be enabled automatically when chip enters Power-down mode.
26. If auto-operation mode is started, SCLK will be enabled automatically when chip enters Power-down mode.
27. If auto-operation mode is started, HCLK2 will be enabled automatically when chip enters Power-down mode.
28. If auto-operation mode is started, PCLK4 will be enabled automatically when chip enters Power-down mode.

Wake-up sources in Power-down mode:

EINT, GPIO, UART, USBD, USBH, OTG, CAN, BOD, ACMP, WDT, SDH, Timer, I²C, I³C, USCI, RTC, LPSPI, DMIC and CLKD.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.3-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power Domain	System Can Enter Power-Down Mode Again Condition*
ACMP	Comparator Power-Down Wake-Up Interrupt	D1	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
	ACMPO status change	D3	
AWF	Received data meets threshold conditions	D2	After software writes 1 to clear HTHIS(AWF_STATUS[0]) and LTHIS(AWF_STATUS[1])
BOD	Brown-out Detector Reset / Interrupt	D3	After software writes 1 to clear BODIF (SYS_BODSTS[1]).
CCAP	Motion Detection Modes Interrupt (CCAP_INTSTS[5:4])	D2	After software writes 1 to clear WKF (CCAP_MDTRG_WK[24])
CLKD	LXT clock fail interrupt	D0	After software writes 1 to clear LXTFIF (CLK_CLKDSTS[13]).
DMIC	DMIC Power-Down Wake-Up Interrupt	D2	After software writes 1 to clear VADACTIVE (VAD_STATUS0[30]).
EINT	External Interrupt	D1	After software write 1 to clear the Px_INTSRC[n] bit.
EMAC	Magic Packet Detection	D1	After software read to clear MGKPRCVD(PMT_Control_Status[5]), Magic Packet Received.
GPIO	GPIO Interrupt	D1	After software write 1 to clear the Px_INTSRC[n] bit.
GPA Trigger Wake-up pin	rising or falling edge event, 16-pin	D3	After software writes 1 to clear GPATGWKIF (PMC_INTSTS[16]).
GPB Trigger Wake-up pin	rising or falling edge event, 16-pin	D3	After software writes 1 to clear GPBTGWKIF (PMC_INTSTS[17]).
GPC Trigger Wake-up pin	rising or falling edge event, 15-pin	D3	After software writes 1 to clear GPCTGWKIF (PMC_INTSTS[18]).
GPD Trigger Wake-up pin	rising or falling edge event, 15-pin	D3	After software writes 1 to clear GPDTGWKIF (PMC_INTSTS[19]).
HSOTG	ID pin state be change	D1	After software writes 1 to set WKEN(HSOTG_CTL[5]).
HSUSBD	1.VBUS plug in/out 2.USB Resume/Reset	D1	1. After software writes 1 to clear HSUSBD_BUSINTSTS[8](VBUS) 2. After software writes 1 to clear HSUSBD_BUSINTSTS[2](Resume) or HSUSBD_BUSINTSTS[1](Reset)
I²C	Address match wake-up	D1	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to

			clear WKIF(I2C_WKSTS[0]).
I3C	Master: None Slave: Address match wake-up	D1	After software writes 1 to clear RESPRDY (I3C_INTSTS[4]).
LPADC	1. ADC Conversion End 2. Conversion Result Monitor	D2	1. After software writes 1 to clear ADWKF (LPADC_AUTOSTS[0]). 2. After software writes 1 to clear CMP0WKF (LPADC_AUTOSTS[1]) and CMP1WKF (LPADC_AUTOSTS [2]).
LPI2C	Master: 1. TXCNT count match wake-up 2. RXCNT count match wake-up 3. Transmit address+W/R and receive NACK	D2	Master: 1. After software writes 1 to clear TXWKF (LPI2C_AUTOSTS[0]) 2. After software writes 1 to clear RXWKF (LPI2C_AUTOSTS[1]) 3. After software writes 1 to clear ERRORWKF (LPI2C_AUTOSTS[2])
	Slave: Address match wake-up		Slave: After software writes 1 to clear WKIF (LPI2C_WKSTS[0])
LPPDMA	Master: 1. ALIGNF is high. 2. TDIF is high. 3. ABTIF is high	D2	Master: 1. After software writes 1 to clear ABTIFn and writes 1 to clear WKF. 2. After software writes 1 to clear TDIFn and writes 1 to clear WKF. 3. After software writes 1 to clear ALIGNn and writes 1 to clear WKF.
LPSPI	Master: TCNT[7:0] count match wake-up Slave: SS active wake-up	D2	Master: after software write 1 to clear CNTWKF (LPSPI_AUTOSTS[3]) Slave: after software write 1 to clear SSWKF (LPSPI_AUTOSTS[1])
LPTMR	1.timer count match wake-up 2.pwm count match PIF wake-up 3.pwm count match CMPUIF wake-up 4.IFA count match wake-up	D2	1.After software writes 1 to clear TWKF (LPTMRx_INTSTS[1]) and TIF (LPTMRx_INTSTS[0]). 2. After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and PIF (LPTMRx_PWMINTSTS0[1]). 3.After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and CMPUIF (LPTMRx_PWMINTSTS0[2]). 4.After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and IFAIF (LPTMRx_PWMAINTSTS[0]).
LPUART	1. nCTS wake-up 2. RX Data wake-up 3. Received FIFO Threshold Wake-up 4. RS-485 AAD Mode Wake-up 5. Received FIFO Threshold Time-out Wake-up 6. Bus Idle Time-out Wake-up	D2	1. After software writes 1 to clear CTSWKF (LPUART_WKSTS[0]). 2. After software writes 1 to clear DATWKF (LPUART_WKSTS[1]). 3. After software writes 1 to clear RFRTWKF (LPUART_WKSTS[2]). 4. After software writes 1 to clear RS485WKF (LPUART_WKSTS[3]). 5. After software writes 1 to clear TOUTWKF (LPUART_WKSTS[4]). 6. After software writes 1 to clear AOTOWKF (LPUART_AUTOSTS[0]).
LVR	LVR Reset	D3	After software writes 1 to clear LVRF

			(SYS_RSTSTS[3])
OTG	ID pin state be change	D1	After software writes 1 to set WKEN(OTG_CTL[5]).
Pin 0(PC.0) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN0WKIF (PMC_INTSTS[8]).
Pin 1(PB.0) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN1WKIF (PMC_INTSTS[9]).
Pin 2(PB.2) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN2WKIF (PMC_INTSTS[10]).
Pin 3(PB.12) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN3WKIF (PMC_INTSTS[11]).
Pin 4(PF.6) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN4WKIF (PMC_INTSTS[12]).
Pin 5(PA.12) Wake-up pin	rising or falling edge event	D4	After software writes 1 to clear PIN5WKIF (PMC_INTSTS[13]).
POR	POR Reset	D4	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
RTC	Alarm Interrupt	D5	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	D5	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	RTC Tamper Interrupt	D5	After software writes 1 to clear TAMPxIF (RTC_INTSTS[8:13]).
SDH	Card detection	D1	Clear CDIF0 (SDH_INTSTS[8]) after SDH wake-up.
Standby Timer	Wakeup by standby timer time-out	D3	After software writes 1 to clear STMRWKIF (PMC_INTSTS[1]).
TIMER	Timer Interrupt	D1	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
TTMR	Timer count match wake-up	D2	After software writes 1 to clear TWKF (TTMRx_INTSTS[1]) and TIF (TTMRx_INTSTS[0]).
UART	nCTS wake-up	D1	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	D1	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	D1	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	D1	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	D1	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USBD	1.Remote wake-up 2.Plug in wake-up	D1	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected	D1	1.After write 1 to clear RHSC (HcInterruptStatus[7]). 2.After write 1 to clear RHSC

	3.Remote-wakeup		(HcInterruptStatus[7]). 3.After write 1 to clear RHSC (HcInterruptStatus[7]). and port suspended.
USCI I²C	Data toggle	D1	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	D1	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	D1	After software writes 1 to clear WKF (USPI_WKSTS[0]).
USCI UART	CTS Toggle	D1	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	D1	After software writes 1 to clear WKF (UUART_WKSTS[0]).
UTPCD	PHY active and bus event change (VBUS detect, vcon detect, bus over cuurent etc)	D1	VBUS bus plug in/out or bus power toggle detection
CCAP	Motion Detection Modes Interrupt (CCAP_INTSTS[5:4])	D2	After software writes 1 to clear WKF (CCAP_MDTRG_WK[24])
WDT	WDT Interrupt	D1	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).

Table 6.3-5 Condition of Entering Power-down Mode Again

6.3.3 Power Down and Wake-up Process

Figure 6.3-2 shows the system enters idle mode process. If the CPU executes the WFI/WFE instruction at t0, and CPU clock will stop at t1, and CPU operations will be temporarily stopped during t1 to t2. At t2, the device generates interrupt event to CPU, and CPU starts exiting sleep mode at this moment. The CPU will completely exit sleep mode and resume clock at t3, and CPU will execute interrupt handler at t3. It should be noted that if the interrupt flag is not cleared, the CPU will enter the interrupt handler again. The CPU will execute main function instructions after interrupt flag is cleared at t4.

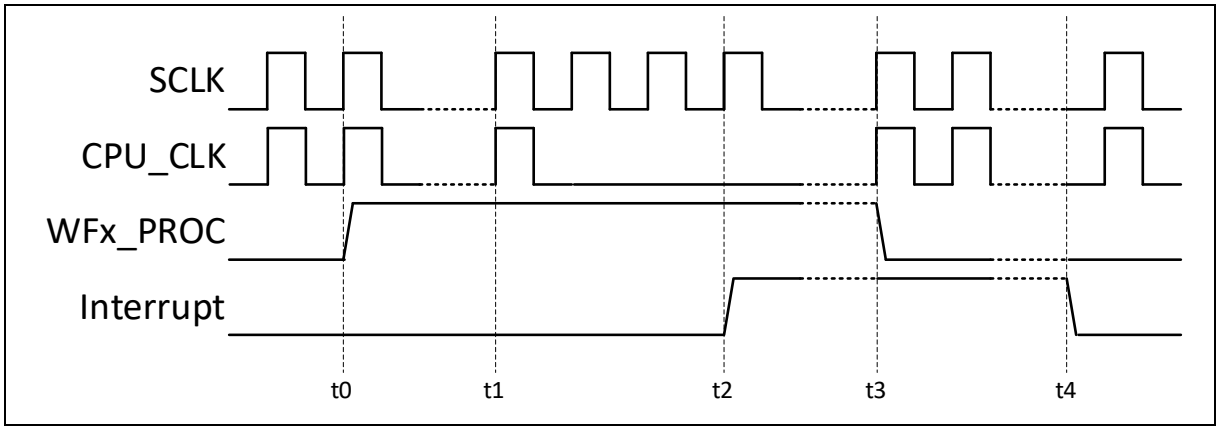


Figure 6.3-2 Idle Mode Process

Figure 6.3-3 shows the system enters Power-down mode process. If the CPU executes the WFI/WFE instruction at t0, and CPU clock will stop at t1, and CPU operations will be temporarily stopped at t1 until wake-up, At t2, SCLK, ACLK, HCLKx and PCLKx clock will be stopped. If auto operating event is triggered in Power-down mode, then SCLK, HCLK2, PCLK4 will be enabled until auto operating is finished.

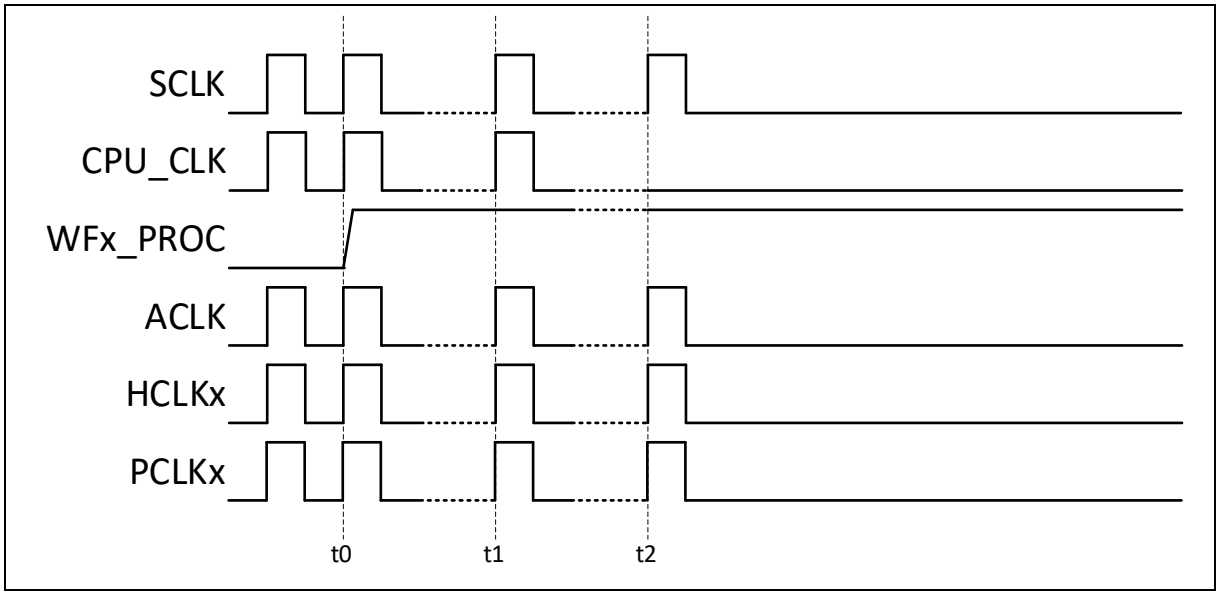


Figure 6.3-3 Enter Power-down Mode Process

Figure 6.3-4 shows the system exits Power-down mode process when CPU clock is not stopped. If CPU clock hasn't been turned off then wake-up event is not necessary for system wake-up. Some device only has the ability to generates interrupt, but does not have the ability to generates wake-up event. If the device generates an interrupt event at t1 in the interval from t0 to t2, then system will be woken up. The CPU will completely exit sleep at t2, and CPU will execute interrupt handler at t2. The CPU will execute main function instructions after interrupt flag is cleared at t3. In the case of wake-up before fully Power-down mode, then PDWKIF(PMC_INTSTS[0]) is not asserted.

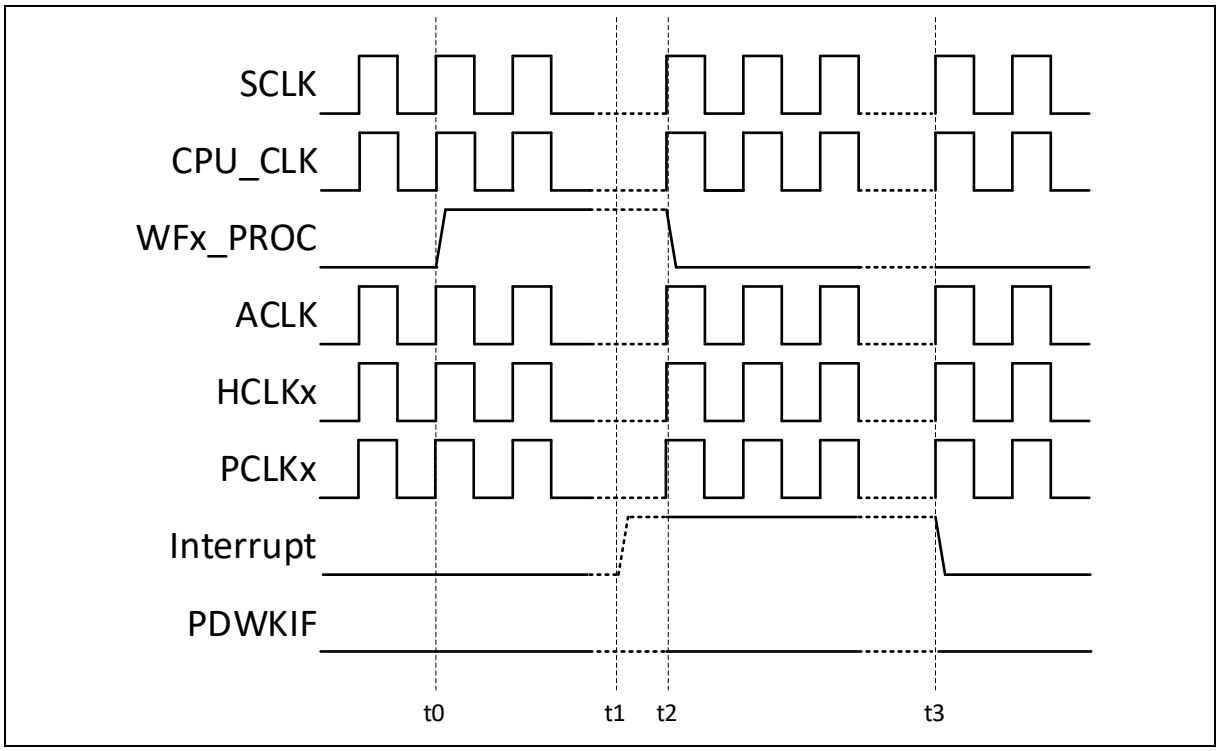


Figure 6.3-4 Wake-up Process When CPU Clock Is Not Stopped

Figure 6.3-5 shows the system exits Power-down mode process when CPU clock is stopped. The CPU

executes the WFI/WFE instruction at t0, and CPU clock will stop at t1, and SCLK clock will stop at t2. If CPU clock has been turned off then wake-up event is necessary for system wake-up. If the device generates an interrupt and wake-up event at t3 after t2, then system will be woken up. The CPU will completely exit sleep at t4, and CPU will execute interrupt handler at t4. The CPU will execute main function instructions after interrupt flag is cleared at t5. In the case of wake-up after fully Power-down mode, then PDWKIF(PMC_INTSTS[0]) is asserted.

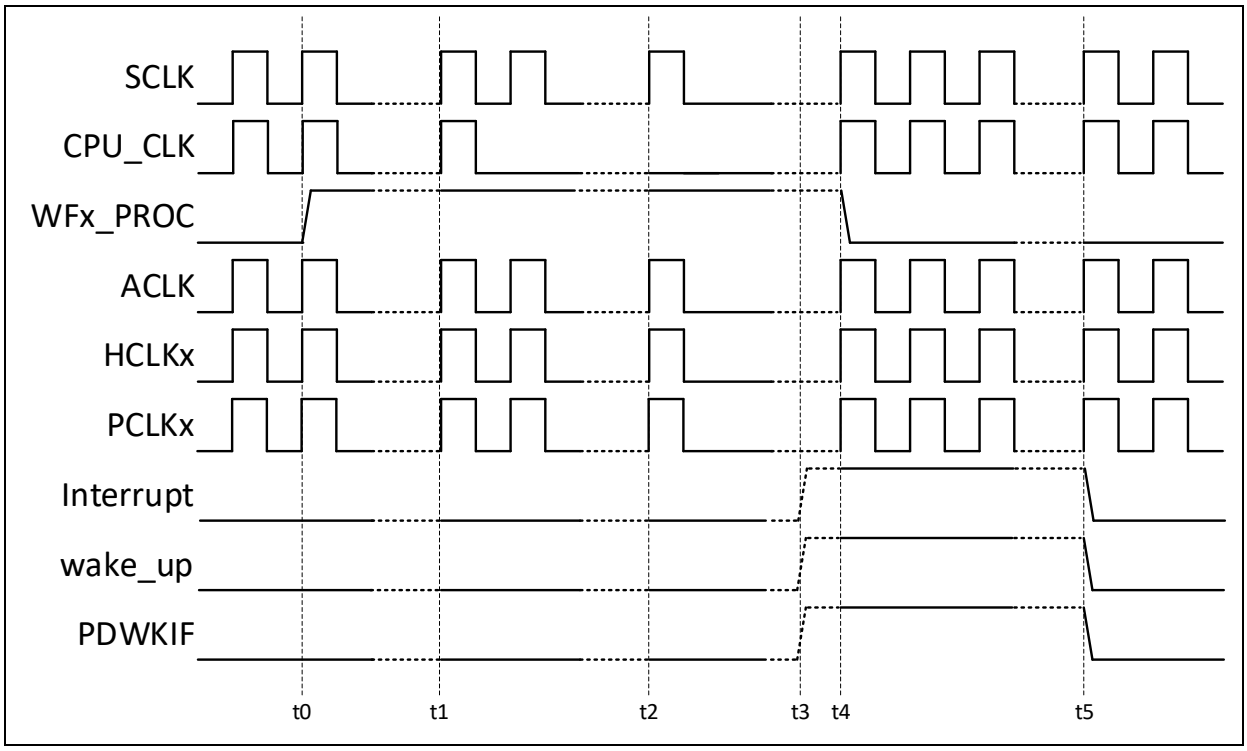


Figure 6.3-5 Wake-up Process When CPU Clock Is Stop

6.3.4 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 0.7V, 1.1V or 1.15V power for digital operation and I/O pins.
- USB transceiver power from V_{DD} offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). The internal voltage regulator can be set to LDO converter mode. Figure 6.3-6 shows the power distribution.

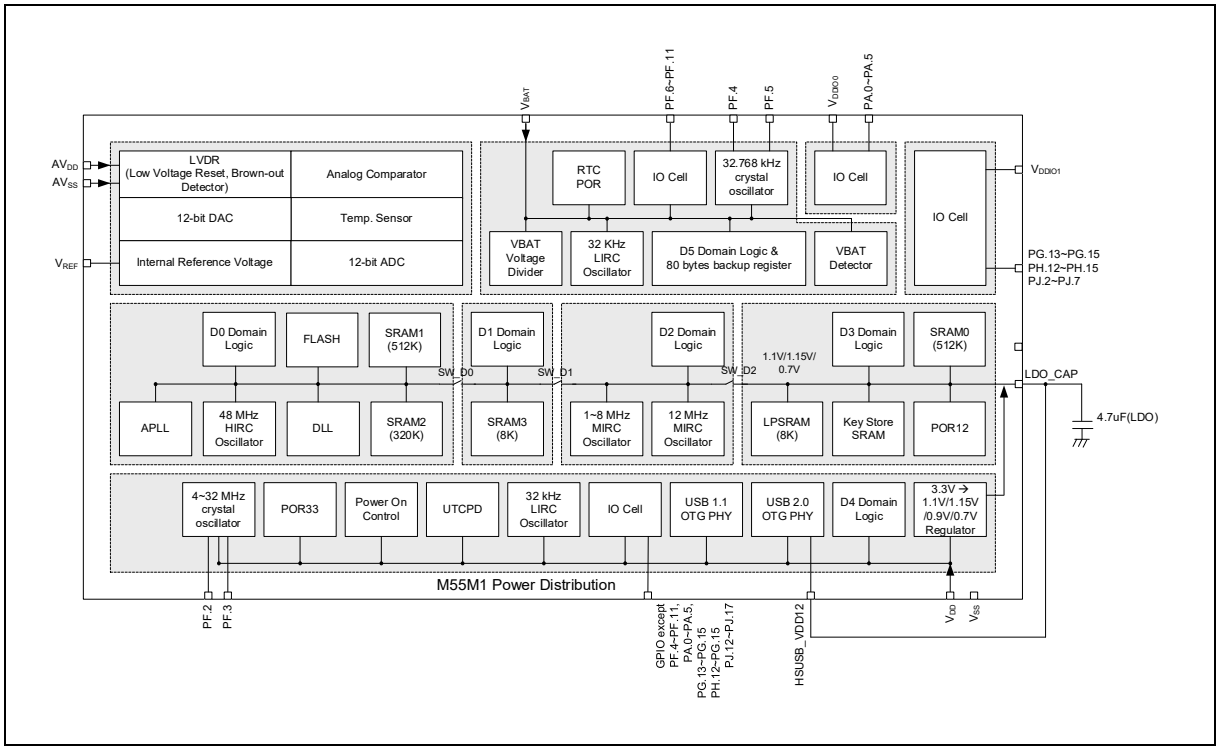


Figure 6.3-6 Power Distribution Diagram

6.3.5 Digital Power Domain Distribution

In this chip, digital power is divided into six domains:

- Performance Domain (D0) for CPU, NPU and very high speed peripheral device.
- Base Domain (D1) for high speed peripheral device.
- Low Power Domain (D2) for low speed peripheral device which support auto operating mode.
- Standby Power Domain (D3) for power management controller and some wake-up source such as standby ACMP, GPA trigger pin, GPB trigger pin, GPC trigger pin and GPD trigger pin .
- High Voltage Power Domain (D4) for high voltage logic and some wake-up source such as PIN0~PIN5 and Standby Timer.
- RTC Power Domain (D5) for real timer controller logic and that wake-up source.

6.3.6 Power-down mode Configuration

In this chip, the feature of Power-down mode can configured by PMC_PWRCTL, Users can freely make settings according to the application situation, Following are traditional Power-down modes as examples:

- Normal Power-down mode 0 (NPD0) is used for fast wake-up needs, in this power-down mode the analog circuits are in active mode and only the high-speed clock sources are disabled.
- Normal Power-down mode 1 (NPD1) is used light power saving needs, in this power-down mode the analog circuits are in low power mode and the high-speed clock sources are disabled.
- Normal Power-down mode 2 (NPD2) is used moderate power saving needs, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled and regulator output drop to low voltage.
- Normal Power-down mode 3 (NPD3) is used light power saving needs and not use peripherals in D0~D1, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled and the power domain D0 ~ D1 are power off, only support PL1(1.1V) if auto operating function is enabled.
- Normal Power-down mode 4 (NPD4) is used moderate power saving needs and not use peripherals in D0~D1, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled, regulator output drop to low voltage and the power domain D0 ~ D1 are power off.
- Standby Power-down mode 0 (SPD0) is used heavy power saving needs and not use peripherals in D0~D2, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled and the power domain D0 ~ D2 are power off.
- Standby Power-down mode 1 (SPD1) is used heavy power saving needs and not use peripherals in D0~D2, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled, regulator output drop to low voltage and the power domain D0 ~ D2 are power off.
- Deep Power-down mode (DPD) is used very heavy power saving needs and not use peripherals in D0~D3 in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled and the power domain D0~D3 are power off.

Each power mode has different setting for PMC_PWRCTL. Table 6.3-6 shows the setting for each Power-down mode.

PD Mode		NPD0	NPD1	NPD2	NPD3	NPD4	SPD0	SPD1	DPD
Vcore		1.1-1.15v[1]	1.1-1.15v[1]	0.7v	1.1-1.15v[1]	0.7v	1.1-1.15v[1]	0.7v	X
Registers	D0PGEN	0	0	0	1	1	1	1	1
	D1PGEN	0	0	0	1	1	1	1	1
	D2PGEN	0	0	0	0	0	1	1	1
	D3PGEN	0	0	0	0	0	0	0	1
	VDROPEN	0	0	1	0	1	0	1	0
	FWEN	1	0	0	0	0	0	0	1
	PRSTDBEN	1	1	0	1	0	0	0	0

Table 6.3-6 Power Mode Configuration Table

Note: Vcore depends on software setting PLSEL(PMC_PLCTL[0]).

6.4 System Manager

6.4.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.4.2 Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset source are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_RSTCTL[0])
  - System Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M55 core only by writing 1 to CPURST (SYS_RSTCTL[7])

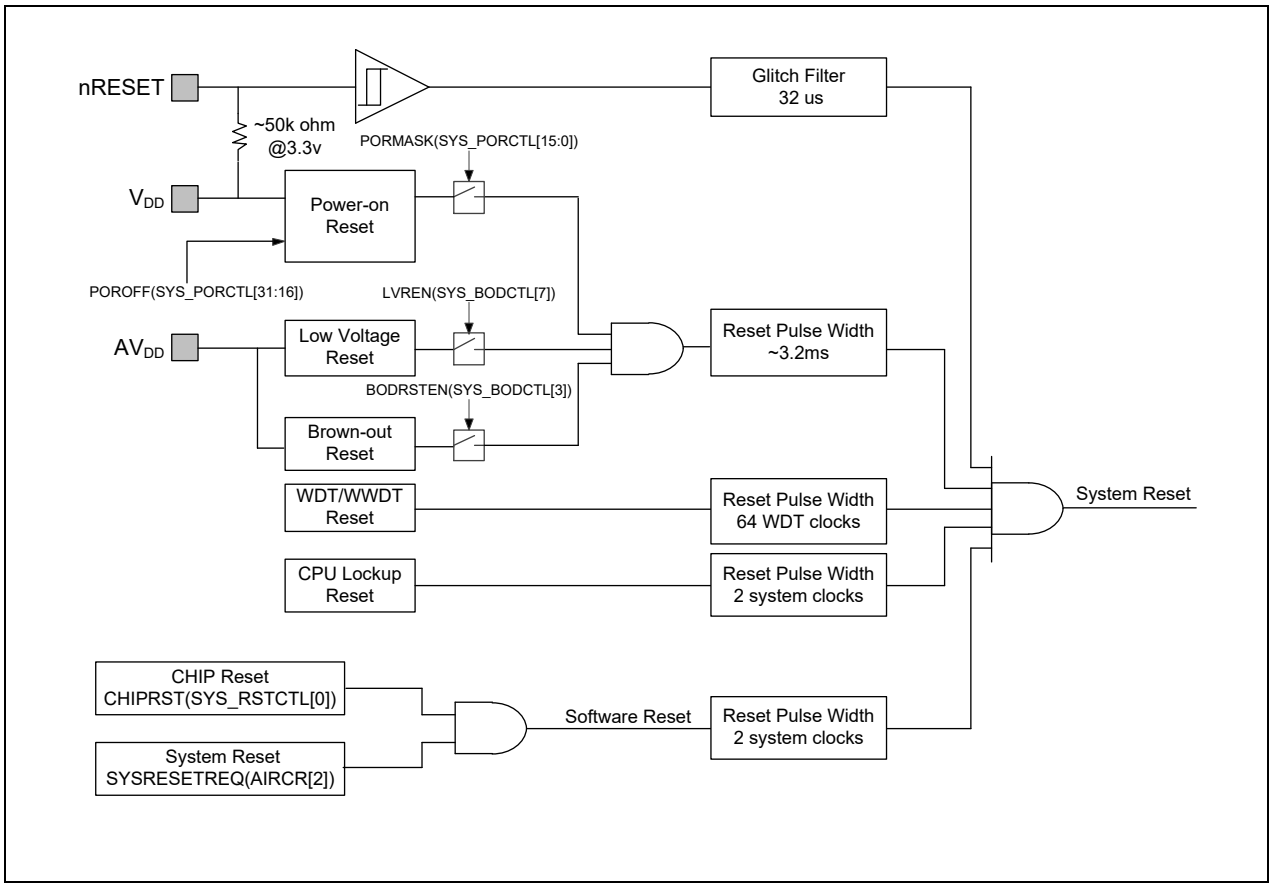


Figure 6.4-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M55 only; the other reset sources will reset Cortex-M55 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.4-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_RSTCTL[0])	0x0	-	-	-	-	-	-	-	-
SCLKSEL (CLK_SCLKSEL[2:0])	0x0 HIRC	0x0 HIRC	0x0 HIRC	0x0 HIRC	0x0 HIRC	0x0 HIRC	0x0 HIRC	0x0 HIRC	-
SCLKDIV (CLK_SCLKDIV[3:0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PLSTATUS (PMC_PLSTS[1:0])	0x1 PL1	0x1 PL1	0x1 PL1	0x1 PL1	0x1 PL1	0x1 PL1	0x1 PL1	-	-
CURMVR (PMC_VRSTS[0])	0x0 LDO	0x0 LDO	0x0 LDO	0x1 PL1	0x1 PL1	0x0 LDO	0x0 LDO	-	-

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[11:8])									
BODRSTEN (SYS_BODCTL[3])									
D0PGEN PMC_PWRCTL[0]	0x0	-	-	-	-	-	-	-	-
D1PGEN PMC_PWRCTL[1]	0x0	-	-	-	-	-	-	-	-
D2PGEN PMC_PWRCTL[2]	0x0	-	-	-	-	-	-	-	-
D3PGEN PMC_PWRCTL[3]	0x0	-	-	-	-	-	-	-	-
VDROPEN PMC_PWRCTL[10]	0x0	-	-	-	-	-	-	-	-
FWEN PMC_PWRCTL[11]	0x0	-	-	-	-	-	-	-	-
PRSTDBEN PMC_PWRCTL[12]	0x1	-	-	-	-	-	-	-	-
PMC_SYSRB0PC	0x0	-	-	-	-	-	-	-	-
PMC_SYSRB1PC	0xAAAA	-	-	-	-	-	-	-	-
PMC_SYSRB2PC	0x0	-	-	-	-	-	-	-	-
PMC_SYSRB3PC	0x2	-	-	-	-	-	-	-	-
PMC_LPSYSRPC	0x0	-	-	-	-	-	-	-	-
PMC_KSRPC	0x0	0x0	0x0	0x0	0x0	-	0x0	-	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
WDT0SEL (CLK_WDTSEL[1:0])	0x2	0x2	-	-	-	-	-	-	-
WDT1SEL (CLK_WDTSEL[5:4])	0x2	0x2	-	-	-	-	-	-	-
LIRCSTB (CLK_STATUS[0])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
MIRCSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[3])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
HXTSTB (CLK_STATUS[4])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
MIRC48MSTB (CLK_STATUS[5])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
APLL0STB (CLK_STATUS[6])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
APLL1STB (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
SCLKSWF (CLK_STATUS[8])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
CLK_APLL0CTL	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	-
CLK_APLL1CTL	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	0x8000_8422	
PMC_PWRCTL	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
Other Peripheral Registers	Reset Value								-
Note: '-' means that the value of register keeps original setting.									

Table 6.4-1 Reset Value of Registers

6.4.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state

keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.4-2 shows the nRESET reset waveform.

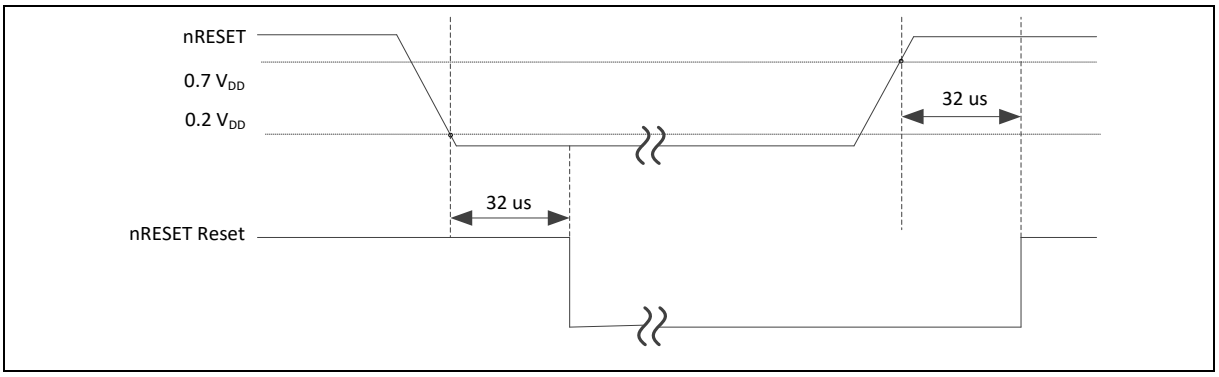


Figure 6.4-2 nRESET Reset Waveform

6.4.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.4-3 shows the power-on reset waveform.

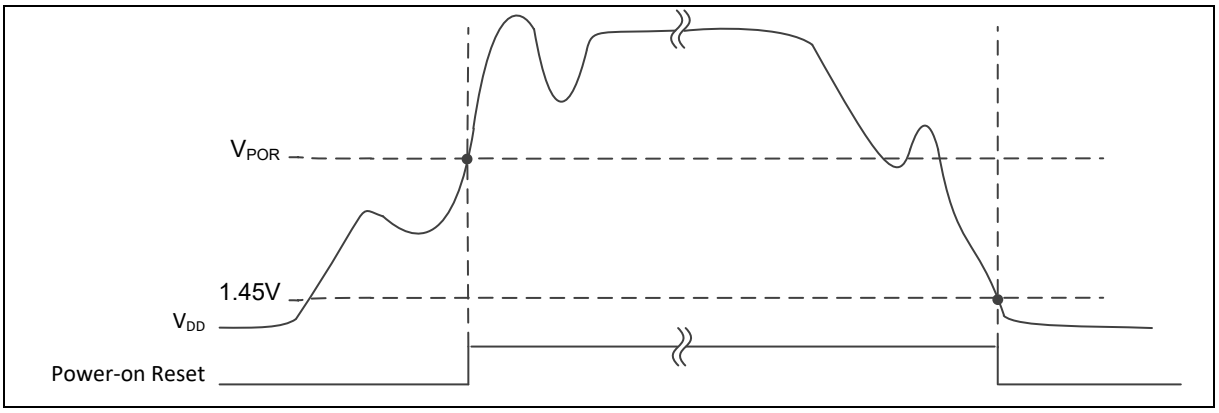


Figure 6.4-3 Power-on Reset (POR) Waveform

6.4.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[16]) to 1, and wait write busy flag (SYS_BODCTL[31]) to 0, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[22:20]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[22:20]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.4-4 shows the Low Voltage Reset waveform.

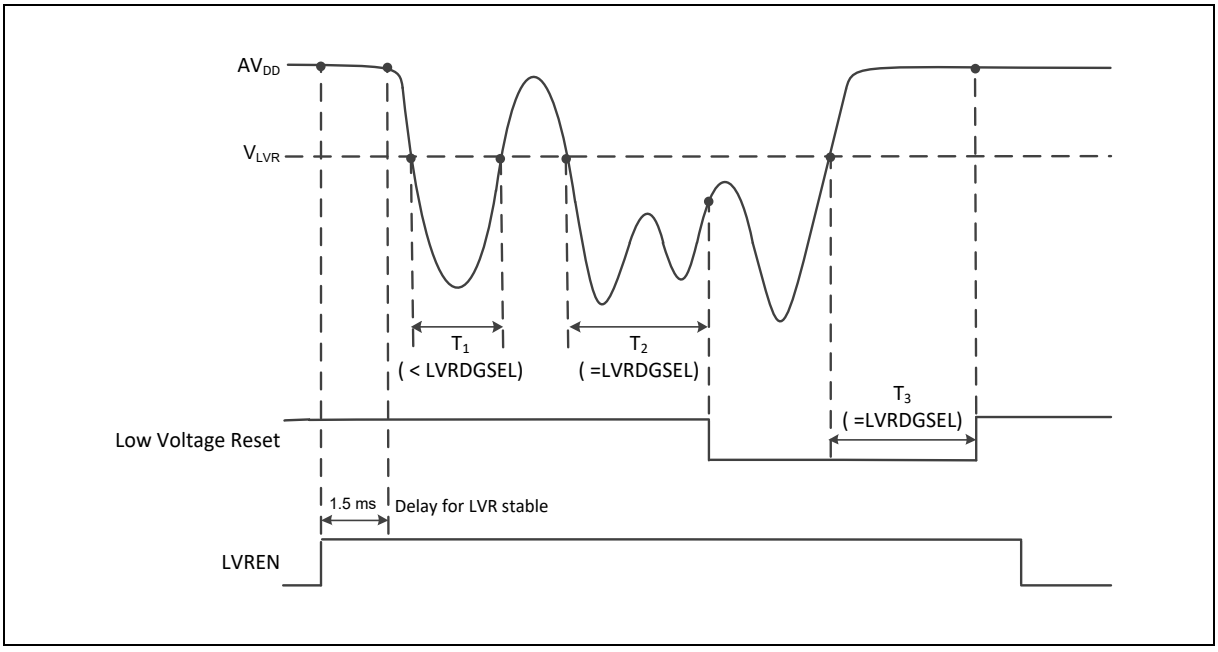


Figure 6.4-4 Low Voltage Reset (LVR) Waveform

6.4.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), and waits write busy flag (SYS_BODCTL[31]) to 0, BOD detection circuit will be stable and the BOD function will be active. Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} that is decided by BODEN and BODVL (SYS_BODCTL[10:8]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[6:4]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[2]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. If the Brown-out Detector (BOD) low power function is enabled by setting the Brown-out Detector Low Power Mode Enable Bit BODLPM (SYS_BODCTL[1]), and AV_{DD} voltage approaches VBODH, The BOD interrupt event may be triggered repeatedly. Figure 6.4-5 shows the Brown-out Detector waveform.

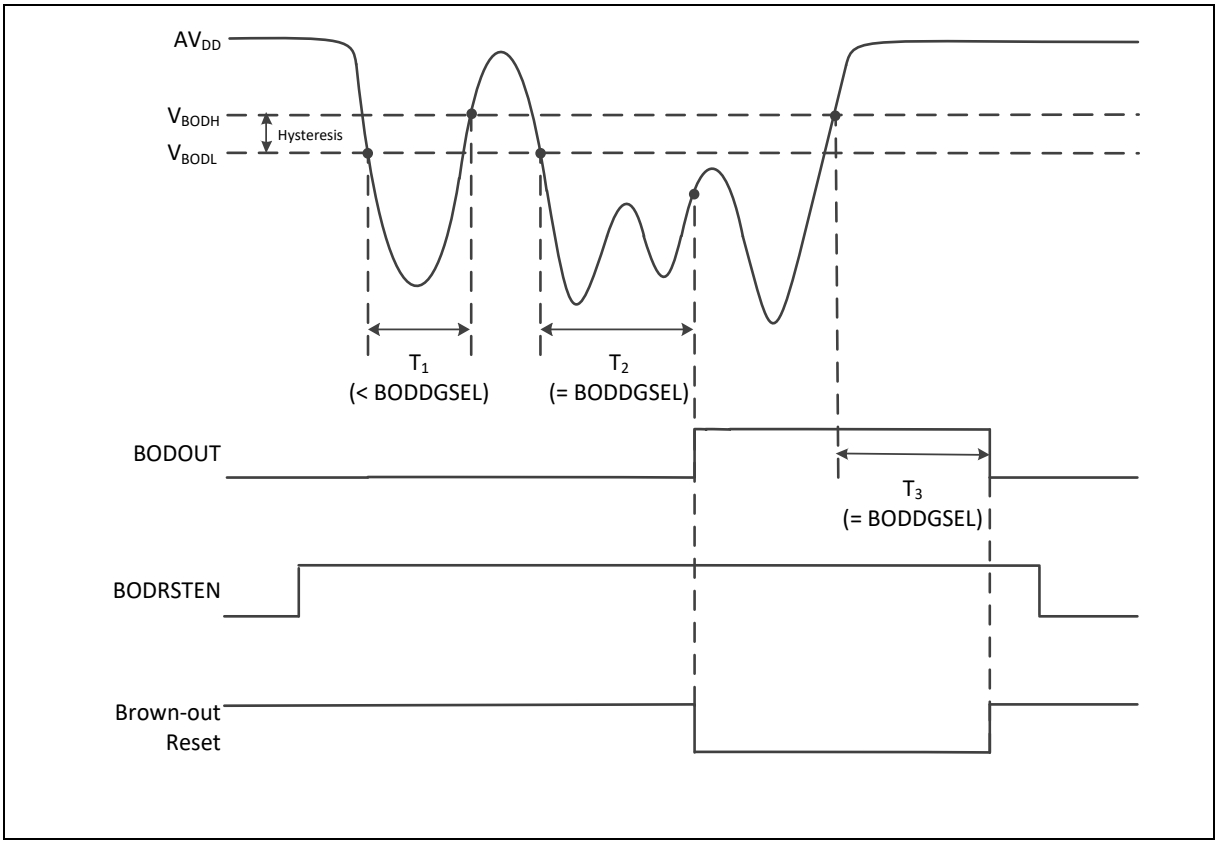


Figure 6.4-5 Brown-out Detector (BOD) Waveform

6.4.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.4.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.4.2.7 CPU Reset, CHIP Reset and System Reset

The CPU Reset means only Cortex-M55 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_RSTCTL[7]) to 1 and execute WFI instruction to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset. User can set the CHIPRSTEN(SYS_RSTCTL[0]) to 1 and execute WFI instruction to assert the CHIP Reset signal.

The System Reset is similar with CHIP Reset. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the System Reset.

6.4.3 Bus Matrix

This chip uses Advanced Microcontroller Bus Architecture (AMBA) protocol to implement system bus., The D0 Domain has two system bus, AXI and AHBP. The D1 Domain has a system bus, which is AHB0. The D2 Domain has a system bus, which is AHB2.

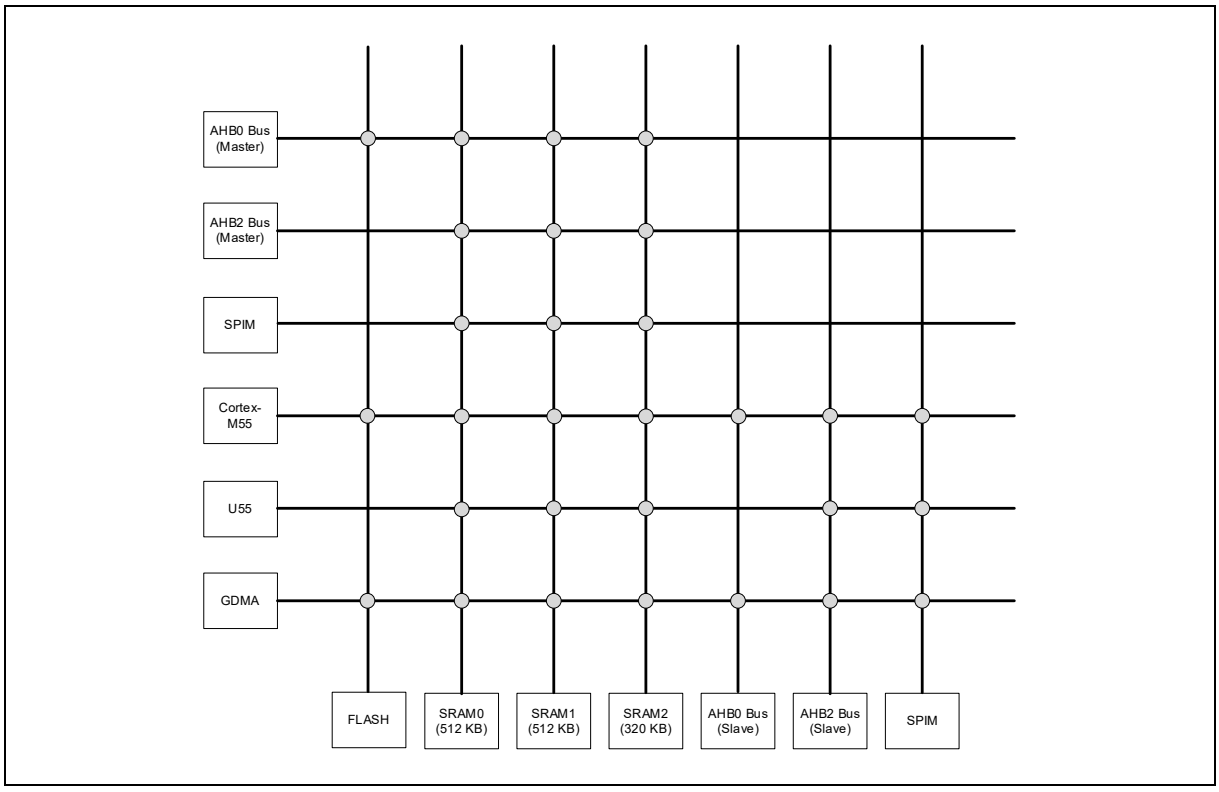


Figure 6.4-6 M55M1AXI Bus Matrix Architecture Diagram

Refer to Figure 6.4-6. The Bus AXI has six masters and seven slaves, in which a different master can communicate with a different slave at the same time through AXI Bus Matrix. The Cortex-M55 core acts as the master in AXI Bus Matrix, which can communicate with any slaves through AXI Bus Matrix. GDMA is Peripheral Direct Memory Access and acts as the master in AXI Bus Matrix, which can communicate with any slaves through AXI Bus Matrix. SPIM and U55 acts as the master role in AXI Bus. AHB0 Bus (Master) is from AHB0 Bus matrix and AHB2 Bus (Master) is from AHB2 Bus matrix.

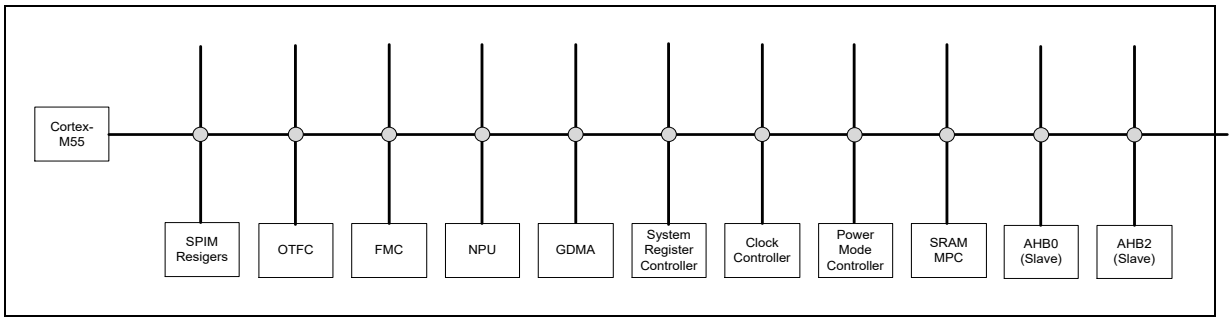


Figure 6.4-7 M55M1AHBP Bus Matrix Architecture Diagram

Refer to Figure 6.4-7. The Bus AHBP has one master and eleven slaves. The Cortex-M55 core acts as the master in AHBP Bus Matrix, which can communicate with any slaves through AHBP Bus Matrix. AHB0 Bus (Slave) is to AHB0 Bus matrix and AHB2 Bus (Slave) is to AHB2 Bus matrix.

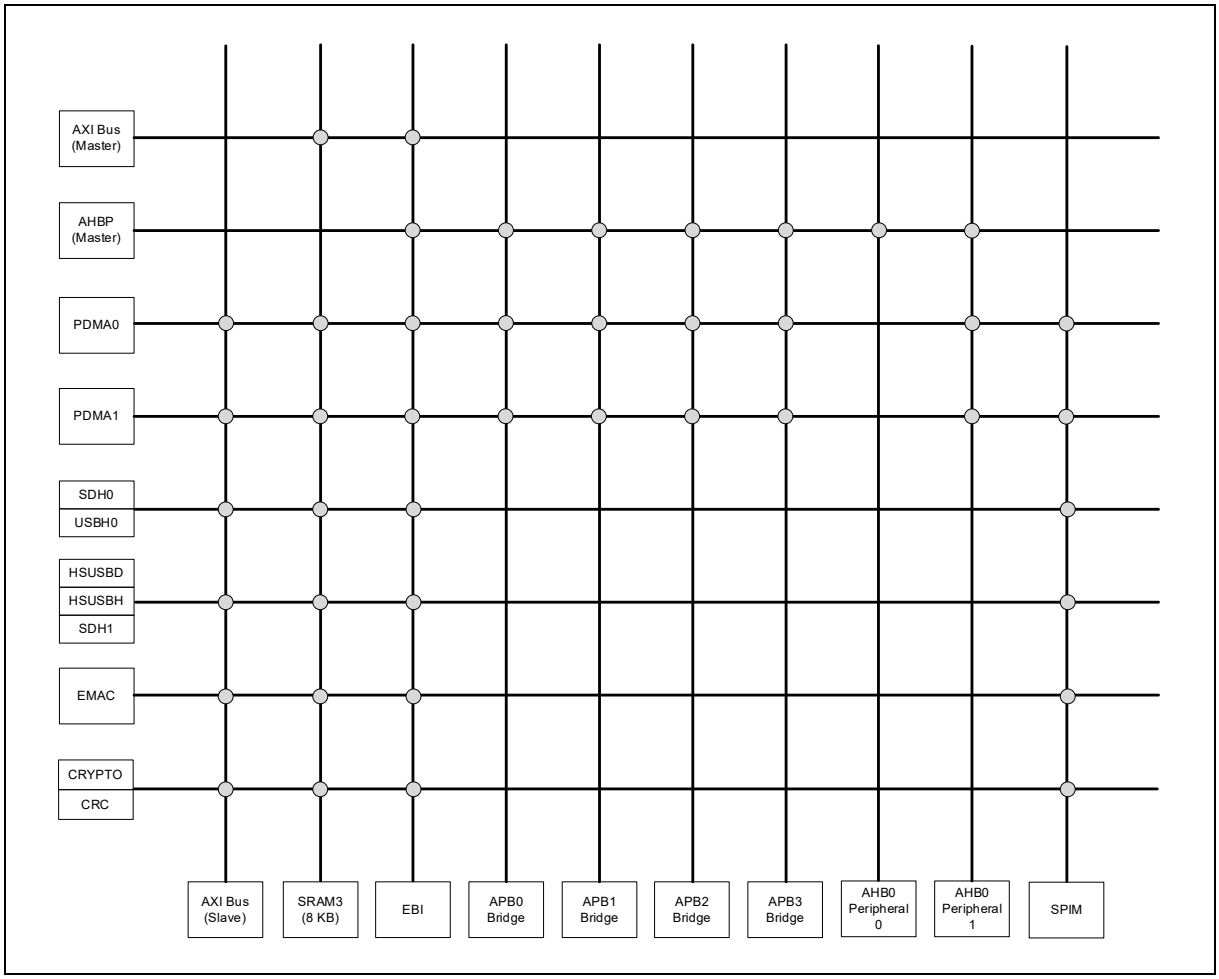


Figure 6.4-8 M55M1AHB0 Bus Matrix Architecture Diagram

Refer to Figure 6.4-8. The Bus AHB0 has eight masters and ten slaves, in which a different master can communicate with a different slave at the same time through Bus Matrix. PDMA0 and PDMA1 are Peripheral Direct Memory Access and act as the master in Bus Matrix, which can communicate with any slaves through Bus Matrix. SDH0, Crypto and USBH0 share the same master bandwidth. HSUSBD, HSUSBH and SDH1 share the same master bandwidth. EMAC and CRC act as the master role in Bus Matrix. AHB0 Peripheral 0 is the Advanced High-performance Bus (AHB) Slave interface controller for PDMA0, PDMA1, USBH0, USBH1, HSUSBH, HSUBSD, SDH0, SDH1, EMAC, Crypto and CRC. AHB0 Peripheral 1 is the Advanced High-performance Bus (AHB) Slave interface controller for KS, KDF0, KDF1, CANFD0, CANFD1, GPIO and EBI.

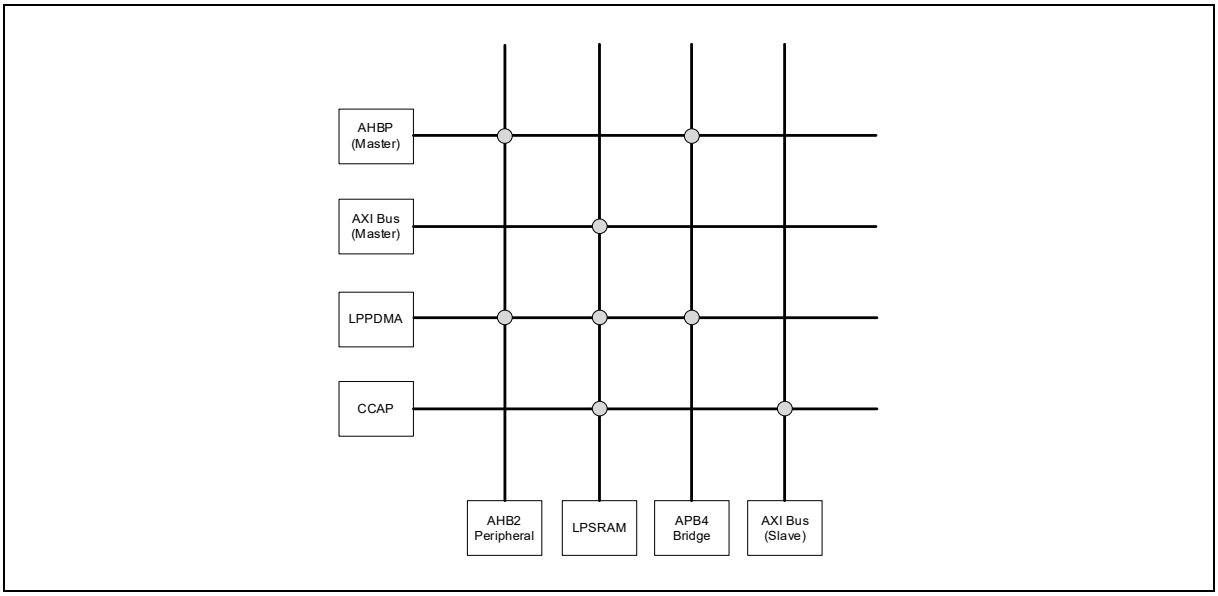


Figure 6.4-9 M55M1AHB2 Bus Matrix Architecture Diagram

Refer to Figure 6.4-9. The Bus AHB2 has four masters and four slaves, in which a different master can communicate with a different slave at the same time through Bus Matrix. LPPDMA is Peripheral Direct Memory Access and act as the master in Bus Matrix, which can communicate with any slaves through Bus Matrix. CCAP acts as the master role in Bus Matrix. AHB2 Peripheral is the Advanced High-performance Bus (AHB) Slave interface controller for LPGPIO and SCU.

6.4.4 System Memory Map

This chip provides 4 Gbytes addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.4-2. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. This chip implement Arm TrustZone Architecture as well as memory alias technique, secure code and non-secure code can run together on the chip well, while both have different memory view. Secure code view is shown in Table 6.4-2 and non-secure code view is shown in Table 6.4-3.

This chip only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory		
0x0000_0000 – 0x0000_FFFF	ITCM_BA	ITCM Memory Space (64 Kbytes)
0x0010_0000 – 0x001F_FFFF	FLASH0_BA	FLASH0 Memory Space (1024 Kbytes)
0x0020_0000 – 0x002F_FFFF	FLASH1_BA	FLASH1 Memory Space (1024 Kbytes)
0x0F10_0000 – 0x0F10_1FFF	LDROM_BA	LDROM Memory Space (8 Kbytes)
0x0F20_0000 – 0x0F20_00FF	XOM_BA	XOM Memory Space (256 bytes)
0x0F21_0000 – 0x0F21_07FF	NSSEC_SET_BA	NSSEC_SET Memory Space (2 Kbytes)
0x0F30_0000 –	UserConfiguration	User Configuration Memory Space (256

0x0F30_00FF		bytes)
0x0F31_0000 – 0x0F31_0FFF	OTP_BA	OTP Memory Space (4 Kbytes)
0x0F61_0000 – 0x0F61_07FF	SEC_SET_BA	SEC_SET Memory Space (2 Kbytes)
0x0F80_0000 – 0x0F80_3FFF	MKROM_BA	MKROM Memory Space (16 Kbytes)
0x2000_0000 – 0x2001_FFFF	DTCM_BA	DTCM Memory Space (128 Kbytes)
0x2010_0000 – 0x2017_FFFF	SRAM0_BA	SRAM0 Memory Space (512 Kbytes)
0x2018_0000 – 0x201F_FFFF	SRAM1_BA	SRAM1 Memory Space (512 Kbytes)
0x2020_0000 – 0x2024_FFFF	SRAM2_BA	SRAM2 Memory Space (320 Kbytes)
0x2030_0000 – 0x2030_1FFF	SRAM3_BA	SRAM3 Memory Space (8 Kbytes)
0x2031_0000 – 0x2031_1FFF	LPSRAM_BA	LPSRAM Memory Space (8 Kbytes)
0x6000_0000 – 0x602F_FFFF	EXTMEM_BA	External Memory Space (3072 Kbytes)
0x81F0_0000 – 0x81F7_FFFF	SRAM0_BA (Alias)	SRAM0 Alias Memory Space (512 Kbytes)
0x81F8_0000 – 0x81FF_FFFF	SRAM1_BA (Alias)	SRAM1 Alias Memory Space (512 Kbytes)
0x8200_0000 – 0x83FF_FFFF	SPIM0_BA	SPIM0 Memory Space (32768 Kbytes)
Secure APB5 Controllers Space (0x4000_0000 ~ 0x4003_FFFF)		
0x4000_0000 – 0x4000_0FFF	SYS_BA	System Control Registers
0x4000_1000 – 0x4000_1FFF	CLK_BA	Clock Control Registers (always secure)
0x4000_2000 – 0x4000_2FFF	PMC_BA	Power Manager Control Registers (always secure)
0x4000_3000 – 0x4000_3FFF	NPU_BA	NPU Control Registers
0x4000_4000 – 0x4000_5FFF	GDMA_BA	GDMA Control Registers
0x4000_8000 – 0x4000_8FFF	SRAM0MPC_BA	SRAM0MPC Control Registers (always secure)
0x4000_9000 – 0x4000_9FFF	SRAM1MPC_BA	SRAM1MPC Control Registers (always secure)
0x4000_A000 – 0x4000_AFFF	SRAM2MPC_BA	SRAM2MPC Control Registers (always secure)
0x4000_B000 – 0x4000_BFFF	SRAM3MPC_BA	SRAM3MPC Control Registers (always secure)

0x4000_D000 – 0x4000_DFFF	SPIM0MPC_BA	SPIM0MPC Control Registers (always secure)
Secure AHB0 Controllers Space (0x4020_0000 ~ 0x4023_FFFF)		
0x4020_0000 – 0x4020_0FFF	PDMA0_BA	PDMA0 Control Registers
0x4020_1000 – 0x4020_1FFF	PDMA1_BA	PDMA1 Control Registers
0x4020_2000 – 0x4020_2FFF	USBH0_BA	USB Host0 Control Registers
0x4020_3000 – 0x4020_3FFF	USBH1_BA	USB Host1 Control Registers
0x4020_4000 – 0x4020_4FFF	HSUSBH_BA	High Speed USB Host Control Registers
0x4020_5000 – 0x4020_5FFF	HSUSBD_BA	High Speed USB Device Control Registers
0x4020_6000 – 0x4020_6FFF	SDH0_BA	SDHOST0 Control Registers
0x4020_7000 – 0x4020_7FFF	SDH1_BA	SDHOST1 Control Registers
0x4020_8000 – 0x4020_9FFF	EMAC_BA	EMAC Control Registers
0x4020_A000 – 0x4020_AFFF	CRYPTO_BA	Cryptographic Accelerator Registers
0x4020_B000 – 0x4020_BFFF	CRC_BA	CRC Control Registers
0x4022_0000 – 0x4022_0FFF	KS_BA	Key Store Control Registers
0x4022_1000 – 0x4022_1FFF	KDF_BA	KDF Control Registers
0x4022_2000 – 0x4022_3FFF	CANFD0_BA	CANFD0 Bus Control Registers
0x4022_4000 – 0x4022_5FFF	CANFD1_BA	CANFD1 Bus Control Registers
0x4022_9000 – 0x4022_9FFF	GPIO_BA	GPIO Control Registers
0x4023_0000 – 0x4023_0FFF	EBI_BA	External Bus Interface Control Registers
Secure AHB1 Controllers Space (0x4004_0000 ~ 0x4007_FFFF)		
0x4004_0000 – 0x4004_0FFF	OTFC0_BA	OTFC0 Control Registers (always secure)
0x4004_2000 – 0x4004_2FFF	SPIM0_BA	SPIM0 Control Registers
0x4004_4000 – 0x4004_4FFF	FMC_BA	Flash Memory Control Registers
Secure AHB2 Controllers Space (0x4040_0000 ~ 0x4043_FFFF)		
0x4040_0000 –	LPPDMA_BA	Lower Power PDMA Control Registers

0x4040_0FFF		
0x4040_1000 – 0x4040_1FFF	CCAP_BA	CCAP Control Registers
0x4040_2000 – 0x4040_2FFF	SCU_BA	Secure Configuration Unit Registers (always secure)
0x4040_3000 – 0x4040_3FFF	LPGPIO_BA	Lower Power GPIO Control Registers
Secure APB0 Controllers Space (0x4024_0000 ~ 0x4024_FFFF)		
0x4024_0000 – 0x4024_0FFF	WWDT0_BA	Window Watchdog Timer 0 Control Registers
0x4024_1000 – 0x4024_1FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 Control Registers
0x4024_2000 – 0x4024_2FFF	EPWM0_BA	EPWM0 Control Registers
0x4024_3000 – 0x4024_3FFF	BPWM0_BA	BPWM0 Control Registers
0x4024_4000 – 0x4024_4FFF	EQEI0_BA	EQEI0 Control Registers
0x4024_5000 – 0x4024_5FFF	EQEI2_BA	EQEI2 Control Registers
0x4024_6000 – 0x4024_6FFF	ECAP0_BA	ECAP0 Control Registers
0x4024_7000 – 0x4024_7FFF	ECAP2_BA	ECAP2 Control Registers
0x4024_8000 – 0x4024_8FFF	I2C0_BA	I2C0 Control Registers
0x4024_9000 – 0x4024_9FFF	I2C2_BA	I2C2 Control Registers
0x4024_A000 – 0x4024_AFFF	QSPI0_BA	QSPI0 Control Registers
0x4024_B000 – 0x4024_BFFF	SPI0_BA	SPI0 Control Registers
0x4024_C000 – 0x4024_CFFF	SPI2_BA	SPI2 Control Registers
0x4024_D000 – 0x4024_DFFF	UART0_BA	UART0 Control Registers
0x4024_E000 – 0x4024_EFFF	UART2_BA	UART2 Control Registers
0x4024_F000 – 0x4024_FFFF	UART4_BA	UART4 Control Registers
Secure APB1 Controllers Space (0x4025_0000 ~ 0x4027_FFFF)		
0x4025_0000 – 0x4025_0FFF	UART6_BA	UART6 Control Registers
0x4025_1000 – 0x4025_1FFF	UART8_BA	UART8 Control Registers
0x4025_2000 –	USCI0_BA	USCI0 Control Registers

0x4025_2FFF		
0x4025_3000 – 0x4025_3FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4025_4000 – 0x4025_4FFF	SC2_BA	Smartcard Host 2 Control Registers
0x4025_5000 – 0x4025_5FFF	PSIO_BA	PSIO Device Control Register
0x4025_6000 – 0x4025_6FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4025_7000 – 0x4025_7FFF	DAC01_BA	DAC0/DAC1 Control Registers
0x4025_9000 – 0x4025_9FFF	HSOTG_BA	HSOTG Control Registers
0x4025_A000 – 0x4025_AFFF	I2S0_BA	I2S0 Interface Control Registers
0x4025_B000 – 0x4025_BFFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x4025_C000 – 0x4025_CFFF	USBD_BA	USB Device Control Register
Secure APB2 Controllers Space (0x4028_0000 ~ 0x4028_FFFF)		
0x4028_0000 – 0x4028_0FFF	WWDT1_BA	Window Watchdog Timer 1 Control Registers
0x4028_2000 – 0x4028_2FFF	EPWM1_BA	EPWM1 Control Registers
0x4028_3000 – 0x4028_3FFF	BPWM1_BA	BPWM1 Control Registers
0x4028_4000 – 0x4028_4FFF	EQEI1_BA	EQEI1 Control Registers
0x4028_5000 – 0x4028_5FFF	EQEI3_BA	EQEI3 Control Registers
0x4028_6000 – 0x4028_6FFF	ECAP1_BA	ECAP1 Control Registers
0x4028_7000 – 0x4028_7FFF	ECAP3_BA	ECAP3 Control Registers
0x4028_8000 – 0x4028_8FFF	I2C1_BA	I2C1 Control Registers
0x4028_9000 – 0x4028_9FFF	I2C3_BA	I2C3 Control Registers
0x4028_A000 – 0x4028_AFFF	QSPI1_BA	QSPI1 Control Registers
0x4028_B000 – 0x4028_BFFF	SPI1_BA	SPI1 Control Registers
0x4028_C000 – 0x4028_CFFF	SPI3_BA	SPI3 Control Registers
0x4028_D000 – 0x4028_DFFF	UART1_BA	UART1 Control Registers

0x4028_E000 – 0x4028_EFFF	UART3_BA	UART3 Control Registers
0x4028_F000 – 0x4028_FFFF	UART5_BA	UART5 Control Registers
Secure APB3 Controllers Space (0x4029_0000 ~ 0x402B_FFFF)		
0x4029_0000 – 0x4029_0FFF	UART7_BA	UART7 Control Registers
0x4029_1000 – 0x4029_1FFF	UART9_BA	UART9 Control Registers
0x4029_2000 – 0x4029_2FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4029_3000 – 0x4029_3FFF	OTG_BA	OTG Control Registers
0x4029_4000 – 0x4029_4FFF	KPI_BA	Key Pad Control Register
0x4029_5000 – 0x4029_5FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4029_6000 – 0x4029_6FFF	TRNG_BA	TRNG Control Registers
0x4029_7000 – 0x4029_7FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4029_8000 – 0x4029_8FFF	I2S1_BA	I2S1 Interface Control Registers
0x4029_9000 – 0x4029_9FFF	ACMP23_BA	Analog Comparator 2/3 Control Registers
0x4029_A000 – 0x4029_AFFF	I3C_BA	I3C Control Registers
0x4029_B000 – 0x4029_BFFF	UTCPD_BA	UTCPD Control Registers
Secure APB4 Controllers Space (0x4044_0000 ~ 0x4047_FFFF)		
0x4044_0000 – 0x4044_0FFF	LPTMR01_BA	Low power Timer0/Timer1 Control Registers
0x4044_1000 – 0x4044_1FFF	TTMR01_BA	Tick Timer0/Timer1 Control Registers
0x4044_2000 – 0x4044_2FFF	LPADC_BA	Low power Analog-Digital-Converter (LPEADC) Control Registers
0x4044_3000 – 0x4044_3FFF	LPI2C_BA	Low power I^2C Control Registers
0x4044_4000 – 0x4044_4FFF	LPSPI_BA	Low power SPI Control Registers
0x4044_5000 – 0x4044_5FFF	DMIC_BA	DMIC Control Registers
0x4044_6000 – 0x4044_6FFF	LPUART_BA	Low power UART Control Registers
0x4044_7000 – 0x4044_7FFF	WDT0_BA	Watchdog Timer 0 Control Registers

0x4044_8000 – 0x4044_8FFF	WDT1_BA	Watchdog Timer 1 Control Registers
0x4044_9000 – 0x4044_9FFF	AWF_BA	Awake Filter Control Registers
0x4045_0000 – 0x4045_0FFF	LPSRAMMPC_BA	LPSRAMMPC Control Registers (Always secure)

Table 6.4-2 Address Space Assignments for On-Chip Controllers

Address Space	Token	Controllers
Flash and SRAM Memory		
0x1000_0000 – 0x1000_FFFF	ITCM_BA	ITCM Memory Space (64 Kbytes)
0x1010_0000 – 0x101F_FFFF	FLASH0_BA	FLASH0 Memory Space (1024 Kbytes)
0x1020_0000 – 0x102F_FFFF	FLASH1_BA	FLASH1 Memory Space (1024 Kbytes)
0x1F10_0000 – 0x1F10_1FFF	LDROM_BA	LDROM Memory Space (8 Kbytes)
0x1F80_0000 – 0x1F80_3FFF	MKROM_BA	MKROM Memory Space (16 Kbytes)
0x3000_0000 – 0x3001_FFFF	DTCM_BA	DTCM Memory Space (128 Kbytes)
0x3010_0000 – 0x3017_FFFF	SRAM0_BA	SRAM Memory Space (512 Kbytes)
0x3018_0000 – 0x301F_FFFF	SRAM1_BA	SRAM Memory Space (512 Kbytes)
0x3020_0000 – 0x3024_FFFF	SRAM2_BA	SRAM Memory Space (320 Kbytes)
0x3030_0000 – 0x3030_1FFF	SRAM3_BA	SRAM Memory Space (8 Kbytes)
0x3031_0000 – 0x3031_1FFF	LPSRAM_BA	LPSRAM Memory Space (8 Kbytes)
0x7000_0000 – 0x702F_FFFF	EXTMEM_BA	External Memory Space (3072 Kbytes)
0x9000_0000 – 0x91FF_FFFF	SPIM0_BA	SPIM0 Memory Space (32768 Kbytes)
Non-secure APB5 Controllers Space (0x5000_0000 ~ 0x5004_FFFF)		
0x5000_0000 – 0x5000_0FFF	SYS_BA	System Control Registers
0x5000_1000 – 0x5000_1FFF	CLK_BA	Clock Control Registers (shared)
0x5000_2000 – 0x5000_2FFF	PMU_BA	Power Manager Control Registers (shared)
0x5000_3000 – 0x5000_3FFF	NPU_BA	NPU Control Registers

0x5000_4000 – 0x5000_5FFF	GDMA_BA	GDMA Control Registers
0x5000_8000 – 0x5000_8FFF	SRAM0MPC_BA	SRAM0MPC Control Registers (always secure)
0x5000_9000 – 0x5000_9FFF	SRAM1MPC_BA	SRAM1MPC Control Registers (always secure)
0x5000_A000 – 0x5000_AFFF	SRAM2MPC_BA	SRAM2MPC Control Registers (always secure)
0x5000_B000 – 0x5000_BFFF	SRAM3MPC_BA	SRAM3MPC Control Registers (always secure)
0x5000_D000 – 0x5000_DFFF	SPIM0MPC_BA	SPIM0MPC Control Registers (always secure)
Non-secure AHB0 Controllers Space (0x5020_0000 ~ 0x503F_FFFF)		
0x5020_0000 – 0x5020_0FFF	PDMA0_BA	PDMA0 Control Registers
0x5020_1000 – 0x5020_1FFF	PDMA1_BA	PDMA1 Control Registers
0x5020_2000 – 0x5020_2FFF	USBH0_BA	USB Host0 Control Registers
0x5020_3000 – 0x5020_3FFF	USBH1_BA	USB Host1 Control Registers
0x5020_4000 – 0x5020_4FFF	HSUSBH_BA	High Speed USB Host Control Registers
0x5020_5000 – 0x5020_5FFF	HSUSBD_BA	High Speed USB Device Control Registers
0x5020_6000 – 0x5020_6FFF	SDH0_BA	SDHOST0 Control Registers
0x5020_7000 – 0x5020_7FFF	SDH1_BA	SDHOST1 Control Registers
0x5020_8000 – 0x5020_9FFF	EMAC_BA	EMAC Control Registers
0x5020_A000 – 0x5020_AFFF	CRYPTO_BA	Cryptographic Accelerator Registers
0x5020_B000 – 0x5020_BFFF	CRC_BA	CRC Control Registers
0x5022_0000 – 0x5022_0FFF	KS_BA	Key Store Control Registers
0x5022_1000 – 0x5022_1FFF	KDF_BA	KDF Control Registers
0x5022_2000 – 0x5022_3FFF	CANFD0_BA	CANFD0 Bus Control Registers
0x5022_4000 – 0x5022_5FFF	CANFD1_BA	CANFD1 Bus Control Registers
0x5022_9000 – 0x5022_9FFF	GPIO_BA	GPIO Control Registers
0x5023_0000 – 0x5023_0FFF	EBI_BA	External Bus Interface Control Registers

Non-secure AHB1 Controllers Space (0x5004_0000 ~ 0x5007_FFFF)		
0x5004_0000 – 0x5004_0FFF	OTFC0_BA	OTFC0 Control Registers (always secure)
0x5004_2000 – 0x5004_2FFF	SPIM0_BA	SPIM0 Control Registers
0x5004_4000 – 0x5004_4FFF	FMC_BA	Flash Memory Control Registers (shared)
Non-secure AHB2 Controllers Space (0x5040_0000 ~ 0x5043_FFFF)		
0x5040_0000 – 0x5040_0FFF	LPPDMA_BA	Lower Power PDMA Control Registers
0x5040_1000 – 0x5040_1FFF	CCAP_BA	CCAP Control Registers
0x5040_2000 – 0x5040_2FFF	SCU_BA	Secure Configuration Unit Registers (always secure)
0x5040_3000 – 0x5040_3FFF	LPGPIO_BA	Lower Power GPIO Control Registers
Non-secure APB0 Controllers Space (0x5024_0000 ~ 0x5024_FFFF)		
0x5024_0000 – 0x54024_0FFF	WWDT0_BA	Window Watchdog Timer 0 Control Registers
0x5024_1000 – 0x5024_1FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 Control Registers
0x5024_2000 – 0x5024_2FFF	EPWM0_BA	EPWM0 Control Registers
0x5024_3000 – 0x5024_3FFF	BPWM0_BA	BPWM0 Control Registers
0x5024_4000 – 0x5024_4FFF	EQEI0_BA	EQEI0 Control Registers
0x5024_5000 – 0x5024_5FFF	EQEI2_BA	EQEI2 Control Registers
0x5024_6000 – 0x5024_6FFF	ECAP0_BA	ECAP0 Control Registers
0x5024_7000 – 0x5024_7FFF	ECAP2_BA	ECAP2 Control Registers
0x5024_8000 – 0x5024_8FFF	I2C0_BA	I2C0 Control Registers
0x5024_9000 – 0x5024_9FFF	I2C2_BA	I2C2 Control Registers
0x5024_A000 – 0x5024_AFFF	QSPI0_BA	QSPI0 Control Registers
0x5024_B000 – 0x5024_BFFF	SPI0_BA	SPI0 Control Registers
0x5024_C000 – 0x5024_CFFF	SPI2_BA	SPI2 Control Registers
0x5024_D000 – 0x5024_DFFF	UART0_BA	UART0 Control Registers
0x5024_E000 –	UART2_BA	UART2 Control Registers

0x5024_EFFF		
0x5024_F000 – 0x5024_FFFF	UART4_BA	UART4 Control Registers
Non-secure APB1 Controllers Space (0x5025_0000 ~ 0x5027_FFFF)		
0x5025_0000 – 0x5025_0FFF	UART6_BA	UART6 Control Registers
0x5025_1000 – 0x5025_1FFF	UART8_BA	UART8 Control Registers
0x5025_2000 – 0x5025_2FFF	USCI0_BA	USCI0 Control Registers
0x5025_3000 – 0x5025_3FFF	SC0_BA	Smartcard Host 0 Control Registers
0x5025_4000 – 0x5025_4FFF	SC2_BA	Smartcard Host 2 Control Registers
0x5025_5000 – 0x5025_5FFF	PSIO_BA	PSIO Device Control Register
0x5025_6000 – 0x5025_6FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x5025_7000 – 0x5025_7FFF	DAC01_BA	DAC0/DAC1 Control Registers
0x5025_9000 – 0x5025_9FFF	HSOTG_BA	HSOTG Control Registers
0x5025_A000 – 0x5025_AFFF	I2S0_BA	I2S0 Interface Control Registers
0x5025_B000 – 0x5025_BFFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x5025_C000 – 0x5025_CFFF	USBD_BA	USB Device Control Register
Non-secure APB2 Controllers Space (0x5028_0000 ~ 0x5028_FFFF)		
0x5028_0000 – 0x5028_0FFF	WWDT1_BA	Window Watchdog Timer 1 Control Registers
0x5028_2000 – 0x5028_2FFF	EPWM1_BA	EPWM1 Control Registers
0x5028_3000 – 0x5028_3FFF	BPWM1_BA	BPWM1 Control Registers
0x5028_4000 – 0x5028_4FFF	EQEI1_BA	EQEI1 Control Registers
0x5028_5000 – 0x5028_5FFF	EQEI3_BA	EQEI3 Control Registers
0x5028_6000 – 0x5028_6FFF	ECAP1_BA	ECAP1 Control Registers
0x5028_7000 – 0x5028_7FFF	ECAP3_BA	ECAP3 Control Registers
0x5028_8000 – 0x5028_8FFF	I2C1_BA	I2C1 Control Registers
0x5028_9000 –	I2C3_BA	I2C3 Control Registers

0x5028_9FFF		
0x5028_A000 – 0x5028_AFFF	QSPI1_BA	QSPI1 Control Registers
0x5028_B000 – 0x5028_BFFF	SPI1_BA	SPI1 Control Registers
0x5028_C000 – 0x5028_CFFF	SPI3_BA	SPI3 Control Registers
0x5028_D000 – 0x5028_DFFF	UART1_BA	UART1 Control Registers
0x5028_E000 – 0x5028_EFFF	UART3_BA	UART3 Control Registers
0x5028_F000 – 0x5028_FFFF	UART5_BA	UART5 Control Registers
Non-secure APB3 Controllers Space (0x5029_0000 ~ 0x502B_FFFF)		
0x5029_0000 – 0x5029_0FFF	UART7_BA	UART7 Control Registers
0x5029_1000 – 0x5029_1FFF	UART9_BA	UART9 Control Registers
0x5029_2000 – 0x5029_2FFF	SC1_BA	Smartcard Host 1 Control Registers
0x5029_3000 – 0x5029_3FFF	OTG_BA	OTG Control Registers
0x5029_4000 – 0x5029_4FFF	KPI_BA	Key Pad Control Register
0x5029_5000 – 0x5029_5FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x5029_6000 – 0x5029_6FFF	TRNG_BA	TRNG Control Registers
0x5029_7000 – 0x5029_7FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x5029_8000 – 0x5029_8FFF	I2S1_BA	I2S1 Interface Control Registers
0x5029_9000 – 0x5029_9FFF	ACMP23_BA	Analog Comparator 2/3 Control Registers
0x5029_A000 – 0x5029_AFFF	I3C_BA	I3C Control Registers
0x5029_B000 – 0x5029_BFFF	UTCPD_BA	UTCPD Control Registers
Non-secure APB4 Controllers Space (0x5044_0000 ~ 0x5047_FFFF)		
0x5044_0000 – 0x5044_0FFF	LPTMR01_BA	Low power Timer0/Timer1 Control Registers
0x5044_1000 – 0x5044_1FFF	TTMR01_BA	Tick Timer0/Timer1 Control Registers
0x5044_2000 – 0x5044_2FFF	LPADC_BA	Low power Analog-Digital-Converter (LPEADC) Control Registers
0x5044_3000 –	LPI2C_BA	Low power I^2C Control Registers

0x5044_3FFF		
0x5044_4000 – 0x5044_4FFF	LPSPI_BA	Low power SPI Control Registers
0x5044_5000 – 0x5044_5FFF	DMIC_BA	DMIC Control Registers
0x5044_6000 – 0x5044_6FFF	LPUART_BA	Low power UART Control Registers
0x5044_7000 – 0x5044_7FFF	WDT0_BA	Watchdog Timer 0 Control Registers
0x5044_8000 – 0x5044_8FFF	WDT1_BA	Watchdog Timer 1 Control Registers
0x5044_9000 – 0x5044_9FFF	AWF_BA	Awake Filter Control Registers
0x5045_0000 – 0x5045_0FFF	LPSRAMMPC_BA	LPSRAMMPC Control Registers (Always secure)

Table 6.4-3 Non-secure Address Space Assignments for On-Chip Controllers

6.4.5 Implementation Defined Attribution Unit (IDAU)

6.4.5.1 Overview

The Armv8-M has the new feature called TrustZone, which adds an additional security state to allow full isolation of two security levels. The processor security state is decided by the memory definition. For example, processor is in Secure state when the code is executed in the Secure region. The memory map security state will be defined by the combination of:

- Internal Security Attribution Unit (SAU)
- Implementation Defined Attribution Unit (IDAU)

These attribution units define the memory space into four type regions:

- Secure Region: contains Secure program code or data
- Non-secure Callable Region (NSC): contains entry functions for Non-secure programs to access Secure functions
- Non-secure Region: contains Non-secure program code or data
- Exempt Region: exempt region will be exempted from security check

Each memory region defined by the SAU and IDAU has a region number generated by the SAU or by the IDAU. Region number is used for determining a group of memory share the same security attribute. Overlapping region numbers are not allow. For testing security attributes and region numbers, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine that the memory range is located entirely in same space. To be more specific, please refer to the Armv8-M Architecture Reference Manual. The IDAU memory map attributions and corresponding region numbers are shown in Figure 6.4-10. The address from 0xE000_0000 to 0xFFFF_FFFF is marked as exempt regions because the behavior of the address is fixed, so their security attributes do not control by the SAU or IDAU.

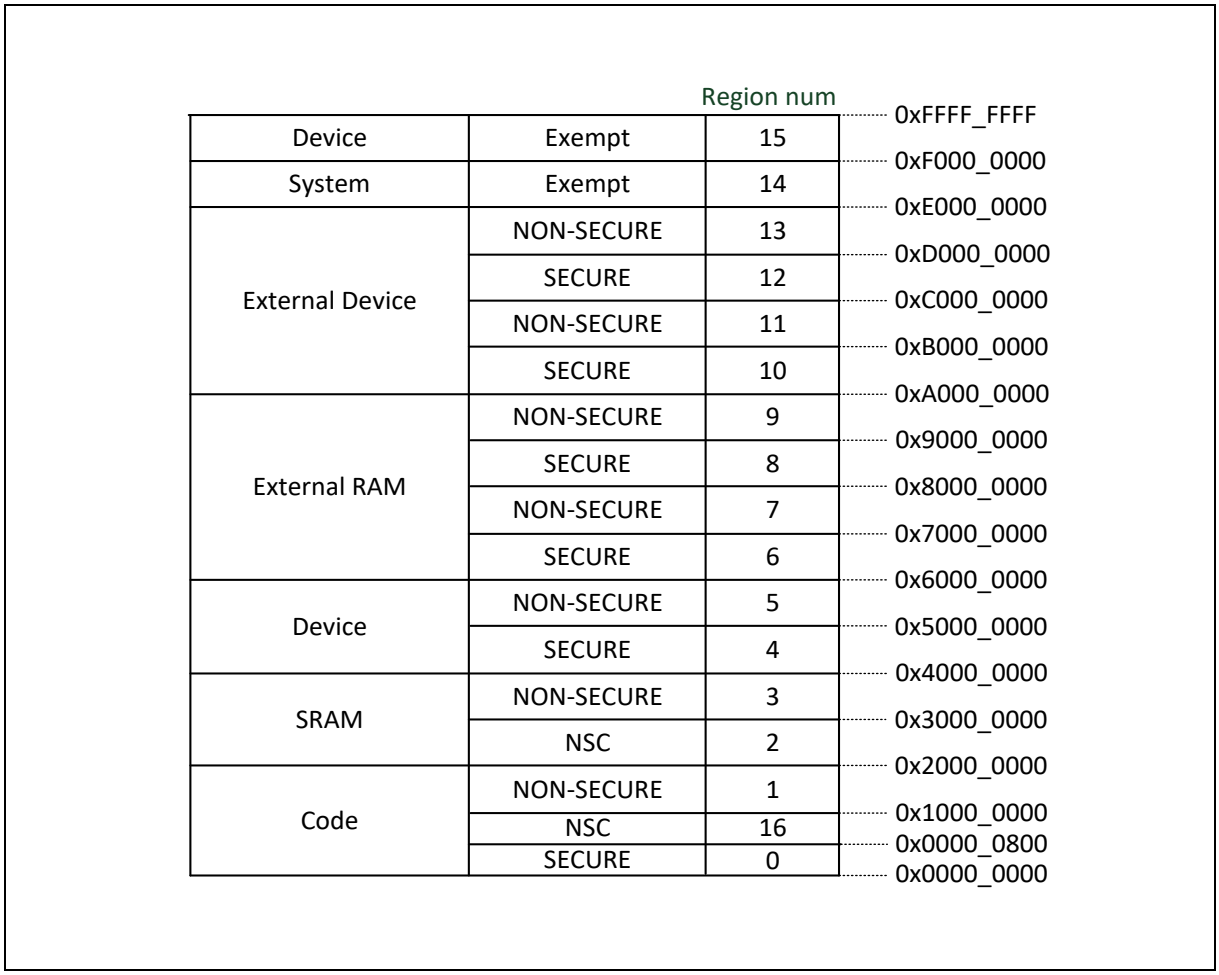


Figure 6.4-10 IDAU Memory Map

6.4.5.2 IDAU Block Diagram

The IDAU block diagram is shown in Figure 6.4-11. IDAU is security attribute unit connected outside of the processor. Both SAU and IDAU are responsible to response the security property of the address from processor, the only difference is that the memory security attribute of the SAU is configurable and the IDAU is fixed. After the processor compares the security property of the IDAU and SAU, it will take the highest security attribute applied. The hierarchy of security levels from high to low is: Secure > NSC > Non-secure.

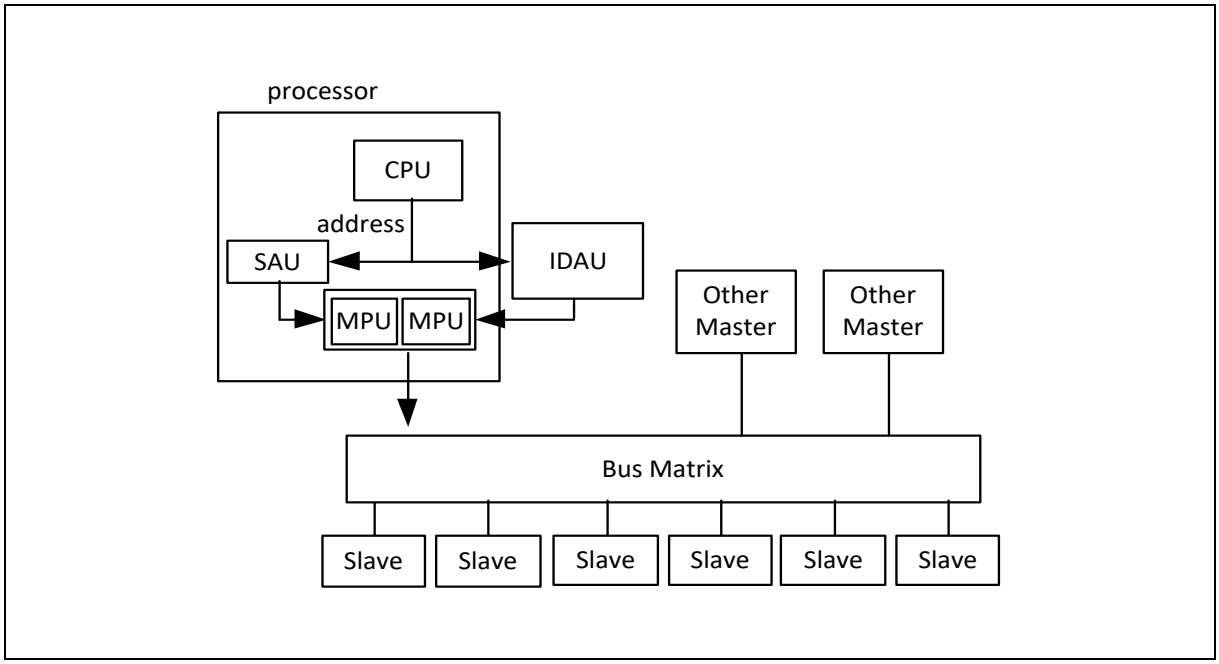


Figure 6.4-11 IDAU Block Diagram

6.4.6 SRAM Memory Organization

This chip supports embedded SRAM with a total of 1344 Kbytes size and one 8K SRAM in low power domain. The SRAM organization is separated into six sections: SRAM0, SRAM1, SRAM2, TCM (tighly couple memory), SRAM3 and LPSRAM. The two in front SRAM have 1024 Kbytes address space, the 3rd SRAM has 320Kbyte address space. The 3 SRAM macro lcate in AXI bus interface. The TCM directly connect from M55 TCM Interfaces. The SRAM3 has 8Kbyte address space and it is located in 32-Bit 200 MHz AHB bus and LPSRAM has 8Kbyte address space and it is located in 32-Bit 100M AHB bus.

- Supports total 1344 Kbytes SRAM and 8K SRAM in Low power domain
- Supports byte / half word / word write/ doble word access
- Support 64 Kbytes parity error functon in region 0

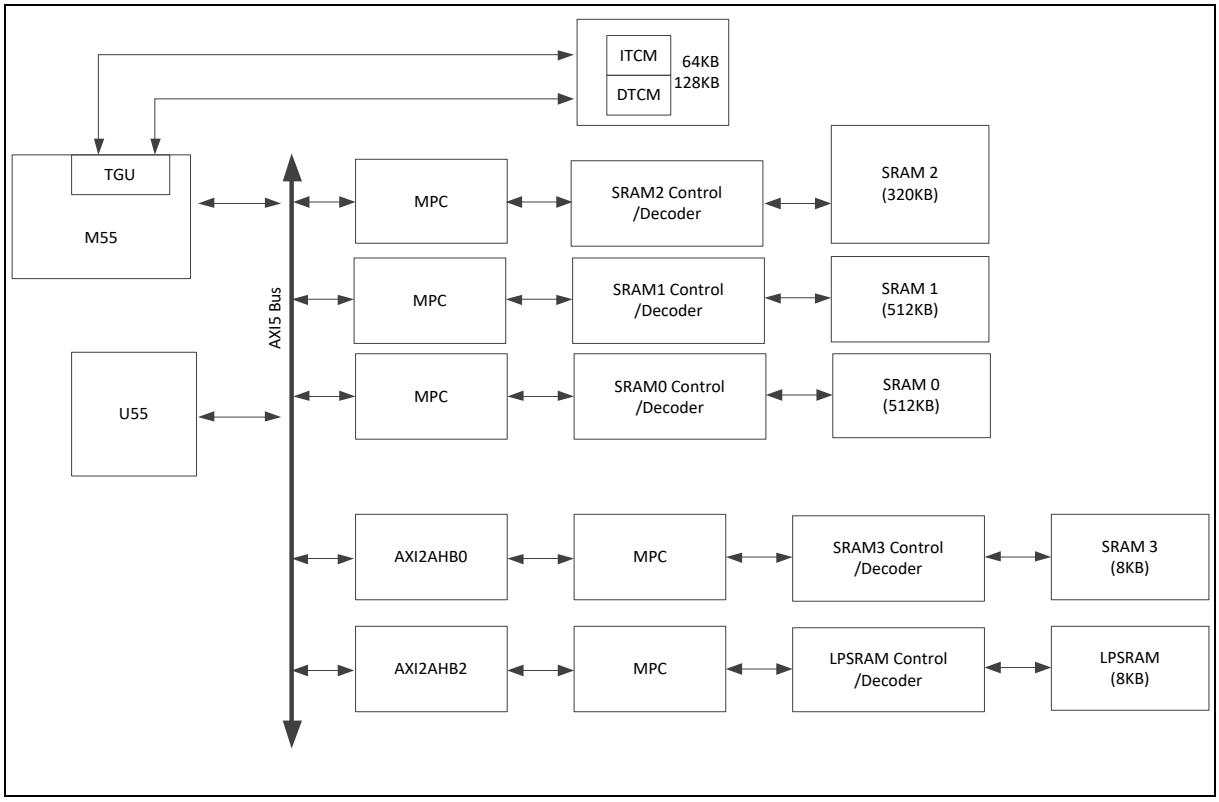


Figure 6.4-12 The structure of SRAM Block Diagram in System

Figure 6.4-12 shows the SRAM organization. There are five SRAM regions. All of region 0~1 are addressed to 512 Kbytes, SRAM2 is 320K and the region 3 and LPSRAM are addressed to 8 Kbytes.

The region 0 address space is from 0x2010_0000 to 0x2017_FFFF(Secure) or 0x3010_0000 to 0x3017_FFFF(Non-secure). The first 64 Kbytes supports parity error in region 0. The region 1 address space is from 0x2018_0000 to 0x201F_FFFF(Secure) or 0x3018_0000 to 0x301F_FFFF(Non-secure). The region 2 address space is from 0x2020_0000 to 0x2024_FFFF(Secure) or 0x3020_0000 to 0x3024_FFFF(Non-secure). The region 3 address space is from 0x2030_0000 to 0x2030_1FFF(Secure) or 0x3030_0000 to 0x3030_1FFF(Non-secure). The region 4 (LPSRAM) which is located in low power domain and its address space is from 0x2031_0000 to 0x2031_1FFF(Secure) or 0x3031_0000 to 0x3031_1FFF(Non-secure). The ITCM address space is from 0x0000_0000 to 0x0000_FFFF (Secure) or 0x1000_0000 to 0x1000_FFFF (Non-Secure) and DTCM address space is from 0x2000_0000 to ox2001_FFFF(Secure) or 0x3000_0000 to ox3001_FFFF(Non-Secure).

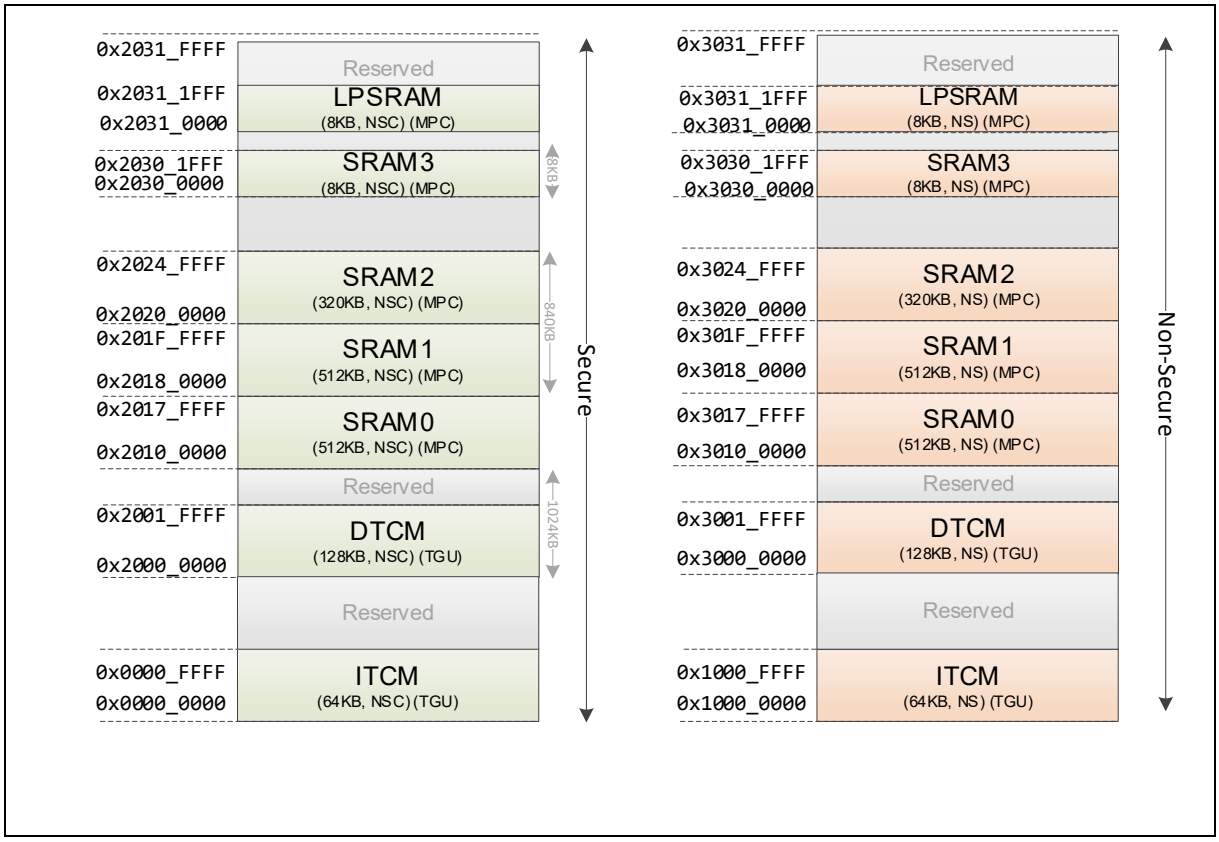


Figure 6.4-13 SRAM Memory Organization

The TCM includes I-TCM and DTCM. ITCM is up to 64 Kbytes and DTCM is up to 128 Kbytes.

For ITCM and DTCM, Table 6.4-4 lists the detailed information.

ITCM			**DTCM**		
StartAddr	EndAddr	Size (KB)	StartAddr	EndAddr	Size (KB)
0x0000_0000	0x0000_FFFF	64	0x2000_0000	0x2001_FFFF	128

Table 6.4-4 Configure Table for TCM

For SRAM1, SRAM3 and LPSRAM are general SRAM macro. The 512 Kbytes SRAM1 is located in 0x2018_0000, the 8 Kbytes SRAM3 is located in 0x20300000 and the 8 Kbytes LPSRAM is located in 0x2031_0000.

SRAM Power Control

All of SRAM have marco retention and power shut down function. It can be configured to retention or power shut down mode by system SRAM power mode controller registers SRAMxPMS (PMC_SYSRB0PC[x*2+1:x*2+0]~ PMC_SYSRB3PC[x*2+1:x*2+0]). When chip is in power down wake up, the SRAM marcos wake up after the PCBUSY flag (PMC_SYSRB0PC[31]~ PMC_SYSRB3PC[31]) goes to LOW.

6.4.7 Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator), HIRC trim (48 MHz RC oscillator) and MIRC trim (1 MHz RC oscillator) according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % /0.5% /0.75% /1% selected by ACCURSEL (SYS_TCTL48M[3:2]/ SYS_TCTL12M[3:2]/ SYS_TCTLMIRC[3:2]) deviation within all temperature ranges.

For some application needs an accurate 12 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL12M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL12M[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS12M[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_TCTL12M[3:2]) set.

For some application needs an accurate 48 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTL48M[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTL48M[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_TCTL48M[3:2]) set.

For some application needs an accurate 1 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_TCTLMIRC[10] reference clock selection) to “1”, set FREQSEL (SYS_TCTLMIRC[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_TISTSMIRC[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_TCTLMIRC[3:2]) set.

RC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock are not stable or the system go into power down, RC trim will not be enable.

6.4.8 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These write-protected system control registers, as listed in Table 6.4-5, have write-protection after the power-on reset till user disables register protection.

Before writing to these protected registers, user has to unlock the write-protected mechanism by writing a register protection disable sequence to the REGLCTL register. The register protection disable sequence is writing the data “59h”, “16h” “88h” sequentially. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

Once a register protection disable sequence is writing to the REGLCTL register successfully, These write-protected registers will be unlocked and able to accept write access. It’s recommended to locked these registers by writing any value to REGLCTL register.

6.4.8.1 Register Lock Control mechanism with Trustzone

For this chip, due to Trustzone technology, system resources are divided into secure and non-secure, leading to type of register of peripheral is either secure or non-secure. Secure registers exist in 0x4nnn_nnnn region (i.e. bit[28] is 0), while non-secure registers exist in 0x5nnn_nnnn region (i.e. bit[28] is 1).

The security types of registers are defined by which peripheral they belong to. Secure peripheral has only secure registers while non-secure peripheral has only non-secure registers. Note that shared registers in some peripherals are also defined as non-secure registers. Refer to **SCU "Memory Access Policy"** section for more details.

There are two REGLCTL registers in system. Secure REGLCTL is SYS_REGLCTL register at address 0x40000100 for secure code to unlock write-protection of both secure and non-secure registers; Non-secure REGLCTL is SYS_REGLCTL register at address 0x50000100, which can be seen as the non-secure alias address of SYS_REGLCTL and is used for non-secure code to unlock write-protection of non-secure registers. Note that address listed in Table 6.4-5 is the address of secure register, for non-secure register, the first nibble of the address is 0x5.

Item	Security Type	Secure Address	Non-Secure Address
SYS_RSTCTL	Secure and Non-secure	0x4000_0004	0x5000_0004
SYS_VTORSET	Secure	0x4000_000C	-
SYS_BODCTL	Secure	0x4000_0020	-
SYS_BODSTS	Secure	0x4000_0024	-
SYS_PORCTL	Secure	0x4000_0028	-
SYS_VREFCTL	Secure	0x4000_002C	-
SYS_USBPHY	Secure	0x4000_0034	-
SYS_DBUSCTL	Secure	0x4000_0040	-
SYS_ACMPRST	Secure	0x4000_0200	-
SYS_AWFRST	Secure	0x4000_0204	-
SYS_BPWMRST	Secure	0x4000_0208	-
SYS_CANFDRST	Secure	0x4000_020C	-
SYS_CCAPRST	Secure	0x4000_0210	-
SYS_CRCRST	Secure	0x4000_0214	-
SYS_CRYPTORST	Secure	0x4000_0218	-
SYS_DACRST	Secure	0x4000_021C	-
SYS_DMICRST	Secure	0x4000_0220	-
SYS_EADCRST	Secure	0x4000_0224	-
SYS_EBIRST	Secure	0x4000_0228	-
SYS_ECAPRST	Secure	0x4000_022C	-
SYS_EMACRST	Secure	0x4000_0230	-
SYS_EPWMRST	Secure	0x4000_0234	-
SYS_EQEIRST	Secure	0x4000_0238	-
SYS_FMCRST	Secure	0x4000_023C	-
SYS_GDMARST	Secure	0x4000_0240	-
SYS_GPIORST	Secure	0x4000_0244	-
SYS_HSOTGRST	Secure	0x4000_0248	-

SYS_HSUSBDRST	Secure	0x4000_024C	-
SYS_HSUSBHRST	Secure	0x4000_0250	-
SYS_I2CRST	Secure	0x4000_0254	-
SYS_I2SRST	Secure	0x4000_0258	-
SYS_I3CRST	Secure	0x4000_025C	-
SYS_KDFRST	Secure	0x4000_0260	-
SYS_KPIRST	Secure	0x4000_0264	-
SYS_KSRST	Secure	0x4000_0268	-
SYS_LPADCRST	Secure	0x4000_026C	-
SYS_LPPDMARST	Secure	0x4000_0270	-
SYS_LPGPIORST	Secure	0x4000_0274	-
SYS_LPI2CRST	Secure	0x4000_0278	-
SYS_LPSPIRST	Secure	0x4000_027C	-
SYS_LPTMRRST	Secure	0x4000_0280	-
SYS_LPUARTRST	Secure	0x4000_0284	-
SYS_OTFCRST	Secure	0x4000_0288	-
SYS_OTGRST	Secure	0x4000_028C	-
SYS_PDMARST	Secure	0x4000_0290	-
SYS_PSIORST	Secure	0x4000_0294	-
SYS_QSPIRST	Secure	0x4000_0298	-
SYS_RTCRST	Secure	0x4000_029C	-
SYS_SCRST	Secure	0x4000_02A0	-
SYS_SCURST	Secure	0x4000_02A4	-
SYS_SDHRST	Secure	0x4000_02A8	-
SYS_SPIRST	Secure	0x4000_02AC	-
SYS_SPIMRST	Secure	0x4000_02B0	-
SYS_TMRRST	Secure	0x4000_02C0	-
SYS_TRNGRST	Secure	0x4000_02C4	-
SYS_TTMRRST	Secure	0x4000_02C8	-
SYS_UARTRST	Secure	0x4000_02CC	-
SYS_USBDRST	Secure	0x4000_02D0	-
SYS_USBHRST	Secure	0x4000_02D4	-
SYS_USCIRST	Secure	0x4000_02D8	-
SYS_UTCPDRST	Secure	0x4000_02DC	-
SYS_NMIEN	Secure	0x4000_0500	-

SYS_SRAMBCTL	Secure	0x4000_0E90	-
CLK_SRCCTL	Secure and Non-secure	0x4000_1000	0x5000_1000
CLK_MIRCCTL	Secure and Non-secure	0x4000_1008	0x5000_1008
CLK_HIRCCTL	Secure	0x4000_100C	
CLK_HXTCTL	Secure	0x4000_1010	
CLK_HIRC48MCTL	Secure	0x4000_1014	
CLK_APLL0CTL	Secure and Non-secure	0x4000_1018	0x5000_1018
CLK_APLL0SEL	Secure and Non-secure	0x4000_101C	0x5000_101C
CLK_APLL1CTL	Secure and Non-secure	0x4000_1020	0x5000_1020
CLK_APLL1SEL	Secure and Non-secure	0x4000_1024	0x5000_1024
CLK_CLKDSTS	Secure	0x4000_1034	
CLK_SCLKSEL	Secure and Non-secure	0x4000_1400	0x5000_1400
CLK_BPWMSEL	Secure and Non-secure	0x4000_1404	0x5000_1404
CLK_CANFDSEL	Secure and Non-secure	0x4000_1408	0x5000_1408
CLK_CCAPSEL	Secure and Non-secure	0x4000_140C	0x5000_140C
CLK_CLKOSEL	Secure and Non-secure	0x4000_1410	0x5000_1410
CLK_DMICSEL	Secure and Non-secure	0x4000_1414	0x5000_1414
CLK_EADCSEL	Secure and Non-secure	0x4000_1418	0x5000_1418
CLK_EPWMSEL	Secure and Non-secure	0x4000_141C	0x5000_141C
CLK_FMCSEL	Secure and Non-secure	0x4000_1420	0x5000_1420
CLK_I2SSEL	Secure and Non-secure	0x4000_1424	0x5000_1424
CLK_I3CSEL	Secure and Non-secure	0x4000_1428	0x5000_1428
CLK_KPISEL	Secure and Non-secure	0x4000_142C	0x5000_142C
CLK_LPADCSEL	Secure and Non-secure	0x4000_1430	0x5000_1430
CLK_LPSPISEL	Secure and Non-secure	0x4000_1434	0x5000_1434
CLK_LPTMRSEL	Secure and Non-secure	0x4000_1438	0x5000_1438
CLK_LPUARTSEL	Secure and Non-secure	0x4000_143C	0x5000_143C
CLK_PSIO	Secure and Non-secure	0x4000_1440	0x5000_1440
CLK_QSPISEL	Secure and Non-secure	0x4000_1444	0x5000_1444
CLK_SCSEL	Secure and Non-secure	0x4000_1448	0x5000_1448
CLK_SDHSEL	Secure and Non-secure	0x4000_144C	0x5000_144C
CLK_SPISEL	Secure and Non-secure	0x4000_1450	0x5000_1450
CLK_STSEL	Secure and Non-secure	0x4000_1454	0x5000_1454
CLK_TMRSEL	Secure and Non-secure	0x4000_1458	0x5000_1458
CLK_TTMRSEL	Secure and Non-secure	0x4000_145C	0x5000_145C

CLK_UARTSEL0	Secure and Non-secure	0x4000_1460	0x5000_1460
CLK_UARTSEL1	Secure and Non-secure	0x4000_1464	0x5000_1464
CLK_USBSEL	Secure and Non-secure	0x4000_1468	0x5000_1468
CLK_WDTSEL	Secure and Non-secure	0x4000_146C	0x5000_146C
CLK_WWDTSEL	Secure and Non-secure	0x4000_1470	0x5000_1470
NMIEN	Secure	0x4000_0300	
FMC_ISPCTL	Secure and Non-secure	0x4000_C000	
FMC_ISPTRG	Secure and Non-secure	0x4000_C010	
FMC_ISPSTS	Secure and Non-secure	0x4000_C040	
FMC_CYCCTL	Secure	0x4000_C04C	
WDT0_CTL	Secure or Non-secure	0x4044_7000	0x5044_7000
WDT0_ALTCTL	Secure or Non-secure	0x4044_7004	0x5044_7004
WDT1_CTL	Secure or Non-secure	0x4044_8000	0x5044_8000
WDT1_ALTCTL	Secure or Non-secure	0x4044_8004	0x5044_8004
TIMER0_CTL	Secure or Non-secure	0x4025_6000	0x5025_6000
TIMER1_CTL	Secure or Non-secure	0x4025_6100	0x5025_6100
TIMER2_CTL	Secure or Non-secure	0x4029_5000	0x5029_5000
TIMER3_CTL	Secure or Non-secure	0x4029_5100	0x5029_5100
TIMER0_PWMDTCTL	Secure or Non-secure	0x4025_6040	0x5025_6040
TIMER1_PWMDTCTL	Secure or Non-secure	0x4025_6140	0x5025_6140
TIMER2_PWMDTCTL	Secure or Non-secure	0x4029_5040	0x5029_5040
TIMER3_PWMDTCTL	Secure or Non-secure	0x4029_5140	0x5029_5140
TIMER0_PWMBRKCTL	Secure or Non-secure	0x4025_6058	0x5025_6058
TIMER1_PWMBRKCTL	Secure or Non-secure	0x4025_6158	0x5025_6158
TIMER2_PWMBRKCTL	Secure or Non-secure	0x4029_5058	0x5029_5058
TIMER3_PWMBRKCTL	Secure or Non-secure	0x4029_5158	0x5029_5158
TIMER0_PWMSWBRK	Secure or Non-secure	0x4025_6070	0x5025_6070
TIMER1_PWMSWBRK	Secure or Non-secure	0x4025_6170	0x5025_6170
TIMER2_PWMSWBRK	Secure or Non-secure	0x4029_5070	0x5029_5070
TIMER3_PWMSWBRK	Secure or Non-secure	0x4029_5170	0x5029_5170
TIMER0_PWMINTSTS1	Secure or Non-secure	0x4025_607C	0x5025_607C
TIMER1_PWMINTSTS1	Secure or Non-secure	0x4025_617C	0x5025_617C
TIMER2_PWMINTSTS1	Secure or Non-secure	0x4029_507C	0x5029_507C
TIMER3_PWMINTSTS1	Secure or Non-secure	0x4029_518C	0x5029_517C
LPTMR0_CTL	Secure or Non-secure	0x4044_0000	0x5044_0000

LPTMR1_CTL	Secure or Non-secure	0x4044_0100	0x5044_0100
LPTMR0_PWMCTL	Secure or Non-secure	0x4044_0040	0x5044_0040
LPTMR1_PWMCTL	Secure or Non-secure	0x4044_0140	0x5044_0140
TTMR0_CTL	Secure or Non-secure	0x4044_1000	0x5044_1000
TTMR1_CTL	Secure or Non-secure	0x4044_1100	0x5044_1100
LPADC_ADCR[12]	Secure or Non-secure	0x4044_2080	0x5044_2080
LPADC_ADTEST[28]	Secure or Non-secure	0x4044_20FC	0x5044_20FC
DAC0_TEST	Secure or Non-secure	0x4025_7FF0	0x5025_7FF0
DAC1_TEST	Secure or Non-secure	0x4025_7FF8	0x5025_7FF8
BPWM0_CTL0[31:30]	Secure or Non-secure	0x4024_3000	0x5024_3000
BPWM1_CTL0[31:30]	Secure or Non-secure	0x4028_3000	0x5028_3000
EPWM0_CTL0[31:30]	Secure or Non-secure	0x4024_2000	0x5024_2000
EPWM0_DTCT0_1	Secure or Non-secure	0x4024_2070	0x5024_2070
EPWM0_DTCT2_3	Secure or Non-secure	0x4024_2074	0x5024_2074
EPWM0_DTCT4_5	Secure or Non-secure	0x4024_2078	0x5024_2078
EPWM0_FDTCT2	Secure or Non-secure	0x4024_22B8	0x5024_22B8
EPWM0_RFDTCT	Secure or Non-secure	0x4024_22C0	0x5024_22C0
EPWM0_BRKCTL0_1	Secure or Non-secure	0x4024_20C8	0x5024_20C8
EPWM0_BRKCTL2_3	Secure or Non-secure	0x4024_20CC	0x5024_20CC
EPWM0_BRKCTL4_5	Secure or Non-secure	0x4024_20D0	0x5024_20D0
EPWM0_SWBRK	Secure or Non-secure	0x4024_20DC	0x5024_20DC
EPWM0_INTEN1	Secure or Non-secure	0x4024_20E4	0x5024_20E4
EPWM0_INTSTS1	Secure or Non-secure	0x4024_20EC	0x5024_20EC
EPWM0_SELFTEST	Secure or Non-secure	0x4024_2300	0x5024_2300
EPWM1_CTL0[31:30]	Secure or Non-secure	0x4028_2000	0x5028_2000
EPWM1_DTCT0_1	Secure or Non-secure	0x4028_2070	0x5028_2070
EPWM1_DTCT2_3	Secure or Non-secure	0x4028_2074	0x5028_2074
EPWM1_DTCT4_5	Secure or Non-secure	0x4028_2078	0x5028_2078
EPWM1_FDTCT2	Secure or Non-secure	0x4028_22B8	0x5028_22B8
EPWM1_RFDTCT	Secure or Non-secure	0x4028_22C0	0x5028_22C0
EPWM1_BRKCTL0_1	Secure or Non-secure	0x4028_20C8	0x5028_20C8
EPWM1_BRKCTL2_3	Secure or Non-secure	0x4028_20CC	0x5028_20CC
EPWM1_BRKCTL4_5	Secure or Non-secure	0x4028_20D0	0x5028_20D0
EPWM1_SWBRK	Secure or Non-secure	0x4028_20DC	0x5028_20DC
EPWM1_INTEN1	Secure or Non-secure	0x4028_20E4	0x5028_20E4

EPWM1_INTSTS1	Secure or Non-secure	0x4028_20EC	0x5028_20EC
EPWM1_SELFTEST	Secure or Non-secure	0x4028_2300	0x5028_2300

Table 6.4-5 List of Registers with Write Protect

6.4.9 System Timer (SysTick)

The Cortex-M55 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*ArmCortex-M55 Technical Reference Manual*" and "*Armv8-M Architecture Reference Manual*".

6.4.10 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and sub priority fields.
- Interrupt tail-chaining.
- An external Non maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.4.10.1 Exception Model and System Interrupt Map

Table 6.4-6 lists the exception model supported in this chip. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-4
NMI	2	0x00000008	-2
Secure Hard Fault (when BFHFNMINS(AIRCR[13]) is 0)	3	0x0000000C	-3
Non-secure Hard Fault (when BFHFNMINS(AIRCR[13]) is 1)	3	0x0000000C	-1
Reserved	4 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable

Reserved	12 ~ 13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ151)	16 ~ 161	0x00000000 + (Vector Number)*4	Configurable

Table 6.4-6 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PMC_INT	Power mode controller interrupt
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	ISP_INT	FMC ISP interrupt
22	6	RTC_INT	Real time clock interrupt
23	7	RTC_TAMPER_INT	Backup register tamper interrupt
24	8	WDT0_INT	Watchdog Timer 0 interrupt
25	9	WWDT0_INT	Window Watchdog Timer 0 interrupt
26	10	Reserved	Reserved
27	11	WDT1_INT	Watchdog Timer 1 interrupt
28	12	WWDT1_INT	Window Watchdog Timer 1 interrupt
29	13	NPU_INT	Neural Network Processor interrupt
30	14	EINT0	External interrupt from PA.6 or PB.5 pins
31	15	EINT1	External interrupt from PA.7 or PB.4 pins
32	16	EINT2	External interrupt from PB.3 or PC.6 pins
33	17	EINT3	External interrupt from PB.2 or PC.7 pins
34	18	EINT4	External interrupt from PA.8 or PB.6 pins
35	19	EINT5	External interrupt from PB.7 or PD.12
36	20	GPA_INT	External interrupt from PA[15:0] pin
37	21	GPB_INT	External interrupt from PB[15:0] pin
38	22	GPC_INT	External interrupt from PC[15:0] pin
39	23	GPD_INT	External interrupt from PD[15:0] pin
40	24	GPE_INT	External interrupt from PE[15:0] pin

41	25	GPF_INT	External interrupt from PF[15:0] pin
42	26	GPG_INT	External interrupt from PG[15:0] pin
43	27	GPH_INT	External interrupt from PH15:0] pin
44	28	GPI_INT	External interrupt from PI[15:0] pin
45	29	GPJ_INT	External interrupt from PJ[15:0] pin
46	30	BRAKE0_INT	EPWM0 brake interrupt
47	31	EPWM0_P0_INT	EPWM0 pair 0 interrupt
48	32	EPWM0_P1_INT	EPWM0 pair 1 interrupt
49	33	EPWM0_P2_INT	EPWM0 pair 2 interrupt
50	34	BRAKE1_INT	EPWM1 brake interrupt
51	35	EPWM1_P0_INT	EPWM1 pair 0 interrupt
52	36	EPWM1_P1_INT	EPWM1 pair 1 interrupt
53	37	EPWM1_P2_INT	EPWM1 pair 2 interrupt
54	38	BPWM0_INT	BPWM0 interrupt
55	39	BPWM1_INT	BPWM1 interrupt
56	40	Reserved	Reserved
57	41	PDMA0_INT	PDMA 0 interrupt
58	42	PDMA1_INT	PDMA 1 interrupt
59	43	LPPDMA_INT	Low Power PDMA interrupt
60	44	SCU_INT	SCU interrupt
61	45	Reserved	Reserved
62	46	KS_INT	Key store interrupt
63	47	TMR0_INT	Timer 0 interrupt
64	48	TMR1_INT	Timer 1 interrupt
65	49	TMR2_INT	Timer 2 interrupt
66	50	TMR3_INT	Timer 3 interrupt
67	51	LPTMR0_INT	Low Power Time 0 interrupt
68	52	LPTMR1_INT	Low Power Time 0 interrupt
69	53	Reserved	Reserved
70	54	TTMR0_INT	Tick Timer 0 interrupt
71	55	TTMR1_INT	Tick Timer 1 interrupt
72	56	USBH0_INT	USB host 0 interrupt
73	57	USBH1_INT	USB host 1 interrupt
74	58	USBD_INT	USB device interrupt
75	59	USBOTG_INT	USB OTG interrupt

76	60	HSUSBH_INT	High speed USB host interrupt
77	61	HSUSBD_INT	High speed USB device interrupt
78	62	HSOTG_INT	High speed USB OTG interrupt
79	63	EMAC_INT	EMAC interrupt
80	64	QSPI0_INT	QSPI0 interrupt
81	65	QSPI1_INT	QSPI1 interrupt
82	66	SPI0_INT	SPI0 interrupt
83	67	SPI1_INT	SPI1 interrupt
84	68	SPI2_INT	SPI2 interrupt
85	69	SPI3_INT	SPI3 interrupt
86	70	Reserved	Reserved
87	71	LPSPI0_INT	Low Power SPI0 interrupt
88	72	Reserved	Reserved
89	73	SPIM0_INT	SPIM0 interrupt
90	74	Reserved	Reserved
91	75	UART0_INT	UART0 interrupt
92	76	UART1_INT	UART1 interrupt
93	77	UART2_INT	UART2 interrupt
94	78	UART3_INT	UART3 interrupt
95	79	UART4_INT	UART4 interrupt
96	80	UART5_INT	UART5 interrupt
97	81	UART6_INT	UART6 interrupt
98	82	UART7_INT	UART7 interrupt
99	83	UART8_INT	UART8 interrupt
100	84	UART9_INT	UART9 interrupt
101	85	Reserved	Reserved
102	86	Reserved	Reserved
103	87	Reserved	Reserved
104	88	EINT6	External interrupt from PB.8 or PD.11 pins
105	89	EINT7	External interrupt from PB.9 or PD.10
106	90	LPUART_INT	Low Power UART interrupt
107	91	Reserved	Reserved
108	92	I2C0_INT	I2C0 interrupt
109	93	I2C1_INT	I2C1 interrupt
110	94	I2C2_INT	I2C2 interrupt

111	95	I2C3_INT	I2C3 interrupt
112	96	LPI2C_INT	Low Power I^2C interrupt
113	97	USCI0_INT	USCI0 interrupt
114	98	Reserved	Reserved
115	99	SC0_INT	Smart card host 0 interrupt
116	100	SC1_INT	Smart card host 1 interrupt
117	101	SC2_INT	Smart card host 2 interrupt
118	102	PSIO_INT	PSIO interrupt
119	103	DMIC0_INT	DMIC0 interrupt
120	104	DMIC0_VAD_INT	DMIC0 VAD interrupt
121	105	I2S0_INT	I2S0 interrupt
122	106	I2S1_INT	I2S1 interrupt
123	107	TRNG_INT	TRNG interrupt
124	108	I3C0_INT	I3C0 interrupt
125	109	Reserved	Reserved
126	110	OTFC0_INT	OTFC0 interrupt
127	111	Reserved	Reserved
128	112	KPI_INT	KPI interrupt
129	113	SDH0_INT	SD host 0 interrupt
130	114	SDH1_INT	SD host 1 interrupt
131	115	CCAP_INT	CCAP interrupt
132	116	CRYPTO	Crypto interrupt
133	117	CANFD0_0_INT	CANFD0 interrupt 0
134	118	CANFD0_1_INT	CANFD0 interrupt 1
135	119	CANFD1_0_INT	CANFD1 interrupt 0
136	120	CANFD1_1_INT	CANFD1 interrupt 1
137	121	ACMP01_INT	ACMP0 and ACMP1 interrupt
138	122	ACMP23_INT	ACMP2 and ACMP3 interrupt
139	123	Reserved	Reserved
140	124	Reserved	Reserved
141	125	CRC_INT	CRC interrupt
142	126	EADC0_0_INT	EADC0 interrupt source 0
143	127	EADC0_1_INT	EADC0 interrupt source 1
144	128	EADC0_2_INT	EADC0 interrupt source 2
145	129	EADC0_3_INT	EADC0 interrupt source 3

146	130	Reserved	Reserved
147	131	Reserved	Reserved
148	132	Reserved	Reserved
149	133	Reserved	Reserved
150	134	LPADC0_INT	Low power ADC0 interrupt
151	135	DAC01_INT	DAC0 and DAC1 interrupt
152	136	Reserved	Reserved
153	137	EQEI0_INT	EQEI0 interrupt
154	138	EQEI1_INT	EQEI1 interrupt
155	139	EQEI2_INT	EQEI2 interrupt
156	140	EQEI3_INT	EQEI3 interrupt
157	141	ECAP0_INT	ECAP0 interrupt
158	142	ECAP1_INT	ECAP1 interrupt
159	143	ECAP2_INT	ECAP2 interrupt
160	144	ECAP3_INT	ECAP3 interrupt
161	145	Reserved	Reserved
165	149	AWF_INT	AWF interrupt
166	150	UTCPD	UTCPD interrupt
167	151	Reserved	Reserved
168	152	Reserved	Reserved
169	153	Reserved	Reserved
170	154	Reserved	Reserved
171	155	Reserved	Reserved
172	156	Reserved	Reserved
173	157	Reserved	Reserved
174	158	Reserved	Reserved
175	159	Reserved	Reserved
176	160	GDMA_CH0	GDMA Channel 0 interrupt
177	161	GDMA_CH1	GDMA Channel 1 interrupt

Table 6.4-7 Interrupt Number Table

6.4.10.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset

or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space.

6.4.11 Security Attribution Unit (SAU)

The Arm Cortex-M55 has an security attribution unit (SAU) to support hardware Arm TrustZone technique. This chip supports up to 8 memory regions in SAU for secure code to configure, and provides the memory alias architecture which can work only with proper setting of SAU, IDAU and SCU. IDAU has already defined all memory regions that should be non-secure (refer to the “Address Space Partition” section). Secure code should properly set these regions to non-secure by setting SAU. However, secure code should overwrite NSC regions to secure regions to prevent from being unexpectedly accessed by non-secure code.

SAU can be accessed by secure code. Non-secure access to all SAU registers will be RAZ/WI.

6.4.12 Programmable MBIST Controller (PMC-100)

Arm PMC-100 is a Programmable MBIST Controller which is typically used in functional safety applications and can be used to carry out testing on a periodic basis, such as power on/off. This chip contains Arm PMC-100 to support transparent, in-field testing of SRAMs within the Cortex-M55 during functional operation, without corrupting memory or logic state.

For more detailed information, please refer to the “Arm PMC-100 Programmable MBIST Controller Technical Reference Manual”.

Note: In order to prevent the sensitive information stored in cache from being disclosed, there are two things should be noticed while using the PMC-100 in this chip.

- The registers PMC100_X0 to PMC100_X7 and PMC100_Y0 to PMC100_Y7 are RAZ/WI.
- All the registers of PMC-100 would be inaccessible if there is any XOM region activated in the system.

6.5 Clock Controller

6.5.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(PMC_PWRCTL[8]) and Cortex-M55 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC48M), 12 MHz internal high speed RC oscillator (HIRC) and APLL to reduce the overall system power consumption. Figure 6.5-1 shows the clock generator and the overview of the clock source control.

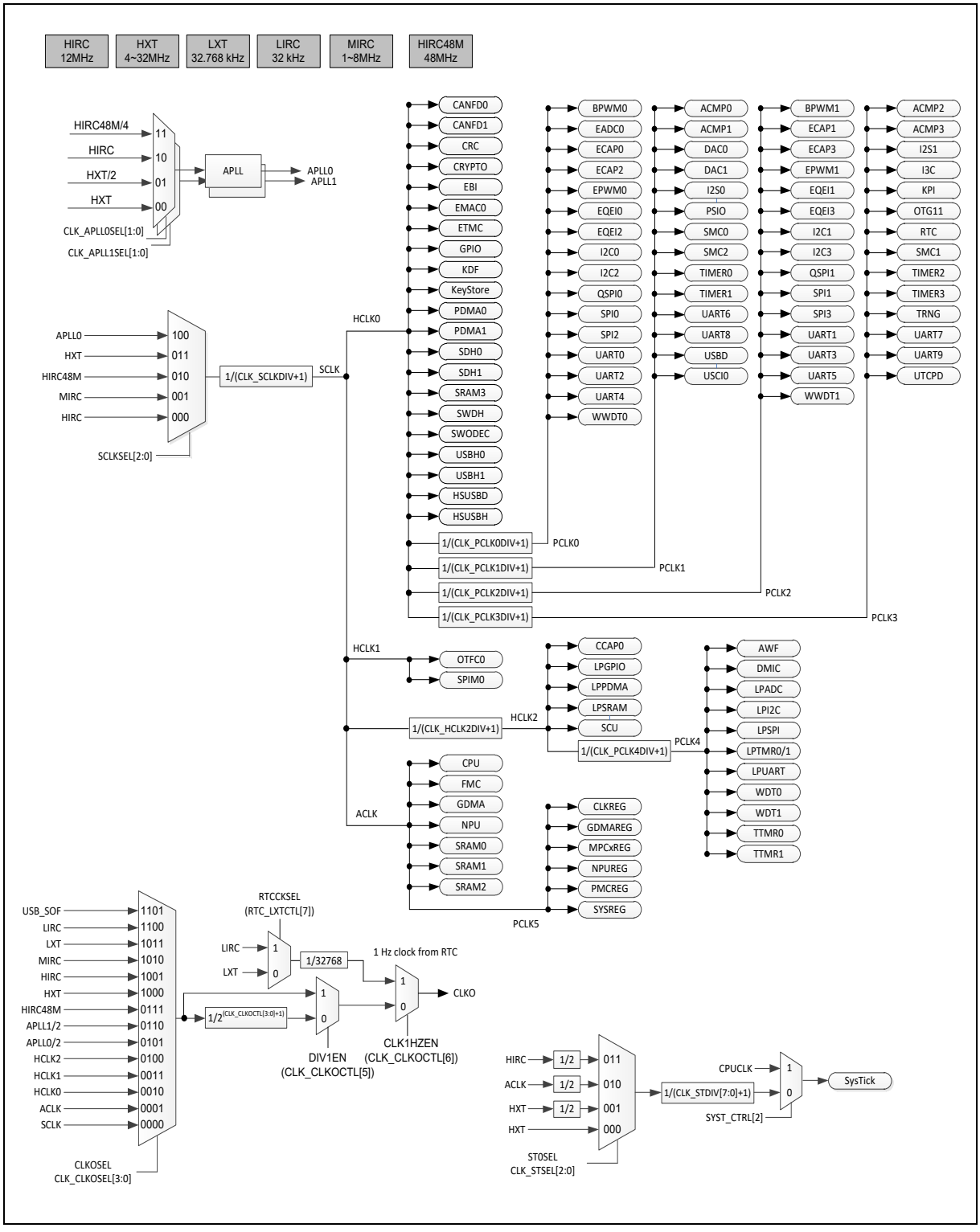


Figure 6.5-1 Clock Generator Global View Diagram (1/5)

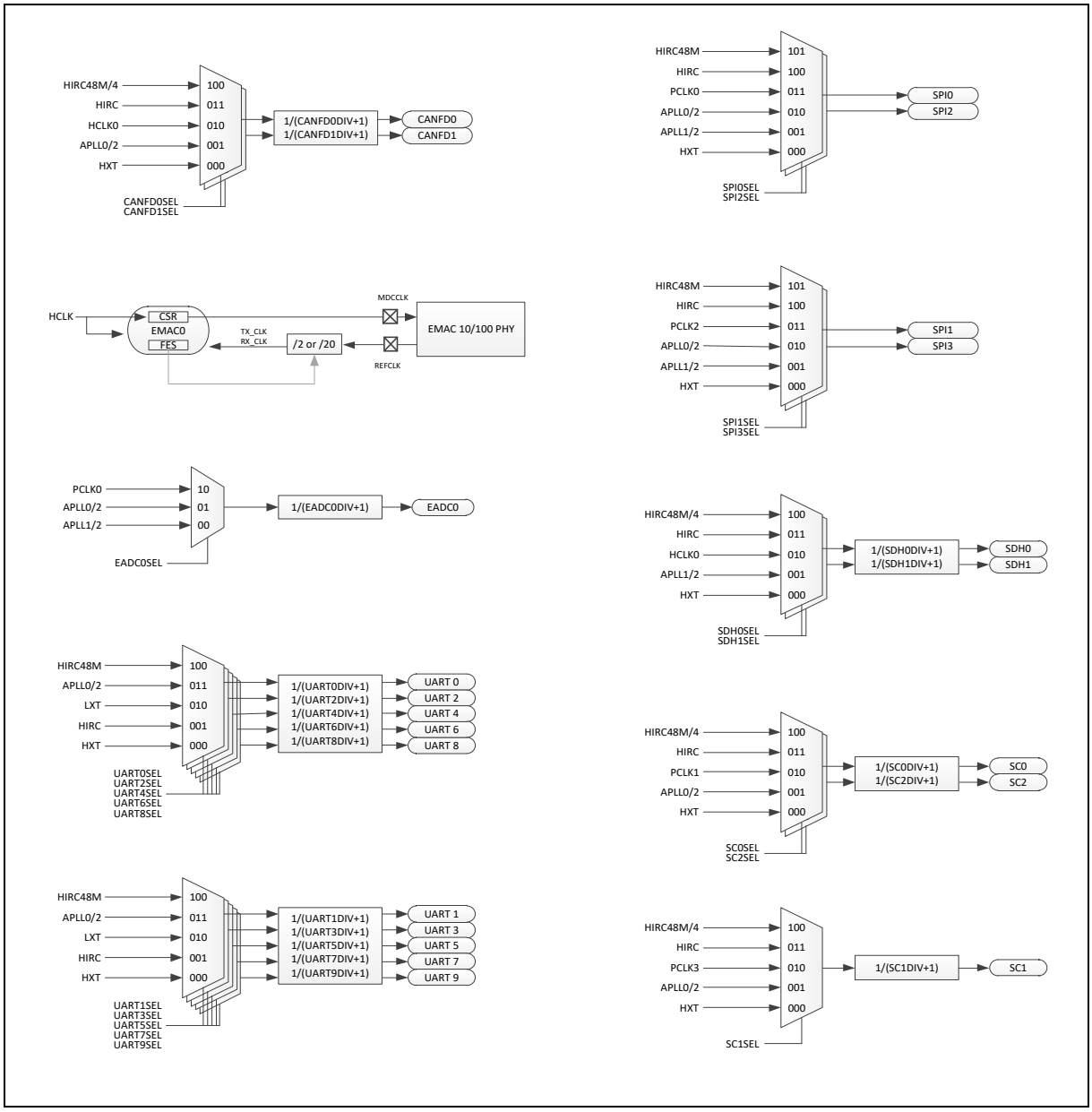


Figure 6.5-2 Clock Generator Global View Diagram (2/5)

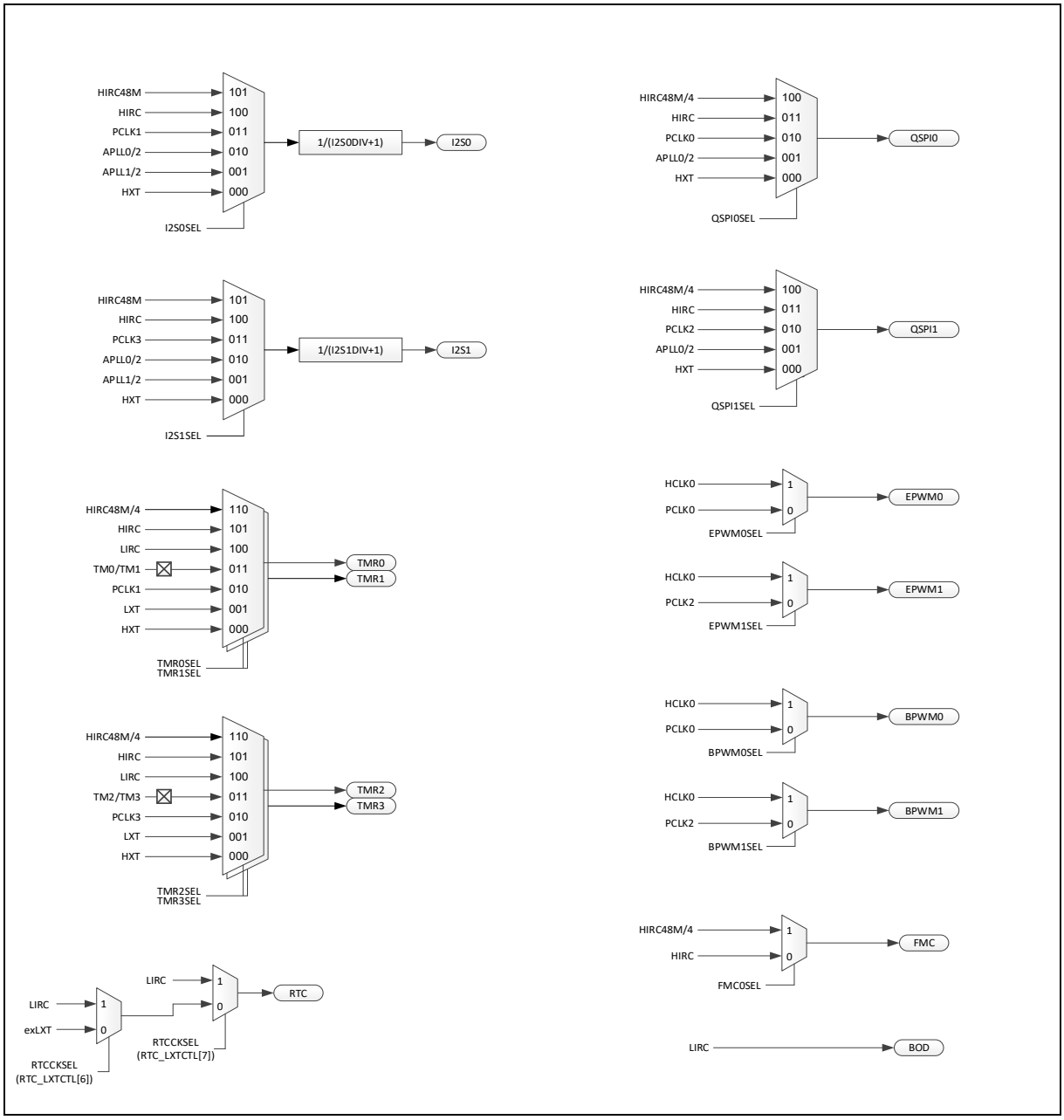


Figure 6.5-3 Clock Generator Global View Diagram (3/5)

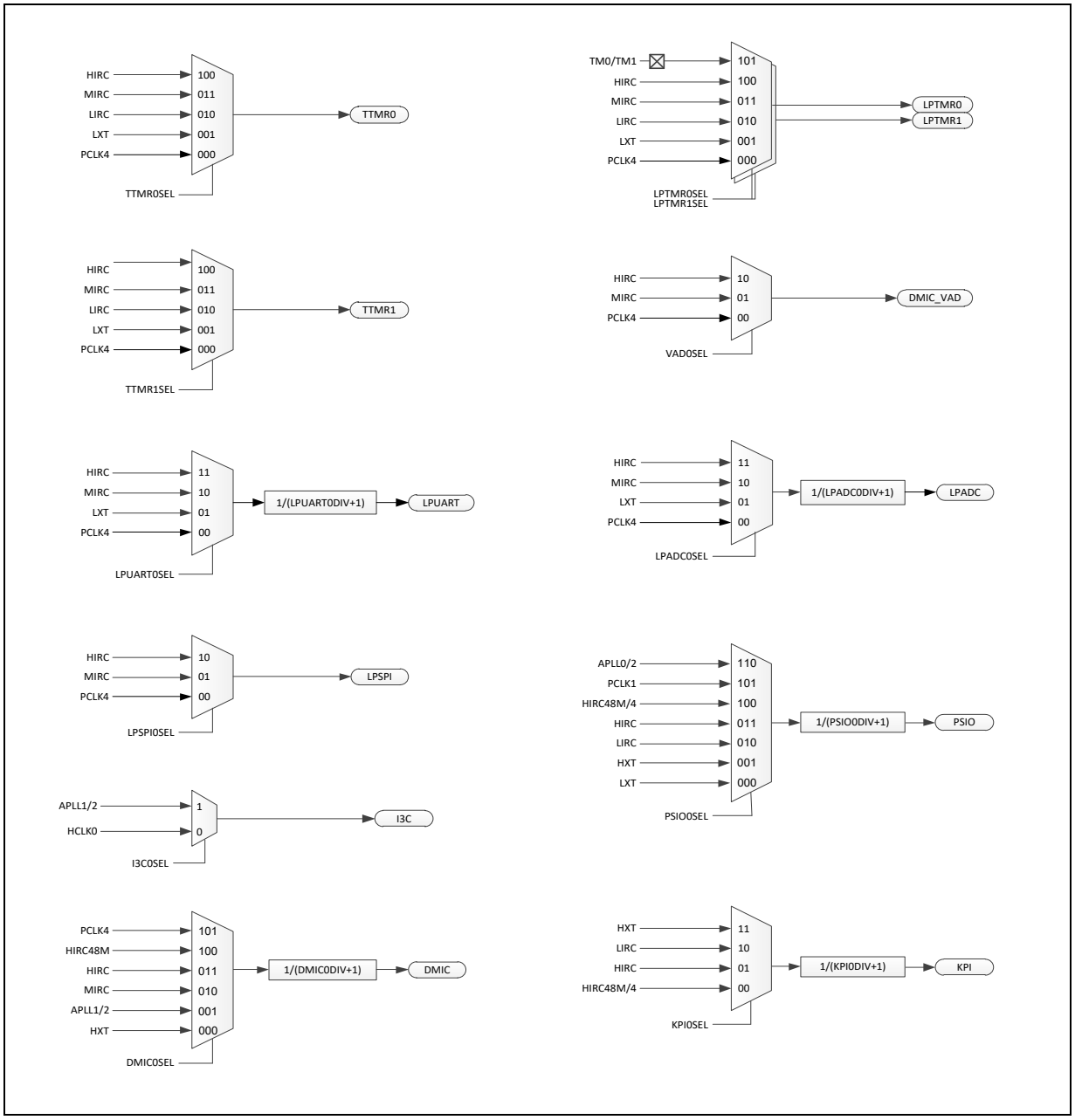


Figure 6.5-4 Clock Generator Global View Diagram (4/5)

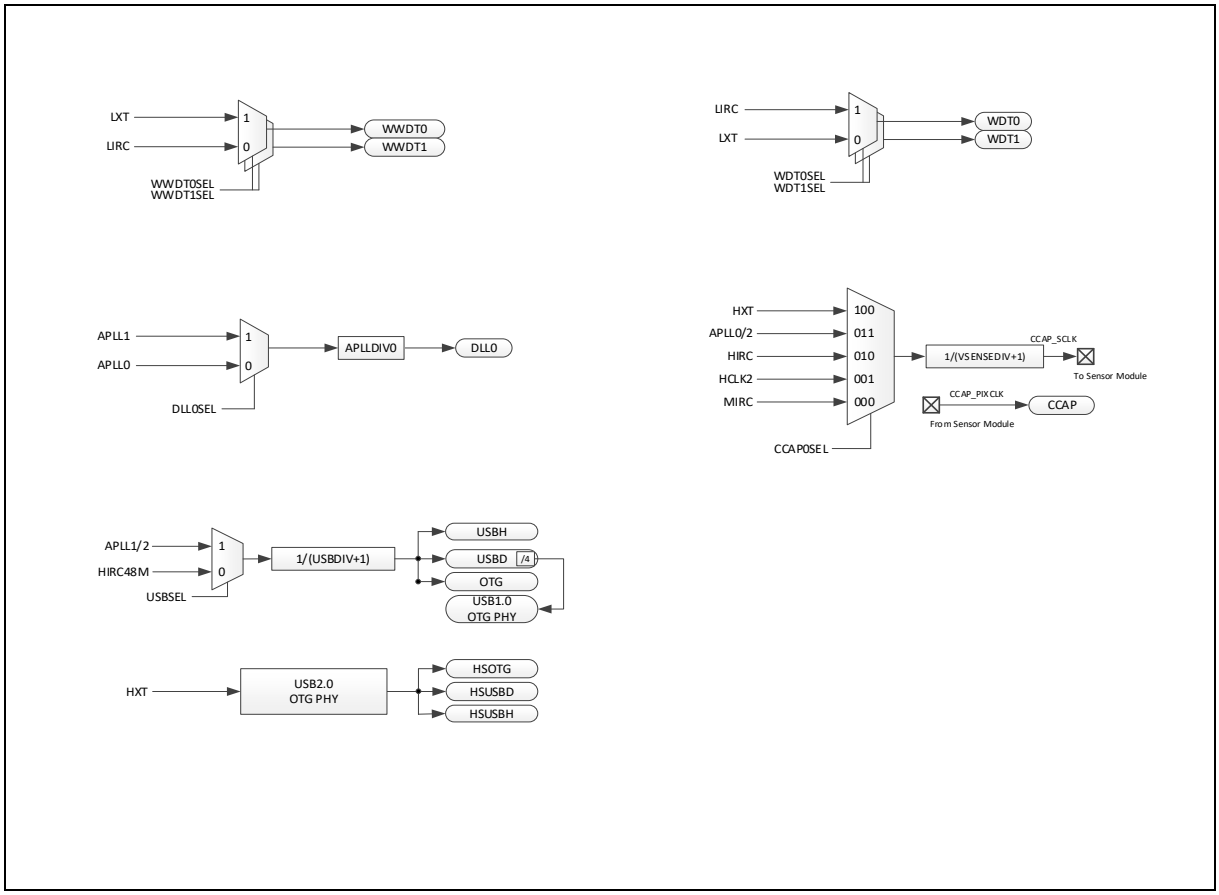


Figure 6.5-5 Clock Generator Global View Diagram (5/5)

Note: The frequency of APLL/2 must not exceed PCLK.

6.5.2 Clock Generator

The clock generator consists of 8 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Two programmable APLL output clock frequency (APLLFOUT), APLL source can be selected from external 4~24 MHz external high speed crystal (HXT), external 24~32 MHz external high speed crystal divide 2 (HXT/2), 12 MHz internal high speed oscillator (HIRC) or 48 MHz internal high speed oscillator divide 4 (HIRC48M/4)
- 12 MHz internal high speed RC oscillator (HIRC)
- 32 kHz internal low speed RC oscillator (LIRC)
- 48 MHz internal high speed RC oscillator (HIRC48M)
- 1~8 MHz internal medium speed RC oscillator (MIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index is set to 1 after stable counter value reach a define value as shown in Table 6.5-1.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.5-2 will auto clear when user disables the clock source.

Besides, the clock stable index of HXT, HIRC48M, APLL0, APLL1 will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
LIRC	1 LIRC clock	31.25us for 32 kHz
LXT	16384 LXT clocks	500ms for 32.768 kHz
MIRC(1M)	4 MIRC clocks (CLK_MIRCCTL[1:0]=0x00) 4 MIRC clocks (CLK_MIRCCTL[1:0]=0x01) 3 MIRC clocks (CLK_MIRCCTL[1:0]=0x10) 3 MIRC clocks (CLK_MIRCCTL[1:0]=0x11)	4us for 1 MHz 4us for 1 MHz 3us for 1 MHz 3us for 1 MHz
MIRC(2M)	6 MIRC clocks (CLK_MIRCCTL[5:4]=0x00) 6 MIRC clocks (CLK_MIRCCTL[5:4]=0x01) 5 MIRC clocks (CLK_MIRCCTL[5:4]=0x10) 5 MIRC clocks (CLK_MIRCCTL[5:4]=0x11)	3us for 2 MHz 3us for 2 MHz 2.5us for 2 MHz 2.5us for 2 MHz
MIRC(4M)	20 MIRC clocks (CLK_MIRCCTL[9:8]=0x00) 17 MIRC clocks (CLK_MIRCCTL[9:8]=0x01) 16 MIRC clocks (CLK_MIRCCTL[9:8]=0x10) 14 MIRC clocks (CLK_MIRCCTL[9:8]=0x11)	5us for 4 MHz 4.25us for 4 MHz 4us for 4 MHz 3.5us for 4 MHz
MIRC(8M)	75 MIRC clocks (CLK_MIRCCTL[13:12]=0x00) 56 MIRC clocks (CLK_MIRCCTL[13:12]=0x01) 48 MIRC clocks (CLK_MIRCCTL[13:12]=0x10) 44 MIRC clocks (CLK_MIRCCTL[13:12]=0x11)	9.38us for 8 MHz 7us for 8 MHz 6us for 8 MHz 5.5us for 8 MHz
HIRC	23 HIRC clocks (CLK_HIRCCTL[1:0]=0x00) 16 HIRC clocks (CLK_HIRCCTL[1:0]=0x01) 14 HIRC clocks (CLK_HIRCCTL[1:0]=0x10) 13 HIRC clocks (CLK_HIRCCTL[1:0]=0x11)	1.92us for 12 MHz 1.33us for 12 MHz 1.17us for 12 MHz 1.08us for 12 MHz
HXT	4096 HXT clocks	341.33us for 12 MHz
HIRC48M	23 HIRC clocks (CLK_HIRC48MCTL[1:0]=0x00) 22 HIRC clocks (CLK_HIRC48MCTL[1:0]=0x01) 21 HIRC clocks (CLK_HIRC48MCTL[1:0]=0x10) 21 HIRC clocks (CLK_HIRC48MCTL[1:0]=0x11)	479.17ns for 48 MHz 458.33ns for 48 MHz 437.5ns for 48 MHz 437.5ns for 48 MHz
APLL0	820 APLL source clocks (CLK_APLL0CTL[29:28]=0x0) 2460 APLL source clocks (CLK_APLL0CTL[29:28]=0x1) 4920 APLL source clocks (CLK_APLL0CTL[29:28]=0x2)	200us for 4 MHz 200us for 12 MHz 200us for 24 MHz
APLL1	820 APLL source clocks (CLK_APLL1CTL[29:28]=0x0) 2460 APLL source clocks (CLK_APLL1CTL[29:28]=0x1) 4920 APLL source clocks (CLK_APLL1CTL[29:28]=0x2)	200us for 4 MHz 200us for 12 MHz 200us for 24 MHz

Table 6.5-1 Clock Stable Count Value Table

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
LIRC	LIRCEN(CLK_SRCCTL[0])	LIRCSTB(CLK_STATUS[0])
LXT	LXTEN(CLK_SRCCTL[1])	LXTSTB(CLK_STATUS[1])
MIRC	MIRCEN(CLK_SRCCTL[2])	MIRCSTB(CLK_STATUS[2])
HIRC	HIRCEN(CLK_SRCCTL[3])	HIRCSTB(CLK_STATUS[3])
HXT	HXTEN(CLK_SRCCTL[4])	HXTSTB(CLK_STATUS[4])
HIRC48M	HIRC48MEN(CLK_SRCCTL[5])	HIRC48MSTB(CLK_STATUS[5])
APLL0	APLL0EN(CLK_SRCCTL[6])	APLL0STB(CLK_STATUS[6])
APLL1	APLL1EN(CLK_SRCCTL[7])	APLL1STB(CLK_STATUS[7])

Table 6.5-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table

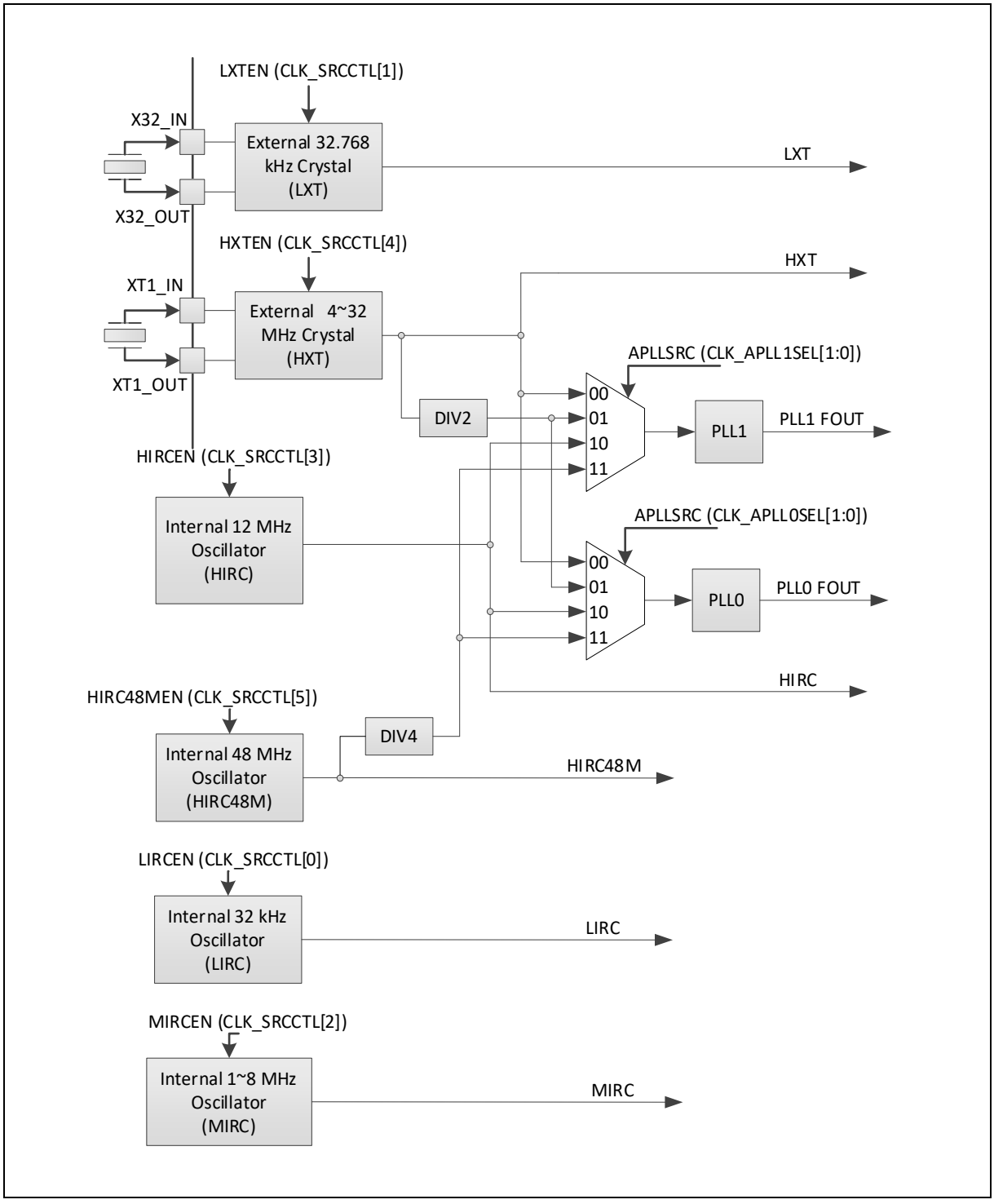


Figure 6.5-5 Clock Generator Block Diagram

6.5.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register SCLKSEL (CLK_SCLKSEL[2:0]). The block diagram is shown in Figure 6.5-6.

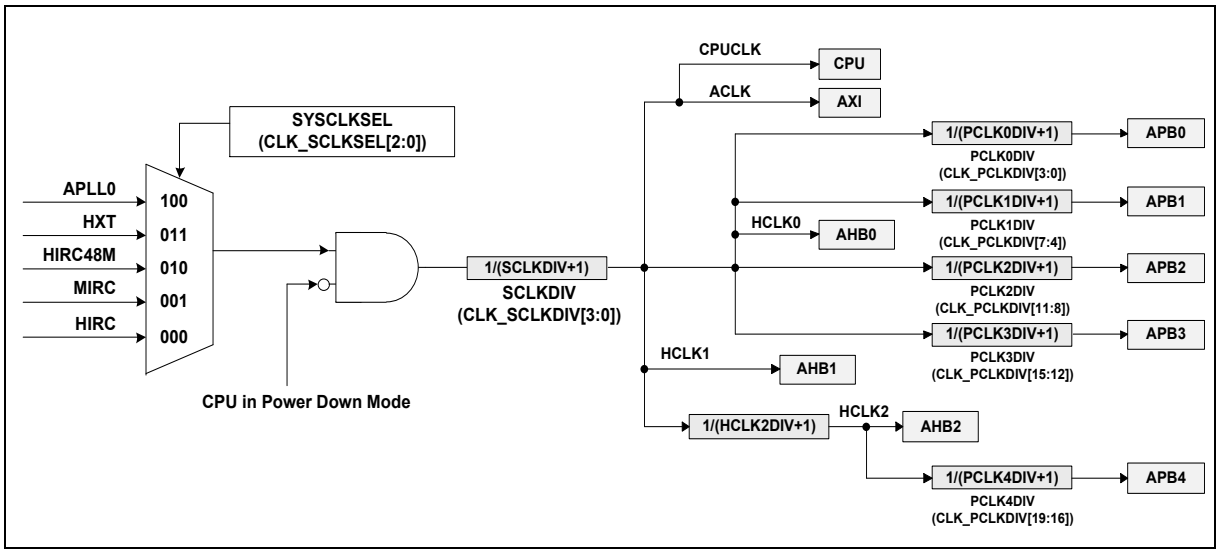


Figure 6.5-6 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from APLL with HXT as the input of APLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[5]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.5-7 shows that the HXT clock stops detection and system clock switches to HIRC procedure.

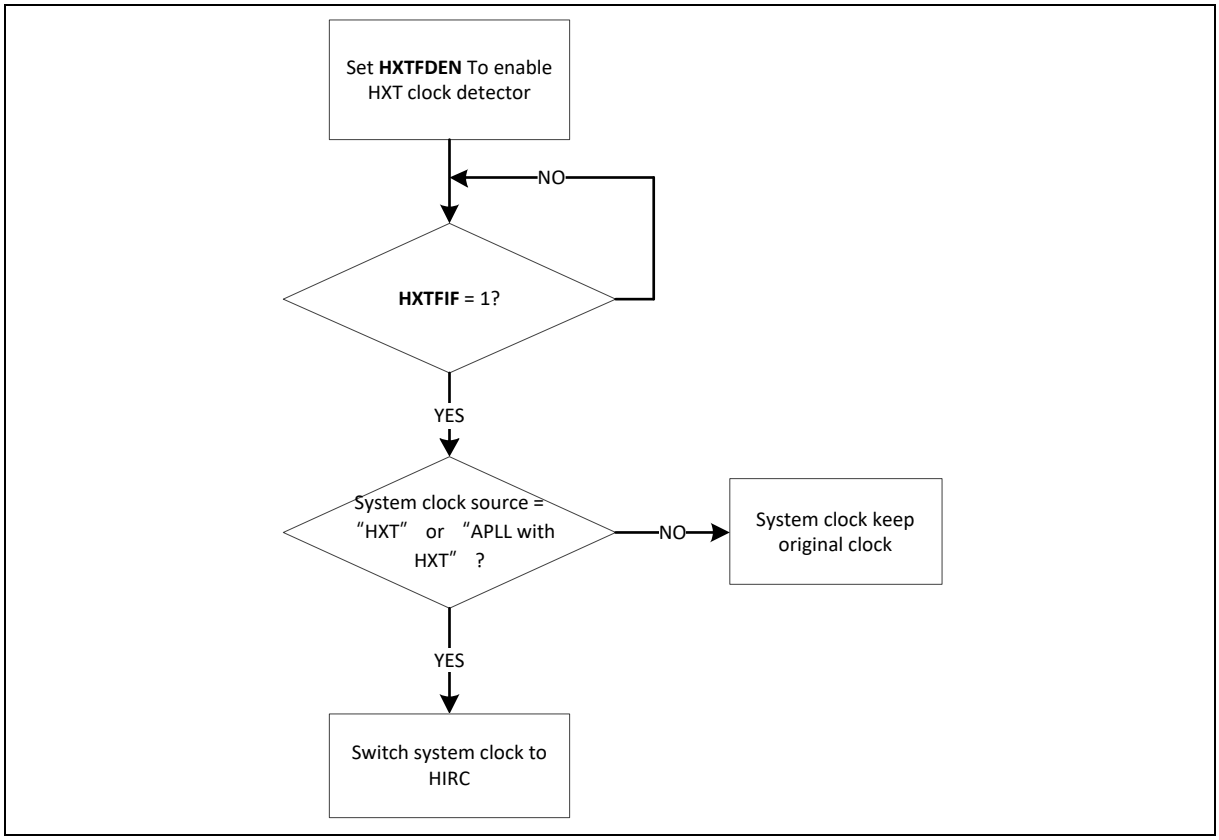


Figure 6.5-7 HXT Stop Protect Procedure

The clock source of SysTick in Cortex-M55 core can use CPU clock or external clock CLKSRC (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register ST0SEL (CLK_STSEL[2:0]). The block diagram is shown in Figure 6.5-8.

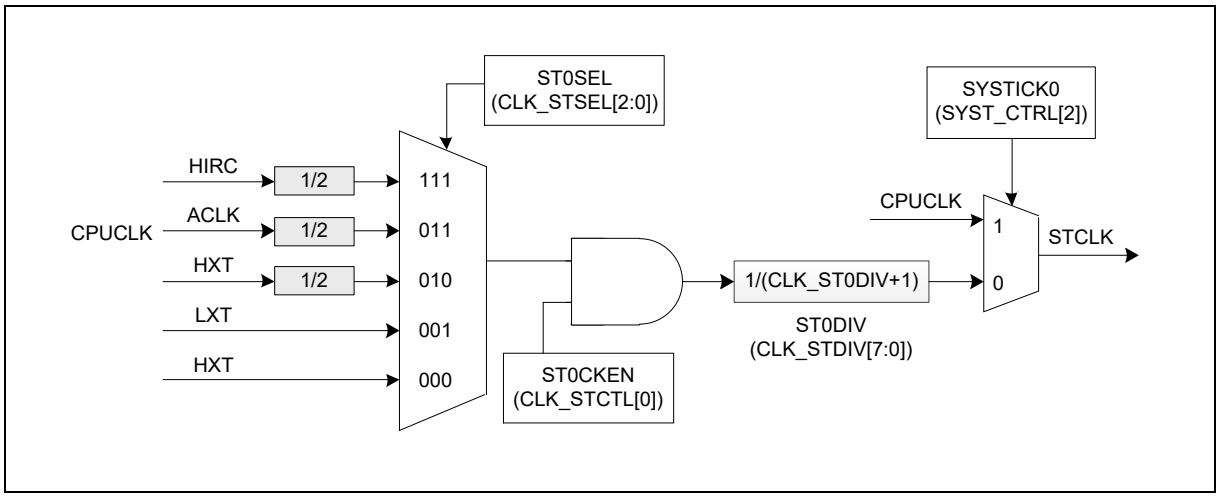


Figure 6.5-8 SysTick Clock Control Block Diagram

6.5.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_BPWMSEL, CLK_CANFDSEL, CLK_CCAPSEL, CLK_CLKOSEL, CLK_DLLSEL, CLK_DMICSEL, CLK_EADCSEL,

CLK_EPWMSEL, CLK_FMCSEL, CLK_I2SSEL, CLK_I3CSEL, CLK_KPISEL, CLK_LPADCSEL, CLK_LPSPISEL, CLK_LPTMRSEL, CLK_LPUARTSEL, CLK_PSIOSEL, CLK_QSPISEL, CLK_SCSEL, CLK_SDHSEL, CLK_SPISEL, CLK_STSEL, CLK_TMRSEL, CLK_TTMRSEL, CLK_UARTSEL0, CLK_UARTSEL1, CLK_USBSEL and CLK_WDTSEL register.

6.5.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 12 MHz internal high speed RC oscillator (HIRC)
  - 1~8 MHz internal medium speed RC oscillator (MIRC)
  - 32 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt HIRC, MIRC, LIRC or LXT as clock source)

6.5.6 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

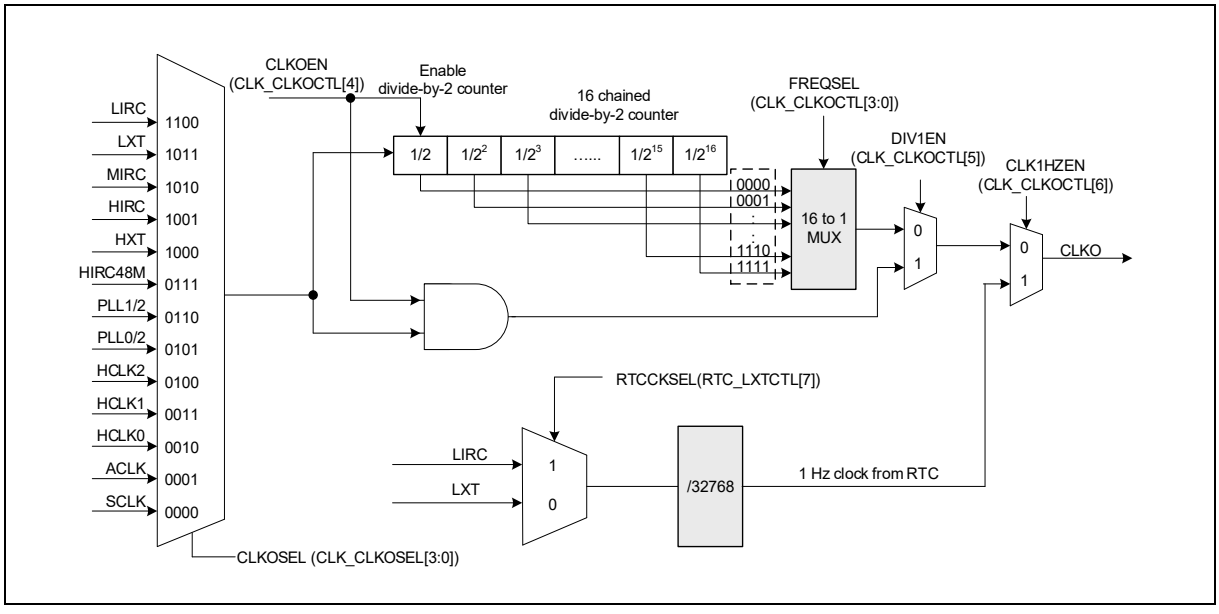


Figure 6.5-9 Clock Output Block Diagram

6.5.7 USB Clock Source

The clock sources of USB 1.1 and 2.0 systems are generated from USB2.0 PHY clock or programmable APLL output. The generated clocks are shown in Figure 6.5-10.

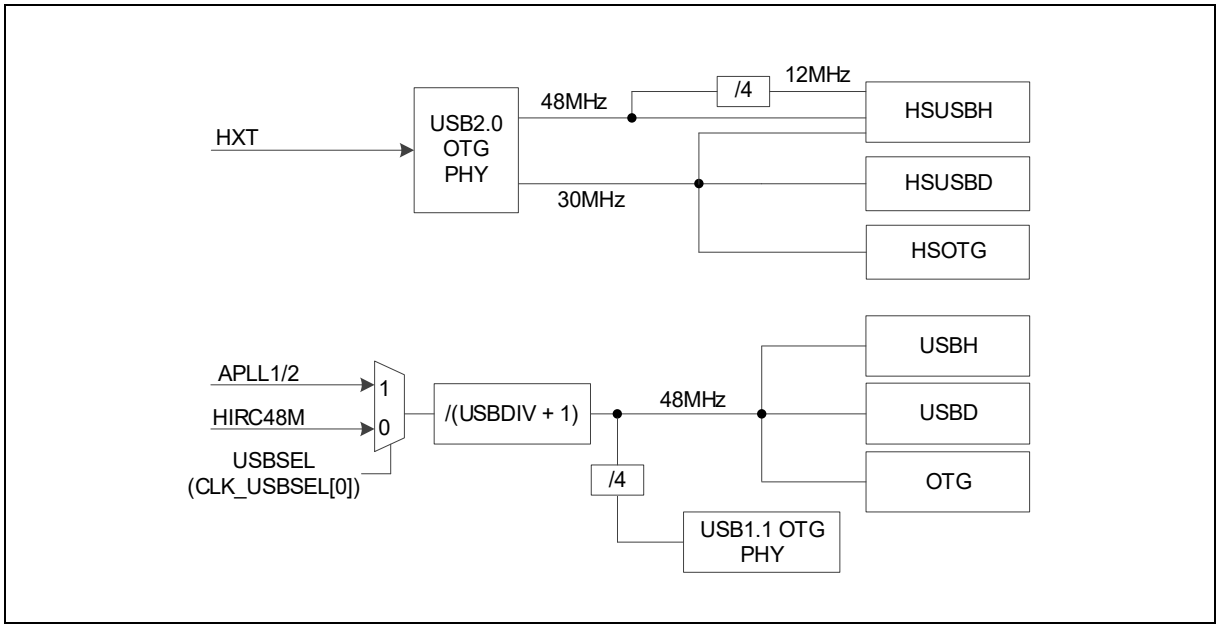


Figure 6.5-10 USB Clock Source

Note: For USB High-speed application and Full-speed Host application, HXT should be 24 MHz.

6.6 Security Configuration Unit (SCU)

6.6.1 Overview

Security configuration unit is designed for Arm® TrustZone®, and used to configure the security and privilege attribution of GPIO and all other peripherals. SCU also collects slaves' security violation response and generates SCU interrupt. SCU is also equipped with a timer to monitor the duration of the core processor in non-secure state.

SCU includes some security features like FVC, DPM and PLM, helping user to setup a secure executing environment more easily.

Note: For details on Arm® TrustZone®, refer to the section "Arm® TrustZone®"

6.6.2 Features

- Configures SRAM's security attribution block by block
- Configures GPIOs' security attribution port by port and EINT's security attribution separately
- Configures peripherals' security and privilege attribution
- Generates security interrupt
- Equipped with a 24-bit timer as a non-secure state monitor
- Monotonic firmware version counter
- Debug protection mechanism
- Product life-cycle management

6.7 True Random Number Generator (TRNG)

6.7.1 Overview

This is a True Random Number Generator (TRNG) consists of an entropy source from analog macro and a CTR_DRBG. There is a calibration mechanism of internal TRNG for randomness of generating true random number. Besides, there is a CTR_DRBG design in this TRNG for the DRBG (deterministic random bit generator) of SP800-90A and the NRBG (non-deterministic random bit generator) of SP800-90C.

6.7.2 Features

- Up to 10Mbit/s data rate for entropy source
- Pass NIST SP800-22A standard
- Include NIST SP800-90A known answer test for DRBG and NIST SP800-90B health test for entropy source (Start-up test, Repetition count test, Adaptive proportion test).
- Provides the true random number seed for PRNG

6.8 Flash Memory Controller (FMC)

6.8.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application. Both BANK0 and BANK1 have 512/1024 Kbytes space. Thus, the total size of application ROM (APROM) is 1024/2048 Kbytes. A User Configuration block provides for system initiation in BANK0. A 8 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function in BANK0. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data in BANK1. A 24 Kbytes Secure Bootloader is used to check boot code integrity and authenticity, and consists of native ISP functions. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.8.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports dual-bank remapping
- Supports 1024/2048 Kbytes application ROM (APROM)
- Supports 8 Kbytes loader ROM (LDROM)
- Supports 4 XOM (Execution Only Memory) regions to conceal user program in APROM.
- Supports 52 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 8 Kbytes page erase for all embedded Flash
- Supports bank erase for APROM, except if XOM regions is set.
- Supports two level locks for protecting secure region and non-sec region.
- Supports Secure Bootloader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for check boot code integrity and authenticity
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports Non-Secure In-System-Programming (NS ISP) to update embedded Non-Secure Flash memory

6.9 External Bus Interface (EBI)

6.9.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.9.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplex mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.10 General Purpose I/O (GPIO)

6.10.1 Overview

This chip has up to 143 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 143 pins are arranged in 10 ports named as PA, PB, PC, PD, PE, PF, PG, PH, PI and PJ. PA, PB, PE and PH has 16 pins on port. PD has 15 pins on port. PC, PG and PJ has 14 pins on port. PF has 12 pins on port. PI has 10 pins on port. Each of the 143 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode.

6.10.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports EINT0~7 edge detect and trigger function

6.11 Low Power General Purpose I/O (LPGPIO)

6.11.1 Overview

This chip has up to 8 Low Power General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 8 pins are named as LPIO0, LPIO1, LPIO2, LPIO3, LPIO4, LPIO5, LPIO6 and LPIO7. Each of the 8 pins is independent and has the corresponding register bits to control the pin function and data. These 8 pins also support output data set/reset registers to allow individual set/reset bitwise control.

6.11.2 Features

- Support function operating in NPD0/1/3
- Two I/O modes:
  - Push-Pull Output mode
  - Input only with high impendence mode
- Support pin output data individual bit set/reset
- Support auto operation

LPGPIO Feature	LPGPIO	GPIO
Support function operating in NPD0/1/3	√	-
Suppot I/O modes: Quasi-bidirectional mode	-	√
Suppot I/O modes: Push-Pull Output mode		
Suppot I/O modes: Open-Drain Output mode	-	√
Suppot I/O modes: Input only with high impendence mode	√	√
Support pin output data individual bit set/reset	√	-
Auto-operation Mode	√	-
I/O pin can be configured as interrupt source with edge/level setting	-	√
Support High Drive and High Slew Rate I/O mode	-	√
Support independent pull-up and pull-down control	-	√
Enabling the pin interrupt function will also enable the wake-up function	-	√

Table 6.11-1 LPGPIO Supported Features

6.12 Graphic Direct Memory Access Controller (GDMA)

6.12.1 Overview

The GDMA is a Direct Memory Access Controller (DMAC) with AMBA® AXI5 interfaces and it is equipped with Arm DMA-350 specification that provides fast memory to memory. The processor in the system can control the DMA channel behavior over an APB4 interface.

The GDMA has configurations for different types of copy, scatter-gather, increment, or two-dimensional image copy operations. It also supports command sequencing capabilities.

The GDMA can have several channels which can have different properties, like FIFO size (16 depth FIFO) , to suit different requirements. Several GDMA commands can be combined with the command linking feature. Using the command linking feature, a complex transfer can be set up and the GDMA can perform without the need for interaction with the processor.

6.12.2 Features

- Programmable APB4 configuration registers
- 2 parallel DMA channels each with 16 depth FIFO
- 1D memory copy including increments
- Interrupt capability for each channel and global events
- Flexible command linking capability
- Extended memory copy capabilities: 2D/wrap/template (support in Channel 0)
- AXI5 address width 32-bit
- AXI5 data width of 64-bit
- Number of DMA channels 2
- Presence of Security Extension for TrustZone support

6.13 PDMA Controller (PDMA)

6.13.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.13.2 Features

- Supports 16 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, USCI, SPI, QSPI, ACMP,PWM, EINT, EPWM, I^2C, I^2S, I^3C, , Timer, , PSIO, EADC, and DAC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports 16 time-out function channels

6.14 Low Power Peripheral Direct Memory Access Controller (LPPDMA)

6.14.1 Overview

The low power peripheral direct memory access (LPPDMA) controller is used to provide high-speed data transfer. The LPPDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. LPPDMA controller has a total of 4 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.14.2 Features

- Supports 4 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and LPUART, LPSPI, LPI2C, LPTMR, TTMR, DMIC and LPADC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type

6.15 Timer Controller (TMR)

6.15.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.15.2 Features

6.15.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- Supports 3-bit capture input noise filter
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, EADC, DAC, EQEI and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports internal capture triggered source from ACMP0~3 output, HXT, HIRC, LIRC, and LXT.
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP0~3_out or internal USB SOF signal
- Supports over-capture flag

6.15.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type

  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports PWM output accumulator event to trigger PDMA transfer and EADC
- Supports PWM output accumulator event to stop PWM counting
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events
- Supports External Pin event to trigger PWM counter action

6.16 Low Power Timer Controller (LPTMR)

6.16.1 Overview

The low power timer controller includes two 32-bit timers, LPTMR0 ~ LPTMR1, allowing user to easily implement a timer control for applications. The low power can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The low power timer controller also provides two PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (LPTMRx or LPTMRx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

6.16.2 Features

6.16.2.1 Low Power Timer Function Features

- Two sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (LPTMRx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (LPTMRx_CAP[23:0])
- Supports external capture pin (LPTMRx_EXT) event for interval measurement
- Supports external capture pin (LPTMRx_EXT) event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt signal or capture interrupt signal to trigger LPADC0,~~,~~ LPI2C0, LPSPI0, LPUART, , CCAP Motion detector, and LPPDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports event counting source from ACMP0_out, ACMP1_out, ACMP2_out or ACMP_3
- Supports internal capture triggered source from ACMP0 output, ACMP1 output, ACMP2 output and ACMP_3 output
- Support over-capture flag

6.16.2.2 PWM Function Features

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels
- Supports interrupt on the following events:

- PWM period point, up-count compared point events

- Supports wake-up when interrupt occurs when clock source is LXT or LIRC
- PWM can generate output in Power-down mode
  - Supports trigger LPADC, LPPDMA, and on the following events:
  - PWM period point and up-count compared point events
- Supports PWM output accumulator event to trigger LPPDMA transfer and LPADC
- Supports PWM output accumulator event to stop PWM counting
- Supports automatic operation mode

6.17 Tick Timer Controller (TTMR)

6.17.1 Overview

The tick timer controller includes two 32-bit timers, TTMR0 ~ TTMR1, allowing user to easily implement a timer control for applications. The tick timer can perform functions, such as frequency measurement, delay timing, clock generation.

6.17.2 Features

6.17.2.1 Tick Timer Function Features

- Two sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TTMRx_CNT[23:0])
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt signal to trigger LPADC, LPI2C, LPSPI, LPUART,-, CCAP Motion detector and LPPDMA function

6.18 Watchdog Timer (WDT)

6.18.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.18.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK = 32 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC 32 kHz or LXT

6.19 Window Watchdog Timer (WWDT)

6.19.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.19.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.20 Real Time Clock (RTC)

6.20.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.20.2 Features

- Supports external power pin V_{BAT}.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up to 6 individual tamper pins or 3 pairs dynamic loop tamper pins.
- Supports 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports Flash mass erase operate will also clear the 80 bytes spare registers content.

6.21 Basic PWM Generator and Capture Timer (BPWM)

6.21.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0/1 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.21.2 Features

6.21.2.1 BPWM Function Features

- Supports maximum clock frequency up to HCLK frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0/1 in the following events:
  - BPWM counter matches 0, period value or compared value

6.21.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.22 EPWM Generator and Capture Timer (EPWM)

6.22.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/LPADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC/LPADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.22.2 Features

6.22.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion independent control with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator, UTCPD, EADC0 result monitor and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/LPADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC/LPADC)
  - Supports EPWM trigger EADC/LPADC event prescaler feature
- Support PDMA transfer for Interrupt Flag Accumulator Function
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect function
- Support External Pin Trigger Function

6.22.2.2 Capture Function Features

- Support 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.23 Enhanced Quadrature Encoder Interface (EQEI)

6.23.1 Overview

There are four EQEI controllers in this device. The Enhanced Quadrature Encoder Interface (EQEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.23.2 Features

6.23.2.1 Enhanced Quadrature Encoder Interface (EQEI) Features

- Up to four EQEI controllers, EQEI0, EQEI1, EQEI2 and EQEI3.
- Two EQEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (EQEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (EQEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (EQEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (EQEI_CNTCMP) with a Pre-set Maximum Count Register (EQEI_CNTMAX)
- A 32-bit up count Unit Timer Pulse Counter (EQEI_UTCNT)
- A 32-bit Unit Timer Pulse Counter Compare Register (EQEI_UTCMP)
- One EQEI control register (EQEI_CTL) and one EQEI Status Register (EQEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Supports X4 free-counting mode
  - Supports X2 free-counting mode
  - Supports X4 compare-counting mode
  - Supports X2 compare-counting mode
- Two Quadrature encoder phase counter operation modes:
  - Supports X1 1-phase 2 input compare-counting mode
  - Supports X2 1-phase 2 input compare-counting mode
- Two Quadrature encoder directional counter operation modes:
  - Supports X1 1-phase 1 input compare-counting mode
  - Supports X2 1-phase 1 input compare-counting mode
- Supports swap function for input signals QEA and QEB
- Supports for detecting the occurrence of phase error from input signals QEA and QEB
- Supports one times index signal reset function for Quadrature encoder pulse counter
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clock/8

6.24 Enhanced Input Capture Timer (ECAP)

6.24.1 Overview

The chip provides up to four units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.24.2 Features

- Up to four Input Capture Timer/Counter units, CAP0, CAP1, CAP2 and CAP3.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.25 Camera Capture Interface Controller (CCAP)

6.25.1 Overview

The camera capture interface controller (CCAP) is designed to capture image data from a sensor. After capturing or fetching image data, it processes the image data. Then, the embedded DMA controller will move the data from the internal FIFO to system memory with AHB bus, except for the motion detection function.

6.25.2 Features

- CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor.
- 8-bit YUV422, 8-bit RGB565 and 8-bit RGB888 color format supported for data-in from CMOS sensor.
- 8-bit/4-bit monochrome format supported for data-in from CMOS sensor.
- YUV422, RGB565, RGB555, RGB888, ARGB8888 and Y-only color supported for packet data output.
- Single interrupt source to interrupt controller from maskable interrupt source: Address Match, Bus Master Transfer Error, Video Frame End and Motion Detection.
- Embedded DMA controller supported to transfer data from internal FIFO to system memory through AHB bus.
- Supports YUV422 and YUV420 planar data output
- CROP function supported to crop input image to the required size for digital application in color CMOS sensor or motion detection function.
- Frame rate scaling-down supported in color CMOS sensor or motion detection function.
- Image scaling-down supported in color CMOS sensor or motion detection function.
- Bit luma output with 8-bit threshold setting supported .
- Supports motion detection engine with 320x240 image data in power-down mode.
- Supports motion detection engine trigger sources from LPTMR0/1 and TTMR0/1.
- Supports chip wake-up from power-down mode if a motion detection interrupt signal is generated.

6.26 UART Interface Controller (UART)

6.26.1 Overview

The chip provides ten channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.26.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0/ UART1	UART2 ~ UART9	USCI-UART
FIFO	16 Bytes	16 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	√	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-
Received Data FIFO reached threshold Time-out Wake-up	√	√	-
Baud Rate Compensation	√	√	-
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.26-1 M55M1 Series UART Features

6.27 Low Power UART Interface Controller (LPUART)

6.27.1 Overview

The chip provides one channel of Low Power Universal Asynchronous Receiver/Transmitters (LPUART). The LPUART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each LPUART controller channel supports nine types of interrupts. The LPUART controller supports flow control function. The LPUART controller also supports RS-485 function mode and auto-baud rate measuring function.

6.27.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (LPUART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for LPUART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports LPPDMA transfer function
- Supports Automatic Operation

LPUART Feature	LPUART0	UART0/ UART1	UART2 ~ UART9	USCI-UART
FIFO	16 Bytes	16 Bytes	16 Bytes	TX: 1byte RX: 2byte
Automatic Operation	√	-	-	-
Auto Flow Control (CTS/RTS)	√	√	√	√
LIN	-	√	-	-

RS-485 Function Mode	√	√	√	√
nCTS Wake-up	√	√	√	√
Incoming Data Wake-up	√	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	√	-
Received Data FIFO reached threshold Time-out Wake-up	√	√	√	-
Baud Rate Compensation	√	√	√	-
Auto-Baud Rate Measurement	√	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√	√
Stick Bit	√	√	√	-

Table 6.27-1 M55M1 Series LPUART Features

6.28 Ethernet MAC Controller (EMAC)

6.28.1 Overview

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The EMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

In addition to the default interfaces defined in the IEEE 802.3 specifications, the EMAC supports several industry standard interfaces to the PHY. The EMAC is compliant with the following standards:

- IEEE 802.3-2008 for Ethernet MAC
- IEEE 1588-2008 standard for precision networked clock synchronization
- AMBA 2.0 for AHB master/slave port
- RMII specification version 1.2 from RMII consortium

6.28.2 Features

- 10 and 100 Mbps data transfer rates with the following PHY interfaces:
  - RMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - Forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size
- Programmable Interframe Gap (IFG) (40-96 bit times in steps of 8)
- Option to transmit frames with reduced preamble size
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces to the application
- Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
- Support Ethernet frame timestamping as described in IEEE 1588-2002 and IEEE 1588-2008.
  - The 64-bit timestamps are given in the transmit or receive status of each frame

- MDIO master interface for PHY device configuration and management
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path

6.29 Smart Card Host Interface (SC)

6.29.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It can also be set as UART mode to communicate with other device.

6.29.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 bytes' entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes' entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.30 I²S Controller (I²S)

6.30.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.30.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.31 Serial Peripheral Interface (SPI)

6.31.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I²S mode to connect external audio CODEC.

6.31.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 100 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I²S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I²S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.32 Low Power Serial Peripheral Interface (LPSPI)

6.32.1 Overview

The Low Power Serial Peripheral Interface (LPSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of LPSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The LPSPI controller can be configured as a master device and supports the LPPDMA function to access the data buffer, or configured as a slave device and monitor the signal level change of SS to wake up system.

6.32.2 Features

- LPSPI Mode
  - One set of LPSPI controller
  - Supports Master or Slave mode operation
  - Master mode up to 50 MHz (when chip works at V_{DD} = 2.7V~3.6V)
  - Slave mode up to 25 MHz when LPSPI master device supports adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7~3.6V)
  - Slave mode up to 25 MHz when LPSPI master device does not support adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7V~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports LPPDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
  - Supports automatic operation mode

6.33 Quad Serial Peripheral Interface (QSPI)

6.33.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains two QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.33.2 Features

- Supports Master or Slave mode operation
- Master mode up to 100 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.34 SPI/HyperBus Synchronous Serial Interface Controller (SPIM)

6.34.1 Overview

The SPI/HyperBus Synchronous Serial Interface Controller for storage components of SPI Flash and HyperBus deive performs a serial-to-parallel conversion on data received from the storage peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI/HyperBus controller can drive one SPI Flash and it is seen as the SPI master mode, and it also can drive one HyperBus device and it is seen as the HyperBus host. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of chip/slave select (CS/SS) signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral.

In controller of SPI Flash and HyperBus device, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8-bits, 16-bits, 24-bits, or 32-bits; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to storage components of SPI Flash and HyperBus device. In DMA read mode, user can move data from storage components of SPI Flash and HyperBus device to SRAM. In Direct Memory Mapping mode (DMM mode), this controller of SPI Flash and HyperBus device will translate the AHB bus commands into operations of SPI Flash and HyperBus device without MCU setting related commands of SPI Flash and HyperBus device. Therefore, users can access storage devices of SPI Flash and HyperBus device as a ROM module or RAM module.

The Synchronous serial Interface Controller supports for STR (Single Transfer Rate) and DTR (Double Transfer Rate) read/write command codes with Standard/Dual/Quad/Octal I/O transfer modes. Once a DTR instruction code is accepted by the device, the transmission data or received data will be output or sampled on both rising and falling edges of the serial clock.

For data protection, the synchronous serial Interface controller supports encryption and decryption of AES cipher circuits outside IP to protect data which user places into storage components of SPI Flash and HyperBus device when DMA read/write mode and direct memory mapping mode are used.

6.34.2 Features

- Supports SPI Flash with maximum 32 Mbytes size
- Supports HyperBus device with maximum 32 Mbytes size
- Supports SPI master mode and HyperBus host mode
- Supports Direct Memory Mapping Mode, Normal I/O Mode, DMA Read Mode, and DMA Write mode
- Supports transaction with data width 8/16/24/32 bits for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports standard (1-bit), dual (2-bit), quad (4-bit), and octal (8-bit) I/O transfer mode
- Supports Single Transfer Rate (STR) mode and Double Transfer Rate (DTR) mode
- Supports AES OTFC (On-The-Fly Cipher) encryption/decryption
- One slave/device select line for storage component of SPI Flash and HyperBus device
- Supports read DQS data strobe from SPI Flash and HyperBus device to sample RX data from SPI Flash and HyperBus device
- Supports Linear Burst Read with Row Boundary Crossing for HyperBus device
- Not supports type of HyperBus device that it is not allowed Linear Burst Write to across Row Boundary

6.35 I²C Serial Interface Controller (I²C)

6.35.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are four sets of I²C controllers which support Power-down Wake-up function.

6.35.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to four I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable
- Add pin swap function
- Supports Bus Management (SM/PM compatible) function Compatible with the SMBUS specification rev 2.0 (http://smbus.org/specs/) and PMBUS specification rev 1.2 (http://pmbus.org/)

6.36 Low Power I²C Serial Interface Controller (LPI2C)

6.36.1 Overview

LPI2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices.

There is one set of LPI2C controller which supports Power-down Wake-up function.

6.36.2 Features

The LPI2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the LPI2C bus include:

- Supports one LPI2C port
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) when clock source is greater than 20 MHz
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the LPI2C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports LPPDMA with one buffer capability
- Supports setup/hold time programmable
- Adds pin swap function
- Supports auto-operation mode
- Supports trigger source from LPTMR0/1, TTMR0/1 and WKIOA/B/C/D rising/falling edge event

6.37 I3C Serial Interface Controller (I3C)

6.37.1 Overview

I3C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The Improved Inter Integrated Circuit (I3C) is part of a group of communication protocols defined by the MIPI Alliance. This specification is developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

The I3C controller is dual role device and meets the requirement of I3C protocol and I^2C protocol as specified by the MIPI I3C Specification. The specific reference documents is:

- MIPI Alliance Specification for I3C BasicSM Version 1.0

6.37.2 Features

- Supports one I3C port
- Supports Master and Slave mode
- Static or Dynamic Slave Device support
- Built-in Hardware Dynamic Address Allocation support (ENTDAA/SETDASA)
- Built-in CCC transfer handler
- Auto Hot-Join request generation support
- In-Band Interrupt request generation support
- Adaptive mode of operation between I^2C and I3C depending on I3C bus traffic
- Built-in S0-S5 Error Handling
- Supports Power-down wake-up function
- Supports PDMA mode for data transfer
- Supports SDR mode, data rates up to 12.5 Mbps
- Supports HDR-DDR mode, data rates up to 25 Mbps
- Supports Secondary Master mode

6.38 USCI - Universal Serial Control Interface Controller (USCI)

6.38.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I²C functional protocol.

6.38.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I²C

6.39 USCI – UART Mode

6.39.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are three conditions to wake up the system.

6.39.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

6.40 USCI - SPI Mode

6.40.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

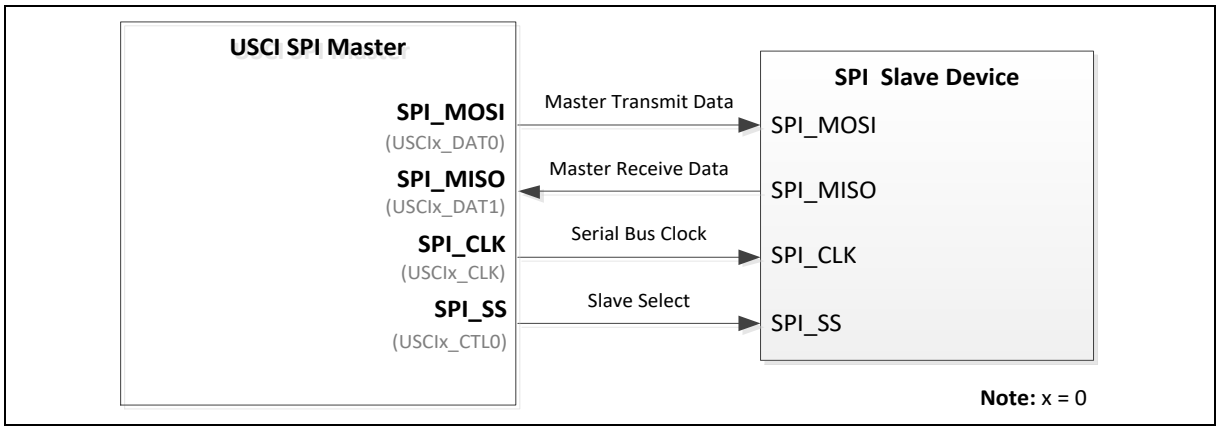


Figure 6.40-1 SPI Master Mode Application Block Diagram

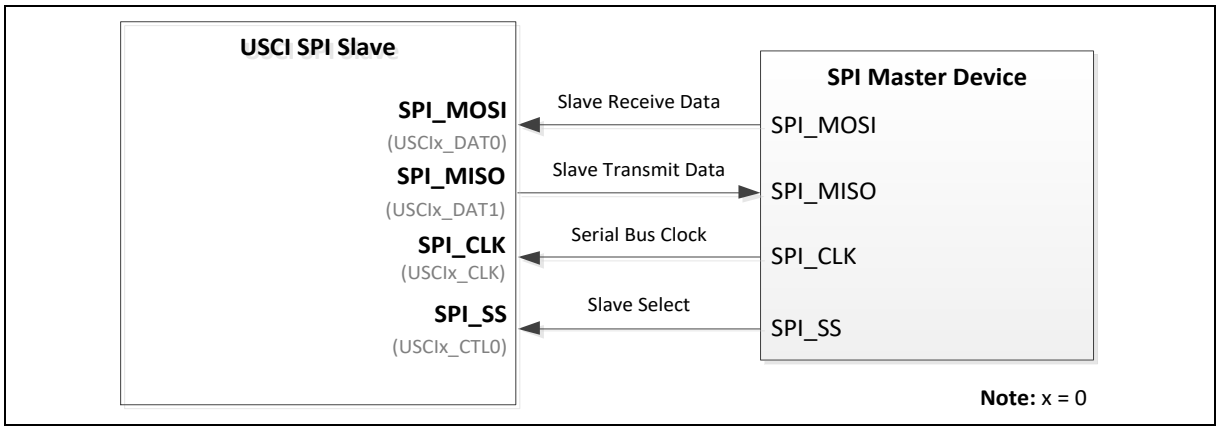


Figure 6.40-2 SPI Slave Mode Application Block Diagram

6.40.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer

- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.41 USCI - I²C Mode

6.41.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.41-1 for more detailed I²C BUS Timing.

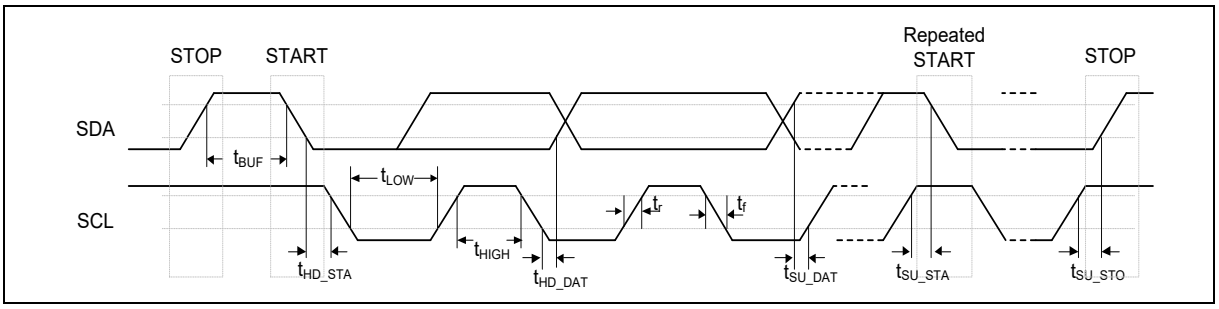


Figure 6.41-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.41.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.42 Secure Digital Host Controller (SDH)

6.42.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.42.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.43 Programmable Serial I/O (PSIO)

6.43.1 Overview

Programmable Serial I/O (PSIO) provides a simple way to implement simple serial signal processing, e.g. UART and IR. The PSIO can control when the pin will output high or low and how long the pin need to output high or low. It also provides the easy way to sample the pin state.

6.43.2 Features

- Supports up to 8 PSIO pins, from PSIO pin0 to PSIO pin7
- Supports 7 clock sources, they are LXT, HXT, LIRC, HIRC, HIRC48M/4, PCLK1, APLL0/2
- Supports one clock divider, which can be divided from 1 to 255
- Supports slot controller for timing sequence control
  - Supports 4 slot controllers, 8 slots in each slot controller
  - Supports counting from 1 PSIO clock to 15 PSIO clocks in each slot
  - Supports 3 slot repeat modes:
    - Normal repeat mode
    - Normal repeat mode with infinity loops
    - Whole repeat mode
  - Supports 4 slot trigger conditions:
    - Triggered by software
    - Triggered by falling edge
    - Triggered by rising edge
    - Triggered by rising edge or falling edge
- Supports PSIO PIN for pin state control
  - Supports 8 check points to connect with slots in each pin
  - Supports 8 check point actions in each check point.
  - Supports 7 kinds of check point action to setting
    - Output high
    - Output low
    - Output data
    - Output toggle
    - Input data
    - Input status
    - Input status update
  - Supports 4 I/O modes, input, output, open-drain, and quasi
  - Supports switch I/O mode in different check points
- Supports 4 kinds of Interrupt trigger conditions
  - Two sets of configurable slot interrupt controllers

- Mismatch interrupt when PSIO is enabled with PDMA
- Transfer Error interrupt
- Slot controller counting done interrupt

- Supports PDMA function

6.44 USB 1.1 Device Controller (USBD)

6.44.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1.5K byte sizes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEG0~24).

There are 25 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, and BUS events, such as suspend and resume and SOF event, receive Start of Frame(SOF) packet in every 1ms event. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0~3) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.44.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBDET, USB, BUS and SOF)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 25 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1.5 Kbyte buffer size
- Provides remote wake-up capability
- Supports double buffer function
- Supports VBUS plug in / out or resume wake up from Power-down mode
- Supports USB 2.0 Link Power Management (LPM)

6.45 USB 1.1 Host Controller (USBH)

6.45.1 Overview

This chip is equipped with two USB 1.1 FS Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB). USBH0 and USBH1 are the companion host controller of HSUSBH0 and HSUSBH1 respectively.

Each USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.45.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.46 USB 1.1 On-The-Go (OTG)

6.46.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of an USB 1.1 host controller and an USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

An USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, the USB frame acts as USB host. The USB frame can support both full-speed and low-speed transfer. In Device-only mode, the USB frame acts as USB device. USB device support full-speed transfer. In ID dependent mode, the USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. The USB frame only supports full-speed transfer when OTG device acts as a peripheral

6.46.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The role of USB frame is only dependent on USB_ID pin state -- as USB Host (USB_ID pin is at low) or USB Device (USB_ID pin is at high). Both HNP and SRP protocols are not supported.
  - OTG device: depends on USB_ID pin state to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). HNP and SRP protocols are supported.

6.47 High Speed USB 2.0 Device Controller (HSUSBD)

6.47.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is compliant with USB 2.0 specification and it contains 18 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.47.2 Features

- USB Specification revision 2.0 compliant
- Supports 18 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- Supports Endpoint Maximum Packet Size up to 1024 bytes
- Supports VBUS / Resume wakeup from system power-down mode
- Supports Link Power Management (LPM) feature
- Supports Battery Charging 1.2 (BC1.2) feature

6.48 USB 2.0 and 1.1 Host Controller (HSUSBH and USBH1)

6.48.1 Overview

This chip is equipped with an individual USB 2.0 Host Controller (HSUSBH) that support Enhanced Host Controller Interface (EHCI) Specification, and an USB 1.1 Host Controller (USBH1) that support Open Host Controller Interface (OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The whole HSUSBH/USBH1 supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The whole HSUSBH/USBH1 is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.48.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.
- Supports OTG function.

6.49 High Speed USB 2.0 On-The-Go (HSOTG)

6.49.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in HSUSBROLE (SYS_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID dependent mode, USB frame can be USB Host or USB device depends on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

6.49.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The USB frame can act as USB Host (USB_ID pin is at low) or USB Device (USB_ID pin is at high) only depending on USB_ID pin state. HNP or SRP protocol is not supported.
  - OTG device: It can be A-device (USB_ID pin state is at low) or B-device (USB_ID pin state is at high) depending on USB_ID pin state. HNP and SRP protocols are supported.

6.50 USB Type C Power Delivery Controller (UTCPD)

6.50.1 Overview

The UTCPD is a USB Type-C Power Delivery controller. UTCPD integrates a Power Delivery PHY with BMC encoding and decoding, protocol layer function and USB Type-C Configuration Channel (CC) logic to fulfill USB Type-C CC sensing and control and USB PD message delivery function.

UTCPD is compliant with USB Type-C 1.2 and USB Power Delivery3.0.

6.50.2 Features

6.50.2.1 Basic Functionality

- Compliant with USB Type-C Cable and Connector Specification Rev1.2 (TYPE-C)
- Supports UFP, DFP and DRD data roles
- Supports Sink, Source and DRP power roles
- Dual-Role Power functionality with Autonomous DRP toggle
- Supports CC1 and CC2 signals
  - Internal Rp and Rd
  - Default, 1.5A and 3A current sourcing advertising
  - Support dead battery
  - Detects cable orientation
  - Transmits and receives BMC encoded, PD messages
  - Transmits and receives Fast Role Swap (FRS) requests
  - Detects VBUS presence
- Monitors VBUS voltage,using system EADC
- Debounces attachment detection on either VBUS or CCx signals
- Detects connection removal via either VBUS or CCx signals
  - Power Delivery Functionality
- Compliant with USB Power Delivery Specification Rev3.0, V1.2 (PD)
- Transmits and receives serial data via CC*x* signals:
  - Limits the slew rate of the transmitted signal
  - Filters the received signal
- Supports Power Delivery PHY Layer
  - Performs BMC and 4b5b encoding/decoding of the transmitted and received data bits stream
  - Generates and decodes Preamble, SOP and EOP
  - Appends and checks CRC
  - Generates and receives Hard Reset
  - Generates and receives Cable Reset
  - Supports Carrier Mode 2 and Test data, BIST modes
  - Supports Power Delivery Protocol Layer

- Supports SOP', SOP" and SOP messages
- Implements and checks the MessageID counter
- Supports Control messages
  - Automatically generates GoodCRC response
  - Generates Hard Reset
- Supports Data messages with up to 30 data bytes
  - Supports Vendor Defined Messages (VDM)
  - Supports long messages via Chunking
- Has separate transmit and receive buffers
- Supports up to three automatic retries
- Supports Data role, power role and V_{CONN} swapping
- Implements the timing critical functions of the PD protocol, such as waiting for a GoodCRC response

6.50.2.2 System Control and Monitoring

- Provides controls for VBUS both "force" and "bleed" bulk capacitors discharge
  - Discharge signal is controlled by monitoring the actual VBUS voltage level

6.50.2.3 Wake-up from Idle mode and NPD0~2

6.51 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.51.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 24 external input channels and 4 internal channels. The EADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger, external pin (EADC0_ST) input signal, and ACMP0~3 triggers.

6.51.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 24 single-end analog external input channels or 12 pair fully differential analog input channels
- Up to 4 internal channels, they are $AV_{DD}/4$, band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and battery power/4 ($V_{BAT}/4$).
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 100 MHz for EADC
- Up to 5 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage V_{REF}: 1.6V, 2V, 2.5V and 3V.
- Up to 28 sample modules
  - Sample module 0~23 is configurable for EADC converter channel (EADC_CH0~23) and trigger source for each EADC.
  - Sample module 24~27 are fixed for input sources band-gap voltage, temperature sensor, battery power/4 ($V_{BAT}/4$), and $AV_{DD}/4$ respectively.
  - Double buffer for sample control logic module 0~3.
  - Configurable sampling time for each sample module.
  - Conversion results are held in 28 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~27)
  - External pin EADC0_ST trigger
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay counter

- ACMP0, ACMP1, ACMP2, and ACMP3 interrupt pulse triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.52 Controller Area Network with Flexible Data Rate (CAN FD)

6.52.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and need be connected to additional transceiver hardware for the physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock (HCLK) . In order to achieve a stable function of the CAN FD controller, the AHB clock must always be faster than or equal to the CAN core clock.

6.52.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.53 CRC Controller (CRC)

6.53.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-8, CRC-16, CRC-32, and 32-bits programmable polynomials settings.

6.53.2 Features

- Supports four common polynomials CRC-8, CRC-16, and CRC-32
- Programmable seed value
- Programmable polynomials settings
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports Master mode

6.54 Cryptographic Accelerator (CRYPTO)

6.54.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA/HMAC, RSA, and ECC algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation. (283~571 bits are only generated for Key Store).

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, CBC-CS3, CCM and GCM mode.

The SHA accelerator is an implementation fully compliant with the SM3, SHA-160, SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/t, SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256. The SHA accelerator supports HMAC (Keyed-Hash Message Authentication Code) algorithms include HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, HMAC-SHA-512, HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with RSA cryptography, CRT decryption algorithm and side-channel attack countermeasures.

The Crypto can get key from Key Store and/or put the key to Key Store determined by the function of each accelerator.

6.54.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits are only generated for Key Store).
  - Can take the true random number seed from TRNG
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports CCM mode, GCM mode and GMAC function
  - Supports SM4 block cipher algorithm
  - Supports key expander for key expansion in FIPS NIST 197
  - Supports one technique to improve side-channel attack protection ability
- SHA
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and SHA-512/t
  - Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256

- Supports SM3 Cryptographic Hash Algorithm

- HMAC
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512
  - Supports HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512
- ECC
  - Supports both prime field GF(p) and binary filed GF(2^m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports Curve25519
  - Supports Edwards curve
  - Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)
  - Supports modulo operation with 1088-bits dividend and 544-bits divisor in GF(p)
  - Supports modulus exponential operation and square root operation in GF(p)
  - Supports three techniques to improve side-channel attack protection ability
- RSA
  - Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits
  - Supports CRT decryption with 2048, 3072 and 4096 bits
  - Supports three techniques to improve side-channel attack protection ability

6.55 Key Store (KS)

6.55.1 Overview

The Key Store (KS) is the key management device and has a 4 Kbytes SRAM, 8 Kbytes Flash and OTP for key storage. The Key Store is capable of providing a crypto engine to access or storing the key while encryption, decryption and generation. The Key Store supports revoke key operation if the key is unused. The Key Store is able to protect the key by integrity checking, silent access, data scrambling and data remanence prevention for SRAM.

6.55.2 Features

- Supports programming interface for key management
- Supports key size required for Cryptographic engine from 128-bit to 4096-bit
- Supports up to 32 SRAM keys by 4 Kbytes SRAM
- Supports up to 32 Flash keys by 8 Kbytes Flash
- Supports 16 OTP keys, maximum key size is 256-bit
- Supports crypto engine access or store key in key store directly
- Supports to store AES/HMAC/ECC/RSA/CPU key
- Supports to store key from KDF
- Supports to store RSA middle data for CRT and SCAP mode
- Supports ECDH operation with ECC and PRNG engine
- Supports revoke operation
- Supports integrity checking
- Supports data scrambling
- Supports silent access for side-channel protection
- Supports data remanence prevention at SRAM
- Supports auto verify function
- Supports lock function for OTP keys

6.56 Keypad Interface (KPI)

6.56.1 Overview

The Keypad Interface (**KPI**) is an APB slave with configurable minimum 2-row up to 6-row scan output and minimum 1-column up to 8-column scan input. Any keys in the array pressed or released are de-bounced and generate an interrupt.

The KPI supports release multiple keys and press multiple keys scan interrupt. The interrupt is generated whenever it detects any key in the keypad pressing or releasing. User can know the interrupt source by querying KPI_STATUS register.

6.56.2 Features

- Matrix keypad interface (maximum 6x8 array, and minimum 2x1 array)
- Programmable de-bounce time
- Generates interrupt and updates all the keys (maximum 48 keys, minimum 2 keys) information (press/release) every time the user pressing or releasing

6.57 Awake Filter (AWF)

6.57.1 Overview

The Awake Filter can filter the received data that meets preset threshold conditions, and will issue an interrupt if conditions meet and interrupt enabled.

6.57.2 Features

- Present as memory in system
- Supports configurable threshold conditions(high threshold and low threshold)
- Supports 8-word buffer

6.58 Digital Microphone Inputs (DMIC)

6.58.1 Overview

The DMIC subsystem includes four-channel digital PDM (Pulse Density Modulation) microphone interface and Voice Active Detection (VAD). DMICn_DAT inputs are able to handle two digital microphones by selecting them alternately for each half of the clock cycle.

There are voice detections in DMIC subsystem which is Voice Active Detection(VAD).

The Voice Active Detection (VAD) analyzes the PCM data from DMIC channel 0, and consists of a SINC filter, a biquad filter and a VAD module. The idea of the VAD is to calculate the short term signal power and long term signal power of the input signal, and then compare the short term power with the short term power threshold. Moreover, the deviation of the short term power and long term power can be calculated and compared with the threshold deviation. Based on these two results, if the input signal is voice or not can be determined.

6.58.2 Features

- DMIC (four-channel digital microphone interface)
- Provides one 32-level FIFO data buffers for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports LPPDMA transfer
- Supports up to four channel digital microphones
- Four digital PDM microphone inputs that can be used simultaneously
- Supports High Pass Filter (HPF) to removed DC offset from digital microphone
- Supports volume gain (+36dB~-128dB) 0.125dB step setting with zero cross gain change
- Support microphone operates at clock frequency between 1 MHz and 6 MHz
- VAD (Voice Active Detection)
- Low power consumption
- Configuration detect levels
- Supports NPD0/1/3/IDLE mode VAD wake-up function
- Generates interrupt requests when voice detected

6.59 Key Derivation Function (KDF)

6.59.1 Overview

The KDF is an implementation fully compliant with RFC 5869 HKDF and NIST SP 800-108 feedback mode. The pseudorandom function (PRF) of this KDF is HMAC-SHA256.

The KDF derives an output key, or called output keying material, from a secret key, an input keying material (IKM, only for RFC 5869 HKDF) and a key information (info). The source of salt and above info can be configured by registers or randomly generated by PRNG with seed from TRNG. The output key, or called output keying material (OKM), can be stored in KeyStore or read from registers.

6.59.2 Features

- Supports IETF Protocols RFC 5869
- Supports NIST SP 800-108 feedback mode
- Supports 65280-bit output key at most
  - KDF output size is 256 bits; supports up to 255 expansions to reach 65280-bit output key
- Supports output key stored in KeyStore
- Supports input keying material from NVM
- Supports key information and salt from random value

6.60 Neural Network Processing Unit (NPU)

6.60.1 Overview

Neural network processing unit (NPU) is an accelerator improving the performance of processing neural network. With the help of Arm NPU Ethos-U55, NPU supports some key operations of neural network inference, such as convolution, pooling, activation. Ethos-U55 helps to do inference of the neural network model in TensorFlow Lite for Microcontrollers framework by executing the stream of commands, which are operations that might be part of or the whole neural network compiled by Vela compiler.

6.60.2 Features

- Supports 8-bit and 16-bit integer operation
  - Activations: 16-bit signed integers
  - Weights: 8-bit signed integers
- Implements 256 MACs, supporting up to 100GOPs
- Supports Performance Monitoring Unit
- Support neural network model protection (NPU_XOM, NPU_DR_XOM)

6.61 On-The-Fly Cipher (OTFC)

6.61.1 Overview

The OTFC (On-The-Fly Cipher) accelerator, integrates an address cipher function with AES-128 encryption, supports on-the-fly both encryption and decryption for external memory controller. There are four 128-bit alignment protection regions in external memory at most. The OTFC can get AES-128 key from key store.

6.61.2 Features

- Supports both on-the-fly encryption and on-the-fly decryption for external memory controller
- Supports four 128-bit alignment protection regions in external memory
- Supports address cipher function
- Supports AES encryption with 128-bits key
- Supports AES 128-bits key from key store
- Supports one technique to improve side-channel attack protection (SCAP) ability
- Supports two techniques to improve differential fault analysis protection (DFAP) ability

6.62 Analog Comparator Controller (ACMP)

6.62.1 Overview

The chip provides two ACMP controllers, each controller supports 2 comparators. Controller ACMP01 supports ACMP0 and ACMP1; controller ACMP23 supports ACMP2 and ACMP3. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.62.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to four rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV,-, 20mV,-, 40mV
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, ACMP0_P3
  - 5 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
    - DAC1 output (DAC1_OUT)
- ACMP1 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, ACMP1_P3
  - 5 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
    - DAC1 output (DAC1_OUT)
- ACMP2 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP2_P0, ACMP2_P1, ACMP2_P2, ACMP2_P3
  - 5 negative sources:
    - ACMP2_N
    - Supports Comparator Reference Voltage (CRV2)

- Internal band-gap voltage (V_{BG})
- DAC0 output (DAC0_OUT)
- DAC1 output (DAC1_OUT)

- ACMP3 support:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP3_P0, ACMP3_P1, ACMP3_P2, ACMP3_P3
  - 5 negative sources:
    - ACMP3_N
    - Supports Comparator Reference Voltage (CRV3)
    - Internal band-gap voltage (V_{BG})
    - DAC0 output (DAC0_OUT)
    - DAC1 output (DAC1_OUT)
- ACMP0 and ACMP1 share one ACMP interrupt vector, and ACMP2 and ACMP3 share one ACMP interrupt vector
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode
- Supports offset calibration
- Supports ACMP0 event, ACMP1 event, ACMP2 event, ACMP3 event be as PDMA request source
- Supports ACMP0 event, ACMP1 event, ACMP2 event, ACMP3 event be as EADC trigger source
- Supports ACMP0 output, ACMP1 output, ACMP2 output, ACMP3 output be as Timer, LPTimer, ECAP,LPADC and EPWM trigger source
- Supports ACMP0 interrupt flag, ACMP1 interrupt flag, ACMP2 interrupt flag, ACMP3 interrupt flag be as UTCPD trigger source

6.63 Digital to Analog Converter (DAC)

6.63.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.63.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 12- or 8-bit output mode.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

6.64 Low Power Analog-to-Digital Converter (LPADC)

6.64.1 Overview

The LPADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 24 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (LPADC0_ST), Low power timer 0/1, Tick timer or Wakeup I/O.

6.64.2 Features

- Supports external reference voltage from V_{REF} pin.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 24 single-end analog input channels or 12 differential analog input channels.
- Maximum LPADC peripheral clock frequency is 50 MHz
- Up to 2 MSPS sampling rate
- Scan on enabled channels
- Threshold voltage detection
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST(LPADC_ADCR[11]) bit
  - External pin (LPADC0_ST)
  - EPWM trigger
  - BPWM trigger
  - ACMP interrupt event
- Support auto-operation mode with A/D conversion can be started by:
  - Low power Timer 0/1
  - Tick Timer 0/1
  - Wakeup I/O
  - ACMP interrupt event
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~16383 LPADC clock).
- Four internal channel from band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), V_{BAT}

voltage divided by 4 and AV_{DD} voltage divided by 4.

- Supports LPPDMA transfer mode.
- Supports Calibration mode.
- Supports Floating Detect Function

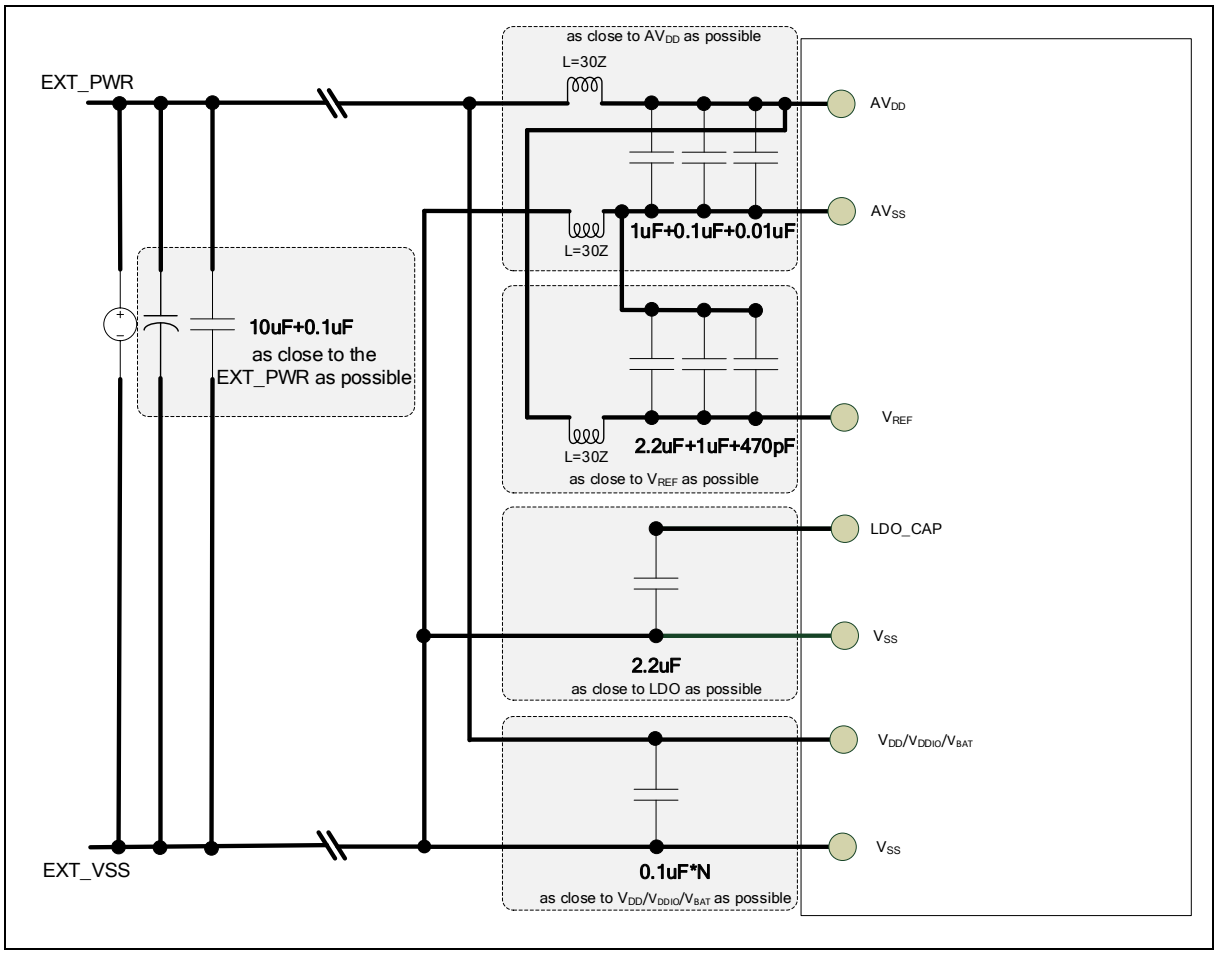
Note1: LPADC sampling rate = (LPADC peripheral clock frequency) / (total LPADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 300k SPS.

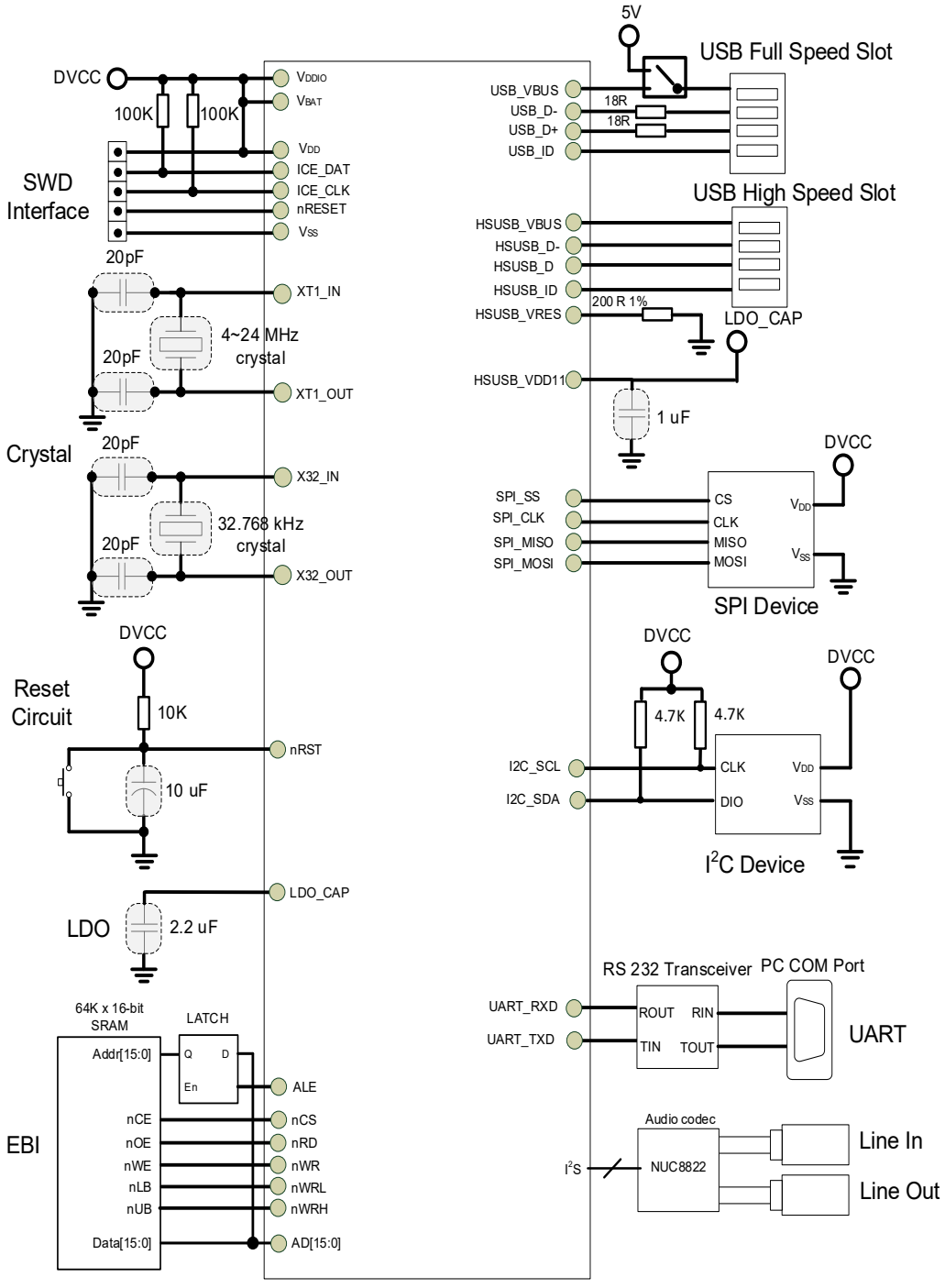
Note3: The LPADC Clock frequency must be slower than or equal to PCLK4.

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: It is recommended to connect HSUSB_VDD11 to the LDO_CAP pin, as HSUSB_VDD11 requires a 1.1 V power supply.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[1]	DC power supply	-0.3	4.5	V
V_{DDIO0}-V_{SS}[1]	V_{DDIO0} Power Supply	-0.3	5.5	V
V_{DDIO1}-V_{SS}[1]	V_{DDIO1} Power Supply	-0.3	4.5	V
V_{BAT}-V_{SS}[1]	V_{BAT} Power Supply	-0.3	4.5	V
V_{BUS}-V_{SS}[1]	V_{BUS} Power Supply	-0.3	4.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\lvert V_{SS} - AV_{SS} \rvert$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance GPIO	V_{SS}-0.3	5.5	V
	Input voltage on any other pin[2]	V_{SS}-0.3	V_{DD}	V

Notes:

1. All main power (V_{DD}, V_{DDIO}, V_{BAT}, AV_{DD}, V_{REF}, V_{BUS}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	-	50	
I_{BAT}	Maximum Current into V_{BAT}	-	50	
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[2]	-	100	
	Maximum current sourced by total I/O Pins[2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- θ_{JC} = thermal resistance junction-case (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1]	Thermal resistance junction-ambient 64-pin LQFP(10x10 mm)	-	28.5	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	21.58	-	℃/Watt
	Thermal resistance junction-ambient 176-pin LQFP(24x24 mm)	-	20.92	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

8.1.4.4 Conducted Immunity (CI)

The conducted immunity testing relates to electromagnetic disturbances coming from intended radio-frequency (RF) transmitters in the frequency range 150 kHz up to 80 MHz. The CI test is one important characteristic of touch key MCU to address the effects of unwanted noise disturbances.

The conducted immunity requirements for electronic products are defined in IEC 61000-4-6 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	-3000	-	3000	V
V_{CDM}[2]	Electrostatic discharge,charge device model	-250	-	250	
LU[3]	Pin current for latch-up[3]	-200 @ Class I	-	200 @ Class I	mA
V_{EFT}[4]	Fast transient voltage burst	-4.4	-	4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.
5. Determinded according to IEC 61000-4-6 standard and the performance class is class A.

Table 8.1-4 EMC characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
64-pin LQFP(10x10 mm) [1]	MSL 3
128-pin LQFP(14x14 mm) [1]	MSL 3
176-pin LQFP(20x20 mm) [1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

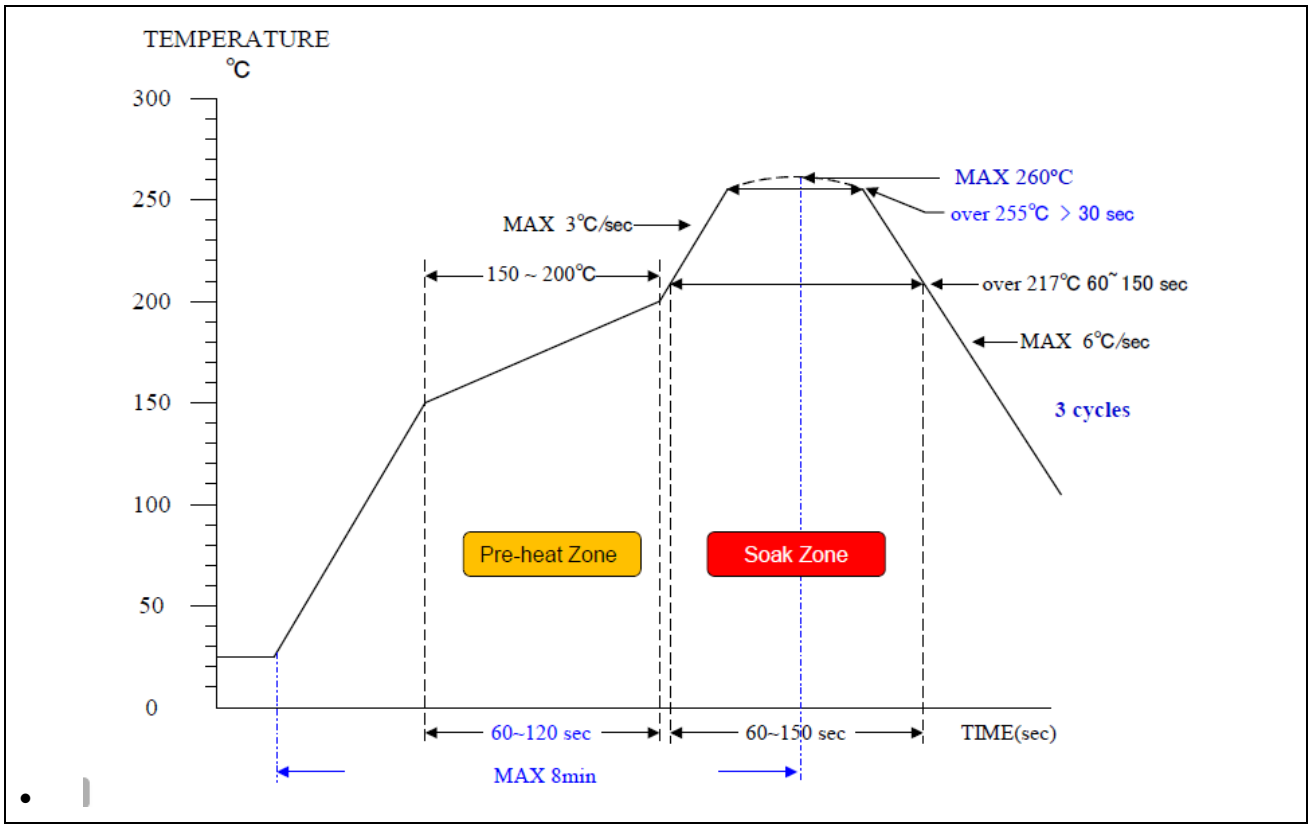


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.71 ~ 3.6 V, T_A = 25°C, HCLK = 220 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	220	MHz	
V_{DD}	Operation voltage	1.71	-	3.6	V	
V_{DDIO}	V_{DDIO} Operation voltage	1.71	-	5.5		
V_{BAT}	V_{BAT} Operation voltage	1.71	-	3.6		
AV_{DD}[1]	Analog operation voltage	V_{DD}				Except ADC, ACMP and DAC[4]
V_{REF}	Analog reference voltage	1.71	-	AV_{DD}		Except ADC[4]
V_{BG}	Band-gap voltage	1.164	1.2	1.236	V	
T_{VBG_ADC}[3]	ADC sampling time when reading the band-gap voltage	100	-	-	µS	
C_{LDO}[2]	LDO output capacitor	4.7			µF	
R_{ESR}[3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	350	450	mA	
E_{RUSH}[3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	5.17	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = TBD mA for TBD µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high(except PC0~3, ICE, Crystal pins).
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.71 ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO0} = V_{DDIO1} = V_{BAT}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT or MIRC clock	220 MHz	20.80	27.73	49.11	67.23	mA
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT or MIRC clock	200 MHz	18.10	23.19	41.05	56.64	
		192 MHz	17.43	22.48	40.29	55.89	
		180 MHz	16.43	21.25	39.14	54.71	
		160 MHz	14.99	19.32	37.19	52.82	
		144 MHz	13.87	17.73	35.65	51.30	
		120 MHz	12.01	15.40	33.31	49.32	
		96 MHz	10.32	13.32	31.34	47.67	
		84 MHz	9.21	12.07	30.22	46.57	
		72 MHz	8.27	10.87	29.29	45.66	
		60 MHz	7.31	9.85	28.35	44.70	
		50 MHz	6.44	8.82	27.48	43.83	
		48 MHz	5.61	8.00	26.57	42.89	
		32 MHz	6.56	8.67	27.75	44.28	
		12 MHz	1.64	2.86	14.40	25.22	
		8 MHz	1.19	2.41	13.96	24.79	
		6 MHz	1.03	2.26	13.81	24.63	
		4 MHz	0.95	2.18	13.73	24.55	
		2 MHz	0.87	2.11	13.67	24.48	

		1 MHz	0.80	2.03	13.59	24.42	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HIRC, PLL, HXT or MIRC clock	220 MHz	67.94	75.82	96.65	114.22	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT or MIRC clock	200 MHz	58.57	63.77	81.14	96.26	
		192 MHz	56.34	61.52	78.82	93.97	
		180 MHz	52.97	57.93	75.35	90.59	
		160 MHz	47.61	52.02	69.56	84.86	
		144 MHz	43.32	47.31	64.89	80.24	
		120 MHz	36.72	40.21	57.87	73.66	
		96 MHz	35.05	38.14	55.91	72.01	
		84 MHz	30.94	33.90	51.83	68.00	
		72 MHz	27.01	29.71	47.93	64.12	
		60 MHz	23.04	25.67	44.01	60.27	
		50 MHz	20.07	22.51	41.07	57.35	
		48 MHz	18.51	20.97	39.33	55.48	
		32 MHz	15.63	17.77	36.91	53.46	
		12 MHz	4.42	5.64	17.20	28.03	
		8 MHz	2.72	3.94	15.53	26.38	
		6 MHz	2.15	3.37	14.97	25.84	
		4 MHz	1.87	3.09	14.69	25.56	
		2 MHz	1.59	2.81	14.41	25.27	
		1 MHz	1.30	2.53	14.12	25.01	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT or MIRC clock	220 MHz	11.63	14.79	36.31	54.58	mA
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT or MIRC clock	200 MHz	10.04	12.36	31.03	47.38	
		192 MHz	9.69	12.02	30.70	47.05	
		180 MHz	9.17	11.50	30.18	46.53	
		160 MHz	8.30	10.63	29.30	45.65	
		144 MHz	7.60	9.93	28.61	44.94	
		120 MHz	6.56	8.90	27.55	43.92	
		96 MHz	5.75	8.09	26.75	43.10	
		84 MHz	5.21	7.54	26.21	42.58	
		72 MHz	4.66	7.00	25.67	42.03	
		60 MHz	4.30	6.63	25.31	41.70	
		50 MHz	3.81	6.15	24.82	41.19	
		48 MHz	3.09	5.45	24.06	40.37	
		32 MHz	4.88	6.99	26.04	42.57	
		12 MHz	1.11	2.33	13.87	24.69	
		8 MHz	0.91	2.15	13.69	24.50	
		6 MHz	0.85	2.08	13.62	24.43	
		4 MHz	0.82	2.05	13.59	24.40	
		2 MHz	0.78	2.02	13.56	24.37	
		1 MHz	0.75	1.99	13.52	24.34	
	Idle mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HIRC, PLL, HXT or MIRC clock	220 MHz	57.69	61.90	82.94	100.69	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT or MIRC clock	200 MHz	49.58	52.05	70.21	86.20	
		192 MHz	47.70	50.16	68.38	84.35	
		180 MHz	44.87	47.33	65.61	81.57	
		160 MHz	40.13	42.59	60.92	76.96	
		144 MHz	36.35	38.78	57.17	73.25	
		120 MHz	30.67	33.08	51.52	67.70	
		96 MHz	30.00	32.41	50.86	66.99	

		84 MHz	26.52	28.91	47.41	63.61	
		72 MHz	23.04	25.40	43.94	60.18	
		60 MHz	19.72	22.07	40.69	56.96	
		50 MHz	17.17	19.51	38.15	54.45	
		48 MHz	15.74	18.18	36.58	52.75	
		32 MHz	13.79	15.91	35.03	51.58	
		12 MHz	3.83	5.05	16.61	27.44	
		8 MHz	2.43	3.64	15.23	26.07	
		6 MHz	1.96	3.18	14.76	25.61	
		4 MHz	1.72	2.94	14.53	25.39	
		2 MHz	1.49	2.71	14.30	25.16	
		1 MHz	1.25	2.48	14.07	24.92	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	Power Level	LXT[1] 32.768 kHz	LIRC 32 kHz	Typ[2]				Max[3][4]			Unit
					T_A= 25 °C				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
					1.7 V	2.4 V	3.0 V	3.6 V	3.6 V	3.6 V	3.6 V	
I_{DD_DPD1}	Deep Power-down mode, all peripherals disable	-	-	-	0.13	0.17	0.28	0.92	3.17	38.57	62.18	µA
	Deep Power-down mode, RTC enable and run	-	V	-	0.69	0.75	0.89	1.57	3.76	39.10	62.66	
	Deep Power-down mode, RTC enable and run	-	-	V	0.41	0.49	0.64	1.33	3.58	38.58	61.90	
I_{DD_DPD0}	Deep Power-down mode, all peripherals disable	-	-	-	0.53	0.56	0.67	1.31	3.54	38.33	61.52	uA
	Deep Power-down mode, RTC enable and run	-	V	-	1.08	1.15	1.28	1.96	4.18	38.96	62.14	
	Deep Power-down mode, RTC enable and run	-	-	V	0.81	0.88	1.03	1.72	3.96	38.51	61.54	
I_{DD_SPD1}	SPD1 mode, all peripherals disable without SRAM retention	PL4	-	-	4.47	4.85	5.61	7.60	11.26	64.30	99.65	µA
	SPD1 mode, all peripherals disable with 64KB SRAM retention	PL4	-	-	4.96	5.34	6.09	8.05	12.70	192.01	311.55	
	SPD1 mode, all peripherals disable with 128KB SRAM retention	PL4	-	-	5.40	5.77	6.53	8.49	14.16	279.15	455.81	
	SPD1 mode, all peripherals disable with 192KB SRAM retention	PL4	-	-	5.86	6.23	6.98	8.96	15.58	366.31	600.12	
	SPD1 mode, all peripherals disable with 256KB SRAM retention	PL4	-	-	6.30	6.69	7.43	9.39	17.11	453.82	744.96	

	SPD1 mode, all peripherals disable with 320KB SRAM retention	PL4	-	-	6.75	7.12	7.86	9.84	18.58	541.13	889.49	
	SPD1 mode, all peripherals disable with 384KB SRAM retention	PL4	-	-	7.21	7.58	8.32	10.30	20.09	628.15	1033.53	
	SPD1 mode, all peripherals disable with 448KB SRAM retention	PL4	-	-	7.65	8.02	8.76	10.78	21.54	715.64	1178.37	
	SPD1 mode, all peripherals disable with 512KB SRAM retention	PL4	-	-	8.10	8.48	9.21	11.20	23.00	802.43	1322.05	
	SPD1 mode, all peripherals disable with 512KB SRAM retention (8K LPSRAM retention)	PL4	-	-	8.19	8.58	9.31	11.30	23.52	809.33	1333.20	
	SPD1 mode, all peripherals disable without SRAM retention, RTC enable and run	PL4	V	-	5.03	5.43	6.20	8.23	11.89	65.26	100.85	
	SPD1 mode, all peripherals disable without SRAM retention, RTC enable and run	PL4	-	V	4.75	5.16	5.96	7.99	11.66	64.75	100.13	
I_{DD_SPD0}	SPD0 mode, all peripherals disable without SRAM retention	PL0	-	-	5.37	5.75	6.50	8.47	16.88	154.65	250.29	uA
		PL1	-	-	5.21	5.59	6.35	8.31	15.88	147.61	238.77	
	SPD0 mode, all peripherals disable with 64KB SRAM retention	PL0	-	-	8.52	8.89	9.64	11.61	18.19	303.83	494.26	
		PL1	-	-	7.88	8.25	9.01	10.99	17.00	286.72	466.54	
	SPD0 mode, all peripherals disable with 128KB SRAM retention	PL0	-	-	11.37	11.75	12.49	14.49	25.11	450.50	734.10	
		PL1	-	-	10.31	10.69	11.42	13.39	23.12	423.82	690.95	

	SPD0 mode, all peripherals disable with 192KB SRAM retention	PL0	-	-	14.25	14.60	15.37	17.33	32.16	597.08	973.69	
		PL1	-	-	12.76	13.12	13.86	15.87	29.23	559.22	912.55	
	SPD0 mode, all peripherals disable with 256KB SRAM retention	PL0	-	-	17.09	17.46	18.21	20.18	39.16	744.09	1214.05	
		PL1	-	-	15.19	15.57	16.32	18.32	35.42	696.08	1136.51	
	SPD0 mode, all peripherals disable with 320KB SRAM retention	PL0	-	-	19.97	20.33	21.07	23.05	46.12	890.70	1453.75	
		PL1	-	-	17.62	17.98	18.76	20.72	41.57	832.82	1360.32	
	SPD0 mode, all peripherals disable with 384KB SRAM retention	PL0	-	-	22.83	23.19	23.93	25.91	53.21	1037.26	1693.30	
		PL1	-	-	20.08	20.43	21.18	23.18	47.78	969.16	1583.42	
	SPD0 mode, all peripherals disable with 448KB SRAM retention	PL0	-	-	25.69	26.06	26.81	28.78	60.17	1183.89	1933.04	
		PL1	-	-	22.50	22.87	23.61	25.60	53.99	1105.84	1807.06	
	SPD0 mode, all peripherals disable with 512KB SRAM retention	PL0	-	-	28.57	28.91	29.62	31.60	67.17	1329.33	2170.77	
		PL1	-	-	24.97	25.31	26.04	28.02	60.00	1241.08	2028.47	
	SPD0 mode, all peripherals disable with 512KB SRAM retention (8K LPSRAM retention)	PL0	-	-	29.07	29.45	30.18	32.14	69.17	1344.03	2193.93	
		PL1	-	-	25.43	25.76	26.50	28.48	61.40	1344.81	2200.41	
	SPD0 mode, all peripherals disable without SRAM retention, RTC enable and run	PL0	V	-	5.93	6.35	7.12	9.13	16.85	155.67	251.55	
		PL1	V	-	5.77	6.17	6.96	8.97	16.47	148.60	240.02	
	SPD0 mode, all peripherals disable without SRAM retention, RTC enable and run	PL0	-	V	5.65	6.05	6.86	8.89	16.67	155.12	250.76	
		PL1	-	V	5.49	5.91	6.71	8.74	16.29	148.08	239.27	
I_{NPD4}	NPD4 mode, all peripherals disable without SRAM retention				10.89	11.25	11.99	13.94	47.51	884.21	1442.01	uA
	NPD4 mode, all peripherals disable with 64KB SRAM retention				11.38	11.76	12.50	14.42	49.01	908.85	1482.08	
	NPD4 mode, all peripherals disable without SRAM retention (8K LPSRAM retention)				10.93	11.29	12.04	13.95	47.70	885.95	1444.79	

	NPD4 mode, all peripherals disable with 512KB SRAM retention (8K LPSRAM retention) (LVR disable)				14.20	14.56	15.33	17.24	58.21	1251.72	2047.40	
	NPD4 mode, RTC enable and run (SRAM with retain 512K)		V		15.12	15.51	16.30	18.23	59.13	1255.65	2053.33	
	NPD4 mode, RTC use RC32K (SRAM with retain 512K)			V	14.84	15.24	16.02	18.01	58.90	1252.78	2048.70	
I_{NPD3}	NPD3 mode, all peripherals disable without SRAM retention	PL0	-	-	32.44	32.80	33.55	35.46	175.16	1892.67	3037.68	uA
		PL1	-	-	28.99	29.34	30.09	31.99	136.72	1749.81	2825.20	
	NPD3 mode, all peripherals disable with 64KB SRAM retention	PL0	-	-	35.58	35.97	36.70	38.61	180.96	1993.35	3201.60	
		PL1	-	-	31.65	32.00	32.71	34.65	142.00	1832.22	2959.03	
	NPD3 mode, all peripherals disable without SRAM retention (8K LPSRAM retention)	PL0	-	-	32.71	33.05	33.81	35.74	175.47	1896.77	3044.30	
		PL1	-	-	29.19	29.57	30.29	32.20	137.13	1752.65	2829.67	
	NPD3 mode, all peripherals disable with 512KB SRAM retention (8K LPSRAM retention) (LVR disable)	PL0	-	-	55.50	55.87	56.59	58.47	219.37	2672.84	4308.49	
		PL1	-	-	48.57	48.91	49.63	51.50	176.38	2387.44	3861.49	
	NPD3 mode, RTC enable and run (SRAM with retain 512K)	PL0	V	-	56.45	56.82	57.57	59.50	220.38	2680.98	4321.38	
		PL1	V	-	49.50	49.86	50.62	52.55	177.48	2394.14	3871.91	
	NPD3 mode, WDT/LPTimer/LPUART/RTC enable and run (SRAM with retain 512K)	PL0	V	-	56.62	56.99	57.71	59.64	220.48	2680.49	4320.51	
		PL1	V	-	49.64	49.98	50.78	52.70	177.49	2393.50	3870.84	
	NPD3 mode, WDT/LPTimer use LIRC, RTC use RC32K (SRAM with retain 512K)	PL0	-	V	56.65	57.08	57.91	59.92	220.55	2673.95	4309.55	
		PL1	-	V	49.65	50.09	50.92	52.90	177.59	2387.83	3861.33	
	NPD3 mode,	PL0	V	V	56.97	57.39	58.17	60.17	220.80	2681.02	4321.16	

	WDT/LPTimer use LIRC, LPUART/RTC use LXT (SRAM with retain 512K)	PL1	V	V	50.01	50.39	51.18	53.20	177.69	2393.82	3871.24	
I_{NPD2}	NPD2 mode, all peripherals disable	PL2			254.40	255.15	256.72	259.95	1880.83	27456.12	44506.31	uA
	NPD2 mode, all peripherals disable (LVR disable)	PL2			254.11	254.89	256.40	259.63	1880.31	27453.42	44502.15	
	NPD2 mode, RTC enable and run	PL2	V		255.17	255.98	257.49	260.82	1882.58	27492.78	44566.24	
	NPD2 mode, RTC use RC32K	PL2		V	254.83	255.57	257.13	260.49	1881.31	27455.91	44505.65	
I_{NPD1}	NPD1 mode, all peripherals disable	PL0	-	-	859.84	860.67	863.03	866.26	6393.83	62793.95	100394.02	uA
		PL1	-	-	762.44	763.31	764.87	770.03	5344.76	54534.24	87327.23	
	NPD1 mode, all peripherals disable (LVR disable)	PL0	-	-	859.70	860.21	862.42	865.51	6391.34	62797.29	100401.26	
		PL1	-	-	762.26	763.06	764.14	768.53	5346.59	54542.05	87339.01	
	NPD1 mode, RTC enable and run	PL0	V	-	860.64	861.10	863.94	867.15	6394.85	62811.77	100423.06	
		PL1	V	-	763.46	763.94	765.39	770.50	5346.32	54567.95	87382.38	
	NPD1 mode, WDT/Timer/UART/RTC enable and run	PL0	V	-	861.67	862.45	864.65	867.99	6394.00	62825.42	100446.36	
		PL1	V	-	764.25	765.26	766.59	770.96	5350.10	54568.93	87381.48	
	NPD1 mode, WDT/Timer use LIRC, RTC use RC32K	PL0	-	V	861.02	861.66	864.02	867.31	6391.17	62788.23	100386.27	
		PL1	-	V	763.53	764.48	765.90	770.18	5344.87	54543.41	87342.43	
	NPD1 mode, WDT/Timer use LIRC, UART/RTC use LXT	PL0	V	V	862.34	862.95	865.49	868.96	6398.12	62813.65	100423.99	
		PL1	V	V	764.31	765.12	766.47	771.13	5351.23	54553.22	87354.55	
I_{NPD0}	NPD0 mode, all peripherals disable	PL0	-	-	944.06	946.46	949.09	952.55	6488.66	63673.97	101797.50	uA
		PL1	-	-	846.30	847.96	849.67	854.28	5437.83	55412.55	88729.03	
	NPD0 mode, WDT/Timer/UART/RTC enable and run	PL0	V	-	946.61	948.39	951.06	954.41	6491.88	63697.49	101834.56	
		PL1	V	-	850.15	851.92	854.10	858.60	5439.31	55442.02	88777.16	
	NPD0 mode, WDT/Timer use LIRC, RTC use RC32	PL0	-	V	946.15	947.92	950.77	954.19	6495.39	63682.73	101807.62	
		PL1	-	V	849.46	851.26	853.56	858.25	5442.47	55418.65	88736.10	
	NPD0 mode, WDT/Timer use LIRC, UART/RTC use LXT	PL0	V	V	947.13	948.88	951.73	955.64	6492.06	63711.87	101858.42	
		PL1	V	V	850.34	852.44	854.59	859.71	5441.82	55436.47	88766.24	

Table 8.3-3 Chip Current Consumption in Power-down mode

Symbol	Test Conditions	LXT[1] 32.768 kHz	LIRC 38.4 kHz	Typ				Max[2]			Unit
				T_A = 25 °C				T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
				1.7 V	2.4 V	3.0V	3.6 V	3.6 V	3.6 V	3.6 V	
I_{BAT}	RTC off	-	-	0.06	0.09	0.15	0.33	0.44	1.15	1.93	µA
	RTC on	V	-	0.59	0.64	0.72	0.92	1.04	1.86	2.74	
	RTC on	-	V	0.34	0.41	0.51	0.75	0.83	1.54	2.37	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a CL of 20 pF for L7 gain level.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-4 V_{BAT} Current Consumption in Power-down mode

Symbol	Test Conditions	Typ[1]			Unit
		25°C	85°C	105°C	
I_{DD_SRAM}	SRAM 64 KB static consumption	2.53	12.85	25.28	µA
	SRAM 128 KB static consumption	4.86	24.40	47.96	
	SRAM 192 KB static consumption	7.15	36.01	76.35	
	SRAM 256 KB static consumption	9.46	47.62	100.38	
	SRAM 320 KB static consumption	11.73	59.16	124.32	
	SRAM 384 KB static consumption	14.10	73.21	148.36	
	SRAM 448 KB static consumption	16.38	85.89	172.51	
	SRAM 512 KB static consumption	18.70	100.10	196.38	

Table 8.3-5 SRAM Static Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{BAT} = 3 V unless otherwise specified.
- All GPIO pins are in push pull mode and output high(except PC0~3, ICE, Crystal pins).
- HCLK is the system clock, f_{HCLK} = 220 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[1]	Unit
CANFD0	1661	uA
CANFD1	1784	
CRC0	240	
CRYPTO0	688	
EBI0	251	
EMAC0	2043	
GPIOA	328	
GPIOB	333	
GPIOC	318	
GPIOD	348	
GPIOE	345	
GPIOF	336	
GPIOG	332	
GPIOH	339	
GPIOI	331	
GPIOJ	339	
KDF0	376	
KS0	411	
PDMA0	499	
PDMA1	512	
SDH0	1334	
SDH1	1461	
SRAM3	222	
USBH0[4]	728	
HSUSBD0[4]	548	
HSUSBH0[4]	2673	
BPWM0	84	
EADC0[2]	1404	

ECAP0	43	
ECAP2	52	
EPWM0	426	
EQEI0	51	
EQEI2	56	
I2C0	73	
I2C2	77	
QSPI0	357	
SPI0	374	
SPI2	395	
UART0	277	
UART2	207	
UART4	196	
WWDT0	78	
ACMP01[3]	267	
DAC01[5]	120	
I2S0	242	
PSIO0	732	
SC0	252	
SC2	179	
TMR0	227	
TMR1	230	
UART6	234	
UART8	240	
USBD0[4]	604	
USCI0	163	
HSOTG0[4]	173	
BPWM1	152	
ECAP1	114	
ECAP3	113	
EPWM1	459	
EQEI1	102	
EQEI3	105	
I2C1	132	
I2C3	115	

QSPI1	424	
SPI1	409	
SPI3	396	
UART1	264	
UART3	215	
UART5	219	
WWDT1	86	
ACMP23[3]	284	
I2S1	223	
I3C0	2096	
KPI0	239	
OTG0[4]	153	
RTC0	133	
SC1	251	
TMR2	226	
TMR3	231	
TRNG0	186	
UART7	225	
UART9	222	
UTCPD0[6]	266	
OTFC0	167	
SPIM0	7434	
CCAP0	453	
LPGPIO0	80	
LPPDMA0	243	
LPSRAM0	118	
SCU0	348	
AWF0	78	
DMIC0	172	
LPADC0[3]	173	
LPI2C0	92	
LPSPI0	213	
LPTMR0	142	
LPTMR1	141	
LPUART0	235	

WDT0	81	
WDT1	81	
TTMR0	143	
TTMR1	149	
FMC0	459	
GDMA0	3052	
NPU0	363	
SRAM0	696	
SRAM1	724	
SRAM2	562	
ISP0	69	
ST0	180	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.
6. When the UTCPD is turned on, add an additional power consumption per UTCPD for the analog part.

Table 8.3-6 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode	3.28	μS
t_{WU_DPD}[1][2]	Wakeup from DPD mode	596.08	
t_{WU_SPD}[1][2]	Wakeup from SPD mode	628.51	
t_{WU_NPD3}[1][2]	Wakeup from NPD3 mode running in flash	84.07	
	Wakeup from NPD3 mode running in RAM	86.68	
t_{WU_NPD2}[1][2]	Wakeup from NPD2 mode running in flash	79.80	
	Wakeup from NPD2 mode running in RAM	79.42	
t_{WU_NPD1}[1][2]	Wakeup from NPD1 mode running in flash	53.38	
	Wakeup from NPD1 mode running in RAM	52.99	
t_{WU_NPD0}[1][2]	Wakeup from NPD0 mode running in flash	26.77	
	Wakeup from NPD0 mode running in RAM	26.52	
t_{ET_IDLE}[1]	Enter to IDLE mode	N/A	
t_{ET_DPD}[1]	Enter to DPD mode	12.43	
t_{ET_SPD}[1]	Enter to SPD mode	13.30	
t_{ET_NPD3}[1]	Enter to NPD3 mode	13.37	
t_{ET_NPD2}[1]	Enter to NPD2 mode	12.37	
t_{ET_NPD1}[1]	Enter to NPD1 mode	12.57	
t_{ET_NPD0}[1]	Enter to NPD0 mode	12.37	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-7 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	-		Injected current on any 5V tolerance I/O except analog input pin
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-8 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	V_{DD}=3.6V
	Input low voltage (TTL trigger)	0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.8 V[1]
		0	-	0.4		V_{DD} = 1.71 V[1]
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 3.6 V
		1.2	-	V_{DD}		V_{DD} = 1.8 V[1]
		1.0	-	V_{DD}		V_{DD} = 1.71 V[1]
V_{HY}[1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[2]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 3.6 V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[1]	Pull up resistor	40	51	61	kΩ	V_{DD}=1.71~3.6V
R_{PD}[1]	Pull down resistor	40	51	61	kΩ	V_{DD}=1.71~3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-9 I/O input characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2] [3]	Source current for quasi-bidirectional mode and high level	-6.82	-7.93	-9.84	µA	V_{DD} = 3.6 V V_{IN}=(V_{DD}-0.4) V
		-	-4.84	-		PC2, PC3
		-6.82	-7.94	-9.82	µA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-	-5.69	-		PC2, PC3
		-6.79	-7.92	-9.77	µA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
		-	-6.52	-		PC2, PC3
		-6.78	-7.91	-9.75	µA	V_{DD} = 1.71 V V_{IN}=(V_{DD}-0.4) V
		-	-6.62	-		PC2, PC3
	Source current for push-pull mode and high level	-15.4	-17.8	-24.3	mA	V_{DD} = 3.6 V V_{IN}=(V_{DD}-0.4) V
		-12	-13.9	-21	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-7.67	-8.82	-13	mA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
		-6.6	-8.38	-11.1	mA	V_{DD} = 1.71 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[1] [2] [4]	Sink current for push-pull mode and low level	14.9	18.8	26.5	mA	V_{DD} = 3.6 V V_{IN}= 0.4 V
		12	16.2	24.5	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		7.54	10.6	16.4	mA	V_{DD} = 1.8 V V_{IN}= 0.4 V
		6.37	9.6	13.9	mA	V_{DD} = 1.71 V V_{IN}= 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.
3. The range of output high level voltage (V_{OH}) is from V_{DD}-0.4 to V_{DD} based on minimum value of source current (I_{SR}).
4. The range of output low level voltage (V_{OL}) is from 0 to 0.4 based on minimum value of sink current (I_{SK}).

Table 8.3-10 I/O output characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	40.6	49.7	58.6	kΩ	V_{DD}=1.71~3.6V
t_{RP}[1]	Minimum nRESET pulse width	33	-	-	µS	Normal run and Idle mode
		35	-	-		NPD0 mode
		35	-	-		NPD1 mode
		0.23	-	-		NPD2 mode
		35	-	-		NPD3 mode
		0.23	-	-		NPD4 mode
		0.23	-	-		SPD mode
		0.25	-	-		DPD mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-11 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	1.71	-	3.6	V	
f_{HIRC}	Oscillator frequnecy	46.8	48	49.2	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2.5	-	2.5	%	T_A = 25 °C, V_{DD} = 3.3V
		-2.5	-	2.5	%	T_A = -20 ~ +85 °C, V_{DD} = 1.71 ~ 3.6 V
		-4	-	4	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.71 ~ 3.6V
I_{HIRC}[1]	Operating current	-	200	-	μA	
T_S [*2]	Stable time	-	5	10	μS	T_A = -40°C ~ +105 °C, V_{DD} = 1.71 ~ 3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

The 12 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	1.71	-	3.6	V	
F_{MIRC}	Oscillator frequnecy	11.82	12	12.18	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2.5	-	+2.5	%	T_A = 0 ~ +85 °C, V_{DD} = 1.71 ~ 3.6 V
		-3.5	-	3.5	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.71 ~ 3.6V
I_{MIRC}[1]	Operating current	-	135	-	μA	V_{DD} = 3.3V
T_S [*2]	Stable time	-	-	20	μS	T_A = -40 ~ +105 °C, V_{DD} = 1.71 ~ 3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.3 1~8 MHz Internal Median Speed RC Oscillator (MIRC)

The 1~8 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operating voltage	1.71	-	3.6	V	
F_{MIRC}	Oscillator frequnecy	0.975	1	1.025	MHz	T_A = 25 °C, V_{DD} = 3.3V
		1.95	2	2.05		
		3.9	4	4.1		
		7.8	8	8.2		
	Frequency drift over temperature and voltage	-2.5	-	+2.5	%	T_A = 25 °C, V_{DD} = 3.3V
		-3.5	-	+3.5	%	T_A = -40 ~ +105 °C V_{DD} = 1.71 ~ 3.6V
I_{MIRC}[*1]	Operating current	-	10	-	μA	1MHz, V_{DD} = 3.3V
		-	15	-		2MHz, V_{DD} = 3.3V
		-	20	-		4MHz, V_{DD} = 3.3V
		-	30	-		8MHz, V_{DD} = 3.3V
T_S[*2]	Stable time	-	10	-	μS	1MHz, T_A = -40 ~ +105 °C, V_{DD} = 1.71 ~ 3.6V
		-	6	-		2MHz, T_A = -40 ~ +105 °C, V_{DD}= 1.71 ~ 3.6V
		-	8	-		4MHz, T_A = -40 ~ +105 °C, V_{DD}= 1.71 ~ 3.6V
		-	10	-		8MHz, T_A = -40 ~ +105 °C, V_{DD} = 1.71 ~ 3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design

Table 8.4-3 1~8 MHz Internal Median Speed RC Oscillator(MIRC) Characteristics

8.4.4 32 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max[1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operating voltage	1.71	-	3.6	V	
F_{LIRC}	Oscillator frequnecy	-	32	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperature and voltage	- 1	-	-1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2	-	+2	%	T_A = -40 ~ +105 °C V_{DD} = 1.71 ~ 3.6V
I_{LIRC}[*1]	Operating current	-	175	230	nA	V_{DD} = 3.3V
T_S [*2]	Stable time	-	-	500	µS	T_A = -40 ~ +105 °C V_{DD} = 1.71 ~ 3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-4 32 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.5 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.71	-	3.6	V	
R_f	Internal feedback resister	-	0.2	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT_INV}	Current consumption	-	350	-	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	2200	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2500	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	2800	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	6400	-		32 MHz, Gain = L4, C_L = 12.5 pF
I_{HXT_GM}	Current consumption	-	350	-	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	650	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	950	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	1500	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	2500	-		32 MHz, Gain = L4, C_L = 12.5 pF
T_{S_INV}	Stable time	-	3050	-	μs	4 MHz, Gain = L0, C_L = 12.5 pF
		-	1600	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	1350	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	770	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	400	-		32 MHz, Gain = L4, C_L = 12.5 pF
T_{S_GM}	Stable time	-	3075	-	μs	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3420	-		12 MHz, Gain = L1, C_L = 12.5 pF

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
		-	2450	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	1720	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	750	-		32 MHz, Gain = L4, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1	-	V	

Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	150	Ω	4 MHz, Gain = L0, C_L = 12.5 pF
		-	-	120		12 MHz, Gain = L1, C_L = 12.5 pF
		-	-	100		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	-	80		24 MHz, Gain = L3, C_L = 12.5 pF
		-	-	50		32 MHz, Gain = L4, C_L = 12.5 pF

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

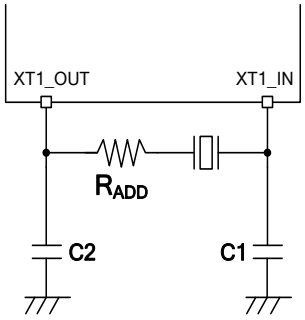


Table 8.4-6 External 4~32 MHz High Speed Crystal Characteristics

8.4.5.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1

4 MHz ~ 32 MHz	10 ~ 20 pF	10 ~ 20 pF	without

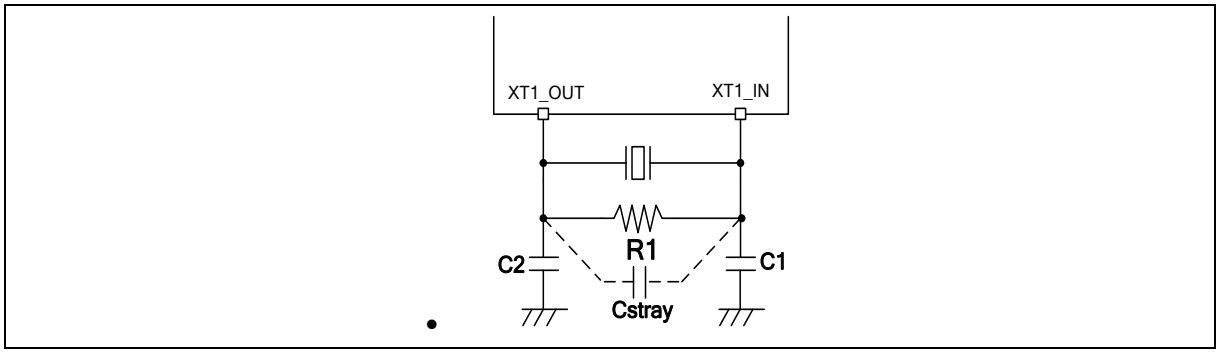
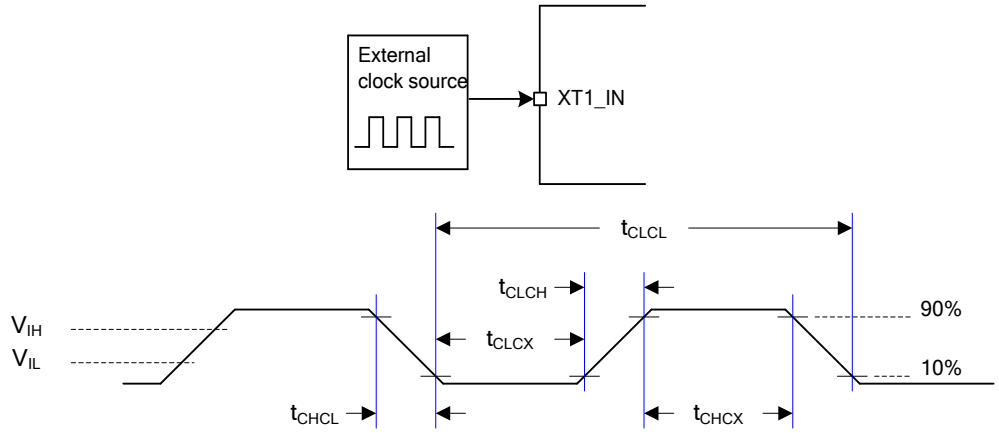


Figure 8.4-1 Typical Crystal Application Circuit

8.4.6 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The XT1_IN is set as schmitt trigger input mode.
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The XT1_IN is set as schmitt trigger input mode.



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-7 External 4~32 MHz High Speed Clock Input Signal

8.4.7 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD} or V_{BAT}	Operation voltage	1.71	-	3.6	V	
R_f	Internal feedback resistor	-	12	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	210	-	nA	ESR=35 kΩ, C_L = 6 pF, Gain = L0
		-	220	-		ESR=35 kΩ, C_L = 6 pF, Gain = L1
		-	240	-		ESR=35 kΩ, C_L = 6 pF, Gain = L2
		-	260	-		ESR=35 kΩ, C_L = 6 pF, Gain = L3
		-	370	-		ESR=35 kΩ, C_L = 6 pF, Gain = L4
		-	390	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L5
		-	410	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L6
		-	490	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L7
		-	510	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L8
		-	530	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L9
		-	660	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L10
		-	680	-		ESR=35 kΩ, C_L = 12.5 pF, Gain = L11
		-	700	-		ESR=70 kΩ, C_L = 12.5 pF, Gain = L12
		-	900	-		ESR=70 kΩ, C_L = 12.5 pF, Gain = L13
		-	920	-		ESR=70 kΩ, C_L = 12.5 pF, Gain = L14
		-	950	-		ESR=70 kΩ, C_L = 12.5 pF, Gain = L15
Ts_{LXT}	Stable time	-	1	2	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.3	-	-	V	

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (Sf) must be higher than 5 for LXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the LXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

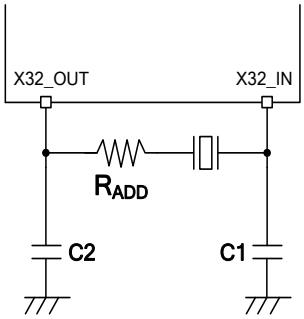


Table 8.4-8 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-9 External 32.768 kHz Low Speed Crystal Characteristics

8.4.7.2 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 5 pF ~ 20 pF range, designed for RTC applications, and selected to match the requirements of the crystal. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	7 ~ 20 pF	7 ~ 20 pF	without

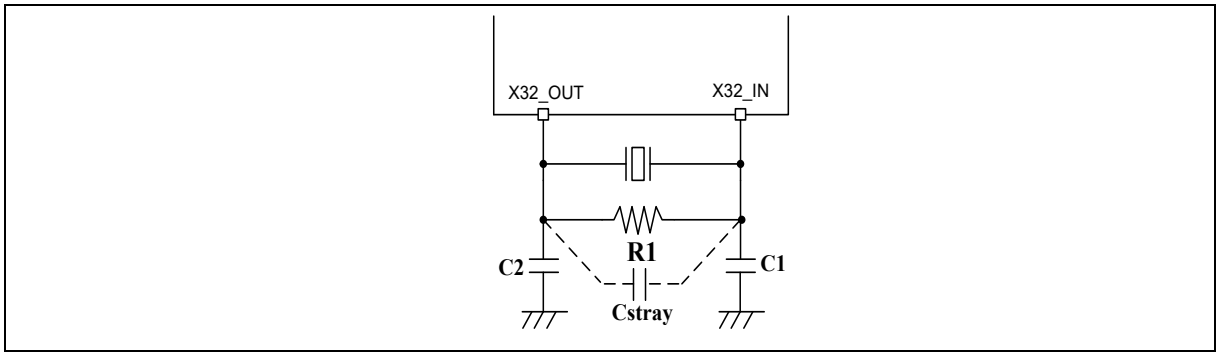
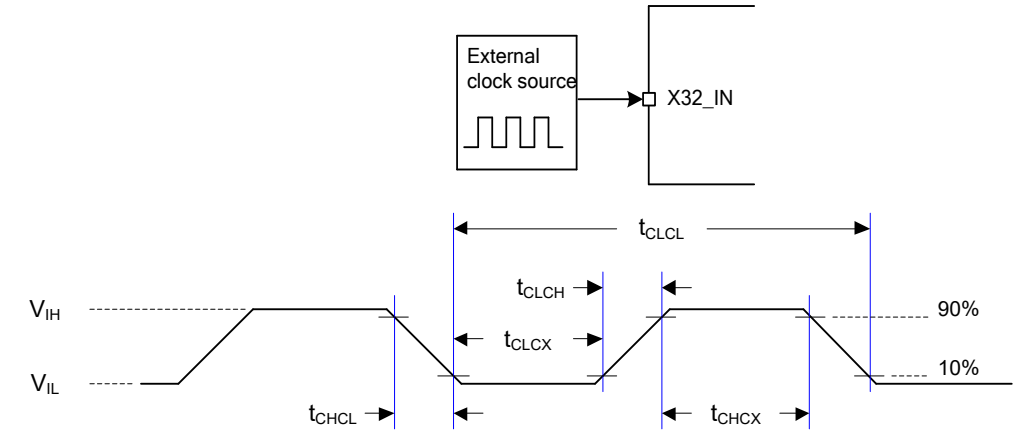


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.8 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
V_{IH}	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	$V_{BAT} = V_{DD}$ The X32_IN is set as schmitt trigger input mode.
V_{IL}	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	$V_{BAT} = V_{DD}$ The X32_IN is set as schmitt trigger input mode.



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-10 External 32.768 kHz Low Speed Clock Input Signal

8.4.9 PLL Characteristics

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{PLL_in}	PLL input clock	1	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	25	-	500	MHz	
f_{PLL_REF}	PLL reference clock	1	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	100	-	500	MHz	
T_L	PLL locking time	-	-	<200	μS	
Jitter[2]	Cycle-to-cycle Jitter	-	250	-	pS	
I_{DD}	Power consumption	-	2.0	2.6	mA	f_{PLL_VCO} = 500 MHz

Notes:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-11 PLL Characteristics

8.4.10 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	8.05	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	5.44		CL = 10 pF, V_{DD} >= 3.6 V
		-	9.67		CL = 30 pF, V_{DD} >= 2.7 V
		-	6.62		CL = 10 pF, V_{DD} >= 2.7 V
		-	14.6		CL = 30 pF, V_{DD} >= 1.71 V
		-	10.2		CL = 10 pF, V_{DD} >= 1.71 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	4.82		C_L = 30 pF, V_{DD} >= 3.6 V
		-	3.08		C_L = 10 pF, V_{DD} >= 3.6 V
		-	5.77		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3.66		C_L = 10 pF, V_{DD} >= 2.7 V
		-	9.20		C_L = 30 pF, V_{DD} >= 1.71 V
		-	5.64		C_L = 10 pF, V_{DD} >= 1.71 V
	Output high (90%) to low level (10%) fall time (Fast Slew Rate)	-	3.04	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.51		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3.72		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.86		C_L = 10 pF, V_{DD} >= 2.7 V
		-	6.69		C_L = 30 pF, V_{DD} >= 1.71 V
		-	3.33		C_L = 10 pF, V_{DD} >= 1.71 V
	Output high (90%) to low level (10%) fall time (Ultra-Fast Slew Rate)	-	2.44	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.23		C_L = 10 pF, V_{DD} >= 3.6 V
		-	2.99		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.51		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5.36		C_L = 30 pF, V_{DD} >= 1.71 V
		-	2.69		C_L = 10 pF, V_{DD} >= 1.71 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	7.93	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	5.48		C_L = 10 pF, V_{DD} >= 3.6 V
		-	9.47		C_L = 30 pF, V_{DD} >= 2.7 V
		-	6.60		C_L = 10 pF, V_{DD} >= 2.7 V
		-	13.74		C_L = 30 pF, V_{DD} >= 1.71 V

		-	9.66		C_L = 10 pF, V_{DD} >= 1.71 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	4.87	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	3.15		C_L = 10 pF, V_{DD} >= 3.6 V
		-	5.80		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3.74		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8.90		C_L = 30 pF, V_{DD} >= 1.71 V
		-	5.54		C_L = 10 pF, V_{DD} >= 1.71 V
	Output low (10%) to high level (90%) rise time (Fast Slew Rate)	-	2.92	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.51		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3.70		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.91		C_L = 10 pF, V_{DD} >= 2.7 V
		-	6.48		C_L = 30 pF, V_{DD} >= 1.71 V
		-	3.32		C_L = 10 pF, V_{DD} >= 1.71 V
	Output low (10%) to high level (90%) rise time (Ultra-Fast Slew Rate)	-	2.38	nS	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.27		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3.01		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.59		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5.26		C_L = 30 pF, V_{DD} >= 1.71 V
		-	2.75		C_L = 10 pF, V_{DD} >= 1.71 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	41.72	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	61.05		C_L = 10 pF, V_{DD} >= 3.6 V
		-	34.83		C_L = 30 pF, V_{DD} >= 2.7 V
		-	50.43		C_L = 10 pF, V_{DD} >= 2.7 V
		-	23.52		C_L = 30 pF, V_{DD} >= 1.71 V
		-	33.57		C_L = 10 pF, V_{DD} >= 1.71 V
	I/O maximum frequency (High Slew Rate)	-	68.80	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	107.01-		C_L = 10 pF, V_{DD} >= 3.6 V
		-	57.62		C_L = 30 pF, V_{DD} >= 2.7 V
		-	90.09		C_L = 10 pF, V_{DD} >= 2.7 V
		-	36.83		C_L = 30 pF, V_{DD} >= 1.71 V

		-	59.63		C_L = 10 pF, V_{DD} >= 1.71 V
	I/O maximum frequency (Fast Slew Rate)	-	111.86	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	220.75		C_L = 10 pF, V_{DD} >= 3.0 V
		-	89.85		C_L = 30 pF, V_{DD} >= 2.7 V
		-	176.83		C_L = 10 pF, V_{DD} >= 2.7 V
		-	50.62		C_L = 30 pF, V_{DD} >= 1.71 V
		-	100.25		C_L = 10 pF, V_{DD} >= 1.71 V
	/O maximum frequency (Ultra-Fast Slew Rate)	-	138.31	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	266.67		C_L = 10 pF, V_{DD} >= 3.0 V
		-	111.11		C_L = 30 pF, V_{DD} >= 2.7 V
		-	215.05		C_L = 10 pF, V_{DD} >= 2.7 V
		-	62.77		C_L = 30 pF, V_{DD} >= 1.71 V
		-	122.55		C_L = 10 pF, V_{DD} >= 1.71 V
I_{DIO}[*4]	I/O dynamic current consumption	-	2.77	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		-	1.18		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		-	0.69		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		-	0.29		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Notes:

1. Guaranteed by design result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-12 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
V_{DD}	Power supply	1.71	-	3.6	V	
V_{LDO}	Output voltage	-	1.15	-	V	MCU @ PL0
V_{LDO}	Output voltage	-	1.1	-	V	MCU @ PL1

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a C_{LDO} capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.
3. V_{LDO} is only used to supply internal power.

Table 8.5-1 LDO characteristics

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
I_{POR}[1]	POR operating current	-	10	20	μA	V_{DD} = AV_{DD} = Max. OP
I_{LVR}[1]	LVR operating current	-	0.3	0.6		V_{DD} = AV_{DD} = Max. OP
I_{BOD}[1]	BOD operating current	-	10	15		V_{DD} = AV_{DD} = Max. OP, Normal mode
		-	1	1.5		V_{DD} = AV_{DD} = Max. OP Low Power mode
V_{POR}	POR reset voltage (Rising edge)	1.45	1.5	1.55	V	
	POR reset voltage (Falling edge)	1.4	1.45	1.5		
V_{LVR}	LVR reset voltage (Rising edge)	1.46	1.5	1.6		
	LVR reset voltage (Falling edge)	1.45	1.5	1.55		
V_{BOD}	BOD brown-out detect voltage (Rising edge)	1.56	1.68	1.8		BODVL = 0
		1.76	1.88	2		BODVL = 1
		1.96	2.08	2.2		BODVL = 2
		2.16	2.28	2.4		BODVL = 3
		2.36	2.48	2.6		BODVL = 4

		2.56	2.68	2.8		BODVL = 5
		2.76	2.88	3		BODVL = 6
		2.96	3.08	3.2		BODVL = 7
	BOD brown-out detect voltage (Falling edge)	1.5	1.6	1.7		BODVL = 0
		1.7	1.8	1.9		BODVL = 1
		1.9	2	2.1		BODVL = 2
		2.1	2.2	2.3		BODVL = 3
		2.3	2.4	2.5		BODVL = 4
		2.5	2.6	2.7		BODVL = 5
		2.7	2.8	2.9		BODVL = 6
		2.9	3	3.1		BODVL = 7
T_{LVR_SU}[1]	LVR startup time	-	-	400	µS	Normal mode
		-	-	2500		Low power mode
T_{LVR_RE}[1]	LVR respond time	-	20	50		LVRDGSEL = 0
T_{BOD_SU}[1]	BOD startup time	-	20	25		
		-	-	2500		
		-	13200	-		Low Power mode
T_{BOD_RE}[1]	BOD respond time	-	20	25		Normal mode BODDGSEL = 3
		-	-	13200		Low Power mode BODDGSEL = default value
R_{VDDR}[1]	V_{DD} rise time rate	10	-	-	µS/V	POR Enabled
R_{VDDF}[1]	V_{DD} fall time rate	10	-	-		POR Enabled
		500	-	-		LVR Enabled
		125	-	-		BOD 1.6V Enabled, Normal mode
		62.5	-	-		BOD 1.8V Enabled, Normal mode
		41.667	-	-		BOD 2.0V Enabled, Normal mode
		31.25	-	-		BOD 2.2V Enabled, Normal mode
		25	-	-		BOD 2.4V Enabled, Normal mode
		20.833	-	-		BOD 2.6V Enabled, Normal mode
		17.857	-	-		BOD 2.8V Enabled, Normal mode
		15.625	-	-		BOD 3.0V Enabled,

						Normal mode
		66000	-	-		BOD 1.6V Enabled, Low Power mode
		33000	-	-		BOD 1.8V Enabled, Low Power mode
		22000	-	-		BOD 2.0V Enabled, Low Power mode
		16500	-	-		BOD 2.2V Enabled, Low Power mode
		13200	-	-		BOD 2.4V Enabled, Low Power mode
		11000	-	-		BOD 2.6V Enabled, Low Power mode
		9428.6	-	-		BOD 2.8V Enabled, Low Power mode
		8250	-	-		BOD 3.0V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-2 Reset and Power Control Unit

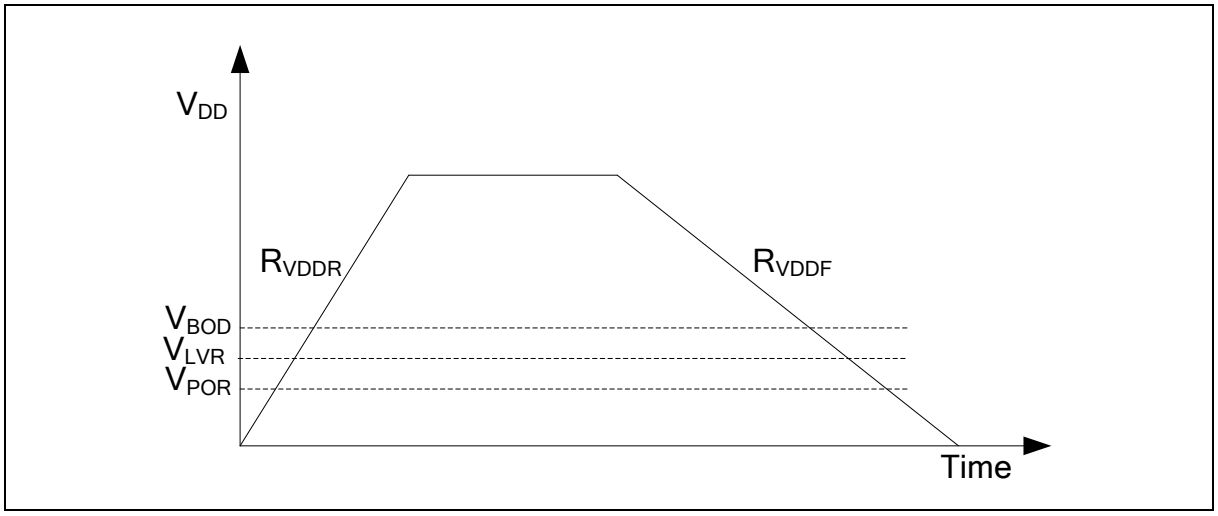


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.71	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.71	-	AV_{DD}	V	$AV_{DD} - V_{REF} < TBD$ V
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[1]	ADC Operating current ($AV_{DD} + V_{REF}$ current)	-	302		μA	$AV_{DD} = V_{DD} = V_{REF} = 3.3$ V F_{ADC} = Max. 90 MHz F_{SPS} = Max. 4286 * kSPS
		-	62		μA	$AV_{DD} = V_{DD} = V_{REF} = 3.3$ V F_{ADC} = Min. 12 MHz F_{SPS} = Min. 571 * kSPS
N_R	Resolution	12			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	12	-	90	MHz	
T_{SMP}[1]	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	20	-		$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 21 * T_{ADC}$
F_{SPS}[1]	Sampling Rate	571	-	4286	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}[1]	Enable to ready time	TBD	-	-	μS	
INL[1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
		-2	-	+2	LSB	$V_{REF} = AV_{DD}$
DNL[1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$,
		-1	-	+2	LSB	$V_{REF} = AV_{DD}$
E_G[1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
		-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_O[1]	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
		-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_A[1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
		-4	-	+4	LSB	$V_{REF} = AV_{DD}$
ENOB[1]	Effective number of bits	-	10	-	bits	F_{ADC} = Max. MHz $AV_{DD} = V_{DD} = V_{REF} = 3.3$ V Input Frequency = 20 kHz T_A = 25 °C
SINAD[1]	Signal-to-noise and distortion ratio	-	66.7	-	dB	
SNR[1]	Signal-to-noise ratio	-	66.7	-		
THD[1]	Total harmonic distortion	-	-69.7	-		
C_{IN}[2]	Internal Capacitance	-	3.1	-	pF	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{IN}[2]	Internal Switch Resistance	-	-	540	Ω	
R_{EX} [3][4]	External input impedance	-	-	0.72 [1]	kΩ	F_{ADC} = max. MHz T_{SMP} = max. * T_{ADC} C_{EX} = C_{IO} = 5 pF T_J = 25 °C

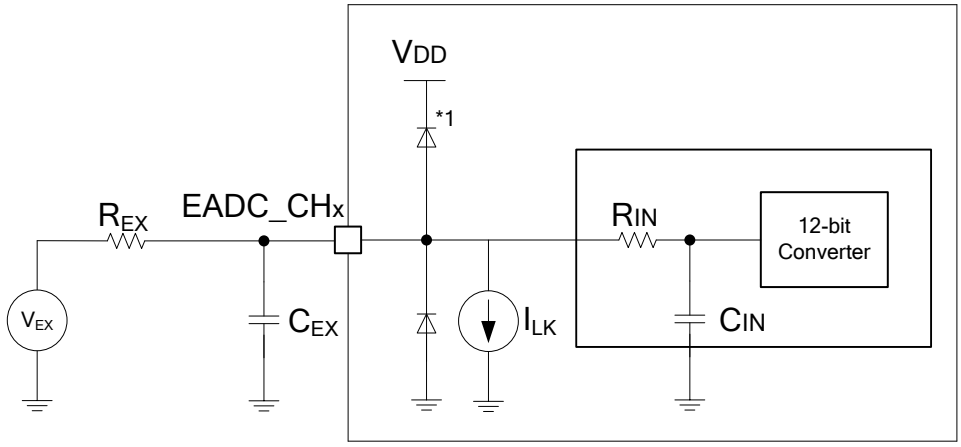
Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.
3. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

4. The signal voltage is affected by IO leakage. When ADC is running at T_J = 125 °C, the R_{EX} should be lower to decrease IR voltage drop effect.

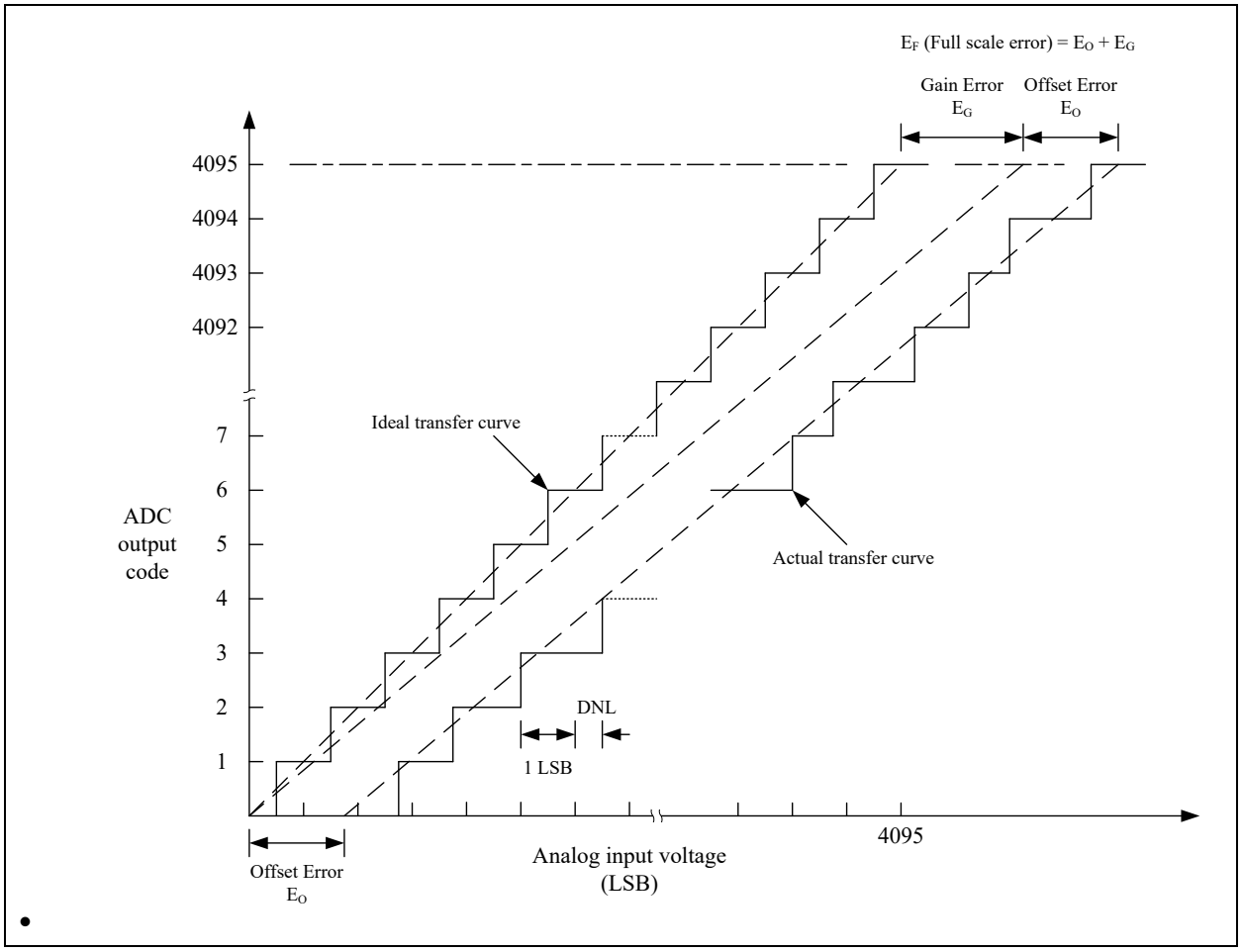
Table 8.5-3 ADC Characteristics



Notes:

1. The internal ESD diode doesn't be supported between IO and V_{DD} at 5V tolerence IO pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Digital to Analog Converter (DAC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	
N_R	Resolution		12		bit	
V_{REF}	Reference supply voltage	1.6	-	AV_{DD}	V	
DNL[2]	Differential non-linearity error	-	-	±2	LSB	12-bit mode
INL[2]	Integral non-linearity error	-	-	±4	LSB	12-bit mode
OE[2]	Offset Error	-	-	±6	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
GE[2]	Gain Error	-	-	±6	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
AE[2]	Absolute Error	-	-	±8	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
-	Monotonic		10-bit guaranteed		-	-
V_O[1]	Output Voltage	0.2	-	AV_{DD} - 0.2	V	DACOUT buffer ON
		1*LSB	-	V_{REF} - 1*LSB	V	DACOUT buffer OFF
R_{LOAD}[2] [3]	Resistive load	7.5	-	-	kΩ	DACOUT buffer ON
R_O[2]	Output impedance	-	10	20	kΩ	DACOUT buffer OFF
C_{LOAD}[2] [4]	Capacitive load	-	-	50	pF	DACOUT buffer ON
		-	-	20	pF	DACOUT buffer OFF
I_{DAC_AVDD}[2]	DAC operating current on AV_{DD} supply	-	50	90	μA	AV_{DD} = 3.3 V, no load, lowest code (0x000)
			320	405		AV_{DD} = 3.3 V, no load, middle code (0x800)
			490	555		AV_{DD} = 3.3 V, R_{LOAD} = 7.5kΩ, highest code (0xFFF)

I_{DAC_VREF}[2]	DAC operating current on V_{REF} supply	-	170	240	μA	V_{REF} = 3.3 V, no load, middle code (0x800)
T_B[2]	Settling Time	-	5	6	μS	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$
F_S	Update Rate	-	-	1000	kSPS	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 7.5k\Omega$
PSRR[1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

Table 8.5-4 DAC Characteristics

8.5.5 Analog Comparator (ACMP)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
AV_{DD}	Analog supply voltage	1.71	-	3.6	V	$V_{DD} = AV_{DD}$
I_{ACMP}[2]	ACMP operating current	-	70	-	μA	MODESEL = 11
		-	35	-		MODESEL = 10
		-	2	-		MODESEL = 01
		-	1	-		MODESEL = 00
V_{CM}[2]	Input common mode voltage range	0		AV_{DD}	V	
V_{DI}[*2]	Differential input voltage sensitivity	20	-	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[2]	Input offset voltage	-	±5	±10	mV	MODESEL =11 Hysteresis disable (HYSSEL = 00)
		-	±10	±20		MODESEL =00~10 Hysteresis disable (HYSSEL = 00)
V_{hys}[2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	60		HYSSEL = 100, MODESEL =10~11
				80		HYSSEL = 100, MODESEL =00~01
A_v[1]	DC voltage Gain	51	70	-	dB	
T_d[2]	Propagation delay	-	30	60	nS	MODESEL = 11, AV_{DD}≥1.8V
				90		MODESEL = 11, AV_{DD}≥1.6V
		-	100	150		MODESEL = 10
		-	0.8	2	μS	MODESEL = 01
		-	1.5	3.5		MODESEL = 00
T_{Setup}[2]	Setup time	-	-	1	μS	MODESEL = 10~11
		-	-	20		MODESEL = 00~01
A_{CRV}[2]	CRV output voltage absolute accuracy	-1	-	1	LSB	AV_{DD} x (CRV_SEL[5:0]/63)
T_{SETUP_CRV}[2]	Setup time	-	-	0.6	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[2]	Operating current	-	30	50	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-5 ACMP Characteristics

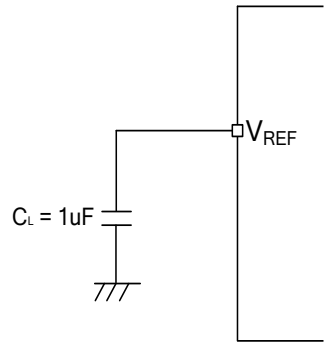
8.5.6 Internal Voltage Reference

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{REF_INT}	Internal reference voltage	1.576	1.6	1.624	V	AV_{DD} >= 2.0 V
		2.017	2.048	2.079		AV_{DD} >= 2.2 V
		2.463	2.5	2.538		AV_{DD} >= 2.7 V
		3.026	3.072	3.118		AV_{DD} >= 3.2 V
T_s[1]	Stable time	-	-	2	mS	C_L = 4.7 uF, V_{REF} initial=0V, Preload=2'b01 is enabled.
		-	-	480	uS	C_L = 1 uF, V_{REF} initial=0V, Preload=2'b00 is enabled.
I_{VREF_INT}[1]	V_{REF_INT} operating current	-	70	-	uA	
I_{VREF_LOAD}[1]	V_{REF_INT} output loading current	-	-	1.5	mA	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.5-6 Internal V_{REF} Characteristics



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.7 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
V_{TEMP_OS}[1]	Temperature sensor offset voltage	935	1010	1105	mV	T_A = 25°C
T_C[1]	Temperature Coefficient	-2.5	-2.7	-3.02	mV/°C	
T_S[2]	Stable time	-	-	5	µS	
T_{TEMP_ADC}[1]	ADC sampling time when reading the temperature	15	-	-	µS	
I_{TEMP}[1]	Temperature sensor operating current	-	5	10	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Table 8.5-7 Temperture Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	100	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2.4	-	-	nS	
t_V	Data output valid time	-	-	1.0	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-1 SPI Master Mode Characteristics

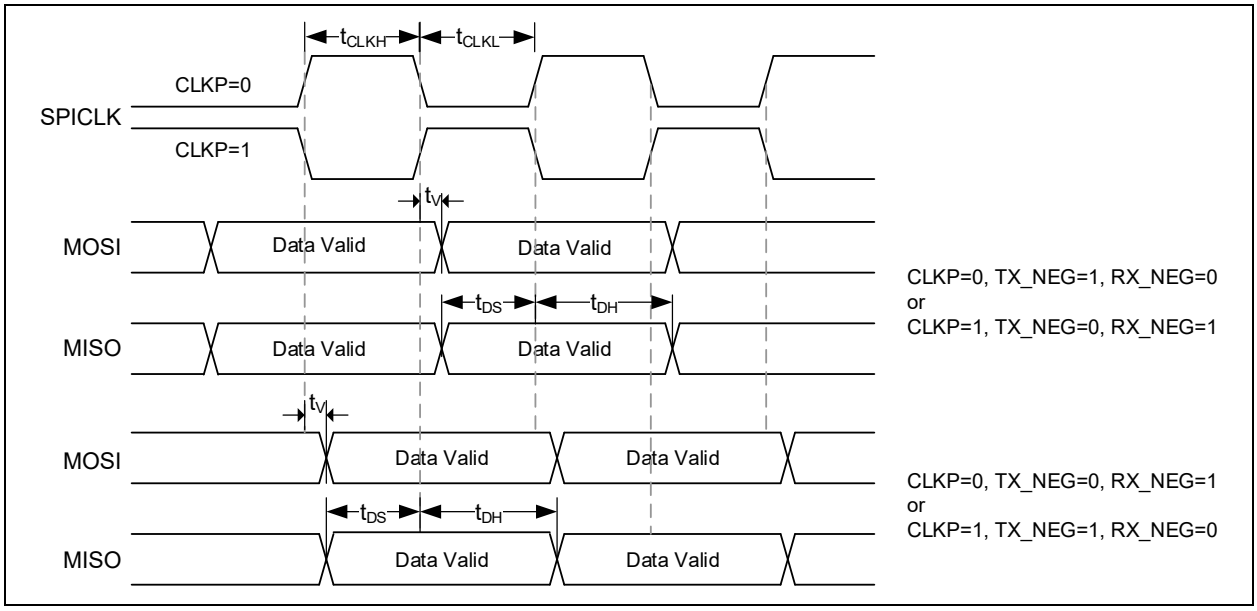


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	50	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	12	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-2 SPI Slave Mode Characteristics

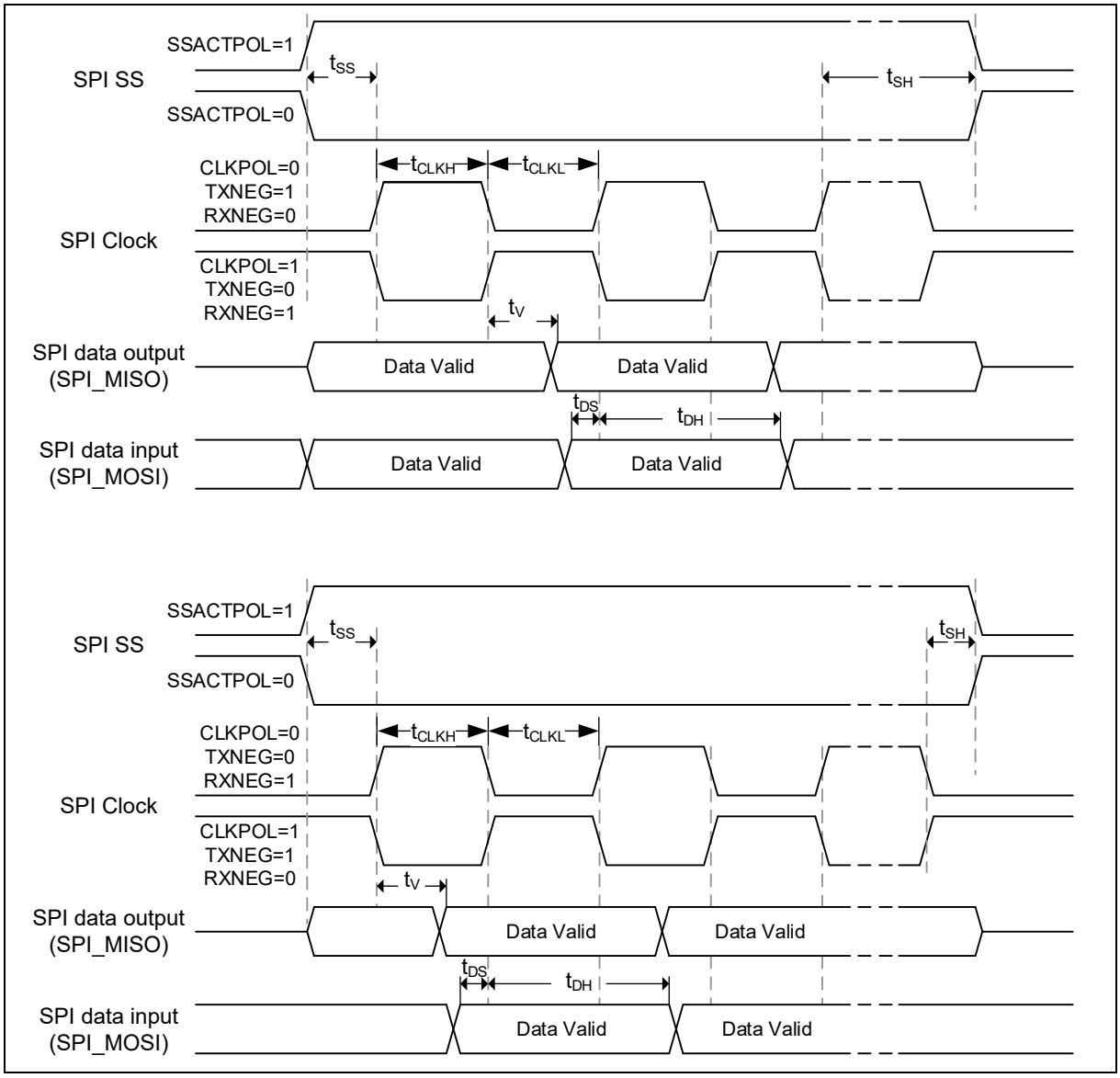


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [1]	Max [1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	nS	Master f_{PCLK} = 100 MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	2	5		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	6	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	40	60	%	Slave mode
$t_{su(SD_MR)}$	Data input setup time	6	-	nS	Master receiver
$t_{su(SD_SR)}$		5	-		Slave receiver
$t_{h(SD_MR)}$	Data input hold time	6	-		Master receiver
$t_{h(SD_SR)}$		3	-		Slave receiver
$t_{v(SD_ST)}$	Data output valid time	-	14		Slave transmitter (after enable edge)
$t_{h(SD_ST)}$	Data output hold time	2	-		Slave transmitter (after enable edge)
$t_{v(SD_MT)}$	Data output valid time	-	2		Master transmitter (after enable edge)
$t_{h(SD_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-3 I²S Characteristics

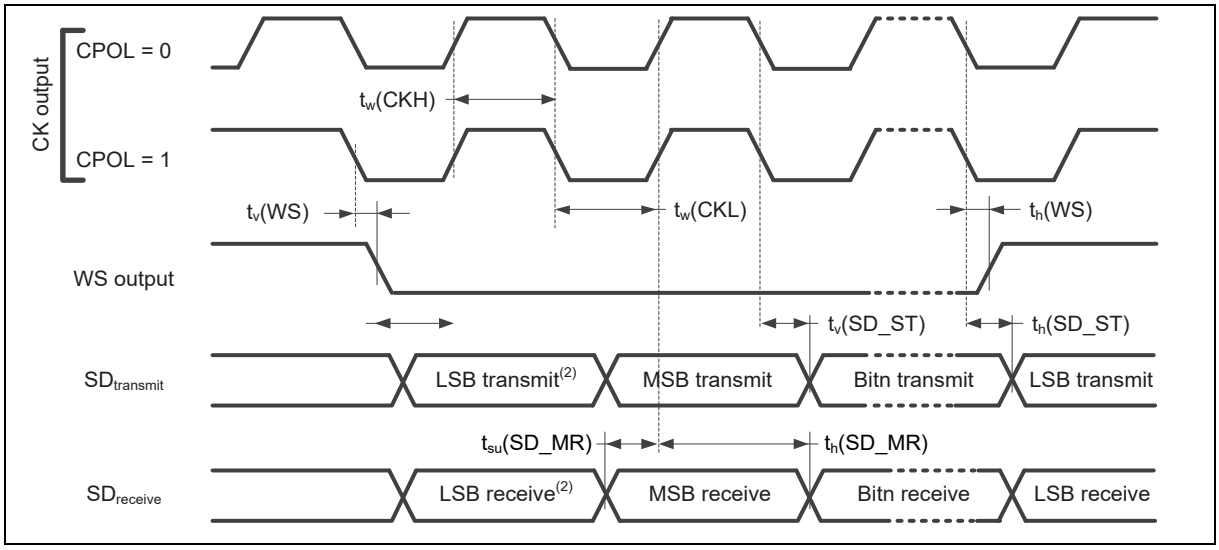


Figure 8.6-3 I²S Master Mode Timing Diagram

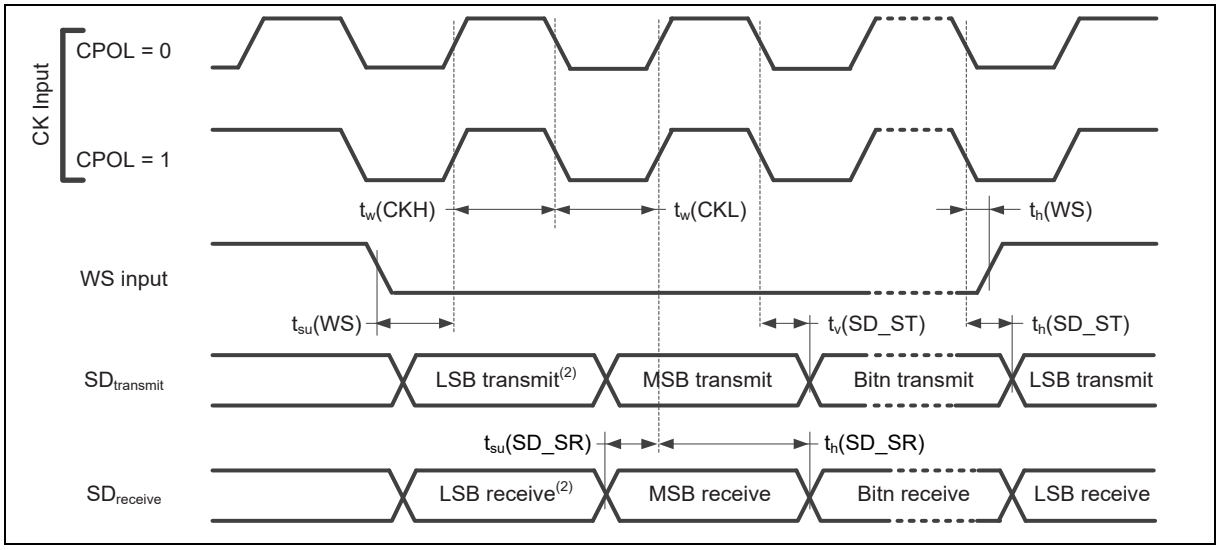


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 SPIM Dynamic Characteristics for HYPER device mode

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
$F_{HYPERCLK}$ = 1/ $T_{HYPERCLK}$	SPIM clock frequency	-	-	110	MHz	Test with HyperRAM, 1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF 2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF
		-	-	100	MHz	Test with HyperFlash, 1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF 2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF
t_{CLKH}	Clock output High time	$T_{HYPERCLK}$ / 2			nS	
t_{CLKL}	Clock output Low time	$T_{HYPERCLK}$ / 2			nS	
t_{CSS}	Chip select setup to next CK rising edge	16.4	-	-	nS	SPIM HCLK frequency = 220MHz
t_{CSH}	Chip select hold after CK falling edge	11.3	-	-	nS	SPIM HCLK frequency = 220MHz
T_{CSHI}	Chip select HIGH between transaction	18	-	-	nS	SPIM HCLK frequency = 220MHz
t_{CKD}	Clock transition to Data valid	-	-	$T_{HYPERCLK}$ / 4	nS	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF 2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF
t_{CKDS}	Clock transition to RWDS valid	-	-	1	nS	
t_{DSS}	RWDS transition to input Data valid	-1	-	1	nS	
t_{DSH}	Input Data invalid to RWDS transition	-1	-	1	nS	

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-4 SPIM Characteristics for HYPER device mode

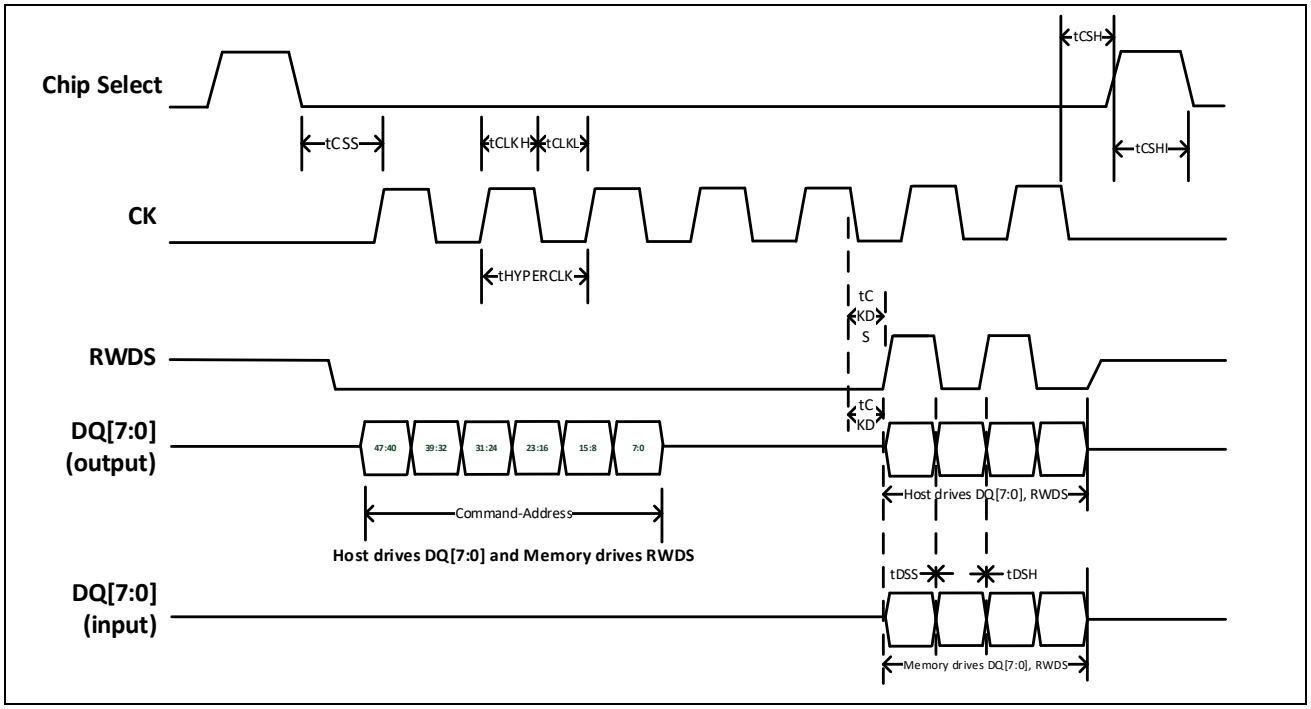


Figure 8.6-5 SPIM Timing Diagram for HYPER device mode

8.6.4 SPIM Dynamic Characteristics for Octal SPI Flash device mode

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPIM clock frequency	-	-	100	MHz	Test with Octal SPI Flash, 1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF 2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	1.8	nS	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF
				1.7	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 20 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-5 SPIM Characteristics for Octal SPI Flash device mode

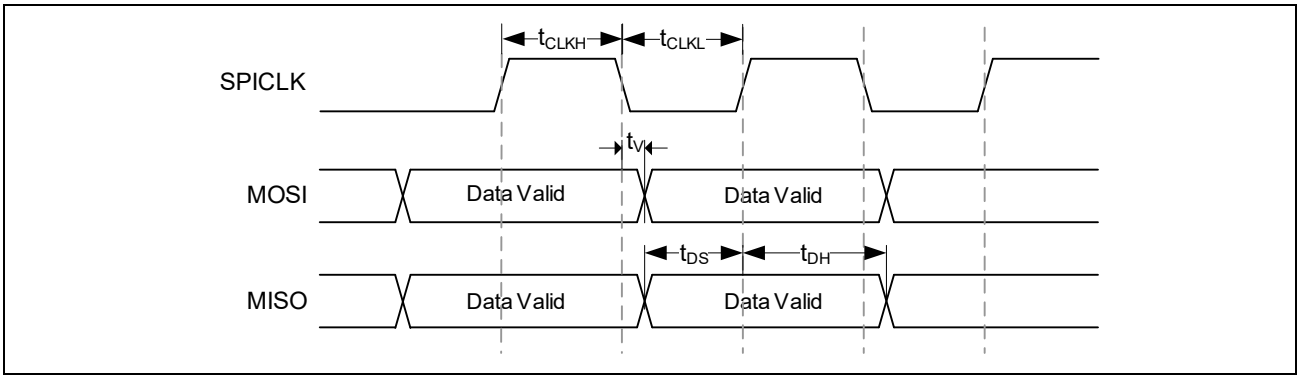


Figure 8.6-6 SPIM Timing Diagram for Octal SPI Flash device mode

8.6.5 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-6 I²C Characteristics

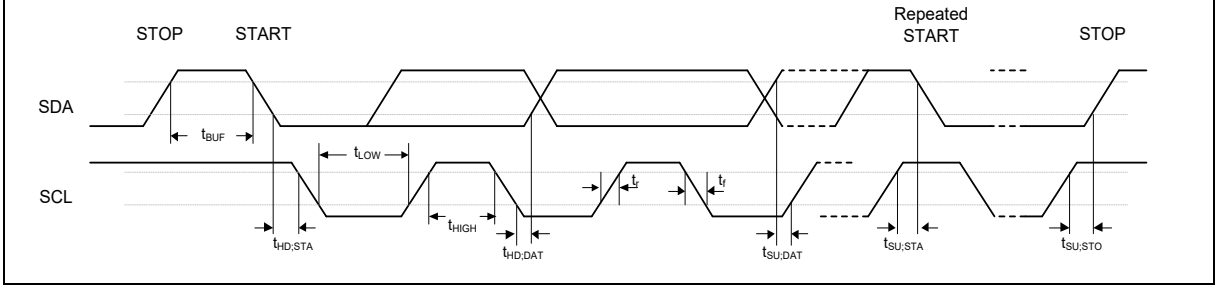


Figure 8.6-7 I²C Timing Diagram

8.6.6 I3C Dynamic Characteristics

Symbol	Parameter		I²C Mode		I3C Mode				Unit
			Open Drain		Open Drain		Push-Pull		
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock frequency		0.01	1	-	-	0.01	12.5	MHz
t_{LOW}	SCL Clock Low Period		500	-	-	-	32	-	nS
t_{HIGH}	SCL Clock High Period		260	-	-	-	32	-	nS
t_{cr}	SCL Clock Rise Time		-	120	-	-	-	12	nS
t_{cf}	SCL Clock Fall Time		-	120	-	-	-	12	nS
t_{SU_DAT}	Data setup time		50	-	3	-	3	-	nS
t_{HD_DAT}	Data hold time	Master	-	-	-	-	15	-	nS
		Slave	-	-	-	-	0	-	
t_{SCO}	Clock in to Data Out for Slave		-	-	-	-	-	12	nS
t_{CAS}	Clock After START(S) Condition		260n	-	34.8n	ENTAS0: 1 µ ENTAS1: 100 µ ENTAS2: 2 m ENTAS3: 50 m	19.2n	-	S
t_{CBP}	Clock Before STOP(P) Condition		260n	-	19.2n	-	19.2n	-	S
t_{CBSr}	Clock Before Repeated START (Sr) Condition		-	-	-	-	19.2	-	nS
t_{BUF}	Time between Stop Condition and next Start Condition		500	-	500	-	-	-	nS
t_{AVAIL}	Bus Available Condition		-	-	1	-	-	-	µS
t_{IDLE}	Bus Idle Condition		-	-	200	-	-	-	µS

Notes:

1. Guaranteed by characteristic, not tested in production.
2. I3C clock source must be greater than 125 MHz to achieve the maximum SCL Clock frequency.
3. Slave that do not support the optional ENTASx CCCs shall use the tCAS Max value *shown for ENTAS3*

Table 8.6-7 I3C Characteristics

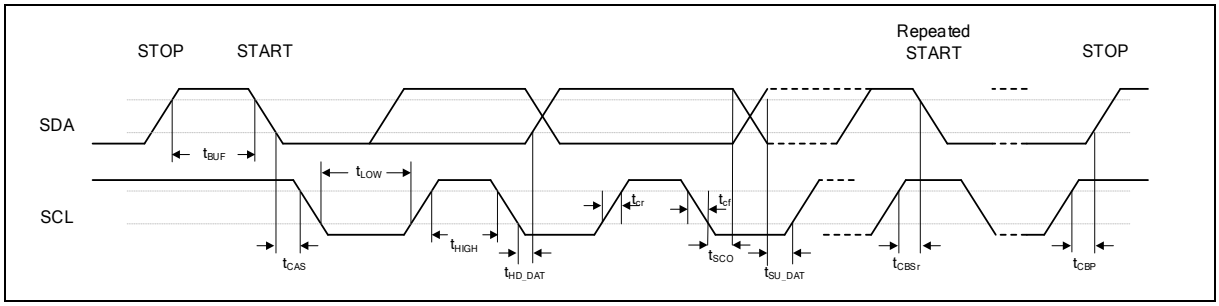


Figure 8.6-8 I3C Timing Diagram

8.6.7 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [1]	Typ	Max[1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	f_{PCLK} / 2	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	1	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-8 USCI-SPI Master Mode Characteristics

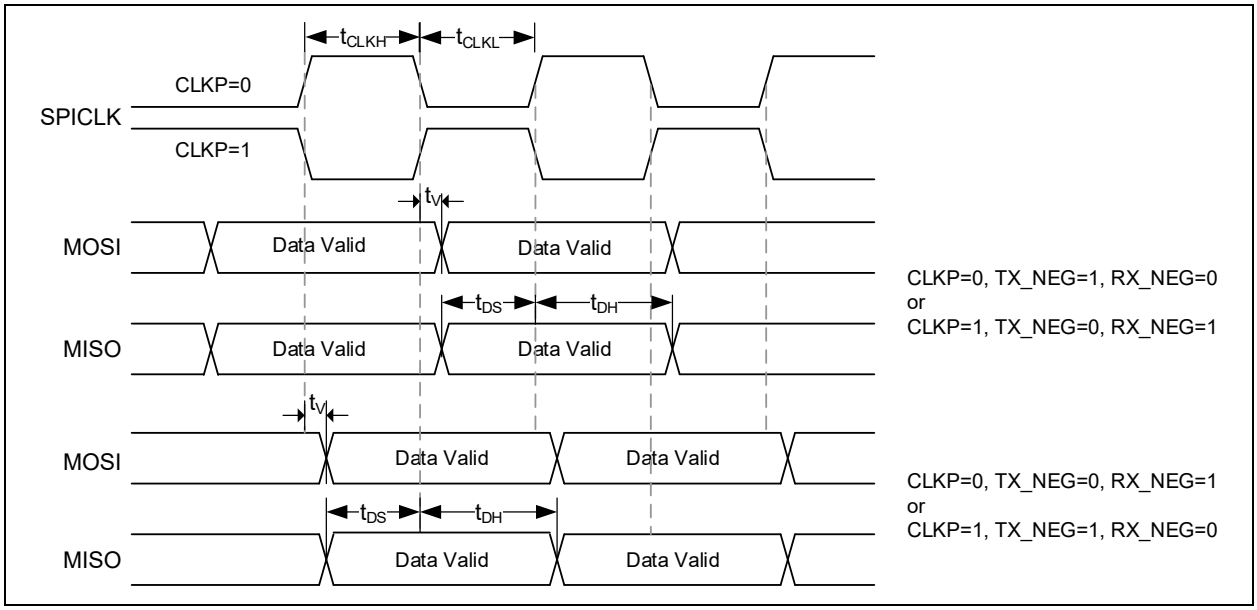


Figure 8.6-9 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	12.7	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	46.5	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-9 USCI-SPI Slave Mode Characteristics

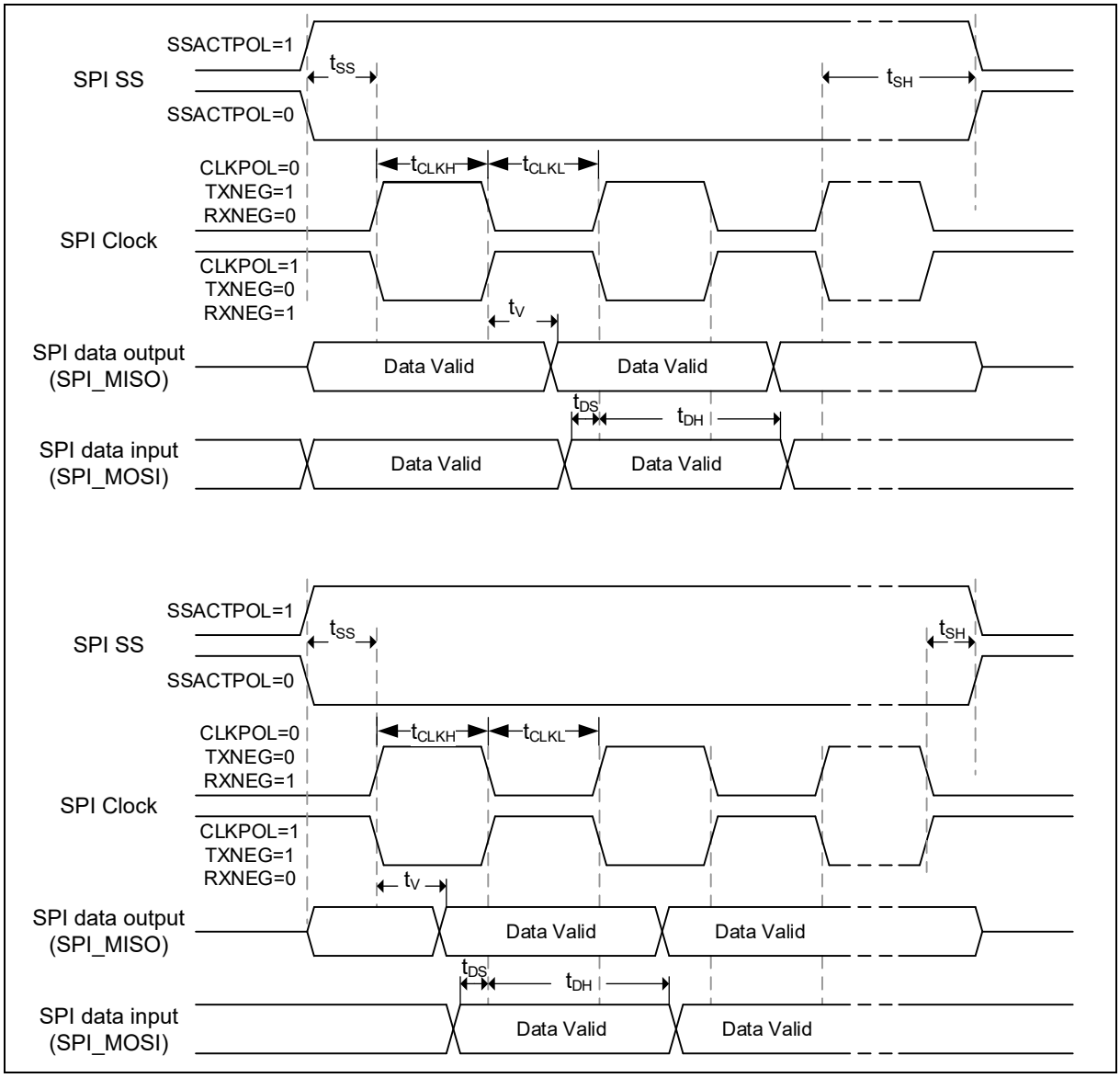


Figure 8.6-10 USCI-SPI Slave Mode Timing Diagram

8.6.8 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1Cb	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-10 USCI-I²C Characteristics

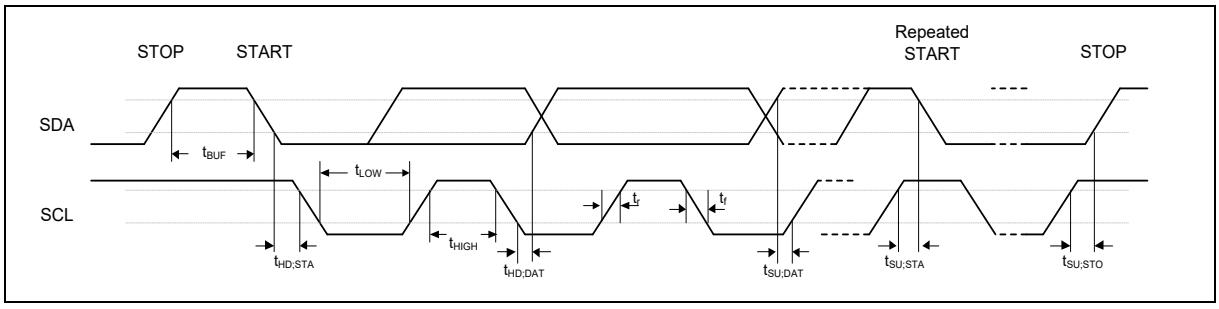


Figure 8.6-11 USCI-I²C Timing Diagram

8.6.9 CAN Characteristics

Symbol	Parameter	Min	Max [1]	Unit	Test Conditions
t_{CAN_TXD}	TXD output delay (Normal Slew Rate)	-	23	nS	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CAN_RXD}	RXD input delay	-	12	nS	2.7 V ≤ V_{DD} ≤ 3.6 V

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-11 CAN Characteristics

8.6.10 USB Characteristics

8.6.10.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
V_{DD}	Operation voltage	3.0	3.3	3.6	V	
V_{BUS}	USB full speed transceiver operating voltage USB V_{BUS} voltage detection voltage	0	-	V_{DD}	V	
V_{IH}	Input high (driven)	2	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	0.4	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2	V	-
R_{PU}	Pull-up resistor	0.9	1.2	1.575	kΩ	-
R_{PD}	Pull-down resistor	14.25	19.5	24.8	kΩ	
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3	-	3.6	V	
Z_{DRV}[3]	Driver output resistance	10.9	-	25.1	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Notes:

1. Guaranteed by characterization result, not tested in production.
2. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 43 Ω).

Table 8.6-12 USB Full-Speed Characteristics

8.6.10.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	nS	C_L=50 pF
T_{FF}	fall time	4	-	20	nS	C_L=50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-13 USB Full-Speed PHY Characteristics

8.6.11 UTCPD Characteristics

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
V_{DD}	UTCPD Operation voltage	3.0	3.3	3.6	V	
V_{BUS}[2]	USB V_{BUS} voltage detection voltage	0.4	-	V_{DD}	V	VBSCALE = 0x0
		0.2	-	V_{DD}	V	VBSCALE = 0x1
V_{OH_CC}	CC output high voltage	1.05	1.125	1.2	V	
V_{OL_CC}	CC output low voltage	-0.075	-	0.075	V	
$t_{f(CC)}$ / $t_{r(CC)}$	CC rising time and falling time. 10% and 90% amplitude points, minimum is under unloaded condition.	300	-	-	nS	
I_{CC_DEF}	Source current for default USB power when acting as DFP	64	80	96	µA	
$I_{CC_1.5A}$	Source current for 1.5A power when acting as DFP	165.6	180	194.4	µA	
I_{CC_3A}	Source current for 3A USB power when acting as DFP	303.6	330	356.4	µA	
Rd	Pull down CC termination resistance when acting as UFP	4.59	5.1	5.61	kΩ	
Rd_db[3]	Pull down CC termination resistance when acting as UFP with dead battery	-	4.5	-	kΩ	All supplies forced to 0V and 1V applied at CC and DB_CC pin.
Rd_ccdb[3]	Pull down CCDB resistance to keep CCDB1 and CCDB2 as low level.	0.75	-	1.25	MΩ	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. When PA.12 (VBUS) OFFDIG is set to 1, the UTCPD will see V_{BUS} voltage. In this condition, V_{BUS} should be divided and make sure no larger than V_{DD} all the time
3. The GPIO characteristics of CC and CCDB pin are affected by Rd_db and Rd_ccdb respectively.

Table 8.6-14 UTCPD Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[2]	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	14.5	-	mS	T_A = 25℃
T_{PROG}	Program time	-	44	-	μS	
I_{DD1}	Read current	-	3.1	-	mA	
I_{DD2}	Program current	-	6.5	-	mA	
I_{DD3}	Erase current	-	4.5	-	mA	
N_{ENDUR}	Cycling Endurance	10,000	-	-	cycles[1]	T_J = -40℃~125℃ or T_A = 25℃
T_{RET}	Data retention	10	-	-	year	TBD kcycle[1], T_J = 125℃
		10	-	-	year	TBD kcycle[1], T_J = 105℃
		10	-	-	year	TBD kcycle[1], T_J = 85℃
		10	-	-	year	TBD kcycle[1], T_J = 25℃

Notes:

1. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
2. Guaranteed by design, not tested in production.
3. The Erase/program command are only supported at power level 0/1/2

Table 8.7-1 Flash DC Electrical Characteristics

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
CCAP	Camera Capture Interface
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop

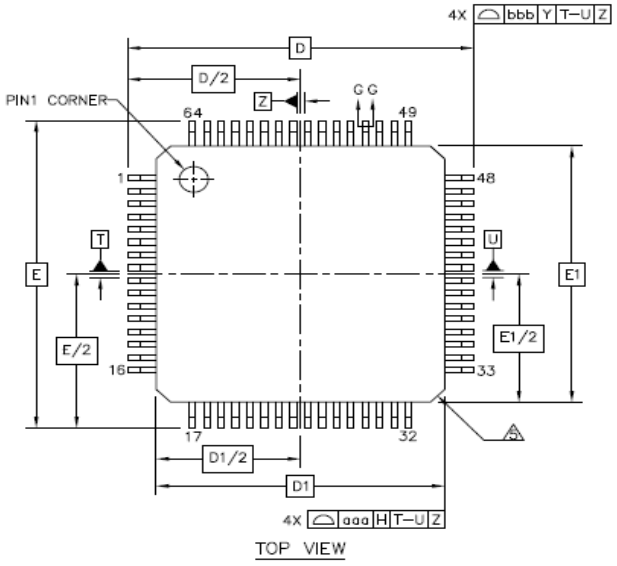
PWM	Pulse Width Modulation
EQEI	Enhanced Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

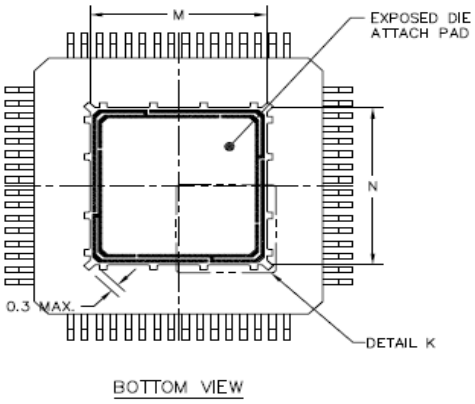
Table 9.1-1 List of Abbreviations

10 PACKAGE DIMENSIONS

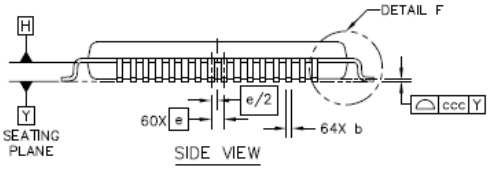
Package is Halogen-free, RoHS-compliant and TSCA-compliant.

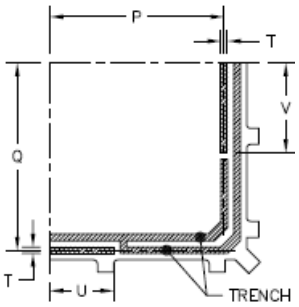
10.1 LQFP64L 10x10mm , Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm, EP_SIZE 6.14x6.14mm



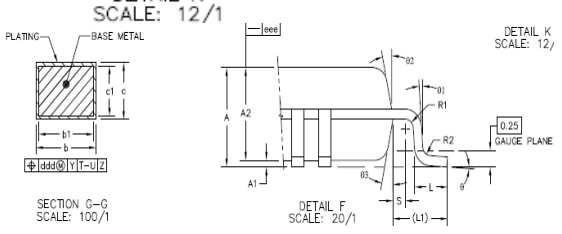


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	12 BSC		
	Y	E	12 BSC		
	X	D1	10 BSC		
	Y	E1	10 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	6.04	6.14	6.24
	Y	N	6.04	6.14	6.24
		P	2.67	2.72	2.77
		Q	2.87	2.92	2.97
		T	0.05	---	0.15
		U	0.95	---	1.05
		V	1.35	---	1.45
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

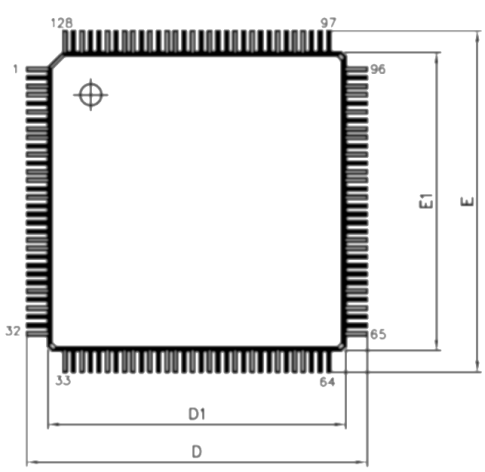


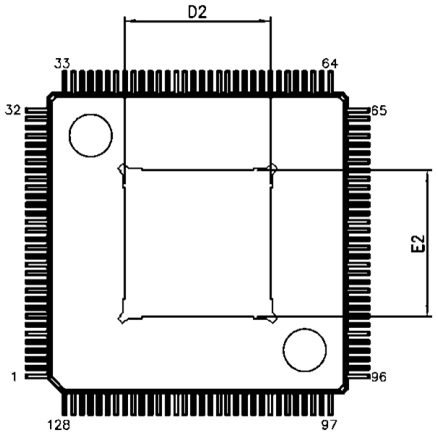


DETAIL K
SCALE: 12/1

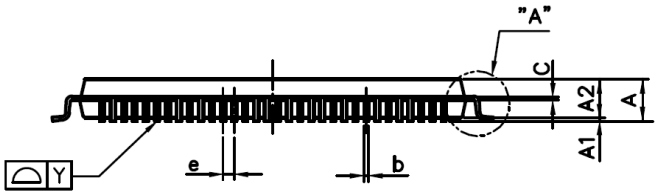


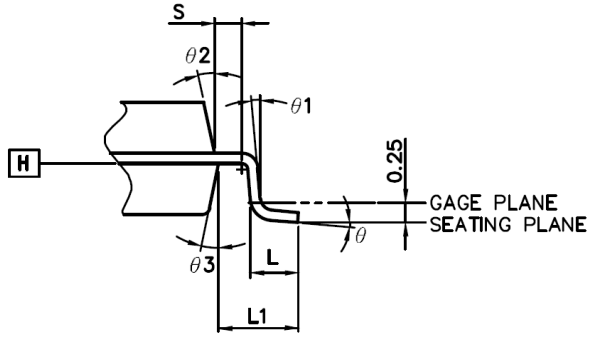
10.2 LQFP128L 14x14mm, Thickness 1.40mm, Lead_Pitch 0.40mm, Lead_Length 1.00mm, EP_SIZE 7.15x7.15mm





27*X27* MIL





DETAIL A

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.13	--	0.23
c	0.09	--	0.20
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
e	0.40 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°
S	0.20	--	--
Y	0.08		

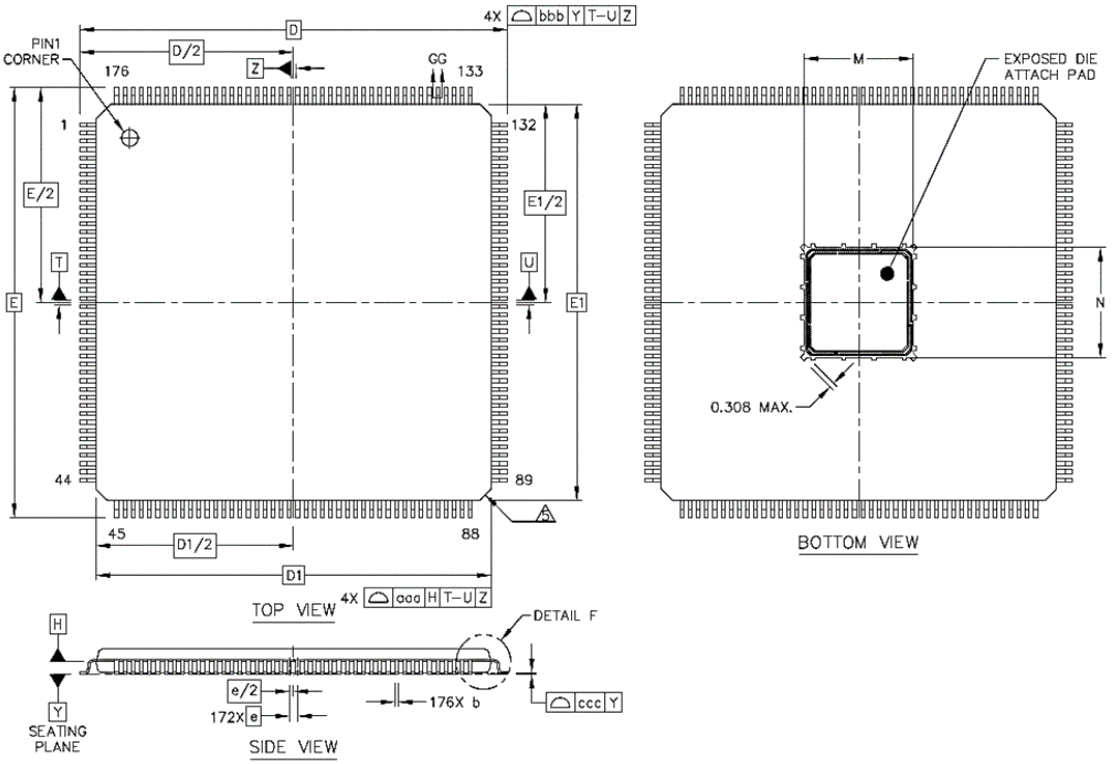
THERMALLY ENHANCED DIMENSIONS(SHOWN IN MM)

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
27*X27* MIL	6.70	7.00	7.15	6.70	7.00	7.15

"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

NOTES:
1. JEDEC NO. : N/A.
2. DATUM PLANE [H] IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE [H].
4. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.

10.3 LQFP176L 24x24mm , Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm, EP_SIZE 6.75x6.75mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	26 BSC		
	Y	E	26 BSC		
	X	D1	24 BSC		
	Y	E1	24 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
EP SIZE	X	M	6.55	6.65	6.75
	Y	N	6.55	6.65	6.75
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

NOTES

1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLDPROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUMb DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

5 EXACT SHAPE OF EACH CORNER IS OPTIONAL.

11 REVISION HISTORY

Date	Revision	Description
2025.09.08	1.00	• Initial version.
2026.08.20	1.01	• Modified chapter 10.1 LQFP64 package EP_SIZE 6.14x6.14mm. • Added the note “It is recommended to connect HSUSB_VDD11 to the LDO_CAP pin, as HSUSB_VDD11 requires a 1.1 V power supply.” in section 7.2.

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