NuMicro® Family

Arm® Cortex®-M4-based Microcontroller

M433 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro® M433 series is a 32-bit microcontroller based on Arm Cortex®-M4F core, with DSP instruction set and single-precision floating-point unit (FPU), targeted for IoT, Industrial, and consumer applications. The M433 series operating frequency is up to 144 MHz and the standby current can be lower to 1 µA. It features 1.7 V to 3.6 V wide operating voltage, -40 °C to 105°C wide operating temperature, a variety of packages choice.

The M433 series provides up to 128 KB Flash memory for code storage and 64 KB SRAM for run time operation. In order to reduce the data access overhead of CPU core to peripherals, 9 channels of peripheral direct memory access (PDMA) is provided.

The M433 series supports plenty of peripherals, including, USB FS OTG, up to 18 channels of 16-bit PWM, 3 sets of UART, 2 sets of SPI/I²S, 1 set of Quad-SPI and 2 sets of I²C.

The M433 series also provides rich analog peripherals including 2 sets of analog comparators, up to 16 channels of 12-bit SAR ADC.

For the development, Nuvoton provides the evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclippse IDE with GNU GCC compilers are also supported.

This series supports five package choices which are designed for home appliance PCB demands.

- LQFP48: Body Size 7 mm x 7 mm, Load Pitch 0.5 mm
- LQFP64: Body Size 7 mm x 7 mm, Load Pitch 0.4 mm

The NuMicro® M433 series is suitable for a wide range of applications such as:

- IoT Gateway
- Industrial Control
- Telecom
- Data Center

2 FEATURES

Core and System	
ARM Cortex-M4	• Arm Cortex-M4 processor, running up to 144 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Boot Loader	• Factory pre-loaded mask ROM for secure boot procedure
Flash	• Up to 128 Kbytes on-chip Application ROM (APROM) • Embedded with 4 Kbytes cache, with performance at zero wait cycle in continuous address read access • 4 Kbytes on-chip Flash for user-defined loader (LDROM) • All on-chip Flash support 4 Kbytes page erase • Fast Flash programming verification with CRC32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 64 Kbytes on-chip SRAM includes: – 32 Kbytes SRAM located in bank 0 with programmable size of SPD retention The first 32 Kbytes supports hardware parity

	check; Exception (NMI) generated upon a parity check error – 32 Kbytes SRAM located in bank 1 with SPD retention • Supports byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports 8-bits, 16-bits and 32-bits configurable polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials included • Programmable initial value • Supports order reverse setting and one's complement setting for input data and CRC checksum • Supports 8-bit, 16-bit, and 32-bit data width • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Up to 9 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Supports Fixed-priority and Round-robin priority modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC48) for crystal-less USB • 12 MHz High-speed Internal RC oscillator (HIRC) can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 400 MHz on-chip PLL, sourced from HIRC or HXT, allowing CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal • Programmable Audio PLL (PLLFN), sourced from HIRC or HXT
Real-Time Clock (RTC)	• Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt

	• Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Six 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Trigger EADC to start conversion immediately • Trigger EADC to start conversion after a short delay • Supports External Pin Trigger Function
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function

	• Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• One sets of 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Two internal channels band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin • Supports Power-down mode • Supports calibration capability • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse or EPWM/BPWM • Configurable EADC sampling time • Up to 18 sample modules • Double data buffers for sample module 0~3 • PDMA operation • Supports Averageing mode and Oversampling mode, where Oversampling mode provides up to 16-bit precision • Supports early interrupt with delay counter feature
Analog Comparator (ACMP)	• Up to two rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports four programmable power modes for power saving • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for

	PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 20mV and 40mV • Supports offset calibration
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 10 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports PDMA operation • Supports Single-wire function mode • Supports TX and RX swap function mode
I^2C	• Up to Two sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) and High speed mode (Up to 3.4Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation • Supports pin swap function • Supports setup/hold time programmable • Supports two level buffer mode
Quad SPI	• Up to one sets of Quad SPI with Master/Slave mode

	• Master mode up to 72 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 36 MHz (V_{DD} = 2.7V ~ 3.6V) • Supports Dual and Quad I/O Transfer mode • Supports one data channel half-duplex transfer • Supports double data rate mode (Master TX DIR Mode Only) • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation
SPI/I²S	• Up to 2 sets of SPI/I²S controllers with Master/Slave mode • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Master mode up to 72 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 36 MHz (V_{DD} = 2.7V ~ 3.6V) • Configurable bit length of a transfer word from 4 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O • Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode

Control Interfaces	
Enhanced Quadrature Encoder Interface (EQEI)	• One EQEI phase inputs (EQEI_A, EQEI_B) and one Index input (EQEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP • Supports swap function for input signals (EQEI_A, EQEI_B) • Supports for detecting the occurrence of phase error • Supports one times index signal reset function
Enhanced Capture (ECAP)	• One sets of Enhanced input Capture units • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver. • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only or ID-dependent **USB 2.0 Full Speed Host Controller** • Compliant with USB Revision 1.1 Specification. • Compatible with OHCI (Open Host Controller Interface) Revision 1.0. • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices. • Supports Control, Bulk, Interrupt, Isochronous and Split transfers. • Integrated a port routing logic to route full/low speed device to OHCI controller. • Supports an integrated Root Hub. • Supports port power control and port over current detection. • Built-in DMA. **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification. • Supports suspend function when no bus activity existing for 3 ms. • 12 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types. • 1024 bytes configurable RAM for endpoint buffer.

	• Remote wake-up capability. • Supports crystall-less features
Controller Area Network (CAN)	• Up to two sets of CAN 2.0B controllers. • Each supports 32 Message Objects; each Message Object has its own identifier mask. • Programmable FIFO mode (concatenation of Message Object). • Disabled Automatic Re-transmission mode for Time Triggered CAN applications. • Supports power-down wake-up function.

3 PARTS INFORMATION

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1 Package Type

Part No.	LQFP48 (7x7mm)	LQFP64 (7x7mm)
M433	M433LE8AE	M433SE8AE

3.2 M433 Series Naming Rule

M4	33	S	E	8	A	E
Core	Series	Package	Flash Size	SRAM Size	Revision	Temperature
Cortex-M4F	33: Based Series	L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm)	E: 128 Kbytes	8: 64 Kbytes	A	E:-40˚C ~ 105˚C

3.3 M433 Series Selection Guide

3.3.1 M433 Series

PART NUMBER		M433LE8AE	M433SE8AE
System Frequency (MHz)		144	
Flash (KB)		128	
SRAM (KB)		64	
LDROM (KB)		4	
PDMA		9-ch	
I/O		41	52
32-bit Timer		4	
16-bit EPWM		6	
16-bit BPWM		12	
Connectivity	UART	4	
	QSPI	1	
	SPI/I²S	2	
	I²C	2	
	CAN	2	
USB Full Speed OTG with PHY		√	
EQEI		1	
ECAP		1	
12-bit ADC		16	
Analog Comparator		2	
Operating Temperature		-40˚C ~ 105˚C	
Package		LQFP 48 (7x7mm)	LQFP 64 (7x7mm)

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in chapter 4 or by using NuTool - PinConfig. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 LQFP-48 Pin Diagram

Corresponding Part Number: M433LE8AE

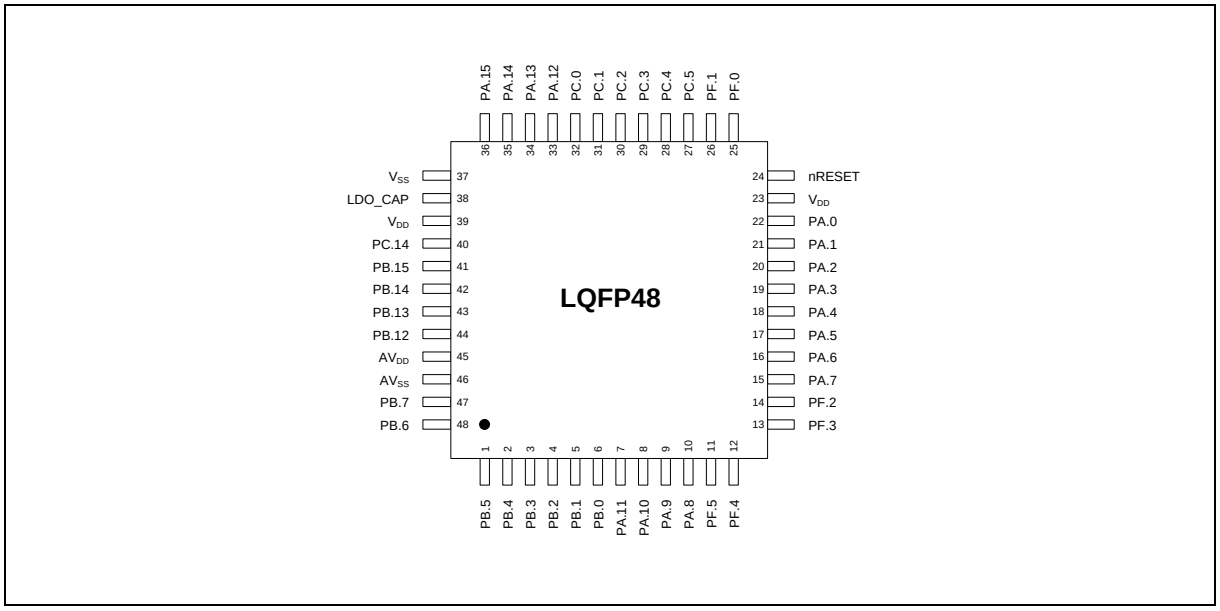


Figure 4.1-1 LQFP-48 Pin Diagram

4.1.2 LQFP-64 Pin Diagram

Corresponding Part Number: M433SE8AE

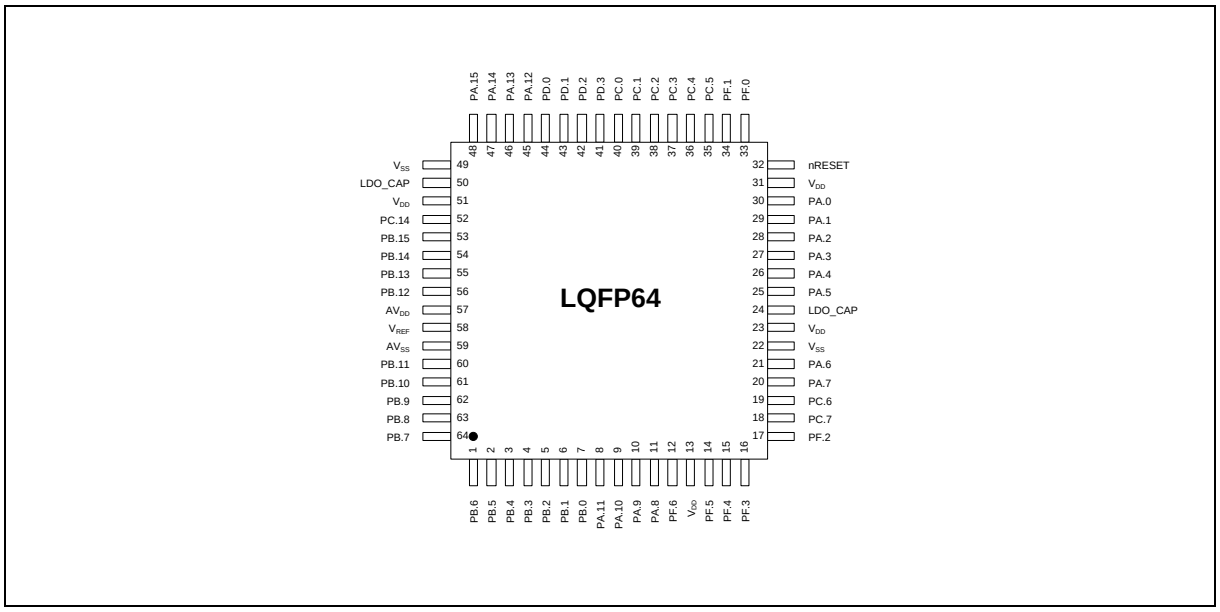


Figure 4.1-2 LQFP-64 Pin Diagram

4.1.3 LQFP-48 Multi-function Pin Diagram

Corresponding Part Number: M433LE8AE

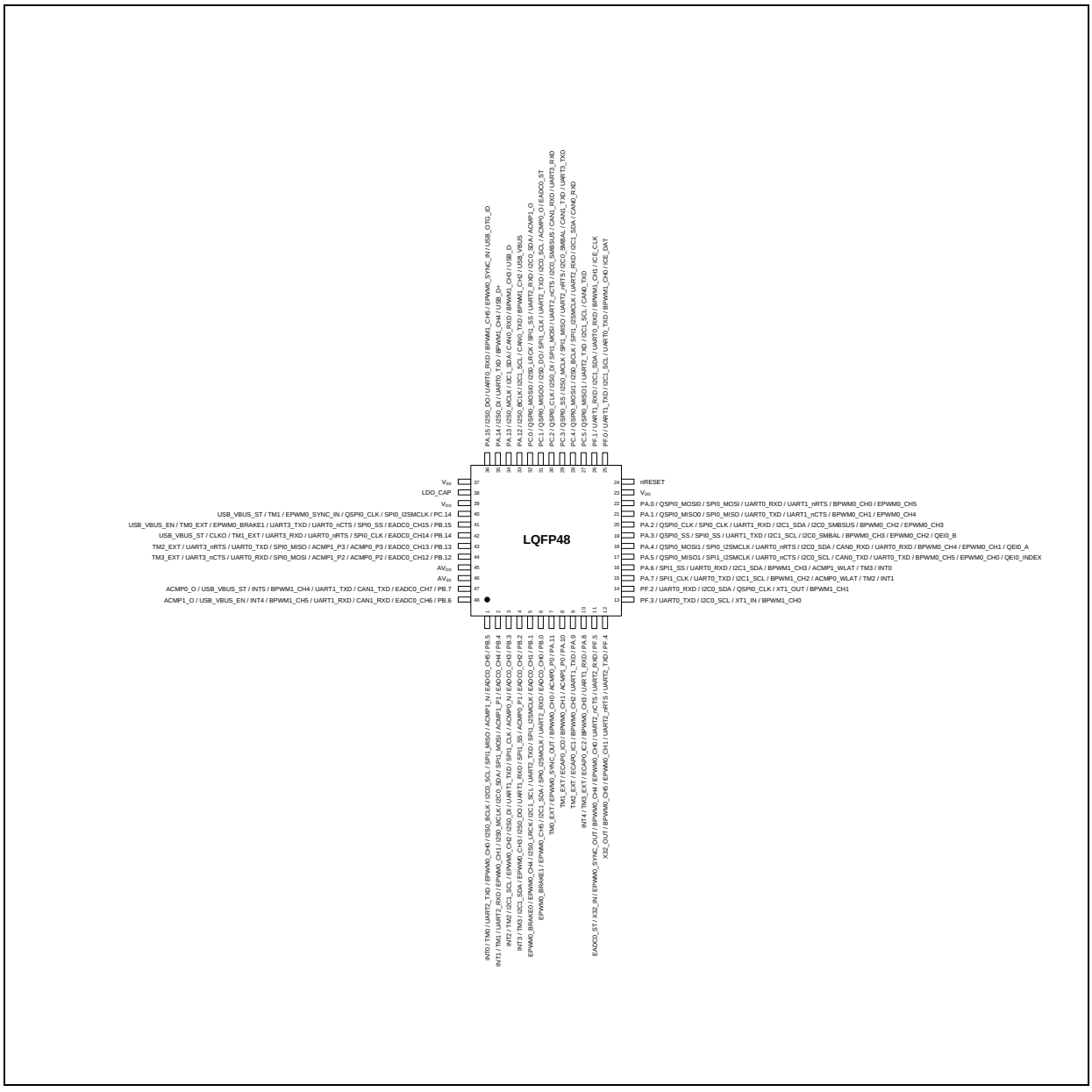


Figure 4.1-3 M433LE8AE Multi-function Pin Diagram

Pin	Type	M433LE8AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / SPI1_MISO / I2C0_SCL / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / SPI1_MOSI / I2C0_SDA / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / SPI1_CLK / UART1_TXD / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / SPI1_SS / UART1_RXD / I2S0_DO / EPWM0_CH3 / I2C1_SDA

Pin	Type	M433LE8AE Pin Function
		/ TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / SPI1_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM0_BRAKE0
6	I/O	PB.0 / EADC0_CH0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM0_BRAKE1
7	I/O	PA.11 / ACMP0_P0 / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
15	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / QEI0_INDEX
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / QEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / QEI0_B
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5
23	P	V_{DD}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK
27	I/O	PC.5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD
28	I/O	PC.4 / QSPI0_MOSI1 / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD
29	I/O	PC.3 / QSPI0_SS / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CAN1_TXD / UART3_TXD
30	I/O	PC.2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD
31	I/O	PC.1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O / EADC0_ST
32	I/O	PC.0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
33	I/O	PA.12 / I2S0_BCLK / I2C1_SCL / CAN0_TXD / BPWM1_CH2 / USB_VBUS

Pin	Type	M433LE8AE Pin Function
34	I/O	PA.13 / I2S0_MCLK / I2C1_SDA / CAN0_RXD / BPWM1_CH3 / USB_D-
35	I/O	PA.14 / I2S0_DI / UART0_TXD / BPWM1_CH4 / USB_D+
36	I/O	PA.15 / I2S0_DO / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / QSPI0_CLK / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST
41	I/O	PB.15 / EADC0_CH15 / SPI0_SS / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / UART0_nRTS / UART3_RXD / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / UART0_TXD / UART3_nRTS / TM2_EXT
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / UART0_RXD / UART3_nCTS / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / CAN1_TXD / UART1_TXD / BPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / CAN1_RXD / UART1_RXD / BPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.1-1 M433LE8AE Multi-function Pin Table

4.1.4 LQFP-64 Multi-function Pin Diagram

Corresponding Part Number: M433SE8AE

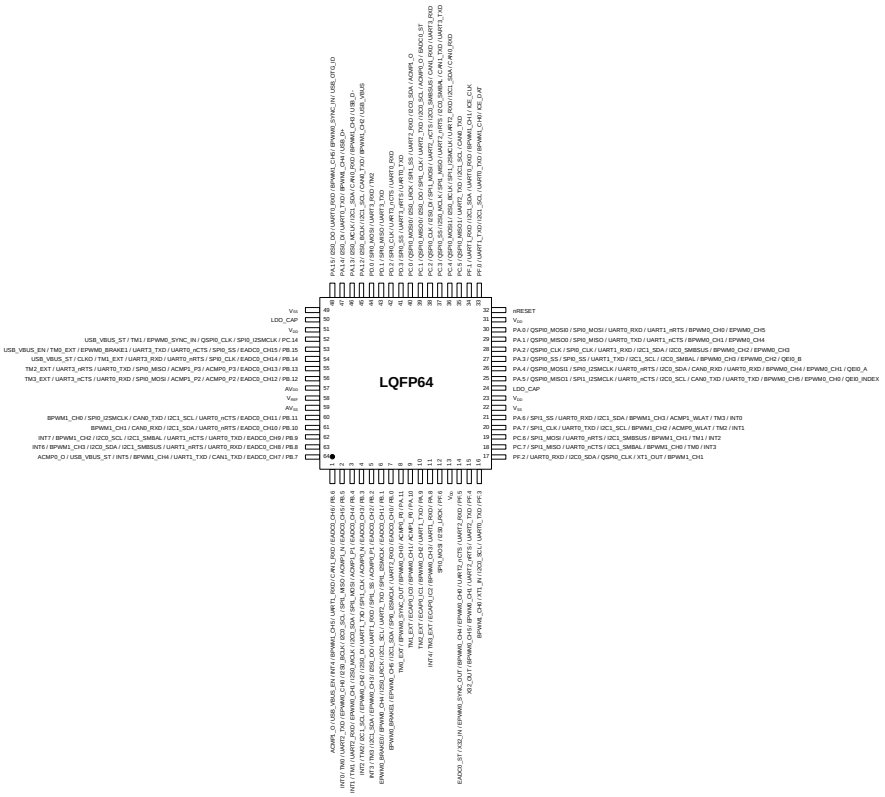


Figure 4.1-4 M433SE8AE Multi-function Pin Diagram

Pin	Type	M433SE8AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / CAN1_RXD / UART1_RXD / BPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / SPI1_MISO / I2C0_SCL / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / SPI1_MOSI / I2C0_SDA / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / SPI1_CLK / UART1_TXD / I2S0_DI / EPWM0_CH2 / I2C1_SCL /

Pin	Type	M433SE8AE Pin Function
		TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / SPI1_SS / UART1_RXD / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / SPI1_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM0_BRAKE0
7	I/O	PB.0 / EADC0_CH0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM0_BRAKE1
8	I/O	PA.11 / ACMP0_P0 / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT
10	I/O	PA.9 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT
11	I/O	PA.8 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / INT4
12	I/O	PF.6 / I2S0_LRCK / SPI0_MOSI
13	P	V_{DD}
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1
18	I/O	PC.7 / SPI1_MISO / UART0_nCTS / I2C1_SMBAL / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / SPI1_MOSI / UART0_nRTS / I2C1_SMBSUS / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / UART0_RXD / I2C1_SDA / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / QEI0_INDEX
26	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / QEI0_A
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / QEI0_B
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5
31	P	V_{DD}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / BPWM1_CH0 / ICE_DAT
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / BPWM1_CH1 / ICE_CLK

Pin	Type	M433SE8AE Pin Function
35	I/O	PC.5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD
36	I/O	PC.4 / QSPI0_MOSI1 / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD
37	I/O	PC.3 / QSPI0_SS / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CAN1_TXD / UART3_TXD
38	I/O	PC.2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD
39	I/O	PC.1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / ACMP0_O / EADC0_ST
40	I/O	PC.0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / ACMP1_O
41	I/O	PD.3 / SPI0_SS / UART3_nRTS / UART0_TXD
42	I/O	PD.2 / SPI0_CLK / UART3_nCTS / UART0_RXD
43	I/O	PD.1 / SPI0_MISO / UART3_TXD
44	I/O	PD.0 / SPI0_MOSI / UART3_RXD / TM2
45	I/O	PA.12 / I2S0_BCLK / I2C1_SCL / CAN0_TXD / BPWM1_CH2 / USB_VBUS
46	I/O	PA.13 / I2S0_MCLK / I2C1_SDA / CAN0_RXD / BPWM1_CH3 / USB_D-
47	I/O	PA.14 / I2S0_DI / UART0_TXD / BPWM1_CH4 / USB_D+
48	I/O	PA.15 / I2S0_DO / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / QSPI0_CLK / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST
53	I/O	PB.15 / EADC0_CH15 / SPI0_SS / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / TM0_EXT / USB_VBUS_EN
54	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / UART0_nRTS / UART3_RXD / TM1_EXT / CLKO / USB_VBUS_ST
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / UART0_TXD / UART3_nRTS / TM2_EXT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / UART0_RXD / UART3_nCTS / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / UART0_nCTS / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / I2C1_SDA / CAN0_RXD / BPWM1_CH1
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
64	I/O	PB.7 / EADC0_CH7 / CAN1_TXD / UART1_TXD / BPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

Table 4.1-2 M433SE8AE Multi-function Pin Table

4.2 Pin Mapping Table

The following is the pin mapping table of M433 series

	M433 Series	
Pin Name	48 Pin	64 Pin
PB.5	1	2
PB.4	2	3
PB.3	3	4
PB.2	4	5
PB.1	5	6
PB.0	6	7
PA.11	7	8
PA.10	8	9
PA.9	9	10
PA.8	10	11
PF.6		12
V_{DD}		13
PF.5	11	14
PF.4	12	15
PF.3	13	16
PF.2	14	17
PC.7		18
PC.6		19
PA.7	15	20
PA.6	16	21
V_{SS}		22
V_{DD}		23
LDO_CAP		24
PA.5	17	25
PA.4	18	26
PA.3	19	27
PA.2	20	28
PA.1	21	29
PA.0	22	30
V_{DD}	23	31

nRESET	24	32
PF.0	25	33
PF.1	26	34
PC.5	27	35
PC.4	28	36
PC.3	29	37
PC.2	30	38
PC.1	31	39
PC.0	32	40
PD.3		41
PD.2		42
PD.1		43
PD.0		44
PA.12	33	45
PA.13	34	46
PA.14	35	47
PA.15	36	48
V_{SS}	37	49
LDO_CAP	38	50
V_{DD}	39	51
PC.14	40	52
PB.15	41	53
PB.14	42	54
PB.13	43	55
PB.12	44	56
AV_{DD}	45	57
V_{REF}		58
AV_{SS}	46	59
PB.11		60
PB.10		61
PB.9		62
PB.8		63
PB.7	47	64
PB.6	48	1

4.3 Pin Functional Description

4.3.1 M433 Series Summary Function Pin Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CAN0	CAN0_RXD	I	CAN0 bus receiver input.
	CAN0_TXD	O	CAN0 bus transmitter output.
CAN1	CAN1_RXD	I	CAN1 bus receiver input.
	CAN1_TXD	O	CAN1 bus transmitter output.
CLKO	CLKO	O	Clock Out

Group	Pin Name	Type	Description
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_ST	I	EADC0 external trigger input.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
EPWM0	EPWM0_BRAKE0	I	EPWM0 Brake 0 input pin.
	EPWM0_BRAKE1	I	EPWM0 Brake 1 input pin.
	EPWM0_CH0	I/O	EPWM0 channel 0 output/capture input.
	EPWM0_CH1	I/O	EPWM0 channel 1 output/capture input.
	EPWM0_CH2	I/O	EPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	EPWM0 channel 3 output/capture input.
	EPWM0_CH4	I/O	EPWM0 channel 4 output/capture input.
	EPWM0_CH5	I/O	EPWM0 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	O	EPWM0 counter synchronous trigger output pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin

Group	Pin Name	Type	Description
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	O	I2S0 bit clock output pin.
	I2S0_DI	I	I2S0 data input pin.
	I2S0_DO	O	I2S0 data output pin.
	I2S0_LRCK	O	I2S0 left right channel clock output pin.
	I2S0_MCLK	O	I2S0 master clock output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
INT6	INT6	I	External interrupt 6 input pin.
INT7	INT7	I	External interrupt 7 input pin.
QEI0	QEI0_A	I	QEI0 phase A input
	QEI0_B	I	QEI0 phase B input
	QEI0_INDEX	I	QEI0 index input
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.

Group	Pin Name	Type	Description
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_OTG_ID	I	USB_ identification.

Group	Pin Name	Type	Description
	USB_VBUS	P	Power supply from USB host or HUB.
	USB_VBUS_EN	O	USB external VBUS regulator enable pin.
	USB_VBUS_ST	I	USB external VBUS regulator status pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. Note: This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{REF}	A	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. Note: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

5 BLOCK DIAGRAM

5.1 M433 Block Diagram

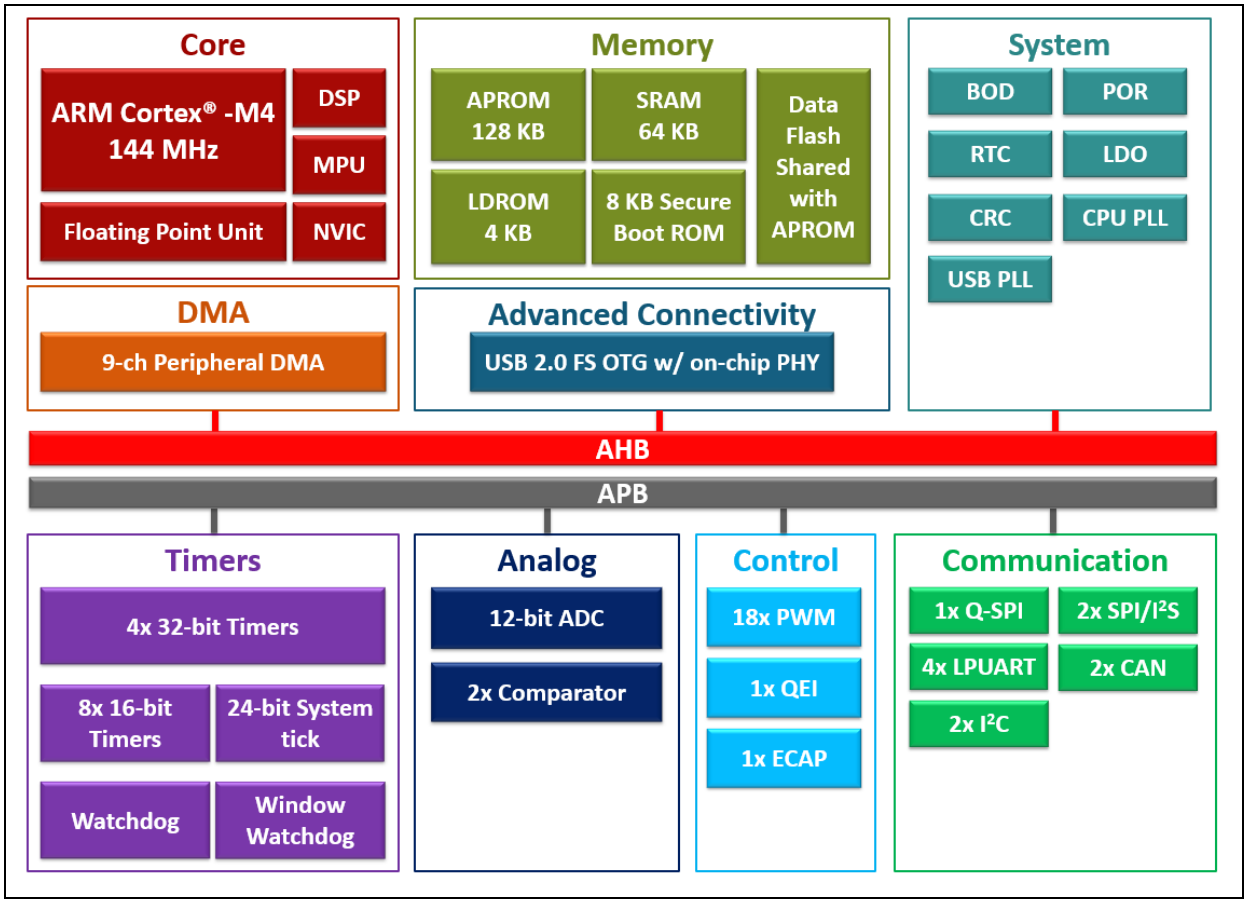


Figure 5.1-1 NuMicro® M433 Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M4F Core

The Cortex®-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex®-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex®-M4F is a processor with the same capability as the Cortex®-M4 processor and includes floating point arithmetic functionality. The NuMicro® M433 series is embedded with Cortex®-M4F processor. Throughout this document, the name Cortex®-M4 refers to both Cortex®-M4 and Cortex®-M4F processors. Figure 6.1-1 shows the functional controller of the processor.

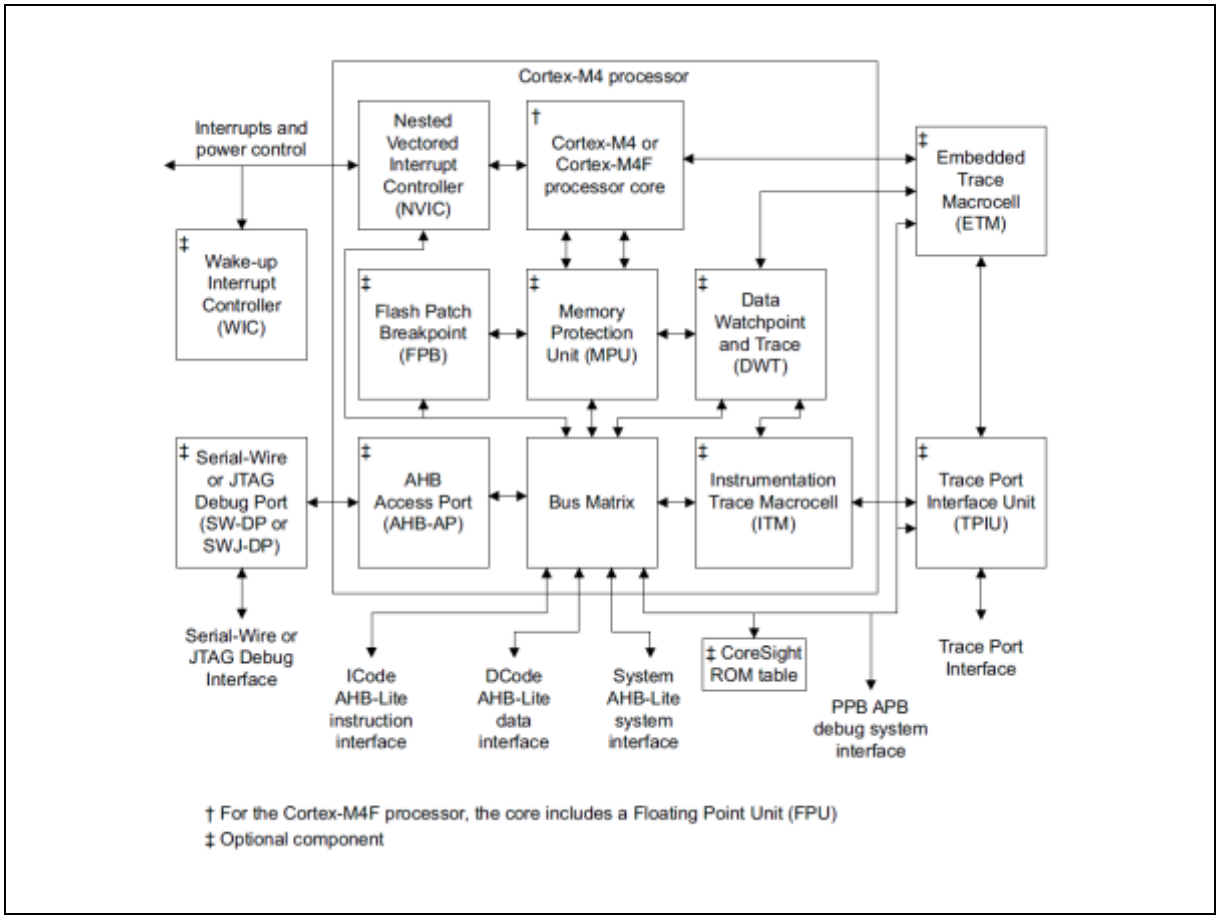


Figure 6.1-1 Cortex®-M4F Block Diagram

Cortex®-M4F processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *Armv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes

- Thumb and Debug states
- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for Armv6 big-endian byte-invariant or little-endian accesses
- Support for Armv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex®-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240 (the NuMicro® M433 series configured with 64 interrupts)
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and

code patches

- Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling
- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sourcces are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

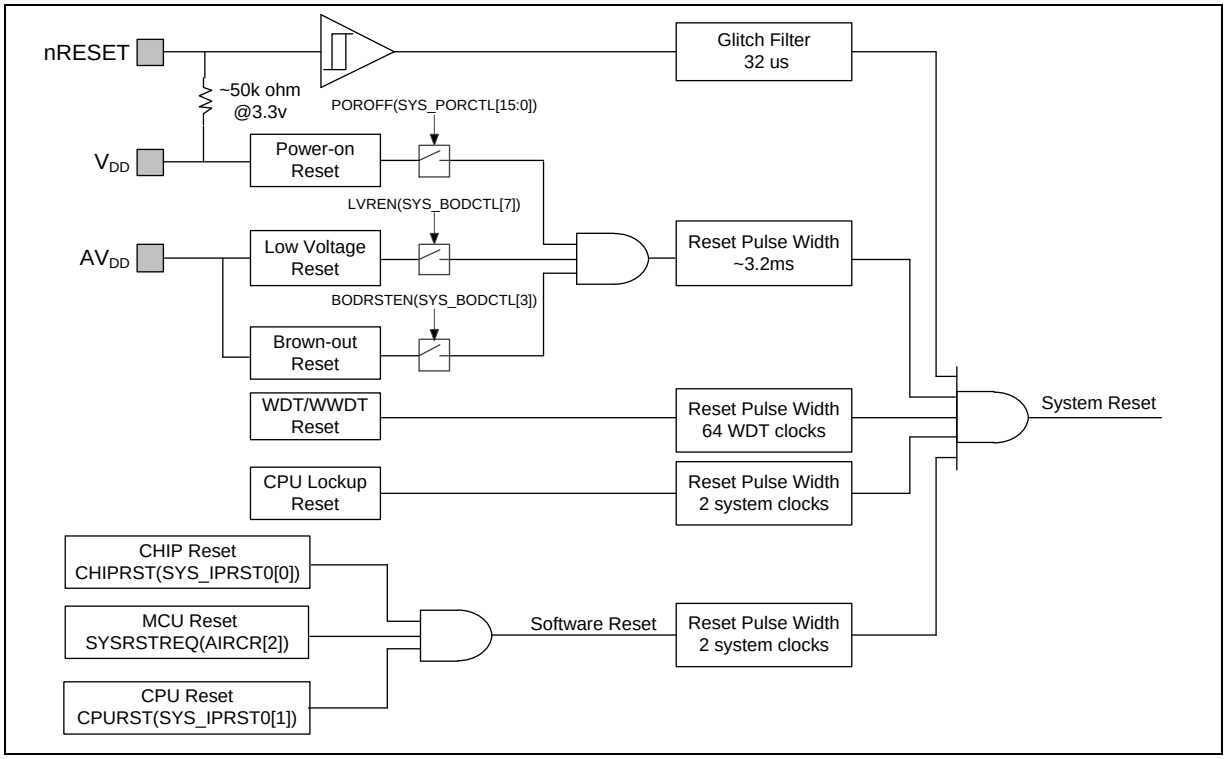


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M4 only; the other reset sources will reset Cortex®-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	-

(CLK_CLKSEL0[2:0])	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) BL (FMC_ISPCTL[16])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset Figure 6.2-2 shows the nRESET reset waveform.

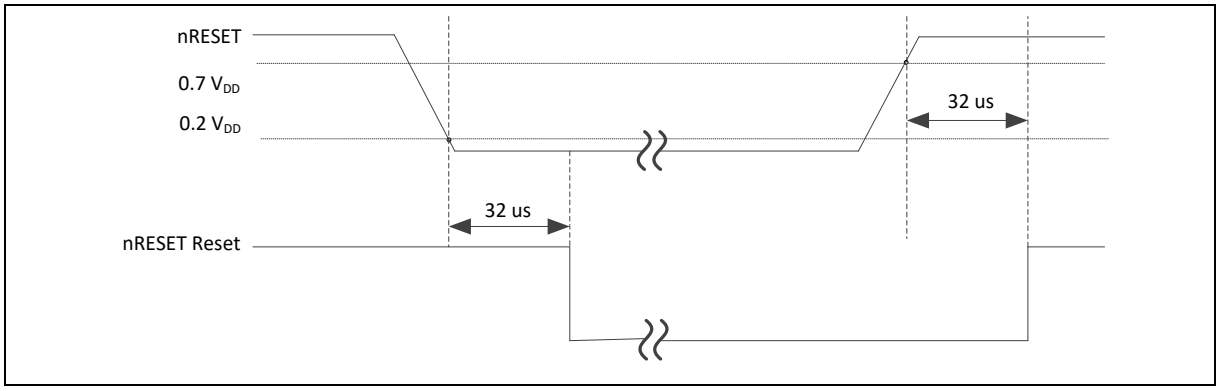


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it.Figure 6.2-3 shows the power-on reset waveform.

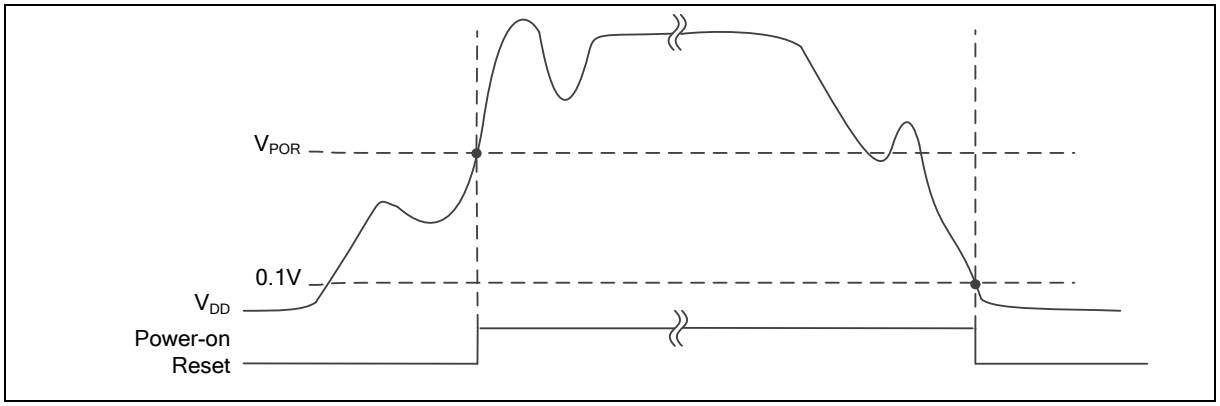


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the

AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function.Figure 6.2-4 shows the Low Voltage Reset waveform.

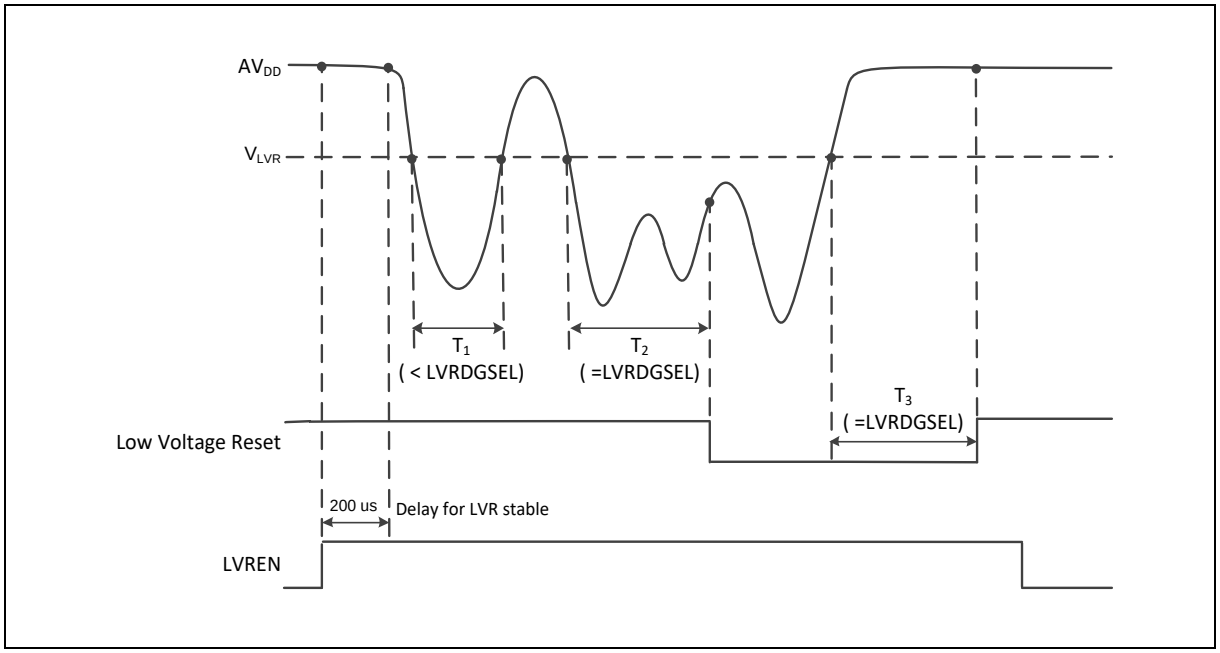


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

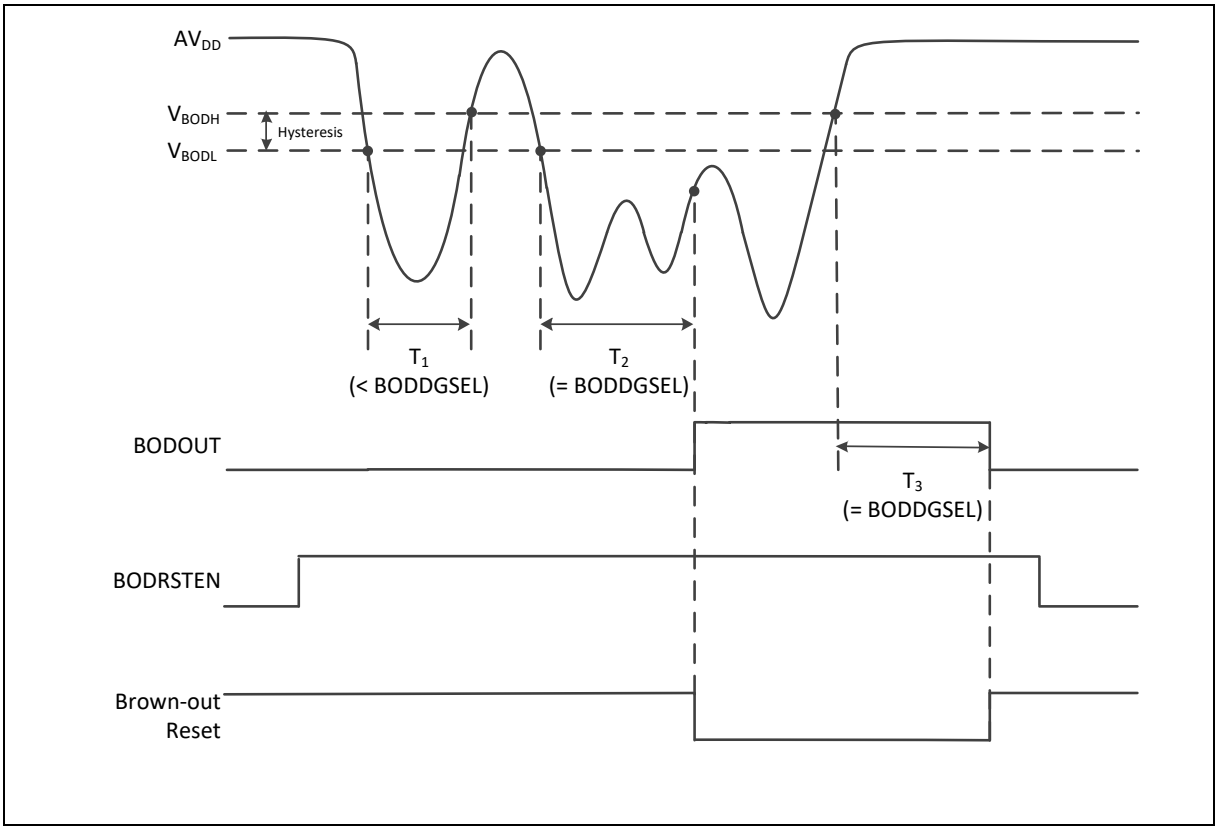


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8 V power for digital operation and I/O pins.
- USB transceiver power from V_{BUS} offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC and 80 bytes backup registers.

The outputs of internal voltage regulators, LDO and V_{DD33}, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-6 shows the NuMicro® M433 power distribution.

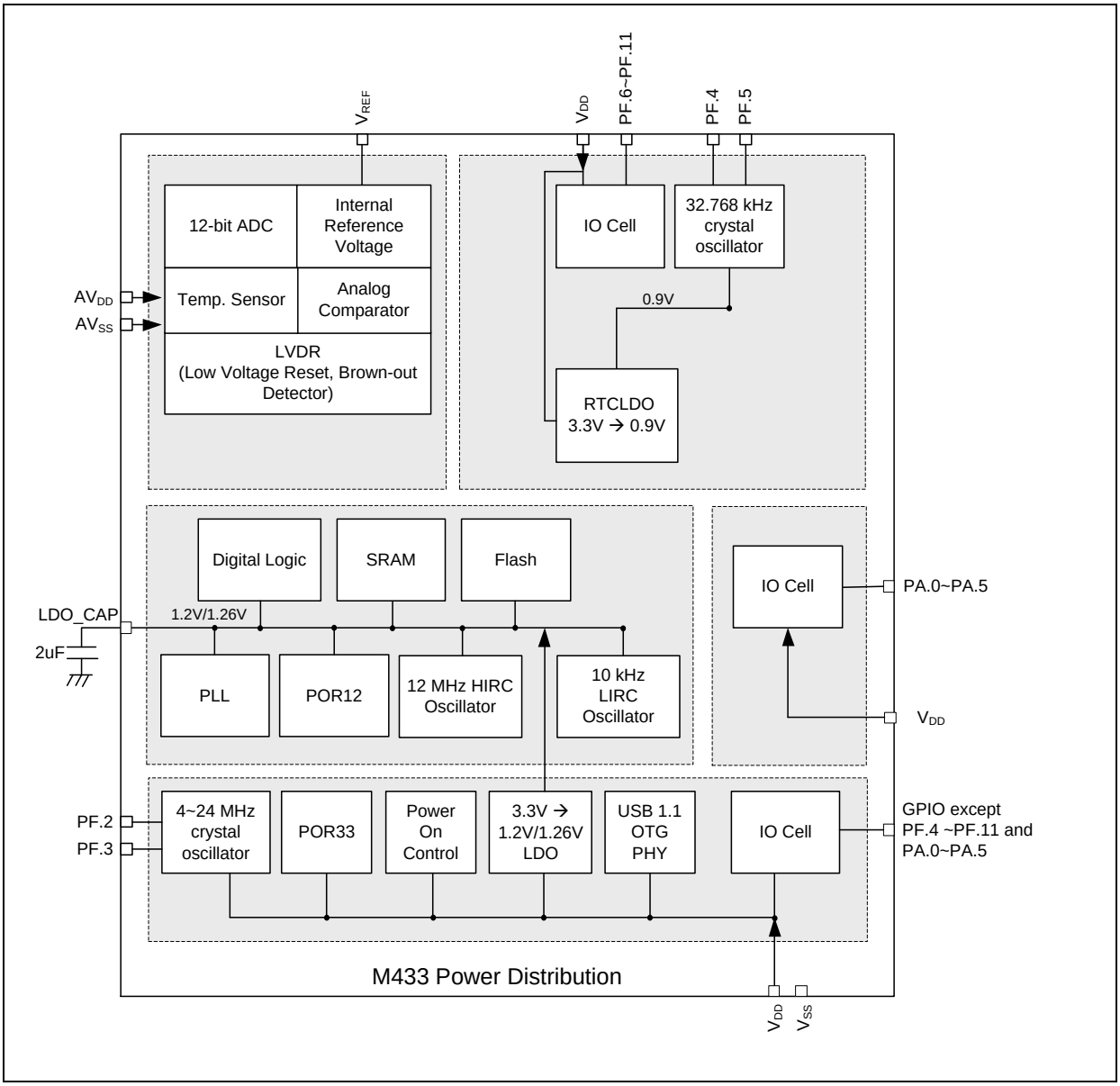


Figure 6.2-6 NuMicro® M433 Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The NuMicro® M433 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode at NuMicro® M433 series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	144	1.20	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	1.20	Only CPU clock is disabled.
Fast Wakeup Power-down mode (FWPD)	CPU enters Deep Sleep mode	1.20	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode (NPD)	CPU enters Deep Sleep mode	1.20	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage
Deep Power-down mode (DPD)	Power off	Floating	Only LIRC/LXT still enable for RTC function and wake-up timer usage

Table 6.2-2 Power Mode Table

Note:

1. User must turn on LIRC before entering SPD mode.
2. SPD mode data retension size is configurable.

There are different power mode entry setting For each power mode, they have different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running ar normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction. And

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Fast Wakeup Power-down mode	1	1	2	YES
Normal Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Standby Power-down mode (SRAM retention)	1	1	4	YES
Standby Power-down mode	1	1	5	YES
Deep Power-down mode	1	1	6	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP and BOD.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Definition Table

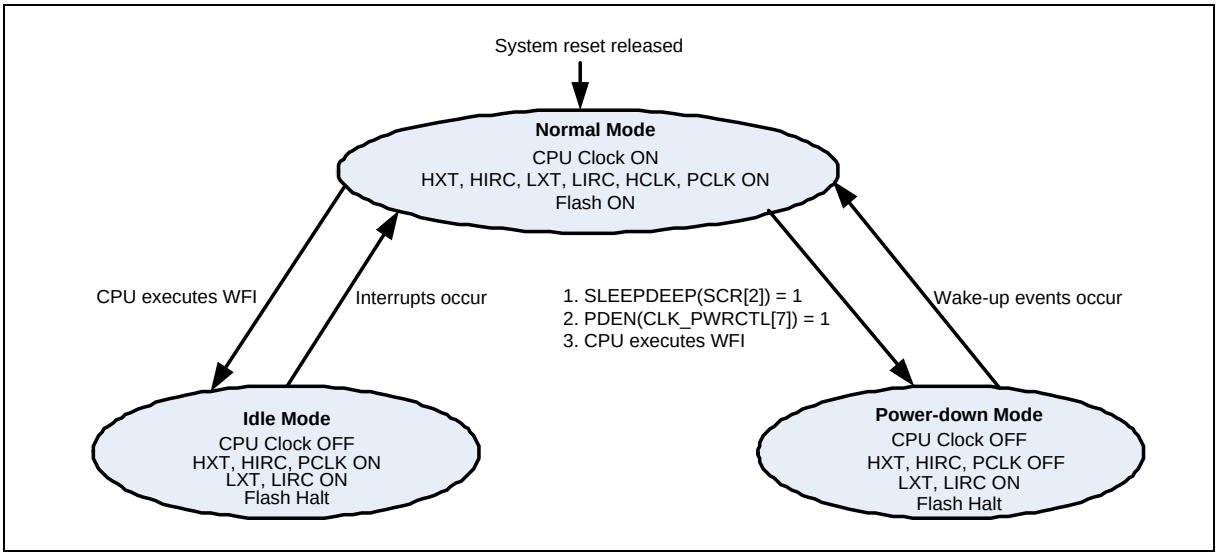


Figure 6.2-7 Power Mode State Machine

	Idle Mode	NPD, LLPD, FWPD	SPD	DPD
HXT	ON	Halt	Halt	Halt
HIRC	ON	Halt	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]	ON/OFF[2,8]
PLL	ON	Halt	Halt	Halt
HCLK/PCLK	ON	Halt	Halt	Halt
CPU	Halt	Halt	Halt	Halt
SRAM retention	ON	ON	ON/OFF[7]	Halt

FLASH	ON	Halt	Halt	Halt
TIMER	ON	ON/OFF[3]	Halt	Halt
WDT	ON	ON/OFF[4]	Halt	Halt
RTC (LXT)	ON	ON/OFF[5]	ON/OFF[5]	ON/OFF[5]
UART	ON	ON/OFF[6]	Halt	Halt
Others	ON	Halt	Halt	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on SW setting in normal mode.
2. LIRC ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.
7. SRAM retention size depends on SW setting in normal mode.
8. If timer wake up function is disabled, LIRC will be disabled automatically when chip enter DPD mode for power saving.

Wake-up sources in Normal Power-down mode (NPD):

RTC, WDT, I²C, Timer, UART, BOD, EBOD, GPIO, USBD, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode			Re-Entering Power-Down Mode Condition
		NPD/ FWPD/ LLPD	SPD	DPD	
BOD	Brown-Out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	-	After software writes 1 to clear PORF (SYS_RSTSTS[0])
INT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.

GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 64-pin	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered.
GPIO(PC.0/PB.0/PB.2/PB.12/PF.6) Wake-up pin	rising or falling edge event, 5-pin	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear PINWKx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.
	Wakeup by RTC tick time	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I^2C_WKSTS[1]). Then software writes 1 to clear WKIF(I^2C_WKSTS[0]).
USBD	Remote Wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).
ACMP	ACMPO status change	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWK (CLK_PMUSTS[14]) when SPD mode is entered.

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes and Power Level Transition

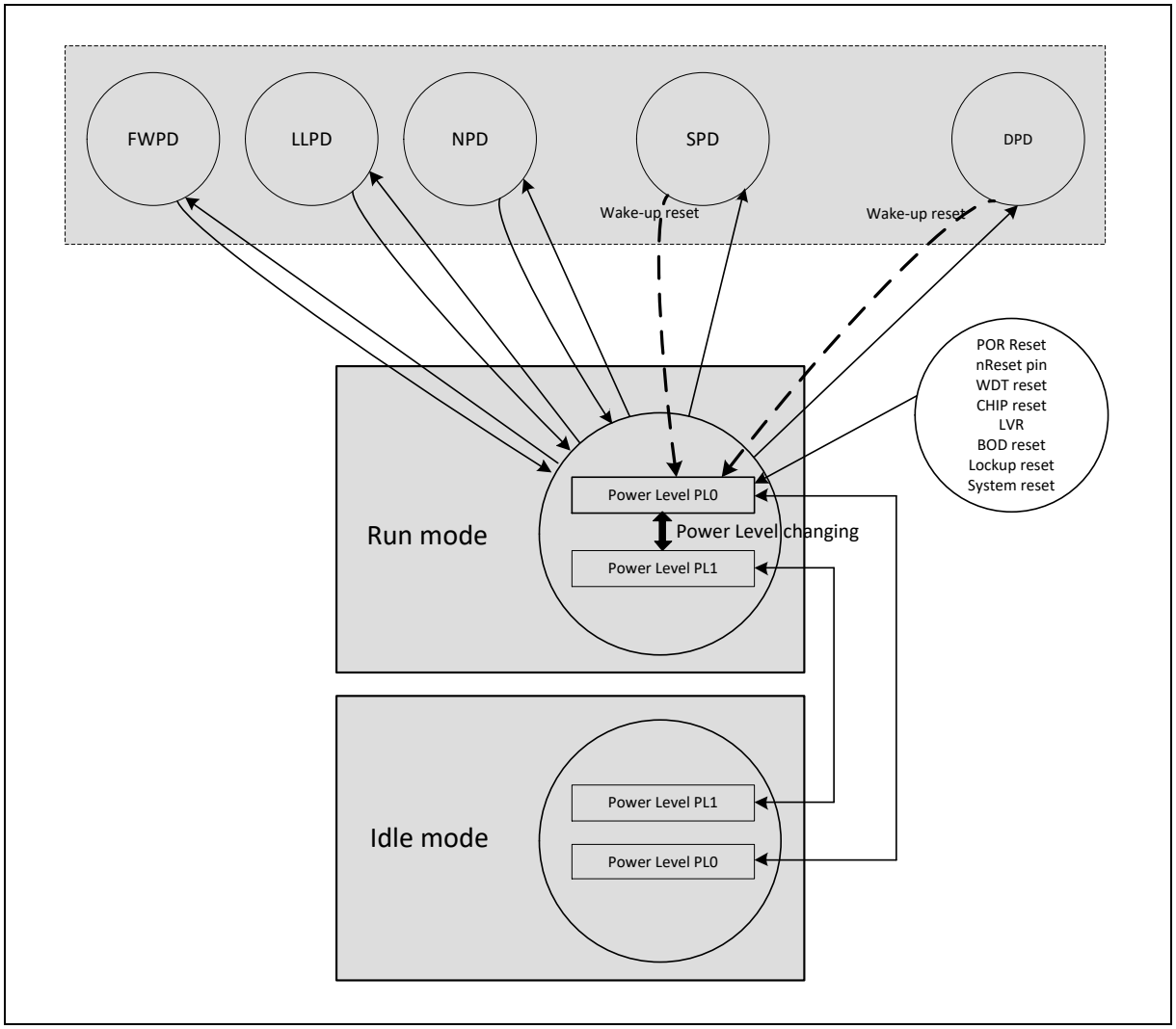


Figure 6.2-8 NuMicro® M433 Power Distribution Diagram

6.2.6 System Memory Map

The NuMicro® M433 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro® M433 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 Kbytes)
0x2000_0000 – 0x2000_7FFF	SRAM0_BA	SRAM Memory Space (32 Kbytes)
0x2000_8000 – 0x2000_FFFF	SRAM1_BA	SRAM Memory Space (32 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers

0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_E000 – 0x4003_EFFF	SWDC_BA	SWD Control Registers
0x4003_F000 – 0x4003_FFFF	ETMC_BA	ETM Control Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I2S0 Interface Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4008_0000 – 0x4008_0FFF	I^2C0_BA	I^2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I^2C1_BA	I^2C1 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Bus Control Registers
0x400A_1000 – 0x400A_1FFF	CAN1_BA	CAN1 Bus Control Registers
0x400B_0000 – 0x400B_0FFF	QEI0_BA	QEI0 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register

System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 SRAM Memory Orginization

The M433 series supports embedded SRAM with total 64 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0 and SRAM bank1. The first bank has 32 Kbytes address space, the second bank has 32 Kbyte address space. These two banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable.

- Supports total 64 Kbytes SRAM
- Supports byte / half word / word write
- Supports fixed 32 Kbytes SRAM bank0 for independent access
- Supports parity error check function for SRAM bank0
- Supports oversize response error
- Supports remap address to 0x1000_0000

Figure 6.2-9 SRAM Block Diagram

There are two SRAM banks in M433. The bank0 is addressed to 32 Kbytes, the bank1 is addressed to 32 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF. The bank1 address space is from 0x2000_8000 to 0x2000_FFFF. The address between 0x2001_0000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

	64KB Device	Read access
SRAM bank0	0x2000_0000 ~ 0x2000_7FFF or 0x1000_0000 ~ 0x1000_7FFF	Zero wait cycle for continuous access
SRAM bank1	0x2000_8000 ~ 0x2000_FFFF or 0x1000_8000 ~ 0x1000_FFFF	Zero wait cycle for continuous access

Table 6.2-8 SRAM Organization

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_7FFF or 0x1000_0000 to 0x1000_7FFF, and access SRAM bank1 through 0x2000_8000 to 0x2000_FFFF or 0x1000_8000 to 0x1000_FFFF.

SRAM bank0 has byte parity error check function. When CPU is accessing SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

6.2.8 Bus Matrix

The M433 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex®-M4 CPU as the highest bus priority.

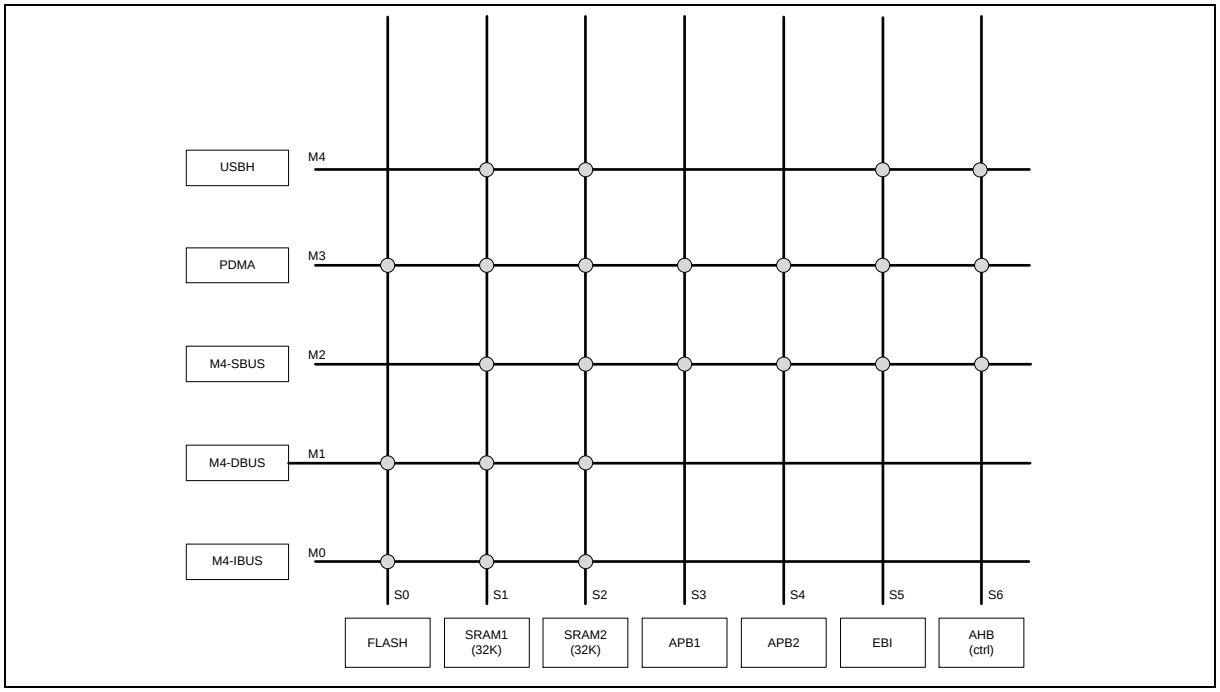


Figure 6.2-10 NuMicro® M433 Bus Matrix Diagram

6.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and HIRC trim (48 MHz RC oscillator,), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.10 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_BODCTL	address 0x4000_0018
SYS_VREFCTL	address 0x4000_0028
SYS_USBPHY	address 0x4000_002C
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_PORDISAN	address 0x4000_01EC
SYS_PLCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_FTCTL	address 0x4000_5018
FMC_ICPCMD	address 0x4000_501C
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
FMC_KPKEYTRG	address 0x4000_C05C
FMC_KPKEYSTS	address 0x4000_C060
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100

TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170
TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_CTL1	address 0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	address 0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	address 0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	address 0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC

BPWM_CTL0	address 0x4005_A000/0x4005_B000
SYST_VAL	address 0xE000_E018

6.2.11 System Timer (SysTick)

The Cortex®-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm® Cortex®-M4 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

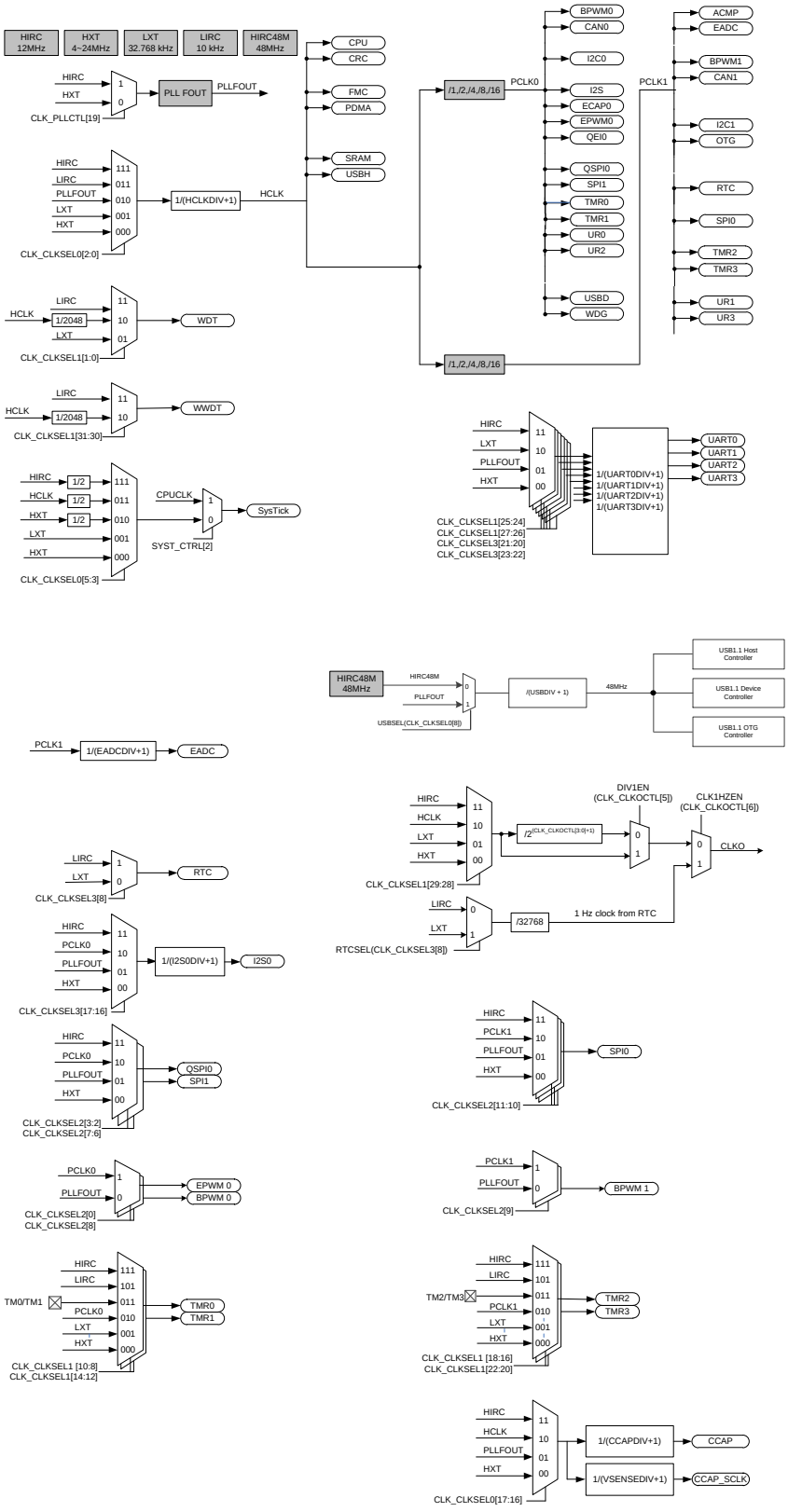
- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-16 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M4F core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 12 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.



Note: If HCLK clock source frequency is PLL, HCLKDIV setting should not be '1'. HCLK should not be equal to PLL/2.

Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

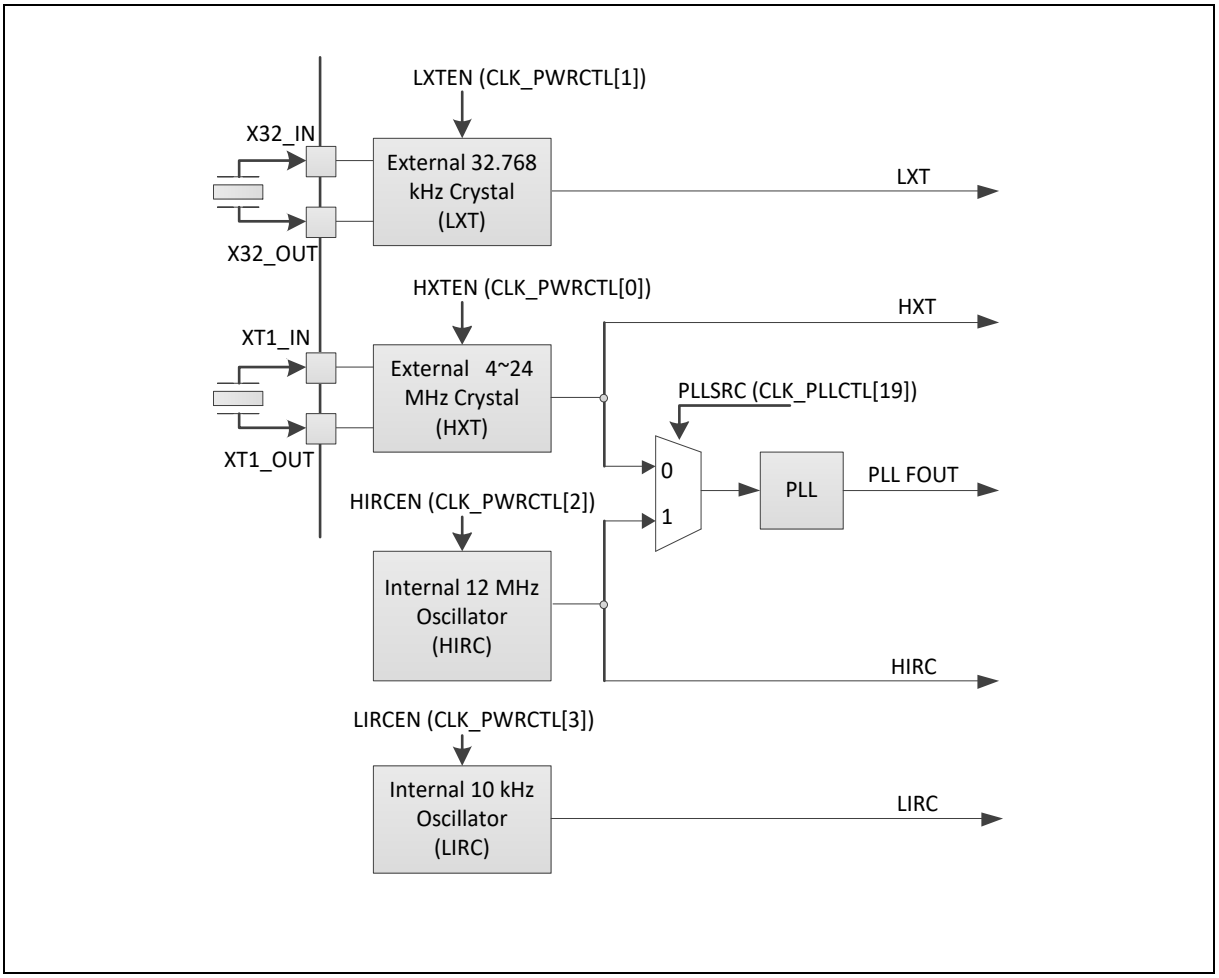


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3.

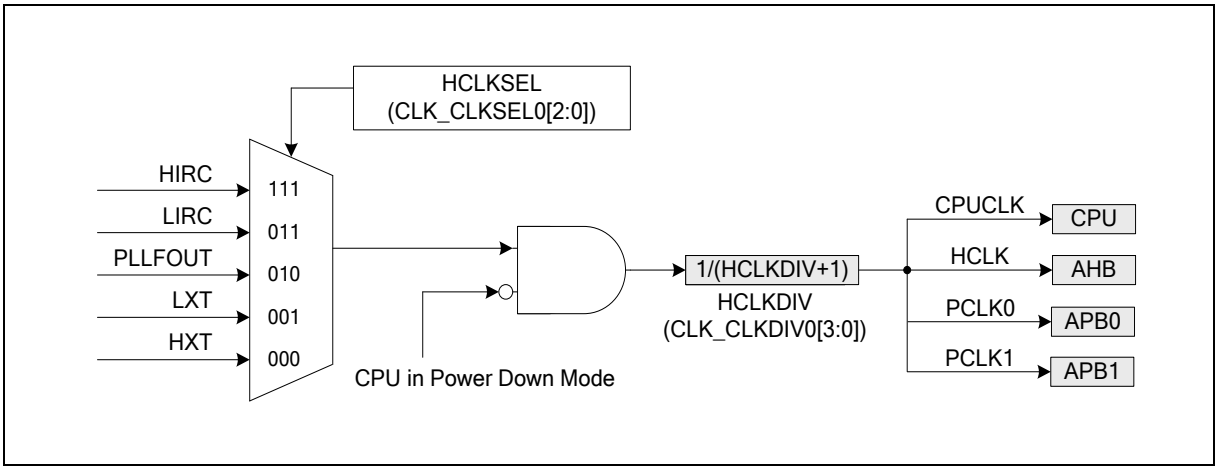


Figure 6.3-3 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-4 shows The HXT clock stops detection and system clock switches to HIRC procedure

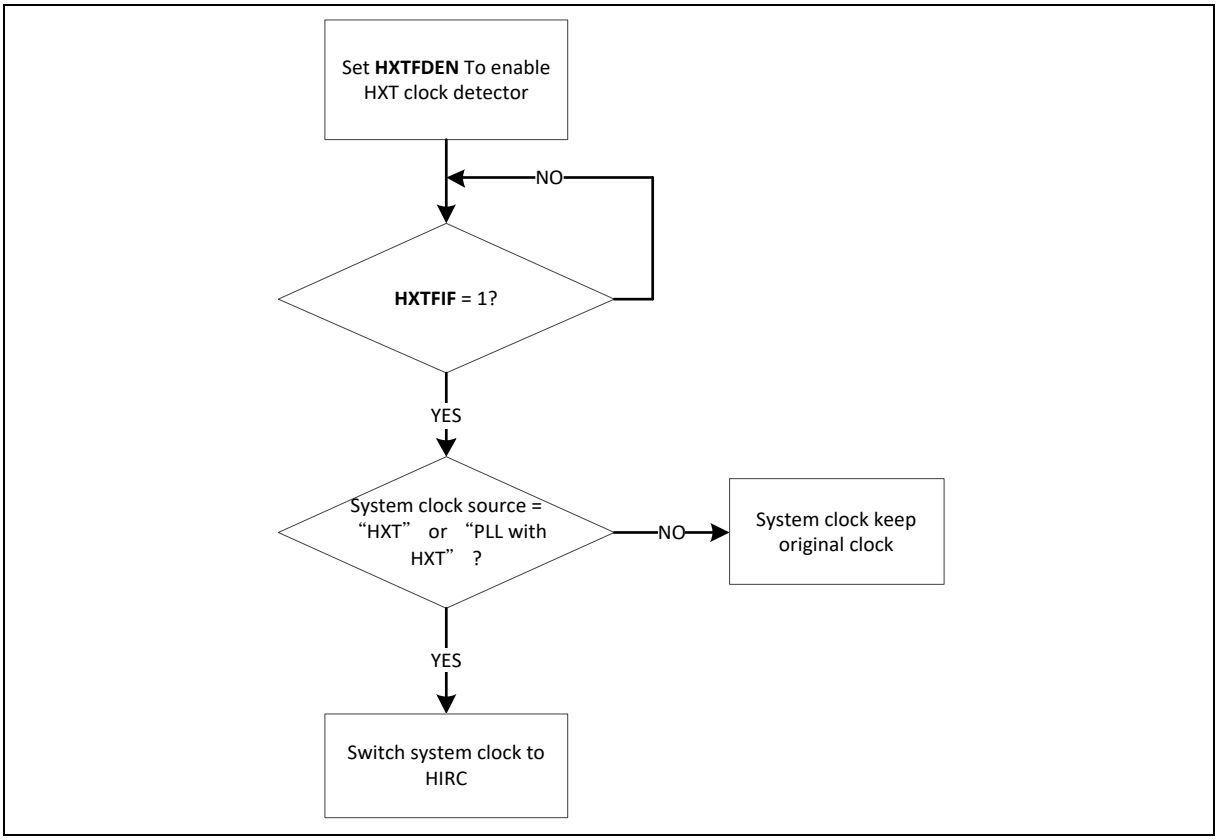


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M4F core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

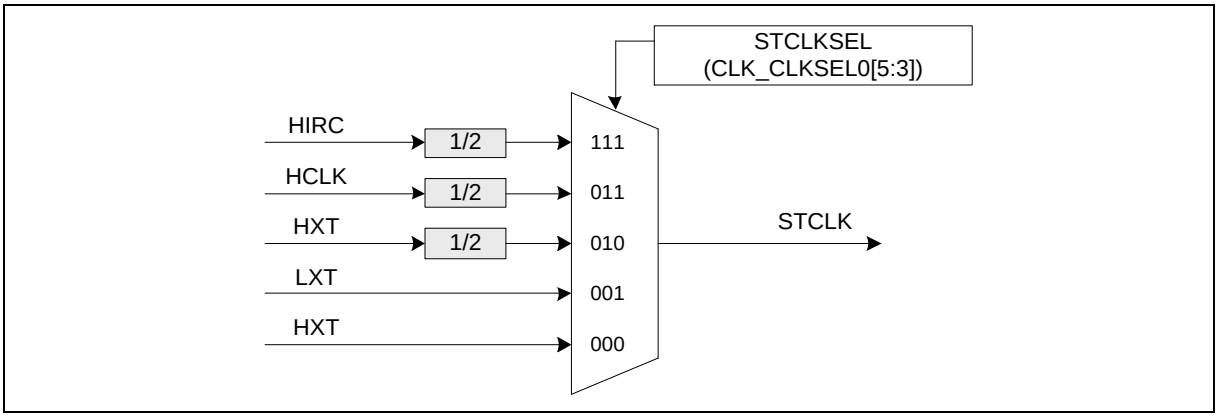


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1, CLK_CLKSEL2

and CLK_CLKSEL3 register.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

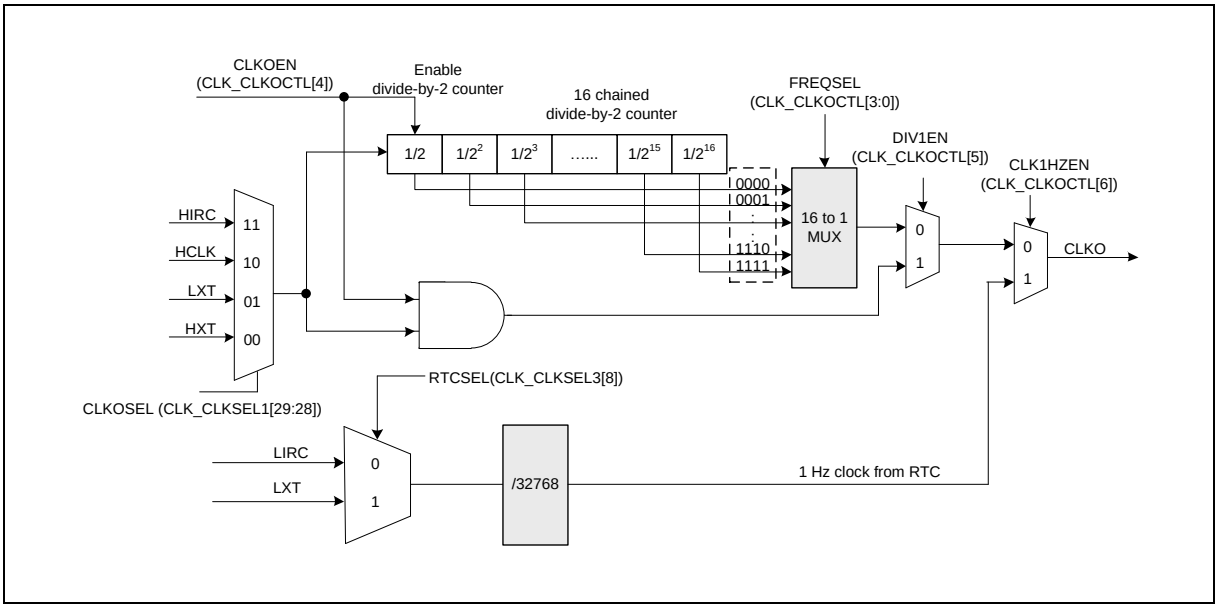


Figure 6.3-6 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock sources of USB 1.0 and 2.0 systems are generated from external crystal clock 12MHz or programmable PLL output. M433 has a HIRC48M for USB 1.0 system. The generated clocks are shown in Figure 6.3-7.

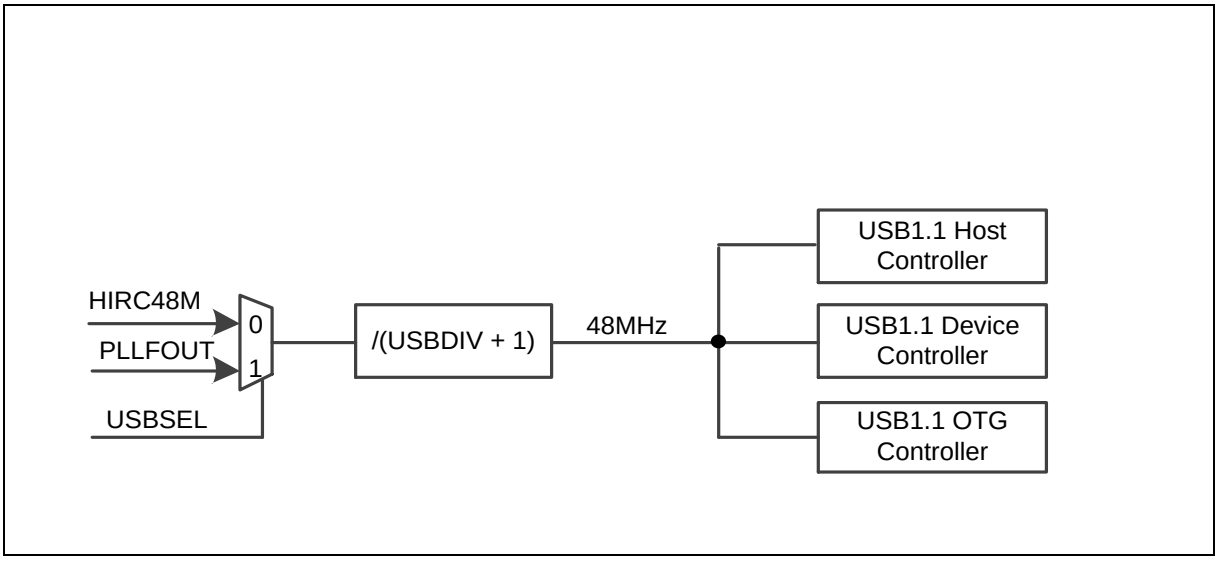


Figure 6.3-7 USB Clock Source

6.4 Flash Memeory Controller (FMC)

6.4.1 Overview

The FMC is equipped with 128 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. Thus, the total size of application rom (APROM) is 128 Kbytes. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 128 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports block and bank erase for APROM
- Supports Secure Boot function for code integrity and authenticity
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 52 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 52 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. Each of the 52 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]).

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 9 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 9 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and SPI, UART, ADC and PWM request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1
- Supports stride function from channel 0 to channel 5
- Enhanced Stride Function for image processing

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, QEI, EADC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports Inter-Timer trigger mode
- Supports event counting source from internal USB SOF signal

6.7.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin

- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 1.6 ms ~ 26.214 s if WDT_CLK = 10 kHz.
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 10 kHz or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 Real Time Clock (RTC)

6.10.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.10.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.

6.11 EPWM Generator and Capture Timer (EPWM)

6.11.1 Overview

The chip provides a EPWM generators — EPWM0. The EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.11.2 Features

6.11.2.1 EPWM Function Features

- Supports maximum clock frequency up to 144MHz
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value
  - Supports EPWM trigger EADC event prescaler feature
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect function

6.11.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.12 Basic PWM Generator and Capture Timer (BPWM)

6.12.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.12.2 Features

6.12.2.1 BPWM Function Features

- Supports maximum clock frequency up to 144MHz.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0 in the following events:
  - BPWM counter matches 0, period value or compared value

6.12.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.13 Quadrature Encoder Interface (QEI)

6.13.1 Overview

There are one QEI controllers in this device. The Quadrature Encoder Interface (QEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.13.2 Features

6.13.2.1 Quadrature Encoder Interface (QEI) Features

- One QEI controllers, QEI0.
- Two QEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (QEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (QEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (QEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (QEI_CNTCMP) with a Pre-set Maximum Count Register (QEI_CNTMAX)
- One QEI control register (QEI_CTL) and one QEI Status Register (QEI_STATUS)
- Four Quadrature encoder pulse counter operation modes
  - Support x4 free-counting mode
  - Support x2 free-counting mode
  - Support x4 compare-counting mode
  - Support x2 compare-counting mode
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clk/8

6.14 Enhanced Input Capture Timer (ECAP)

6.14.1 Overview

The chip provides one units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.14.2 Features

- One Input Capture Timer/Counter units, CAP0.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.15 UART Interface Controller (UART)

6.15.1 Overview

The chip provides four channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs Normal Speed UART and supports flow control function. The UART controller performs a serial-to-parallel conversion on data received from the peripheral and a parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.15.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0/UART1	UART2 ~ UART3
FIFO	16 Bytes	16 Bytes
Auto Flow Control (CTS/RTS)	√	√
IrDA	√	√
LIN	√	-
RS-485 Function Mode	√	√
nCTS Wake-up	√	√
Imcoming Data Wake-up	√	√
Received Data FIFO reached threshold Wake-up	√	√
RS-485 Address Match (AAD mode) Wake-up	√	√
Auto-Baud Rate Measurement	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits
Even / Odd Parity	√	√
Stick Bit	√	√

Table 6.15-1 M433 Series UART Features

6.16 I²S Controller (I²S)

6.16.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.16.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.17 Serial Peripheral Interface (SPI)

6.17.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to two sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.17.2 Features

- SPI Mode
  - Up to two sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 72 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Slave mode up to 72 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7~3.6V)
  - Slave mode up to 36 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7~3.6V)
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.18 Quad Serial Peripheral Interface (QSPI)

6.18.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.18.2 Features

- Supports Master or Slave mode operation
- Master mode up to 72 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Slave mode up to 72 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7V~3.6V)
- Slave mode up to 36 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at V_{DD} = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.19 I²C Serial Interface Controller (I²C)

6.19.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers which support Power-down wake-up function.

6.19.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports High speed mode 3.4Mbps
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function

6.20 Controller Area Network (CAN)

6.20.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 Mbps. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.20.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 Mbps
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.21 USB 1.1 Device Controller (USBD)

6.21.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/ isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytesytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEGx).

There are 12 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK etc, and BUS events, like suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disable the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.21.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3 ms
- Supports 12 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability

6.22 USB 1.1 Host Controller (USBH)

6.22.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port over current detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting over current of attached USB devices.

6.22.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port over current detection.
- Supports DMA for real-time data transfer.

6.23 USB On-The-Go (OTG)

6.23.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID-dependent or OTG Device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, USB frame acts as USB host. USB frame can support both full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame only supports full-speed transfer. In ID-dependent mode, USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame only supports full-speed transfer when OTG device acts as a peripheral.

6.23.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID-dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). Not support HNP or SRP protocol.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). Support HNP and SRP protocols.

6.24 CRC Controller (CRC)

6.24.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.24.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.25 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.25.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 16 external input channels and 3 internal channels. The EADC0 converter can be started by software trigger, EPWM0 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.25.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and power (V_{DD})
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for each EADC
- Maximum EADC clock frequency is 72 MHz for each EADC
- Up to 5.14 MSPS conversion rate for each EADC at the same time
- Configurable EADC internal sampling time for each EADC
- 12-bit, 10-bit, 8-bit, 6-bit configurable resolution for each EADC
- Supports calibration and load calibration words capability for each EADC
- Supports internal reference voltage V_{REF}: 1.6V, 2.0V, 2.5V, and 3.0V.
- Supports three power saving modes:
  - Deep Power-down mode
  - Power-down mode
  - Standby mode
- Up to 19 sample modules
  - Each of sample modules which is configurable for EADC converter channel (EADC0_CH0~15) and trigger source for each EADC
  - Sample module 16~18 is fixed for EADC0channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and power (V_{DD})
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC0_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers

  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.26 Analog Comparator Controller (ACMP)

6.26.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.26.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV and 30mV
- Supports wake-up function
- Supports programmable propagation speed and low power consumption
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Comparator Reference Voltage (CRV)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode

6.27 Peripherals Interconnection

6.27.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

6.27.2 Peripherals Interconnect Matrix Table

Source	Destination								
	BPWM	EADC	ECAP	EPWM	HIRC	IRCTRIM	HIRC48M	TIMERPWM	QEI
ACMP	-	-	-	3	-	-	-	3,6	
BOD	-	-	-	3	-	-	-	3	
BPWM	4	1	-	4	-	-	-	-	
Clock Fail	-	-	-	3	-	-	-	3	
CPU Lockup	-	-	-	3	-	-	-	3	
EADC	-	-	-	3	-	-	-	-	
EPWM	4	1	-	4	-	-	-	-	
IRCTRIM	-	-	-	-	2	-	2	-	
LIRC	-	-	-	-	-	-	-	6	
LXT	-	-	-	-	-	2	-	-	
QEI	-	-	8	-	-	-	-	-	
SRAM	-	-	-	3	-	-	-	3	
TIMERPWM	5	1	-	5	-	-	-	7	9
USB11Device	-	-	-	-	-	2	-	-	

Table 6.27-1 Peripherals Interconnect Matrix Table

6.27.3 Functional Description

6.27.3.1 From EPWM, TIMER to EADC

EPWM Trigger EADC Conversion

EPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from EPWM trigger.

BPWM Trigger EADC Conversion

BPWM can be one of the EADC conversion trigger source.

Setting the EADC external hardware trigger input source from BPWM trigger.

Timer Trigger EADC Conversion

Timer0 ~ Timer3 can be one of the EADC conversion trigger source. When timer counter value matches the timer compared value or when the TMx_EXT pin edge transition meets setting, timer will trigger the ADC to start the conversion.

Setting the EADC external hardware trigger input source from timer trigger.

6.27.3.2 From LXT and USB 1.1 Device to HIRC TRIM & RC 48 MHz

Use LXT or USB Synchronous Mode to System Auto-trim HIRC Circuit

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and RC 48 MHz oscillator, according to the accurate external 32.768 kHz crystal oscillator or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

6.27.3.3 From ACMP, BOD, Clock Fail,SRAM Parity Error and CPU Lockup to EPWM/ TIMERPWM

EPWM Brake Source

EPWM brake source can be ACMP0/1_O output signal or EADC result monitor or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

TIMERPWM Brake Source

TIMERPWM brake source can be ACMP0/1_O output signal or several different system fail conditions include clock fail, Brown-out detect, and Core lockup and SRAM Parity Error. When system fault, EPWM brake signal generated, EPWM output will be set to protect the power switch controlled by EPWM.

6.27.3.4 From EPWM/ BPWM to EPWM/ BPWM

EPWM Synchronous Start Function

Select synchronous source from EPWM0 or BPWM0 or BPWM1, and select EPWM channels. The chosen EPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(EPWM_SSTRG[0]) is set.

BPWM Synchronous Start Function

Select synchronous source from EPWM0 or BPWM0 or BPWM1, and select BPWM channels. The chosen BPWM channels will start counting at the same time once the synchronous start function is enabled and CNTSEN(BPWM_SSTRG[0]) is set.

6.27.3.5 From TIMER to EPWM/BPWM

Timer Generates Trigger Pulses as EPWM External Clock Source

Timer0 ~ Timer3 can generates trigger pules as EPWM/BPWM external clock source.

When timer counter value matches the timer compared value or when the TMx_EXT pin edge transition meets setting, timer can generate a trigger pulse by setting.

6.27.3.6 From ACMP and LIRC to Timer Capture Function

Measure the Time Interval of ACMP0/1 Output Signal or LIRC Clock Speed

Sets the timer capture source from ACMP0/1 output signal or LIRC clock and measures the time interval of the signal by using timer capture function. Users can use the results of time interval to trim LIRC through software or to get the ACMP0/1 output pulse width.

6.27.3.7 From Timer0/2 to Timer1/3

Inter-Timer Trigger Capture Mode

Timer0/2 will be forced in event counting mode, counting with external event, and will generate an

internal signal (INTR_TMR_TRG) to trigger Timer1/3 start or stop counting. The Timer1/3 will be forced in capture mode and start/stop trigger-counting by Timer0/2 counter status.

6.27.3.8 From QEI to ECAP

ECAP Input Noise Filter

The architecture of ECAP input noise filter is similar to that one used for QEI. With 6 sampling-rate options, it supports a wide range of filtering noise, the duration of filtered noise and the duration of the signal that is guaranteed to be sampled.

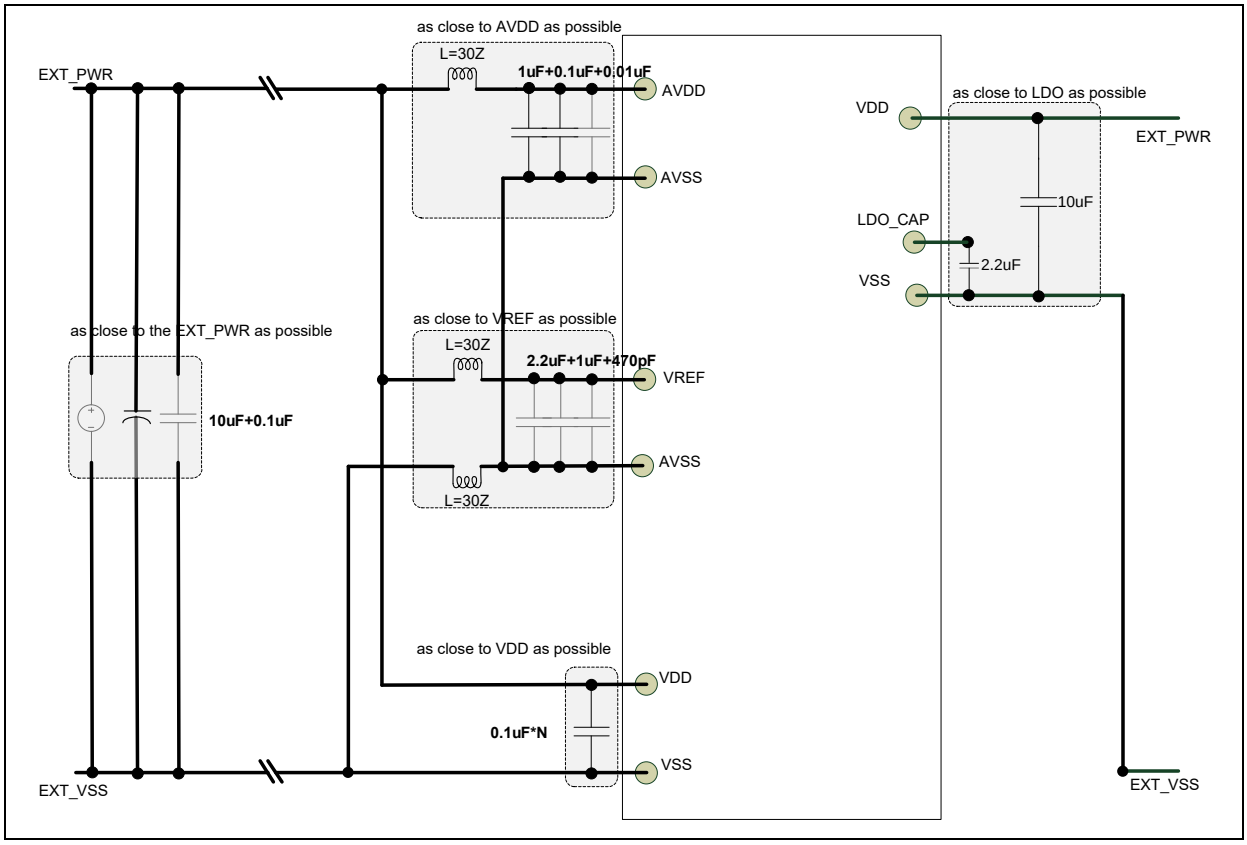
6.27.3.9 From TIMER to QEI

TIMER TIF Event to QEI

When QEI bit HOLDCNT(QEI_CTL[24]) set, the CNT(QEI_CNT[31:0]) content will be captured into QEI Counter Hold Register CNTHOLD(QEI_CNTHOLD[31:0]), the data will be held until the next HOLDCNT (QEI_CTL[24]) trigger comes. The bit HOLDCNT can be set by writing 1 to it or the rising edge of timers interrupt flags TIF (TIMERx_INTSTS[0]).

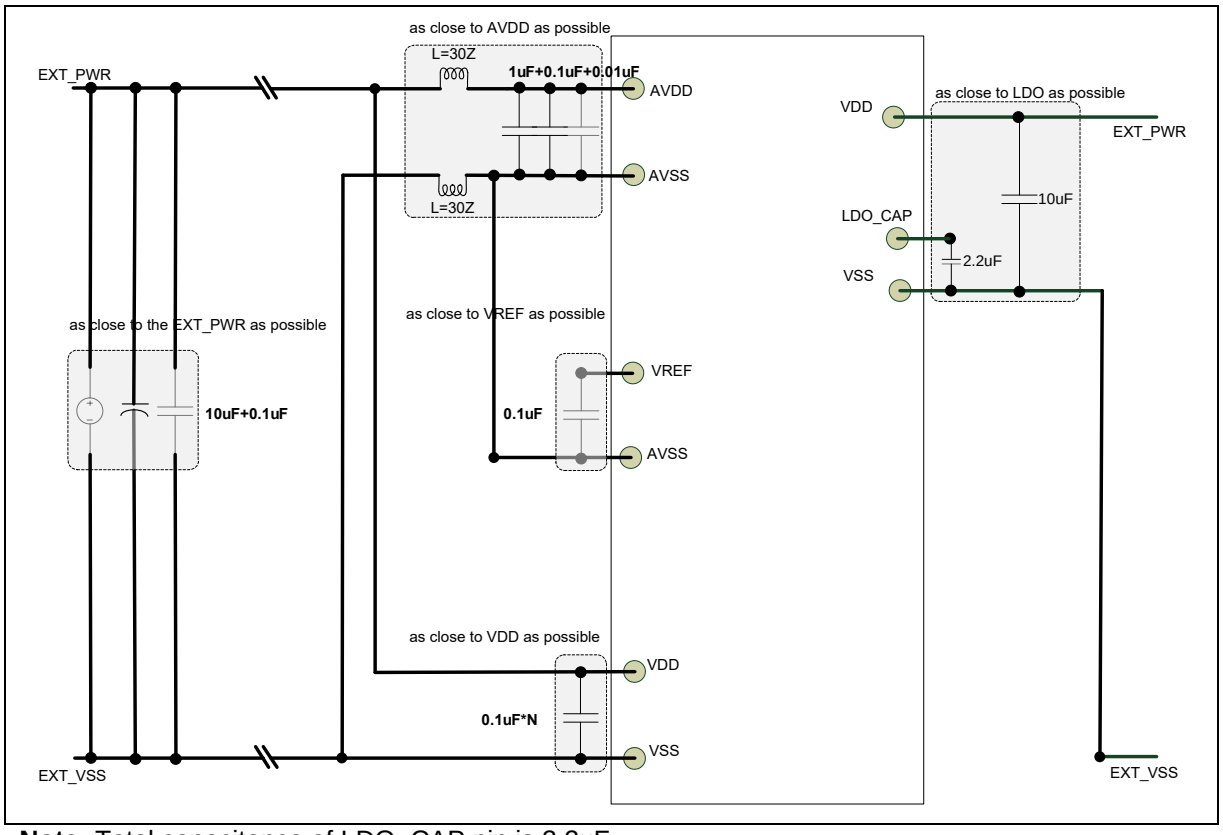
7 APPLICATION CIRCUIT

7.1 Power Supply Scheme with External V_{REF}



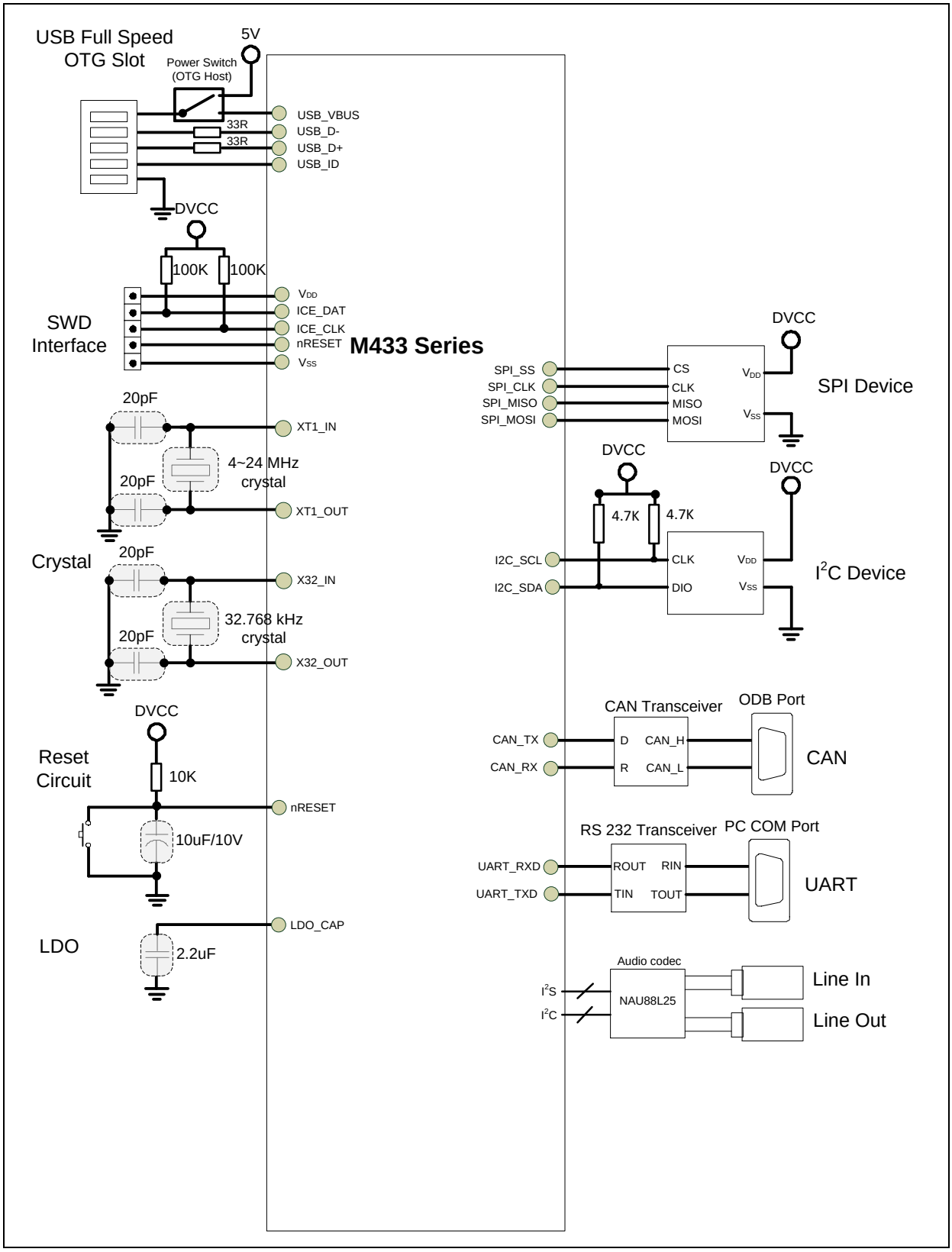
Note: Total capacitance of LDO_CAP pin is 2.2uF.

7.2 Power Supply Scheme with Internal V_{REF}



Note: Total capacitance of LDO_CAP pin is 2.2uF.

7.3 Peripheral Application Scheme



Note 1: USB_ID could be floating using USB without OTG.

Note 2: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 3: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 4: Total capacitance of LDO_CAP pin is 2.2uF.

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC Power Supply	-0.3	4	V
$\|V_{DDX} - V_{DD}\|$	Variations between different power pins		50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}		50	mV
$\|V_{SSX} - V_{SS}\|$	Variations between different ground pins		50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}		50	mV
V_{IN}	Input Voltage on 5V-tolerance GPIO		5.5	V
	Input Voltage on RTC domain (PF.6 ~ PF.11)		V_{DD}	V
	Input Voltage on any other pin[*2]		V_{DD}	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. Non 5V-tolerance PIN: PA.8 ~ 15; PB.0 ~ 15; PD.10, 11, 12; PF.2, 3, 4, 5; All USB High Speed PIN and nRESET PIN.

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Conditions	Maximum Value	Unit
V_{EFTB}	1. Fast transient voltage burst limits to be applied through 100 pF + 47uF on V_{DD} and V_{SS} pins to induce a functional disturbance 2. to be applied through 2.2uF on LDO_Pin and V_{SS} pins	V_{DD} = 3.3 V, LQFP64, T_A = +25 °C, f_{HCLK} = 144 MHz	4.4	kV

Table 8.1-4 EMS Characteristics

Symbol	Ratings	Conditions	Maximum Value	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C	2[*1]	kV
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C	0.5[*1]	
Note: 1. Guaranteed by characterization results, not tested in production.				

Table 8.1-5 ESD Characteristics

Symbol	Parameter	Conditions	Value	Unit
LU	Static latch-up class	T_A +25 °C	400mA	mA
Note: 1. Guaranteed by characterization results, not tested in production.				

Table 8.1-6 Electrical Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-7 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

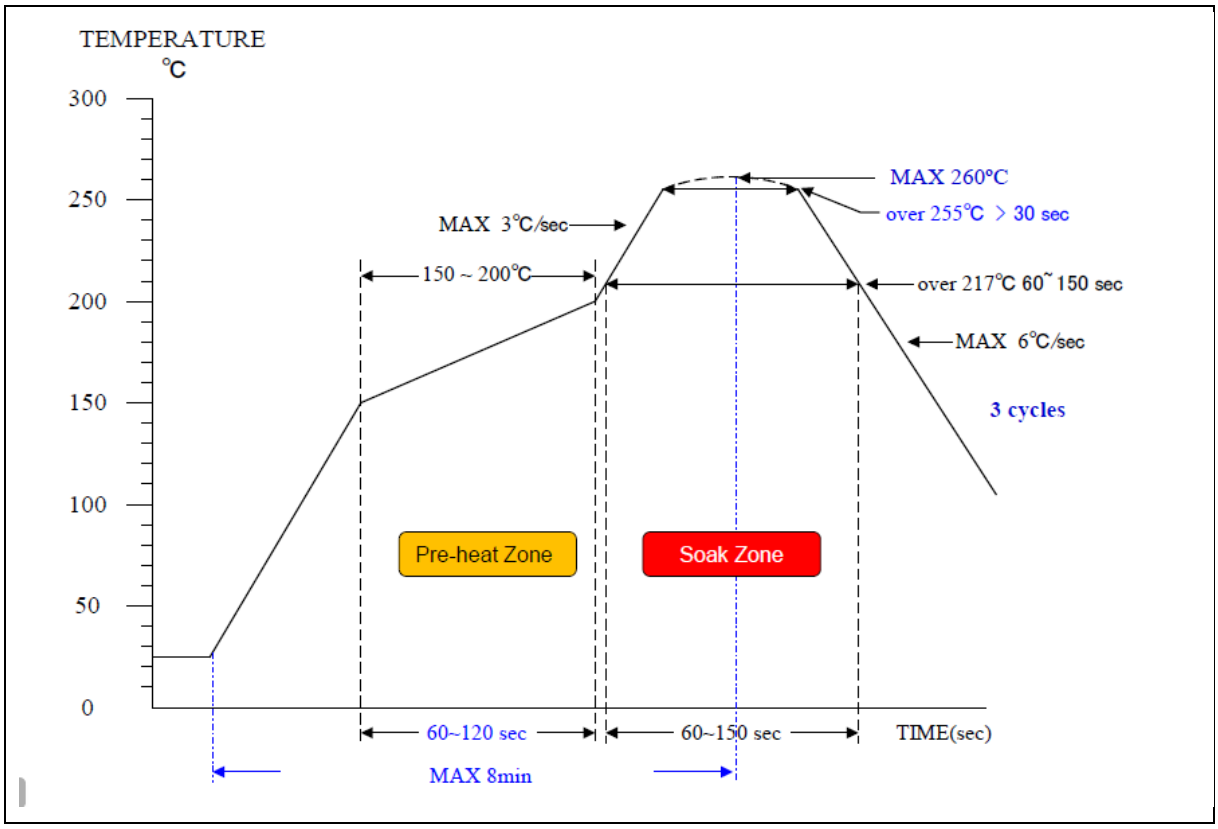


Figure 8.1-1 Soldering Profile From J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3℃/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6℃/sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-8 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.8 ~ 3.6V, T_A = 25°C, HCLK = 144 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	144	MHz	
V_{DD}	Operation voltage	1.8	-	3.6	V	
V_{DDIO}	V_{DDIO} Operation voltage	1.8	-	3.6		
V_{BAT}	V_{BAT} Operation voltage	1.8	-	3.6		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.8	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.20	-		
V_{BG}	Band-gap voltage	1.17		1.23		
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	LQFP64
		2.2			µF	LQFP48
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	0.1	-	10	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	-	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3.65	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 146 mA for 25 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.8~3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run while(1){} from Flash

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max [*1][*2]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable HIRC, PLL, HXT,LIRC or LXT clock	144 MHz	19.19	17.94	20.86	47	mA
		120 MHz	17.4	17	19.39	45.94	
		12 MHz	3.1	2.36	4.55	29.92	
		32.768 kHz	1.54	0.99	3.11	28.20	
		10 kHz	1.07	0.39	2.63	27.6	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock	144 MHz	33.93	33.65	35.84	63.83	
		120 MHz	28.53	27.99	30.41	57.68	
		12 MHz	4.63	4.14	6.13	32.02	
		32.768 kHz	1.85	1.30	3.5	28.82	
		10 kHz	1.39	0.73	3.01	28.11	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, PLL, HXT, LIRC or LXT clock	144 MHz	7.29	6.41	8.78	34.46	mA
		120 MHz	6.47	5.63	7.95	33.56	
		12 MHz	2.15	1.5	3.61	28.9	
		32.768 kHz	1.54	0.99	3.11	28.18	
		10 kHz	1.07	0.68	2.63	27.58	
	Idle mode, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock	144 MHz	23.63	22.67	25.37	51.83	
		120 MHz	20.13	19.25	21.82	48.15	
		12 MHz	3.80	3.1	5.36	30.80	
		32.768 kHz	1.88	1.31	3.49	28.74	
		10 kHz	1.39	1.01	3.01	28.12	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 10 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_DPD}	Deep Power-down mode, all peripherals disable	-	-	0.35	0.15	1.1	18.5	µA
	Deep Power-down mode, RTC enable	V	-	0.81	0.62	1.59	19	
I_{DD_SPD}	Standby Power-down mode, all peripherals disabled	-	-	1.48	0.98	3.45	404	µA
	Standby Power-down mode, RTC enable	V	-	1.95	1.46	3.95	405	
	Standby Power-down mode, RTC enable RTC with LIRC10k	-	V	1.93	1.3	4.17	406	
	Standby Power-down mode with 16 KB RAM retention:	-	-	5.89	1.6	14.15	524	
	Standby Power-down mode with 32 KB RAM retention:	-	-	10.19	2.11	25.46	814	
	Standby Power-down mode with 64 KB RAM retention:	-	-	18.35	3.19	46.86	1374	
I_{DD_LLPD}	Low leakage Power-down mode, all peripherals disabled	-	-	230	52.65	682	19161	µA
	Low leakage Power-down mode, RTC/WDT/Timer/UART enable	V	-	231	54.23	683	19270	
	Low leakage Power-down mode, RTC/WDT/Timer enable RTC/WDT/Timer with LIRC10k	-	V	230	54.16	681	19301	
	Low leakage Power-down mode, WDT/Timer use LIRC, RTC/UART use LXT	V	V	232	54.32	685	19334	
I_{DD_NPD}	Normal-Power-down mode, all peripherals disable	-	-	672	185	2062	32045	µA
	Normal-Power-down mode, WDT/Timer/UART/RTC enable	V	-	677	187	2090	32167	
	Normal-Power-down mode, WDT/Timer/UART enable RTC/WDT/Timer with LIRC10k	-	V	677	186	2091	32121	
	Normal-Power-down mode, WDT use LIRC, UART/Timer/RTC use LXT	V	V	678	187	2092	32165	
I_{DD_FWPD}	Fast wake up Power-down mode, all peripherals disable	-	-	793	291	2204	32308	µA

Symbol	Test Conditions	LXT[*1]	LIRC	Typ[*2]	Max[*3][*4]			Unit
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable	V	-	797	293	2216	32403	
	Fast wake up Power-down mode, WDT/Timer/UART enable RTC/WDT/Timer with LIRC10k	-	V	796	293	2212	32357	
	Fast wake up Power-down mode, WDT use LIRC, UART/Timer/RTC use LXT	V	V	796	293	2213	32383	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L3 gain level
2. $V_{DD} = AV_{DD} = 3.3V$.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 144 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	1166.72	µA
CRC	63.38	
USBH	858.77	
WDT	45.9	
RTC	127.59	
TMR0	361.64	
TMR1	352.25	
TMR2	314.95	
TMR3	295.1	
CLKO	84.24	
ACMP01	60.76	
I^2C0	28.94	
I^2C1	17.5	
QSPI0	575.19	
SPI0	560.07	
SPI1	595.36	
UART0	272.94	
UART1	208.76	
UART2	263.46	
UART3	170.93	
CAN0	236.13	
CAN1	216.79	
USB FS OTG	333.04	
EADC0	391.46	
I^2S0	307.91	
EPWM0	364.43	
BPWM0	363.07	
BPWM1	278.82	
QEI0	51.81	

Peripheral	I_{DD}[*1]	Unit
ECAP0	66.53	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 12 MHz HIRC oscillator.

Symbol	Parameter	Typ	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	cycles
t_{WU_FWPD}	Wakeup from Fast-wakeup power down mode	10	µs
t_{WU_PD}	Wakeup from normal power down mode	15	
t_{WU_LLPD}	Wakeup from low leakage power down mode	58	
t_{WU_SPD}	Wakeup from Standby Power-down mode	200	
t_{WU_DPD}	Deep Power-down mode (DPD)	200	

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-5 Low-power Mode Wake-up Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative Injection	Positive Injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	-		Injected current on any 5V tolerance I/O except analog input pin
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.8 V
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	1.5	-	V_{DD}		V_{DD} = 3.3 V
		0.8	-	V_{DD}		V_{DD} = 1.8 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	45	52	57	kΩ	
R_{PD}[*1]	Pull down resistor	45	52	57	kΩ	

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	6.91		7.76	µA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		6.79		7.59	µA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	16.98		17.40	mA	V_{DD} = 3.3 V V_{IN}=(V_{DD}-0.4) V
		9.85		10.19	mA	V_{DD} = 1.8 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	16.21		16.63	mA	V_{DD} = 3.3 V V_{IN}= 0.4 V
		9.59		10.41	mA	V_{DD} = 1.8 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	45	52	47	kΩ	
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	µs	Normal run and Idle mode
		-	24	-		Fast wake up Power-down mode
		75	-	155		Power-down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC48M)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} =1.8 ~ 3.6V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 1.8 ~ 3.6V
		-4[*1]	-	4[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V
I_{HRC}[*1]	Operating current	-	-	230	µA	
T_S[*2]	Stable time	-	-	20	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-148 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

The 12 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
F_{MRC}	Oscillator frequnecy	11.76	12	12.24	MHz	T_A = 25 °C, V_{DD} = 1.8 ~ 3.6V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 1.8 ~ 3.6V
		-3[*1]	-	3[*1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V
I_{MRC}[*1]	Operating current	-	-	215	µA	
T_S[*2]	Stable time	-	-	20	µs	T_A = -40°C ~ +105 °C, V_{DD} = 1.8 ~ 3.6V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.3 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	10	-	kHz	T_A = 25 °C, V_{DD} = 1.8 ~ 3.6V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 1.8 ~ 3.6V
		-10	-	10	%	T_A=-40~105°C V_{DD}=1.8V~3.6V Without software calibration
I_{LRC}	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C V_{DD}=1.8V~3.6V

Note:

1. Guaranteed by characterization, not tested in production.
2. The10 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.
4. The LIRC duty cycle is 16/84, if need 50/50 duty clock output, user should divided by 2 at least.

Table 8.4-3 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.4 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.8	-	3.6	V	
R_f	Internal feedback resister	-	1000	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	160	281	µA	4 MHz, Gain = L0
			280	417		12 MHz, Gain = L1
		-	400	540		16 MHz, Gain = L2
		-	600	690		24 Mhz, Gain = L3
T_S	Stable time	-	1300	1974	µs	4 MHz, Gain = L0
			458	605		12 MHz, Gain = L1
		-	326	439		16 MHz, Gain = L2
		-	268	414		24 Mhz, Gain = L3
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1.47	-	V	V_{DD} = 3.3V @ f_{HXT} = 12 MHz

Note:

1. Guaranteed by characterization, not tested in production.
2. Recommended crystal resonators for the HXT oscillator in M433 Series MCUs
   2.1 EPSON FA-238A 12MHz (C_L=12pF, ESR= 120 Ω), X1E000341000400
   2.2 EPSON FA-238A 16MHz (C_L=12pF, ESR= 80 Ω), X1E000341003900
   2.3 EPSON FA-238A 24MHz (C_L=12pF, ESR= 60 Ω), X1E000341014800

Table 8.4-4 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	150	Ω	Crystal @4 MHz
				50		Crystal @12 MHz
		-	-	40		Crystal @16 MHz
		-	-	40		Crystal @24 MHz

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~24 MHz High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	20 pF	20 pF	without

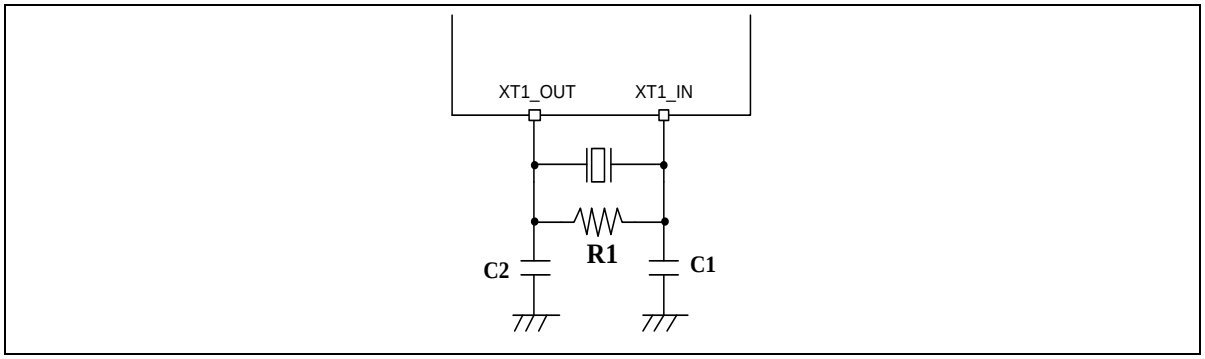
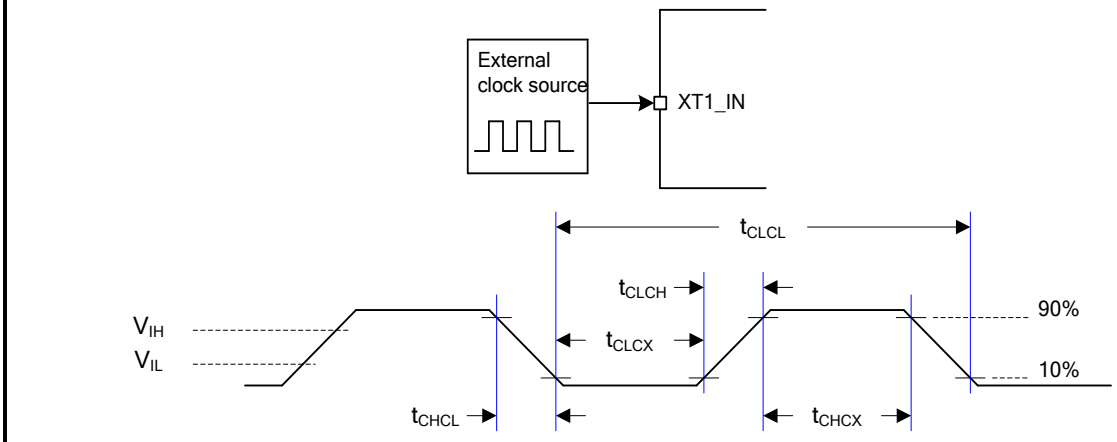


Figure 8.4-1 Typical Crystal Application Circuit

8.4.5 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the Table 8.4-6. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 4~24 MHz High Speed Clock Input Signal

8.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	1.8	-	3.6	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	0.25	0.49	µA	ESR=35 kΩ, Gain = L1
			0.42	0.8		ESR=35 kΩ, Gain = L4
		-	0.85	1.66		ESR=70 kΩ, Gain = L7
Ts_{LXT}	Stable time	-	1.5	2	s	
Du_{LXT}	Duty cycle	30	-	70	%	

Note:

1. Guaranteed by characterization, not tested in production.
2. Recommended crystal resonators for the LXT oscillator in M433 Series MCUs
   2.1 EPSON FC-13A 32.768 kHz (C_L= 12.5pF, ESR=70 kΩ), X1A000091000100

Table 8.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-8 External 32.768 kHz Low Speed Crystal Characteristics

8.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	20 pF	20 pF	without

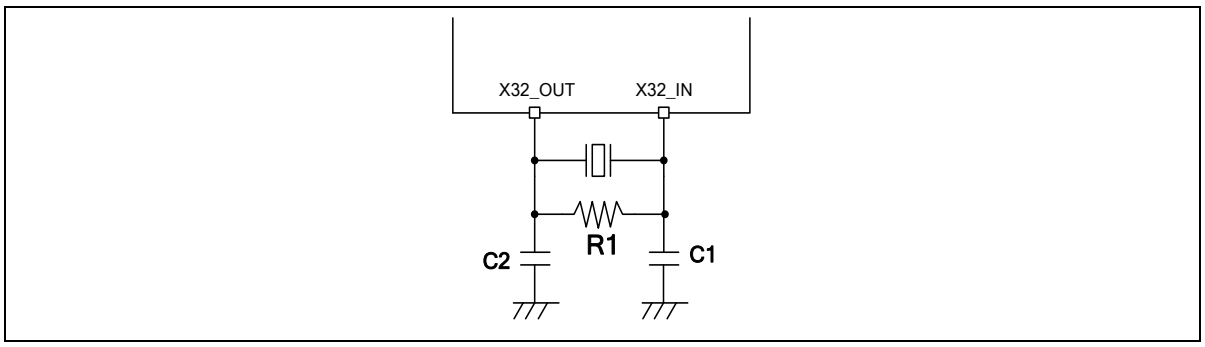
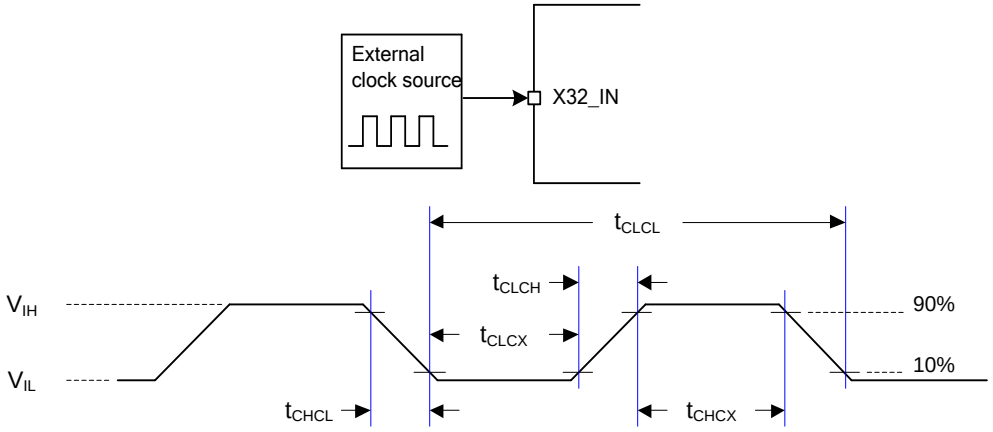


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the Table 8.4-9. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LSE_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

Table 8.4-9 External 32.768 kHz Low Speed Clock Input Signal

8.4.8 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	480	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	480	MHz	
T_L	PLL locking time	-	-	100	µs	
Jitter[*2]	Cycle-to-cycle Jitter	-	-	500	ps	
I_{DD}	Power consumption	-	3.56	4.4	mA	V_{DD}=3.3V @ f_{PLL_VCO} = 500 MHz

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-10 PLL Characteristics

8.4.9 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	3.5	ns	C_L = 30 pF, V_{DD} >= 3.6 V
		-	2		C_L = 10 pF, V_{DD} >= 3.6 V
		-	4.5		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8		C_L = 30 pF, V_{DD} >= 1.8 V
		-	5.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	3		C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.5		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3.5		C_L = 30 pF, V_{DD} >= 2.7 V
		-	2		C_L = 10 pF, V_{DD} >= 2.7 V
		-	6.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	3.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output high (90%) to low level (10%) fall time (Fast Slew Rate)	-	2.5		C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.5		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3		C_L = 30 pF, V_{DD} >= 2.7 V
		-	2		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	3.5		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	4	ns	C_L = 30 pF, V_{DD} >= 3.6 V
		-	2.5		C_L = 10 pF, V_{DD} >= 3.6 V
		-	4.5		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	8		C_L = 30 pF, V_{DD} >= 1.8 V
		-	5.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	2.5	ns	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.5		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3		C_L = 30 pF, V_{DD} >= 2.7 V
		-	2		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	3		C_L = 10 pF, V_{DD} >= 1.8 V

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
	Output low (10%) to high level (90%) rise time (Fasr Slew Rate)	-	2.5	ns	C_L = 30 pF, V_{DD} >= 3.6 V
		-	1.5		C_L = 10 pF, V_{DD} >= 3.6 V
		-	3		C_L = 30 pF, V_{DD} >= 2.7 V
		-	2		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	3		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	88.9	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	148.1		C_L = 10 pF, V_{DD} >= 3.6 V
		-	74.1		C_L = 30 pF, V_{DD} >= 2.7 V
		-	111.1		C_L = 10 pF, V_{DD} >= 2.7 V
		-	41.7		C_L = 30 pF, V_{DD} >= 1.8 V
		-	60.6		C_L = 10 pF, V_{DD} >= 1.8 V
	I/O maximum frequency (High Slew Rate)	-	121.2	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	222.2		C_L = 10 pF, V_{DD} >= 3.6 V
		-	102.6		C_L = 30 pF, V_{DD} >= 2.7 V
		-	166.7		C_L = 10 pF, V_{DD} >= 2.7 V
		-	58.0		C_L = 30 pF, V_{DD} >= 1.8 V
		-	102.6		C_L = 10 pF, V_{DD} >= 1.8 V
	I/O maximum frequency (Fastigh Slew Rate)	-	133.3	MHz	C_L = 30 pF, V_{DD} >= 3.6 V
		-	222.2		C_L = 10 pF, V_{DD} >= 3.6 V
		-	111.1		C_L = 30 pF, V_{DD} >= 2.7 V
		-	166.7		C_L = 10 pF, V_{DD} >= 2.7 V
		-	63.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	102.6		C_L = 10 pF, V_{DD} >= 1.8 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-11 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.8	-	3.6	V	
V_{LDO}	Output voltage	-	1.20	-	V	
T_A	Temperature	-40	-	105	°C	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.

8.5.2 Reset and Power Control Block Characteristics

The parameters in Table 8.5-1 are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	35	45	μA	AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	0.3	0.6		AV_{DD} = 3.6V, Normal mode
I_{BOD}[*1]	BOD operating current	-	30	40		AV_{DD} = 3.6V, Normal mode
		-	1	-		AV_{DD} = 3.6V, Low Power mode
V_{POR}	POR reset voltage	1.38	1.46	1.54	V	-
V_{LVR}	LVR reset voltage	1.45	1.50	1.55		-
V_{BOD}	BOD brown-out detect voltage (Falling edge)	1.45	1.60	1.70		BODVL = 0
		1.65	1.80	1.90		BODVL = 1
		1.85	2.00	2.10		BODVL = 2
		2.05	2.20	2.30		BODVL = 3
		2.25	2.40	2.50		BODVL = 4
		2.45	2.60	2.70		BODVL = 5
		2.65	2.80	2.90		BODVL = 6
		2.85	3.00	3.10		BODVL = 7
	BOD brown-out detect voltage (Rising edge)	1.58	1.68	1.78		BODVL = 0
		1.78	1.88	1.98		BODVL = 1
		1.98	2.08	2.18		BODVL = 2
		2.18	2.28	2.38		BODVL = 3
		2.38	2.48	2.58		BODVL = 4
		2.58	2.68	2.78		BODVL = 5
		2.78	2.88	2.98		BODVL = 6
		2.98	3.08	3.18		BODVL = 7
T_{LVR_SU}[*1]	LVR startup time	-	200	256	μs	-
T_{LVR_RE}[*1]	LVR respond time	-	1	2		Normal mode
T_{BOD_SU}[*1]	BOD startup time	-	1000	-		-
T_{BOD_RE}[*1]	BOD respond time	-	-	100		Normal mode
		-	-	12000		Low Power mode
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	μs/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		300	-	-		LVR Enabled
		666	-	-		BOD 1.6V Enabled, Normal mode

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
		285	-	-		BOD 1.8V Enabled, Normal mode
		180	-	-		BOD 2.0V Enabled, Normal mode
		133	-	-		BOD 2.2V Enabled, Normal mode
		105	-	-		BOD 2.4V Enabled, Normal mode
		85	-	-		BOD 2.6V Enabled, Normal mode
		75	-	-		BOD 2.8V Enabled, Normal mode
		65				BOD 3.0V Enabled, Normal mode

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

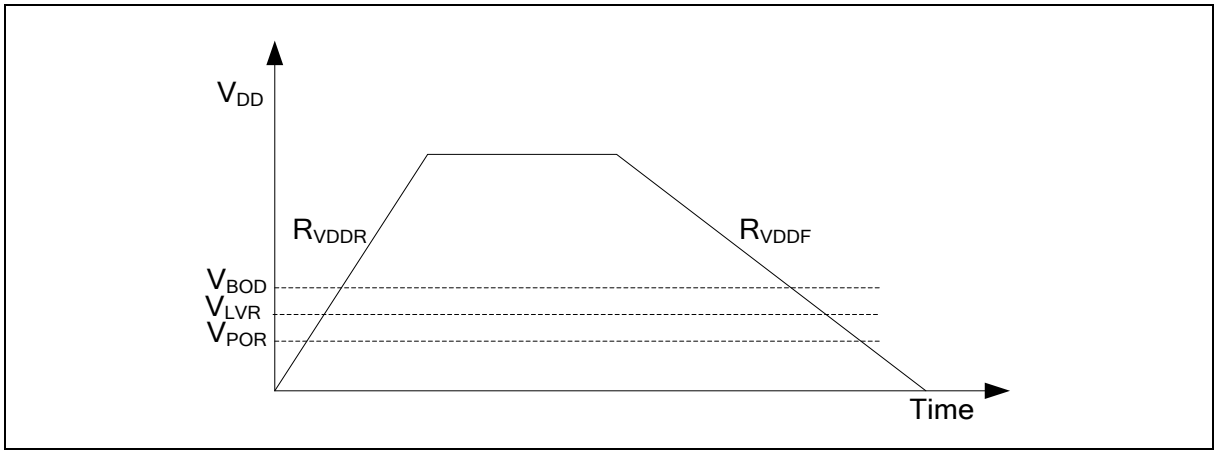


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR ADC

8.5.3.1 ADC0 Characteristics

Fast Speed Channel

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	1.8	-	3.6	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	1.6	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	599	-	629	µA	$AV_{DD} = V_{DD} = V_{REF} = 3.3V$ ADC Clock Rate = 80 MHz High speed channel
N_R	Resolution	12			Bit	
F_{ADC}	ADC Clock frequency	TBD	-	80	MHz	$F_{ADC} = 1/T_{ADC}$
T_{SMP}	Sampling Time		2		$1/F_{ADC}$	
T_{CONV}	Conversion time		14		$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 12$
F_{SPS}	Sampling Rate	TBD	-	5	MSPS	High speed channel
T_{EN}	Enable to ready time	TBD	-	-	µs	
INL	Integral Non-Linearity Error	-4.42	-	2.4	LSB	$V_{REF} = AV_{DD} = 3.3V$ package with V_{REF} pin
DNL	Differential Non-Linearity Error	-1	-	4.62	LSB	$V_{REF} = AV_{DD} = 3.3V$ package with V_{REF} pin
E_G	Gain error	0.5	-	2.06	LSB	$V_{REF} = AV_{DD} = 3.3V$ package with V_{REF} pin
E_O	Offset error	0	-	1.81	LSB	$V_{REF} = AV_{DD} = 3.3V$ package with V_{REF} pin
E_A	Absolute Error	3.69	-	6.37	LSB	$V_{REF} = AV_{DD} = 3.3V$ package with V_{REF} pin
C_{IN}[*1]	Internal Capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$

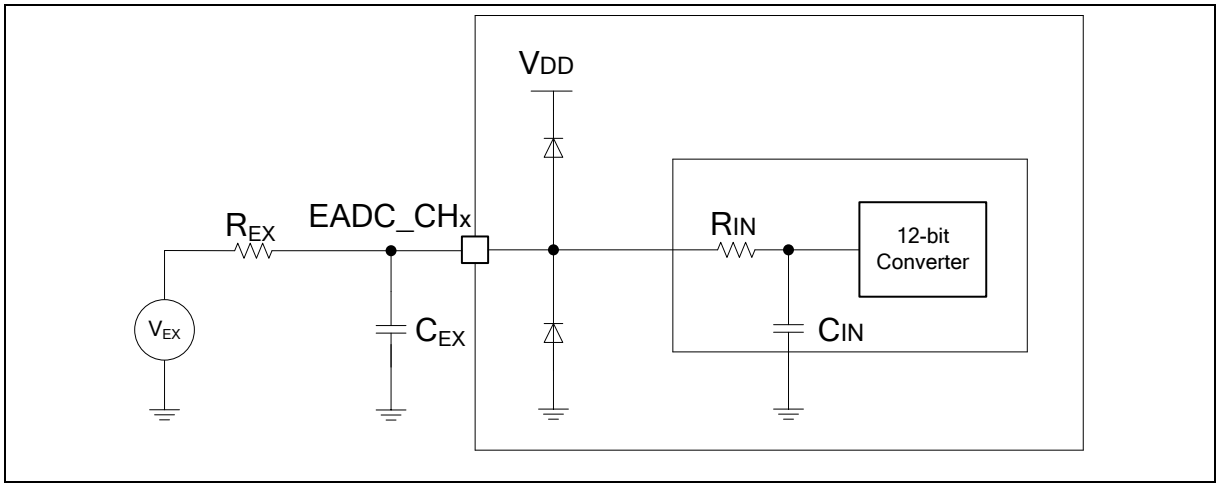
Low Speed Channel

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	1.8	-	3.6	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	1.6	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	Operating current (AV_{DD} current) (Enable ADC and disable all other analog modules)	163	-	270	µA	$AV_{DD} = V_{DD} = V_{REF}$ = 1.62V ~ 3.3V ADC Clock Rate = 32 MHz High speed channel
N_R	Resolution	12			Bit	
F_{ADC}	ADC Clock frequency	TBD	-	80	MHz	$F_{ADC} = 1/T_{ADC}$
T_{SMP}	Sampling Time		2		$1/F_{ADC}$	
T_{CONV}	Conversion time		14		$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 12$
F_{SPS}	Sampling Rate	0.1	-	2	MSPS	Low speed channel **Note:** it needs more extend sampling time to slow down the sampling rate.
T_{EN}	Enable to ready time	TBD	-	-	µs	
INL	Integral Non-Linearity Error	-2.17	-	1.89	LSB	$V_{REF} = AV_{DD}$ = 1.62V ~ 3.3V package with V_{REF} pin
DNL	Differential Non-Linearity Error	-1	-	1.87	LSB	$V_{REF} = AV_{DD}$ = 1.62V ~ 3.3V package with V_{REF} pin
E_G	Gain error	0.31	-	2.56	LSB	$V_{REF} = AV_{DD}$ = 1.62V ~ 3.3V package with V_{REF} pin
E_O	Offset error	-0.31	-	2.19	LSB	$V_{REF} = AV_{DD}$ = 1.62V ~ 3.3V package with V_{REF} pin
E_A	Absolute Error	-3.5	-	5.87	LSB	$V_{REF} = AV_{DD}$ = 1.62V ~ 3.3V package with V_{REF} pin
C_{IN}[*1]	Internal Capacitance	-	5	-	pF	

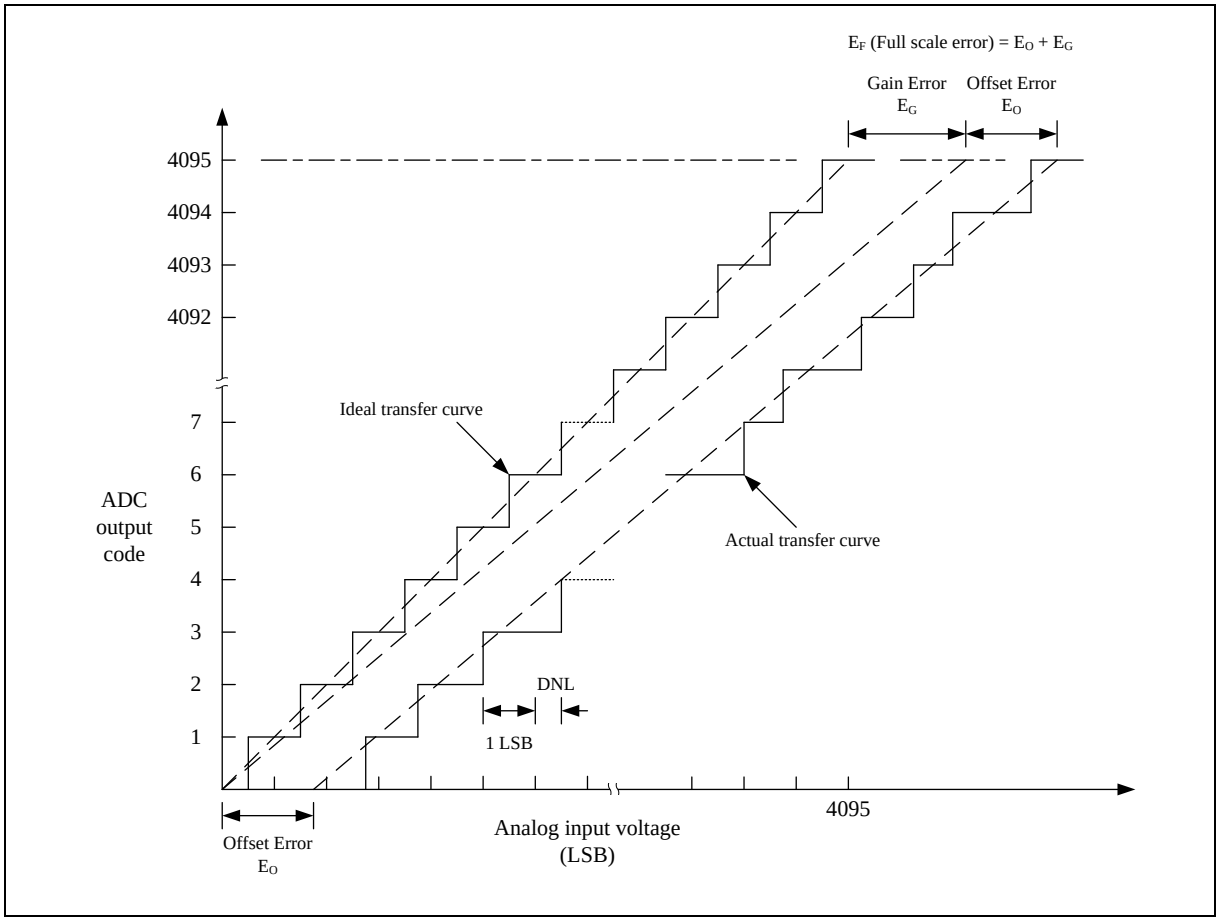
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit
V_{DD}	Operating Voltage	1.8		3.6	V
T_A	Temperature Range	-40		105	°C
I_{TEMP}	Current Consumption [*3]		16		µA
T_c	Temperature Coefficient [*3]	-1.77	-1.82	-1.84	mV/°C
V_{os}	Offset Voltage when T_A = 0°C [*3]	710.2		716.8	mV
t_S	Stable time[*2]		1		µs
T_{S_temp}	ADC sampling time when reading the temperature (5pF cap load) [*1]		3		µs

Note:

1. V_{TEMP} (mV) = T_c (mV/°C) x Temperature (°C) + V_{os} (mV)
2. Guaranteed by design, not tested in production
3. Guaranteed by characteristic, not tested in production

8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	$V_{DD} = AV_{DD}$
T_A	Temperature	-40	-	105	°C	
I_{ACMP}[*2]	ACMP operating current	-	75	90	µA	MODESEL = 11
		-	10	30		MODESEL = 10
		-	3	10		MODESEL = 01
		-	1.2	6		MODESEL = 00
V_{CM}[*2]	Input common mode voltage range	0.1	1/2 AV_{DD}	AV_{DD} -0.1		
V_{DI}[*2]	Differential input voltage sensitivity	-	10	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	5	10	mV	Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	10	20	mV	HYSSEL = 01
			20	40		HYSSEL = 10
			30	60		HYSSEL = 11
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	180	250	ns	MODESEL = 11
		-	350	600		MODESEL = 10
		-	750	2000		MODESEL = 01
		-	1600	4500		MODESEL = 00
T_{Setup}[*2]	Setup time	-	250 + T_d	450 + T_d	ns	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	AV_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	4.2	-	kΩ	
T_{SETUP_CRV}[*2]	Setup time	-	-	TBD	µs	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	32.7	-	µA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

8.5.6 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Comments
V_{REF_INT}	Internal reference voltage	1.55	1.6	1.65	V	AV_{DD} >= 2.0 V
		1.95	2.0	2.05		AV_{DD} >= 2.2 V
		2.45	2.5	2.55		AV_{DD} >= 2.7 V
		2.95	3.0	3.05		AV_{DD} >= 3.2 V
T_s[*1]	Stable time	-	0.5	0.8	ms	C_L =4.7 uF, V_{REF} initial=0
		-	9.3	13	ms	C_L =4.7 uF, V_{REF} initial=3.6
		-	24	180	us	C_L =1 uF, V_{REF} initial=0
		-	2	2.6	ms	C_L =1 uF, V_{REF} initial=3.6

Note:

1. Guaranteed by characterization, not tested in production

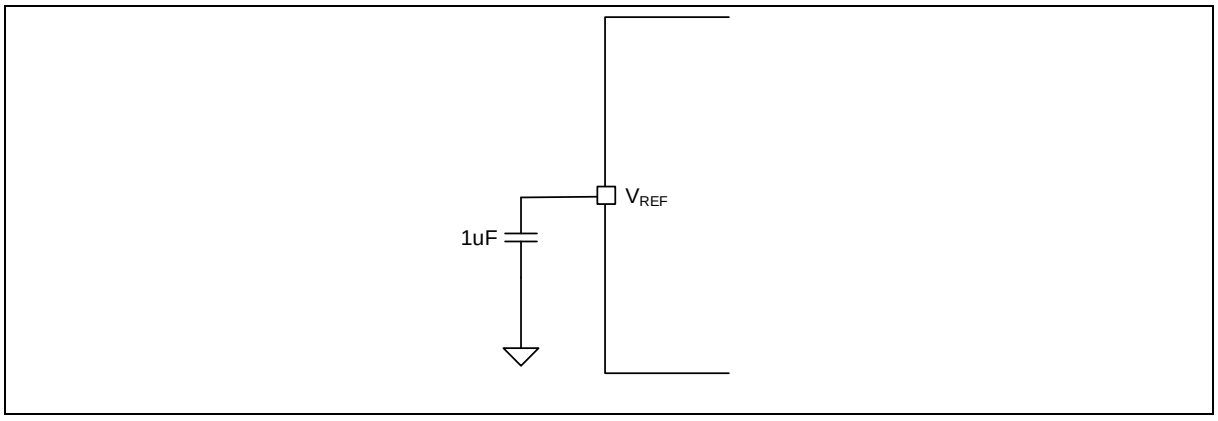


Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	72	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
				72		2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	72		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	
t_V	Data output valid time	-	-	2	ns	3.0 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
				2	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	2.2	ns	1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

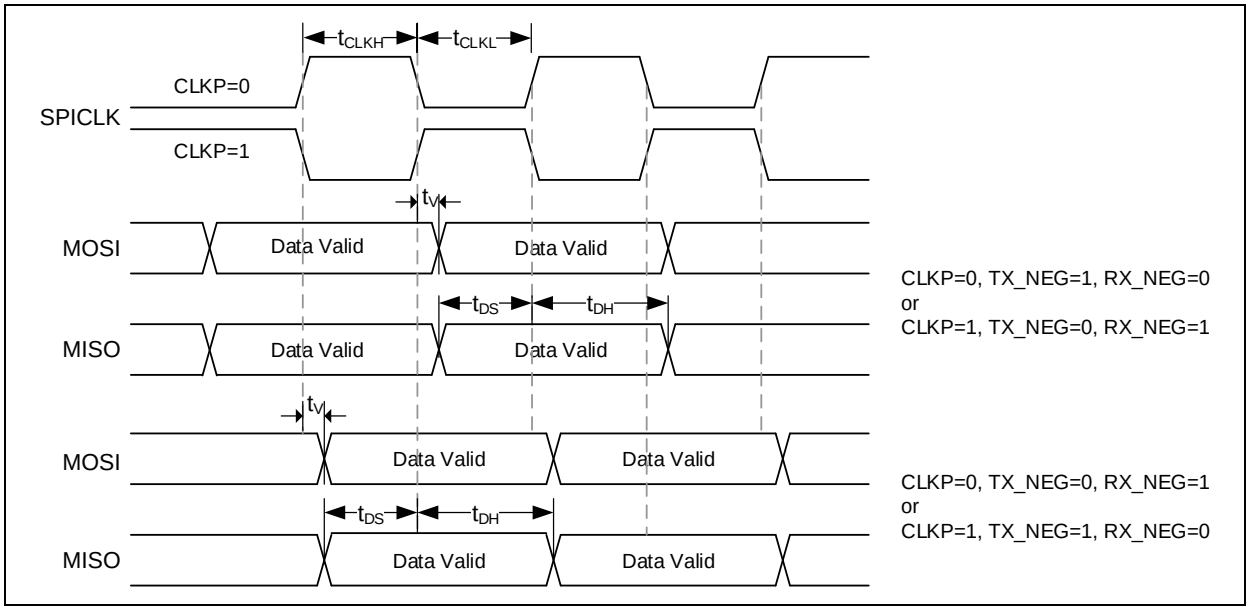


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	36	MHz	3.0 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
				36		2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	33		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	3.0 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 2ns				2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	
t_V	Data output valid time	-	-	11	ns	3.0 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
				11		2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	15		1.8 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

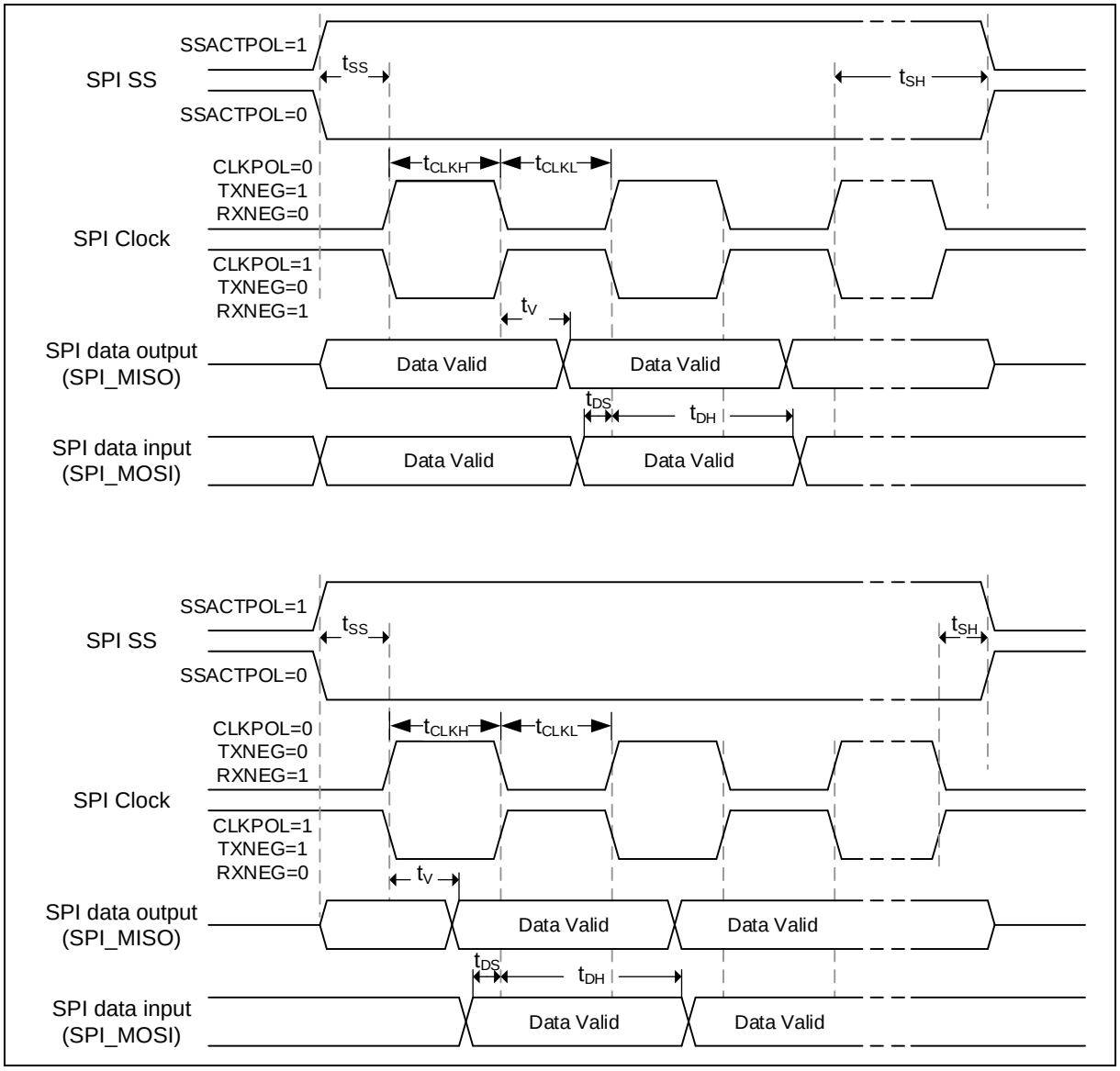


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	ns	Master f_{PCLK} = 36 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I²S Characteristics

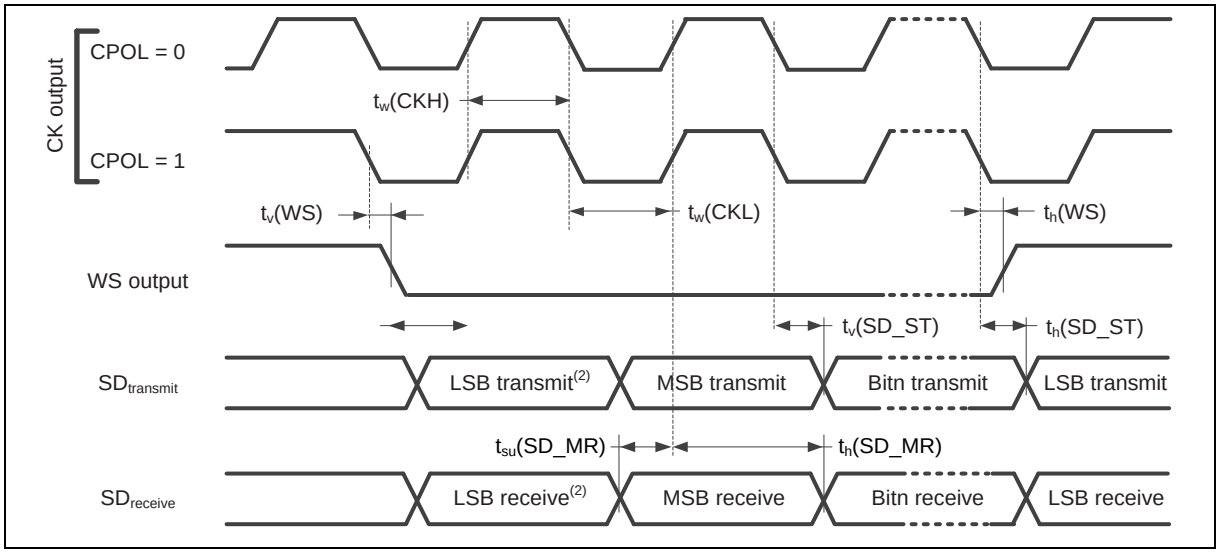


Figure 8.6-3 I²S Master Mode Timing Diagram

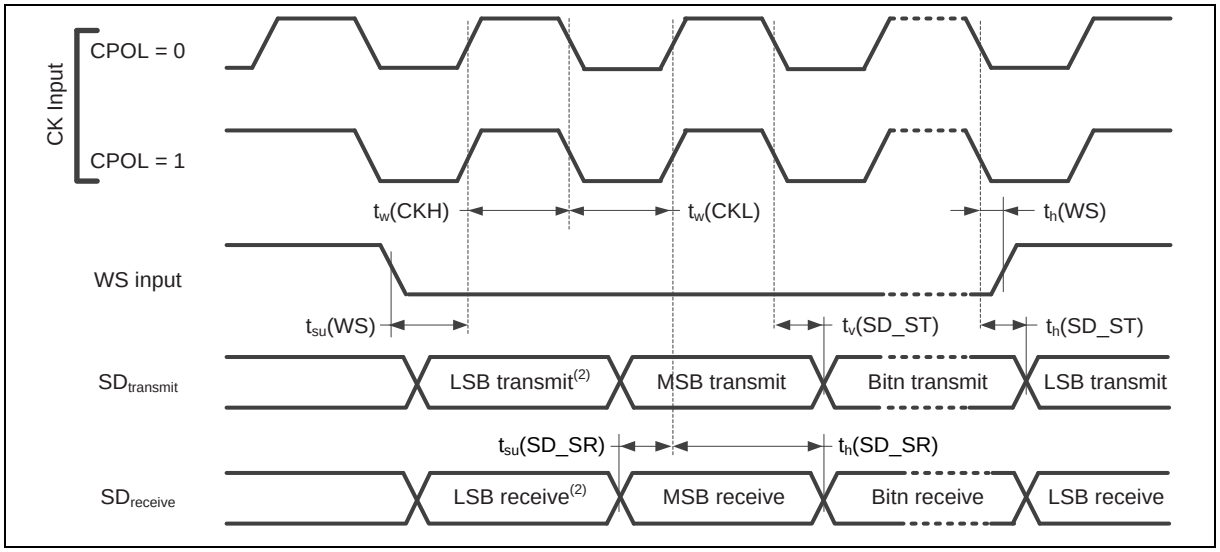


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = 36 MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	16		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-4 I²S Characteristics

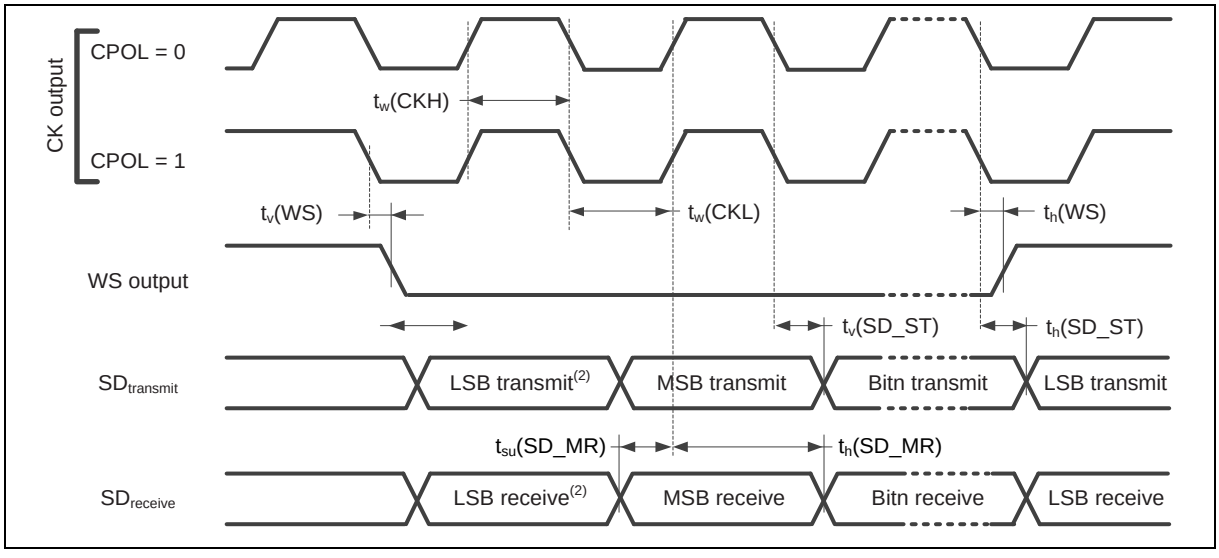


Figure 8.6-5 I²S Master Mode Timing Diagram

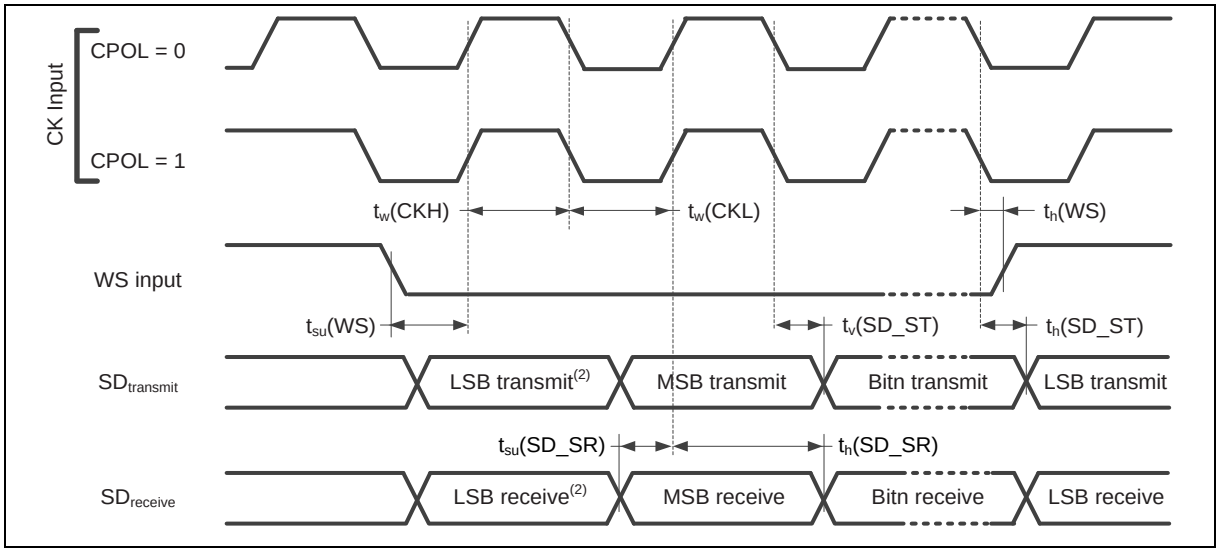


Figure 8.6-6 I²S Slave Mode Timing Diagram

8.6.4 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	µs
t_{HIGH}	SCL high period	4	-	0.6	-	µs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	µs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	µs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	µs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	µs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	µs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-5 I²C Characteristics

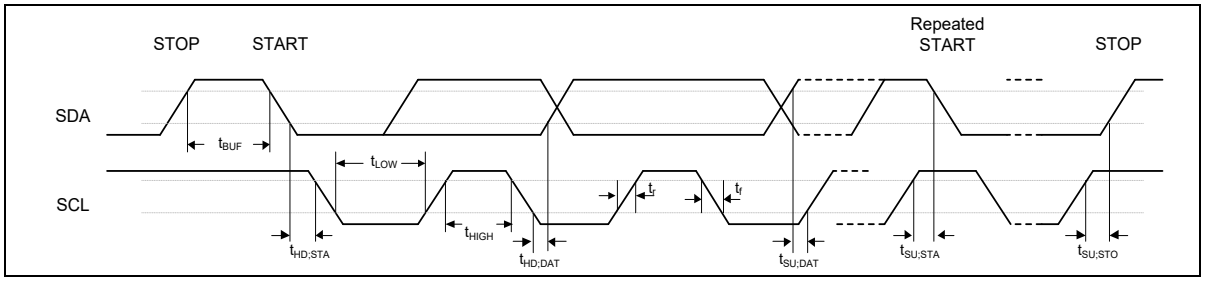


Figure 8.6-7 I²C Timing Diagram

8.6.5 USB Characteristics

8.6.5.1 USB Full-Speed Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4		5.25	V	
V_{DD}	Operation Voltage	3.0		3.6	V	
V_{IH}	Input High (driven)	2.0	-	-	V	-
V_{IL}	Input Low	-	-	0.8	V	-
V_{DI}	Differential Input Sensitivity	-	0.2	-	V	|PADP-PADM|
V_{CM}	Differential Common-mode Range	0.8	-	2.5	V	-
V_{SE}	Single-ended Receiver Threshold	0.8	-	2.0	V	-
	Receiver Hysteresis	-	200	-	mV	Single End RX
V_{OL}	Output Low (driven)	0	-	0.3	V	-
V_{OH}	Output High (driven)	2.8	-	3.6	V	-
V_{CRS}	Output Signal Cross Voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up Resistor	0.9	1.2	1.575	kΩ	DATARPU2=1
R_{PU}	Pull-up Resistor	1.425	2.3	3.09	kΩ	DATARPU2=0
R_{PD}	Pull-down Resistor	14.25	19.5	24.8	kΩ	-
V_{TRM}	TERMINATION Voltage for Uptream port pull up (RPU)	3.0	-	3.6	V	-
Z_{DRV}	Driver Output Resistance	-	10	-	Ω	-
C_{IN}	Transceiver Capacitance	-	-	26	pF	-

Table 8.6-6 USB Full-Speed Characteristics

8.6.5.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	ns	-
T_{FF}	fall time	4	-	20	ns	-
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-7 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.08	-	1.32	V	T_A = 25°C
T_{ERASE}	Page erase time	-	-	160	ms	
T_{PROG}	Program time	-	-	50	μs	
I_{DD1}	Read current	-	4.12	-	mA	
I_{DD2}	Program current	-	5	-	mA	
I_{DD3}	Erase current	-	5	-	mA	
N_{ENDUR}	Endurance	10,000	-		cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	TBD	-	-	year	10 kcycle[3] T_A = 55°C
		10	-	-	year	10 kcycle[3] T_A = 85°C
		TBD	-	-	year	10 kcycle[3] T_A = 125°C

Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
CCAP	Camera Capture Interface
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop

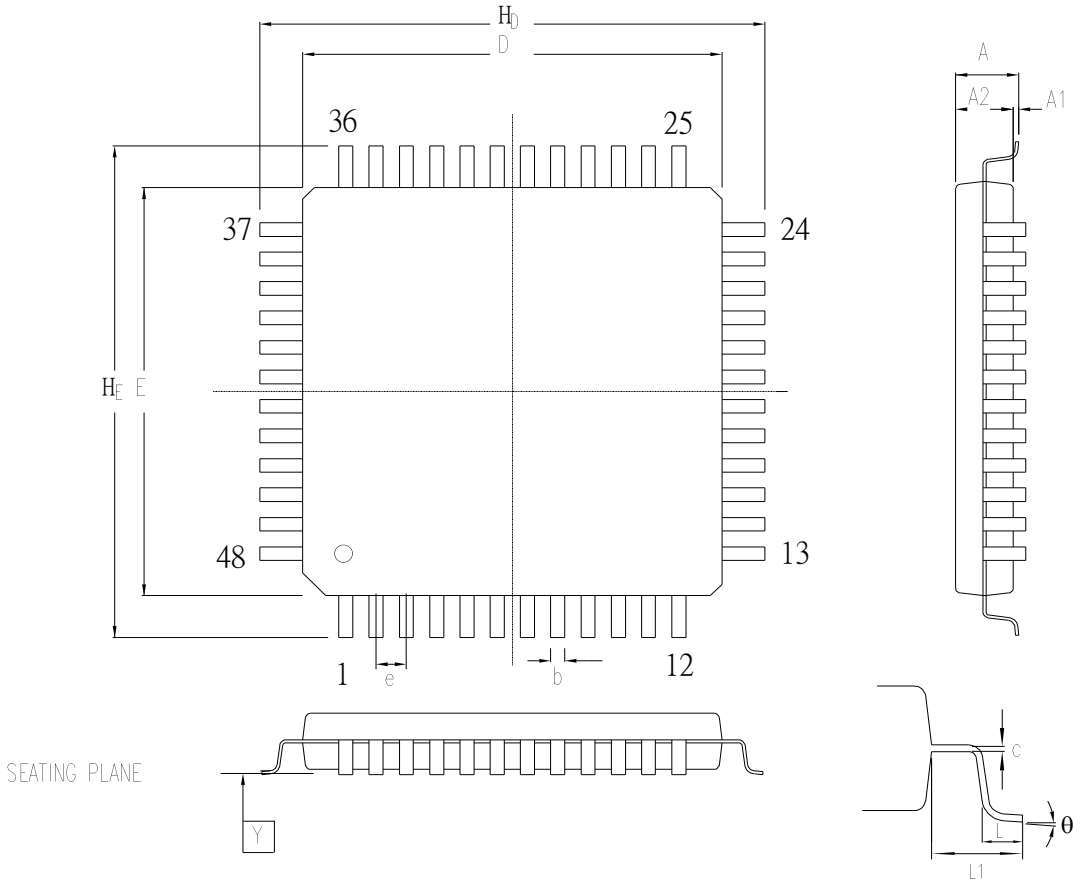
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 9.1-1 List of Abbreviations

10 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

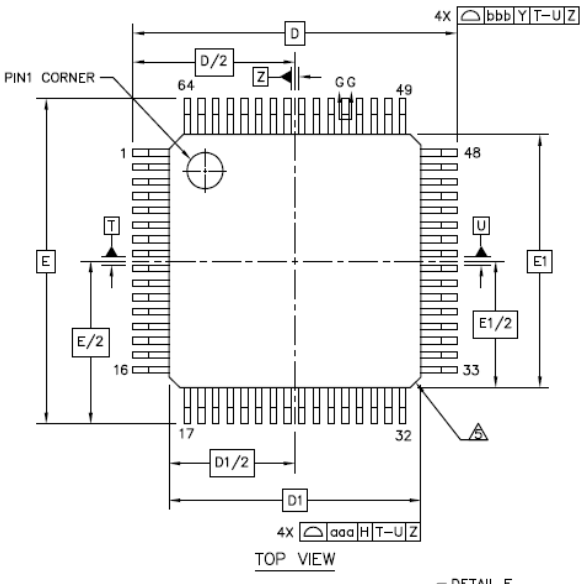
10.1 LQFP 48L (7x7x1.4 mm Footprint 2.0mm)



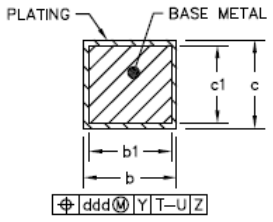
Controlling dimension : Millimeters

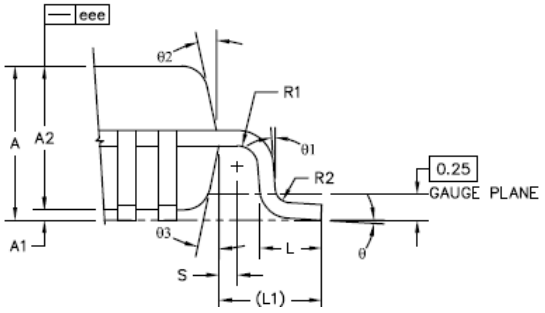
Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

10.2 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





11 REVISION HISTORY

Date	Revision	Description
2024.01.02	1.00	• Initial version.

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