NuMicro® Family

Arm® Cortex®-M33-based Microcontroller

M3351 Series
Datasheet

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TABLE OF CONTENTS

1 GENERAL DESCRIPTION 13
2 FEATURES 14
2.1 M3351 Series Features 14
3 PARTS INFORMATION 25
3.1 Package Type 25
3.1.1 M3351 Series 25
3.2 M3351 Series Naming Rule 26
3.3 M3351 Series Selection Guide 27
4 PIN CONFIGURATION 29
4.1 Pin Configuration 29
4.2 M3351 Series Pin Diagram 29
4.2.1 QFN33-Pin Diagram 29
4.2.2 LQFP48-Pin Diagram 30
4.2.3 QFN48-Pin Diagram 31
4.2.4 LQFP64-Pin Diagram 32
4.2.5 LQFP100-Pin Diagram 33
4.2.6 LQFP128-Pin Diagram 34
4.3 M3351xIC/M3351xJC Multi-function Pin Diagram 35
4.3.1 QFN48-Pin Multi-function Pin Diagram 35
4.3.2 LQFP48-Pin Multi-function Pin Diagram 41
4.3.3 LQFP64-Pin Multi-function Pin Diagram 47
4.3.4 LQFP100-Pin Multi-function Pin Diagram 55
4.3.5 LQFP128-Pin Multi-function Pin Diagram 65
4.4 M3351xG7 Multi-function Pin Diagram 77
4.4.1 QFN33-Pin Multi-function Pin Diagram 77
4.4.2 QFN48-Pin Multi-function Pin Diagram 80
4.4.3 LQFN48-Pin Multi-function Pin Diagram 83
4.4.4 LQFN64-Pin Multi-function Pin Diagram 86
4.5 Pin Mapping Table 90
4.5.1 M3351 Series Mapping Table 90
4.6 Pin Functional Description 94
4.6.1 M3351 Series Summary Function Pin Description 94
5 BLOCK DIAGRAM 103
5.1 M3351 Series Block Diagram 103
6 FUNCTIONAL DESCRIPTION 104
6.1 ARM Cortex-M33 Core 104
6.2 System Manager 106

6.2.1 Overview 106
6.2.2 System Reset 106
6.2.3 System Power Distribution 112
6.2.4 Power Modes and Wake-up Sources 113
6.2.5 Power Modes Transition 117
6.2.6 System Memory Map 118
6.2.7 Implementation defined attribution unit (IDAU) 120
6.2.8 SRAM Memory Organization 122
6.2.9 Bus Matrix 125
6.2.10 HIRC Auto Trim 127
6.2.11 Register Lock Control 127
6.2.12 Wake-up Timer (WKTMR) and Wake-up I/O (WKIO) Function 129
6.2.13 System Timer (SysTick) 130
6.2.14 Nested Vectored Interrupt Controller (NVIC) 131
6.2.15 System Control Register 166
6.3 Clock Controller 176
6.3.1 Overview 176
6.3.2 Clock Generator 178
6.3.3 System Clock and SysTick Clock 181
6.3.4 Clock Fail Detection 182
6.3.5 Peripherals Clock 182
6.3.6 Power-down Mode Clock 183
6.3.7 Clock Output 183
6.3.8 Share Registers 183
6.3.9 USB Clock Source 184
6.4 Security Configuration Unit (SCU) 185
6.4.1 Overview 185
6.4.2 Features 185
6.5 True Random Number Generator (TRNG) 186
6.5.1 Overview 186
6.5.2 Features 186
6.6 CACHE Controller (CACHE) 187
6.6.1 Overview 187
6.6.2 Features 187
6.7 External Bus Interface (EBI) 188
6.7.1 Overview 188
6.7.2 Features 188
6.8 Flash Memory Controller (FMC) 189
6.8.1 Overview 189
6.8.2 Features 189
6.9 Data Flash Memory Controller (DFMC) 190

6.9.1 Overview 190
6.9.2 Features 190
6.10 General Purpose I/O (GPIO) 191
6.10.1 Overview 191
6.10.2 Features 191
6.11 PDMA Controller (PDMA) 192
6.11.1 Overview 192
6.11.2 Features 192
6.12 Timer Controller (TMR) 193
6.12.1 Overview 193
6.12.2 Features 193
6.13 PWM Generator and Capture Timer (PWM) 195
6.13.1 Overview 195
6.13.2 Features 195
6.14 Basic PWM Generator and Capture Timer (BPWM) 197
6.14.1 Overview 197
6.14.2 Features 197
6.15 Enhanced Input Capture Timer (ECAP) 198
6.15.1 Overview 198
6.15.2 Features 198
6.16 Enhanced Quadrature Encoder Interface (EQEI) 199
6.16.1 Overview 199
6.16.2 Features 199
6.17 Watchdog Timer (WDT) 200
6.17.1 Overview 200
6.17.2 Features 200
6.18 Window Watchdog Timer (WWDT) 201
6.18.1 Overview 201
6.18.2 Features 201
6.19 Enhanced LED Light Strip Interface (ELLSI) 202
6.19.1 Overview 202
6.19.2 Features 202
6.20 Real Time Clock (RTC) 203
6.20.1 Overview 203
6.20.2 Features 203
6.21 UART Interface Controller (UART) 204
6.21.1 Overview 204
6.21.2 Features 204
6.22 I²C Serial Interface Controller (I²C) 206
6.22.1 Overview 206

6.22.2Features 206
6.23 I3C Serial Interface Controller (I3C) 207
6.23.1Overview 207
6.23.2Features 207
6.24 LED Light Strip Interface (LLSI) 208
6.24.1Overview 208
6.24.2Features 208
6.25 Serial Peripheral Interface (SPI) 209
6.25.1Overview 209
6.25.2Features 209
6.26 Quad Serial Peripheral Interface (QSPI) 210
6.26.1Overview 210
6.26.2Features 210
6.27 USCI - Universal Serial Control Interface Controller (USCI) 211
6.27.1Overview 211
6.27.2Features 211
6.28 USCI – UART Mode 212
6.28.1Overview 212
6.28.2Features 212
6.29 USCI - SPI Mode 213
6.29.1Overview 213
6.29.2Features 213
6.30 USCI - I²C Mode 215
6.30.1Overview 215
6.30.2Features 215
6.31 USB 1.1 Device Controller (USBD) 216
6.31.1Overview 216
6.31.2Features 216
6.32 USB 1.1 Host Controller (USBH) 217
6.32.1Overview 217
6.32.2Features 217
6.33 Controller Area Network with Flexible DataRate (CAN FD) 218
6.33.1Overview 218
6.33.2Features 218
6.34 CRC Controller (CRC) 219
6.34.1Overview 219
6.34.2Features 219
6.35 Enhanced 12-bit Analog-to-Digital Converter (EADC0) 220
6.35.1Overview 220
6.35.2Features 220

6.36 Enhanced 14-bit Analog-to-Digital Converter (EADC1) 222
6.36.1 Overview 222
6.36.2 Features 222
6.37 Digital to Analog Converter (DAC) 223
6.37.1 Overview 223
6.37.2 Features 223
6.38 Analog Comparator Controller (ACMP) 224
6.38.1 Overview 224
6.38.2 Features 224
6.39 Cryptographic Accelerator (CRYPTO) 225
6.39.1 Overview 225
6.39.2 Features 225
6.40 Peripherals Interconnection 226
6.40.1 Overview 226
6.40.2 Peripherals Interconnect Matrix Table 226
7 APPLICATION CIRCUIT 227
7.1 Power Supply Scheme 227
7.2 Peripheral Application Scheme 228
7.3 USB Dual Role Application Scheme 229
8 ELECTRICAL CHARACTERISTICS 230
8.1 Absolute Maximum Ratings 230
8.1.1 Voltage Characteristics 230
8.1.2 Current Characteristics 231
8.1.3 Thermal Characteristics 232
8.1.4 EMC Characteristics 233
8.1.5 Package Moisture Sensitivity(MSL) 233
8.1.6 Soldering Profile 235
8.2 General Operating Conditions 236
8.3 DC Electrical Characteristics 237
8.3.1 Supply Current Characteristics 237
8.3.2 On-Chip Peripheral Current Consumption 243
8.3.3 Wakeup Time from Low-Power Modes 246
8.3.4 I/O Current Injection Characteristics 247
8.3.5 I/O DC Characteristics 247
8.4 AC Electrical Characteristics 251
8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC) 251
8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC) 252
8.4.3 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics 253

8.4.4 External 4~32 MHz High Speed Clock Input Signal Characteristics 256
8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics 257
8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics 259
8.4.7 PLL Characteristics 260
8.4.8 I/O AC Characteristics 261
8.5 Analog Characteristics 263
8.5.1 LDO Characteristics 263
8.5.2 Reset and Power Control Block Characteristics 263
8.5.3 12-bit SAR Analog To Digital Converter (ADC) 265
8.5.4 14-bit SAR Analog To Digital Converter (ADC) 268
8.5.5 Digital to Analog Converter (DAC) 270
8.5.6 Analog Comparator (ACMP) 273
8.5.7 Internal Voltage Reference 274
8.5.8 Temperature Sensor 275
8.6 Communications Characteristics 276
8.6.1 SPI Dynamic Characteristics 276
8.6.2 SPI - I²S Dynamic Characteristics 279
8.6.3 I²C Dynamic Characteristics 281
8.6.4 I3C Dynamic Characteristics 282
8.6.5 USCI - SPI Dynamic Characteristics 283
8.6.6 USCI-I²C Dynamic Characteristics 286
8.6.7 CAN Characteristics 287
8.6.8 USB Characteristics 288
8.7 Flash DC Electrical Characteristics 290
9 PACKAGE DIMENSIONS 291
9.1 QFN 33L (5x5x0.8 mm, Pitch 0.5 mm, Lead Length 0.4 mm) 291
9.2 QFN 48L (5x5x0.8 mm, Pitch 0.35 mm, Lead Length 0.4 mm) 292
9.3 LQFP 48L (7x7x1.4 mm, Footprint 2.0mm) 293
9.4 LQFP 64L (7x7x1.4 mm, Footprint 2.0 mm) 294
9.5 LQFP 100L (14x14x1.4 mm, Footprint 2.0 mm) 295
9.6 LQFP 128L (14x14x1.4 mm, Footprint 2.0 mm) 296
10 ABBREVIATIONS 297
10.1 Abbreviations 297
11 REVISION HISTORY 299

LIST OF FIGURES

Figure 4.2-1 QFN33-Pin Diagram 29
Figure 4.2-2 LQFN48-Pin Diagram 30

Figure 4.2-3 QFN48-Pin Diagram 31
Figure 4.2-4 LQFP64-Pin Diagram 32
Figure 4.2-5 LQFN100-Pin Diagram 33
Figure 4.2-6 LQFP48-Pin Diagram 34
Figure 4.3-1 M3351YICAE Multi-function Pin Diagram 35
Figure 4.3-2 M3351YJCAE Multi-function Pin Diagram 38
Figure 4.3-3 M3351LICAE Multi-function Pin Diagram 41
Figure 4.3-4 M3351LJCAE Multi-function Pin Diagram 44
Figure 4.3-5 M3351SICAE Multi-function Pin Diagram 47
Figure 4.3-6 M3351SJCAE Multi-function Pin Diagram 51
Figure 4.3-7 M3351VICAE Multi-function Pin Diagram 55
Figure 4.3-8 M3351VJCAE Multi-function Pin Diagram 60
Figure 4.3-9 M3351KICAE Multi-function Pin Diagram 65
Figure 4.3-10 M3351KJCAE Multi-function Pin Diagram 71
Figure 4.4-1 M3351ZG7AE Multi-function Pin Diagram 77
Figure 4.4-2 M3351YG7AE Multi-function Pin Diagram 80
Figure 4.4-3 M3351LG7AE Multi-function Pin Diagram 83
Figure 4.4-4 M3351SG7AE Multi-function Pin Diagram 86
Figure 5.1-1 M3351 Series Block Diagram 103
Figure 6.1-1 Cortex-M33 Block Diagram 104
Figure 6.2-1 System Reset Sources 107
Figure 6.2-2 Reset Event State Machine 107
Figure 6.2-3 nRESET Reset Waveform 109
Figure 6.2-4 Power-on Reset (POR) Waveform 110
Figure 6.2-5 Low Voltage Reset (LVR) Waveform 110
Figure 6.2-6 Brown-out Detector (BOD) Waveform 111
Figure 6.2-7 NuMicro M3351 Series Power Distribution Diagram 113
Figure 6.2-8 Power Mode State Machine 115
Figure 6.2-9 NuMicro M3351 Power Transition Graph 118
Figure 6.2-10 IDAU Memory Map 121
Figure 6.2-11 System Block Diagram 122
Figure 6.2-12 SRAM Block Diagram 123
Figure 6.2-13 SRAM Memory Organization for 48 Kbytes Device 124
Figure 6.2-14 SRAM Memory Organization for 128 Kbytes Device 125
Figure 6.2-15 NuMicro M3351 Bus Matrix Diagram 127
Figure 6.2-16 NMI Interrupt Structure 138
Figure 6.3-1 Clock Generator Global View Diagram (1/2) 177
Figure 6.3-2 Clock Generator Global View Diagram (2/2) 178

Figure 6.3-3 Clock Generator Block Diagram 180
Figure 6.3-4 System Clock Block Diagrams 181
Figure 6.3-5 SysTick Clock Control Block Diagram 181
Figure 6.3-6 HXT Stop Protect Procedure 182
Figure 6.3-7 Clock Output Block Diagram 183
Figure 6.3-8 USB Clock Source 184
Figure 6.29-1 SPI Master Mode Application Block Diagram 213
Figure 6.29-2 SPI Slave Mode Application Block Diagram 213
Figure 6.30-1 I²C Bus Timing 215
Figure 8.1-1 Soldering Profile from J-STD-020C 235
Figure 8.4-1 Typical Crystal Application Circuit 255
Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit 258
Figure 8.5-1 Power Ramp Up/Down Condition 264
Figure 8.5-2 Typical Connection with Internal Voltage Reference 274
Figure 8.6-1 SPI Master Mode Timing Diagram 276
Figure 8.6-2 SPI Slave Mode Timing Diagram 278
Figure 8.6-3 I²S Master Mode Timing Diagram 279
Figure 8.6-4 I²S Slave Mode Timing Diagram 280
Figure 8.6-5 I²C Timing Diagram 281
Figure 8.6-6 I3C Timing Diagram 283
Figure 8.6-7 USCI-SPI Master Mode Timing Diagram 283
Figure 8.6-8 USCI-SPI Slave Mode Timing Diagram 285
Figure 8.6-9 USCI-I²C Timing Diagram 286

LIST OF TABLE

Table 1-1 NuMicro M3351 Series Key Features Support Table 13
Table 4.3-1 M3351YICAE Multi-function Pin Table 37
Table 4.3-2 M3351YJCAE Multi-function Pin Table 40
Table 4.3-3 M3351LICAE/ M3351LJCAE Multi-function Pin Table 43
Table 4.3-4 M3351LJCAE Multi-function Pin Table 46
Table 4.3-5 M3351SICAE Multi-function Pin Table 50
Table 4.3-6 M3351SJCAE Multi-function Pin Table 54
Table 4.3-7 M3351VICAE Multi-function Pin Table 59
Table 4.3-8 M3351VJCAE Multi-function Pin Table 64
Table 4.3-9 M3351KICAE Multi-function Pin Table 70
Table 4.3-10 M3351KJCAE Multi-function Pin Table 76
Table 4.4-1 M3351YG7AE Multi-function Pin Table 79
Table 4.4-2 M3351YG7AE Multi-function Pin Table 82
Table 4.4-3 M3351YG7AE Multi-function Pin Table 85
Table 4.4-4 M3351YG7AE Multi-function Pin Table 89
Table 6.2-1 Reset Value of Registers 109
Table 6.2-2 Power Mode Table 114
Table 6.2-3 Power Mode Difference Table 114
Table 6.2-4 Power Mode Definition Table 115
Table 6.2-5 Clocks in Power Modes 116
Table 6.2-6 Re-Entering Power-down Mode Condition 117
Table 6.2-7 Address Space Assignments for On-Chip Controllers 120
Table 6.2-8 Exception Model 132
Table 6.2-9 Interrupt Number Table 136
Table 6.2-10 NMIMSEL Mapping Table 138
Table 6.3-1 Clock Stable Count Value Table 179
Table 6.3-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table 179
Table 6.3-3 Clock Controller Share Register List 184
Table 6.6-1 CACHE Features 187
Table 6.21-1 M3351 Series UART Features 205
Table 6.40-1 Peripherals Interconnect Matrix Table 226
Table 8.1-1 Voltage Characteristics 230
Table 8.1-2 Current Characteristics 231
Table 8.1-3 Thermal Characteristics 232
Table 8.1-4 EMC Characteristics 233
Table 8.1-5 Package Moisture Sensitivity(MSL) 234

Table 8.1-6 Soldering Profile 235
Table 8.2-1 General Operating Conditions 236
Table 8.3-1 Current Consumption in Normal Run Mode 238
Table 8.3-2 Current Consumption in Idle Mode 239
Table 8.3-3 Chip Current Consumption in Power-down Mode 241
Table 8.3-4 SRAM Static Current Consumption in Power-down Mode 242
Table 8.3-5 Peripheral Current Consumption 245
Table 8.3-6 Low-power Mode Wakeup Timings 246
Table 8.3-7 I/O Current Injection Characteristics 247
Table 8.3-8 I/O Input Characteristics 248
Table 8.3-9 I/O Output Characteristics 249
Table 8.3-10 PA0/1/4/5 Additional PMOS/NMOS Output Characteristics 250
Table 8.3-11 nRESET Input Characteristics 250
Table 8.4-1 48 MHz Internal High Speed RC Oscillator (HIRC) Characteristics 251
Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator (LIRC) Characteristics 252
Table 8.4-3 External 4~32 MHz High Speed Crystal (HXT) Oscillator 253
Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics 254
Table 8.4-5 External 4~32 MHz High Speed Clock Input Signal 256
Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator 257
Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics 258
Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal 259
Table 8.4-9 PLL Characteristics 260
Table 8.4-10 I/O AC Characteristics 262
Table 8.5-1 LDO Characteristics 263
Table 8.5-2 Reset and Power Control Unit 264
Table 8.5-3 ADC Characteristics 266
Table 8.5-3 ADC Characteristics 269
Table 8.5-4 DAC Characteristics 272
Table 8.5-5 ACMP Characteristics 273
Table 8.5-6 Internal V_{REF} Characteristics 274
Table 8.5-7 Temperature Sensor Characteristics 275
Table 8.6-1 SPI Master Mode Characteristics 276
Table 8.6-2 SPI Slave Mode Characteristics 277
Table 8.6-3 I^2S Characteristics 279
Table 8.6-4 I^2C Characteristics 281
Table 8.6-5 I3C Characteristics 282
Table 8.6-6 USCI-SPI Master Mode Characteristics 283
Table 8.6-7 USCI-SPI Slave Mode Characteristics 284

Table 8.6-8 USCI-I²C Characteristics 286
Table 8.6-9 CAN Characteristics..... 287
Table 8.6-10 USB Full-Speed Characteristics 288
Table 8.6-11 USB Full-Speed PHY Characteristics..... 289
Table 8.7-1 Flash DC Electrical Characteristics 290
Table 10.1-1 List of Abbreviations..... 298

1 GENERAL DESCRIPTION

The NuMicro M3351 series is the high-performance microcontroller with strong noise tolerance for 5V Power supply. Based on Arm Cortex-M33 core, this series features a comprehensive DSP instruction set and a single-precision floating-point unit (FPU), making it ideal for demanding computational tasks. The M3351 series runs up to 144 MHz and features 256 Kbytes to 1 Mbyte Flash memory, 48 Kbytes to 128 Kbytes SRAM, 2.7V to 5.5V operating voltage, -40°C to +105°C wide operating temperature and excellent high immunity characteristics by ESD HBM 4 kV and EFT 4.4 kV, making the series ideal for expanding the functionality of home appliances and industrial equipment.

The M3351 series offers up to 1024 Kbytes dual-bank Flash memory with ECC check, which supports background and SWAP operations and enables firmware updates through the Over-The-Air (FOTA) process. Additionally, the M3351 series features 64 Kbytes independent Data Flash, so users can execute instructions executed in Flash memory while writing Data Flash.. To reduce the data access overhead of CPU core to peripherals, a peripheral direct memory access (PDMA) with up to 12 channels is provided.

Security is another pivotal consideration for the M3351 series, featuring advanced security features such as secure boot, Arm TrustZone, PRNG,TRNG, AES/SHA/HMAC-SHA cryptography accelerators.

The M3351 series also provides a wide array of communication and peripheral interfaces, including up to 10 sets of UART, 1 set of EBI, 1 set of USB 2.0 full speed Device/Host, 3 sets of I^2C, 1 set of I3C, 2 sets of CAN FD, 1 set of QSPI, 1 set of SPI/I2S, 1 set of SPI , 2 sets of Universal Serial Control Interfaces (USCI), supporting up to 10 channels of LED Light Strip Interface (LLSI) and 2 channels of Enhanced LED Light Strip Interface (ELLSI).

For analog and control functions, the M3351 series implements up to 24 channels of 16-bit PWM, 4 sets of 32-bit timers, 2 sets of analog comparators with 5 input pins and 8-bit DAC as internal reference, up to 1 set of 12-bit DAC, 1 set of 12-bit SAR ADC with total up to 24 channels, and 1 set of 14-bit SAR ADC with total up to 16 channels.

For the development, Nuvoton provides the NuMaker-M3351KJ evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK Nuvoton Edition, IAR EWARM, VS Code compilers are also supported.

Product Line	Secure Boot	I3C	USB FS	PWM	BPWM	CAN FD	ELLSI	LLSI	*USCI	UART	I^2C	SPI/ I^2S	SPI	QSPI	EBI
M3351 Series	√	1	1	12	12	2	2	10	2	10	3	1	1	1	√
*USCI can be configured as UART/I^2C/SPI															

Table 1-1 NuMicro M3351 Series Key Features Support Table

The M3351 series supports five package choices which are designed for home appliance PCB demands.

- QFN33: 5mm x 5mm, Lead pitch 0.4 mm
- QFN48: 5mm x 5mm, Lead pitch: 0.35mm
- LQFP48: 7mm x7mm, Lead pitch: 0.5mm
- LQFP64: 7mm x7mm, Lead pitch: 0.4mm
- LQFP100: 14mm x 14mm, Lead pitch: 0.5mm
- LQFP128: 14mm x 14mm, Lead Pitch 0.4mm

The M3351 series is suitable for a wide range of applications such as:

- Gateway market such as CAN FD converter
- Industrial market such as firefighting system
- Consumer market such as label printer

2 FEATURES

2.1 M3351 Series Features

Core and System	
Arm Cortex-M33 with TrustZone	• Arm Cortex-M33 processor, running up to 144 MHz • Built-in Memory Protection Unit (MPU) • 8 Security Attribution Unit (SAU) memory regions • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports XOM feature with 2 regions • Supports DSP instruction set
Low power mode and current	• Low Power mode: – Idle mode • Power-down mode: – Normal Power-down mode 0 (NPD0) – Normal Power-down mode 1 (NPD1) – Normal Power-down mode 2 (NPD2) – Standby Power-down mode 0 (SPD0) – Standby Power-down mode 1 (SPD1)
Power supply and low voltage detect	• Built-in LDO for wide operating voltage from 2.7V to 5.5V • Core power voltage: 0.9 ~ 1.21V • Brown-out detector – With 3 levels: 4.4V/3.7V/2.7V – Supports Brown-out Interrupt and Reset option • Low Voltage Reset (LVR) with 2.5V threshold voltage level
Cyclic Redundancy Calculation Unit	• Supports four common polynomials CRC-8, CRC-16, and CRC-32 • Programmable seed value • Supports programmable order reverse setting for input data and CRC checksum • Supports programmable 1's complement setting for input data and CRC checksum • Supports 8/16/32-bit of data width • 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC • Supports Master mode
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)

Memories	
Boot Loader	• Factory pre-loaded mask ROM for secure boot procedure and ISP procedure • Uses SHA-256 and ECDSA-P256 to validate data in APROM and LDROM • NuMicro ISP Programming Tool for firmware upgrade via UART, CAN FD, SPI, I²C and Full speed USB device
Flash	• Up to 1024 Kbytes on-chip Application ROM (APROM) • 16 Kbytes on-chip Flash for user-defined loader (LDROM) • 16 Kbytes Data Flash0 • Dual bank 512 Kbytes APROM for Over-The-Air (OTA) upgrade • Four eXecute-Only-Memory (XOM) regions for code protection • Embedded with 8 Kbytes cache, with performance at zero wait cycle in continuous address read access • Independent 64 Kbytes Data Flash1 for 100K endurance times • All on-chip Flash support 8 Kbytes page erase • Fast Flash programming verification with CRC32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • Supports 64-bit multi-word Flash programming function
SRAM	• Up to 128 Kbytes on-chip SRAM includes: – 64 Kbytes SRAM located in bank 0 with programmable size of SPD retention and supports hardware one bit correction and two bits error detect ECC check; Exception (NMI) generated upon a ECC error – 64 Kbytes SRAM located in bank 1 with programmable size of SPD retention and supports hardware one bit correction and two bits error detect ECC check; Exception (NMI) generated upon a ECC error – Supports byte-, half-word- and word-access – PDMA operation
Peripheral DMA (PDMA)	• Up to 12 independent and configurable channels for automatic data transfer between memories and peripherals • Selectable 2 level of priority (fixed priority or round-robin priority) • Supports transfer data width of 8, 16, and 32 bits • Supports source and destination address increment size can be byte, half-word, word or no increment • Supports software and USB, UART, USCI, SPI, QSPI, ACMP, EINT, PWM, I²C, I3C, Timer, LLSI, ELLSI, EADC and DAC request • Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table • Supports single and burst transfer type
Clocks	
External Clock Source	• Built-in 4~32 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation

	• Built-in 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• Built-in 48 MHz High-speed Internal RC oscillator (HIRC48) for crystal-less USB • Built-in 38 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Supports one PLL up to 144 MHz for high performance system operation, sourced from HIRC and HXT
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter • Independent clock source for each timer • Provides one-shot, periodic, toggle-output and continuous counting operation modes • 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0]) • Supports event counting function • Supports 3-bit capture input noise filter • 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0]) • Supports external capture pin event for interval measurement • Supports external capture pin event to reset 24-bit up counter • Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event • Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, BPWM, EADC, DAC,EQEI and PDMA function • Supports internal capture triggered while internal ACMP output signal transition • Supports Inter-Timer trigger mode • Supports event counting source from ACMP or internal USB SOF signal • Supports internal capture triggered source from ACMP output, HXT, HIRC, LIRC and LXT **PWM** • Supports PWM generator with two selectable output channels • Supports 16-bit PWM counter: – Up count operation type – One-shot or auto-reload counter operation mode • Supports 8-bit prescale from 1 to 256 • Supports 16-bit compare register and period register and double buffer for period register and compare register • Supports tri-state enable and polarity control for each PWM selectable output channels • Supports interrupt on the following events: – PWM period point, up-count compared point events • Supports wake-up when interrupt occurs when clock source is LXT or LIRC • PWM can generate output in Power-down mode • Supports trigger EADC, PDMA, and DAC on the following events:

	– PWM period point and up-count compared point events • Supports PWM output accumulator event to trigger PDMA transfer and EADC • Supports PWM output accumulator event to stop PWM counting
PWM (PWM)	• Supports up to two PWM modules, each module provides 6 output channels • Supports independent mode for PWM output/Capture input channel • Supports complementary mode for 3 complementary paired PWM output channel – Dead-time insertion with 12-bit resolution – Two compared values during one period • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution PWM counter – Up, down and up/down counter operation type • Supports mask function and tri-state enable for each PWM pin • Supports brake function – Brake source from pin, analog comparator, EADC result monitor – Edge detect brake source to control brake state until brake interrupt cleared – Level detect brake source to auto recover function after brake condition removed • Supports interrupt on the following events: – PWM counter matches 0, period value or compared value – Brake condition happened • Supports trigger EADC on the following events: – PWM counter matches 0, period value or compared value • Supports PDMA transfer for Interrupt Flag Accumulator Function • Supports PWM output accumulator stop counter mode • Supports External Pin Trigger Function
Basic PWM (BPWM)	• Supports up to two BPWM modules; each module provides 6 output channels • Supports independent mode for BPWM output/Capture input channel • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter – Up, down and up/down counter operation type • Supports mask function and tri-state enable for each BPWM pin • Supports interrupt in the following events: – BPWM counter matches 0, period value or compared value • Supports trigger EADC in the following events: – BPWM counter matches 0, period value or compared value • Supports up to 12 capture input channels with 16-bit resolution • Supports rising or falling capture condition • Supports input rising/falling capture interrupt • Supports rising/falling capture with counter reload option
Watchdog	• 20-bit free running up counter for WDT time-out interval • Selectable time-out interval (24 ~ 220) * (1 / WDT_CLK) • System kept in reset state for a period of (1 / WDT_CLK) * 63

	• Supports selectable WDT reset delay period, including 1026/130/18/3 WDT_CLK reset delay period • Supports to force Secure only WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register • Supports WDT time-out wake-up function only if WDT clock source is selected as 38.4 kHz LIRC or LXT
RTC	• Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check • Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM • Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK • Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register • Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM • Supports Leap Year indication in RTC_LEAPYEAR register • Supports Day of the Week counter in RTC_WEEKDAY register • Frequency of RTC clock source compensate by RTC_FREQADJ register • All time and calendar message expressed in BCD format • Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second • Supports RTC Time Tick and Alarm Match interrupt • Supports 1 Hz clock output • Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated • Supports Daylight Saving Time software control in RTC_DSTCTL
Analog Interfaces	
Enhanced Analog-to-Digital Converter 12 Bit (EADC0)	• One set of 12-bit, 1.7MSPS SAR EADC with up to 24 external single-ended and 3 internal input channels, they are band-gap voltage (VBG), temperature sensor (VTEMP), and AVDD/4. 10-bit accuracy is guaranteed • Four EADC0 interrupts (ADINT0~3) with individual interrupt vector addresses for EADC0 • Supports calibration function and calibration interrupt • Averaging (2n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2n times, n=0~8) to support up to 16-bit result • Supports conversion results left-alignment • Supports PDMA transfer • Conversion Result Monitor by Compare Mode
Enhanced Analog-to-Digital Converter 14 Bit (EADC1)	• One set of 14-bit, 1.0MSPS SAR EADC with up to 16 external single-ended input channels. 11-bit accuracy is guaranteed • Four EADC1 interrupts (ADINT0~3) with individual interrupt vector addresses for EADC1 • Supports calibration function and calibration interrupt • Averaging (2n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2n times, n=0~8) to support up to 16-bit result • Supports conversion results left-alignment • Supports PDMA transfer • Conversion Result Monitor by Compare Mode

Analog Comparator (ACMP)	• Up to two rail-to-rail analog comparators • Supports hysteresis function – Supports programmable hysteresis window: 0mV, 10mV, 20mV, 40mV • Supports wake-up function • Selectable input sources of positive input and negative input • Shares one ACMP interrupt vector for two comparators • Interrupts generated when compare results change (Interrupt event condition is programmable) • Supports triggers for break events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports offset calibration • Supports ACMP0 event, ACMP1 event be as PDMA request source • Supports ACMP0 event, ACMP1 event be as EADC trigger source • Supports ACMP0 output, ACMP1 output be as Timer, ECAP and PWM trigger source
Digital to Analog Converter (DAC)	• Analog output voltage range: 0~AV_{DD} • Supports 12-bit or 8-bit output mode • Rail to rail settle time 8us • Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin • DAC maximum conversion updating rate 1 MSPS • Supports voltage output buffer mode and bypass voltage output buffer mode • Supports software and hardware trigger, including Timer0~3, PWM0, PWM1 and external trigger pin to start DAC conversion • Supports PDMA mode
Internal Reference Voltage	• Internal reference voltage select: 2.56V, 3.072V, 4.096V for EADC, DAC and CRV (comparator reference voltage) reference voltage • One built-in temperature sensor • Supported temperature range: –40°C to +105°C
Communication Interfaces	
UART	• Full-duplex asynchronous communications • Separates receive and transmit 16/16 bytes entry FIFO for data payloads (UART0~7 support FIFO, UART8,9 do not support FIFO and CTS/RTS) • Supports hardware auto-flow control • Programmable receiver buffer trigger level • Supports programmable baud rate generator for each channel individually • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function • Supports 8-bit receiver buffer time-out detection function • Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8]) • Supports Auto-Baud Rate measurement and baud rate compensation function • 9600 bps for UART_CLK is selected LXT • Supports break error, frame error, parity error and receive/transmit buffer overflow detection function • Fully programmable serial-interface characteristics

	• Programmable number of data bit, 5-, 6-, 7-, 8- bit character • Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection • Programmable STOP bit, 1, 1.5, or 2 STOP bit generation • Supports IrDA SIR function mode • 3/16 bit duration for normal mode • Supports LIN function mode (Only UART0/UART1 with LIN function) • LIN master/slave mode • Programmable break generation function for transmitter • Break detection function for receiver • LIN slave header time-out detection function • LIN response time-out detection function • LIN wake-up function • Supports RS-485 function mode • RS-485 9-bit mode • Hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports PDMA transfer function • Supports Single-wire function mode • Supports bus idle time-out mode • Supports fractional Baud Rate divider
I^2C	• Supports up to three I2C ports • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • Supports High speed mode 3.4Mbps • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Arbitration between simultaneously transmitting masters without corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer • Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflow • Programmable clocks allow for versatile rate control • Supports 7-bit addressing and 10-bit addressing mode • Supports multiple address recognition (four slave address with mask option) • Supports Power-down wake-up function • Supports PDMA with one buffer capability • Supports setup/hold time programmable • Supports Bus Management (SM/PM compatible) function
Quad SPI	• Supports Master or Slave mode operation • Master mode up to 50 MHz (when chip works at VDD = 2.7V~5.5V)

	• Slave mode up to 40 MHz (when chip works at VDD = 2.7~5.5V) • Supports 2-bit Transfer mode • Supports Dual and Quad I/O Transfer mode • Configurable bit length of a transaction word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports Transmit Double Transfer Rate Mode (TX DTR mode) • Supports receive-only mode
SPI/I²S	• One set of SPI/I²S and one set of SPI only controllers with Master/Slave mode **SPI** • Supports Master or Slave mode operation • Master mode up to 36 MHz (when chip works at VDD = 2.7~5.5V) • Slave mode up to 18 MHz (when chip works at VDD = 2.7~5.5V) • Configurable bit length of a transaction word from 4 to 32-bit • Provides separate 4-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports Master or Slave • Capable of handling 8-, 16-, 24- and 32-bit word sizes • Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving • Supports monaural and stereo audio data • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • Supports two PDMA requests, one for transmitting and the other for receiving
Universal Serial Control Interface (USCI)	• Configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffer for data payload • Supports hardware auto flow control function • Supports programmable baud-rate generator • Supports 9-bit Data Transfer (9-bit RS-485)

	• Baud rate detection possible by built-in capture event of baud rate generator • Supports PDMA transfer • Supports Wake-up function (Incoming Data and nCTS Wakeup) **SPI** • Supports Master or Slave mode operation (the maximum frequency -- Master = fPCLK/2, Slave < fPCLK/5) • Configurable bit length of a transfer word from 4 to 16-bit • Supports one transmit buffer and two receive buffers for data payload • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function by slave select signal in Slave mode • Supports one data channel half-duplex transfer **I^2C** • Full master and slave device capability • Supports of 7-bit addressing, as well as 10-bit addressing • Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s) • Supports multi-master bus • Supports one transmit buffer and two receive buffer for data payload • Supports 10-bit bus time-out capability • Supports bus monitor mode • Supports Power down wake-up by START signal or address match • Supports setup/hold time programmable • Supports multiple address recognition (two slave address with mask option)
Controller Area Network with Flexible Data Rate (CAN FD)	• Conforms to CAN protocol version 2.0 part A, B and ISO 11898-1:2015 • CAN FD with up to 64 data bytes supported • CAN Error Logging • AUTOSAR and SAE J1939 support • Improved acceptance filtering • Two configurable Receive FIFOs • Separate signaling on reception of High Priority Messages • Configurable Transmit FIFO, Transmit Queue and Transmit Event FIFO • Direct Message RAM access for CPU • Programmable loop-back test mode • Maskable module interrupts • Two clock domains (CAN Core clock and AHB clock) • Power-down support
External Bus Interface (EBI)	• Supports up to three memory banks • Supports dedicated external chip select pin with polarity control for each bank • Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out • Supports 8-/16-bit data width

	• Supports byte write in 16-bit data width mode • Supports Address/Data multiplexed Mode • Supports Timing parameters individual adjustment for each memory block • Supports LCD interface i80 mode • Supports PDMA mode • Supports variable external bus base clock (MCLK) which based on HCLK • Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports address bus and data bus separate mode
LED Light Strip Interface (LLSI)	• 10 sets of LLSI channels with IDLE polarity control • Each LLSI has 4x32-bit TX FIFO • Configurable transfer period and frame reset length • Configurable T0H and T1H duty cycle • Supports RGB and GRB output format • Supports Software mode and PDMA base mode transfer
Enhanced LED Light Strip Interface (ELLSI)	• 2 sets of ELLSI channels with IDLE polarity control • Each ELLSI has 4x32-bit TX FIFO • Configurable transfer period and frame reset length • Configurable T0H and T1H duty cycle • Supports RGB and GRB output format • Supports Software mode and PDMA base mode transfer • Supports LED advanced command mode(Feedback, TH20 Setting mode, Command mode) • Configurable advanced command pulse width
I3C	• Supports one I3C port • Supports Controller and Target mode • Static or Dynamic Target Device support • Built-in Hardware Dynamic Address Allocation support • Built-in CCC transfer handler • Auto Hot-Join request generation support • In-Band Interrupt request generation support • Adaptive mode of operation between I^2C and I3C depending on I3C bus traffic • Built-in TE0-TE5 Error Handling • Supports Power-down wake-up function • Supports PDMA mode for data transfer • Supports SDR mode, data rates up to 12.5 Mbps • Supports HDR-DDR mode, data rates up to 25 Mbps • Supports Secondary Controller mode • Supports Target Reset – basic V1.1.1 IP • Supports Set Static Address as Dynamic Address CCC – basic V1.1.1 IP • Supports Asynchronous Timing control (Mode 0) – basic V1.1.1 IP • Supports Grouped Addressing – basic V1.1.1 IP

	• Supports HDR-BT mode – basic V1.1.1 IP • Supports Composited / Virtual Targets – basic V1.1.1 IP
Control Interfaces	
Enhanced Quadrature Encoder Interface (EQEI)	• Up to two EQEI controllers, EQEI0, EQEI1 • Two EQEI phase inputs, QEA and QEB; One Index input • A 32-bit up/down Quadrature Encoder Pulse Counter • Supports swap function for input signals QEA and QEB • Supports for detecting the occurrence of phase error from input signals QEA and QEB • Supports one times index signal reset function for Quadrature encoder pulse counter • Encoder Pulse Width measurement mode
Enhanced Capture (ECAP)	• One Input Capture Timer/Counter unit • Each unit has 3 input channels • Each unit has its own interrupt vector • Each input channel has its own capture counter hold register • 24-bit Input Capture up-counting timer/counter • With noise filter in front end of input ports • Captured events reset and/or reload capture counter • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed Host Controller** • Compliant with Universal Serial Bus (USB) Specification Revision 2.0 • Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Supports an integrated Root Hub • Supports port power control and port overcurrent detection • Supports DMA for real-time data transfer USB 2.0 Full Speed Device Controller • Compliant with USB 2.0 Full-Speed specification • Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBDET, USB, BUS and SOF) • Supports Control/Bulk/Interrupt/Isochronous transfer type • Supports suspend function when no bus activity existing for 3ms • Supports 23 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size • Provides remote wake-up capability • Supports double buffer function • Supports VBUS plug in / out or resume wake up from Power-down mode • Supports USB 2.0 Link Power Management (LPM)

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1.1 M3351 Series

Part No.	QFN33 (5x5mm)	QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)	LQFP100 (14x14mm)	LQFP128 (14x14mm)
M3351I		M3351YICAE	M3351LICAE	M3351SICAE	M3351VICAE	M3351KICAE
M3351J		M3351YJCAE	M3351LJCAE	M3351SJCAE	M3351VJCAE	M3351KJCAE
M3351G	M3351ZG7AE	M3351YG7AE	M3351LG7AE	M3351SG7AE		

3.2 M3351 Series Naming Rule

M33	51	K	J	C	A	E
Core	Series	Package	Flash Size	SRAM Size	Revision	Temperature
Cortex-33	51: 5V operating voltage	Z: QFN33 (5x5 mm) Y: QFN48 (5x5 mm) L: LQFP48 (7x7 mm) S: LQFP64(7x7 mm) V: LQFP100(14x14 mm) K: LQFP128(14x14 mm)	G: 256 Kbytes I: 512 Kbytes J:1MB	7: 48KB C: 128KB	A	E:-40°C ~ 105°C

3.3 M3351 Series Selection Guide

PART NUMBER		M3351													
		ZG7AE	LG7AE	YG7AE	SG7AE	LICAE	YICAE	SICAE	VICAE	KICAE	LJCAE	YJCAE	SJCAE	VJCAE	KJCAE
Package		QFN33	LQFP48	QFN48	LQFP64	LQFP48	QFN48	LQFP64	LQFP100	LQFP128	LQFP48	QFN48	LQFP64	LQFP100	LQFP128
Frequency (MHz)		144	144	144	144	144	144	144	144	144	144	144	144	144	144
Flash Memory (KB)		256	256	256	256	512	512	512	512	512	1024	1024	1024	1024	1024
Data Flash (KB)		16	16	16	16	16+64	16+64	16+64	16+64	16+64	16+64	16+64	16+64	16+64	16+64
SRAM (KB)		48	48	48	48	128	128	128	128	128	128	128	128	128	128
LDROM (KB)		16	16	16	16	16	16	16	16	16	16	16	16	16	16
XOM (regions)		2	2	2	2	2	2	2	2	2	2	2	2	2	2
PDMA		10	10	10	10	12	12	12	12	12	12	12	12	12	12
I/O		22	37	37	50	37	37	50	82	106	37	37	50	82	106
RTC		√	√	√	√	√	√	√	√	√	√	√	√	√	√
32-bit Timer		4	4	4	4	4	4	4	4	4	4	4	4	4	4
ECAP		1	1	1	1	1	1	1	1	1	1	1	1	1	1
16-bit PWM		12	12	12	12	12	12	12	12	12	12	12	12	12	12
16-bit BPWM		7	12	12	12	12	12	12	12	12	12	12	12	12	12
Connectivity	UART	6	8	8	8	8	8	8	10	10	8	8	8	10	10
	QSPI	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	SPI/I²S	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	SPI	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	I²C	2	2	2	2	3	3	3	3	3	3	3	3	3	3
	I3C	-	-	-	-	1	1	1	1	1	1	1	1	1	1
	USCI	2	2	2	2	2	2	2	2	2	2	2	2	2	2
	LLSI	9	10	10	10	10	10	10	10	10	10	10	10	10	10
	ELLSI	2	2	2	2	2	2	2	2	2	2	2	2	2	2
CAN FD		-	2	2	2	2	2	2	2	2	2	2	2	2	2
USB 2.0 FS		√	√	√	√	√	√	√	√	√	√	√	√	√	√
External Bus Interface		-	-	-	-	√	√	√	√	√	√	√	√	√	√
EQEI		-	1	1	1	1	1	1	2	2	1	1	1	2	2
12-bit EADC		10	16	16	20	16	16	20	23	24	16	16	20	23	24
14-bit EADC		-	-	-	-	5	5	9	11	16	5	5	9	11	16
12-bit DAC		-	-	-	-	1	1	1	1	1	1	1	1	1	1
Analog Comparator		2	2	2	2	2	2	2	2	2	2	2	2	2	2
Crypto		SHA-256	SHA-256	SHA-256	SHA-256	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512	AES-256, SHA-512, HMAC-SHA-512

PRNG	-	-	-	-	√	√	√	√	√	√	√	√	√	√
TRNG	-	-	-	-	√	√	√	√	√	√	√	√	√	√

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in the M3351 Series Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.2 M3351 Series Pin Diagram

4.2.1 QFN33-Pin Diagram

Corresponding Part Number: M3351ZG7AE

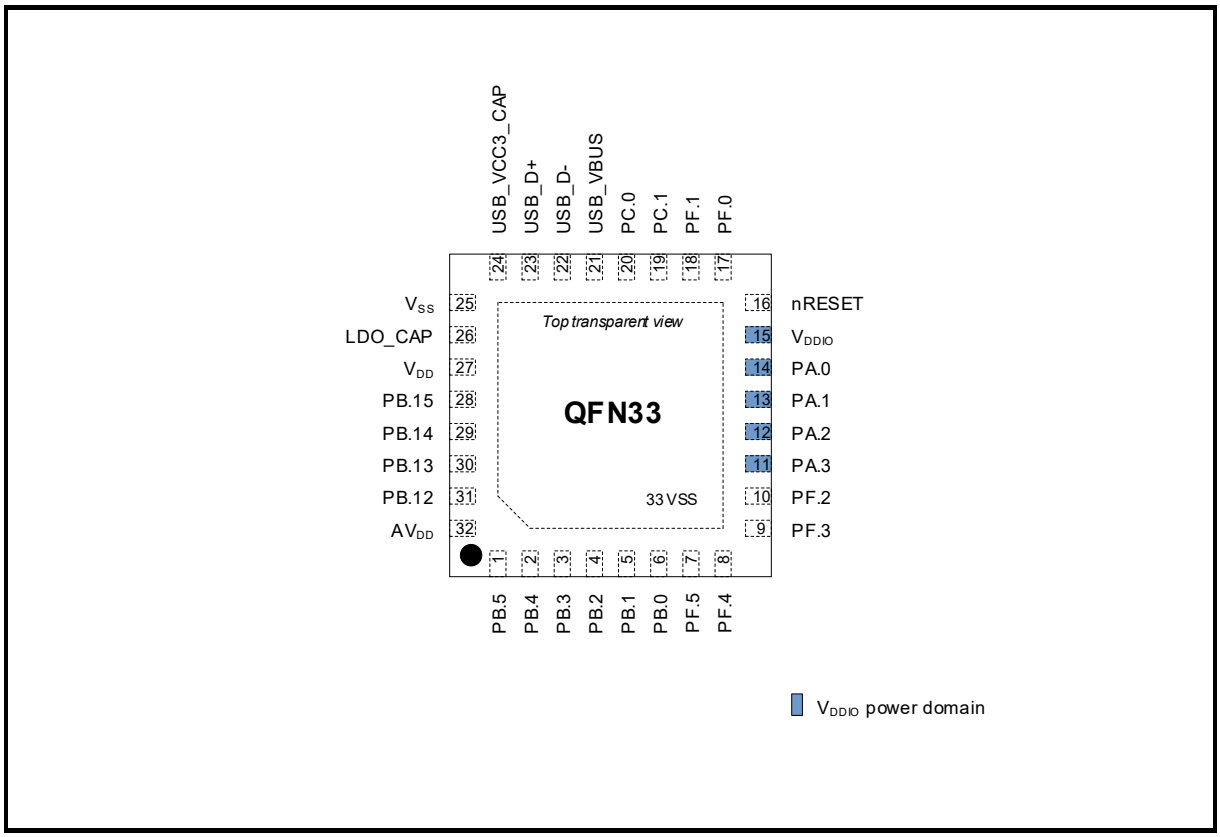


Figure 4.2-1 QFN33-Pin Diagram

4.2.2 LQFP48-Pin Diagram

Corresponding Part Number: M3351LICAE/ M3351LJCAE/M3351LG7AE

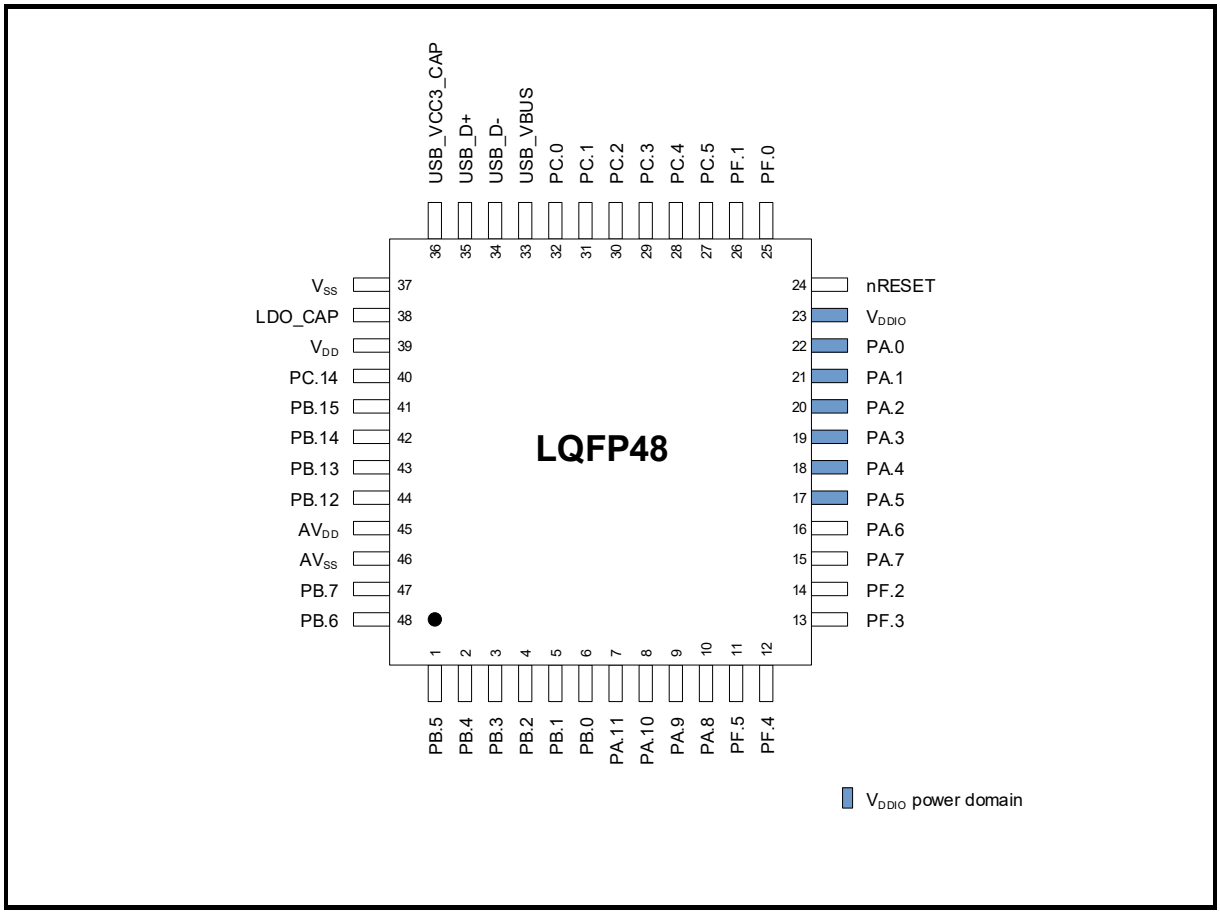


Figure 4.2-2 LQFN48-Pin Diagram

4.2.3 QFN48-Pin Diagram

Corresponding Part Number: M3351YICAE/ M3351YJCAE/M3351YG7AE

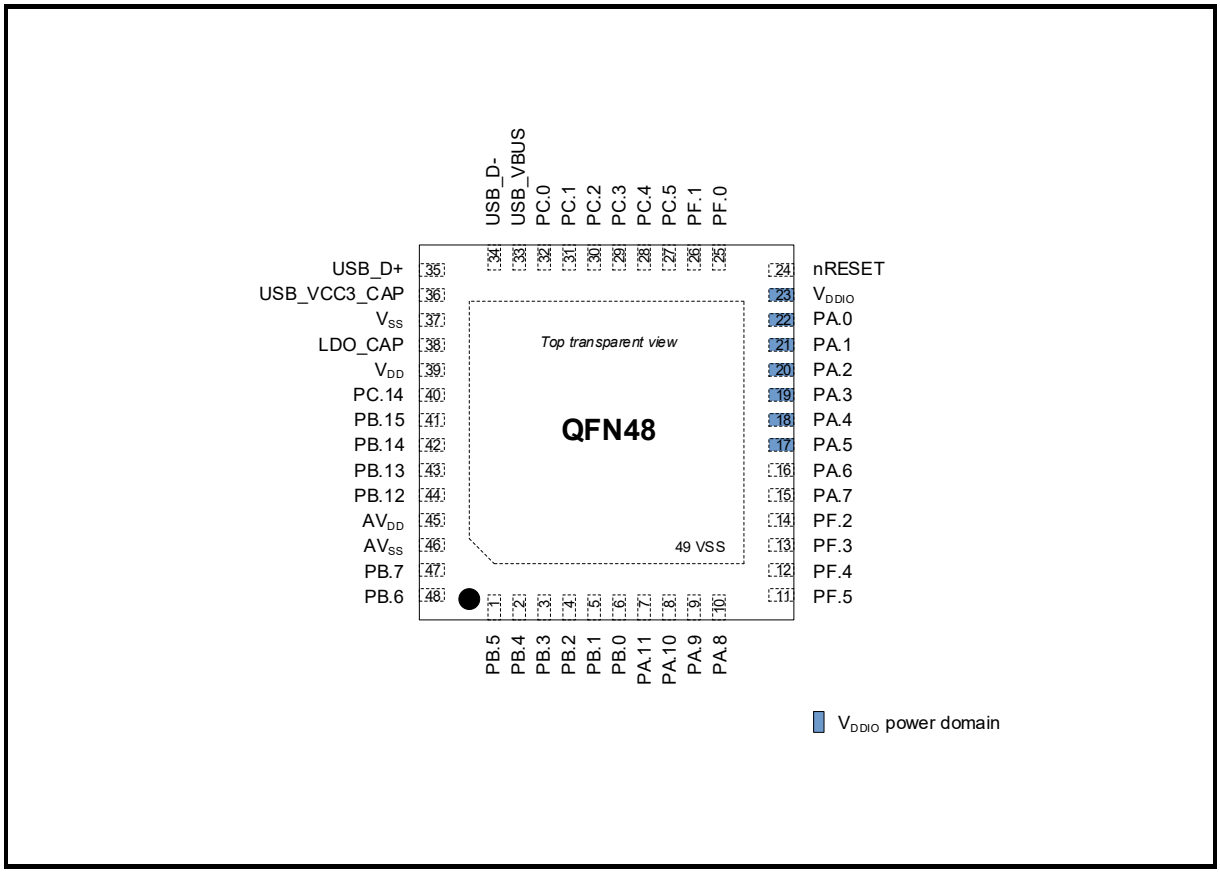


Figure 4.2-3 QFN48-Pin Diagram

4.2.4 LQFP64-Pin Diagram

Corresponding Part Number: M3351SICAE/ M3351SJCAE/M3351SG7AE

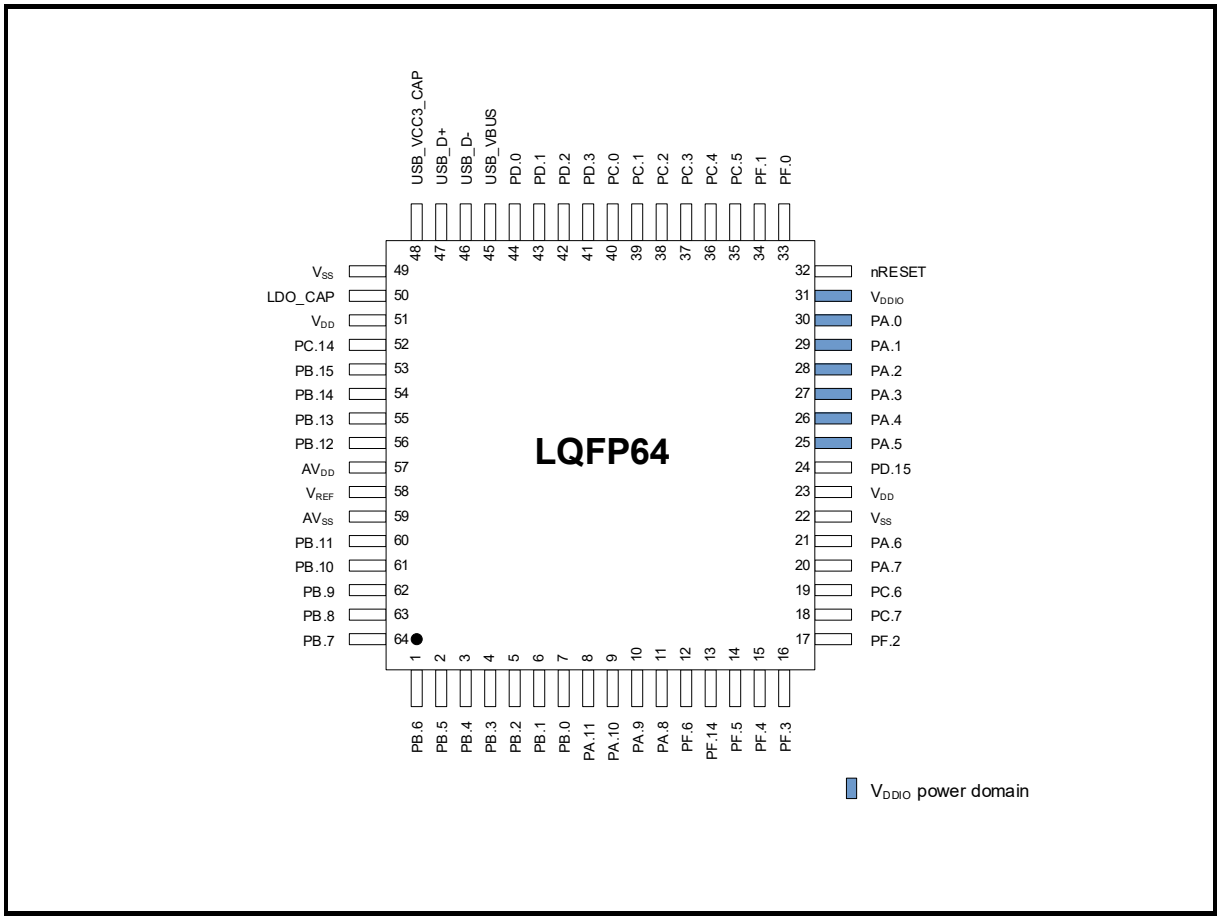


Figure 4.2-4 LQFP64-Pin Diagram

4.2.5 LQFP100-Pin Diagram

Corresponding Part Number: M3351VICAE/ M3351VJCAE

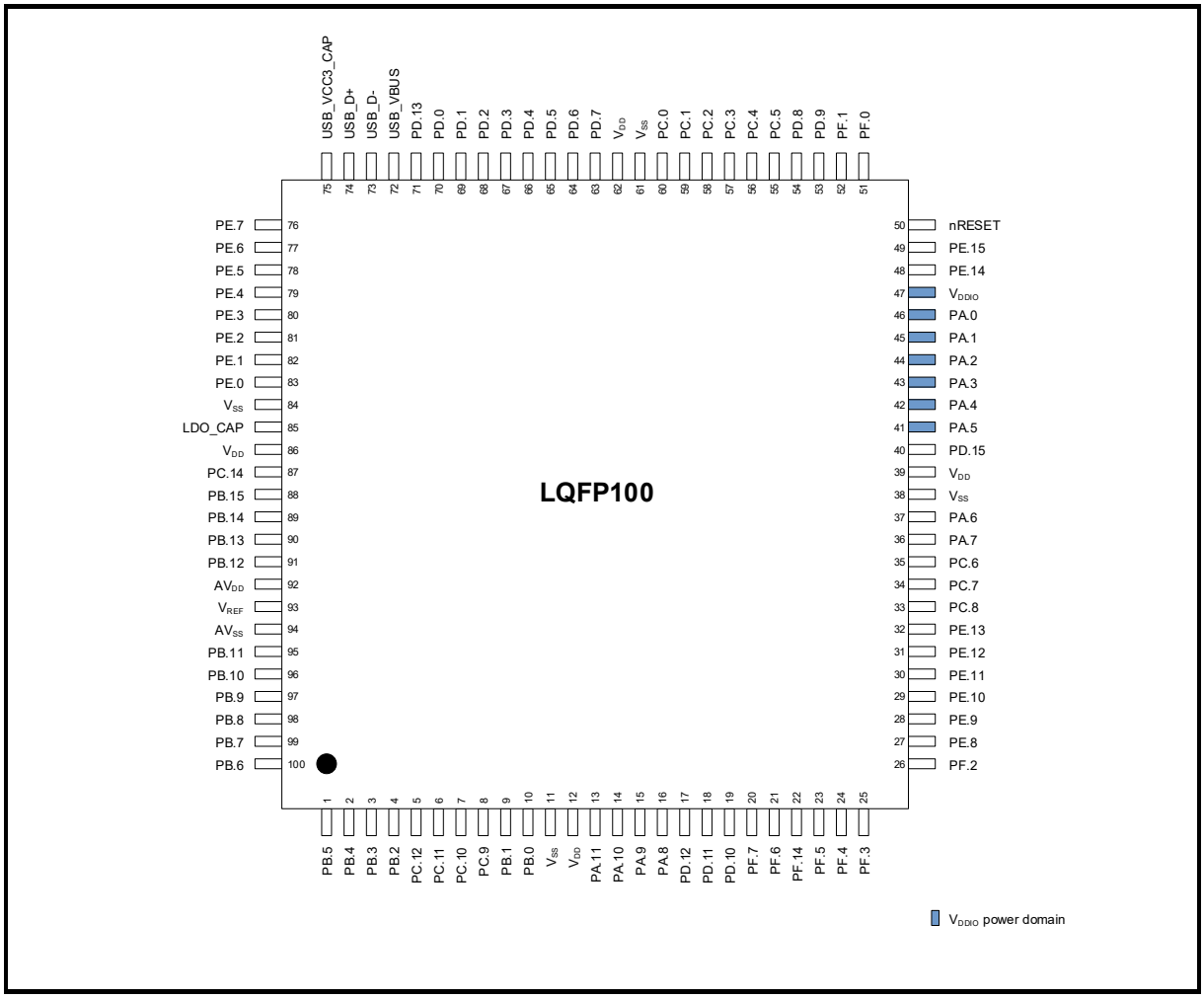


Figure 4.2-5 LQFN100-Pin Diagram

4.2.6 LQFP128-Pin Diagram

Corresponding Part Number: M3351KICAE/ M3351KJCAE

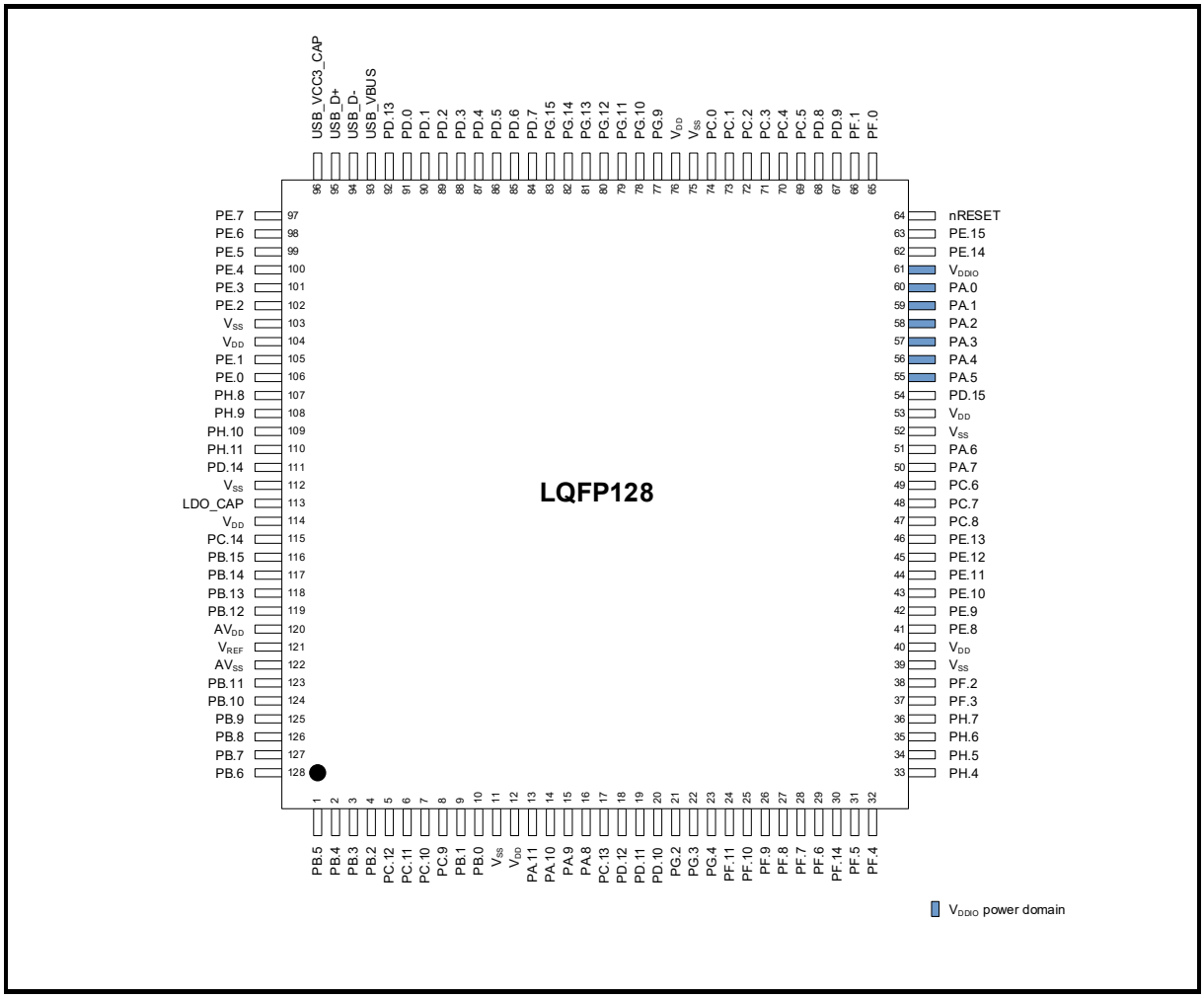


Figure 4.2-6 LQFP48-Pin Diagram

4.3 M3351xIC/M3351xJC Multi-function Pin Diagram

4.3.1 QFN48-Pin Multi-function Pin Diagram

4.3.1.1 M3351YICAE

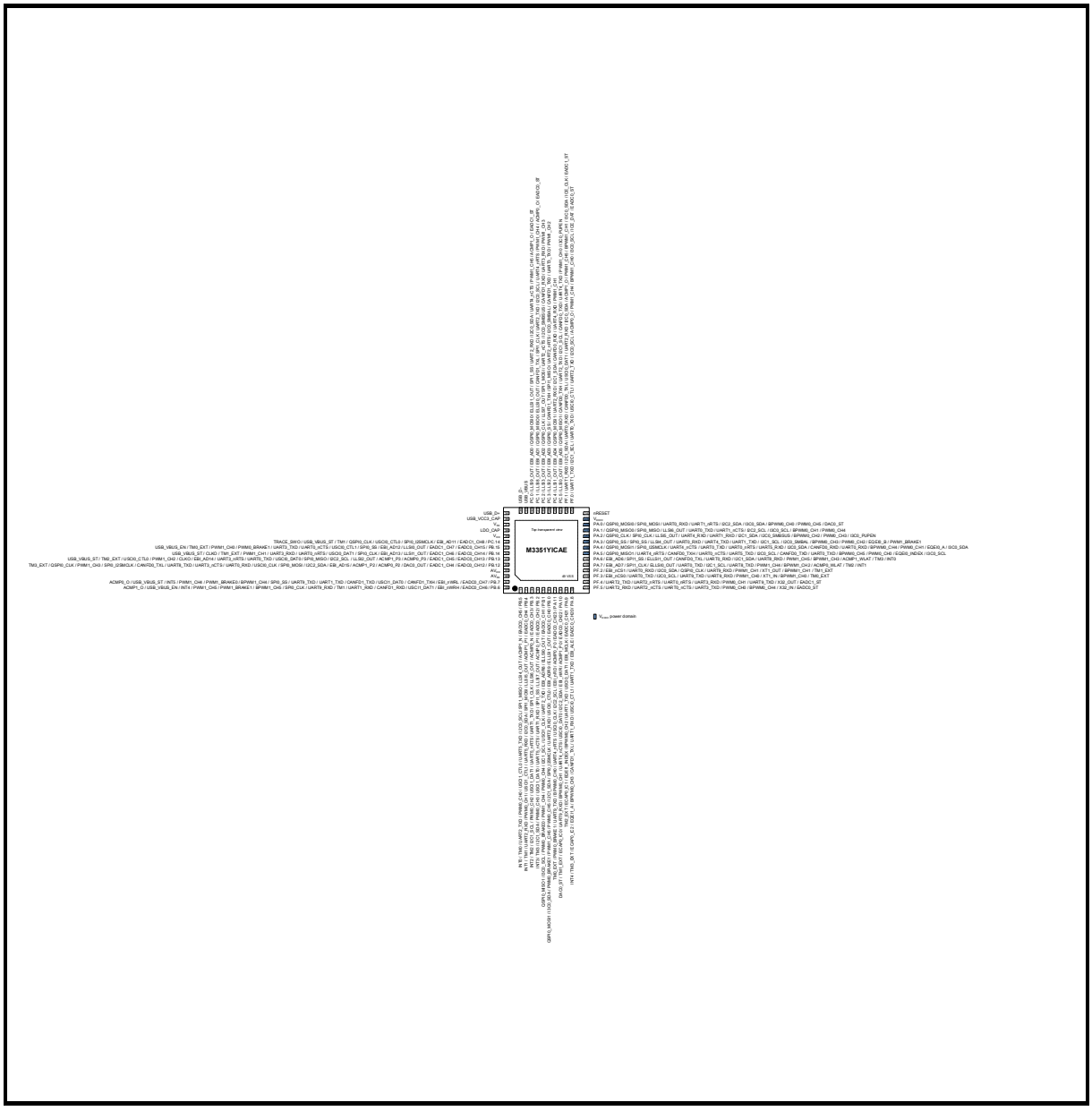


Figure 4.3-1 M3351YICAE Multi-function Pin Diagram

Pin	Type	M3351YICAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351YICAE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
9	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
27	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN

Pin	Type	M3351YICAE Pin Function
28	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
29	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
49	P	V_{SS}

Table 4.3-1 M3351YICAE Multi-function Pin Table

4.3.1.2 M3351YJCAE

Corresponding Part Number: M3351YJCAE

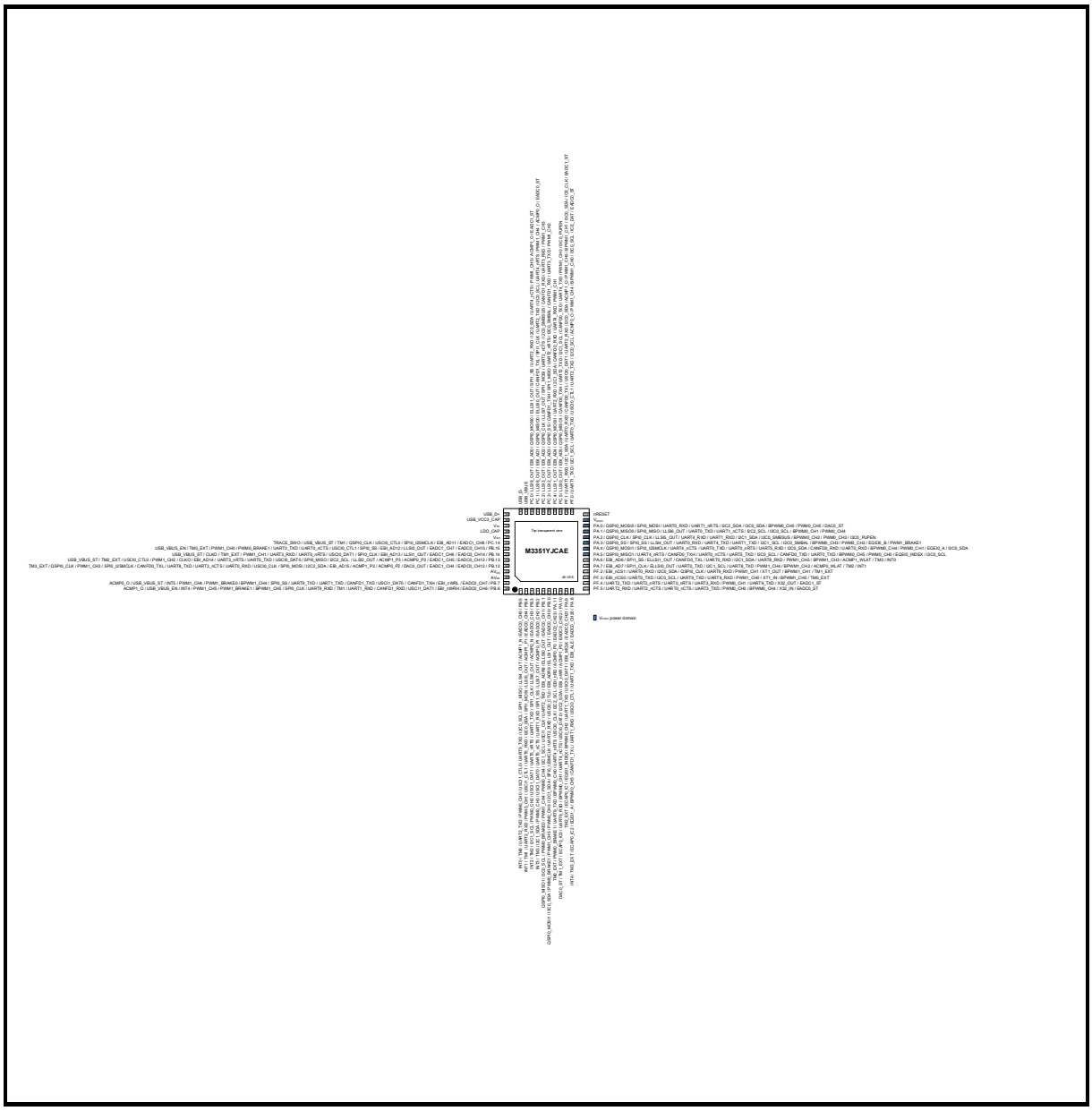


Figure 4.3-2 M3351YJCAE Multi-function Pin Diagram

Pin	Type	M3351YJCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3

Pin	Type	M3351YJCAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
9	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
27	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
28	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1

Pin	Type	M3351YJCAE Pin Function
29	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
49	P	V_{SS}

Table 4.3-2 M3351YJCAE Multi-function Pin Table

4.3.2 LQFP48-Pin Multi-function Pin Diagram

Corresponding Part Number: M335LICAE

4.3.2.1 M3351LICAE

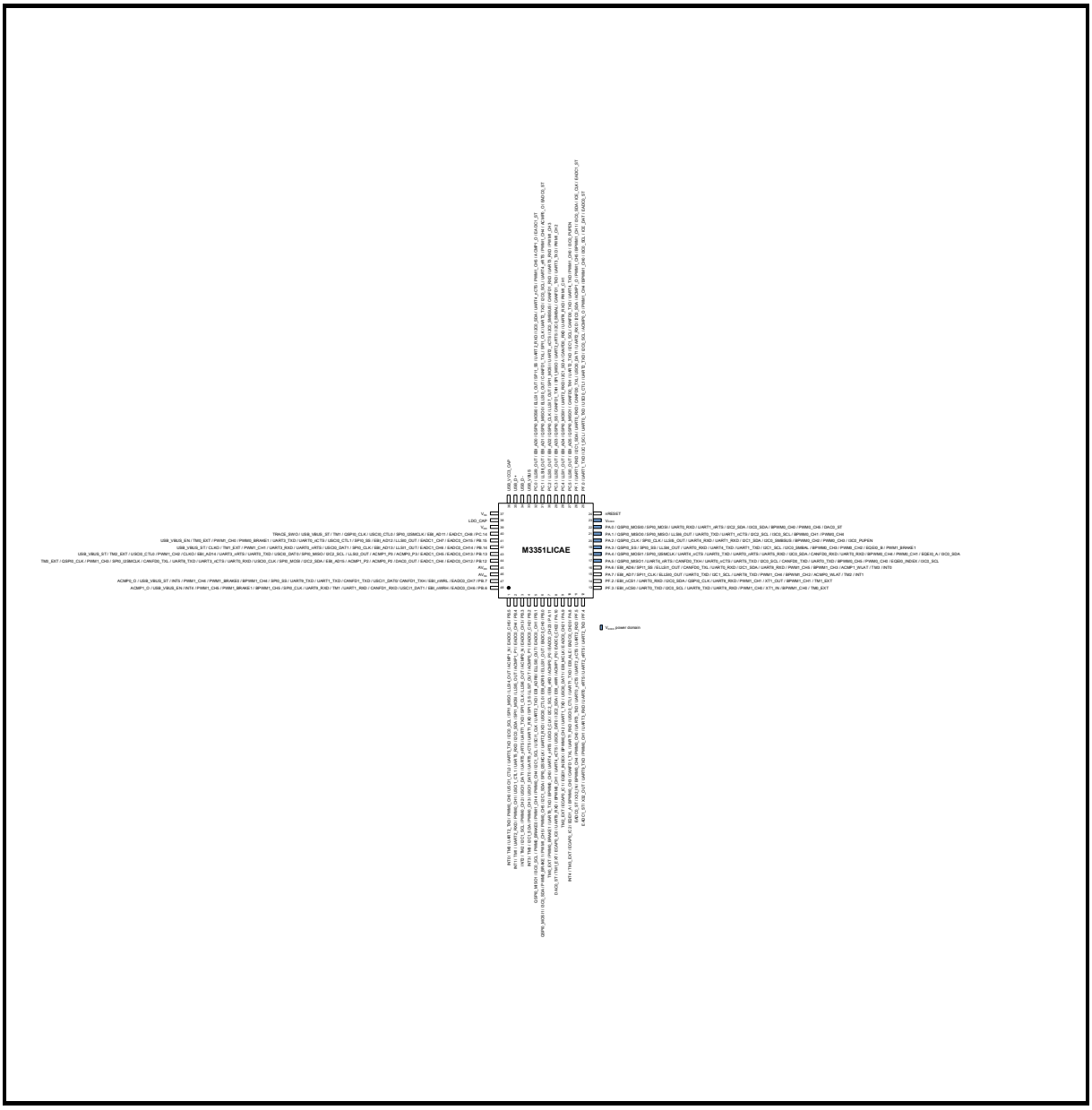


Figure 4.3-3 M3351LICAE Multi-function Pin Diagram

Pin	Type	M3351LICAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351LICAE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
9	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
27	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN

Pin	Type	M3351LICAE Pin Function
28	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
29	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-3 M3351LICAE/ M3351LJCAE Multi-function Pin Table

4.3.2.2 M3351LJCAE

Corresponding Part Number: M3351LICAE/M3351LJCAE

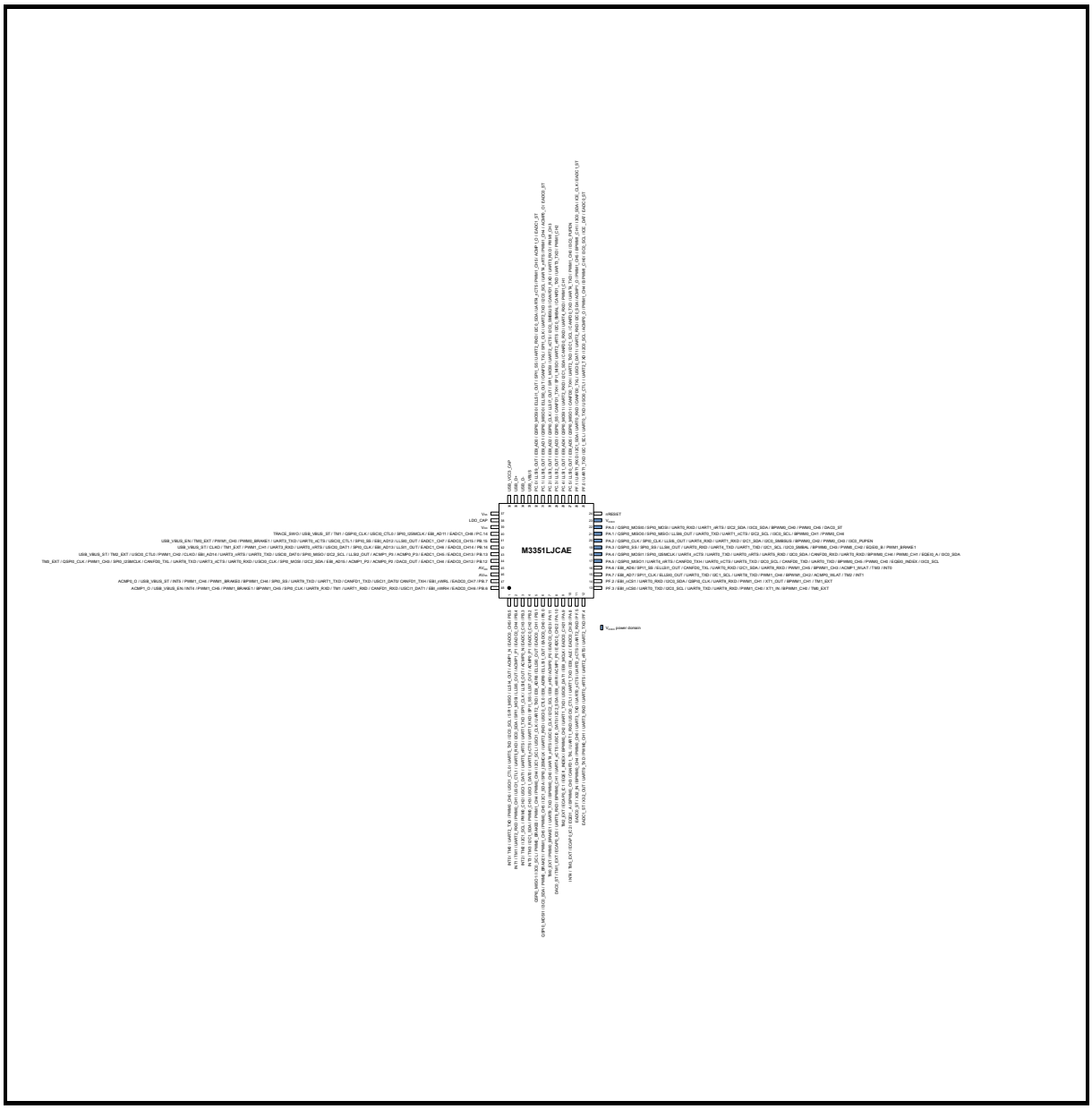


Figure 4.3-4 M3351LJCAE Multi-function Pin Diagram

Pin	Type	M3351LJCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3

Pin	Type	M3351LJCAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
9	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
27	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
28	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1

Pin	Type	M3351LJCAE Pin Function
29	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-4 M3351LJCAE Multi-function Pin Table

4.3.3 LQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M3351SICAE

4.3.3.1 M3351SICAE

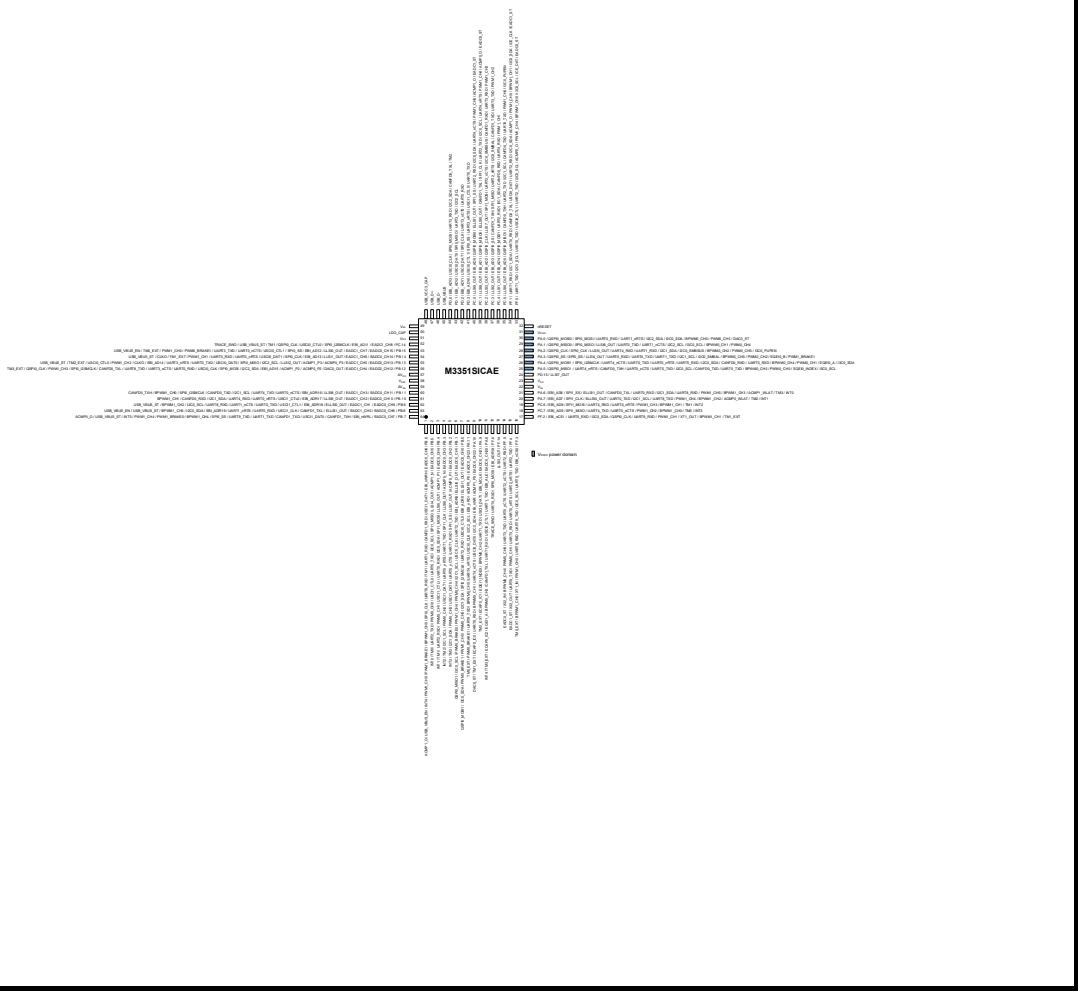


Figure 4.3-5 M3351SICAE Multi-function Pin Diagram

Pin	Type	M3351SICAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1

Pin	Type	M3351SICAE Pin Function
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
7	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
8	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
9	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
10	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
11	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
13	I/O	PF.14 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
18	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / LLSI7_OUT
25	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
26	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN

Pin	Type	M3351SICAE Pin Function
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
31	P	V_{DDIO}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
35	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
36	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
37	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
38	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
39	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
40	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
41	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
42	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
43	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
44	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
45	P	USB_VBUS
46	A	USB_D-
47	A	USB_D+
48	A	USB_VCC3_CAP
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
53	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
54	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
55	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST

Pin	Type	M3351SICAE Pin Function
56	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
61	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
62	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
63	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
64	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

Table 4.3-5 M3351SICAE Multi-function Pin Table

4.3.3.2 M3351SJCAE

Corresponding Part Number: M3351SJCAE

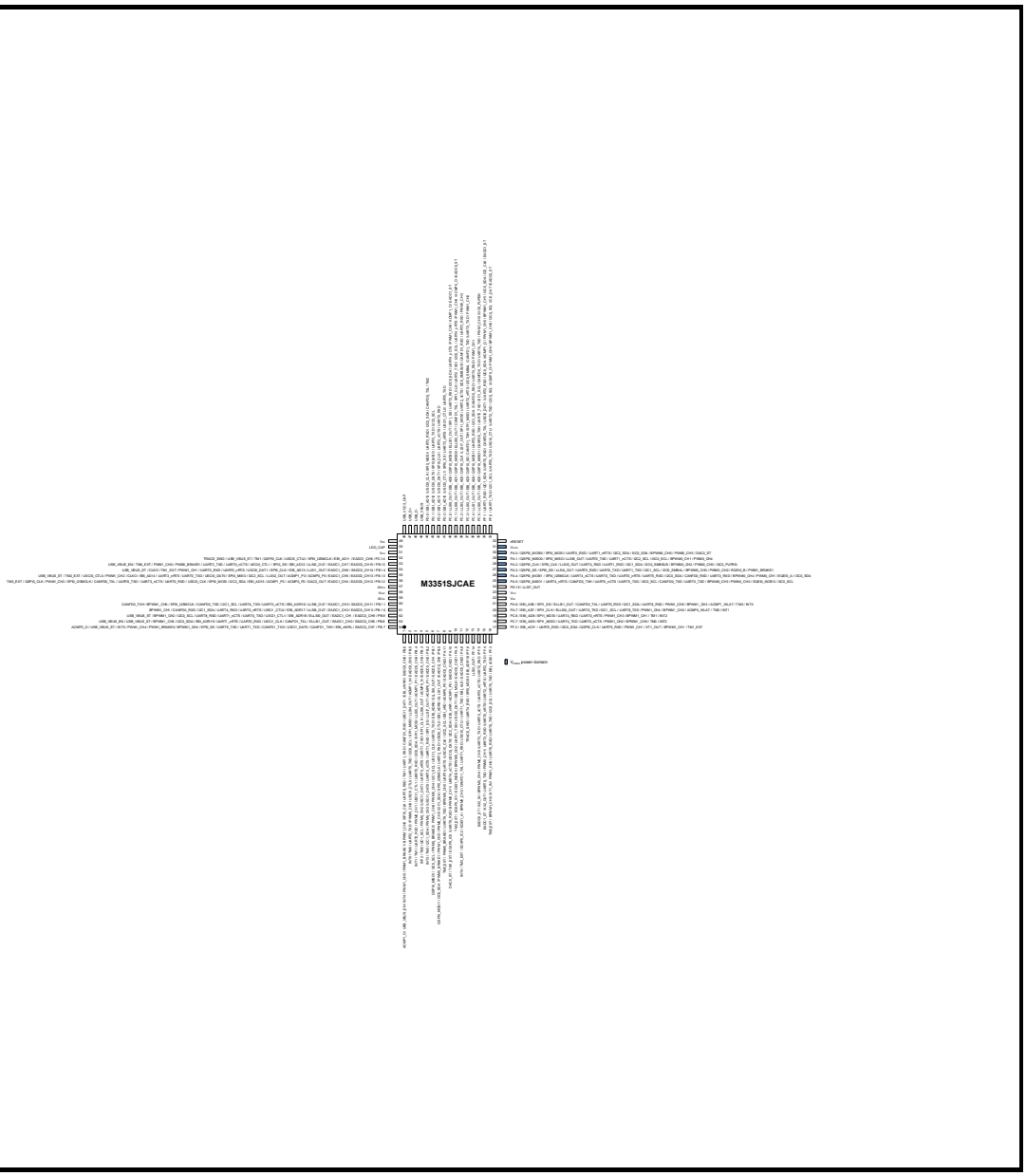


Figure 4.3-6 M3351SJCAE Multi-function Pin Diagram

M3351SJCAE Multi-function Pin Table

Pin	Type	M3351SJCAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS /

Pin	Type	M3351SJCAE Pin Function
		USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
7	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
8	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
9	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
10	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
11	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
13	I/O	PF.14 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
18	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / LLSI7_OUT
25	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
26	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL

Pin	Type	M3351SJCAE Pin Function
		/ BPWM0_CH1 / PWM0_CH4
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
31	P	V_{DDIO}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
35	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
36	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
37	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
38	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
39	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
40	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
41	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
42	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
43	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
44	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
45	P	USB_VBUS
46	A	USB_D-
47	A	USB_D+
48	A	USB_VCC3_CAP
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
53	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
54	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
55	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
56	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL /

Pin	Type	M3351SJCAE Pin Function
		SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
61	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
62	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
63	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
64	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

Table 4.3-6 M3351SJCAE Multi-function Pin Table

4.3.4 LQFP100-Pin Multi-function Pin Diagram

Corresponding Part Number: M3351VICAE

4.3.4.1 M3351VICA

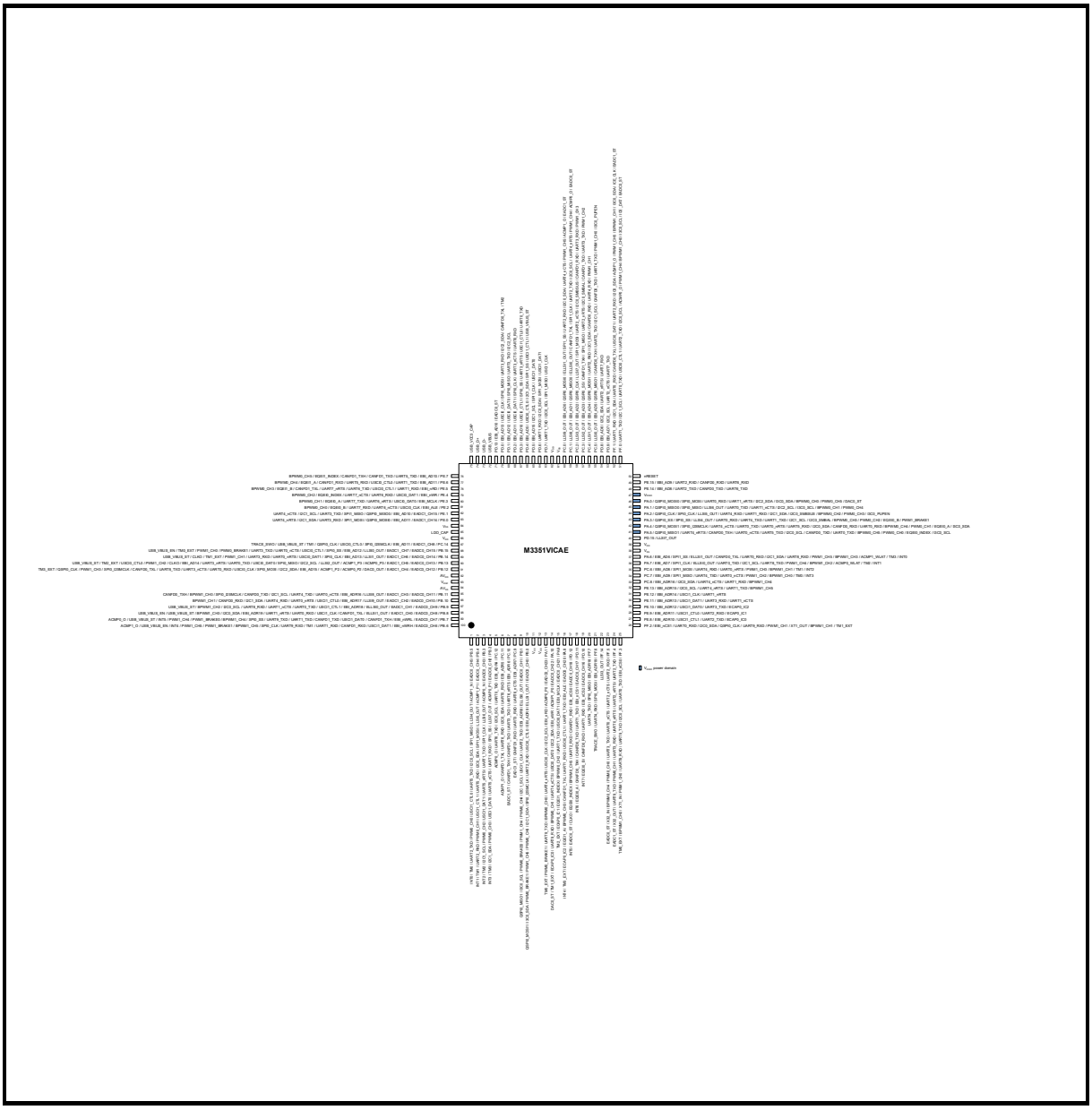


Figure 4.3-7 M3351VICAE Multi-function Pin Diagram

Pin	Type	M3351VICAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351VICAE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / CANFD1_TXL / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART6_nRTS / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EADC1_ST
8	I/O	PC.9 / EBI_ADR7 / UART6_nCTS / UART3_RXD / CANFD1_RXD / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
10	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
14	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
16	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
17	I/O	PD.12 / EADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5
18	I/O	PD.11 / EADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / INT6
19	I/O	PD.10 / EADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7
20	I/O	PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD
21	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
22	I/O	PF.14 / LLSI3_OUT
23	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
24	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
25	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
26	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
27	I/O	PE.8 / EBI_ADR10 / USCI1_CTL1 / UART2_TXD / ECAP0_IC0
28	I/O	PE.9 / EBI_ADR11 / USCI1_CTL0 / UART2_RXD / ECAP0_IC1
29	I/O	PE.10 / EBI_ADR12 / USCI1_DAT0 / UART3_TXD / ECAP0_IC2
30	I/O	PE.11 / EBI_ADR13 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
31	I/O	PE.12 / EBI_ADR14 / USCI1_CLK / UART1_nRTS
32	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / BPWM1_CH5

Pin	Type	M3351VICAE Pin Function
33	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / BPWM1_CH4
34	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
35	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
36	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
37	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
38	P	V_{SS}
39	P	V_{DD}
40	I/O	PD.15 / LLSI7_OUT
41	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
42	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
43	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
44	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
45	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
46	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
47	P	V_{DDIO}
48	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD
49	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD
50	I	nRESET
51	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
52	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
53	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD
54	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD
55	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
56	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
57	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
58	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
59	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST

Pin	Type	M3351VICAE Pin Function
60	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
61	P	V_{SS}
62	P	V_{DD}
63	I/O	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK
64	I/O	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1
65	I/O	PD.5 / EBI_AD15 / I2C1_SCL / SPI1_CLK / USCI1_DAT0
66	I/O	PD.4 / EBI_AD5 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / USB_VBUS_ST
67	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
68	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
69	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
70	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
71	I/O	PD.13 / EBI_AD10 / EADC0_ST
72	P	USB_VBUS
73	A	USB_D-
74	A	USB_D+
75	A	USB_VCC3_CAP
76	I/O	PE.7 / EBI_AD10 / UART5_TXD / CANFD1_TXD / CANFD1_TXH / EQEI1_INDEX / BPWM0_CH5
77	I/O	PE.6 / EBI_AD11 / UART1_TXD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / BPWM0_CH4
78	I/O	PE.5 / EBI_nRD / UART1_RXD / USCI0_CTL1 / UART6_TXD / UART7_nRTS / CANFD1_TXL / EQEI1_B / BPWM0_CH3
79	I/O	PE.4 / EBI_nWR / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / BPWM0_CH2
80	I/O	PE.3 / EBI_MCLK / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / BPWM0_CH1
81	I/O	PE.2 / EBI_ALE / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / BPWM0_CH0
82	I/O	PE.1 / EADC1_CH15 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS
83	I/O	PE.0 / EADC1_CH14 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS
84	P	V_{SS}
85	A	LDO_CAP
86	P	V_{DD}
87	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
88	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
89	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
90	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO

Pin	Type	M3351VICAE Pin Function
		/ USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
91	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
92	P	AV_{DD}
93	A	V_{REF}
94	P	AV_{SS}
95	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
96	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
97	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
98	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
99	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
100	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-7 M3351VICAE Multi-function Pin Table

4.3.4.2 M3351VJCAE

Corresponding Part Number: M3351VJCAE

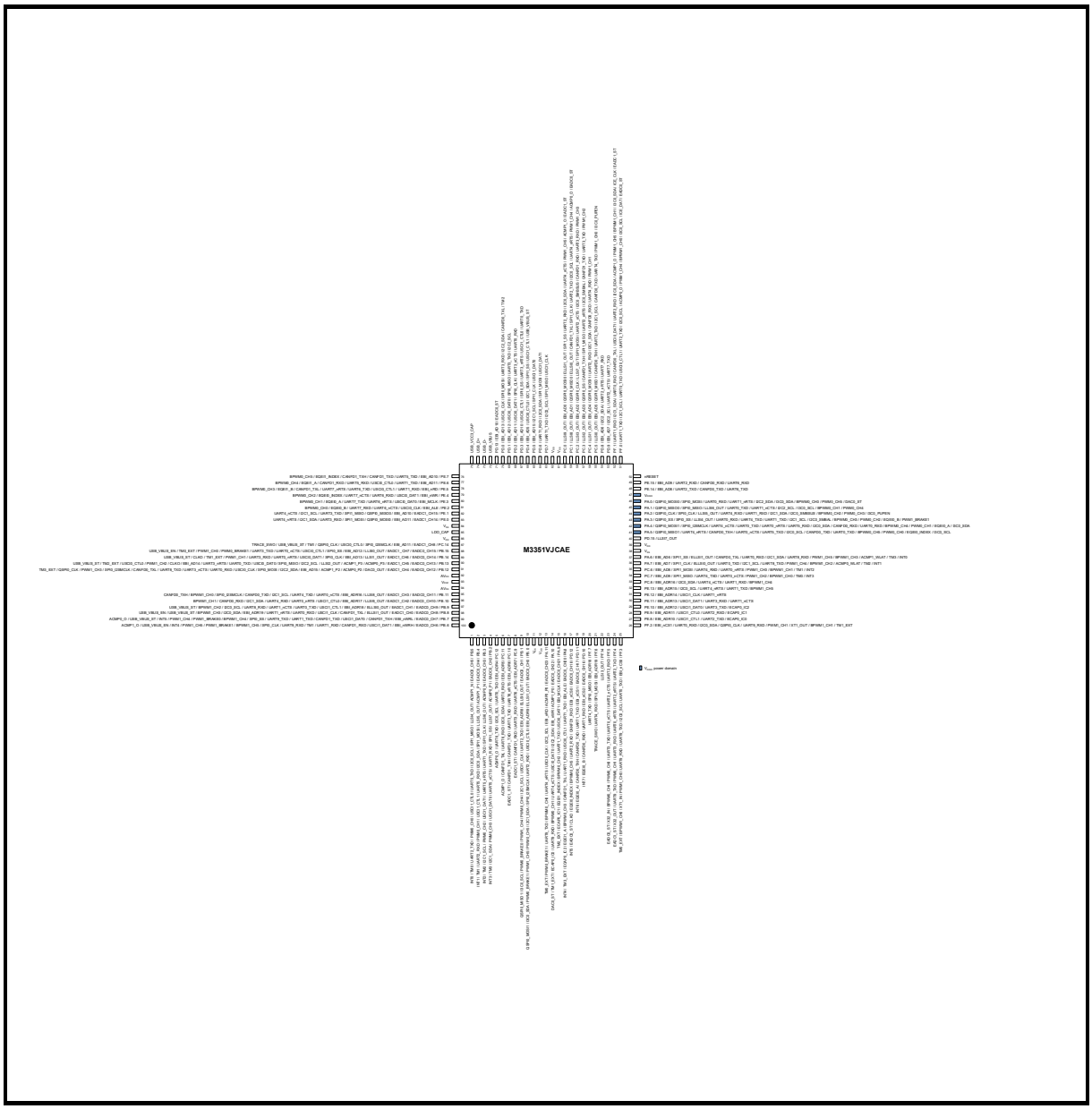


Figure 4.3-8 M3351VJCAE Multi-function Pin Diagram

Pin	Type	M3351VJCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3

Pin	Type	M3351VJCAE Pin Function
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / CANFD1_TXL / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART6_nRTS / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EADC1_ST
8	I/O	PC.9 / EBI_ADR7 / UART6_nCTS / UART3_RXD / CANFD1_RXD / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
10	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
14	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
16	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
17	I/O	PD.12 / EADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5
18	I/O	PD.11 / EADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / INT6
19	I/O	PD.10 / EADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7
20	I/O	PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD
21	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
22	I/O	PF.14 / LLSI3_OUT
23	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
24	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
25	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
26	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
27	I/O	PE.8 / EBI_ADR10 / USCI1_CTL1 / UART2_TXD / ECAP0_IC0
28	I/O	PE.9 / EBI_ADR11 / USCI1_CTL0 / UART2_RXD / ECAP0_IC1
29	I/O	PE.10 / EBI_ADR12 / USCI1_DAT0 / UART3_TXD / ECAP0_IC2
30	I/O	PE.11 / EBI_ADR13 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
31	I/O	PE.12 / EBI_ADR14 / USCI1_CLK / UART1_nRTS
32	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / BPWM1_CH5
33	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / BPWM1_CH4

Pin	Type	M3351VJCAE Pin Function
34	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
35	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
36	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
37	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
38	P	V_{SS}
39	P	V_{DD}
40	I/O	PD.15 / LLSI7_OUT
41	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
42	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
43	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
44	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
45	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
46	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
47	P	V_{DDIO}
48	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD
49	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD
50	I	nRESET
51	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
52	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
53	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD
54	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD
55	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
56	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
57	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
58	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
59	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
60	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA /

Pin	Type	M3351VJCAE Pin Function
		UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
61	P	V_{SS}
62	P	V_{DD}
63	I/O	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK
64	I/O	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1
65	I/O	PD.5 / EBI_AD15 / I2C1_SCL / SPI1_CLK / USCI1_DAT0
66	I/O	PD.4 / EBI_AD5 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / USB_VBUS_ST
67	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
68	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
69	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
70	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
71	I/O	PD.13 / EBI_AD10 / EADC0_ST
72	P	USB_VBUS
73	A	USB_D-
74	A	USB_D+
75	A	USB_VCC3_CAP
76	I/O	PE.7 / EBI_AD10 / UART5_TXD / CANFD1_TXD / CANFD1_TXH / EQEI1_INDEX / BPWM0_CH5
77	I/O	PE.6 / EBI_AD11 / UART1_TXD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / BPWM0_CH4
78	I/O	PE.5 / EBI_nRD / UART1_RXD / USCI0_CTL1 / UART6_TXD / UART7_nRTS / CANFD1_TXL / EQEI1_B / BPWM0_CH3
79	I/O	PE.4 / EBI_nWR / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / BPWM0_CH2
80	I/O	PE.3 / EBI_MCLK / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / BPWM0_CH1
81	I/O	PE.2 / EBI_ALE / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / BPWM0_CH0
82	I/O	PE.1 / EADC1_CH15 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS
83	I/O	PE.0 / EADC1_CH14 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS
84	P	V_{SS}
85	A	LDO_CAP
86	P	V_{DD}
87	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
88	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
89	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
90	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 /

Pin	Type	M3351VJCAE Pin Function
		TM2_EXT / USB_VBUS_ST
91	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
92	P	AV_{DD}
93	A	V_{REF}
94	P	AV_{SS}
95	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
96	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
97	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
98	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
99	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
100	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-8 M3351VJCAE Multi-function Pin Table

4.3.5 LQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M3351KICAE

4.3.5.1 M3351KICAE

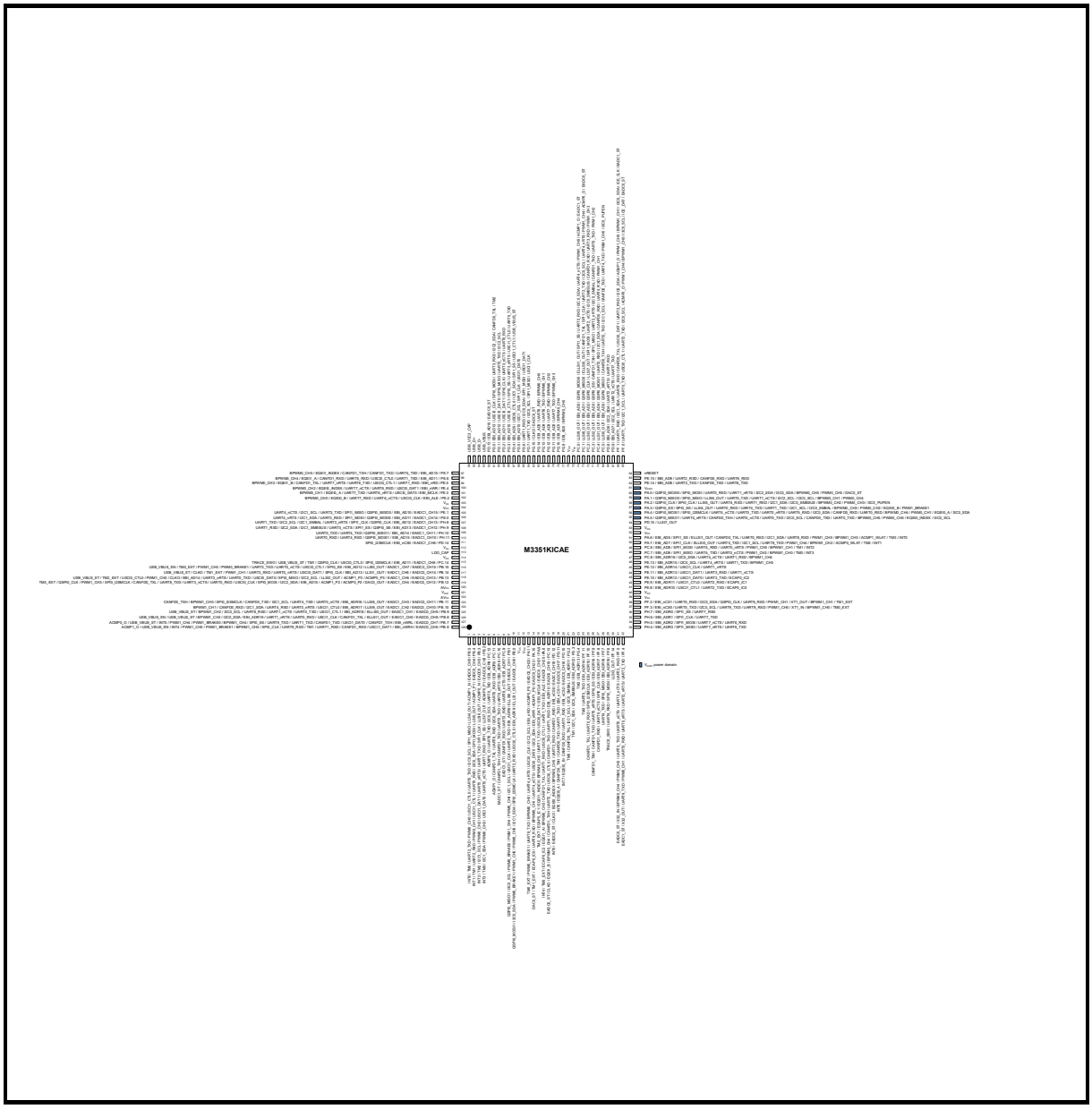


Figure 4.3-9 M3351KICAE Multi-function Pin Diagram

Pin	Type	M3351KICAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351KICAE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / CANFD1_TXL / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART6_nRTS / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EADC1_ST
8	I/O	PC.9 / EBI_ADR7 / UART6_nCTS / UART3_RXD / CANFD1_RXD / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
10	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
14	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
16	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
17	I/O	PC.13 / EADC0_CH19 / EBI_ADR10 / UART1_RXD / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / CANFD1_TXH / BPWM0_CH4 / EQEI1_B / CLKO / EADC0_ST
18	I/O	PD.12 / EADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / INT6
20	I/O	PD.10 / EADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7
21	I/O	PG.2 / EBI_ADR11 / I2C0_SMBAL / I2C1_SCL / CANFD0_TXL / TM0
22	I/O	PG.3 / EBI_ADR12 / I2C0_SMBSUS / I2C1_SDA / TM1
23	I/O	PG.4 / EBI_ADR13 / TM2
24	I/O	PF.11 / EBI_ADR14 / UART5_TXD / TM3
25	I/O	PF.10 / EBI_ADR15 / SPI0_I2SMCLK / UART5_RXD / CANFD1_TXL
26	I/O	PF.9 / EBI_ADR16 / SPI0_SS / UART5_nRTS / CANFD1_TXD / CANFD1_TXH
27	I/O	PF.8 / EBI_ADR17 / SPI0_CLK / UART5_nCTS / CANFD1_RXD
28	I/O	PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD
29	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
30	I/O	PF.14 / LLSI3_OUT
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST

Pin	Type	M3351KICAE Pin Function
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / USCI1_CTL1 / UART2_TXD / ECAP0_IC0
42	I/O	PE.9 / EBI_ADR11 / USCI1_CTL0 / UART2_RXD / ECAP0_IC1
43	I/O	PE.10 / EBI_ADR12 / USCI1_DAT0 / UART3_TXD / ECAP0_IC2
44	I/O	PE.11 / EBI_ADR13 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
45	I/O	PE.12 / EBI_ADR14 / USCI1_CLK / UART1_nRTS
46	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / BPWM1_CH5
47	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / BPWM1_CH4
48	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / LLSI7_OUT
55	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
56	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
61	P	V_{DDIO}

Pin	Type	M3351KICAE Pin Function
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD
69	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
70	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
71	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
72	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
73	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
74	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
75	P	V_{SS}
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / BPWM0_CH5
78	I/O	PG.10 / EBI_AD1 / BPWM0_CH4
79	I/O	PG.11 / EBI_AD2 / UART7_TXD / BPWM0_CH3
80	I/O	PG.12 / EBI_AD3 / UART7_RXD / BPWM0_CH2
81	I/O	PG.13 / EBI_AD4 / UART6_TXD / BPWM0_CH1
82	I/O	PG.14 / EBI_AD5 / UART6_RXD / BPWM0_CH0
83	I/O	PG.15 / CLKO / EADC0_ST
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1
86	I/O	PD.5 / EBI_AD15 / I2C1_SCL / SPI1_CLK / USCI1_DAT0
87	I/O	PD.4 / EBI_AD5 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / USB_VBUS_ST
88	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
89	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
90	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
91	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
92	I/O	PD.13 / EBI_AD10 / EADC0_ST

Pin	Type	M3351KICAE Pin Function
93	P	USB_VBUS
94	A	USB_D-
95	A	USB_D+
96	A	USB_VCC3_CAP
97	I/O	PE.7 / EBI_AD10 / UART5_TXD / CANFD1_TXD / CANFD1_TXH / EQEI1_INDEX / BPWM0_CH5
98	I/O	PE.6 / EBI_AD11 / UART1_TXD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / BPWM0_CH4
99	I/O	PE.5 / EBI_nRD / UART1_RXD / USCI0_CTL1 / UART6_TXD / UART7_nRTS / CANFD1_TXL / EQEI1_B / BPWM0_CH3
100	I/O	PE.4 / EBI_nWR / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / BPWM0_CH2
101	I/O	PE.3 / EBI_MCLK / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / BPWM0_CH1
102	I/O	PE.2 / EBI_ALE / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / BPWM0_CH0
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EADC1_CH15 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS
106	I/O	PE.0 / EADC1_CH14 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS
107	I/O	PH.8 / EADC1_CH13 / EBI_AD12 / QSPI0_CLK / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD
108	I/O	PH.9 / EADC1_CH12 / EBI_AD13 / QSPI0_SS / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD
109	I/O	PH.10 / EADC1_CH11 / EBI_AD14 / QSPI0_MISO1 / UART4_TXD / UART0_TXD
110	I/O	PH.11 / EADC1_CH10 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD
111	I/O	PD.14 / EADC1_CH9 / EBI_nCS0 / SPI0_I2SMCLK
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
116	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
117	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
118	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
119	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
120	P	AV_{DD}

Pin	Type	M3351KICAE Pin Function
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
124	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
125	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
126	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
127	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-9 M3351KICAE Multi-function Pin Table

4.3.5.2 M3351KJCAE

Corresponding Part Number: M3351KJCAE

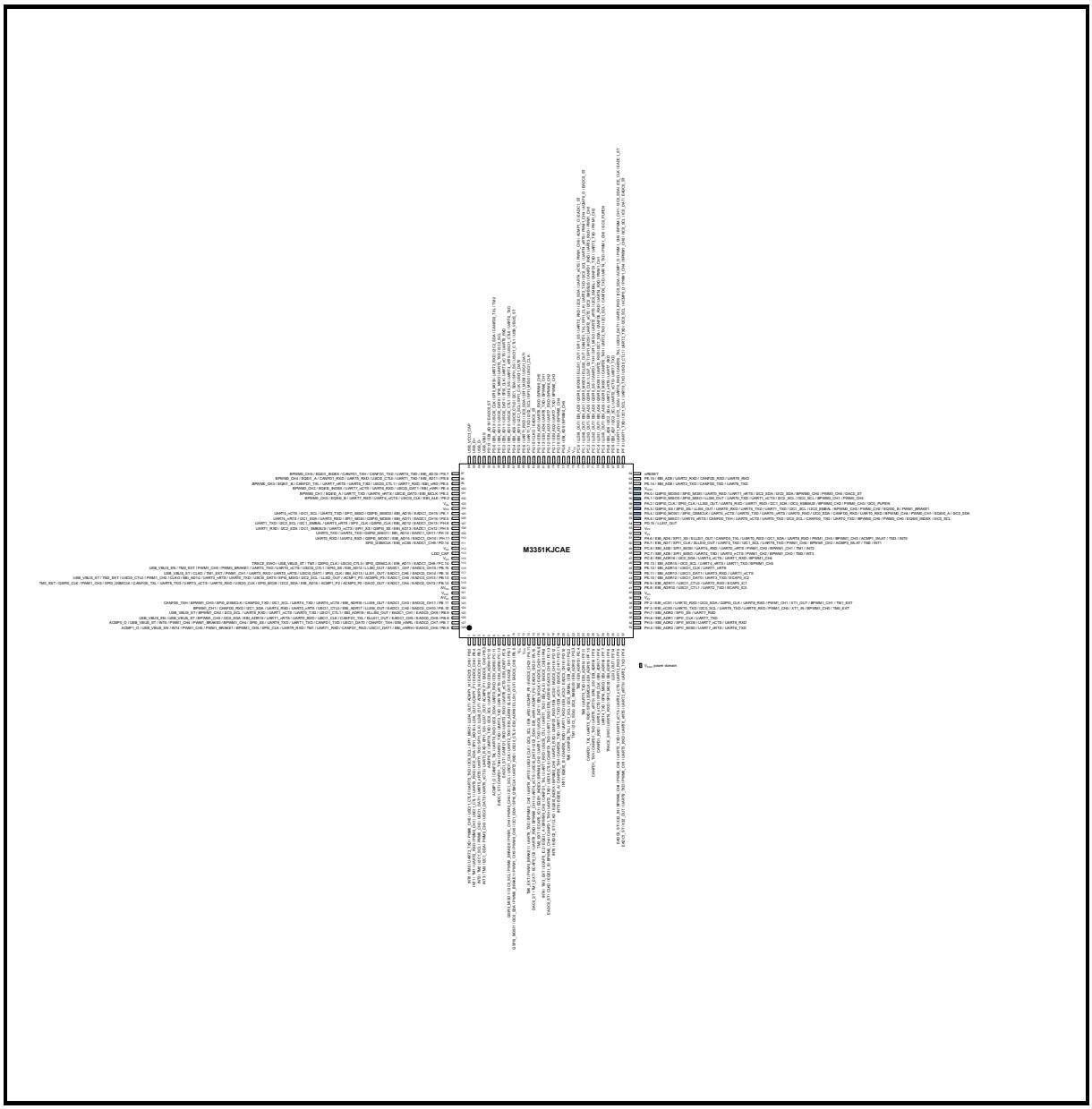


Figure 4.3-10 M3351KJCAE Multi-function Pin Diagram

Pin	Type	M3351KJCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3

Pin	Type	M3351KJCAE Pin Function
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / CANFD1_TXL / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART6_nRTS / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EADC1_ST
8	I/O	PC.9 / EBI_ADR7 / UART6_nCTS / UART3_RXD / CANFD1_RXD / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1
10	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / EBI_nRD / I2C2_SCL / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
14	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / EBI_nWR / I2C2_SDA / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT / DAC0_ST
15	I/O	PA.9 / EADC0_CH21 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / EQEI1_INDEX / ECAP0_IC1 / TM2_EXT
16	I/O	PA.8 / EADC0_CH20 / EBI_ALE / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / EQEI1_A / ECAP0_IC2 / TM3_EXT / INT4
17	I/O	PC.13 / EADC0_CH19 / EBI_ADR10 / UART1_RXD / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / CANFD1_TXH / BPWM0_CH4 / EQEI1_B / CLKO / EADC0_ST
18	I/O	PD.12 / EADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / INT6
20	I/O	PD.10 / EADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7
21	I/O	PG.2 / EBI_ADR11 / I2C0_SMBAL / I2C1_SCL / CANFD0_TXL / TM0
22	I/O	PG.3 / EBI_ADR12 / I2C0_SMBSUS / I2C1_SDA / TM1
23	I/O	PG.4 / EBI_ADR13 / TM2
24	I/O	PF.11 / EBI_ADR14 / UART5_TXD / TM3
25	I/O	PF.10 / EBI_ADR15 / SPI0_I2SMCLK / UART5_RXD / CANFD1_TXL
26	I/O	PF.9 / EBI_ADR16 / SPI0_SS / UART5_nRTS / CANFD1_TXD / CANFD1_TXH
27	I/O	PF.8 / EBI_ADR17 / SPI0_CLK / UART5_nCTS / CANFD1_RXD
28	I/O	PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD
29	I/O	PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / TRACE_SWO
30	I/O	PF.14 / LLSI3_OUT
31	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT / EADC1_ST
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD

Pin	Type	M3351KJCAE Pin Function
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / USCI1_CTL1 / UART2_TXD / ECAP0_IC0
42	I/O	PE.9 / EBI_ADR11 / USCI1_CTL0 / UART2_RXD / ECAP0_IC1
43	I/O	PE.10 / EBI_ADR12 / USCI1_DAT0 / UART3_TXD / ECAP0_IC2
44	I/O	PE.11 / EBI_ADR13 / USCI1_DAT1 / UART3_RXD / UART1_nCTS
45	I/O	PE.12 / EBI_ADR14 / USCI1_CLK / UART1_nRTS
46	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / BPWM1_CH5
47	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / BPWM1_CH4
48	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / EBI_AD7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
51	I/O	PA.6 / EBI_AD6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	I/O	PD.15 / LLSI7_OUT
55	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX / I3C0_SCL
56	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A / I3C0_SDA
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3 / I3C0_PUPEN
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / PWM0_CH4
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / PWM0_CH5 / DAC0_ST
61	P	V_{DDIO}
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD

Pin	Type	M3351KJCAE Pin Function
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / I3C0_SCL / ICE_DAT / EADC0_ST
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / I3C0_SDA / ICE_CLK / EADC1_ST
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD
69	I/O	PC.5 / LLSI0_OUT / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0 / I3C0_PUPEN
70	I/O	PC.4 / LLSI1_OUT / EBI_AD4 / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
71	I/O	PC.3 / LLSI2_OUT / EBI_AD3 / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
72	I/O	PC.2 / LLSI3_OUT / EBI_AD2 / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
73	I/O	PC.1 / LLSI8_OUT / EBI_AD1 / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
74	I/O	PC.0 / LLSI9_OUT / EBI_AD0 / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O / EADC1_ST
75	P	V_{SS}
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / BPWM0_CH5
78	I/O	PG.10 / EBI_AD1 / BPWM0_CH4
79	I/O	PG.11 / EBI_AD2 / UART7_TXD / BPWM0_CH3
80	I/O	PG.12 / EBI_AD3 / UART7_RXD / BPWM0_CH2
81	I/O	PG.13 / EBI_AD4 / UART6_TXD / BPWM0_CH1
82	I/O	PG.14 / EBI_AD5 / UART6_RXD / BPWM0_CH0
83	I/O	PG.15 / CLKO / EADC0_ST
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1
86	I/O	PD.5 / EBI_AD15 / I2C1_SCL / SPI1_CLK / USCI1_DAT0
87	I/O	PD.4 / EBI_AD5 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / USB_VBUS_ST
88	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
89	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
90	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
91	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / CANFD0_TXL / TM2
92	I/O	PD.13 / EBI_AD10 / EADC0_ST
93	P	USB_VBUS
94	A	USB_D-

Pin	Type	M3351KJCAE Pin Function
95	A	USB_D+
96	A	USB_VCC3_CAP
97	I/O	PE.7 / EBI_AD10 / UART5_TXD / CANFD1_TXD / CANFD1_TXH / EQEI1_INDEX / BPWM0_CH5
98	I/O	PE.6 / EBI_AD11 / UART1_TXD / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / BPWM0_CH4
99	I/O	PE.5 / EBI_nRD / UART1_RXD / USCI0_CTL1 / UART6_TXD / UART7_nRTS / CANFD1_TXL / EQEI1_B / BPWM0_CH3
100	I/O	PE.4 / EBI_nWR / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / BPWM0_CH2
101	I/O	PE.3 / EBI_MCLK / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / BPWM0_CH1
102	I/O	PE.2 / EBI_ALE / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / BPWM0_CH0
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EADC1_CH15 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS
106	I/O	PE.0 / EADC1_CH14 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS
107	I/O	PH.8 / EADC1_CH13 / EBI_AD12 / QSPI0_CLK / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD
108	I/O	PH.9 / EADC1_CH12 / EBI_AD13 / QSPI0_SS / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD
109	I/O	PH.10 / EADC1_CH11 / EBI_AD14 / QSPI0_MISO1 / UART4_TXD / UART0_TXD
110	I/O	PH.11 / EADC1_CH10 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD
111	I/O	PD.14 / EADC1_CH9 / EBI_nCS0 / SPI0_I2SMCLK
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EADC1_CH8 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
116	I/O	PB.15 / EADC0_CH15 / EADC1_CH7 / LLSI0_OUT / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
117	I/O	PB.14 / EADC0_CH14 / EADC1_CH6 / LLSI1_OUT / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
118	I/O	PB.13 / EADC0_CH13 / EADC1_CH5 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / I2C2_SCL / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / EBI_AD14 / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
119	I/O	PB.12 / EADC0_CH12 / EADC1_CH4 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / I2C2_SDA / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}

Pin	Type	M3351KJCAE Pin Function
123	I/O	PB.11 / EADC0_CH11 / EADC1_CH3 / LLSI8_OUT / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
124	I/O	PB.10 / EADC0_CH10 / EADC1_CH2 / LLSI9_OUT / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
125	I/O	PB.9 / EADC0_CH9 / EADC1_CH1 / ELLSI0_OUT / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
126	I/O	PB.8 / EADC0_CH8 / EADC1_CH0 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / EBI_ADR19 / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
127	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.3-10 M3351KJCAE Multi-function Pin Table

4.4 M3351xG7 Multi-function Pin Diagram

4.4.1 QFN33-Pin Multi-function Pin Diagram

4.4.1.1 M3351ZG7AE

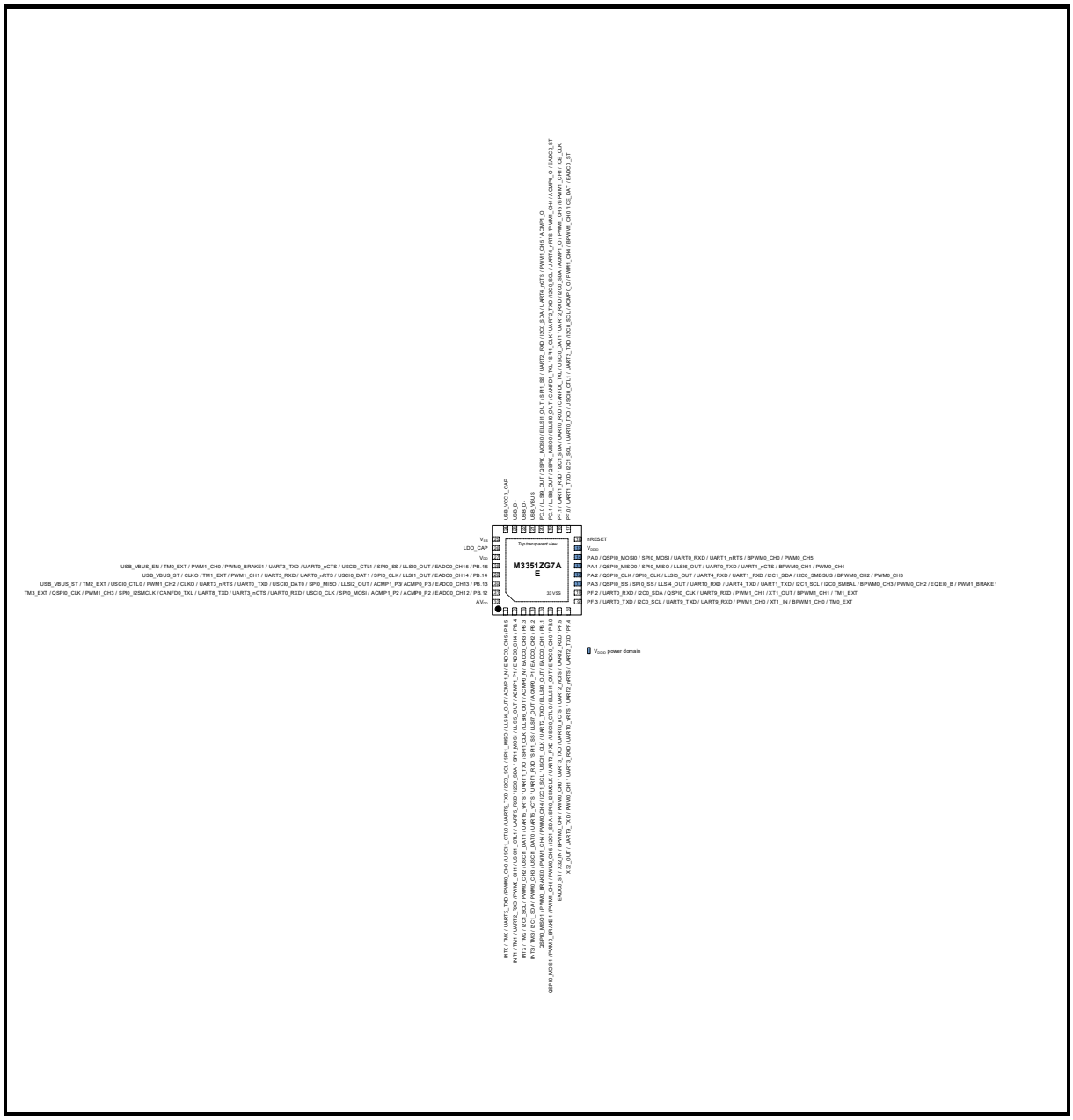


Figure 4.4-1 M3351ZG7AE Multi-function Pin Diagram

Pin	Type	M3351ZG7AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0

Pin	Type	M3351ZG7AE Pin Function
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / QSPI0_MOSI1
7	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
8	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT
9	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
10	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
11	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
12	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3
13	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4
14	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
15	P	V_{DDIO}
16	I	nRESET
17	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / ICE_DAT / EADC0_ST
18	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / ICE_CLK
19	I/O	PC.1 / LLSI8_OUT / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
20	I/O	PC.0 / LLSI9_OUT / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O
21	P	USB_VBUS
22	A	USB_D-
23	A	USB_D+
24	A	USB_VCC3_CAP
25	P	V_{SS}
26	A	LDO_CAP
27	P	V_{DD}
28	I/O	PB.15 / EADC0_CH15 / LLSI0_OUT / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD /

Pin	Type	M3351ZG7AE Pin Function
		PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
29	I/O	PB.14 / EADC0_CH14 / LLSI1_OUT / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
30	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
31	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
32	P	AV_{DD}
33	P	V_{SS}

Table 4.4-1 M3351YG7AE Multi-function Pin Table

4.4.2 QFN48-Pin Multi-function Pin Diagram

4.4.2.1 M3351YG7AE

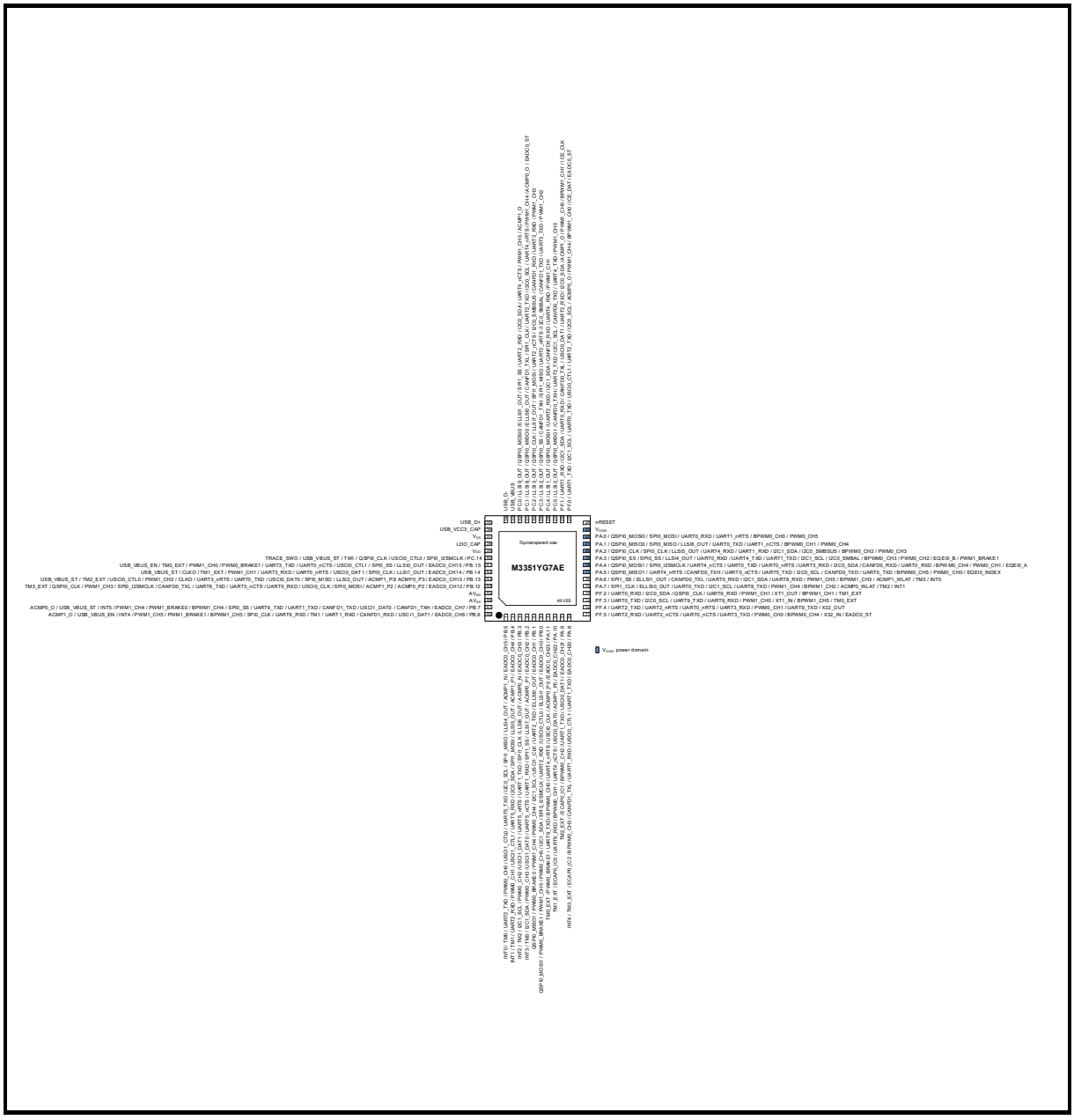


Figure 4.4-2 M3351YG7AE Multi-function Pin Diagram

Pin	Type	M3351YG7AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351YG7AE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT
9	I/O	PA.9 / EADC0_CH21 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0
28	I/O	PC.4 / LLSI1_OUT / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD /

Pin	Type	M3351YG7AE Pin Function
		PWM1_CH1
29	I/O	PC.3 / LLSI2_OUT / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / LLSI0_OUT / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / LLSI1_OUT / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
49	P	V_{SS}

Table 4.4-2 M3351YG7AE Multi-function Pin Table

4.4.3 LQFN48-Pin Multi-function Pin Diagram

4.4.3.1 M3351LG7AE

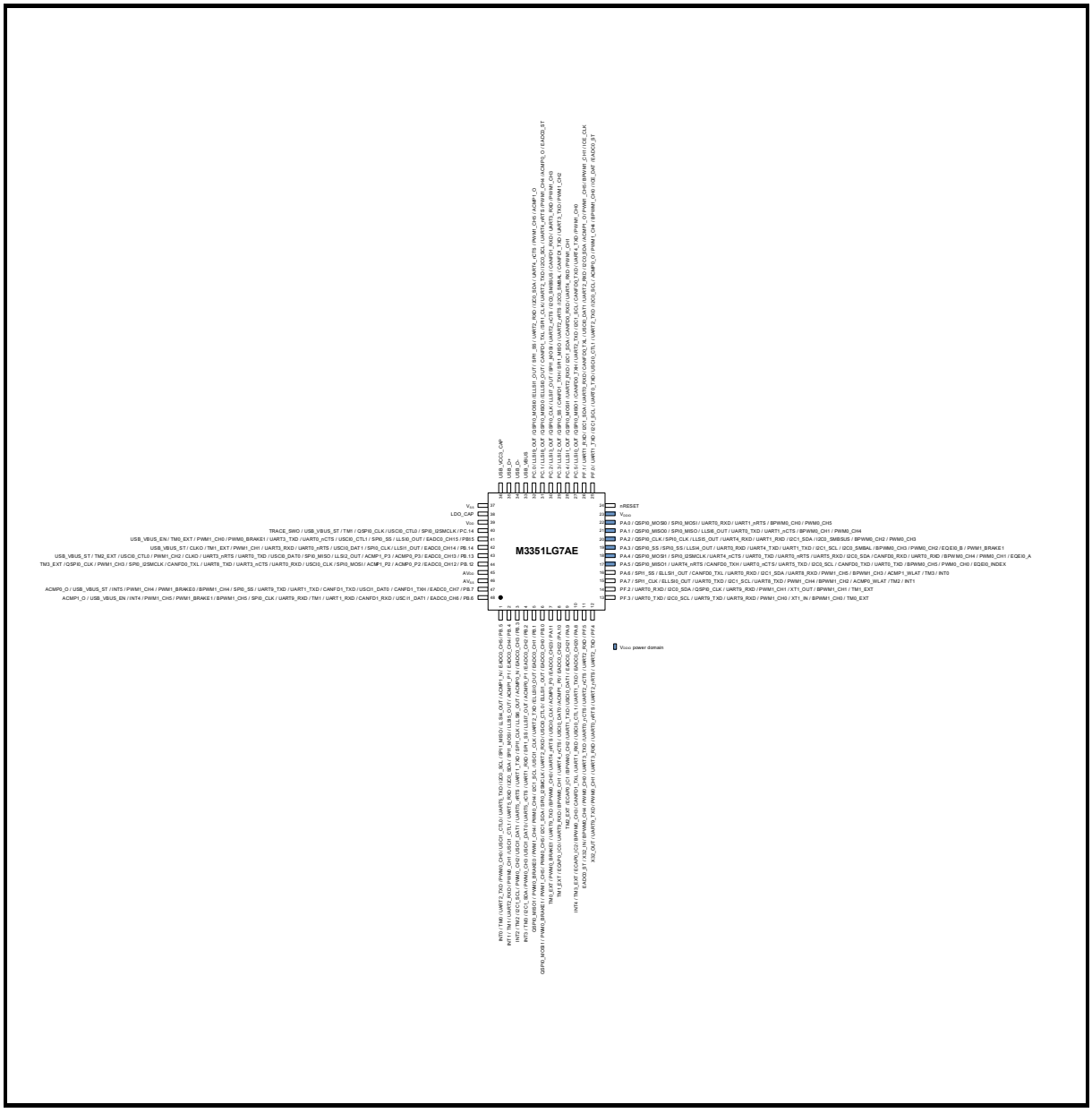


Figure 4.4-3 M3351LG7AE Multi-function Pin Diagram

Pin	Type	M3351LG7AE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2

Pin	Type	M3351LG7AE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
5	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / QSPI0_MOSI1
7	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
8	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT
9	I/O	PA.9 / EADC0_CH21 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EADC0_CH20 / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0
28	I/O	PC.4 / LLSI1_OUT / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD /

Pin	Type	M3351LG7AE Pin Function
		PWM1_CH1
29	I/O	PC.3 / LLSI2_OUT / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
30	I/O	PC.2 / LLSI3_OUT / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
31	I/O	PC.1 / LLSI8_OUT / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
32	I/O	PC.0 / LLSI9_OUT / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O
33	P	USB_VBUS
34	A	USB_D-
35	A	USB_D+
36	A	USB_VCC3_CAP
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
41	I/O	PB.15 / EADC0_CH15 / LLSI0_OUT / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
42	I/O	PB.14 / EADC0_CH14 / LLSI1_OUT / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O

Table 4.4-3 M3351YG7AE Multi-function Pin Table

4.4.4 LQFN64-Pin Multi-function Pin Diagram

4.4.4.1 M3351SG7AE

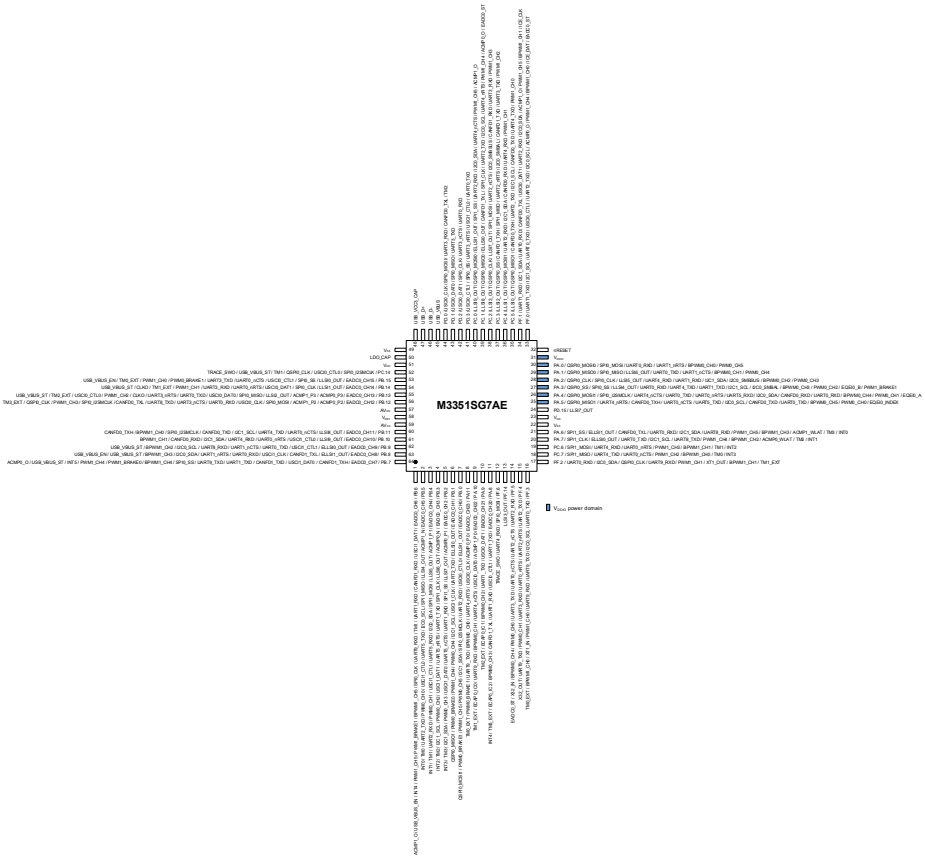


Figure 4.4-4 M3351SG7AE Multi-function Pin Diagram

Pin	Type	M3351SG7AE Pin Function
1	I/O	PB.6 / EADC0_CH6 / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / TM1 / UART9_RXD / SPI0_CLK / BPWM1_CH5 / PWM1_BRAKE1 / PWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / LLSI4_OUT / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / PWM0_CH0 / UART2_TXD / TM0 / INT0
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / LLSI5_OUT / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / PWM0_CH1 / UART2_RXD / TM1 / INT1

Pin	Type	M3351SG7AE Pin Function
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / LLSI6_OUT / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / PWM0_CH2 / I2C1_SCL / TM2 / INT2
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / LLSI7_OUT / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / PWM0_CH3 / I2C1_SDA / TM3 / INT3
6	I/O	PB.1 / EADC0_CH1 / ELLSI0_OUT / UART2_TXD / USCI1_CLK / I2C1_SCL / PWM0_CH4 / PWM1_CH4 / PWM0_BRAKE0 / QSPI0_MISO1
7	I/O	PB.0 / EADC0_CH0 / ELLSI1_OUT / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PWM0_CH5 / PWM1_CH5 / PWM0_BRAKE1 / QSPI0_MOSI1
8	I/O	PA.11 / EADC0_CH23 / ACMP0_P0 / USCI0_CLK / UART4_nRTS / BPWM0_CH0 / UART9_TXD / PWM0_BRAKE1 / TM0_EXT
9	I/O	PA.10 / EADC0_CH22 / ACMP1_P0 / USCI0_DAT0 / UART4_nCTS / BPWM0_CH1 / UART9_RXD / ECAP0_IC0 / TM1_EXT
10	I/O	PA.9 / EADC0_CH21 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT
11	I/O	PA.8 / EADC0_CH20 / UART1_TXD / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / INT4
12	I/O	PF.6 / SPI0_MOSI / UART4_RXD / TRACE_SWO
13	I/O	PF.14 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / PWM0_CH0 / BPWM0_CH4 / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / PWM0_CH1 / UART9_TXD / X32_OUT
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / UART9_TXD / UART9_RXD / PWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / PWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
18	I/O	PC.7 / SPI1_MISO / UART4_TXD / UART0_nCTS / PWM1_CH2 / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / SPI1_MOSI / UART4_RXD / UART0_nRTS / PWM1_CH3 / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / SPI1_CLK / ELLSI0_OUT / UART0_TXD / I2C1_SCL / UART8_TXD / PWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / ELLSI1_OUT / CANFD0_TXL / UART0_RXD / I2C1_SDA / UART8_RXD / PWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / LLSI7_OUT
25	I/O	PA.5 / QSPI0_MISO1 / UART4_nRTS / CANFD0_TXH / UART0_nCTS / UART5_TXD / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / PWM0_CH0 / EQEI0_INDEX
26	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART4_nCTS / UART0_TXD / UART0_nRTS / UART5_RXD / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / PWM0_CH1 / EQEI0_A
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / LLSI4_OUT / UART0_RXD / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / PWM0_CH2 / EQEI0_B / PWM1_BRAKE1
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / LLSI5_OUT / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / PWM0_CH3
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / LLSI6_OUT / UART0_TXD / UART1_nCTS / BPWM0_CH1 / PWM0_CH4

Pin	Type	M3351SG7AE Pin Function
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0 / PWM0_CH5
31	P	V_{DDIO}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / USCI0_CTL1 / UART2_TXD / I2C0_SCL / ACMP0_O / PWM1_CH4 / BPWM1_CH0 / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / CANFD0_TXL / USCI0_DAT1 / UART2_RXD / I2C0_SDA / ACMP1_O / PWM1_CH5 / BPWM1_CH1 / ICE_CLK
35	I/O	PC.5 / LLSI0_OUT / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / PWM1_CH0
36	I/O	PC.4 / LLSI1_OUT / QSPI0_MOSI1 / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / PWM1_CH1
37	I/O	PC.3 / LLSI2_OUT / QSPI0_SS / CANFD1_TXH / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / PWM1_CH2
38	I/O	PC.2 / LLSI3_OUT / QSPI0_CLK / LLSI7_OUT / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / PWM1_CH3
39	I/O	PC.1 / LLSI8_OUT / QSPI0_MISO0 / ELLSI0_OUT / CANFD1_TXL / SPI1_CLK / UART2_TXD / I2C0_SCL / UART4_nRTS / PWM1_CH4 / ACMP0_O / EADC0_ST
40	I/O	PC.0 / LLSI9_OUT / QSPI0_MOSI0 / ELLSI1_OUT / SPI1_SS / UART2_RXD / I2C0_SDA / UART4_nCTS / PWM1_CH5 / ACMP1_O
41	I/O	PD.3 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD
42	I/O	PD.2 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD
43	I/O	PD.1 / USCI0_DAT0 / SPI0_MISO / UART3_TXD
44	I/O	PD.0 / USCI0_CLK / SPI0_MOSI / UART3_RXD / CANFD0_TXL / TM2
45	P	USB_VBUS
46	A	USB_D-
47	A	USB_D+
48	A	USB_VCC3_CAP
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TM1 / USB_VBUS_ST / TRACE_SWO
53	I/O	PB.15 / EADC0_CH15 / LLSI0_OUT / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / PWM0_BRAKE1 / PWM1_CH0 / TM0_EXT / USB_VBUS_EN
54	I/O	PB.14 / EADC0_CH14 / LLSI1_OUT / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / PWM1_CH1 / TM1_EXT / CLKO / USB_VBUS_ST
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / LLSI2_OUT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / PWM1_CH2 / USCI0_CTL0 / TM2_EXT / USB_VBUS_ST
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / UART8_TXD / CANFD0_TXL / SPI0_I2SMCLK / PWM1_CH3 / QSPI0_CLK / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}

Pin	Type	M3351SG7AE Pin Function
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / LLSI8_OUT / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / CANFD0_TXH
61	I/O	PB.10 / EADC0_CH10 / LLSI9_OUT / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1
62	I/O	PB.9 / EADC0_CH9 / ELLSI0_OUT / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART8_RXD / I2C0_SCL / BPWM1_CH2 / USB_VBUS_ST
63	I/O	PB.8 / EADC0_CH8 / ELLSI1_OUT / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C0_SDA / BPWM1_CH3 / USB_VBUS_ST / USB_VBUS_EN
64	I/O	PB.7 / EADC0_CH7 / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / UART9_TXD / SPI0_SS / BPWM1_CH4 / PWM1_BRAKE0 / PWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O

Table 4.4-4 M3351YG7AE Multi-function Pin Table

4.5 Pin Mapping Table

4.5.1 M3351 Series Mapping Table

	M3351 Series					
Pin Name	M3351ZG7AE	M3351LICAE M3351LJCAE M3351LG7AE	M3351YICAE M3351YJCAE M3351YG7AE	M3351SICAE M3351SJCAE M3351SG7AE	M3351VICAE M3351VJCAE	M3351KICAE M3351KJCAE
PB.5	1	1	1	2	1	1
PB.4	2	2	2	3	2	2
PB.3	3	3	3	4	3	3
PB.2	4	4	4	5	4	4
PC.12					5	5
PC.11					6	6
PC.10					7	7
PC.9					8	8
PB.1	5	5	5	6	9	9
PB.0	6	6	6	7	10	10
V_{SS}					11	11
V_{DD}					12	12
PA.11		7	7	8	13	13
PA.10		8	8	9	14	14
PA.9		9	9	10	15	15
PA.8		10	10	11	16	16
PC.13						17
PD.12					17	18
PD.11					18	19
PD.10					19	20
PG.2						21
PG.3						22
PG.4						23
PF.11						24
PF.10						25
PF.9						26
PF.8						27
PF.7					20	28
PF.6				12	21	29
PF.14				13	22	30

PF.5	7	11	11	14	23	31
PF.4	8	12	12	15	24	32
PH.4						33
PH.5						34
PH.6						35
PH.7						36
PF.3	9	13	13	16	25	37
PF.2	10	14	14	17	26	38
V_{SS}						39
V_{DD}						40
PE.8					27	41
PE.9					28	42
PE.10					29	43
PE.11					30	44
PE.12					31	45
PE.13					32	46
PC.8					33	47
PC.7				18	34	48
PC.6				19	35	49
PA.7		15	15	20	36	50
PA.6		16	16	21	37	51
V_{SS}				22	38	52
V_{DD}				23	39	53
PD.15				24	40	54
PA.5		17	17	25	41	55
PA.4		18	18	26	42	56
PA.3	11	19	19	27	43	57
PA.2	12	20	20	28	44	58
PA.1	13	21	21	29	45	59
PA.0	14	22	22	30	46	60
V_{DDIO}	15	23	23	31	47	61
PE.14					48	62
PE.15					49	63
nRESET	16	24	24	32	50	64
PF.0	17	25	25	33	51	65
PF.1	18	26	26	34	52	66

PD.9					53	67
PD.8					54	68
PC.5		27	27	35	55	69
PC.4		28	28	36	56	70
PC.3		29	29	37	57	71
PC.2		30	30	38	58	72
PC.1	19	31	31	39	59	73
PC.0	20	32	32	40	60	74
V_{SS}					61	75
V_{DD}					62	76
PG.9						77
PG.10						78
PG.11						79
PG.12						80
PG.13						81
PG.14						82
PG.15						83
PD.7					63	84
PD.6					64	85
PD.5					65	86
PD.4					66	87
PD.3				41	67	88
PD.2				42	68	89
PD.1				43	69	90
PD.0				44	70	91
PD.13					71	92
USB_VBUS	21	33	33	45	72	93
USB_D-	22	34	34	46	73	94
USB_D+	23	35	35	47	74	95
USB_V_{CC3_CAP}	24	36	36	48	75	96
PE.7					76	97
PE.6					77	98
PE.5					78	99
PE.4					79	100
PE.3					80	101
PE.2					81	102

V_{SS}		37	37	49		103
V_{DD}						104
PE.1					82	105
PE.0					83	106
PH.8						107
PH.9						108
PH.10						109
PH.11						110
PD.14						111
V_{SS}	25				84	112
LDO_CAP	26	38	38	50	85	113
V_{DD}	27	39	39	51	86	114
PC.14		40	40	52	87	115
PB.15	28	41	41	53	88	116
PB.14	29	42	42	54	89	117
PB.13	30	43	43	55	90	118
PB.12		44	44	56	91	119
AV_{DD}	32	45	45	57	92	120
V_{REF}	32	45	45	58	93	121
AV_{SS}		46	46	59	94	122
PB.11				60	95	123
PB.10				61	96	124
PB.9				62	97	125
PB.8				63	98	126
PB.7		47	47	64	99	127
PB.6		48	48	1	100	128
V_{SS}	33	49				

4.6 Pin Functional Description

4.6.1 M3351 Series Summary Function Pin Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CANFD0	CANFD0_RXD	I	CANFD0 bus receiver input.
	CANFD0_TXD	O	CANFD0 bus transmitter output.
	CANFD0_TXH	O	CANFD0 bus transmitter high level line digital output.
	CANFD0_TXL	O	CANFD0 bus transmitter low level line digital output.
CANFD1	CANFD1_RXD	I	CANFD1 bus receiver input.
	CANFD1_TXD	O	CANFD1 bus transmitter output.

Group	Pin Name	Type	Description
	CANFD1_TXH	O	CANFD1 bus transmitter high level line digital output.
	CANFD1_TXL	O	CANFD1 bus transmitter low level line digital output.
CLKO	CLKO	O	Clock Out.
DAC0	DAC0_OUT	A	DAC0 channel analog output.
	DAC0_ST	I	DAC0 external trigger input.
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_CH16	A	EADC0 channel 16 analog input.
	EADC0_CH17	A	EADC0 channel 17 analog input.
	EADC0_CH18	A	EADC0 channel 18 analog input.
	EADC0_CH19	A	EADC0 channel 19 analog input.
	EADC0_CH20	A	EADC0 channel 20 analog input.
	EADC0_CH21	A	EADC0 channel 21 analog input.
	EADC0_CH22	A	EADC0 channel 22 analog input.
	EADC0_CH23	A	EADC0 channel 23 analog input.
	EADC0_ST	I	EADC0 external trigger input.
EADC1	EADC1_CH0	A	EADC1 channel 0 analog input.
	EADC1_CH1	A	EADC1 channel 1 analog input.
	EADC1_CH2	A	EADC1 channel 2 analog input.
	EADC1_CH3	A	EADC1 channel 3 analog input.
	EADC1_CH4	A	EADC1 channel 4 analog input.

Group	Pin Name	Type	Description
	EADC1_CH5	A	EADC1 channel 5 analog input.
	EADC1_CH6	A	EADC1 channel 6 analog input.
	EADC1_CH7	A	EADC1 channel 7 analog input.
	EADC1_CH8	A	EADC1 channel 8 analog input.
	EADC1_CH9	A	EADC1 channel 9 analog input.
	EADC1_CH10	A	EADC1 channel 10 analog input.
	EADC1_CH11	A	EADC1 channel 11 analog input.
	EADC1_CH12	A	EADC1 channel 12 analog input.
	EADC1_CH13	A	EADC1 channel 13 analog input.
	EADC1_CH14	A	EADC1 channel 14 analog input.
	EADC1_CH15	A	EADC1 channel 15 analog input.
	EADC1_ST	I	EADC1 external trigger input.
EBI	EBI_AD0	I/O	EBI address/data bus bit 0.
	EBI_AD1	I/O	EBI address/data bus bit 1.
	EBI_AD2	I/O	EBI address/data bus bit 2.
	EBI_AD3	I/O	EBI address/data bus bit 3.
	EBI_AD4	I/O	EBI address/data bus bit 4.
	EBI_AD5	I/O	EBI address/data bus bit 5.
	EBI_AD6	I/O	EBI address/data bus bit 6.
	EBI_AD7	I/O	EBI address/data bus bit 7.
	EBI_AD8	I/O	EBI address/data bus bit 8.
	EBI_AD9	I/O	EBI address/data bus bit 9.
	EBI_AD10	I/O	EBI address/data bus bit 10.
	EBI_AD11	I/O	EBI address/data bus bit 11.
	EBI_AD12	I/O	EBI address/data bus bit 12.
	EBI_AD13	I/O	EBI address/data bus bit 13.
	EBI_AD14	I/O	EBI address/data bus bit 14.
	EBI_AD15	I/O	EBI address/data bus bit 15.
	EBI_ADR0	O	EBI address bus bit 0.
	EBI_ADR1	O	EBI address bus bit 1.
	EBI_ADR2	O	EBI address bus bit 2.
	EBI_ADR3	O	EBI address bus bit 3.
	EBI_ADR4	O	EBI address bus bit 4.
	EBI_ADR5	O	EBI address bus bit 5.
	EBI_ADR6	O	EBI address bus bit 6.

Group	Pin Name	Type	Description
	EBI_ADR7	O	EBI address bus bit 7.
	EBI_ADR8	O	EBI address bus bit 8.
	EBI_ADR9	O	EBI address bus bit 9.
	EBI_ADR10	O	EBI address bus bit 10.
	EBI_ADR11	O	EBI address bus bit 11.
	EBI_ADR12	O	EBI address bus bit 12.
	EBI_ADR13	O	EBI address bus bit 13.
	EBI_ADR14	O	EBI address bus bit 14.
	EBI_ADR15	O	EBI address bus bit 15.
	EBI_ADR16	O	EBI address bus bit 16.
	EBI_ADR17	O	EBI address bus bit 17.
	EBI_ADR18	O	EBI address bus bit 18.
	EBI_ADR19	O	EBI address bus bit 19.
	EBI_ALE	O	EBI address latch enable output pin.
	EBI_MCLK	O	EBI external clock output pin.
	EBI_nCS0	O	EBI chip select 0 output pin.
	EBI_nCS1	O	EBI chip select 1 output pin.
	EBI_nCS2	O	EBI chip select 2 output pin.
	EBI_nRD	O	EBI read enable output pin.
	EBI_nWR	O	EBI write enable output pin.
	EBI_nWRH	O	EBI high byte write enable output pin
	EBI_nWRL	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
ELLSI0	ELLSI0_OUT	O	Enhanced LED Lighting Strip Interface 0 output pin.
ELLSI1	ELLSI1_OUT	O	Enhanced LED Lighting Strip Interface 1 output pin.
EQEI0	EQEI0_A	I	EQEI0 phase A input.
	EQEI0_B	I	EQEI0 phase B input.
	EQEI0_INDEX	I	EQEI0 index input.
EQEI1	EQEI1_A	I	EQEI1 phase A input.
	EQEI1_B	I	EQEI1 phase B input.
	EQEI1_INDEX	I	EQEI1 index input.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.

Group	Pin Name	Type	Description
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin.
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin.
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
I3C0	I3C0_PUPEN	O	I3C0 pull-up resistor enable pin.
	I3C0_SCL	I/O	I3C0 serial clock pin.
	I3C0_SDA	I/O	I3C0 serial data pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
INT6	INT6	I	External interrupt 6 input pin.
INT7	INT7	I	External interrupt 7 input pin.
LLSI0	LLSI0_OUT	O	LED Lighting Strip Interface 0 output pin.
LLSI1	LLSI1_OUT	O	LED Lighting Strip Interface 1 output pin.
LLSI2	LLSI2_OUT	O	LED Lighting Strip Interface 2 output pin.
LLSI3	LLSI3_OUT	O	LED Lighting Strip Interface 3 output pin.
LLSI4	LLSI4_OUT	O	LED Lighting Strip Interface 4 output pin.
LLSI5	LLSI5_OUT	O	LED Lighting Strip Interface 5 output pin.
LLSI6	LLSI6_OUT	O	LED Lighting Strip Interface 6 output pin.
LLSI7	LLSI7_OUT	O	LED Lighting Strip Interface 7 output pin.
LLSI8	LLSI8_OUT	O	LED Lighting Strip Interface 8 output pin.
LLSI9	LLSI9_OUT	O	LED Lighting Strip Interface 9 output pin.
PWM0	PWM0_BRAKE0	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE1	I	PWM0 Brake 1 input pin.

Group	Pin Name	Type	Description
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
PWM1	PWM1_BRAKE0	I	PWM1 Brake 0 input pin.
	PWM1_BRAKE1	I	PWM1 Brake 1 input pin.
	PWM1_CH0	I/O	PWM1 channel 0 output/capture input.
	PWM1_CH1	I/O	PWM1 channel 1 output/capture input.
	PWM1_CH2	I/O	PWM1 channel 2 output/capture input.
	PWM1_CH3	I/O	PWM1 channel 3 output/capture input.
	PWM1_CH4	I/O	PWM1 channel 4 output/capture input.
	PWM1_CH5	I/O	PWM1 channel 5 output/capture input.
QEI1	QEI1_A	I	QEI1 phase A input.
	QEI1_B	I	QEI1 phase B input.
	QEI1_INDEX	I	QEI1 index input.
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I^2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.

Group	Pin Name	Type	Description
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TRACE	TRACE_SWO	O	Trace Single Wire output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
UART4	UART4_RXD	I	UART4 data receiver input pin.
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
UART5	UART5_RXD	I	UART5 data receiver input pin.
	UART5_TXD	O	UART5 data transmitter output pin.
	UART5_nCTS	I	UART5 clear to Send input pin.
	UART5_nRTS	O	UART5 request to Send output pin.
UART6	UART6_RXD	I	UART6 data receiver input pin.
	UART6_TXD	O	UART6 data transmitter output pin.
	UART6_nCTS	I	UART6 clear to Send input pin.
	UART6_nRTS	O	UART6 request to Send output pin.
UART7	UART7_RXD	I	UART7 data receiver input pin.

Group	Pin Name	Type	Description
	UART7_TXD	O	UART7 data transmitter output pin.
	UART7_nCTS	I	UART7 clear to Send input pin.
	UART7_nRTS	O	UART7 request to Send output pin.
UART8	UART8_RXD	I	UART8 data receiver input pin.
	UART8_TXD	O	UART8 data transmitter output pin.
UART9	UART9_RXD	I	UART9 data receiver input pin.
	UART9_TXD	O	UART9 data transmitter output pin.
USB	USB_VBUS_EN	O	USB external V_{BUS} regulator enable pin.
	USB_VBUS_ST	I	USB external V_{BUS} regulator status pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	I/O	USCI1 clock pin.
	USCI1_CTL0	I/O	USCI1 control 0 pin.
	USCI1_CTL1	I/O	USCI1 control 1 pin.
	USCI1_DAT0	I/O	USCI1 data 0 pin.
	USCI1_DAT1	I/O	USCI1 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_VBUS	P	Power supply from USB host or HUB.
	USB_VCC3_CAP	A	USB 3.3V LDO output. **Note:** This pin needs to be connected to a 1uF capacitor.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. **Note:** This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{DDIO}	P	Power supply for PA.0~PA.5.
	V_{REF}	A	ADC reference voltage input.

Group	Pin Name	Type	Description
			Note: This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

5 BLOCK DIAGRAM

5.1 M3351 Series Block Diagram

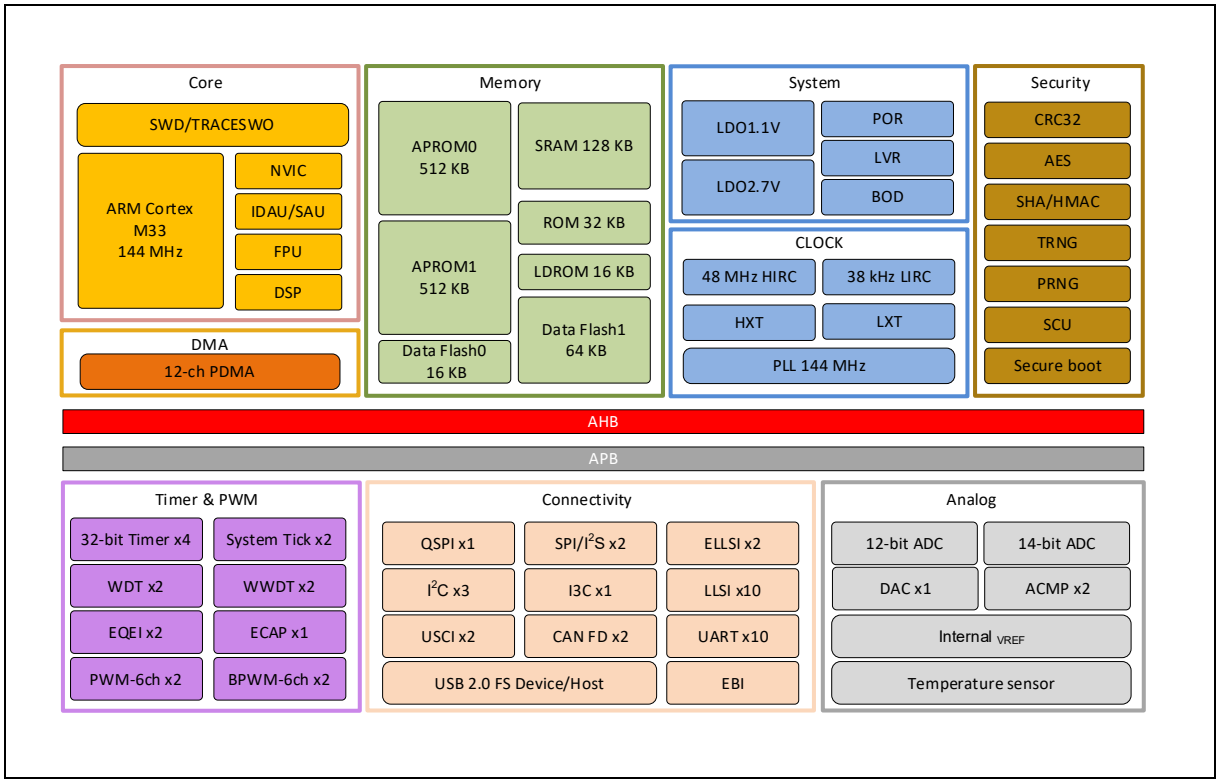


Figure 5.1-1 M3351 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM Cortex-M33 Core

The Cortex-M33 processor is a low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications. The processor is based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration. TrustZone security for hardware-enforced isolation, memory-protection units (MPUs) and a floating-point unit (FPU). Figure 6.1-1shows the functional controller of the processor.

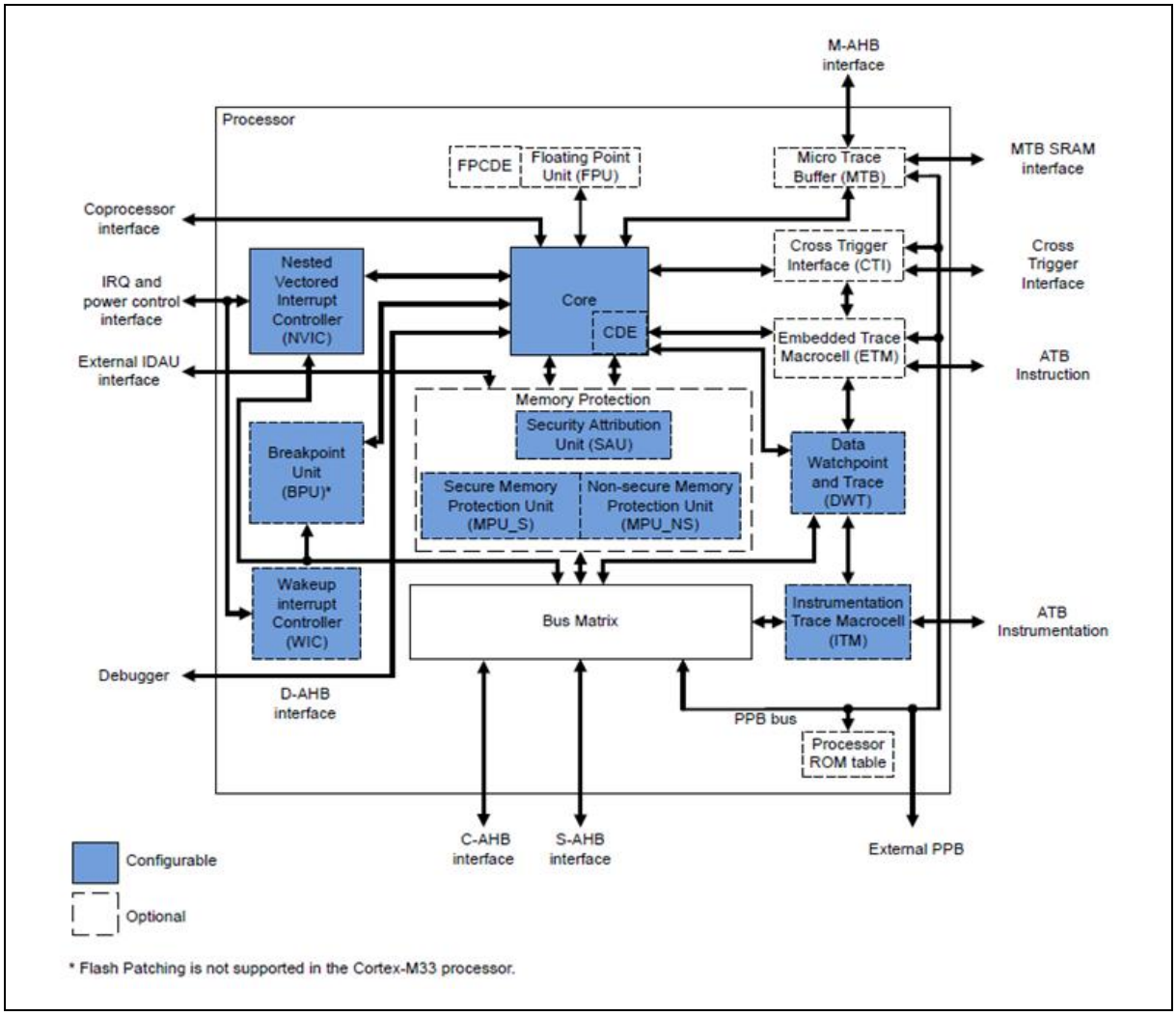


Figure 6.1-1 Cortex-M33 Block Diagram

Cortex-M33 processor features:

- The processor core provides:
  - Limited dual-issue of common 16-bit instruction pairs
  - Integer divide unit with support for operand-dependent early termination.
  - Support for interrupted continuable load and store multiple operations.
  - Load and store operations that both support precise bus errors.
- Floating Point Unit (FPU) provides:

- Instructions for single-precision (C programming language float type) data-processing operations.
- Instructions for double-precision (C double type) load and store operations.
- Combined multiply-add instructions for increased precision (Fused MAC).
- Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root.
- Hardware support for denormals and all IEEE Standard 754-2008 rounding modes.
- 32 32-bit single-precision registers or 16 64-bit double-precision registers.
- Lazy floating-point context save. Automated stacking of floating-point state is delayed until the ISR attempts to execute a floating-point instruction. This reduces the latency to enter the ISR and removes floating-point context save for ISRs that do not use floating-point.

- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Functions of the NVIC include:
  - External interrupts, configurable from 1 to 480 using a contiguous or non-contiguous mapping. This is configured at implementation
  - Configurable levels of interrupt priority from 8 to 256. This is configured at implementation.
  - Dynamic reprioritization of interrupts.
  - Priority grouping. This enables selection of preempting interrupt levels and non-preempting interrupt levels.
  - Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
- Debug support
  - Debug and trace components include a configurable Breakpoint Unit (BPU) for implementing breakpoints, and configurable Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling.
- Bus interfaces:
  - The System AHB (S-AHB) interface is used for any instruction fetch and data access to the memory-mapped SRAM, Peripheral, External RAM and External device, or Vendor_SYS regions of the Armv8-M memory map.
  - The Code AHB (C-AHB) interface is used for any instruction fetch and data access to the Code region of the Armv8-M memory map.
  - The External PPB (EPPB) APB interface enables access to CoreSight-compatible debug and trace components in a system connected to the processor.
  - The Debug AHB (D-AHB) slave interface allows a debugger access to registers, memory, and peripherals. The D-AHB interface provides debug access to the processor and the complete memory map.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M33 core only by writing 1 to CPURST (SYS_IPRST0[1])

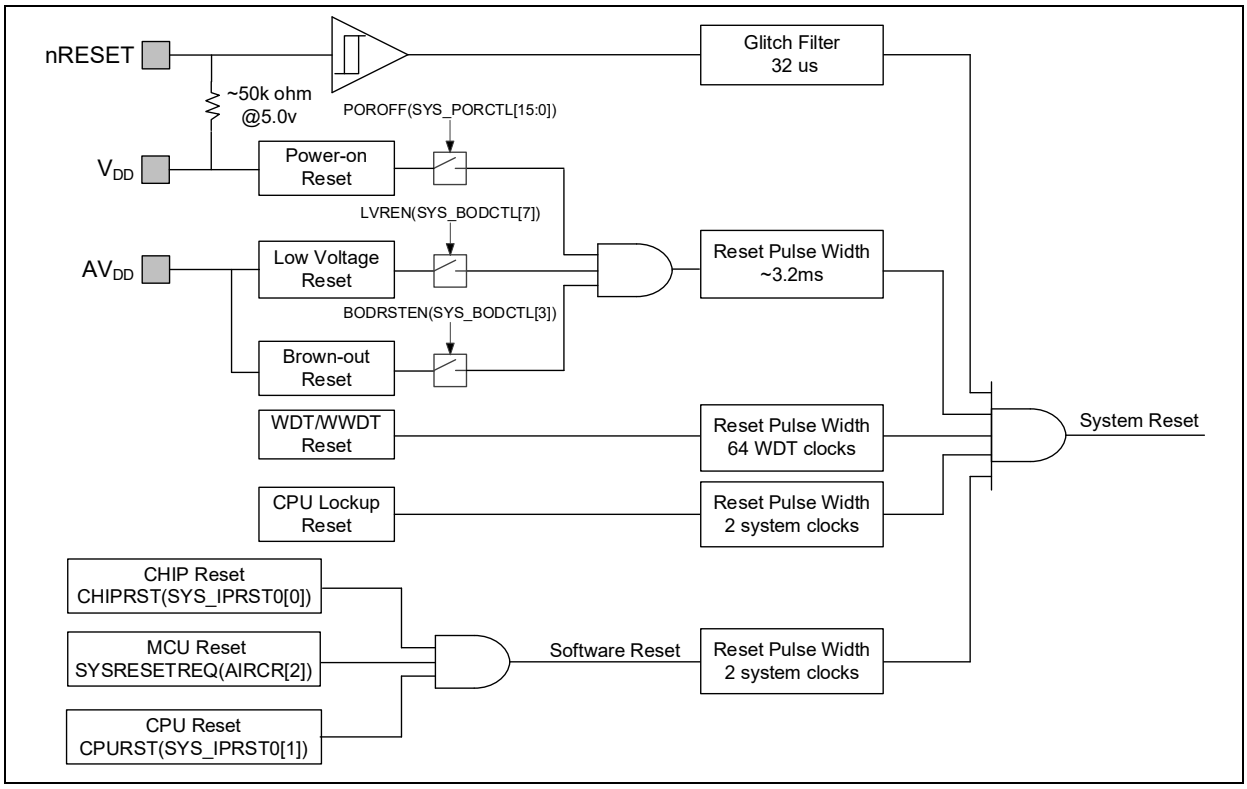


Figure 6.2-1 System Reset Sources

The Mask ROM which is built-in secure boot and ROM ISP function is the initial boot source after chip is powered on or cold reset. User can refer to Mask ROM application note for the detailed features and functions. System cold reset events include nRESET pin, WDT/WWDT, LVR, BOD and CHIP reset. Other reset events include MCU, CPU, Lockup reset and wake-up from Standby Power-down mode (SPD) are defined as warm reset events. Figure 6.2-2 shows the Reset Event State Machine.

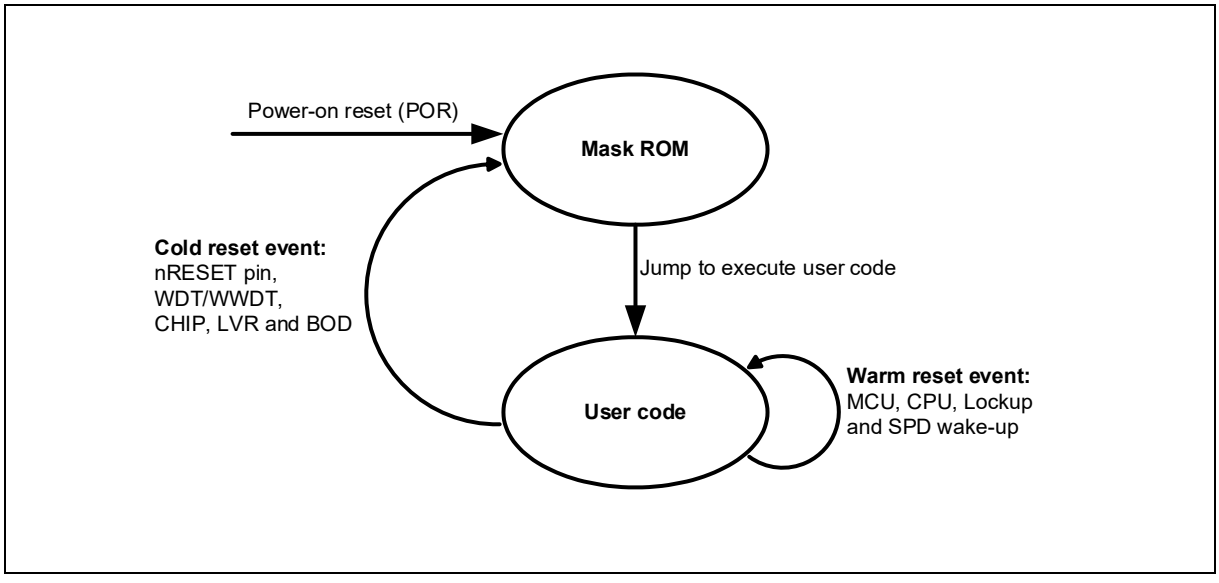


Figure 6.2-2 Reset Event State Machine

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M33 only; the other reset sources will reset Cortex-M33 and all peripherals. However, there are small

differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	nRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[19:16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	-
CLK_PCLKDIV	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
CLK_PLLCTL	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[4])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PDMSEL (CLK_PMUCTL[2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL	0x0800	0x0800	0x0800	0x0800	0x0800	0x0800	0x0800	-	-

except bit 1 and bit 7.									
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
FMC_CYCCTL	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than V_{ILR} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above V_{IHR} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-3 shows the nRESET reset waveform. Note that the nRESET de-glitch time is typically 300ns in SPD mode.

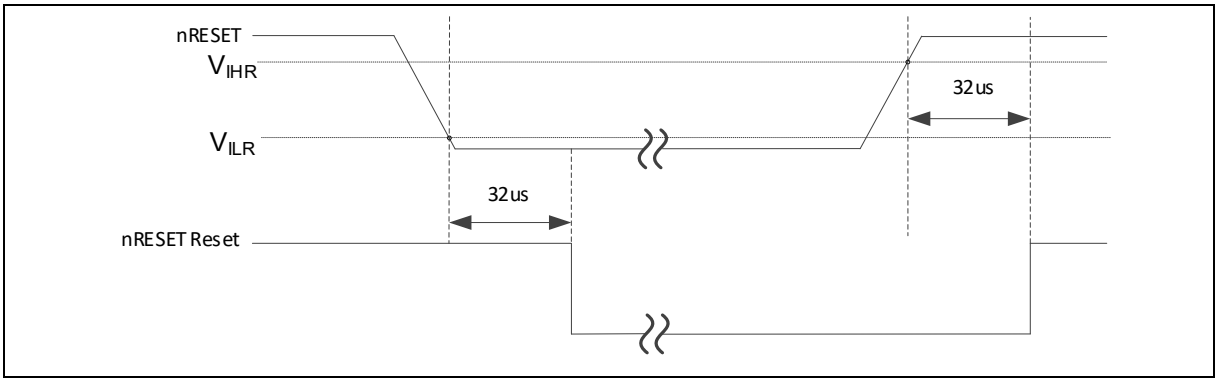


Figure 6.2-3 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-4 shows the power-on reset waveform.

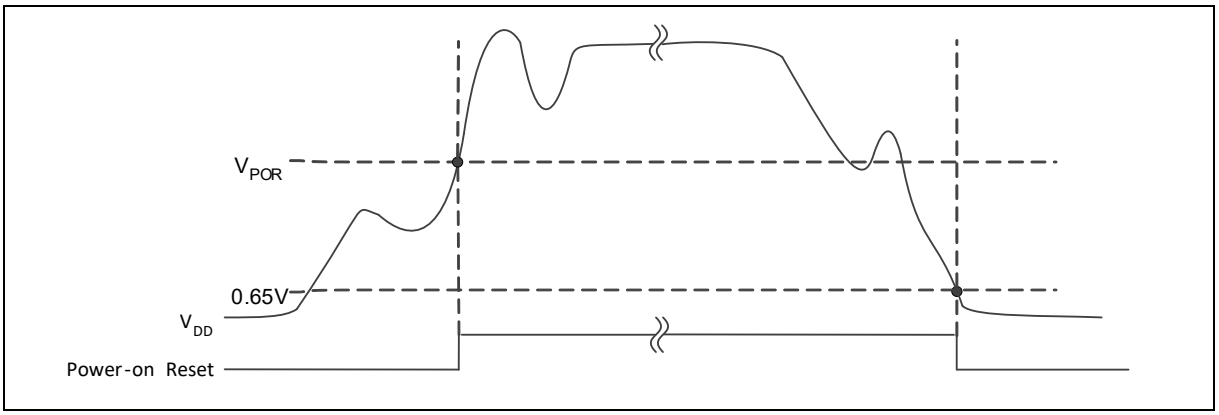


Figure 6.2-4 Power-on Reset (POR) Waveform

6.2.2.3 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 100us~200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-5 shows the Low Voltage Reset waveform.

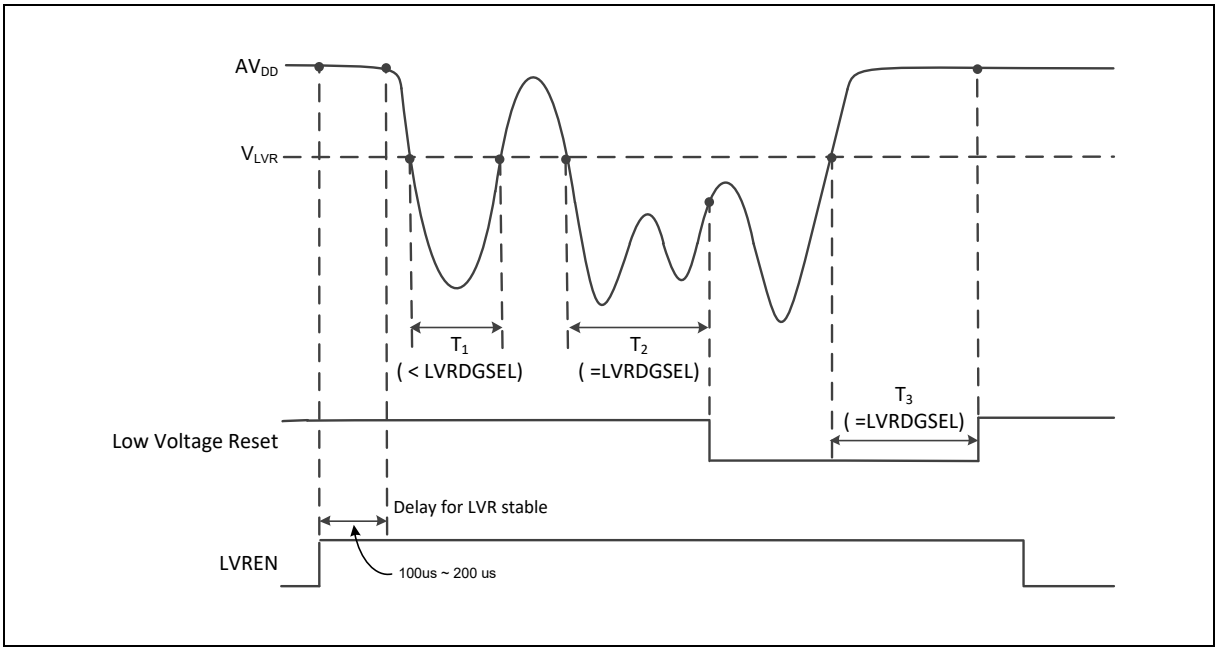


Figure 6.2-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 *Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[19:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default

value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-6 shows the Brown-out Detector waveform.

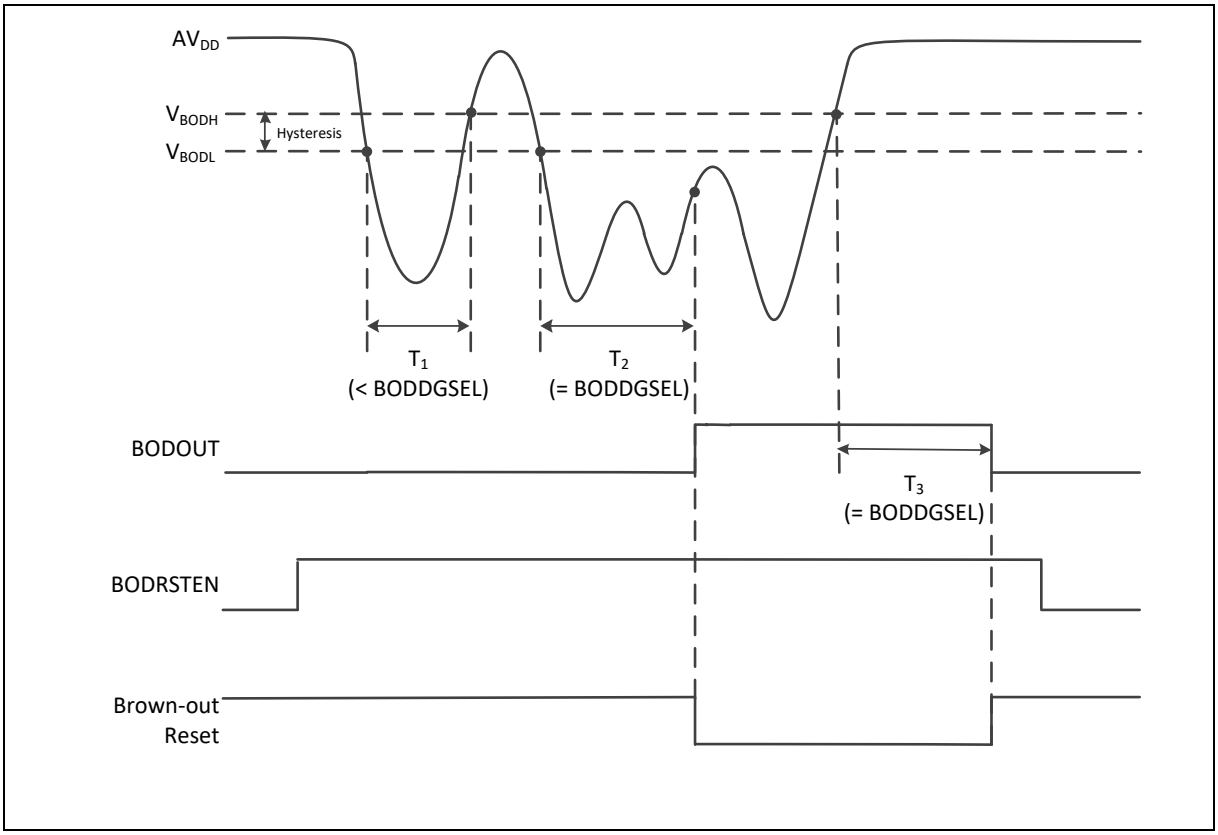


Figure 6.2-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex-M33 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and the Chip Booting Selection is automatically reloaded from CONFIG0[7] setting. User can set the

CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that the Chip Booting Selection will not be reloaded from CBS(CONFIG0[7]) setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator VDD_{11} and VDD_{33}. VDD_{11} provides power for digital operation and I/O pins; VDD_{33} provide power for Flash operation.
- I/O power from V_{DDIO} supplies the power for PA.0 ~ PA.5
- V_{BUS} supplies the power to the internal regulator which provides power to USB 2.0 transceiver power.

The outputs pin of internal voltage regulator VDD_{11} is LDO_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). The outputs pin of internal USB PHY voltage regulator is USB_VDD33. Figure 6.2-7 shows the NuMicro M3351 series power distribution.

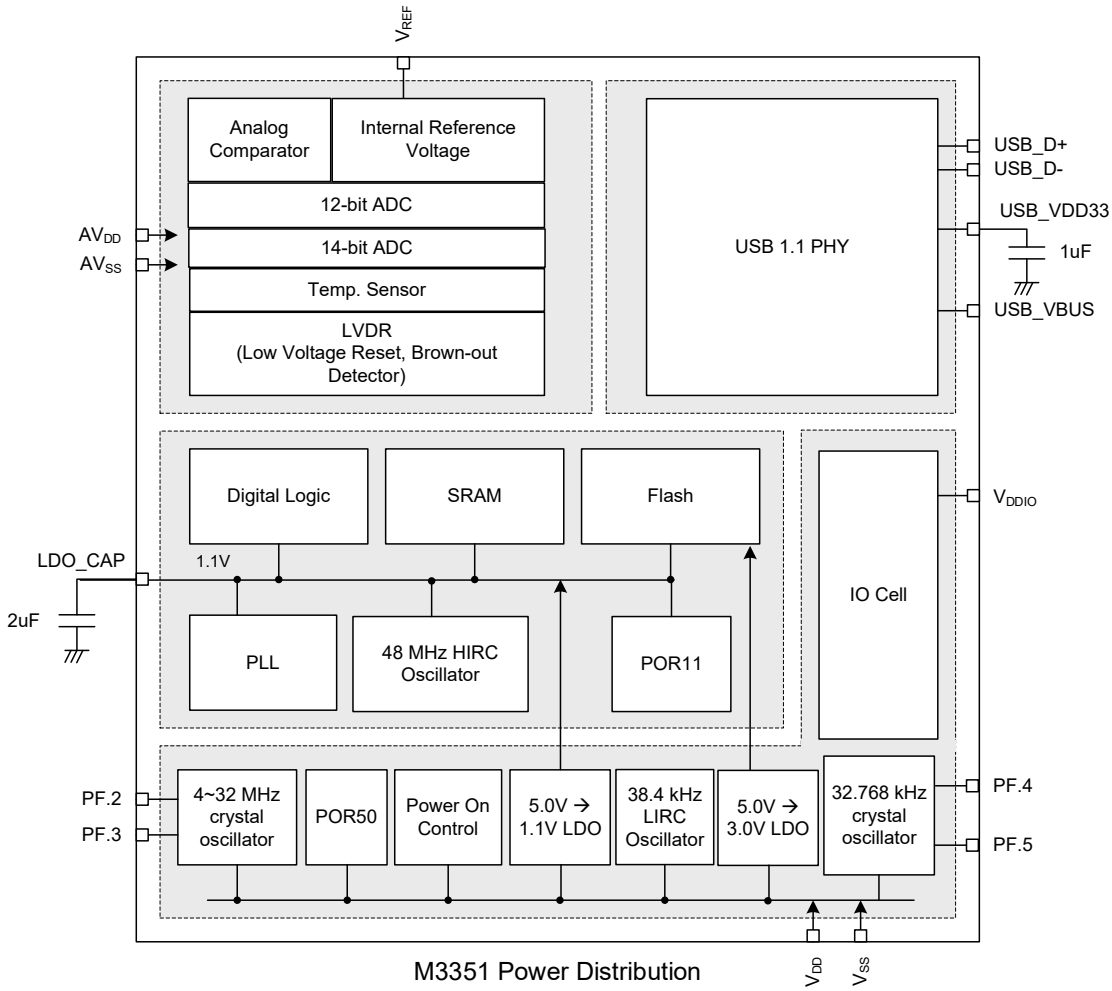


Figure 6.2-7 NuMicro M3351 Series Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M3351 series has power management unit to support several operating modes for saving power. Following are traditional Power-down modes as examples:

- Normal Power-down mode 0 (NPD0) is used for fast wake-up needs, in this power-down mode the analog circuits are in active mode and only the high-speed clock sources are disabled.
- Normal Power-down mode 1 (NPD1) is used light power saving needs, in this power-down mode the analog circuits are in low power mode and the high-speed clock sources are disabled.
- Normal Power-down mode 2 (NPD2) is used moderate power saving needs, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled and regulator output drop to low voltage.
- Standby Power-down mode 0 (SPD0) is used heavy power saving needs, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled, and the core power domain is power off.

- Standby Power-down mode 1 (SPD1) is used heavy power saving needs, in this power-down mode the analog circuits are in low power mode, the high-speed clock sources are disabled, regulator output drop to low voltage and the core power domain is power off.

Mode	CPU Operating and HCLK Maximum Speed (MHz)	APB and PCLK Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	144	72	1.1	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	CPU enter Sleep mode	1.1	Only CPU clock is disabled.
Normal Power-down mode 0 (NPD0)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.1	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode 1 (NPD1)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.1	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode 2 (NPD2)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode 0 (SPD0)	Power off	Power off	1.1	Only LIRC still enabled for wake-up timer usage. Only LXT still enabled for RTC function usage.
Standby Power-down mode 1 (SPD1)	Power off	Power off	0.9	Only LIRC still enabled for wake-up timer usage. Only LXT still enabled for RTC function usage.

Table 6.2-2 Power Mode Table

There are different power mode entry setting for each power mode, with different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running at normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Mode	Register/Instruction			
	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
NPD0	1	1	2	YES
NPD1	1	1	0	YES
NPD2	1	1	1	YES
SPD0	1	1	4	YES
SPD1	1	1	5	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retain.

Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, I3C, Timer, UART, BOD, GPIO, INT, USCI, USBD, USBH, ACMP.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Definition Table

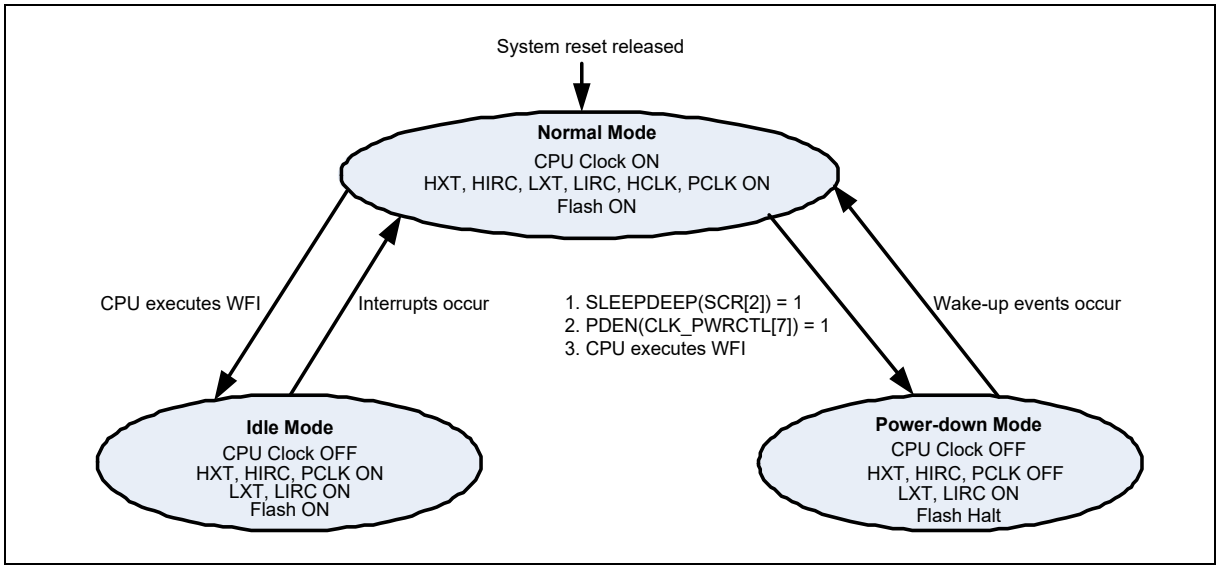


Figure 6.2-8 Power Mode State Machine

	Idle Mode	NPD0/1/2	SPD0/1
HXT	ON	Halt	Halt
HIRC	ON	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]
PLL	ON	Halt	Halt
HCLK/PCLK	ON	Halt	Halt
CPU	Halt	Halt	Halt
SRAM retention	ON	ON	ON/OFF[7]
FLASH	ON	Halt	Halt
TIMER	ON	ON/OFF[3]	Halt
WDT	ON	ON/OFF[4]	Halt
RTC	ON	ON/OFF[5]	ON/OFF[8]
UART	ON	ON/OFF[6]	Halt
Others	ON	Halt	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on software setting in normal mode.
2. LIRC ON or OFF depends on software setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
5. If RTC clock source is selected as LIRC/LXT and LIRC/LXT is on.
6. If UART clock source is selected as LXT and LXT is on.
7. SRAM retention size depends on software setting in normal mode.
8. If RTC clock source is selected as LXT and LXT is on.

Wake-up sources in Normal Power-down mode (NPD):

RTC, WDT, I²C, I3C, Timer, UART, USCI, BOD, GPIO, INT, USBD, USBH, ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode		Re-Entering Power-Down Mode Condition
		NPD0/1/2	SPD0/1	
BOD	Brown-Out Detector Reset / Interrupt	V	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	After software writes 1 to clear LVRRF (SYS_RSTSTS[3])
		-	V	After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
RST pin	RST pin Reset	V	-	After software writes 1 to clear PINRF (SYS_RSTSTS[1]).
		-	V	After software writes 1 (CLK_PMUSTS[31]) to clear RSTWK (CLK_PMUSTS[15]) when SPD mode is entered.
INT	External Interrupt	V	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear GPxWK0 (CLK_PMUSTS[11:8]) and GPxWK1 (CLK_PMUSTS[27:24]) when SPD mode is entered.
TIMER	Timer Interrupt	V	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD mode is entered.
CLKD	Clock fail interrupt	V		After software writes 1 to clear LXTFIF (CLK_CLKDSTS[1]) and HXTFIF (CLK_CLKDSTS[0])

WDT	WDT Interrupt	V	-	After software writes 1 to clear WKF (WDT_STATUS[1]) and IF (WDT_STATUS[0]).
RTC	Alarm Interrupt	V	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
	Wakeup by RTC tick time	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
UART	nCTS wake-up	V	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
I3C	Address match wake-up	V	-	Auto clear after an address mismatch or on STOP or RE-START followed by 0x7E.
USBD	1.Remote Wake-up 2.Plug in wake-up	V	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected 3.Remote-wakeup	V	-	1.After write 1 to clear RHSC (HcInterruptStatus[6]). 2.After write 1 to clear RHSC (HcInterruptStatus[6]). 3.After write 1 to clear RHSC (HcInterruptStatus[6]). and port suspended.
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	After software writes 1 to clear WKIF0 (ACMPx_STATUS[8]) and WKIF1 (ACMPx_STATUS[9])
	ACMPO status change	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWKx (CLK_PMUSTS[17:16]) when SPD mode is entered.

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes Transition

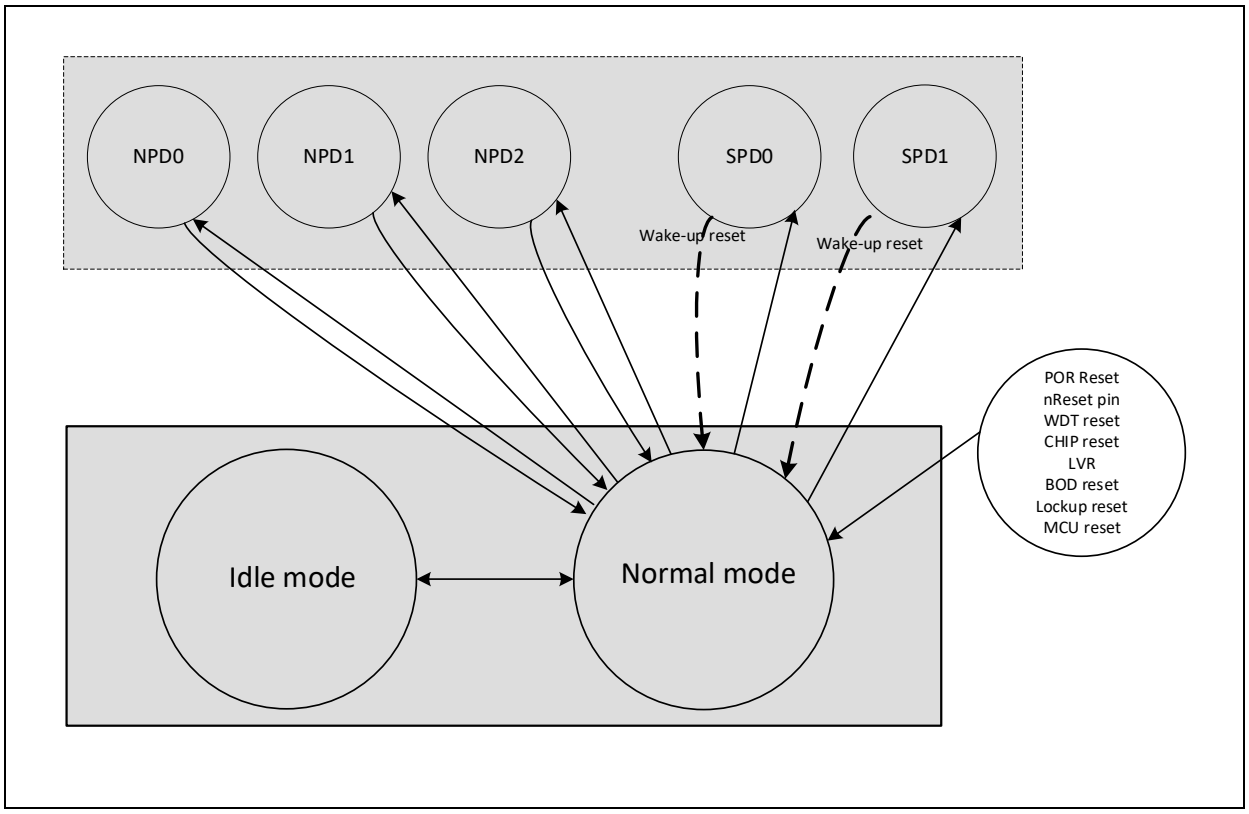


Figure 6.2-9 NuMicro M3351 Power Transition Graph

6.2.6 System Memory Map

The NuMicro M3351 series provides 4 Gbytes addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro M3351 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x000F_FFFF	FLASH_BA	FLASH APROM Memory Space (1024 Kbytes)
0x0F10_0000 – 0x0F10_3FFF	FLASH_BA	FLASH LDROM Memory Space
0x0F20_0000 – 0x0F20_3FFF	FLASH_BA	DATA FLASH 0 Memory Space
0x0F21_0000 – 0x0F21_FFFF	FLASH_BA	DATA FLASH 1 Memory Space
0x0080_0000 – 0x0081_FFFF	SRAM_BA	SRAM Memory Space Remapping (128 Kbytes)
0x0080_0000 – 0x0082_7FFF	SRAM_BA	SRAM Memory Space Remapping (160 Kbytes ecc_off)
0x2000_0000 – 0x2001_FFFF	SRAM_BA	SRAM Memory Space (128 Kbytes)
0x2000_0000 – 0x2002_7FFF	SRAM_BA	SRAM Memory Space Remapping (160 Kbytes ecc_off)
0x6000_0000 – 0x602F_FFFF	EXTMEM_BA	External Memory Space (3 Mbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers

0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA0 Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_F000 – 0x4000_FFFF	DFMC_BA	Data Flash Memory Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4002_0000 – 0x4002_1FFF	CANFD0_BA	CANFD0 Control Registers
0x4002_4000 – 0x4002_5FFF	CANFD1_BA	CANFD1 Control Registers
0x4002_F000 – 0x4002_FFFF	SCU_BA	SCU Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
0x4003_2000 – 0x4003_2FFF	CRYPTO_BA	Cryptographic Accelerator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT0_BA	Watchdog Timer 0 Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_2000 – 0x4004_2FFF	WDT1_BA	Watchdog Timer 1 Control Registers
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers (12-bit ADC)
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x4004_B000 – 0x4004_BFFF	EADC1_BA	Enhanced Analog-Digital-Converter 1 (EADC1) Control Registers (14-bit ADC)
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_C000 – 0x4005_CFFF	PWM0_BA	PWM0 Control Registers
0x4005_D000 – 0x4005_DFFF	PWM1_BA	PWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4007_6000 – 0x4007_6FFF	UART6_BA	UART6 Control Registers

0x4007_7000 – 0x4007_7FFF	UART7_BA	UART7 Control Registers
0x4007_8000 – 0x4007_8FFF	UART8_BA	UART8 Control Registers
0x4007_9000 – 0x4007_9FFF	UART9_BA	UART9 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I2C2 Control Registers
0x4008_6000 – 0x4008_6FFF	I3C_BA	I3C Control Registers
0x4008_8000 – 0x4008_8FFF	LLSI0/2/4/6/8_BA	LLSI0/2/4/6/8 Control Registers
0x4008_9000 – 0x4008_9FFF	LLSI1/3/5/7/9_BA	LLSI1/3/5/7/9 Control Registers
0x4008_A000 – 0x4008_AFFF	ELLSI0_BA	ELLSI0 Control Registers
0x4008_B000 – 0x4008_BFFF	ELLSI1_BA	ELLSI1 Control Registers
0x4009_6000 – 0x4009_9FFF	WWDT0_BA	Window Watchdog Timer 0 Control Registers
0x4009_8000 –0x4009_8FFF	WWDT1_BA	Window Watchdog Timer 1 Control Registers
0x400B_0000 – 0x400B_0FFF	EQEI0_BA	EQEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	EQEI1_BA	EQEI1 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 Implementation defined attribution unit (IDAU)

6.2.7.1 Overview

ARMv8-M introduces TrustZone, which allows full isolation of two security levels – Secure and Non-Secure. The memory map security attribute is defined by the combination of:

- Security Attribution Unit (SAU).
- Implementation Defined Attribution Unit (IDAU).

These attribution units define the memory space into four type regions:

- Secure Region: contains Secure program code or data.
- Non-Secure Callable Region (NSC): contains entry functions for Non-Secure programs to access Secure functions.
- Non-Secure Region: contains Non-Secure program code or data.
- Exempt Region: exempt region will be exempted from security check.

Each memory region defined by the SAU and IDAU has a region number generated by the SAU or by

the IDAU. Region number is used for determine a group of memory sharing the same security attribute. For testing security attributes and region numbers, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine the memory range is located entirely in the same range of attribute. For more details, please refer to the ARMv8-M Architecture Reference Manual. The M3351 IDAU memory map attributions and corresponding region numbers are shown in Figure 6.2-10. The address from 0xE000_0000 to 0xFFFF_FFFF is exempt regions and its region number is always not valid, that is, return data bit [23], IRVALID, of TT instruction is always 0.

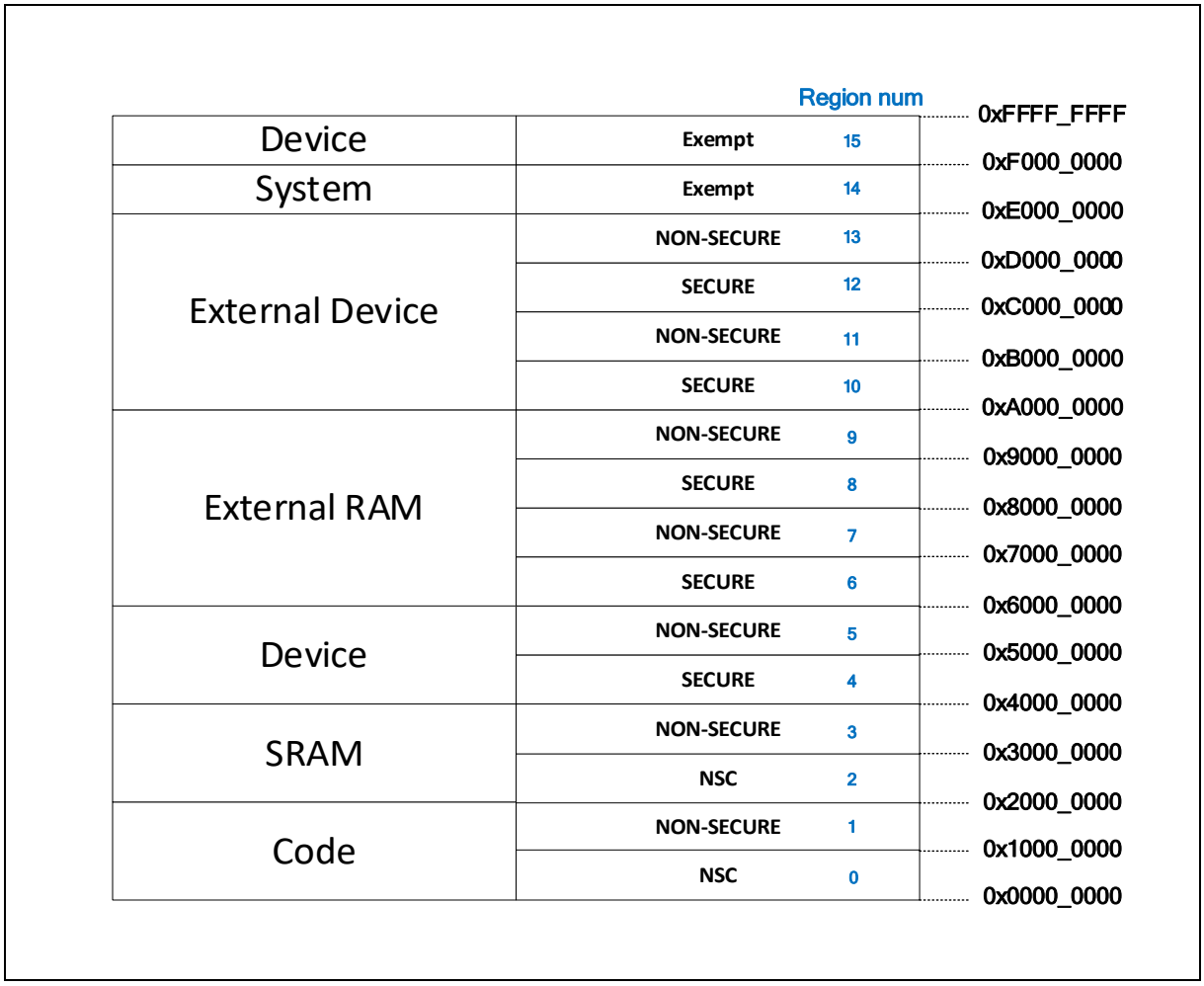


Figure 6.2-10 IDAU Memory Map

6.2.7.2 Block diagram

The system block diagram is shown in Figure 6.2-11. IDAU is responsible to response the security property of the address from processor, the processor compare the security property of the IDAU and SAU, and take the highest security attribute applied. There are four information IDAU can reply: Secure, Non-Secure Callable, Non-Secure and exempt region, after CPU get the information of the region security, it will choose the right MPU to control accesses to the address space. The hierarchy of security levels from high to low is: Secure > NSC > Non-Secure.

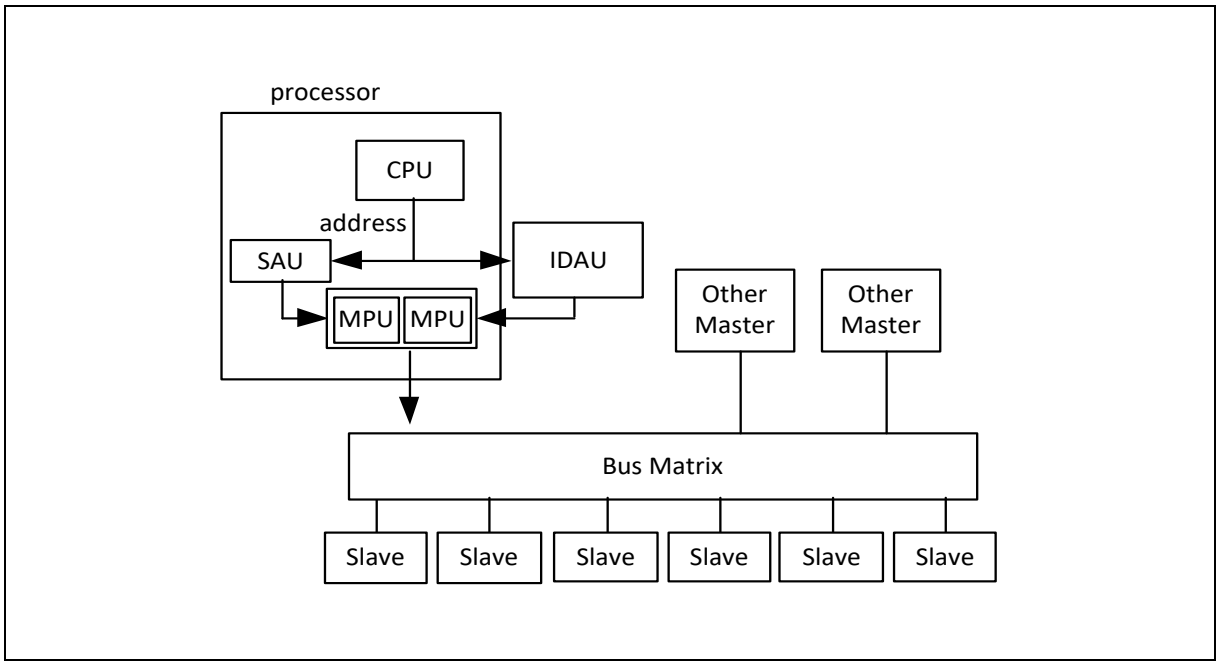


Figure 6.2-11 System Block Diagram

6.2.8 SRAM Memory Organization

The M3351 supports embedded SRAM with total up to 128 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0, SRAM bank1 and SRAM bank2 (only in ECC function off). The first bank has 64 Kbytes address space, the second bank has 64 Kbyte address space and the third bank has 32 Kbyte address space(only in ECC function off). These three banks address space can be accessed simultaneously. The SRAM supports ECC error check to make sure chip operating more stable.

- Supports total up to 128/160(ECC function off) Kbytes SRAM
- Supports byte / half word / word write
- Supports ECC error check function for entire SRAM
- Supports oversize response error
- Supports remap address to 0x0080_0000

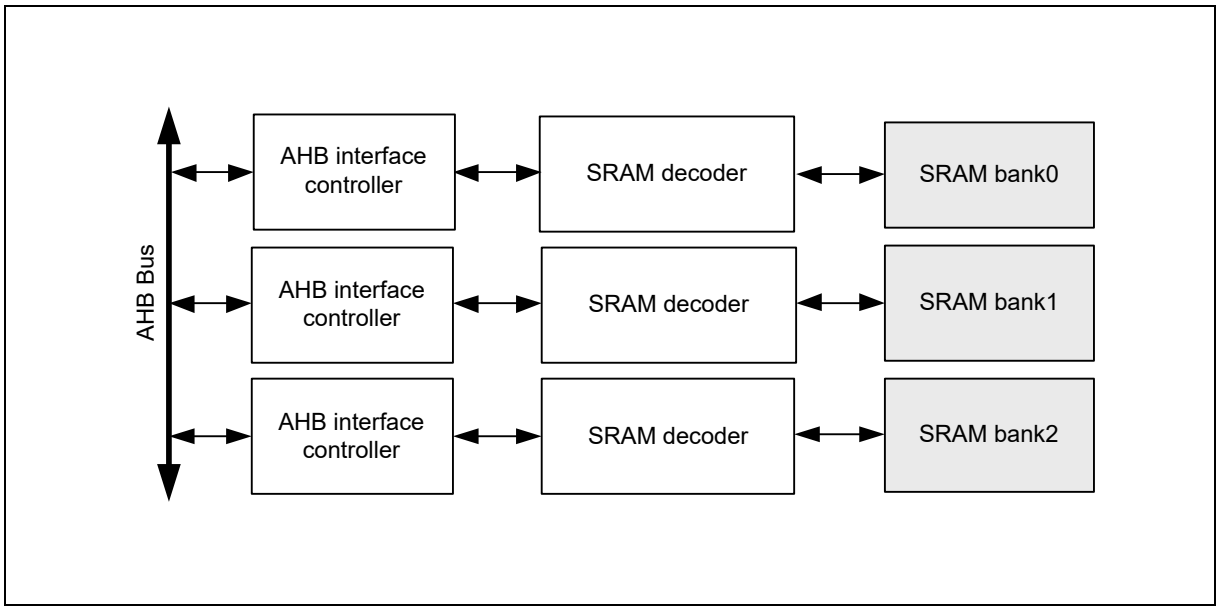


Figure 6.2-12 SRAM Block Diagram

Figure 6.2-12 shows the SRAM organization of M3351. There are three SRAM banks in M3351. The bank0 is addressed to 64 Kbytes, bank1 is addressed to 64 Kbytes and the bank2 is addressed to 32 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_7FFF (Non-Secure Callable) or 0x3000_0000 to 0x3000_7FFF (Non-Secure). The bank1 address space is from 0x2000_8000 to 0x2000_FFFF (Non-Secure Callable) or 0x3000_8000 to 0x3000_FFFF (Non-Secure). The bank2 address space is from 0x2001_0000 to 0x2001_FFFF (Non-Secure Callable) or 0x3001_0000 to 0x3001_FFFF (Non-Secure). The address between 0x2002_0000 to 0x2FFF_FFFF (Non-Secure Callable) and 0x3002_0000 to 0x3FFF_FFFF (Non-Secure) is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x0080_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_FFFF or 0x0080_0000 to 0x0080_FFFF, and access SRAM bank1 through 0x2001_0000 to 0x2001_FFFF or 0x0081_0000 to 0x0081_FFFF and access SRAM bank2 through 0x2002_0000 to 0x2002_7FFF or 0x0082_0000 to 0x0082_7FFF.

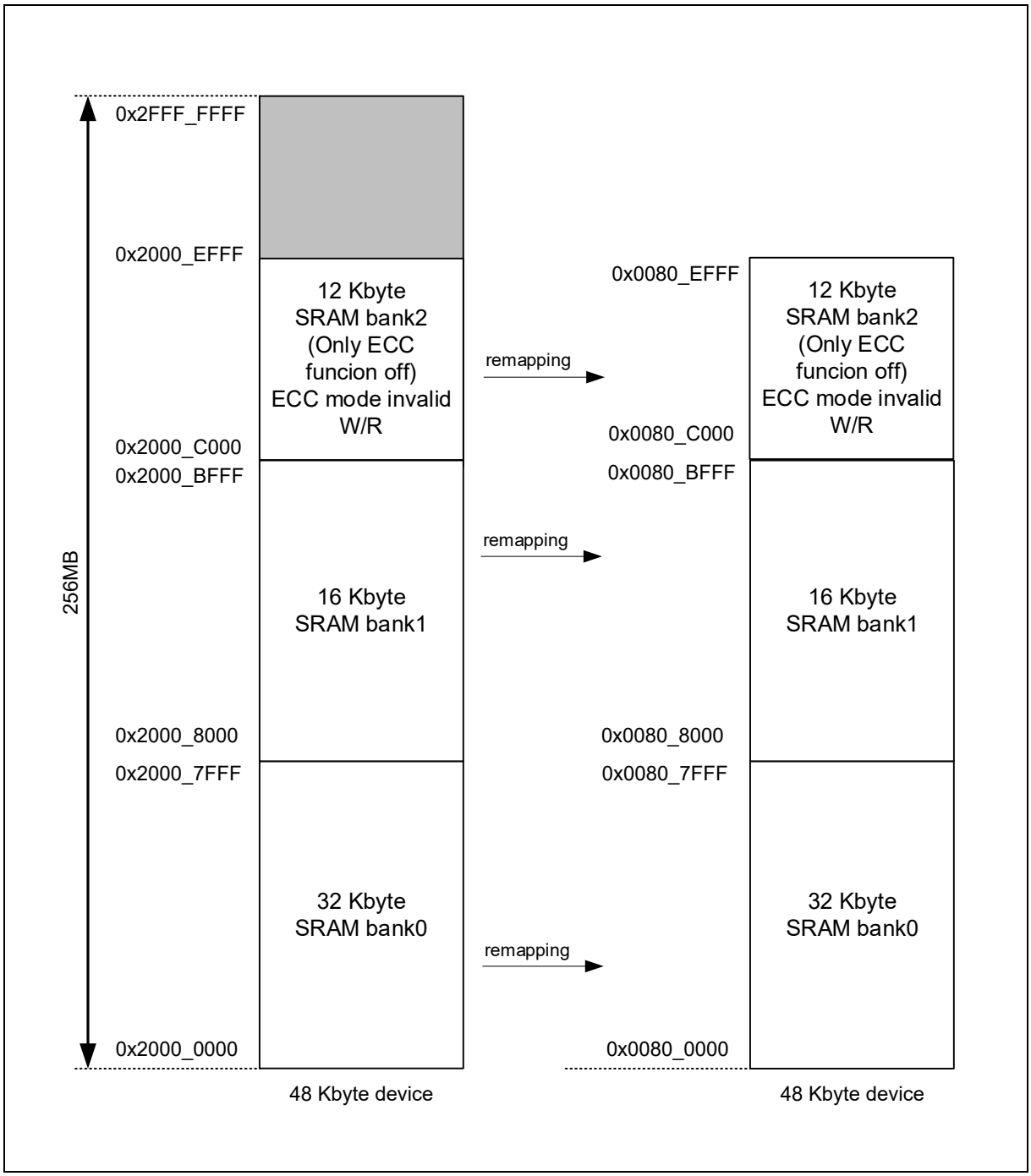


Figure 6.2-13 SRAM Memory Organization for 48 Kbytes Device

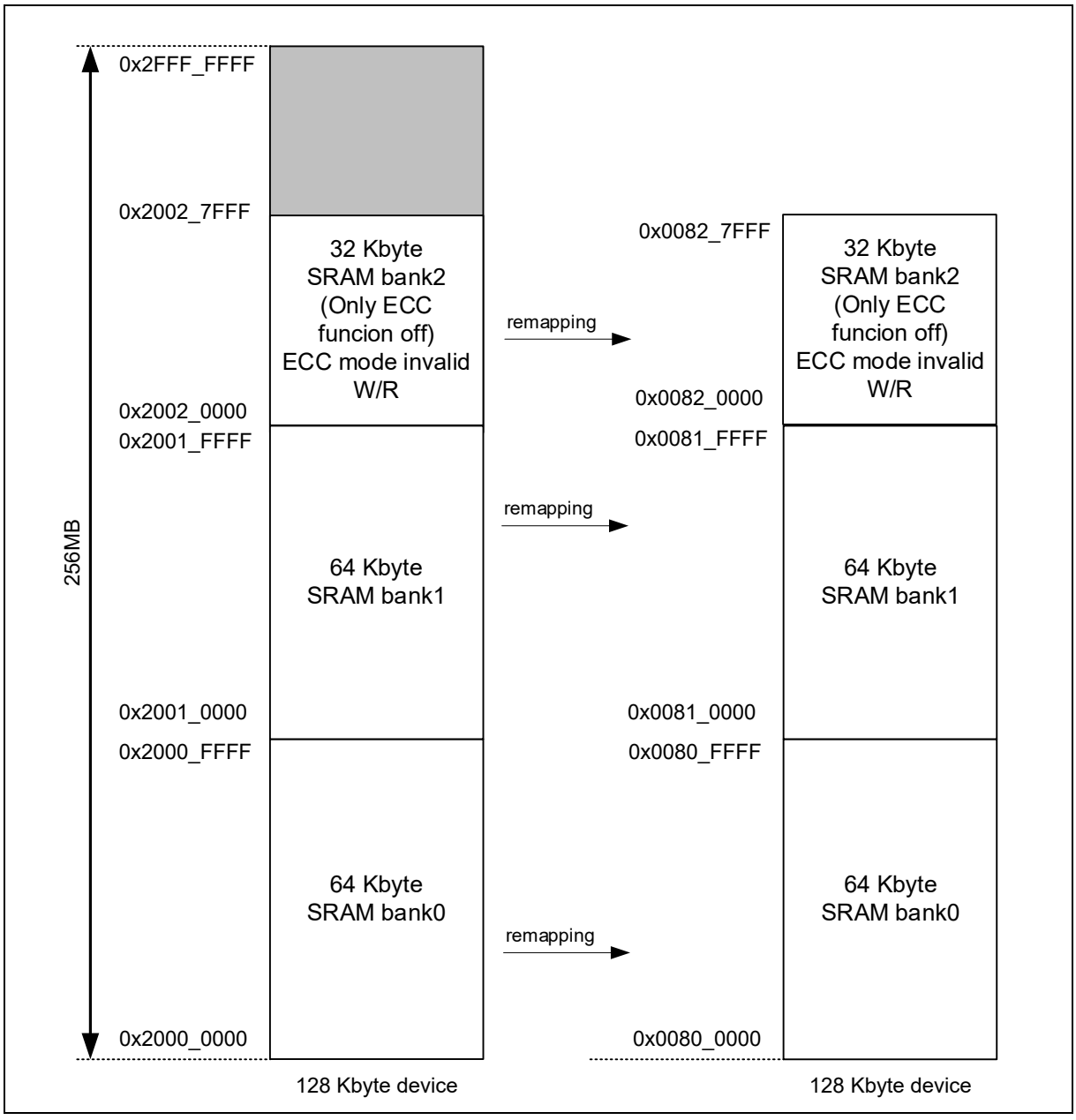


Figure 6.2-14 SRAM Memory Organization for 128 Kbytes Device

The entire system SRAM has word ECC error check function. When CPU is accessing system SRAM, the ECC error checking mechanism is dynamic operating. As ECC error occurred, the EERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with ECC error. Chip will enter interrupt when SRAM ECC error occurred if EERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM ECC error occurred, chip will stop detecting SRAM ECC error until user writes 1 to clear the EERRIF(SYS_SRAM_STATUS[0]) bit.

For security consideration, all content in SRAM will be cleaned when chip execute FLASH mass erase.

6.2.9 Bus Matrix

The M3351 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex-M33 CPU as the highest bus priority.

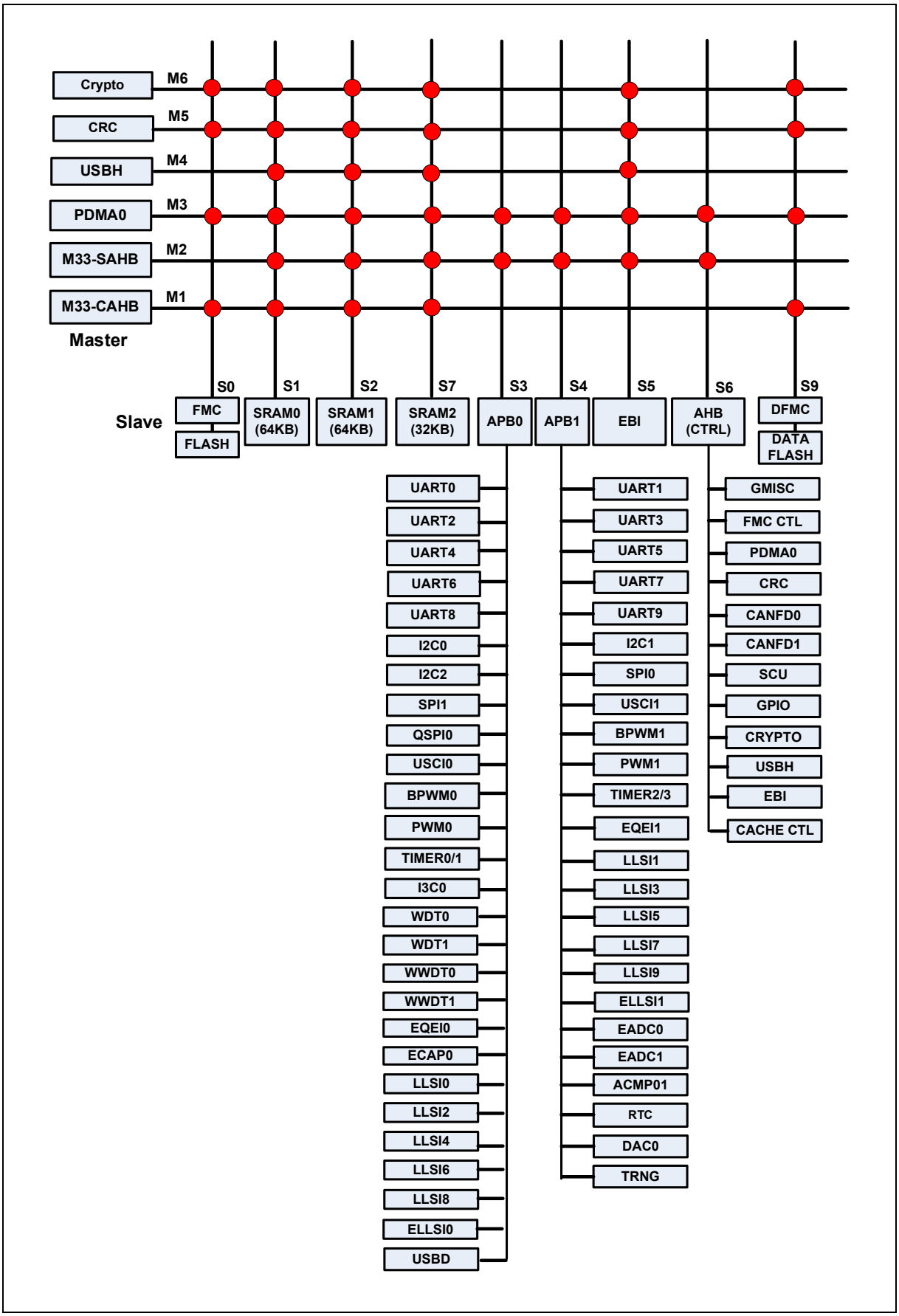

Crypto
CRC
USBH
PDMA0
M33-SAHB
M33-CAHB
Master
M6
M5
M4
M3
M2
M1
Slave
S0
S1
S2
S7
S3
S4
S5
S6
S9
FMC
FLASH
SRAM0 (64KB)
SRAM1 (64KB)
SRAM2 (32KB)
APB0
APB1
EBI
AHB (CTRL)
DFMC
DATA FLASH
UART0
UART2
UART4
UART6
UART8
I2C0
I2C2
SPI1
QSPI0
USCI0
BPWM0
PWM0
TIMER0/1
I3C0
WDT0
WDT1
WWDT0
WWDT1
EQEI0
ECAP0
LLSI0
LLSI2
LLSI4
LLSI6
LLSI8
ELLSI0
USBD
UART1
UART3
UART5
UART7
UART9
I2C1
SPI0
USCI1
BPWM1
PWM1
TIMER2/3
EQEI1
LLSI1
LLSI3
LLSI5
LLSI7
LLSI9
ELLSI1
EADC0
EADC1
ACMP01
RTC
DAC0
TRNG
GMISC
FMC CTL
PDMA0
CRC
CANFD0
CANFD1
SCU
GPIO
CRYPTO
USBH
EBI
CACHE CTL

Figure 6.2-15 NuMicro M3351 Bus Matrix Diagram

6.2.10 HIRC Auto Trim

This chip supports auto-trim function: HIRC48M trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

In HIRC48M case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.11 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_BODCTL	address 0x4000_0018
SYS_VREFCTL	address 0x4000_0028
SYS_USBPHY	address 0x4000_002C
SYS_VTORSET	address 0x4000_00A8
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_SRAM_ECCEN	address 0x4000_00DC
SYS_PORDISAN	address 0x4000_01EC
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_CLKDSTS	address 0x4000_0274
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C

FMC_APWPROT0	address 0x4000_C110
FMC_APWPROT1	address 0x4000_C114
FMC_APWPKEEP	address 0x4000_C118
FMC_SCACT	address 0x4000_C11C
FMC_LDWPROT	address 0x4000_C120
FMC_LDWPKEEP	address 0x4000_C124
FMC_DFWPROT	address 0x4000_C128
FMC_DFWPKEEP	address 0x4000_C12C
FMC_ECCCTL	address 0x4000_C130
DFMC_ISPCTL	address 0x400F_0000
DFMC_ISPTRG	address 0x400F_0010
DFMC_ISPSTS	address 0x400F_0040
DFMC_CYCCTL	address 0x400F_004C
DFMC_ECCCTL	address 0x400F_0130
WDT0_CTL	address 0x4004_0000
WDT0_ALTCTL	address 0x4004_0004
WDT1_CTL	address 0x4004_2000
WDT1_ALTCTL	address 0x4004_2004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
PWM0_CTL0	address 0x4005_C000
PWM1_CTL0	address 0x4005_D000
PWM0_DTCTL0_1/2_3/4_5	address 0x4005_C070/0x4005_C074/0x4005_C078
PWM1_DTCTL0_1/2_3/4_5	address 0x4005_D070/0x4005_D074/0x4005_D078
PWM0_DTCTL0_1	address 0x4005_C070
PWM0_DTCTL2_3	address 0x4005_C074
PWM0_DTCTL4_5	address 0x4005_C078
PWM1_DTCTL0_1	address 0x4005_D070
PWM1_DTCTL2_3	address 0x4005_D074
PWM1_DTCTL4_5	address 0x4005_D078

PWM0_BRKCTL0_1	address 0x4005_C0C8
PWM0_BRKCTL2_3	address 0x4005_C0CC
PWM0_BRKCTL4_5	address 0x4005_C0D0
PWM1_BRKCTL0_1	address 0x4005_D0C8
PWM1_BRKCTL2_3	address 0x4005_D0CC
PWM1_BRKCTL4_5	address 0x4005_D0D0
PWM0_SWBRK	address 0x4005_C0DC
PWM1_SWBRK	address 0x4005_D0DC
PWM0_INTEN1	address 0x4005_C0E4
PWM1_INTEN1	address 0x4005_D0E4
PWM0_INTSTS1	address 0x4005_C0EC
PWM1_INTSTS1	address 0x4005_D0EC
BPWM0_CTL0	address 0x4005_A000
BPWM1_CTL0	address 0x4005_B000
NS_FMC_ISPCTL	address 0x5000_C000
NS_FMC_ISPTRG	address 0x5000_C010
NS_FMC_ISPSTS	address 0x5000_C040
NS_FMC_APWPROT0	address 0x5000_C110
NS_FMC_APWPROT1	address 0x5000_C114
NS_FMC_APWPKEEP	address 0x5000_C118
NS_DFMC_ISPCTL	address 0x5000_F000
NS_DFMC_ISPTRG	address 0x5000_F010
NS_DFMC_ISPSTS	address 0x5000_F040

6.2.12 Wake-up Timer (WKTMR) and Wake-up I/O (WKIO) Function

The WKTMR function can be enabled by WKTMREN (CLK_PMUCTL[8]), WKTMRMOD (CLK_PMUCTL[13]) and WKTMRIS (CLK_PMUCTL[12:9]). WKTMR can wake-up chip from SPD modes.

When WKTMR wake-up event occurred in SPD mode, chip will be reset and re-run. Users can check wakeup flag from TMRWK (CLK_PMUSTS[1]).

The WKIO function can be enabled by CLK_PASPWKCTL, CLK_PBSPWKCTL, CLK_PCSPWKCTL, and CLK_PDSPWKCTL. WKIO can wakeup chip from SPD modes.

When WKIO wake-up event occurred in SPD modes, chip will be reset and re-run. Users can check wakeup flag from GPXWKx (CLK_PMUSTS[27:24], CLK_PMUSTS[11:8]).

6.2.13 System Timer (SysTick)

The Cortex-M33 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm Cortex-M33 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.2.14 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-480 interrupts.
- A programmable priority level of 0-7 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.14.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by M3351 Series. Software can set 256 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xE0” (The 5-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000000 to 0xFFFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-4
NMI	2	0x00000008	-2
Secure HardFault when AIRCR.BFHFNMINS is 1	3	0x0000000C	-3
Secure HardFault when AIRCR.BFHFNMINS is 0			-1
Non-Secure Hard Fault			-1
Memory Manager Fault	4	0x00000010	Configurable

Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Secure Fault	7	0x0000001C	Configurable
Reserved	8 ~ 10	-	Reserved
SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13	-	Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt(IRQ0~IRQ138)	16 ~ 154	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAME	SRAM ECC check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	FMC_ISP_INT	FMC ISP interrupt
22	6	RTC_INT	Real time clock interrupt
23	7	Reserved	Reserved
24	8	WDT0_INT	Watchdog Timer 0 interrupt
25	9	WWDT0_INT	Window Watchdog 0 Timer interrupt
26	10	EINT0	External interrupt from INT0 pin
27	11	EINT1	External interrupt from INT1 pin
28	12	EINT2	External interrupt from INT2 pin
29	13	EINT3	External interrupt from INT3 pin
30	14	EINT4	External interrupt from INT4 pin
31	15	EINT5	External interrupt from INT5 pin
32	16	GPA_INT	External interrupt from PA pin
33	17	GPB_INT	External interrupt from PB pin
34	18	GPC_INT	External interrupt from PC pin
35	19	GPD_INT	External interrupt from PD pin

36	20	GPE_INT	External interrupt from PEpin
37	21	GPF_INT	External interrupt from PF pin
38	22	QSPI0_INT	QSPI0 interrupt
39	23	SPI0_INT	SPI0 interrupt
40	24	BRAKE0_INT	PWM0 brake interrupt
41	25	PWM0_P0_INT	PWM0 pair 0 interrupt
42	26	PWM0_P1_INT	PWM0 pair 1 interrupt
43	27	PWM0_P2_INT	PWM0 pair 2 interrupt
44	28	BRAKE1_INT	PWM1 brake interrupt
45	29	PWM1_P0_INT	PWM1 pair 0 interrupt
46	30	PWM1_P1_INT	PWM1 pair 1 interrupt
47	31	PWM1_P2_INT	PWM1 pair 2 interrupt
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA0_INT	PDMA0 interrupt
57	41	DAC0_INT	DAC0 interrupt
58	42	EADC0_INT0	EADC0 interrupt source 0
59	43	EADC0_INT1	EADC0 interrupt source 1
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	Reserved	Reserved
62	46	EADC0_INT2	EADC0 interrupt source 2
63	47	EADC0_INT3	EADC0 interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	UART3_INT	UART3 interrupt
66	50	Reserved	Reserved
67	51	SPI1_INT	SPI1 interrupt
68	52	Reserved	Reserved
69	53	USBD_INT	USB device interrupt
70	54	USBH_INT	USB host interrupt
71	55	Reserved	Reserved

72	56	ETI_INT	External trigger interrupt
73	57	CRC_INT	CRC interrupt
74	58	Reserved	Reserved
75	59	FMC_NS_INT	FMC non-secure interrupt
76	60	SCU_INT	Security configuration unit interrupt
77	61	Reserved	Reserved
78	62	Reserved	Reserved
79	63	Reserved	Reserved
80	64	Reserved	Reserved
81	65	Reserved	Reserved
82	66	Reserved	Reserved
83	67	WDT1_INT	Watchdog Timer 1 interrupt
84	68	Reserved	Reserved
85	69	Reserved	Reserved
86	70	Reserved	Reserved
87	71	CRYPTO	Crypto interrupt
88	72	GPG_INT	External interrupt from PG pin
89	73	EINT6	External interrupt from INT6 pin
90	74	UART4_INT	UART4 interrupt
91	75	UART5_INT	UART5 interrupt
92	76	USCI0_INT	USCI0 interrupt
93	77	USCI1_INT	USCI1 interrupt
94	78	BPWM0_INT	BPWM0 interrupt
95	79	BPWM1_INT	BPWM1 interrupt
96	80	Reserved	Reserved
97	81	Reserved	Reserved
98	82	I2C2_INT	I2C2 interrupt
99	83	Reserved	Reserved
100	84	EQEI0_INT	EQEI0 interrupt
101	85	EQEI1_INT	EQEI1 interrupt
102	86	ECAP0_INT	ECAP0 interrupt
103	87	Reserved	Reserved
105	88	GPH_INT	External interrupt from PH pin
105	89	EINT7	External interrupt from INT7 pin
106	90	Reserved	Reserved
107	91	WWDT1_INT	Window Watchdog 1 Timer interrupt

108	92	Reserved	Reserved
109	93	Reserved	Reserved
110	94	Reserved	Reserved
111	95	Reserved	Reserved
112	96	SRAME_NS	SRAM non-secure ECC check error interrupt
113	97	ICACHE	ICACHE parity error interrupt
114	98	Reserved	Reserved
115	99	UART8_INT	UART8 interrupt
116	100	UART9_INT	UART9 interrupt
117	101	TRNG_INT	TRNG interrupt
118	102	UART6_INT	UART6 interrupt
119	103	UART7_INT	UART7 interrupt
120	104	EADC1_INT0	EADC1 interrupt source 0
121	105	EADC1_INT1	EADC1 interrupt source 1
122	106	EADC1_INT2	EADC1 interrupt source 2
123	107	EADC1_INT3	EADC1 interrupt source 3
124	108	I3C0_INT	I3C interrupt source 0
125	109	Reserved	Reserved
126	110	Reserved	Reserved
127	111	DFMC_INT	DFMC ISP interrupt
128	112	CANFD0_INT0	CANFD0 interrupt source 0
129	113	CANFD0_INT1	CANFD0 interrupt source 1
130	114	CANFD1_INT0	CANFD1 interrupt source 0
131	115	CANFD1_INT1	CANFD1 interrupt source 1
132	116	Reserved	Reserved
133	117	Reserved	Reserved
134	118	Reserved	Reserved
135	119	DFMC_NS_INT	FMC non-secure interrupt
136	120	Reserved	Reserved
137	121	Reserved	Reserved
138	122	Reserved	Reserved
139	123	Reserved	Reserved
140	124	Reserved	Reserved
141	125	Reserved	Reserved
142	126	Reserved	Reserved
143	127	Reserved	Reserved

144	128	LLSI0_INT	LED Light Strip Interface interrupt source 0
145	129	LLSI1_INT	LED Light Strip Interface interrupt source 1
146	130	LLSI2_INT	LED Light Strip Interface interrupt source 2
147	131	LLSI3_INT	LED Light Strip Interface interrupt source 3
148	132	LLSI4_INT	LED Light Strip Interface interrupt source 4
149	133	LLSI5_INT	LED Light Strip Interface interrupt source 5
150	134	LLSI6_INT	LED Light Strip Interface interrupt source 6
151	135	LLSI7_INT	LED Light Strip Interface interrupt source 7
152	136	LLSI8_INT	LED Light Strip Interface interrupt source 8
153	137	LLSI9_INT	LED Light Strip Interface interrupt source 9
154	138	ELLSI0_INT	Enhanced LED Light Strip Interface interrupt source 0
155	139	ELLSI1_INT	Enhanced LED Light Strip Interface interrupt source 1

Table 6.2-9 Interrupt Number Table

6.2.14.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.14.3 NMI Multiplexer Source Select

The chip supports the NMI multiplexer function, which allows users to select one of the interrupt sources from IRQ5~IRQ139 to be an NMI, named INTMUX. Users can set INTMUX(NMIEN[18]) to 1 to enable this NMI and set NMIMSEL(NMIMSEL[7:0]) to select IRQ source. The Table 6.2-10 lists all available IRQ sources of INTMUX. If NMIMSEL is set to an unavailable value, INTMUX will not activate.

NMIMSEL (NMIMSEL[7:0])	Interrupt IRQ	Interrupt Name	NMIMSEL (NMIMSEL [7:0])	Interrupt IRQ	Interrupt Name
0x5	IRQ5	FMC_ISP_INT	0x48	IRQ72	GPG_INT
0x6	IRQ6	RTC_INT	0x49	IRQ73	EINT6
0x8	IRQ8	WDT0_INT	0x4A	IRQ74	UART4_INT
0x9	IRQ9	WWDT0_INT	0x4B	IRQ75	UART5_INT

0x10	IRQ16	GPA_INT	0x4C	IRQ76	USCI0_INT
0x11	IRQ17	GPB_INT	0x4D	IRQ77	USCI1_INT
0x12	IRQ18	GPC_INT	0x4E	IRQ78	BPWM0_INT
0x13	IRQ19	GPD_INT	0x4F	IRQ79	BPWM1_INT
0x14	IRQ20	GPE_INT	0x52	IRQ82	I2C2_INT
0x15	IRQ21	GPF_INT	0x54	IRQ84	EQEI0_INT
0x16	IRQ22	QSPI0_INT	0x55	IRQ85	EQEI1_INT
0x17	IRQ23	SPI0_INT	0x56	IRQ86	ECAP0_INT
0x18	IRQ24	BRAKE0_INT	0x58	IRQ88	GPH_INT
0x19	IRQ25	PWM0_P0_INT	0x59	IRQ89	EINT7
0x1A	IRQ26	PWM0_P1_INT	0x5B	IRQ91	WWDT1_INT
0x1B	IRQ27	PWM0_P2_INT	0x60	IRQ96	SRAME_NS
0x1C	IRQ28	BRAKE1_INT	0x63	IRQ99	UART8_INT
0x1D	IRQ29	PWM1_P0_INT	0x64	IRQ100	UART9_INT
0x1E	IRQ30	PWM1_P1_INT	0x65	IRQ101	TRNG_INT
0x1F	IRQ31	PWM1_P2_INT	0x66	IRQ102	UART6_INT
0x20	IRQ32	TMR0_INT	0x67	IRQ103	UART7_INT
0x21	IRQ33	TMR1_INT	0x68	IRQ104	EADC1_INT0
0x22	IRQ34	TMR2_INT	0x69	IRQ105	EADC1_INT1
0x23	IRQ35	TMR3_INT	0x6A	IRQ106	EADC1_INT2
0x24	IRQ36	UART0_INT	0x6B	IRQ107	EADC1_INT3
0x25	IRQ37	UART1_INT	0x6C	IRQ108	I3C0_INT
0x26	IRQ38	I2C0_INT	0x6F	IRQ111	DFMC_INT
0x27	IRQ39	I2C1_INT	0x70	IRQ112	CANFD0_INT0
0x28	IRQ40	PDMA0_INT	0x71	IRQ113	CANFD0_INT1
0x29	IRQ41	DAC0_INT	0x72	IRQ114	CANFD1_INT0
0x2A	IRQ42	EADC0_INT0	0x73	IRQ115	CANFD1_INT1
0x2B	IRQ43	EADC0_INT1	0x77	IRQ119	DFMC_NS_INT
0x2C	IRQ44	ACMP01_INT	0x80	IRQ128	LLSI0_INT
0x2E	IRQ46	EADC0_INT2	0x81	IRQ129	LLSI1_INT
0x2F	IRQ47	EADC0_INT3	0x82	IRQ130	LLSI2_INT
0x30	IRQ48	UART2_INT	0x83	IRQ131	LLSI3_INT
0x31	IRQ49	UART3_INT	0x84	IRQ132	LLSI4_INT
0x33	IRQ51	SPI1_INT	0x85	IRQ133	LLSI5_INT
0x35	IRQ53	USBD_INT	0x86	IRQ134	LLSI6_INT
0x36	IRQ54	USBH_INT	0x87	IRQ135	LLSI7_INT

0x38	IRQ56	ETI_INT	0x88	IRQ136	LLSI8_INT
0x39	IRQ57	CRC_INT	0x89	IRQ137	LLSI9_INT
0x3B	IRQ59	FMC_NS_INT	0x8A	IRQ138	ELLSI0_INT
0x3C	IRQ60	SCU_INT	0x8B	IRQ139	ELLSI1_INT
0x43	IRQ67	WDT1_INT	Others	Reserved	
0x47	IRQ71	CRYPTO			

Table 6.2-10 NMIMSEL Mapping Table

The diagram of NMI interrupt structure is shown in Figure 6.2-16.

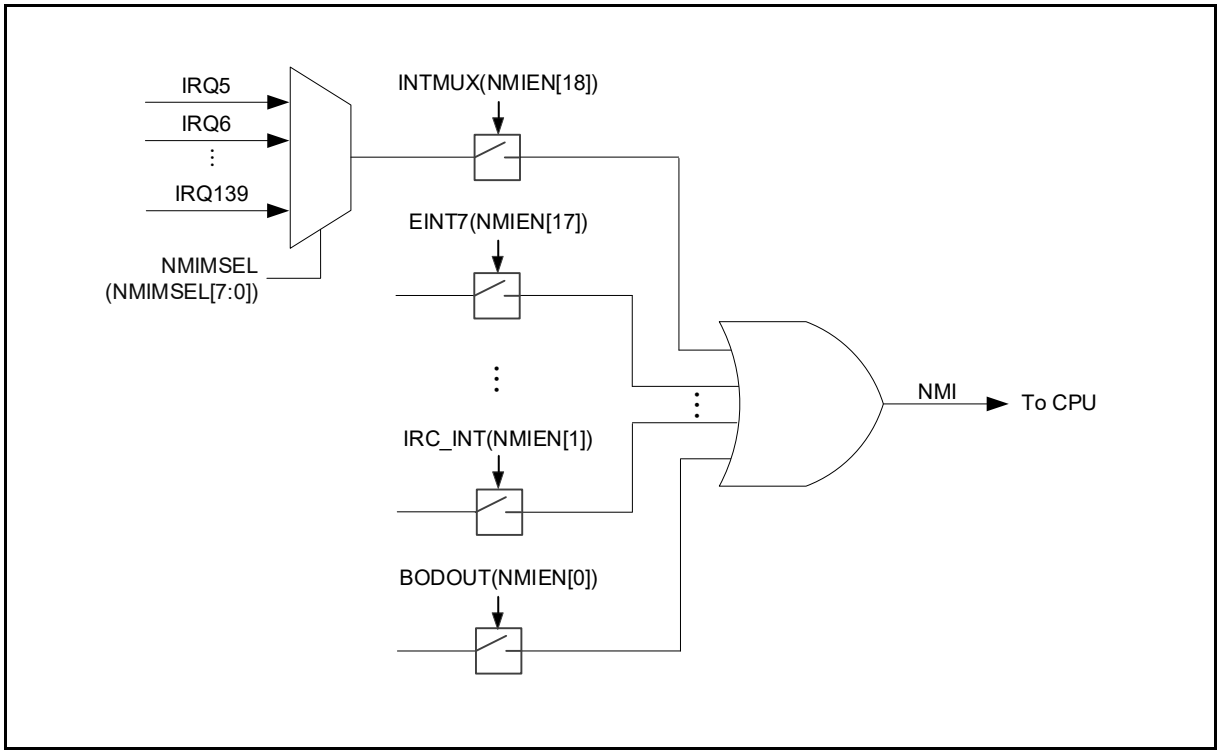


Figure 6.2-16 NMI Interrupt Structure

6.2.14.4 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x00	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000
NVIC_ISER1	NVIC_BA+0x04	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000
NVIC_ISER2	NVIC_BA+0x08	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000
NVIC_ISER3	NVIC_BA+0x0C	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x80	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000
NVIC_ICER1	NVIC_BA+0x84	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000
NVIC_ICER2	NVIC_BA+0x88	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000
NVIC_ICER3	NVIC_BA+0x8C	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000
NVIC_ISPR2	NVIC_BA+0x108	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000
NVIC_ISPR3	NVIC_BA+0x10C	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000
NVIC_ICPR2	NVIC_BA+0x188	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000
NVIC_ICPR3	NVIC_BA+0x18C	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000
NVIC_IABR2	NVIC_BA+0x208	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000
NVIC_IABR3	NVIC_BA+0x20C	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000
NVIC_ITNS0	NVIC_BA+0x280	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000
NVIC_ITNS1	NVIC_BA+0x284	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000
NVIC_ITNS2	NVIC_BA+0x288	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000
NVIC_ITNS3	NVIC_BA+0x28C	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..34**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ138 Priority Control Register	0x0000_0000
STIR	NVIC_BA+0xE00	W	Software Trigger Interrupt Registers	0x0000_0000

IRQ0 ~ IRQ138 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x00	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Set-enable Control Register (NVIC_ISER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER1	NVIC_BA+0x04	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Set-enable Control Register (NVIC_ISER2)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER2	NVIC_BA+0x08	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Set-enable Control Register (NVIC_ISER3)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER3	NVIC_BA+0x0C	R/W	IRQ0 ~ IRQ138 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x80	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Clear-enable Control Register (NVIC_ICER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER1	NVIC_BA+0x84	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Clear-enable Control Register (NVIC_ICER2)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER2	NVIC_BA+0x88	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Clear-enable Control Register (NVIC_ICER3)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER3	NVIC_BA+0x8C	R/W	IRQ0 ~ IRQ138 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ138 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Set-pending Control Register (NVIC_ISPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Set-pending Control Register (NVIC_ISPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR2	NVIC_BA+0x108	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Set-pending Control Register (NVIC_ISPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR3	NVIC_BA+0x10C	R/W	IRQ0 ~ IRQ138 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Clear-pending Control Register (NVIC_ICPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Clear-pending Control Register (NVIC_ICPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR2	NVIC_BA+0x188	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Clear-pending Control Register (NVIC_ICPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR3	NVIC_BA+0x18C	R/W	IRQ0 ~ IRQ138 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ138 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ138 Active Bit Register (NVIC_IABR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ138 Active Bit Register (NVIC_IABR2)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR2	NVIC_BA+0x208	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ138 Active Bit Register (NVIC_IABR3)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR3	NVIC_BA+0x20C	R/W	IRQ0 ~ IRQ138 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ138 Target Bit Register (NVIC_ITNS0)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS0	NVIC_BA+0x280	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
TARGET							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TARGET							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TARGET							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TARGET							

Bits	Description	
[31:0]	**TARGET**	**Interrupt Target Flags** The NVIC_ITNS0-NVIC_ITNS3 registers indicate and allows modification of the target security state. 0 = Interrupt targets secure state. 1 = Interrupt targets non secure state.

IRQ0 ~ IRQ138 Target Bit Register (NVIC_ITNS1)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS1	NVIC_BA+0x284	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
TARGET							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TARGET							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TARGET							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TARGET							

Bits	Description	
[31:0]	**TARGET**	**Interrupt Target Flags** The NVIC_ITNS0-NVIC_ITNS3 registers indicate and allows modification of the target security state. 0 = Interrupt targets secure state. 1 = Interrupt targets non secure state.

IRQ0 ~ IRQ138 Target Bit Register (NVIC_ITNS2)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS2	NVIC_BA+0x288	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
TARGET							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TARGET							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TARGET							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TARGET							

Bits	Description	
[31:0]	**TARGET**	**Interrupt Target Flags** The NVIC_ITNS0-NVIC_ITNS3 registers indicate and allows modification of the target security state. 0 = Interrupt targets secure state. 1 = Interrupt targets non secure state.

IRQ0 ~ IRQ138 Target Bit Register (NVIC_ITNS3)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS3	NVIC_BA+0x28C	R/W	IRQ0 ~ IRQ138 Target Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
TARGET							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TARGET							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TARGET							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TARGET							

Bits	Description	
[31:0]	**TARGET**	**Interrupt Target Flags** The NVIC_ITNS0-NVIC_ITNS3 registers indicate and allows modification of the target security state. 0 = Interrupt targets secure state. 1 = Interrupt targets non secure state.

IRQ0 ~ IRQ138 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..34**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ138 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3			Reserved				
23	22	21	20	19	18	17	16
PRI_4n_2			Reserved				
15	14	13	12	11	10	9	8
PRI_4n_1			Reserved				
7	6	5	4	3	2	1	0
PRI_4n_0			Reserved				

Bits	Description	
[31:29]	**PRI_4n_3**	**Priority of IRQ_4n+3** “0” denotes the highest priority and “7” denotes the lowest priority.
[28:24]	**Reserved**	Reserved.
[23:21]	**PRI_4n_2**	**Priority of IRQ_4n+2** “0” denotes the highest priority and “7” denotes the lowest priority.
[20:16]	**Reserved**	Reserved.
[15:13]	**PRI_4n_1**	**Priority of IRQ_4n+1** “0” denotes the highest priority and “7” denotes the lowest priority.
[12:8]	**Reserved**	Reserved.
[7:5]	**PRI_4n_0**	**Priority of IRQ_4n+0** “0” denotes the highest priority and “7” denotes the lowest priority.
[4:0]	**Reserved**	Reserved.

Software Trigger Interrupt Register (STIR)

Register	Offset	R/W	Description	Reset Value
STIR	NVIC_BA+0xE00	W	Software Trigger Interrupt Registers	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**INTID**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTID							

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8:0]	**INTID**	**Interrupt ID (Write Only)** Write to the STIR To Generate An Interrupt from Software When the USERSETMPEND bit in the CCR is set to 1, unprivileged software can access the STIR. Number of valid Interrupt ID refers to Table 6.2-9. For example, a value of 0x03 specifies interrupt IRQ3.

6.2.15 System Control Register

The Cortex-M33 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex-M33 interrupt priority and Cortex-M33 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm Cortex-M33 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCR Base Address: **SCS_BA = 0xE000_E000**				
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

Interrupt Control State Register (ICSR)

Register	Offset	R/W	Description	Reset Value
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000

31	30	29	28	27	26	25	24
PENDNMISET	PENDNMICLR	Reserved	PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved
23	22	21	20	19	18	17	16
ISRPREEMPT	ISRPENDING	Reserved	VECTPENDING				
15	14	13	12	11	10	9	8
VECTPENDING				RETTOBASE	Reserved		VECTACTIVE
7	6	5	4	3	2	1	0
VECTACTIVE							

Bits	Description	
[31]	PENDNMISET	**NMI Set-pending Bit** Write Operation: 0 = No effect. 1 = Change NMI exception state to pending. Read Operation: 0 = NMI exception is not pending. 1 = NMI exception is pending. **Note:** Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30]	PENDNMICLR	**Pend NMI clear Bit** Write Operation: 0 = No effect. 1 = Clear pending status. **Note:** This bit is write-one-to-clear. Writes of zero are ignored.
[29]	Reserved	Reserved.
[28]	PENDSVSET	**PendSV Set-pending Bit** Write Operation: 0 = No effect. 1 = Change PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note:** Writing 1 to this bit is the only way to set the PendSV exception state to pending.

[27]	**PENDSVCLR**	**PendSV Clear-pending Bit (Write Only)** Write Operation: 0 = No effect. 1 = Remove the pending state from the PendSV exception. **Note:** This is a write only bit. To clear the PENDSV bit, you must "write 0 to PENDSVSET and write 1 to PENDSVCLR" at the same time.
[26]	**PENDSTSET**	**SysTick Exception Set-pending Bit** Write Operation: 0 = No effect. 1 = Change SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	**PENDSTCLR**	**SysTick Exception Clear-pending Bit (Write Only)** Write Operation: 0 = No effect. 1 = Remove the pending state from the SysTick exception. **Note:** This is a write only bit. To clear the PENDST bit, you must "write 0 to PENDSTSET and write 1 to PENDSTCLR" at the same time.
[24]	**Reserved**	Reserved.
[23]	**ISRPREEMPT**	**Interrupt Preempt Bit (Read Only)** 0 = Pending exception is not handled on exit from debug state. 1 = Pending exception is handled on exit from debug state. If set, a pending exception will be serviced on exit from the debug halt state.
[22]	**ISRPENDING**	**Interrupt Pending Flag, Excluding NMI and Faults (Read Only)** 0 = Interrupt not pending. 1 = Interrupt pending.
[21]	**Reserved**	Reserved.
[20:12]	**VECTPENDING**	**Number of the Highest Pended Exception** Indicate the Exception Number of the Highest Priority Pending Enabled Exception. 0 = No pending exceptions. Nonzero = the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.
[11]	**RETTOBASE**	**Preempted Active Exceptions Indicator** Indicate whether There are Preempted Active Exceptions. 0 = There are preempted active exceptions to execute. 1 = There are no active exceptions, or the currently-executing exception is the only active exception.
[10:9]	**Reserved**	Reserved.
[8:0]	**VECTACTIVE**	**Number of the Current Active Exception** 0 = Thread mode. Non-zero = The exception number of the currently active exception.

Vector Table Offset Register (VTOR)

Register	Offset	R/W	Description	Reset Value
VTOR	SCS_BA+0xD08	R/W	Vector Table Offset Register	0x0000_0000

31	30	29	28	27	26	25	24
TBLOFF							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
TBLOFF							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
TBLOFF							**Reserved**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:9]	**TBLOFF**	**Table Offset Bits** The vector table address for the selected Security state.
[8:0]	**Reserved**	Reserved.

Application Interrupt and Reset Control Register (AIRCR)

Register	Offset	R/W	Description	Reset Value
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

31	30	29	28	27	26	25	24
VECTORKEY							
23	22	21	20	19	18	17	16
VECTORKEY							
15	14	13	12	11	10	9	8
ENDIANNESS	PRIS	BFHFNMINS	Reserved		PRIGROUP		
7	6	5	4	3	2	1	0
Reserved				SYSRESETREQS	SYSRESETREQ	VECTCLRACTIVE	Reserved

Bits	Description	
[31:16]	**VECTORKEY**	**Register Access Key** When writing this register, this field should be 0x05FA, otherwise the write action will be unpredictable. The VECTORKEY filed is used to prevent accidental write to this register from resetting the system or clearing of the exception status.
[15]	**ENDIANNESS**	**Data Endianness** 0 = Little-endian. 1 = Big-endian.
[14]	**PRIS**	**Prioritize Secure exceptions** 0 = Priority ranges of Secure and Non-secure exceptions are identical. 1 = Non-secure exceptions are de-prioritized. The value of this bit defines whether Secure exception priority boosting is enabled.
[13]	**BFHFNMINS**	**BusFault, HardFault, and NMI Non-secure enable** 0 = BusFault, HardFault, and NMI are Secure. 1 = BusFault and NMI are Non-secure and exceptions can target Non-secure HardFault. The value of this bit defines whether BusFault and NMI exceptions are Non-secure, and whether exceptions target the Non-secure HardFault exception.
[13:11]	**Reserved**	Reserved.
[10:8]	**PRIGROUP**	**Interrupt Priority Grouping** This field determines the Split Of Group priority from subpriority,
[7:4]	**Reserved**	Reserved.
[3]	**SYSRESETREQS**	**System reset request, Secure state only** 0 = SYSRESETREQ functionality is available to both Security states. 1 = SYSRESETREQ functionality is only available to Secure state. The value of this bit defines whether the SYSRESETREQ bit is functional for Non-secure use.
[2]	**SYSRESETREQ**	**System Reset Request (Write Only)**

		Writing this bit to 1 will cause a reset signal to be asserted to the chip and indicate a reset is requested. This bit is write only and self-cleared as part of the reset sequence.
[1]	**VECTCLRACTIVE**	**Exception Active Status Clear Bit (Write Only)** Setting this bit to 1 will clear all active state information for fixed and configurable exceptions. This bit is write only and can only be written when the core is halted. **Note:** It is the debugger's responsibility to re-initialize the stack.
[0]	**Reserved**	Reserved.

PRIGROUP	Binary Point	Group Priority Bits	Subpriority Bits	Number Of Group Priorities	Subpriorities
0b000	bxxxxxxx.y	[7:1]	[0]	128	2
0b001	bxxxxxx.yy	[7:2]	[1:0]	64	4
0b010	bxxxxx.yyy	[7:3]	[2:0]	32	8
0b011	bxxxx.yyyy	[7:4]	[3;0]	16	16
0b100	bxxx.yyyyy	[7:5]	[4:0]	8	32
0b101	bxx.yyyyyy	[7:6]	[5:0]	4	64
0b110	bx.yyyyyyy	[7]	[6:0]	2	128
0b111	b.yyyyyyyy	None	[7:0]	1	256

Table 6.2-11 Priority Grouping

System Control Register (SCR)

Register	Offset	R/W	Description	Reset Value
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved			SEVONPEND	Reserved	SLEEPDEEP	SLEEPONEXIT	Reserved

Bits	Description	
[31:5]	**Reserved**	Reserved.
[4]	**SEVONPEND**	**Send Event on Pending** 0 = Only enabled interrupts or events can wake up the processor, while disabled interrupts are excluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	**Reserved**	Reserved.
[2]	**SLEEPDEEP**	**Processor Deep Sleep and Sleep Mode Selection** Control whether the Processor Uses Sleep Or Deep Sleep as its Low Power Mode. 0 = Sleep. 1 = Deep sleep.
[1]	**SLEEPONEXIT**	**Sleep-on-exit Enable Control** This bit indicates Sleep-On-Exit when Returning from Handler Mode to Thread Mode. 0 = Do not sleep when returning to Thread mode. 1 = Enter sleep, or deep sleep, on return from an ISR to Thread mode. Set this bit to 1 enable an interrupt driven application to avoid returning to an empty main application.
[0]	**Reserved**	Reserved.

System Handler Priority Register 1 (SHPR1)

Register	Offset	R/W	Description	Reset Value
SHPR1	SCS_BA+0xD18	R/W	System Handler Priority Register 1	0x0000_0000

31	30	29	28	27	26	25	24
PRI_7							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_6							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_5							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4							

Bits	Description	
[31:24]	**PRI_7**	Priority of system handler 7
[23:16]	**PRI_6**	Priority of system handler 6, UsageFault
[15:8]	**PRI_5**	Priority of system handler 5, BusFault
[7:0]	**PRI_4**	Priority of system handler 4, MemManage

System Handler Priority Register 2 (SHPR2)

Register	Offset	R/W	Description	Reset Value
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:24]	**PRI_11**	**Priority of System Handler 11 – SVCall** "0" denotes the highest priority and "15" denotes the lowest priority.
[27:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:24]	**PRI_15**	**Priority of System Handler 15 – SysTick** “0” denotes the highest priority and “15” denotes the lowest priority.
[23:16]	**PRI_14**	**Priority of System Handler 14 – PendSV** “0” denotes the highest priority and “15” denotes the lowest priority.
[15:0]	**Reserved**	Reserved.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex-M33 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC) and PLL to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

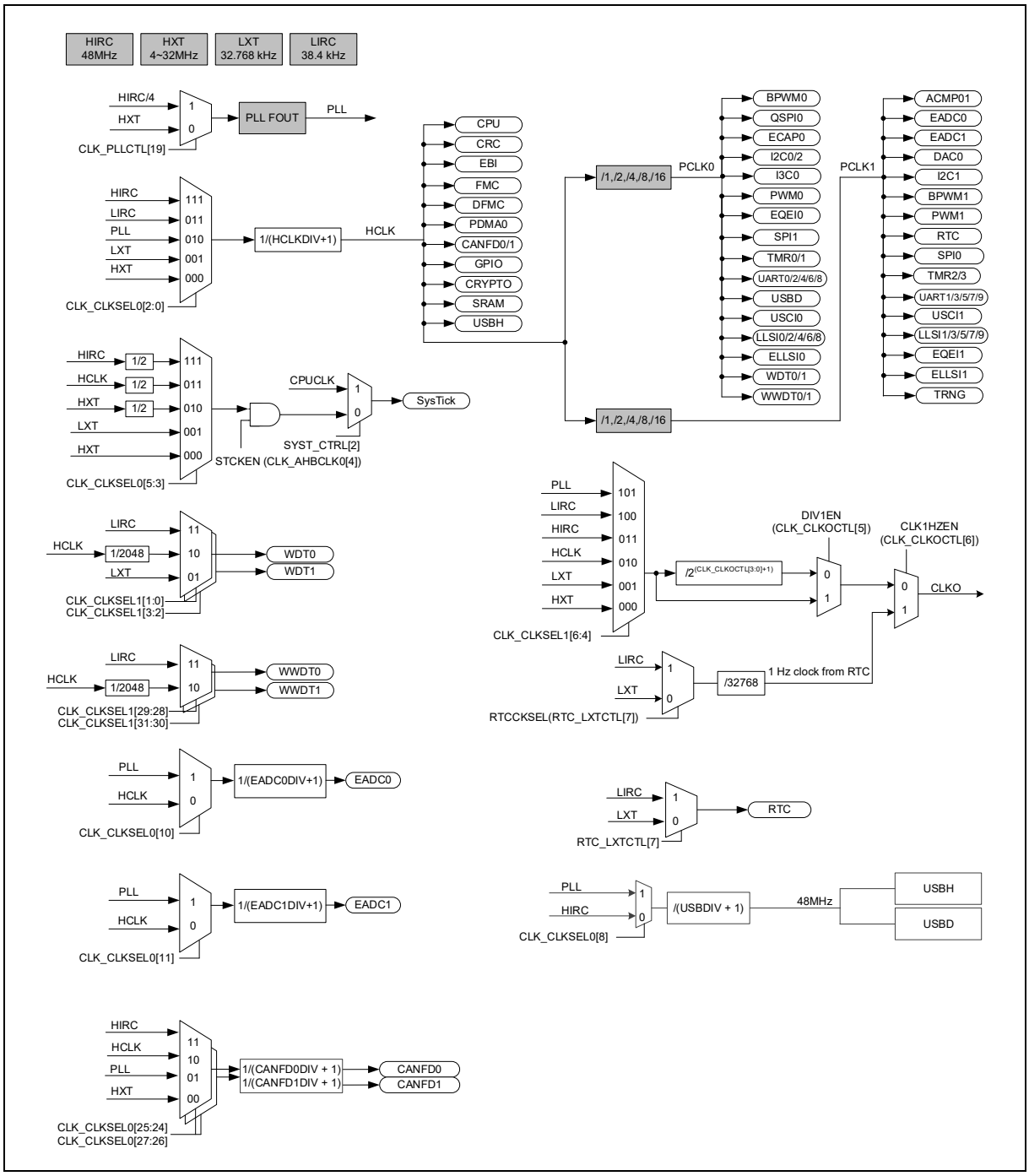


Figure 6.3-1 Clock Generator Global View Diagram (1/2)

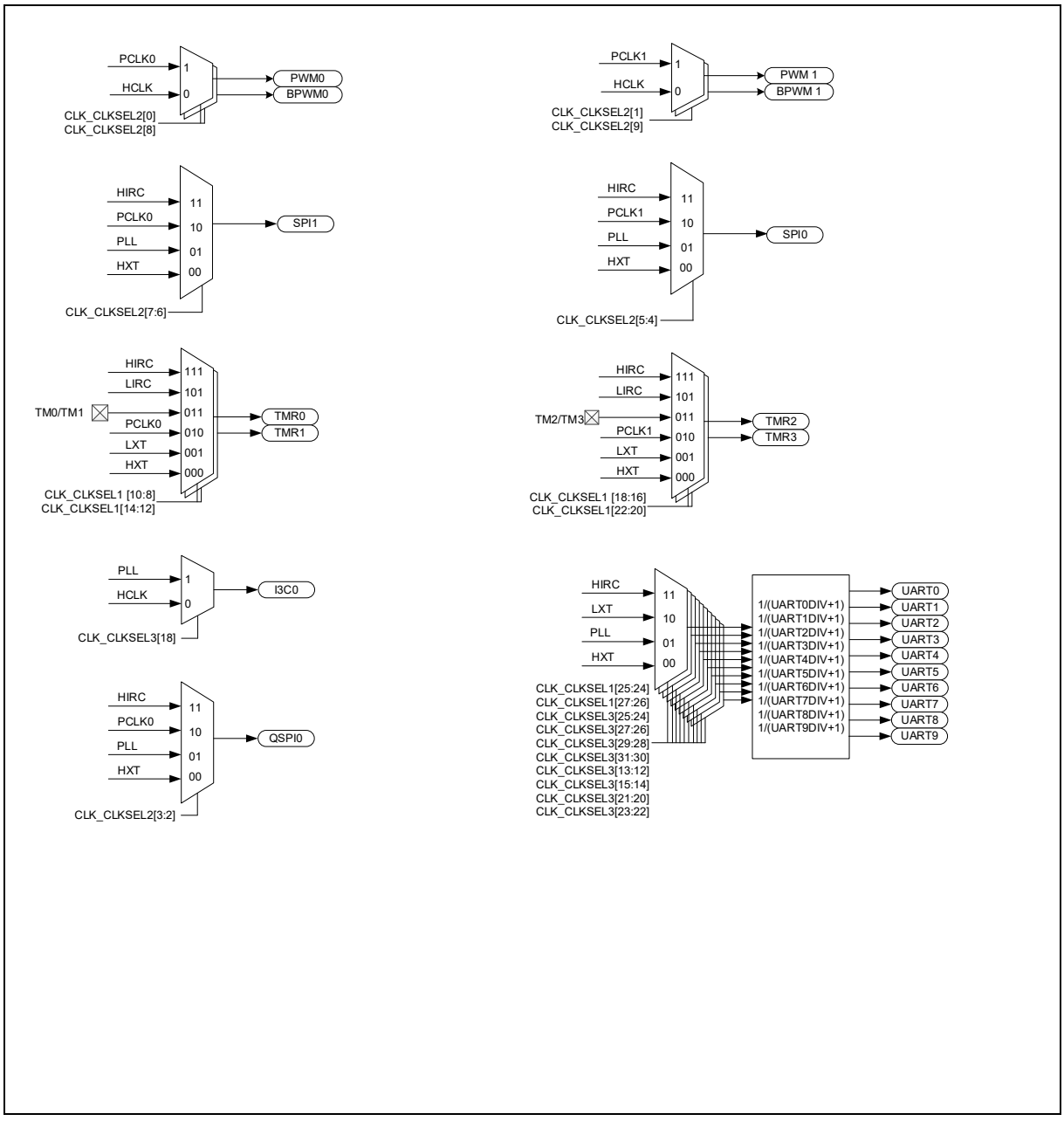


Figure 6.3-2 Clock Generator Global View Diagram (2/2)

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~32 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator (HIRC) divided 4
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index is set to 1 after stable counter value reach a define value as shown in Table 6.3-1.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-2 will auto clear when user disables the clock source.

Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clocks	341.33us for 12 MHz
LXT	32768 LXT clocks	1s for 32.768 kHz
PLL	2400 PLL source clocks STBSEL(CLK_PLLCTL[23])=0 6400 PLL source clocks STBSEL(CLK_PLLCTL[23])=1	200us for 12 MHz 533us for 12 MHz
LIRC	1 LIRC clock	26.04us for 38.4 kHz
HIRC	1024 HIRC clocks HIRCSTBS(CLK_PWRCTL[17:16])=0x0 512 HIRC clocks HIRCSTBS (CLK_PWRCTL[17:16])=0x1	21.33us for 48 MHz 10.66us for 48 MHz

Table 6.3-1 Clock Stable Count Value Table

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
HXT	HXTEN(CLK_PWRCTL[0])	HXTSTB(CLK_STATUS[0])
LXT	LXTEN(CLK_PWRCTL[1])	LXTSTB(CLK_STATUS[1])
PLL	PD(CLK_PLLCTL[16])	PLLSTB(CLK_STATUS[2])
LIRC	LIRCEN(CLK_PWRCTL[3])	LIRCSTB(CLK_STATUS[3])
HIRC	HIRCEN(CLK_PWRCTL[2])	HIRCSTB(CLK_STATUS[4])

Table 6.3-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table

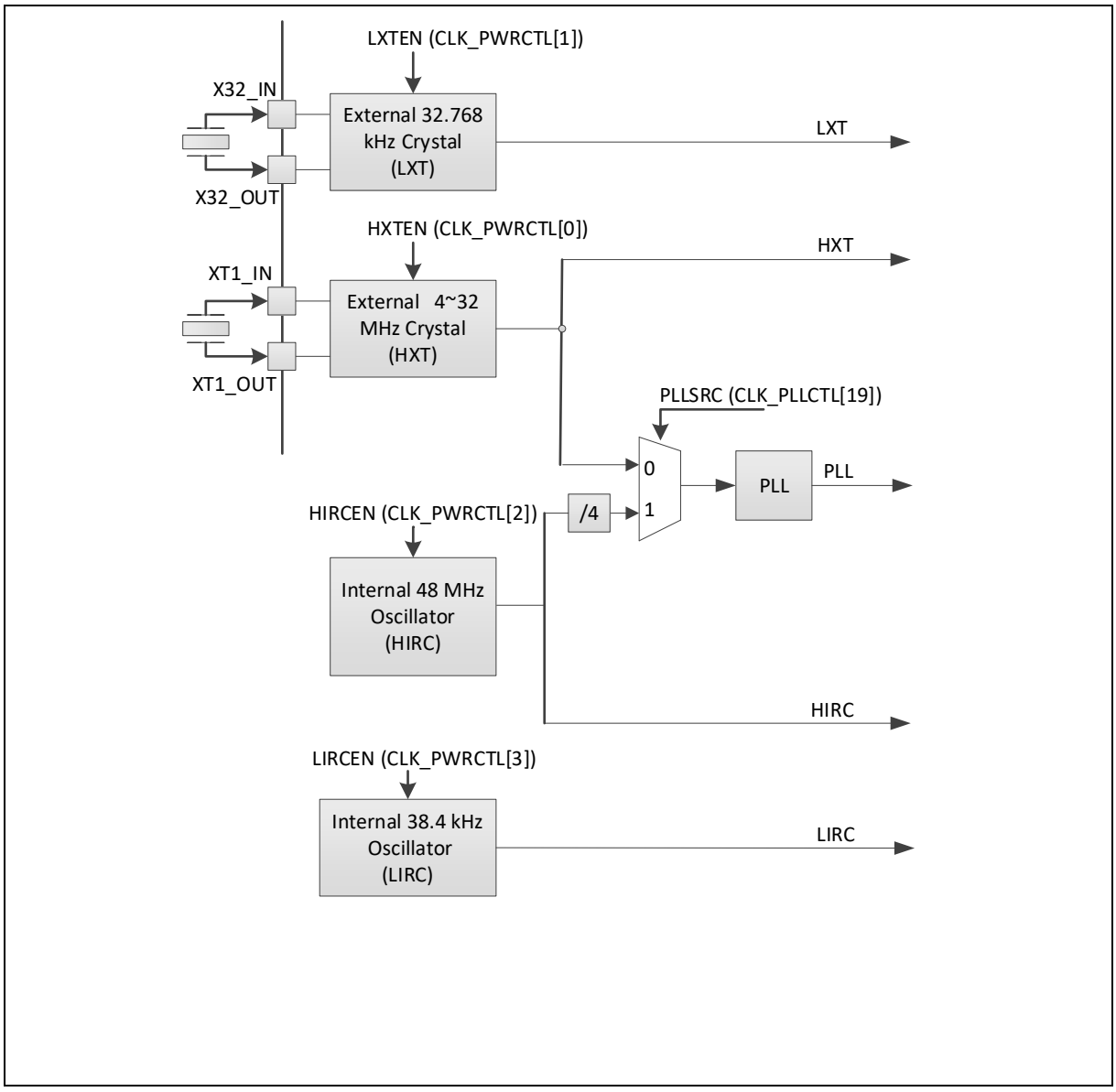


Figure 6.3-3 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-4.

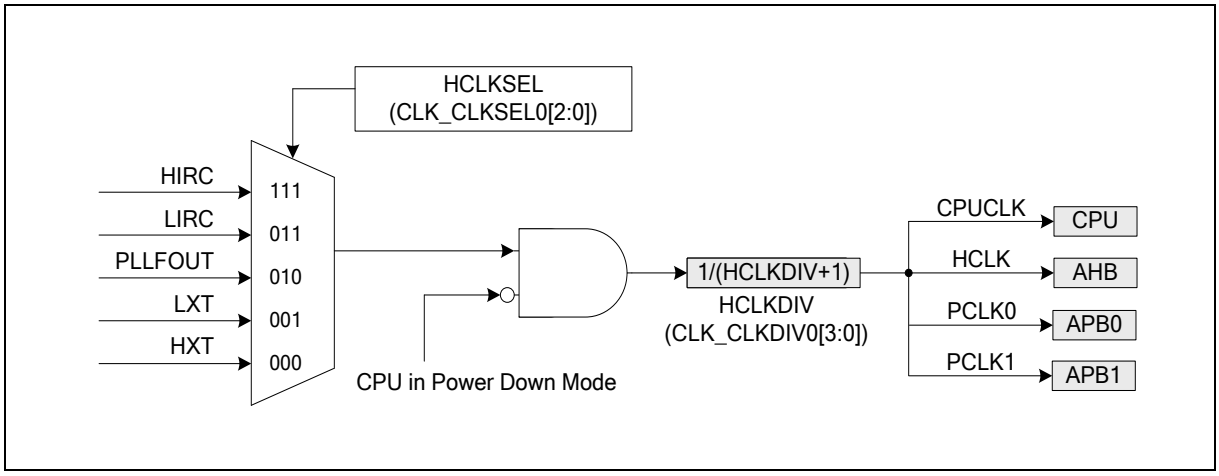


Figure 6.3-4 System Clock Block Diagrams

The clock source of SysTick in Cortex-M33 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5 SysTick Clock Control Block Diagram.

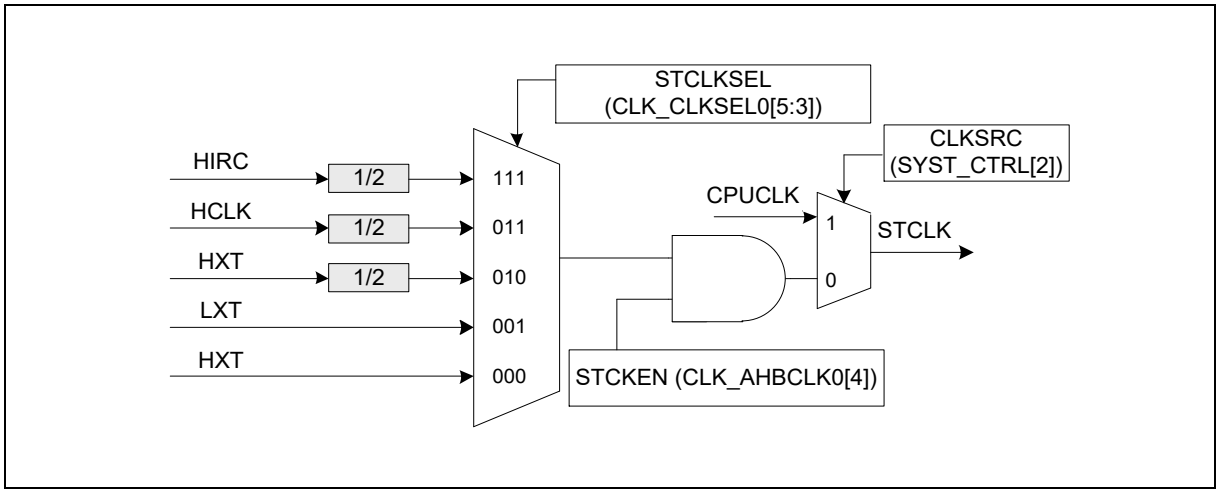


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Clock Fail Detection

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-6 shows that the HXT clock stops detection and system clock switches to HIRC procedure.

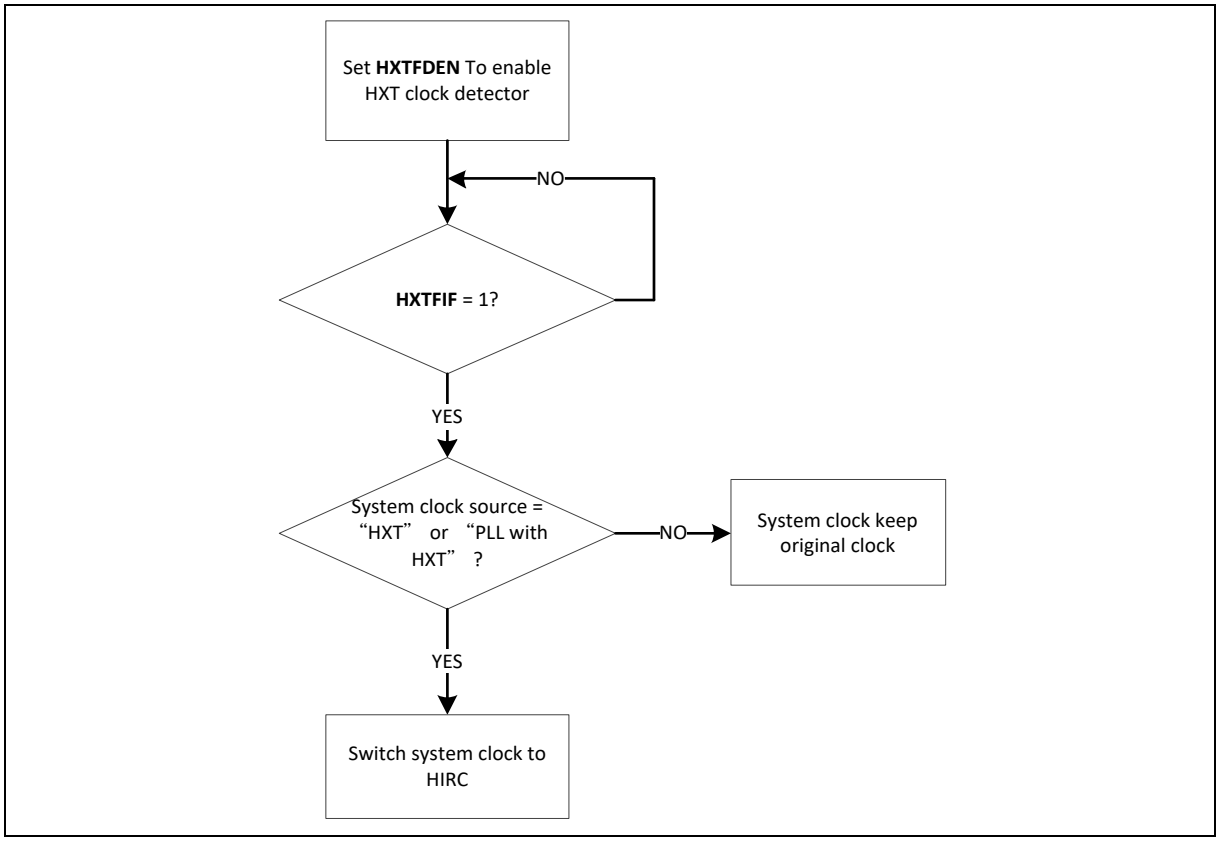


Figure 6.3-6 HXT Stop Protect Procedure

Besides, User can also monitor HXT CLK frequency range by HIRC clock. User can set UPERBD (CLK_CDUPB[10:0]) and LOWERBD (CLK_CDLOWB[10:0]) to decide monitoring frequency window.

The formula of UPERBD and LOWERBD is listed below.

HIRC_period* 1024 < HXT_period* UPERBD

HIRC_period* 1024 > HXT_period* LOWERBD

6.3.5 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

6.3.6 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.7 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT or LIRC.

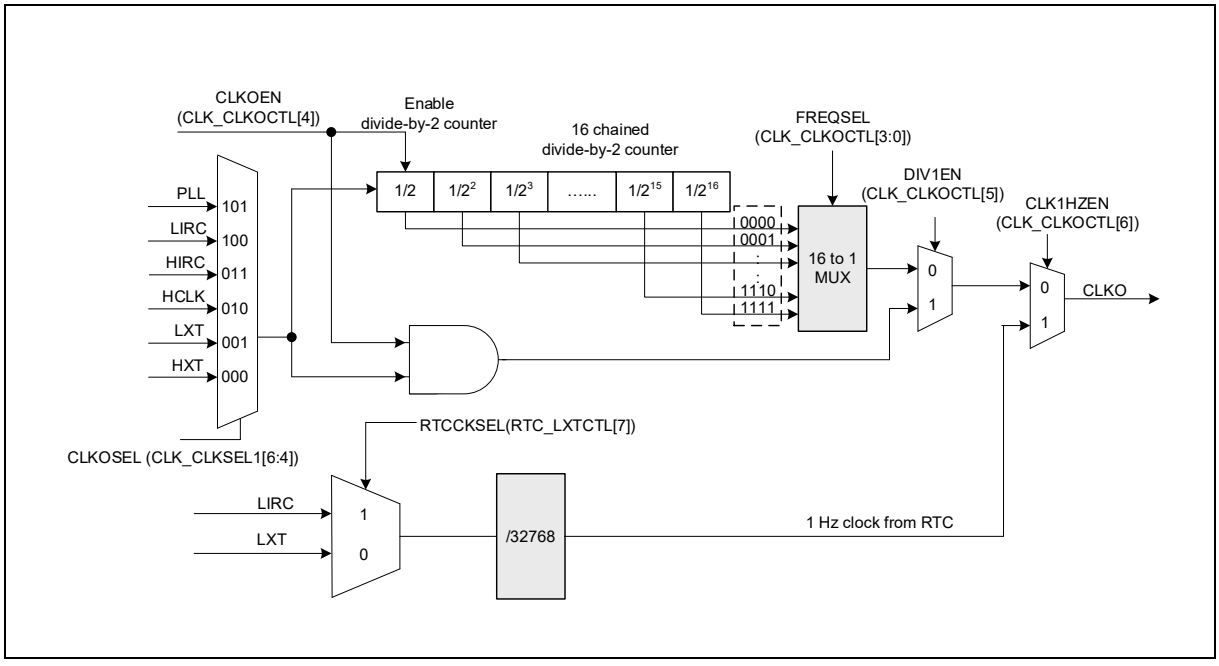


Figure 6.3-7 Clock Output Block Diagram

6.3.8 Share Registers

The clock controller shares part of register information to non-secure world with enable bits in SYSSIAEN (SCU_SINFAEN[1]) register. Shared registers are enabled by default.

Shared Register Access	Clock Controller

R/W	NA
Read only	CLK_PWRCTL, CLK_AHBCLK0, CLK_APBCLK0, CLK_APBCLK1, CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3, CLK_CLKDIV0, CLK_CLKDIV1, CLK_PCLKDIV, CLK_PLLCTL, CLK_STATUS
Write only	NA

Table 6.3-3 Clock Controller Share Register List

6.3.9 USB Clock Source

The clock sources of USB 1.1 systems are generated from HIRC or programmable PLL output. The generated clocks are shown in Figure 6.3-8.

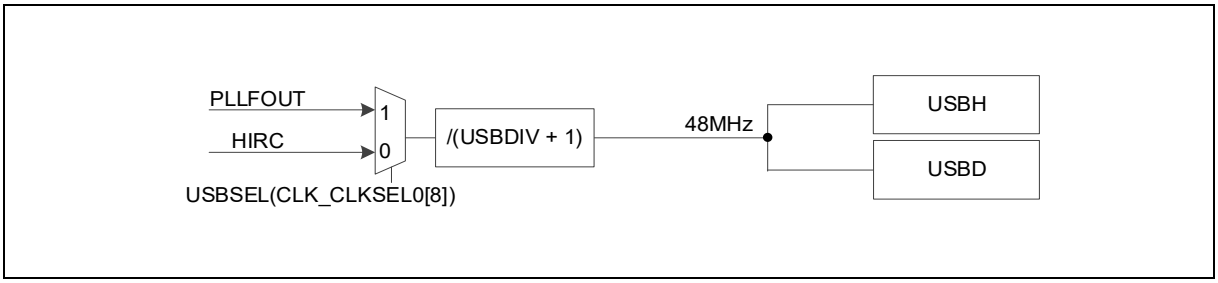


Figure 6.3-8 USB Clock Source

6.4 Security Configuration Unit (SCU)

6.4.1 Overview

Security configuration unit is designed for Arm® TrustZone®, and used to configure the security attribution of SRAM, GPIO as well as all other peripherals. SCU also collects AHB slaves' security violation response and generates SCU interrupt. SCU is also equipped with a timer to monitor the duration of the core processor in non-secure state.

Note: For details on Arm® TrustZone®, refer to the section "Arm® TrustZone®"

6.4.2 Features

- Configure SRAM's security attribution block by block
- Configure GPIOs' security attribution port by port and EINT's security attribution separately
- Configure peripherals' security attribution
- Generate secure violation interrupt
- Equipped with a 24-bit timer as a non-secure state monitor

6.5 True Random Number Generator (TRNG)

6.5.1 Overview

True Random Number Generator (TRNG) consists of an entropy source from analog macro and a CTR_DRBG. There is a calibration mechanism of internal TRNG for randomness of generating true random number. Besides, there is a CTR_DRBG design in this TRNG for the DRBG (deterministic random bit generator) of SP800-90A and the NRBG (non-deterministic random bit generator) of SP800-90C.

6.5.2 Features

- Up to 10Mbit/s data rate for entropy source
- Passes NIST SP800-22A standard
- Includes NIST SP800-90A known answer test for DRBG and NIST SP800-90B health test for entropy source (Start-up test, Repetition count test, Adaptive proportion test)
- Provides the true random number seed for PRNG

6.6 CACHE Controller (CACHE)

6.6.1 Overview

The CACHE is introduced on C-AHB bus of Cortex-M33 processor to improve memory access performance and reduce power consumption.

6.6.2 Features

- Supports one 32-bit AHB slave port
- Supports one 32-bit AHB master port
- Supports zero wait state on cache hits
- Supports LRU replacement (least recently used)
- Supports write-through policy
- Supports 32-bit hit monitor counter
- Supports 16-bit miss monitor counter
- Supports critical-word-first refill policy
- 8 Kbytes cache size
- Supports 1-bit parity check

Feature	CACHE
Number of ways	2
Cache size	8 Kbytes
Cache line width	8 bytes
Data width of AHB slave port	32 bits
Data width of AHB master port	32 bits

Table 6.6-1 CACHE Features

6.7 External Bus Interface (EBI)

6.7.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.7.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplex mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.8 Flash Memory Controller (FMC)

6.8.1 Overview

The FMC is equipped with dual-bank on-chip embedded Flash (BANK0 and BANK1) for application. Both BANK0 and BANK1 have 256/512 Kbytes space. Thus, the total size of application ROM (APROM) is 512/1024 Kbytes. A User Configuration block provides for system initiation. A 16 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. . A 32 Kbytes Secure Bootloader is used to check boot code integrity and authenticity, and consists of native ISP functions . A 8 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.8.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports dual-bank remapping
- Supports 512/1024 Kbytes application ROM (APROM)
- Supports 16 Kbytes loader ROM (LDROM)
- Supports 2 XOM (Execution Only Memory) regions to conceal user program in APROM.
- Supports 16 Kbytes Data Flash
- Supports User Configuration block for system initiation control
- Supports 8 Kbytes page erase for all embedded Flash
- Supports two level locks for protecting secure region and non-secure region.
- Supports Secure Bootloader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for check boot code integrity and authenticity
- Supports 32-bit/64-bit Flash programming function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports Non-Secure In-System-Programming (NS ISP) to update embedded Non-Secure Flash memory

6.9 Data Flash Memory Controller (DFMC)

6.9.1 Overview

The DFMC is equipped with 64 Kbytes of on-chip Data Flash to store application-dependent data, and supports a 256 bytes EEPROM emulation area. The emulated EEPROM provides word read and byte/word write functions.

6.9.2 Features

- Supports 64 Kbytes application Data Flash
- Supports 4096 bytes page erase for all embedded Flash
- Supports CRC32 checksum calculation function
- Supports Data Flash all one verification function
- Supports In-System-Programming (ISP) to update embedded Data Flash memory
- Supports hardware EEPROM emulation (256 bytes, with byte write capability)

6.10 General Purpose I/O (GPIO)

6.10.1 Overview

This chip has up to 110 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB, PD and PE has 16 pins on port. PC has 15 pins on port. PF has 13 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of these pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. Please refer to the Datasheet for detailed pin operation voltage information about V_{DD}, V_{DDIO} and V_{BAT} electrical characteristics.

6.10.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports EINT0~7 edge detect and trigger function

6.11 PDMA Controller (PDMA)

6.11.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. PDMA controller has a total of 12 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.11.2 Features

- Supports 12 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, USCI, SPI, QSPI, ACMP,PWM, EINT, I^2C, I3C, Timer, LLSI, ELLSI, EADC, and DAC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type

6.12 Timer Controller (TMR)

6.12.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (TMx or TMx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

6.12.2 Features

6.12.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, BPWM, EADC, DAC, EQEI, and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP0 output, ACMP1 output, or internal USB SOF signal
- Supports internal capture triggered source from ACMP0 output, ACMP1 output, HXT, HIRC, LIRC and LXT.

6.12.2.2 PWM Function Features

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter:
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels

- Supports interrupt on the following events:
  - PWM period point, up-count compared point events
- Supports wake-up when interrupt occurs when clock source is LXT or LIRC
- PWM can generate output in Power-down mode
- Supports trigger EADC, PDMA, and DAC on the following events:
  - PWM period point and up-count compared point events
- Supports PWM output accumulator event to trigger PDMA transfer and EADC
- Supports PWM output accumulator event to stop PWM counting

6.13 PWM Generator and Capture Timer (PWM)

6.13.1 Overview

The chip provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for EADC, PDMA and DAC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.13.2 Features

6.13.2.1 PWM Function Features

- Supports maximum clock frequency up to maximum 144 MHz frequency
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin, analog comparator, EADC result monitor and system safety events (clock failed, Brown-out detection, SRAM ECC double error and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC on the following events:
  - PWM counter matches 0, period value or compared value
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports PWM output accumulator stop counter mode
- Support External Pin Trigger Function

6.13.2.2 Capture Function Features

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.14 Basic PWM Generator and Capture Timer (BPWM)

6.14.1 Overview

The chip provides two BPWM generators. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0/1 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.14.2 Features

6.14.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum HCLK frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0/1in the following events:
  - BPWM counter matches 0, period value or compared value

6.14.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.15 Enhanced Input Capture Timer (ECAP)

6.15.1 Overview

The chip provides up to one unit of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.15.2 Features

- Up to one Input Capture Timer/Counter unit, CAP0
- Each unit has 3 input channels
- Each unit has its own interrupt vector
- Each input channel has its own capture counter hold register
- 24-bit Input Capture up-counting timer/counter
- With noise filter in front end of input ports
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter
- Supports compare-match function

6.16 Enhanced Quadrature Encoder Interface (EQEI)

6.16.1 Overview

There are two EQEI controllers in this device. The Enhanced Quadrature Encoder Interface (EQEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.16.2 Features

- Up to two EQEI controllers, EQEI0, EQEI1
- Two EQEI phase inputs, QEA and QEB; One Index input
- A 32-bit up/down Quadrature Encoder Pulse Counter (EQEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (EQEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (EQEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (EQEI_CNTCMP) with a Pre-set Maximum Count Register (EQEI_CNTMAX)
- A 32-bit up count Unit Timer Pulse Counter (EQEI_UTCNT)
- A 32-bit Unit Timer Pulse Counter Compare Register (EQEI_UTCMP)
- One EQEI control register (EQEI_CTL) and one EQEI Status Register (EQEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Supports X4 free-counting mode
  - Supports X2 free-counting mode
  - Supports X4 compare-counting mode
  - Supports X2 compare-counting mode
- Two Quadrature encoder phase counter operation modes:
  - Supports X1 1-phase 2 input compare-counting mode
  - Supports X2 1-phase 2 input compare-counting mode
- Two Quadrature encoder directional counter operation modes:
  - Supports X1 1-phase 1 input compare-counting mode
  - Supports X2 1-phase 1 input compare-counting mode
- Supports swap function for input signals QEA and QEB
- Supports for detecting the occurrence of phase error from input signals QEA and QEB
- Supports one times index signal reset function for Quadrature encoder pulse counter
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clock/8

6.17 Watchdog Timer (WDT)

6.17.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.17.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK = 32 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force Secure only WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.18 Window Watchdog Timer (WWDT)

6.18.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.18.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.19 Enhanced LED Light Strip Interface (ELLSI)

6.19.1 Overview

The ELLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There is one set of ELLSI that can be used.

The ELLSI also supports LED strip advanced command protocol, including Set ID Command (SET_ID), Clear ID Command (CLR_ID), Check ID Command (CHK_ID), Specify ID Command (SPE_ID), Feedback Command and TH20 SET Command (TH20_SET), etc.

6.19.2 Features

- 2 set of ELLSI channels with IDLE polarity control
- ELLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer
- Supports LED advanced command mode (Feedback, TH20 SET Mode, Command mode)
- Configurable advanced command pulse width

6.20 Real Time Clock (RTC)

6.20.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.20.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM
- Supports Leap Year indication in RTC_LEAPYEAR register
- Supports Day of the Week counter in RTC_WEEKDAY register
- Frequency of RTC clock source compensate by RTC_FREQADJ register
- All time and calendar message expressed in BCD format
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports RTC Time Tick and Alarm Match interrupt
- Supports 1 Hz clock output
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated
- Supports Daylight Saving Time software control in RTC_DSTCTL

6.21 UART Interface Controller (UART)

6.21.1 Overview

The chip provides ten channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485, Single-wire function modes and auto-baud rate measuring function.

6.21.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads

  (UART0~7 support FIFO, UART8,9 do not support FIFO and CTS/RTS)
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
  - LIN slave header time-out detection function
  - LIN response time-out detection function
  - LIN wake-up function
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission

direction

- Supports PDMA transfer function
- Supports Single-wire function mode.
- Supports bus idle time-out mode
- Supports fractional Baud Rate divider

UART Feature	UART0/ UART1	UART0 ~ UART7	UART8~ UART9	USCI-UART
FIFO	16 Bytes	16 Bytes	1 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√		√
IrDA	√	√		-
LIN	√	-	-	-
RS-485 Function Mode	√	√		√
nCTS Wake-up	√	√		√
Incoming Data Wake-up	√	√		√
Received Data FIFO reached threshold Wake-up	√	√		-
RS-485 Address Match (AAD mode) Wake-up	√	√		-
Received Data FIFO reached threshold Time-out Wake-up	√	√		-
Baud Rate Compensation	√	√		-
Auto-Baud Rate Measurement	√	√		√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√		√
Stick Bit	√	√		-

Table 6.21-1 M3351 Series UART Features

6.22 I²C Serial Interface Controller (I²C)

6.22.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are three sets of I²C controllers which support Power-down wake-up function.

6.22.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable
- Supports pin swap function
- Only I2C0 and I2C1 support Bus Management (SM/PM compatible) function Compatible with the SMBUS specification rev 2.0 (http://smbus.org/specs/) and PMBUS specification rev 1.2 (http://pmbus.org/)

6.23 I3C Serial Interface Controller (I3C)

6.23.1 Overview

I3C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The Improved Inter Integrated Circuit (I3C) is part of a group of communication protocols defined by the MIPI Alliance. This specification is developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

The I3C controller is dual role device and meets the requirement of I3C protocol and I^2C protocol as specified by the MIPI I3C Specification. The specific reference documents is:

- MIPI Alliance Specification for I3C Basic Specification Version 1.1.1

6.23.2 Features

- Supports one I3C port
- Supports Controller and Target mode
- Static or Dynamic Target Device support
- Built-in Hardware Dynamic Address Allocation support
- Built-in CCC transfer handler
- Auto Hot-Join request generation support
- In-Band Interrupt request generation support
- Adaptive mode of operation between I^2C and I3C depending on I3C bus traffic
- Built-in TE0-TE5 Error Handling
- Supports Power-down wake-up function
- Supports PDMA mode for data transfer
- Supports SDR mode, data rates up to 12.5 Mbps
- Supports HDR-DDR mode, data rates up to 25 Mbps
- Supports Secondary Controller mode
- Supports Set Static Address as Dynamic Address CCC
- Supports Target Reset
- Supports Asynchronous Timing Control(Modes 0)
- Supports Grouped Addressing
- Supports HDR-BT mode

6.24 LED Light Strip Interface (LLSI)

6.24.1 Overview

The LLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There are ten sets of LLSI that can be used.

6.24.2 Features

- 10 sets of LLSI channels with IDLE polarity control
- Each LLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer

6.25 Serial Peripheral Interface (SPI)

6.25.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to 2 sets of SPI controllers (detail to refer “M3351 feature comparison table” section) performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.25.2 Features

- SPI Mode
  - Up to 2 sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 36 MHz (when chip works at V_{DD} = 2.7~5.5V)
  - Slave mode up to 18 MHz (when chip works at V_{DD} = 2.7~5.5V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports 1 set of Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.26 Quad Serial Peripheral Interface (QSPI)

6.26.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains a QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.26.2 Features

- Supports Master or Slave mode operation
- Master mode up to 36 MHz (when chip works at V_{DD} = 4.5V~5.5V)
- Slave mode up to 18 MHz (when chip works at V_{DD} = 4.5V~5.5V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.27 USCI - Universal Serial Control Interface Controller (USCI)

6.27.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.27.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.28 USCI – UART Mode

6.28.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.28.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup)

6.29 USCI - SPI Mode

6.29.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

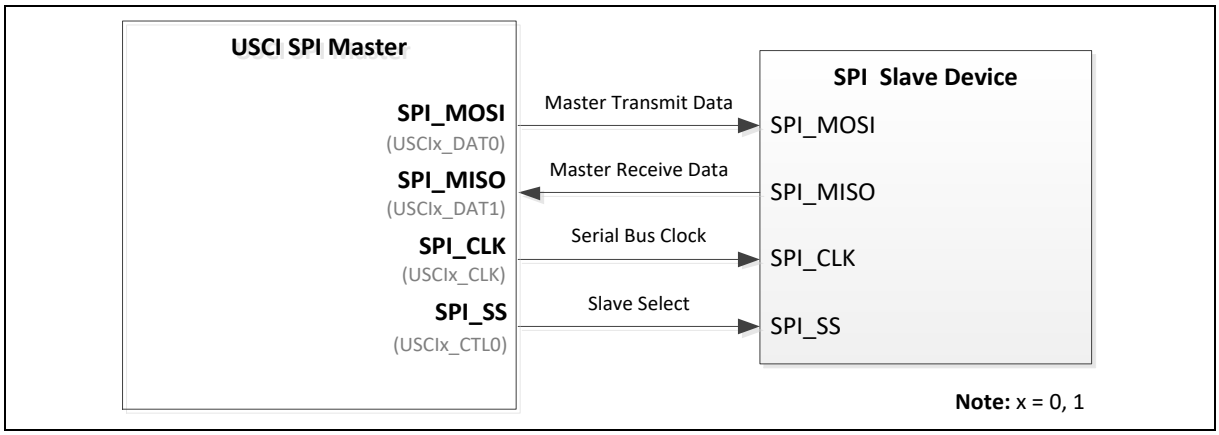


Figure 6.29-1 SPI Master Mode Application Block Diagram

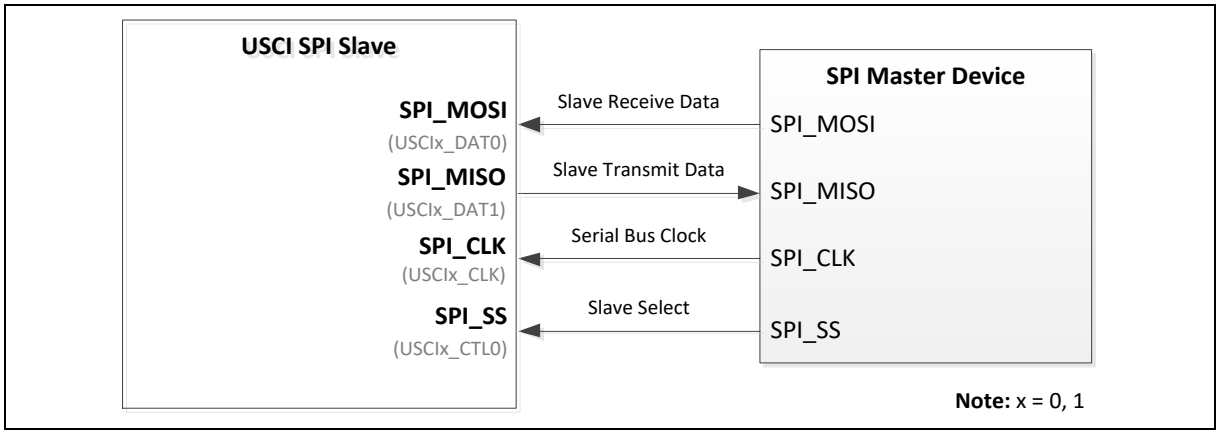


Figure 6.29-2 SPI Slave Mode Application Block Diagram

6.29.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer

- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.30 USCI - I²C Mode

6.30.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.30-1 for more detailed I²C Bus Timing.

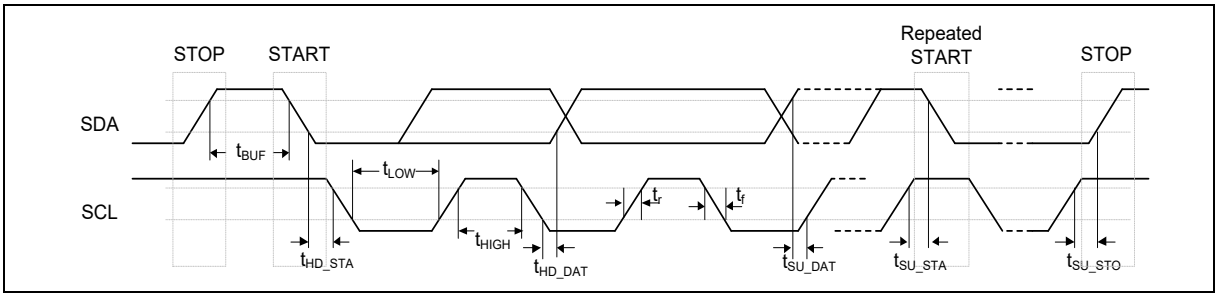


Figure 6.30-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.30.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.31 USB 1.1 Device Controller (USBD)

6.31.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1K byte sizes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEG0~22).

There are 23 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, and BUS events, such as suspend and resume and SOF event, receive Start of Frame(SOF) packet in every 1ms event. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0~3) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.31.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBDET, USB, BUS and SOF)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 23 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability
- Supports double buffer function
- Supports V_{BUS} plug in / out or resume wake up from Power-down mode
- Supports USB 2.0 Link Power Management (LPM)

6.32 USB 1.1 Host Controller (USBH)

6.32.1 Overview

This chip is equipped with one USB 1.1 FS Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.32.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0
- Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers
- Supports an integrated Root Hub
- Supports port power control and port overcurrent detection
- Supports DMA for real-time data transfer

6.33 Controller Area Network with Flexible DataRate (CAN FD)

6.33.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and needs to be connected to additional transceiver hardware for the CAN bus physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.33.2 Features

- Conforms to CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.34 CRC Controller (CRC)

6.34.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-8, CRC-16, CRC-32, and 32-bits programmable polynomials settings.

6.34.2 Features

- Supports four common polynomials CRC-8, CRC-16, and CRC-32
- Programmable seed value
- Programmable polynomials settings
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports Master mode

6.35 Enhanced 12-bit Analog-to-Digital Converter (EADC0)

6.35.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converters (SAR EADC converter) with 24 external input channels and 3 internal channels. The EADC converter can be started by software trigger, PWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger, external pin (EADC0_ST) input signal, and ACMP0~1 triggers.

6.35.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 5.5V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 24 single-end analog external input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and $AV_{DD}/4$.
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 36 MHz for EADC
- Up to 1.71 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage V_{REF}: 2.560V, 3.072V and 4.086V.
- Supports power-down mode
- Up to 27 sample modules
  - Sample modules0~23 is configurable for EADC converter channel (EADC_CH0~23) and trigger source for each EADC
  - Sample module 24~26 is fixed for channel 24, 25, 26 input sources as band-gap voltage, temperature sensor, and $AV_{DD}/4$.
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 27 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~26)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - PWM/BPWM triggers
  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay counter
  - ACMP0, ACMP1 interrupt pulse triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.36 Enhanced 14-bit Analog-to-Digital Converter (EADC1)

6.36.1 Overview

The chip contains 14-bit successive approximation analog-to-digital converters (SAR EADC converter) with 16 external input channels. The EADC converter can be started by software trigger, PWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger, external pin (EADC1_ST) input signal, and ACMP0~1 triggers.

6.36.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 5.5V)
- Reference voltage from V_{REF} pin
- 14-bit resolution
- Up to 16 single-end analog external input channels
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 25 MHz for EADC
- Up to 1 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage V_{REF}: 2.560V, 3.072V and 4.086V .
- Supports power-down mode
- Up to 16 sample modules
  - Sample modules0~15 is configurable for EADC converter channel (EADC_CH0~15) and trigger source for each EADC
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 16 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 14-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 22-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~15)
  - External pin EADC1_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - PWM/BPWM triggers
  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay counter
  - ACMP0, ACMP1 interrupt pulse triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.37 Digital to Analog Converter (DAC)

6.37.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.37.2 Features

- Analog output voltage range: 0~AV_{DD}
- Supports 12- or 8-bit output mode
- Rail to rail settle time 8us
- Supports a 12-bit voltage type DAC
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin
- DAC maximum conversion updating rate 1 MSPS
- Supports voltage output buffer mode and bypass voltage output buffer mode
- Supports software and hardware trigger, including Timer0~3, PWM0, PWM1 and external trigger pin to start DAC conversion
- Supports PDMA mode

6.38 Analog Comparator Controller (ACMP)

6.38.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.38.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 20mV, 40mV.
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2 and ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP0_P2 and ACMP0_P3
  - 4 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- Shares one ACMP interrupt vector for two comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode
- Supports offset calibration
- Supports ACMP0 event, ACMP1 event be as PDMA request source
- Supports ACMP0 event, ACMP1 event be as EADC trigger source
- Supports ACMP0 output, ACMP1 output be as Timer, ECAP and PWM trigger source

6.39 Cryptographic Accelerator (CRYPTO)

6.39.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, and SHA/HMAC algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255 and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, CBC-CS3, CCM and GCM mode.

The SHA accelerator is an implementation fully compliant with the MD5, SHA-160, SHA-224, SHA-256, SHA-384, SHA-512. The SHA accelerator supports HMAC (Keyed-Hash Message Authentication Code) algorithms include HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, HMAC-SHA-512.

6.39.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255 and 256 bits random number
  - Able to take the true random number seed from TRNG
- AES
  - Supports encryption and decryption with 128, 192, and 256 bits key in FIPS NIST 197
  - Supports key expander for key expansion in FIPS NIST 197
  - Supports ECB, CBC, CFB, OFB, CTR modes in SP800-38A
  - Supports CBC-CS1, CBC-CS2 and CBC-CS3 modes in SP800-38A-addendum
  - Supports CCM mode in SP800-38C
  - Supports GCM mode and GMAC mode in SP800-38D
- SHA
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 in FIPS NIST 180, 180-2, 180-4
  - Supports MD5 in IETF Protocols RFC 1321
- HMAC
  - Supports FIPS 198 and IETF Protocols RFC 2104
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512
  - Supports HMAC-MD5

6.40 Peripherals Interconnection

6.40.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

6.40.2 Peripherals Interconnect Matrix Table

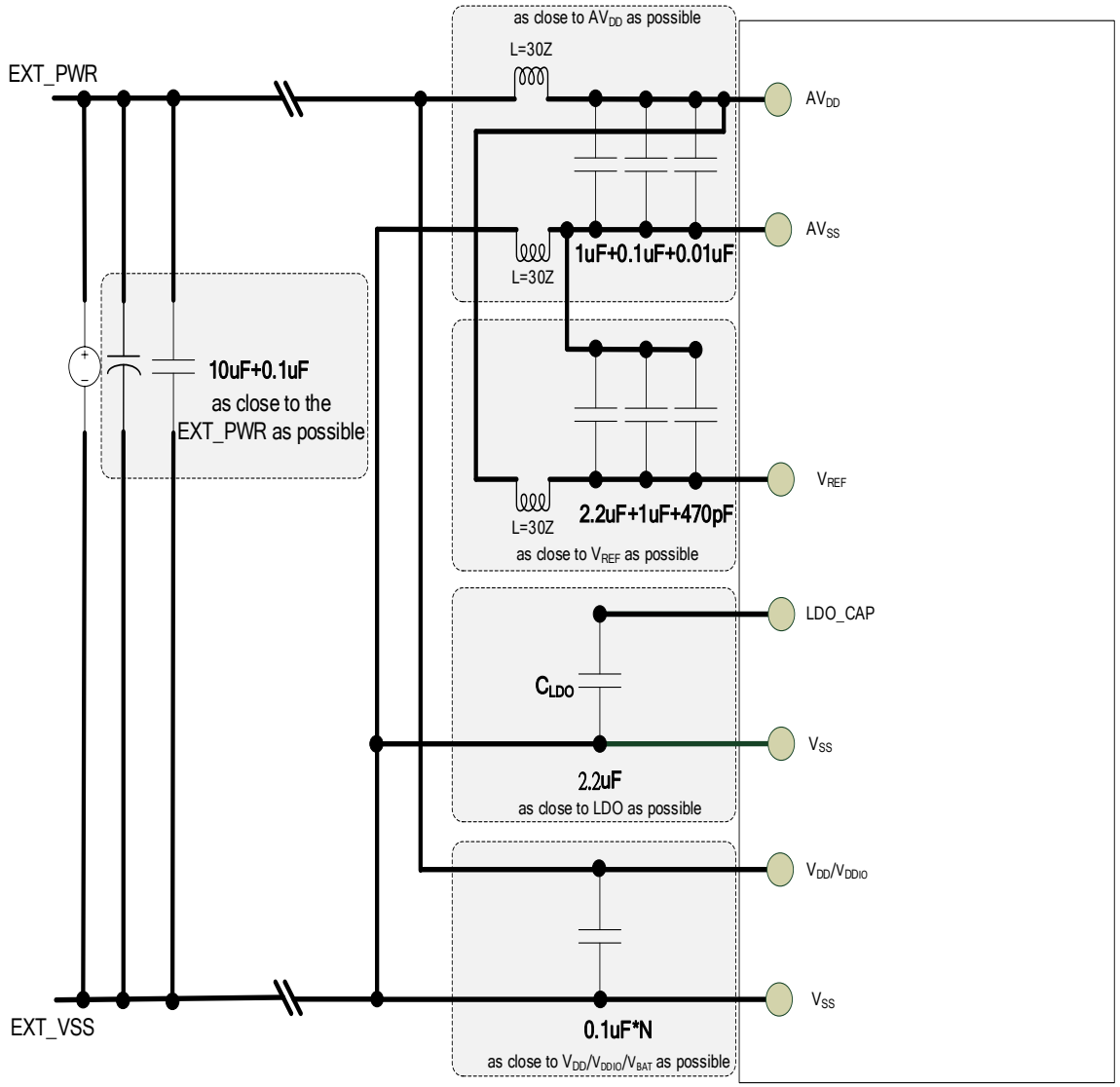
Please refer to the relative Technical Reference Manual for detailed functional description about the peripherals interconnection.

Source		Destination									
		EADC	ACMP		TMR	PWM	BPWM	SYSTEM	ECAP	EQEI	CANFD
		↘	↘	↘	↘	↘	↘	↘	↘	↘	↘
ACMP	√	√	-	-	√	√	-	-	√	-	√
	√	-	√	-	-	-	-	-	-	-	-
CLKCTL	√	-	-	-	√	-	-	-	-	-	-
EADC	√	-	-	-	-	√	-	-	-	-	-
PWM	√	√	-	-	-	√	√	-	-	-	-
EQEI	√	-	-	-	-	-	-	-	√	-	-
BPWM	√	√	-	-	-	√	√	-	-	-	-
SYSTEM	√	-	-	-	√	-	-	√	-	-	-
	√	√	-	-	-	-	-	-	-	-	-
	√	√	√	-	-	-	-	-	-	-	-
	√	√	-	√	-	-	-	-	-	-	-
	√	-	-	-	√	-	-		-	-	-
	√	-	-	-	√	-	-	-	-	-	-
	√	-	-	-	√	-	-	-	-	-	-
	√	-	-	-	√	√	-	-	-	-	-
	√	-	-	-	√	√	-	-	-	-	-
	√	-	-	-	√	√	-	-	-	-	-
	√	-	-	-	√	√	-	-	-	-	-
TMR	√	√	-	-	√	√	√	-	-	√	-

Table 6.40-1 Peripherals Interconnect Matrix Table

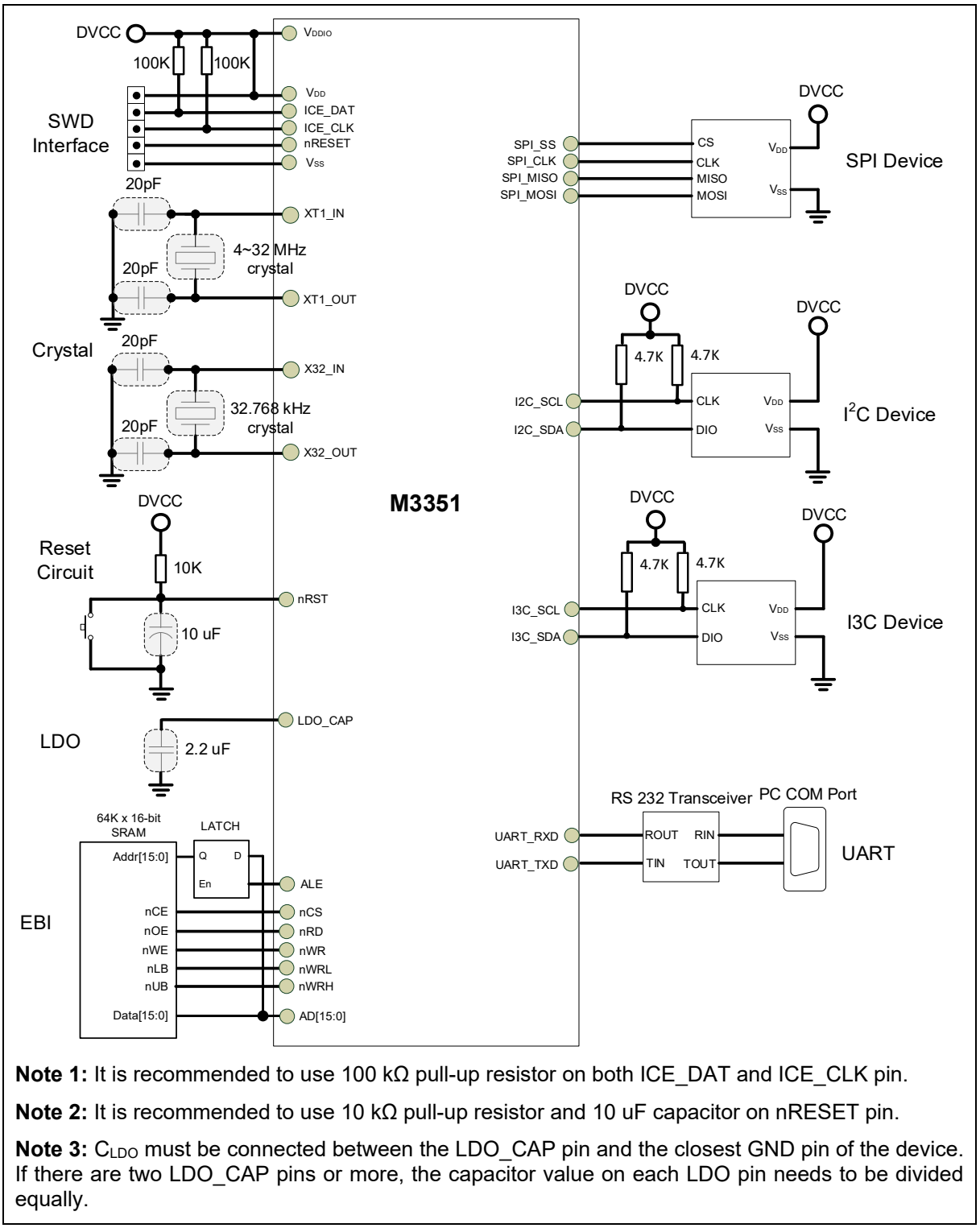
7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



Note: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

7.2 Peripheral Application Scheme

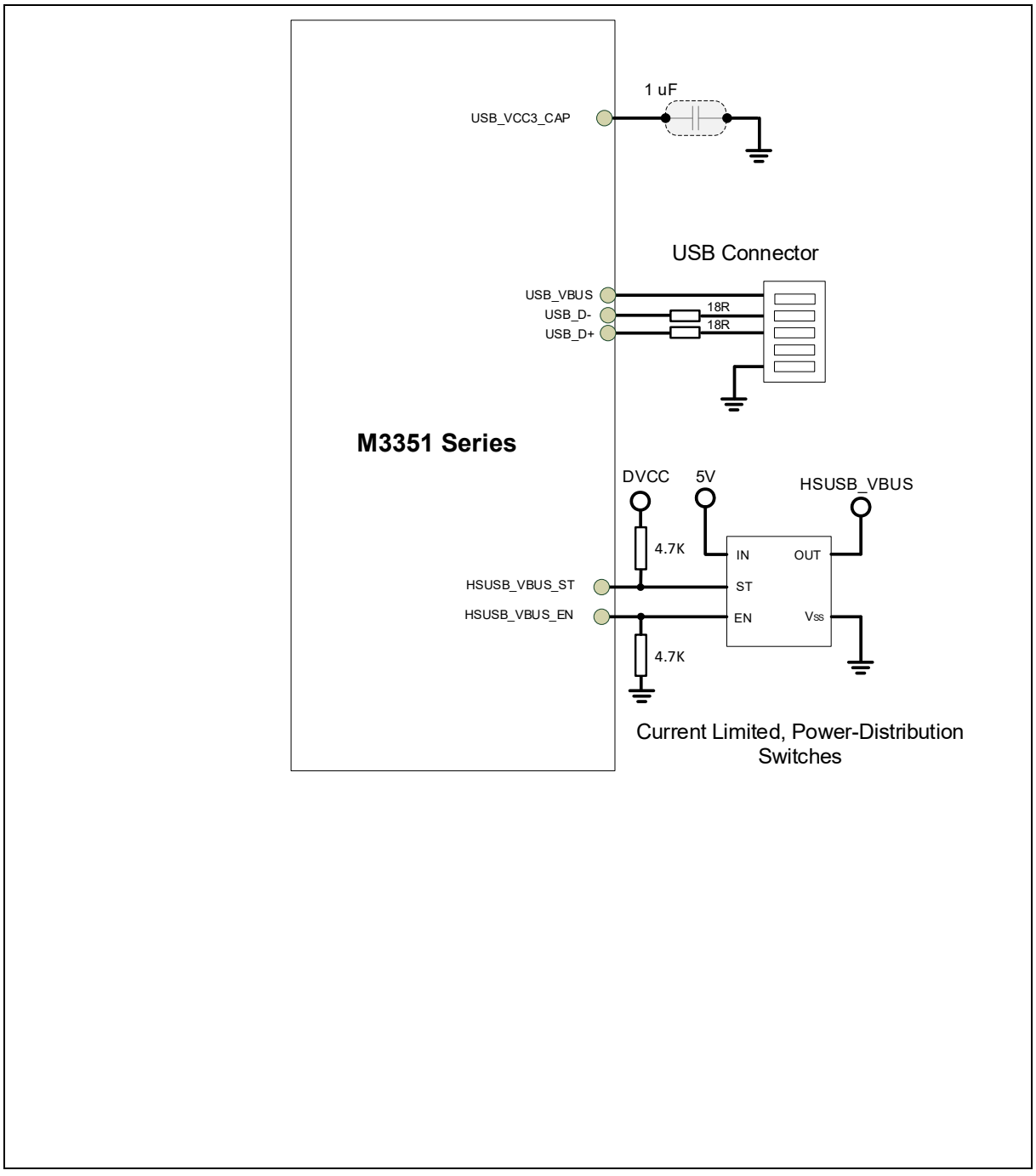


Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

7.3 USB Dual Role Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[1]	DC power supply	-0.3	6.5	V
V_{DDIO}-V_{SS}[1]	V_{DDIO} Power Supply	-0.3	6.5	V
V_{BUS}-V_{SS}[1]	V_{BUS} Power Supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\lvert V_{DD} - AV_{DD} \rvert$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\lvert V_{SS} - AV_{SS} \rvert$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on 5V-tolerance GPIO pin when $V_{DD} \geqslant 2.7V$	V_{SS}-0.3	V_{DD}	V
	Input voltage on any other pin[2]	V_{SS}-0.3	V_{DD}	V

Note:

1. All main power (V_{DD}, V_{DDIO}, AV_{DD}, V_{REF}, V_{BUS}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	-	50	
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[2]	-	100	
	Maximum current sourced by total I/O Pins[2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- θ_{JC} = thermal resistance junction-case (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1] (Still Air)	Thermal resistance junction-ambient 33-pin QFN(5x5 mm)	-	39.6	-	℃/Watt
	Thermal resistance junction-ambient 48-pin QFN(5x5 mm)	-	37.8	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
	Thermal resistance junction-ambient 100-pin LQFP(14x14 mm)	-	46	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	℃/Watt
θ_{JC}[1]	Thermal resistance junction-case 33-pin QFN(5x5 mm)	-	5	-	℃/Watt
	Thermal resistance junction-case 48-pin QFN(5x5 mm)	-	5	-	℃/Watt
	Thermal resistance junction-case 48-pin LQFP(7x7 mm)	-	19.6	-	℃/Watt
	Thermal resistance junction-case 64-pin LQFP(7x7 mm)	-	17	-	℃/Watt
	Thermal resistance junction-case 100-pin LQFP(14x14 mm)	-	11	-	℃/Watt
	Thermal resistance junction-case 128-pin LQFP(14x14 mm)	-	10	-	℃/Watt

Note:

1. The values are provided as reference values based on a four-layer board and are determined in accordance with JESD51. Thermal resistance is influenced by the number of layers and the overall size of the PCB.

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit component will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

8.1.4.4 Conducted Immunity (CI)

The conducted immunity testing relates to electromagnetic disturbances coming from intended radio-frequency (RF) transmitters in the frequency range 150 kHz up to 80 MHz. The CI test is one important characteristic of touch key MCU to address the effects of unwanted noise disturbances.

The conducted immunity requirements for electronic products are defined in IEC 61000-4-6 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	-4K	-	4K	V
V_{CDM}[2]	Electrostatic discharge,charge device model	-750	-	750	
LU[3]	Pin current for latch-up[3]	-200	-	200	mA
V_{EFT}[4]	Fast transient voltage burst	-4.4	-	4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.
5. Determinded according to IEC 61000-4-6 standard and the performance class is class A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
33-pin QFN(5x5 mm) [1]	MSL 3
48-pin QFN(5x5 mm) [1]	MSL 3
48-pin LQFP(7x7 mm) [1]	MSL 3
64-pin LQFP(7x7 mm) [1]	MSL 3
100-pin LQFP(14x14 mm) [1]	MSL 3
128-pin LQFP(14x14 mm) [1]	MSL 3

Note:
1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

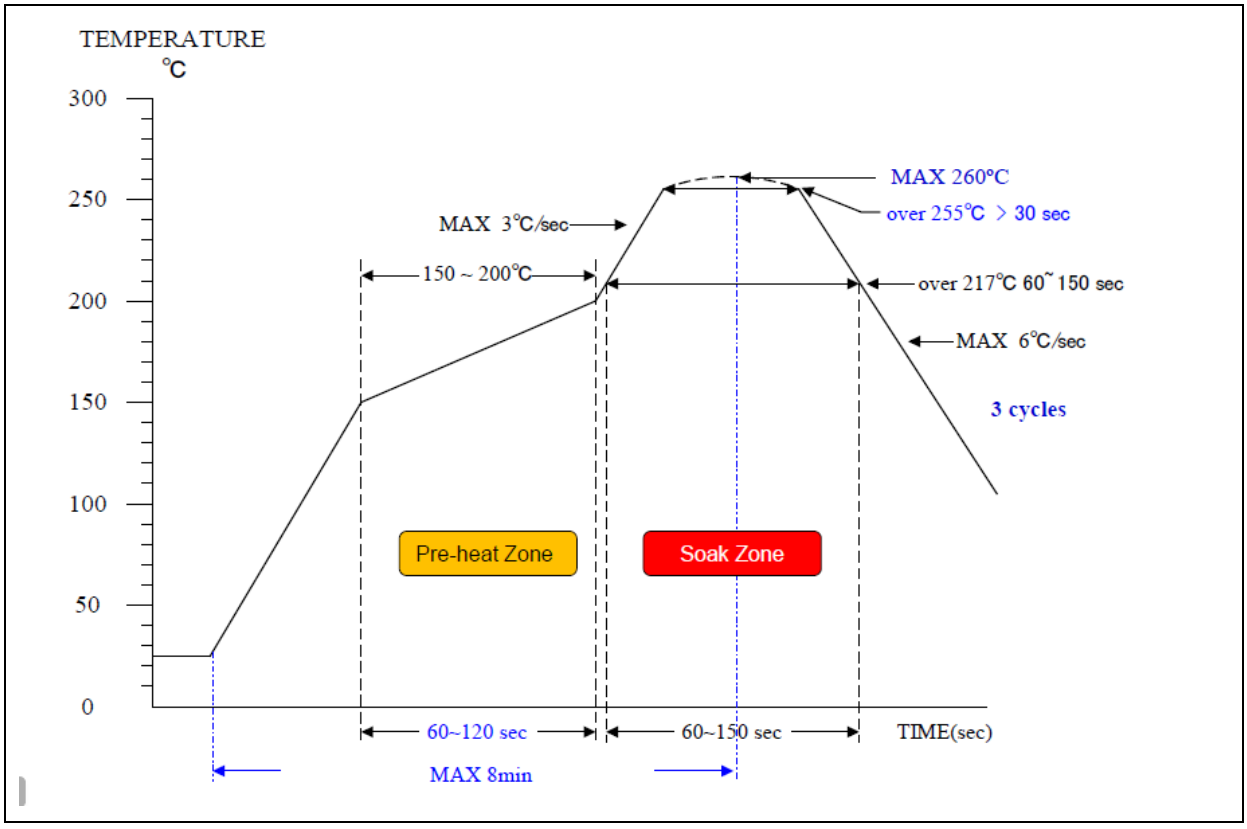


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.7 ~ 5.5 V, T_A = 25°C, HCLK = 144 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	144	MHz	
V_{DD}	Operation voltage	2.7	-	5.5		
V_{DDIO}	V_{DDIO} operation voltage	1.7	-	5.5		
AV_{DD}[1]	Analog operation voltage	V_{DD}				Except ADC, ACMP and DAC[4]
V_{REF}	Analog reference voltage	2.7	-	AV_{DD}		Except ADC[4]
V_{LDO}	LDO output voltage	-	1.18	-		
V_{BG}	Band-gap voltage	-3%	1.2	3%	V	
T_{VBG_ADC}[3]	ADC sampling time when reading the band-gap voltage	100	-	-	µS	
C_{LDO}[2]	LDO regulator output capacitor	2.2			µF	
R_{ESR}[3]	ESR of C_{LDO} capacitor	-	-	0.1	Ω	
I_{RUSH}[3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	200	mA	
E_{RUSH}[3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.596	-	µC	V_{DD} = 5.5 V, T_A = 105 °C, I_{RUSH} = 200 mA for 2000 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.7 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
		V_{DD}	5	5.5	5.5	5.5	V
I_{DD_IOP}	Normal run mode, executed from Flash, all peripherals disable HIRC, PLL, HXT, LXT or LIRC clock	144 MHz	12.54	17.06	33.62	45.20	mA
		120 MHz	11.02	15.50	32.02	43.58	
		96 MHz	9.43	13.87	30.31	41.87	
		84 MHz	8.43	12.84	29.26	40.79	
		72 MHz	7.96	12.35	28.77	40.32	
		60 MHz	6.86	11.22	27.58	39.13	
		50 MHz	5.95	10.28	26.62	38.12	
		48 MHz	5.33	9.66	25.93	37.41	
		32 MHz	10.57	15.51	30.89	42.34	
		24 MHz	3.39	7.66	23.88	35.33	
		12 MHz	2.25	6.49	22.64	34.09	
		6 MHz	1.67	5.90	22.05	33.49	
		3 MHz	1.39	5.61	21.73	33.19	
		38.4 kHz	0.79	5.01	21.12	32.57	
		32.768 kHz	0.79	5.00	21.10	32.54	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL, HXT, LXT or LIRC clock	144 MHz	30.30	35.29	52.18	63.81	
		120 MHz	25.89	30.77	47.57	59.22	
		96 MHz	21.40	26.14	42.87	54.48	
		84 MHz	18.95	23.63	40.29	51.87	
		72 MHz	17.03	21.63	38.30	49.90	

		60 MHz	17.02	21.62	38.25	49.86	
		50 MHz	14.48	19.01	35.57	47.15	
		48 MHz	13.50	18.00	34.50	46.02	
		32 MHz	16.44	21.52	37.10	48.57	
		24 MHz	8.09	12.46	28.81	40.32	
		12 MHz	5.20	9.51	25.77	37.24	
		6 MHz	3.75	8.03	24.25	35.72	
		3 MHz	3.03	7.30	23.50	34.97	
		38.4 kHz	0.80	5.04	21.14	32.58	
		32.768 kHz	0.80	5.03	21.17	32.61	

Note:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
		V_{DD}	5	5.5	5.5	5.5	V
I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, PLL, HXT, LXT or LIRC clock	144 MHz	6.04	10.31	26.57	38.06	mA
		120 MHz	5.26	9.51	25.76	37.22	
		96 MHz	4.49	8.73	24.94	36.42	
		84 MHz	4.11	8.34	24.53	36.01	
		72 MHz	3.94	8.17	24.37	35.88	
		60 MHz	3.51	7.73	23.91	35.41	
		50 MHz	3.15	7.37	23.54	34.99	
		48 MHz	2.38	6.60	22.69	34.14	
		32 MHz	8.60	13.46	28.68	40.08	
		24 MHz	1.75	5.95	22.02	33.47	
		12 MHz	1.43	5.62	21.70	33.11	
		6 MHz	1.26	5.46	21.51	32.92	
		3 MHz	1.18	5.37	21.44	32.84	
		38.4 kHz	0.79	4.98	21.03	32.44	
		32.768 kHz	0.79	4.98	21.02	32.45	
		144 MHz	23.83	28.56	45.21	56.75	

	Idle mode, all peripherals enable HIRC, PLL, HXT, LXT or LIRC clock	120 MHz	20.16	24.78	41.37	52.92	
		96 MHz	16.48	21.00	37.51	49.06	
		84 MHz	14.64	19.11	35.58	47.13	
		72 MHz	13.01	17.44	33.89	45.45	
		60 MHz	13.68	18.12	34.59	46.11	
		50 MHz	11.68	16.07	32.49	44.02	
		48 MHz	10.55	14.92	31.26	42.74	
		32 MHz	14.46	19.44	34.86	46.30	
		24 MHz	6.43	10.73	26.95	38.40	
		12 MHz	4.35	8.61	24.78	36.21	
		6 MHz	3.32	7.56	23.69	35.12	
		3 MHz	2.80	7.03	23.15	34.59	
		38.4 kHz	0.80	5.01	21.07	32.51	
		32.768 kHz	0.79	5.01	21.09	32.51	

Note:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	Power Level	LXT[1] 32.768 kHz	LIRC 38.4 kHz	Typ[2]				Max[3][4]				Unit
					T_A= 25 °C				T_A = 25 °C	T_A = 55 °C	T_A = 85 °C	T_A = 105 °C	
					2.7 V	3.3 V	5.0 V	5.5 V	5.5 V	5.5 V	5.5 V	5.5 V	
I_{DD_SPD1}	SPD1 mode, all peripherals disable without SRAM retention	-	-	-	22	22	23	24	69	151	328	543	μA
	SPD1 mode, all peripherals disable with 64KB SRAM retention	-	-	-	23	23	24	25	72	157	347	585	
	SPD1 mode, all peripherals disable with 128KB SRAM retention	-	-	-	24	24	25	26	74	163	364	623	
	SPD1 mode without SRAM retention, RTC enable and run	-	V	-	24	24	26	27	73	155	333	552	
	SPD1 mode without SRAM retention, wake-up timer enable and run	-	-	V	23	23	25	26	71	154	332	551	
I_{DD_SPD0}	SPD0 mode, all peripherals disable without SRAM retention	-	-	-	29	29	30	30	121	260	536	855	μA
	SPD0 mode, all peripherals disable with 64KB SRAM retention	-	-	-	31	31	32	33	125	270	563	908	
	SPD0 mode, all peripherals disable with 128KB SRAM retention	-	-	-	33	34	34	35	129	279	586	960	
	SPD0 mode without SRAM retention, RTC enable and run	-	V	-	31	31	32	33	123	264	540	859	
	SPD0 mode without SRAM retention, wake-up timer enable and run	-	-	V	30	30	31	31	122	263	539	859	
I_{DD_NPD2}	NPD2 mode, all peripherals disable	-	-	-	218	218	219	221	1784	4286	9180	14740	μA
	NPD2 mode, WDT/Timer/UART/RTC enable and run	-	V	-	221	221	223	224	1789	4297	9196	14749	

	NPD2 mode, WDT/Timer/RTC enable and run	-	-	V	219	219	221	223	1786	4295	9193	14753	
	NPD2 mode, WDT/Timer use LIRC, UART/RTC use LXT	-	V	V	222	222	224	226	1791	4300	9200	14762	
I_{DD_NPD1}	NPD1 mode, all peripherals disable	-	-	-	391	392	393	395	3469	7846	15901	24683	μA
	NPD1 mode, all peripherals disable, LVR disable	-	-	-	390	391	392	395	3465	7841	15906	24706	
	NPD1 mode, RTC enable and run	-	V	-	393	394	396	398	3471	7846	15910	24698	
	NPD1 mode, WDT/Timer/UART/RTC enable and run	-	V	-	395	395	397	399	3475	7862	15920	24718	
	NPD1 mode, WDT/Timer/RTC enable and run	-	-	V	393	393	395	397	3471	7860	15916	24691	
	NPD1 mode, WDT/Timer use LIRC, UART/RTC use LXT	-	V	V	395	396	398	401	3478	7871	15942	24715	
I_{DD_NPD0}	NPD0 mode, all peripherals disable	-	-	-	590	593	599	603	4727	10277	20209	31015	μA
	NPD0 mode, WDT/Timer/UART/RTC enable and run	-	V	-	594	596	602	607	4733	10294	20232	31038	
	NPD0 mode, WDT/Timer/RTC enable and run	-	-	V	593	595	601	606	4734	10312	20227	31049	
	NPD0 mode, WDT/Timer use LIRC, UART/RTC use LXT	-	V	V	596	598	604	609	4746	10321	20248	31048	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L3 gain level.
2. LVR enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
5. ~~5.~~ Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

Symbol	Test Conditions	Typ[1]				Max[2]				Unit
		25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD_SRAM}	SRAM0 64 KB static consumption	2.4	4.6	11.4	22.9	4.2	9.8	27.4	54.2	µA
	SRAM1 128 KB static consumption	4.7	8.9	21.7	43.2	8.0	18.5	51.0	105.5	

Note:

1. Tested in SPD0 mode.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-4 SRAM Static Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{BAT} = 5 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 144 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[1]	Unit
PDMA0	269	uA
ISP	1	
EBI	80	
ST	111	
CRC	27	
CANFD0	692	
CANFD1	713	
CRPT	213	
DFMC	98	
FMCIDLE	91	
USBH[4]	677	
CANRAM0	27	
CANRAM1	26	
TRACE	1	
GPA	18	
GPB	17	
GPC	15	
GPD	16	
GPE	15	
GPF	16	
GPG	17	
GPH	15	
WDT0	124	
RTC	34	
TMR0	206	
TMR1	210	
TMR2	151	

TMR3	155	
CLKO	367	
ACMP01[3]	117	
I2C0	68	
I2C1	40	
I2C2	67	
I3C0	1240	
QSPI0	470	
SPI0	420	
SPI1	452	
UART0	567	
UART1	513	
UART2	531	
UART3	466	
UART4	504	
UART5	465	
UART8	491	
UART9	451	
WWDT0	119	
WWDT1	120	
USBD[4]	603	
EADC0[2]	697	
WDT1	119	
USCI0	68	
USCI1	40	
DAC[5]	27	
PWM0	133	
PWM1	88	
BPWM0	101	
BPWM1	58	
EQEI0	57	
EQEI1	30	
UART6	497	
UART7	466	

ECAP0	60	
ECAP1	576	
LLSI0	104	
LLSI1	77	
LLSI2	105	
LLSI3	74	
LLSI4	99	
LLSI5	72	
LLSI6	101	
LLSI7	74	
LLSI8	101	
LLSI9	74	
LLSI10	118	
LLSI11	84	
TRNG	36	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 8.3-5 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode	0.53	0.54	µS
t_{WU_SPD1}[1][2]	Wakeup from SPD1 mode	249.25	259.10	
t_{WU_SPD0}[1][2]	Wakeup from SPD0 mode	258.79	266.45	
t_{WU_NPD2}[1][2]	Wakeup from NPD2 mode running in Flash	60.42	65.52	
	Wakeup from NPD2 mode running in RAM	58.95	64.10	
t_{WU_NPD1}[1][2]	Wakeup from NPD1 mode running in Flash	61.28	69.94	
	Wakeup from NPD1 mode running in RAM	56.78	59.06	
t_{WU_NPD0}[1][2]	Wakeup from NPD0 mode running in Flash	11.51	11.53	
	Wakeup from NPD0 mode running in RAM	11.52	11.54	
t_{ET_IDLE}[1]	Enter to IDLE mode	N/A	-	
t_{ET_SPD1}[1]	Enter to SPD1 mode	0.51	0.52	
t_{ET_SPD0}[1]	Enter to SPD0 mode	0.52	0.53	
t_{ET_NPD2}[1]	Enter to NPD2 mode	0.45	0.46	
t_{ET_NPD1}[1]	Enter to NPD1 mode	0.46	0.47	
t_{ET_NPD0}[1]	Enter to NPD0 mode	0.21	0.22	

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-6 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PA8~11, PB0~15, PC13~14, PD10~12, PD14, PE0~1 and PH8~11 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-7 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.4		V_{DDIO} = 1.62 V[3]
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2.0	-	V_{DD}		V_{DD} = 5.5 V
		2.0	-	V_{DD}		V_{DD} = 3.6 V
		1.0	-	V_{DD}		V_{DDIO} = 1.62 V[3]
V_{HY}[1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[2]	Input leakage current	-1	-	1	μA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
R_{PU}[1]	Pull up resistor	40	48	59	kΩ	V_{DD} = 2.7 V ~ 5.5V, V_{DDIO} = 1.7 V ~ 5.5V
R_{PU}[1] [4]	Pull up resistor	1.8	2	2.2	kΩ	
R_{PD}[1]	Pull down resistor	40	48	59	kΩ	

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. V_{DDIO} domain I/O (PA0~5) only.
4. I3C SDL and SCL multi-function pins only.

Table 8.3-8 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2] [3]	Source current for quasi-bidirectional mode and high level	-9.8	-8.3	-6.7	μA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-9.8	-8.3	-6.6	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-6.75	-5.4	-4.5	μA	V_{DDIO} = 1.98 V[6] V_{IN}=(V_{DDIO}-0.27) V
		-6.75	-5.2	-4.5	μA	V_{DDIO} = 1.62 V[6] V_{IN}=(V_{DDIO}-0.27) V
	Source current for push-pull mode and high level	-14.5	-11.4	-6.5	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-10.6	-8.3	-5.5	mA	V_{DD} = 4.5 V[7] V_{IN}=(V_{DD}-0.4) V
		-9.5	-7.2	-4.5	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-6.8	-5.1	-3.4	mA	V_{DD} = 2.7 V[7] V_{IN}=(V_{DD}-0.4) V
		-9.1	-6.8	-3.2	mA	V_{DDIO} = 1.98 V[5] V_{IN}=(V_{DDIO}-0.27) V
		-6.5	-4.9	-2.4	mA	V_{DDIO} = 1.62 V[5] V_{IN}=(V_{DDIO}-0.27) V
		-5.1	-3.5	-2.3	mA	V_{DDIO} = 1.98 V[6] V_{IN}=(V_{DDIO}-0.27) V
		-3.6	-2.7	-1.8	mA	V_{DD} = 1.62 V[6] V_{IN}=(V_{DDIO}-0.27) V
I_{SK}[1] [2] [4]	Sink current for push-pull mode and low level	7.2	13.5	19.3	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		7.1	13.1	19.2	mA	V_{DD} = 4.5 V[7] V_{IN}= 0.4 V
		4.8	8.4	11.7	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V

		4.5	8	11.5	mA	V_{DD} = 2.7 V[7] V_{IN}= 0.4 V
		4.1	7.2	10.0	mA	V_{DDIO} = 1.98 V[5] V_{IN}= 0.27 V
		3.2	5.4	7.2	mA	V_{DDIO} = 1.62 V[5] V_{IN}= 0.27 V
		2.2	4.2	5.9	mA	V_{DDIO} = 1.98 V[6] V_{IN}= 0.27 V
		1.7	3	4.2	mA	V_{DDIO} = 1.62 V[6] V_{IN}= 0.27 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.
3. The range of output high level voltage (V_{OH}) is from V_{DD}-0.4 to V_{DD} based on minimum value of source current (I_{SR}).
4. The range of output low level voltage (V_{OL}) is from 0 to 0.4 based on minimum value of sink current (I_{SK}).
5. VDDIO domain IO only. The current be tested under the condition of PA0/1/4/5 additional PMOS/NMOS bit = 1. Please refer to SYS_I3C0PADCTL register
6. VDDIO domain IO(PA0~5) only
7. PF4 and PF5 only.

Table 8.3-9 I/O Output Characteristics

8.3.5.3 PA0/1/4/5 additional PMOS/NMOS Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2] [3] [5]	Source current for push-pull mode and high level	-38.1	-21.4	-15.3	mA	V_{DD} = 4.5 V V_{IN}=(V_{DD}-0.4) V
		-24.3	-13.6	-9.0	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		-14.8	-8.2	-5.0	mA	V_{DDIO} = 1.8 V V_{IN}=(V_{DDIO}-0.4) V
		-13.7	-7.5	-4.5	mA	V_{DDIO} = 1.7 V V_{IN}=(V_{DDIO}-0.4) V
I_{SK}[1] [2] [4] [5]	Sink current for push-pull mode and low level	17.2	24.5	46.3	mA	V_{DD} = 4.5 V V_{IN}= 0.4 V
		9.9	14.9	26.8	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		5.4	8.4	15.0	mA	V_{DDIO} = 1.8 V V_{IN}= 0.4 V
		4.5	7.7	13.6	mA	V_{DDIO} = 1.7 V V_{IN}= 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the absolute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.
3. The range of output high level voltage (V_{OH}) is from V_{DD}-0.4 to V_{DD} based on minimum value of source current (I_{SR}).
4. The range of output low level voltage (V_{OL}) is from 0 to 0.4 based on minimum value of sink current (I_{SK}).
5. The current be tested under the condition of PA0/1/4/5 additional PMOS/NMOS bit = 1. Please refer to SYS_I3C0PADCTL register.

Table 8.3-10 PA0/1/4/5 Additional PMOS/NMOS Output Characteristics

8.3.5.4 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	41	48	59	kΩ	VDD=2.7~5.5V
t_{RP}[1]	Minimum nRESET pulse width	32.1	-	-	μS	Normal run and Idle mode
		32.2	-	-		NPD0 mode
		71.3	-	-		NPD1 mode
		71.1	-	-		NPD2 mode
		0.21	-	-		SPD0 mode
		0.21	-	-		SPD1 mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-11 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	2.7	-	5.5	V	
f_{HIRC}	Oscillator frequency	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[1]	-	-2[1]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.7 ~ 5.5V
I_{HIRC}[1]	Operating current	-	500	-	μA	
T_S[2]	Stable time	-	5	-	μS	T_A = -40°C ~ +105 °C, V_{DD} = 2.7 ~ 5.5V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator (HIRC) Characteristics

8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operating voltage	2.7	-	5.5	V	
F_{LIRC} [2]	Oscillator frequency	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-3	-	3	%	T_A=-40~105°C V_{DD}=2.7V~5.5V Without software calibration
I_{LIRC}	Operating current	-	1	2	μA	V_{DD} = 3.3V
T_S [3]	Stable time	-	150	-	μS	T_A=-40~105°C V_{DD}=1.75V~5.5V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design, not tested in production.

Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator (LIRC) Characteristics

8.4.3 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.7	-	5.5	V	
R_f	Internal feedback resister	-	0.2	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT}	Current consumption	-	350	-	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	400	-		8 MHz, Gain = L1, C_L = 12.5 pF
		-	650	-		12 MHz, Gain = L2, C_L = 12.5 pF
		-	950	-		16 MHz, Gain = L3, C_L = 12.5 pF
		-	3200	-		24 MHz, Gain = L4, C_L = 12.5 pF
		-	3500	-		32 MHz, Gain = L5, C_L = 12.5 pF
T_S	Stable time	-	3500	-	μS	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3500	-		8 MHz, Gain = L1, C_L = 12.5 pF
		-	3000	-		12 MHz, Gain = L2, C_L = 12.5 pF
		-	2450	-		16 MHz, Gain = L3, C_L = 12.5 pF
		-	1720	-		24 MHz, Gain = L4, C_L = 12.5 pF
		-	750	-		32 MHz, Gain = L5, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
Rs	Equivalent series resistor (ESR)	-	-	150	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	80		Crystal @8 MHz, C_L = 12.5 pF, Gain = L1
		-	-	120		Crystal @12 MHz, C_L = 12.5 pF, Gain = L2
		-	-	100		Crystal @16 MHz, C_L = 12.5 pF, Gain = L3
		-	-	80		Crystal @24 MHz, C_L = 12.5 pF, Gain = L4
		-	-	50		Crystal @32 MHz, C_L = 12.5 pF, Gain = L5

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass production.

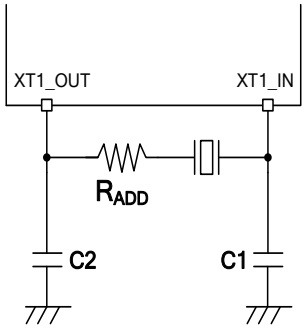


Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics

8.4.3.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 20 pF	10 ~ 20 pF	without

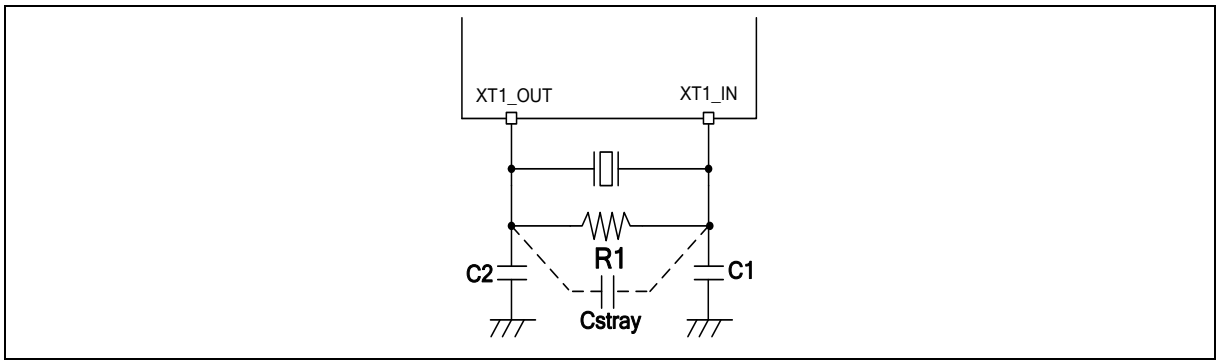
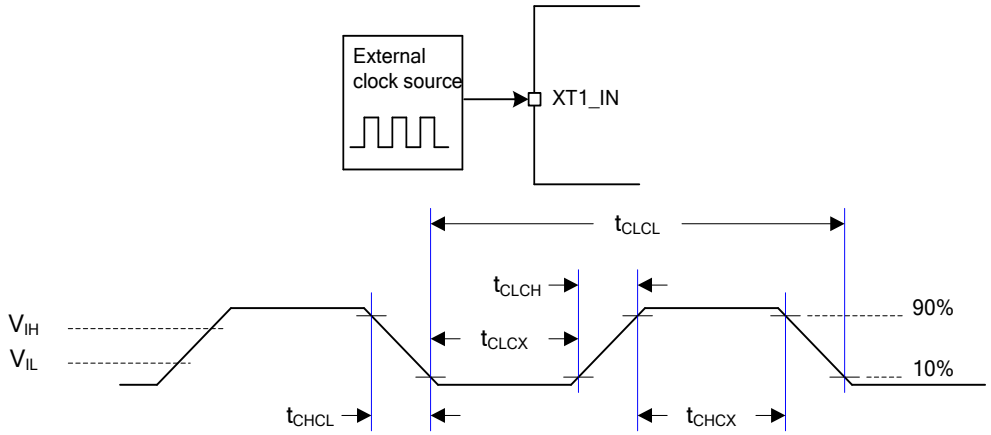


Figure 8.4-1 Typical Crystal Application Circuit

8.4.4 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The XT1_IN is set as schmitt trigger input mode.
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The XT1_IN is set as schmitt trigger input mode.



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~32 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.7	5	5.5	V	
R_f	Internal feedback resistor	-	12	-	MΩ	
F_{LXT}	Oscillator frequency	32.768			kHz	
I_{LXT}	Current consumption	370	852	1800	nA	ESR=50 kΩ, C_L = 6 pF, Gain = L0
		670	1255	2600		ESR=50 kΩ, C_L = 12.5 pF, Gain = L1
		970	1896	3500		ESR=70 kΩ, C_L = 12.5 pF, Gain = L2
		1300	2586	4400		ESR=90 kΩ, C_L = 12.5 pF, Gain = L3
Ts_{LXT}	Stable time	-	1	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.3	-	-	V	

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (Sf) must be higher than 5 for LXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the LXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass production.

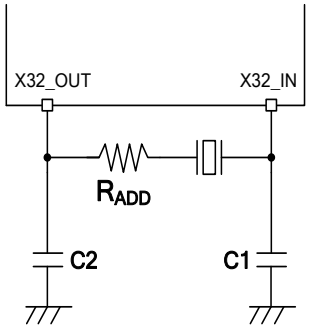


Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalent Series Resistor (ESR)	-	50	90	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.2 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 5 pF ~ 20 pF range, designed for RTC applications, and selected to match the requirements of the crystal. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 90 KΩ	7 ~ 20 pF	7 ~ 20 pF	without

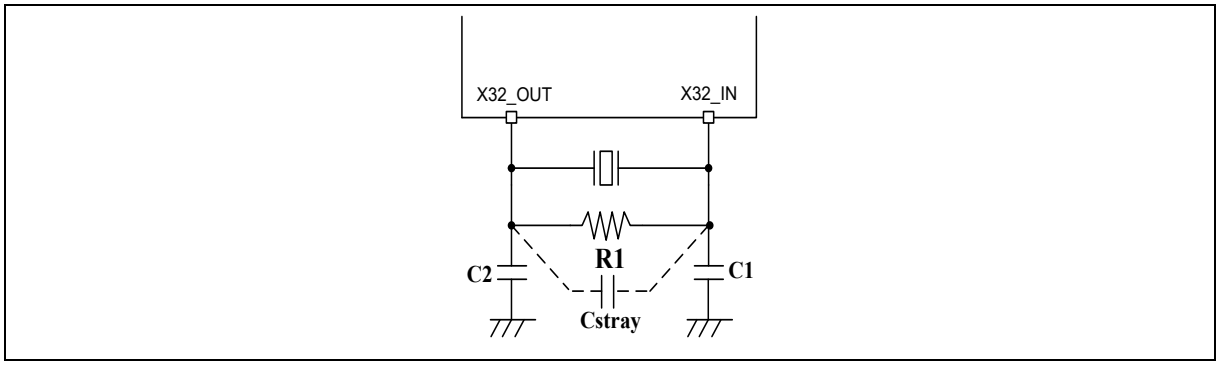
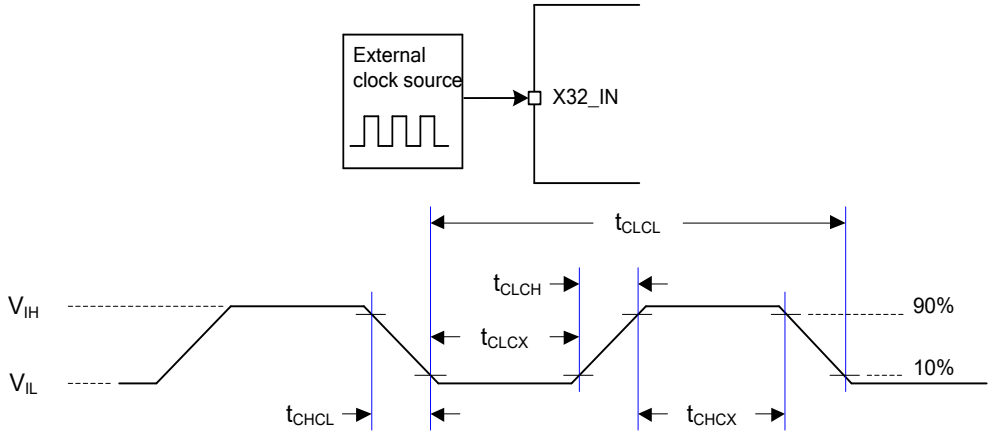


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
V_{IH}	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The X32_IN is set as schmitt trigger input mode.
V_{IL}	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The X32_IN is set as schmitt trigger input mode.



Note:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{PLL_in}	PLL input clock	1	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	36	-	144	MHz	
f_{PLL_REF}	PLL reference clock	1	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	120	-	320	MHz	
T_L	PLL locking time	-	-	600	μS	
Jitter[2]	Cycle-to-cycle Jitter	-	300	700	pS	
I_{DD}	Power consumption	-	1.4	2.5	mA	f_{PLL_VCO} = 144 MHz

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-9 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[1].	Unit	Test Conditions[2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	7.5	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	12.1		C_L = 30 pF, V_{DD} >= 2.7 V
		-	7.4		C_L = 10 pF, V_{DD} >= 2.7 V
		-	22.7		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	14.4		C_L = 10 pF, V_{DDIO} >= 1.7 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	6.2		C_L = 30 pF, V_{DD} >= 4.5 V
		-	3.3		C_L = 10 pF, V_{DD} >= 4.5 V
		-	9.6		C_L = 30 pF, V_{DD} >= 2.7 V
		-	5.3		C_L = 10 pF, V_{DD} >= 2.7 V
		-	17.3		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	9.5		C_L = 10 pF, V_{DDIO} >= 1.7 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	8.0	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	5.0		C_L = 10 pF, V_{DD} >= 4.5 V
		-	13.5		C_L = 30 pF, V_{DD} >= 2.7 V
		-	8.5		C_L = 10 pF, V_{DD} >= 2.7 V
		-	25.8		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	16.4		C_L = 10 pF, V_{DDIO} >= 1.7 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	6.1		C_L = 30 pF, V_{DD} >= 4.5 V
		-	3.4		C_L = 10 pF, V_{DD} >= 4.5 V
		-	10.1		C_L = 30 pF, V_{DD} >= 2.7 V
		-	5.6		C_L = 10 pF, V_{DD} >= 2.7 V
		-	18.5		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	10.4		C_L = 10 pF, V_{DDIO} >= 1.7 V
$f_{max(IO)out}$[3]	I/O maximum frequency	-	32.26	MHz	C_L = 30 pF, V_{DD} >= 4.5 V

	(Normal Slew Rate)	-	52.63		C_L = 10 pF, V_{DD} >= 4.5 V
		-	19.53		C_L = 30 pF, V_{DD} >= 2.7 V
		-	31.45		C_L = 10 pF, V_{DD} >= 2.7 V
		-	10.31		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	16.23		C_L = 10 pF, V_{DDIO} >= 1.7 V
	I/O maximum frequency (High Slew Rate)	-	40.65	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	74.63		C_L = 10 pF, V_{DD} >= 4.5 V
		-	25.38		C_L = 30 pF, V_{DD} >= 2.7 V
		-	45.87		C_L = 10 pF, V_{DD} >= 2.7 V
		-	13.97		C_L = 30 pF, V_{DDIO} >= 1.7 V
		-	25.13		C_L = 10 pF, V_{DDIO} >= 1.7 V
I_{DIO}[4]	I/O dynamic current consumption	1.39	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 12 MHz
		0.59	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 12 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. Maximum output frequency is achieved if ((TR + TF) ≤ 1/2) T and if the duty cycle is (45%-55%) when loaded by the specified capacitance but the maximum system frequency is limited to CPU.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
V_{DD}	Power supply	2.7	-	5.5	V	
V_{LDO}	Output voltage	-	1.18	-	V	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a C_{LDO} capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.
3. V_{LDO} is only used to supply internal power.

Table 8.5-1 LDO Characteristics

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
I_{POR}[1]	POR operating current	-	-	20	μA	V_{DD} = AV_{DD} = Max. OP
I_{LVR}[1]	LVR operating current	-	-	4.5		V_{DD} = AV_{DD} = Max. OP
I_{BOD}[1]	BOD operating current	-	-	15		V_{DD} = AV_{DD} = Max. OP, Normal mode
		-	-	1.5		V_{DD} = AV_{DD} = Max. OP Low Power mode
V_{POR_R}	POR reset voltage (Rising edge)	2.3	2.5	2.7	V	
V_{POR_F}	POR reset voltage (Falling edge)	2.2	2.4	2.6		
V_{LVR_R}	LVR reset voltage (Rising edge)	2.5	2.6	2.7		
V_{LVR_F}	LVR reset voltage (Falling edge)	2.45	2.55	2.65		
V_{BOD_R}	BOD brown-out detect voltage (Rising edge)	2.78	2.88	3.0		BODVL = 0xB
		3.66	3.76	3.88		BODVL = 0xD
		4.37	4.47	4.59		BODVL = 0xF
V_{BOD_F}	BOD brown-out detect voltage (Falling edge)	2.68	2.80	2.92		BODVL = 0xB
		3.58	3.70	3.82		BODVL = 0xD
		4.28	4.40	4.52		BODVL = 0xF
T_{LVR_SU}[1]	LVR startup time	-	-	2500	μS	-
T_{LVR_RE}[1]	LVR respond time	-	30	100		LVRDGSEL = 0

T_{BOD_SU}[1]	BOD startup time	-	-	300		Normal mode, LVR ON BODDGSEL = 3
		-	-	400		Low Power mode, LVR ON BODDGSEL = 3
T_{BOD_RE}[1]	BOD respond time	-	-	10		Normal mode BODDGSEL = 3
		-	-	4000		Low Power mode BODDGSEL = 3
R_{VDDR}[1]	VDD rise time rate	10	-	-	μS/V	POR Enabled
R_{VDDF}[1]	VDD fall time rate	50	-	-		POR Enabled
		500	-	-		LVR Enabled
		22.2	-	-		BOD 2.8V Enabled, Normal mode
		7.4	-	-		BOD 3.7V Enabled, Normal mode
		4.88	-	-		BOD 4.4V Enabled, Normal mode
		8888.88	-	-		BOD 2.8V Enabled, Low Power mode
		2962.96	-	-		BOD 3.7V Enabled, Low Power mode
		1951.22	-	-		BOD 4.4V Enabled, Low Power mode

Note:

1. Guaranteed by characterization, not tested in production.
2. Designd for specified application.

Table 8.5-2 Reset and Power Control Unit

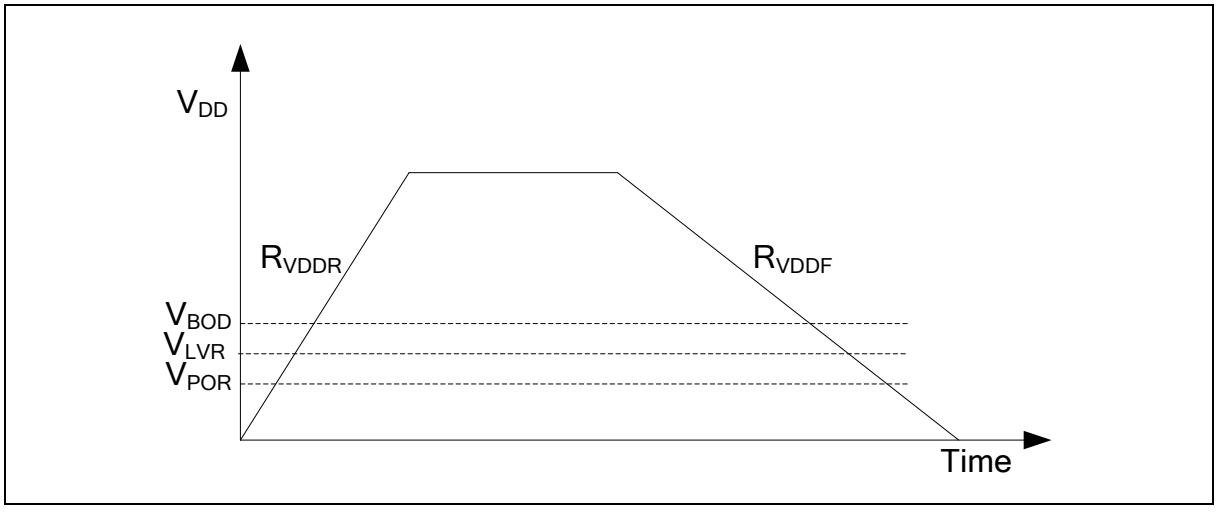


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.0	-	AV_{DD}	V	3V <AV_{DD} < 5.5 V
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	3V <AV_{DD} < 5.5 V
I_{ADC}[1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	201	350	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = Max. 36 MHz F_{SPS} = Max. 1710 * kSPS
		-	136	200	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = Min. 12 MHz F_{SPS} = Min. 571 * kSPS
N_R	Resolution	12			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	12	-	36	MHz	
T_{SMP}[1]	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	21	-	276	$1/F_{ADC}$	$T_{CONV} = T_{SMP}$ + 20 * T_{ADC}
F_{SPS}[1]	Sampling Rate	571	-	1710	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}[1]	Enable to ready time	5	-	-	$1/F_{ADC}$	
INL[1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD.}$
DNL[1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD.}$
E_G[1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD.}$
E_O[1]	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD.}$
E_A[1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD.}$
ENOB[1]	Effective number of bits	-	10.8	-	bits	F_{ADC} = Max. 25MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SNR[1]	Signal-to-noise ratio	-	66.74	-	dB	
C_{IN}[2]	Internal Capacitance	-	4	-	pF	
R_{IN}[2]	Internal Switch Resistance	-	-	2100	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{EX}	External input impedance at room temperature [1] [3]	0.39	-	0.5	kΩ	F_{ADC} = max. 36MHz Tconv = T_{SMP+} 21 * T_{ADC} C_{EX} = C_{IO} = 5 pF T_J = 25 °C

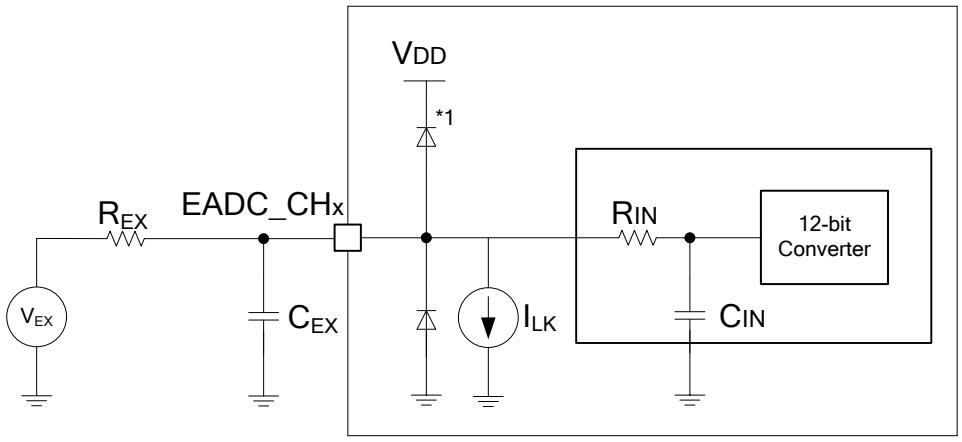
Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.
3. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

4. The signal voltage is affected by I/O leakage and internal ADC leakage. When ADC is running at high temperature, the R_{EX} should be lower to decrease IR voltage drop effect.

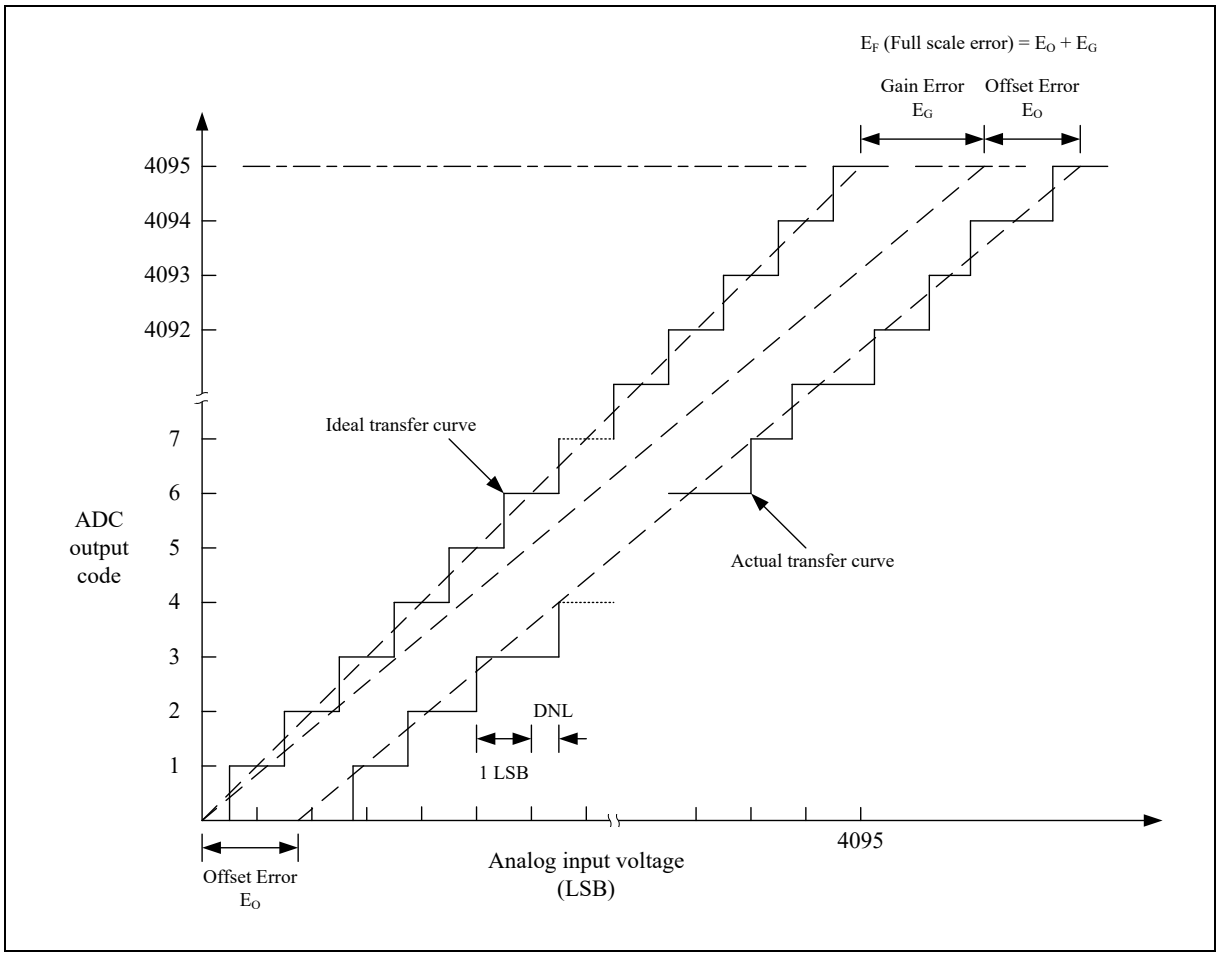
Table 8.5-3 ADC Characteristics



Note:

1. The internal ESD diode is not supported between I/O and V_{DD} at 5V tolerence I/O pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 14-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.0	-	AV_{DD}	V	3V <AV_{DD} < 5.5 V
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	-196	350	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = Max. 25 MHz F_{SPS} = Max. 1710 * kSPS
		-	-	280	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5 V F_{ADC} = Min. 12 MHz F_{SPS} = Min. 571 * kSPS
N_R	Resolution	14			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	12	-	20	MHz	
T_{SMP}[1]	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	24	-	279	$1/F_{ADC}$	$T_{CONV} = T_{SMP}$ + 23 * T_{ADC}
F_{SPS}[1]	Sampling Rate	480	-	1000	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}[1]	Enable to ready time	5	-	-	$1/F_{ADC}$	
INL[1]	Integral Non-Linearity Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
DNL[1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$
E_G[1]	Gain error	-6	-	+6	LSB	$V_{REF} = AV_{DD}$
E_O[1]	Offset error	-6	-	+6	LSB	$V_{REF} = AV_{DD}$
E_A[1]	Absolute Error	-14	-	+14	LSB	$V_{REF} = AV_{DD}$
ENOB[1]	Effective number of bits	-	11.8	-	bits	F_{ADC} = Max. 25MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SNR[1]	Signal-to-noise ratio	-	72	-	dB	
C_{IN}[2]	Internal Capacitance	-	9	-	pF	
R_{IN}[2]	Internal Switch Resistance	-	-	1500	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
R_{EX}	External input impedance at room temperature [1] [3]	-	-	0.5	kΩ	F_{ADC} = max. MHz T_{SMP} = max. * T_{ADC} C_{EX} = C_{IO} = 5 pF T_J = 25 °C

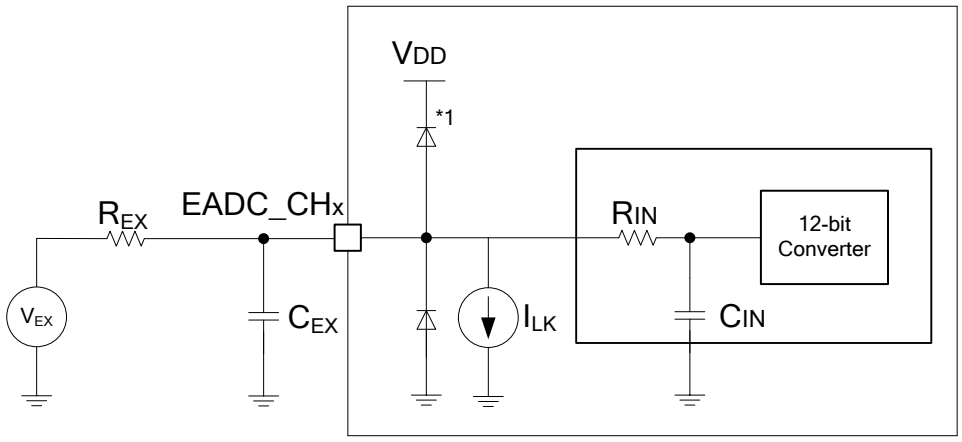
Note:

5. Guaranteed by characterization result, not tested in production.
6. Guaranteed by design, not tested in production.
7. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

8. The signal voltage is affected by I/O leakage and internal ADC leakage. When ADC is running at high temperature, the R_{EX} should be lower to decrease IR voltage drop effect.

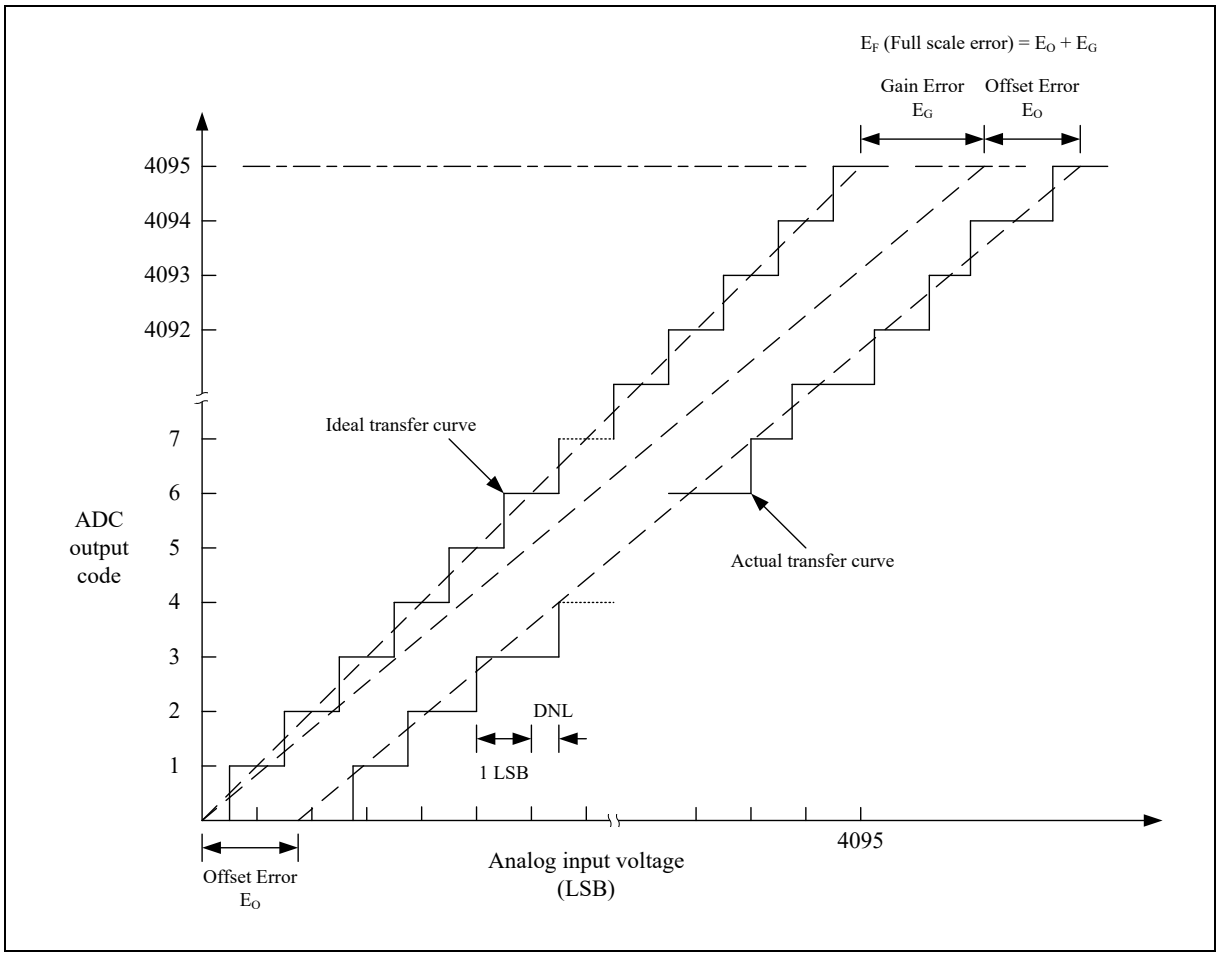
Table 8.5-4 ADC Characteristics



Note:

1. The internal ESD diode is not supported between I/O and V_{DD} at 5V tolerence I/O pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.5 Digital to Analog Converter (DAC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog supply voltage	2.7	-	5.5	V	
N_R	Resolution		12		bit	
V_{REF}	Reference supply voltage	1.6	-	AV_{DD}	V	
DNL[2]	Differential non-linearity error	-	-	±2	LSB	12-bit mode
INL[2]	Integral non-linearity error	-	-	±4	LSB	12-bit mode DACOUT buffer OFF
		-	-	±6	LSB	12-bit mode DACOUT buffer ON
OE[2]	Offset Error	-	-	±6	LSB	12-bit mode

						DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
GE[2]	Gain Error	-	-	±10	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
AE[2]	Absolute Error	-	-	±10	LSB	12-bit mode DACOUT buffer ON
		-	-	±4	LSB	12-bit mode DACOUT buffer OFF
-	Monotonic	10-bit guaranteed			-	-
V_O[1]	Output Voltage	0.2	-	AVDD-0.25	V	DACOUT buffer ON
		1*LSB	-	V_{REF} - 1*LSB	V	DACOUT buffer OFF
R_{LOAD}[2] [3]	Resistive load	3.1	-	-	kΩ	DACOUT buffer ON
R_O[2]	Output impedance	-	10	20	kΩ	DACOUT buffer OFF
C_{LOAD}[2] [4]	Capacitive load	-	-	20	pF	DACOUT Buffer OFF
		-	-	50	pF	DACOUT Buffer ON
I_{DAC_AVDD}[2]	DAC operating current on AV_{DD} supply	-	-	130 340	µA	AV_{DD} = 5.5 V, no load, lowest code (0x000) Buffer On
				340	µA	AV_{DD} = 5.5 V, no load, middle code (0x800) Buffer On
I_{DAC_VREF}[2]	DAC operating current on V_{REF} supply	-	-	1840	µA	V_{REF} = 5.5 V, no load, high code (0xFFF) Buffer On
T_B[2]	Settling Time	-	3	6	µS	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$
F_S	Update Rate	-	-	1000	kSPS	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$
T_{WAKEUP}	Wake-up Time	-	3	6	µS	Wakeup time from OFF state. Input code between lowest and highest possible codes. PCLK = 72 MHz
PSRR[1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

Table 8.5-5 DAC Characteristics

8.5.6 Analog Comparator (ACMP)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog supply voltage	2.7	-	5.5	V	$V_{DD} = AV_{DD}$
I_{ACMP}[2]	ACMP operating current	-	70	90	μA	MODESEL = 11
		-	35	70		MODESEL = 10
		-	6	10		MODESEL = 01
		-	3	5		MODESEL = 00
V_{CM}[2]	Input common mode voltage range	0	-	AVDD	V	
V_{offset}[2]	Input offset voltage	-	-	±10	mV	MODESEL = 11 Hysteresis disable (HYSSEL = 00)
			-	±20		MODESEL = 00~10 Hysteresis disable (HYSSEL = 00)
V_{hys}[2]	Hysteresis window	-	0	2	mV	HYSSEL = 000
		-	10	20		HYSSEL = 001
		-	20	40		HYSSEL = 010
A_v[1]	DC voltage Gain	43	70	-	dB	
T_d[2]	Propagation delay	-	30	90	nS	MODESEL = 11; 200 mV step, 100 mV overdrive
		-	100	150		MODESEL = 10
		-	0.8	2	μs	MODESEL = 01
		-	1.5	3.5		MODESEL = 00
T_{Setup}[2]	Setup time	-	-	3u	μs	MODESEL = 10~11
			-	30		MODESEL = 00~01
A_{CRV}[2]	CRV output voltage	-2	-	2	LSB	CRV0 source voltage * (CRV0SEL)/ 255.
R_{CRV}[2]	Unit resistor value	-	1.5	-	kΩ	
T_{SETUP_CRV}[2]	Setup time	-	-	4.5	μs	CRV output voltage settle to ±0.2%
I_{DD_CRV}[2]	Operating current	-	10	-	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-6 ACMP Characteristics

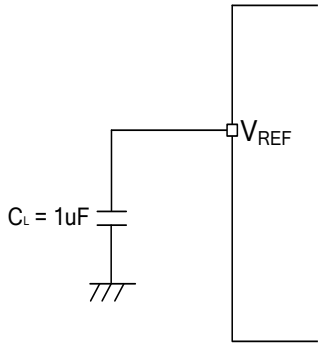
8.5.7 Internal Voltage Reference

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{REF_INT}	Internal reference voltage	2.540	2.560	2.580	V	AV_{DD} >= 2.9 V
		3.052	3.072	3.092		AV_{DD} >= 3.4 V
		4.076	4.096	4.116		AV_{DD} >= 4.5 V
T_s[1]	Stable time	-	-	1.6	ms	C_L = 2.2 uF, V_{REF} initial=0V, Preload is enabled.
		-	-	7	ms	C_L = 2.2 uF, V_{REF} initial= max.VDD V, Preload is enabled.
		-	-	4	ms	C_L = 4.7 uF, V_{REF} initial=0V, Preload is enabled.
		-	-	15	ms	C_L = 4.7 uF, V_{REF} initial=max.VDD V, Preload is enabled.
I_{VREF_INT}[1]	V_{REF_INT} operating current	-	-	250	uA	
I_{VREF_LOAD}[1]	V_{REF_INT} output loading current	-	-	18	mA	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.5-7 Internal V_{REF} Characteristics



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.8 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{TEMP_OS}[1]	Temperature sensor offset voltage	616	685	754	mV	Tj = 25°C
T_C[1]	Temperature Coefficient	|-1.56|	|-1.74|	|-1.9|	mV/°C	
T_S[2]	Stable time	-	-	5	µS	
T_{TEMP_ADC}[1]	ADC sampling time when reading the temperature	-	10	-	µS	
I_{TEMP}[1]	Temperature sensor operating current	-	5	8	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Table 8.5-8 Temperature Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specifications[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/T_{SPICLK}$	SPI clock frequency	-	-	36	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	36		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	36		1.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	1.2	-	-	nS	
t_{DH}	Data input hold time	0	-	-	nS	
t_V	Data output valid time	-	-	2.1	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	2.1	nS	2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	4.23	nS	1.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:
1. Guaranteed by design, not tested in production.

Table 8.6-1 SPI Master Mode Characteristics

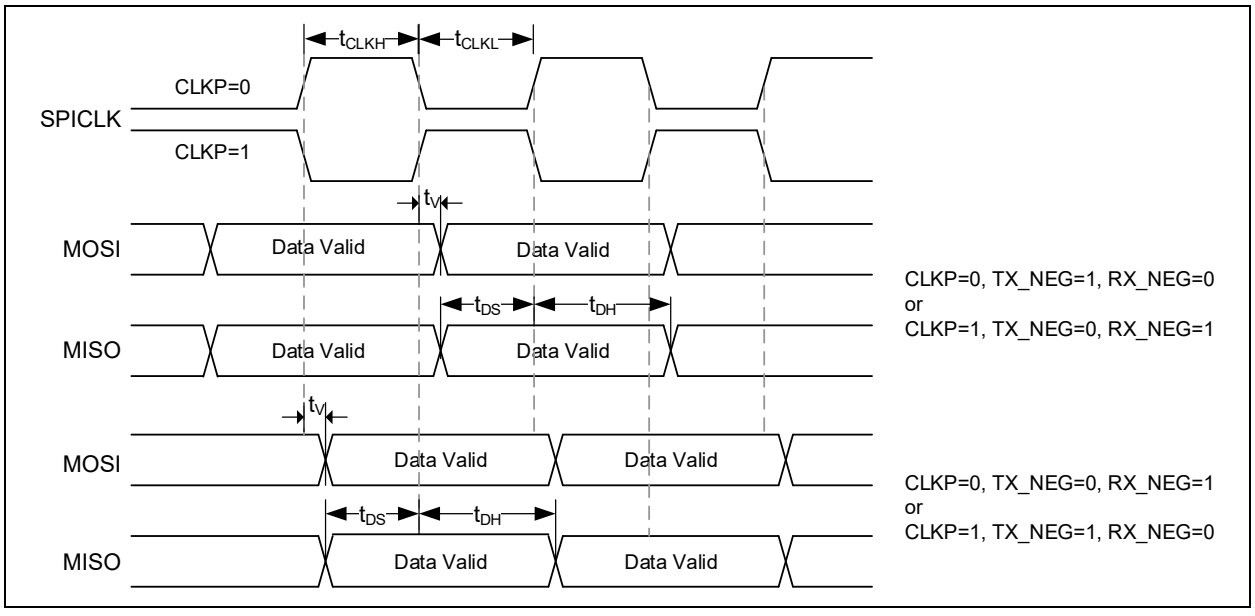


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[1]	Test Conditions

		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	20.5	MHz	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	13		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	7.87		1.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 4.5ns	-	-		1.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	3.7	-		nS	
t_V	Data output valid time	-	-	24.3	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	38.34		2.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	63.52		1.7 V ≤ VDD ≤ 5.5 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-2 SPI Slave Mode Characteristics

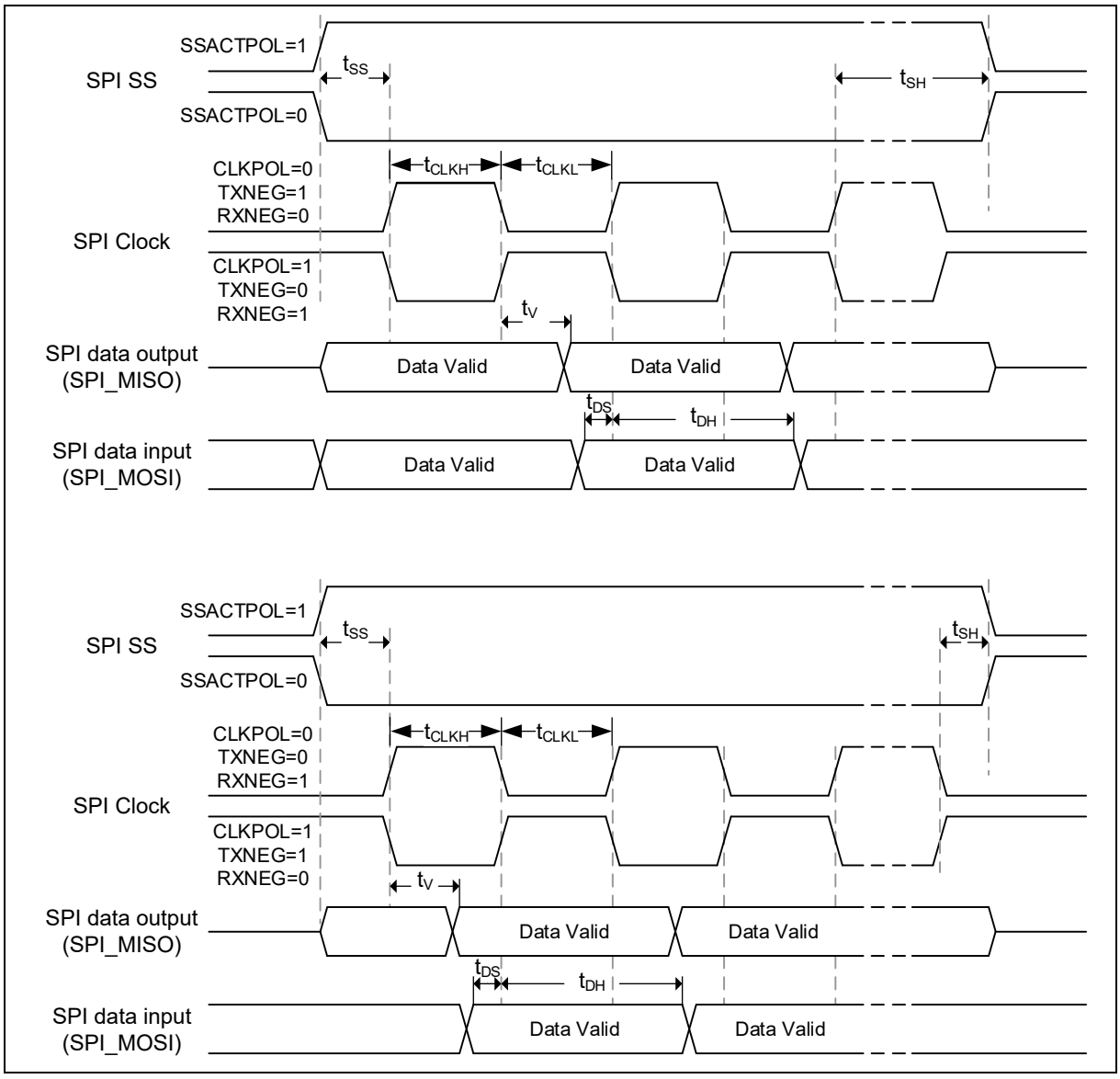


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [1]	Max [1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	69.4	-	nS	Master f_{PCLK} = 72 MHz, data: 24 bits, audio frequency = 150 kHz
$t_{w(CKL)}$	I²S clock low time	69.4	-		
$t_{v(LR)}$	LR valid time	-	3		Master mode
$t_{su(LR)}$	LR setup time	9	-		Slave mode
$t_{h(LR)}$	LR hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	40	60	%	Slave mode
$t_{su(SD_MR)}$	Data input setup time	35	-	nS	Master receiver
$t_{su(SD_SR)}$		5	-		Slave receiver
$t_{h(SD_MR)}$	Data input hold time	1	-		Master receiver
$t_{h(SD_SR)}$		2 T_{PCLK}	-		Slave receiver
$t_{v(SD_ST)}$	Data output valid time	-	41		Slave transmitter (after enable edge)
$t_{v(SD_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-3 I²S Characteristics

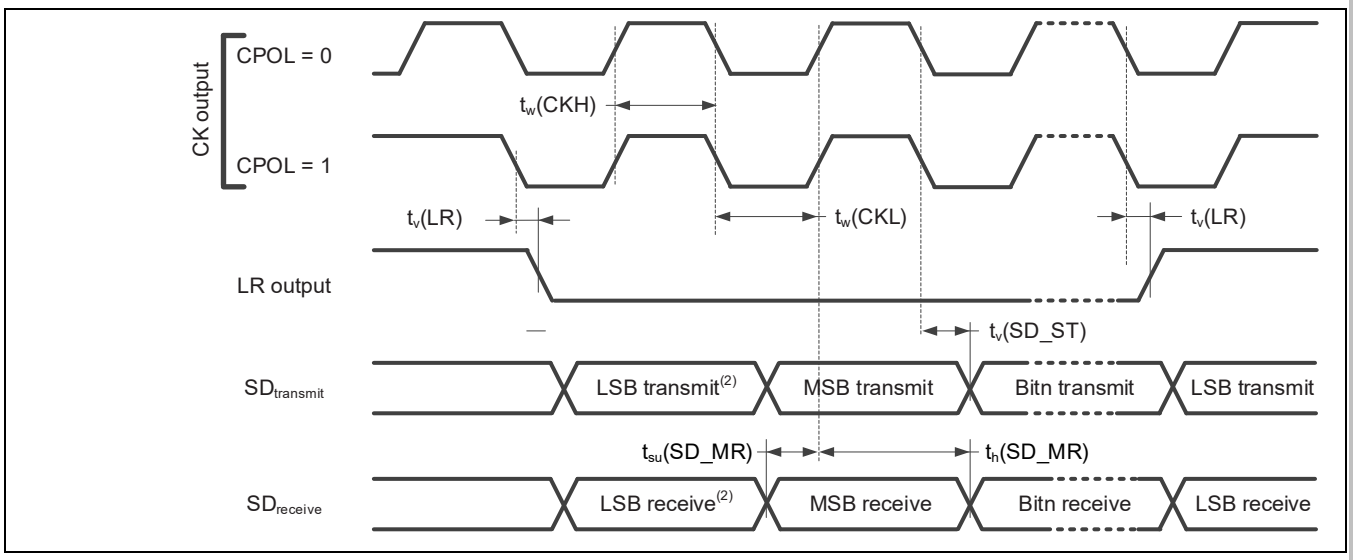


Figure 8.6-3 I²S Master Mode Timing Diagram

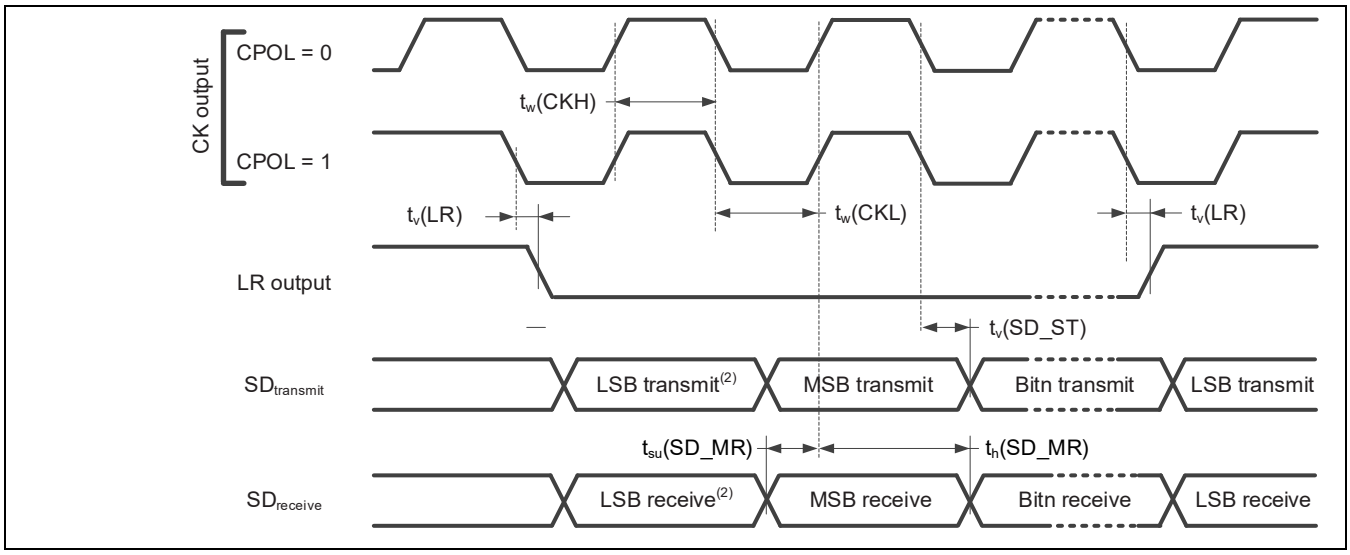


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

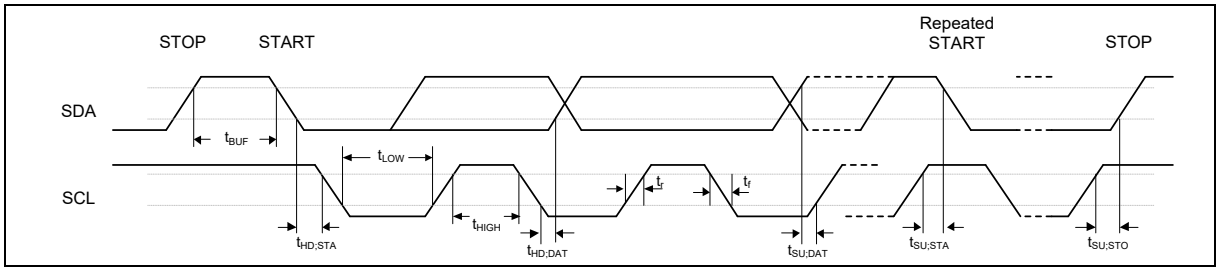


Figure 8.6-5 I²C Timing Diagram

8.6.4 I3C Dynamic Characteristics

Symbol	Parameter		I²C Mode		I3C Mode				Unit
			Open Drain		Open Drain		Push-Pull		
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock frequency		0.01	1	-	-	0.01	12.5[4][5]	MHz
t_{LOW}	SCL Clock Low Period		-	-	-	-	0.01	12.5[4][5]	nS
t_{HIGH}	SCL Clock High Period		-	-	-	-	0.01	10.3[4]/8.0[5]	nS
t_{cr}	SCL Clock Rise Time		500	-	-	-	32	-	nS
t_{cf}	SCL Clock Fall Time		260	-	-	-	32	-	nS
t_{SU_DAT}	Data setup time		-	120	-	-	-	5.5[4]/9.5[5]	nS
t_{HD_DAT}	Data hold time	-	120	-	-	-	5.5[4]/9.5[5]	-	nS
		50	-	3	-	3	-	-	
t_{SCO}	Clock in to Data Out for Slave		-	-	-	-	T_{I3CCLK}	7* T_{I3CCLK}	nS
t_{CAS}	Clock After START(S) Condition		-	-	-	-	0	-	S
t_{CBP}	Clock Before STOP(P) Condition		-	-	-	-	-	36[4]/58[5]	S
t_{CBSr}	Clock Before Repeated START (Sr) Condition		260 n	-	34.8 n	ENTAS0: 1 µ ENTAS1: 100 µ ENTAS2: 2 m ENTAS3: 50 m	19.2 n	-	nS
t_{BUF}	Time between Stop Condition and next Start Condition		260	-	19.2	-	19.2	-	nS
t_{AVAIL}	Bus Available Condition		-	-	-	-	19.2	-	µS
t_{IDLE}	Bus Idle Condition		500	-	500	-	-	-	µS

Note:

1. Guaranteed by characteristic, not tested in production.
2. I3C clock source must be greater than 125 MHz to achieve the maximum SCL Clock frequency.
3. Slave that do not support the optional ENTASx CCCs shall use the tCAS Max value *shown for ENTAS3*
4. Test condition: V_{DDIO}<2.7V, C_L=35pF and I^{3}C pad 3.3V configuration.
5. Test condition: V_{DDIO}<1.7V, C_L=35pF and I^{3}C pad 1.8V configuration.

Table 8.6-5 I3C Characteristics

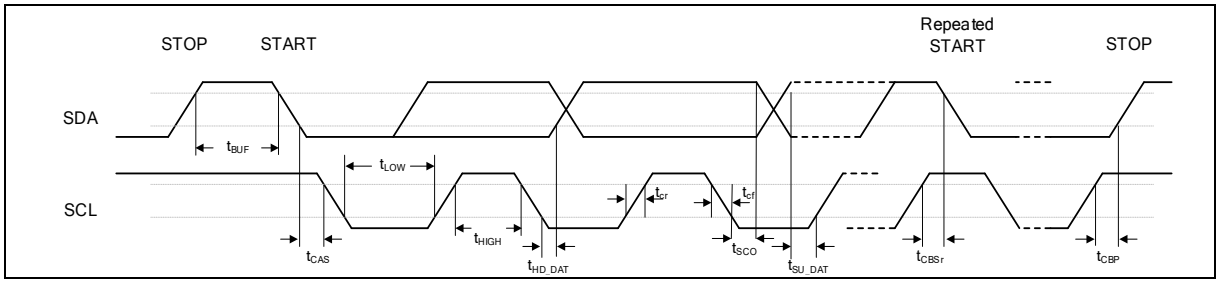


Figure 8.6-6 I3C Timing Diagram

8.6.5 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [1]	Typ	Max[1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	19.4	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	14.9		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2				
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2				
t_{DS}	Data input setup time	18.4	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		24.3	-	-		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{DH}	Data input hold time	0	-	-	nS	
t_V	Data output valid time	-	-	2.9	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	3.4	nS	2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-6 USCI-SPI Master Mode Characteristics

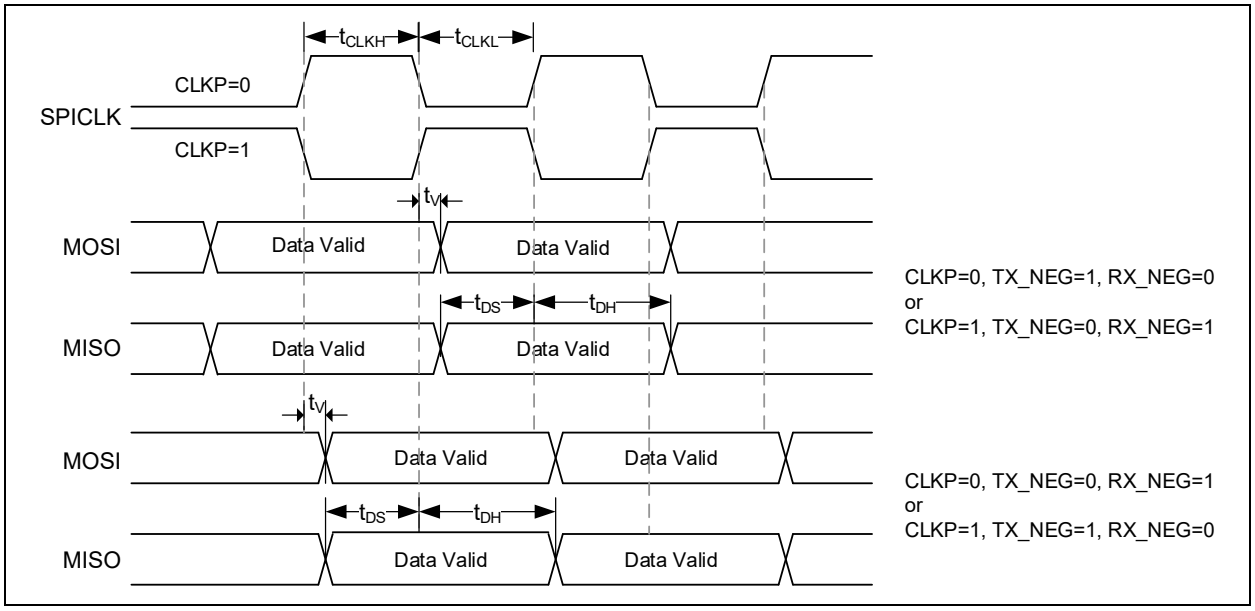


Figure 8.6-7 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	12.0	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	10.3		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2				
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2				
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 2	-	-		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2 T_{PCLK}	-	-	nS	
t_V	Data output valid time	-	-	41.4	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	48.4		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-7 USCI-SPI Slave Mode Characteristics

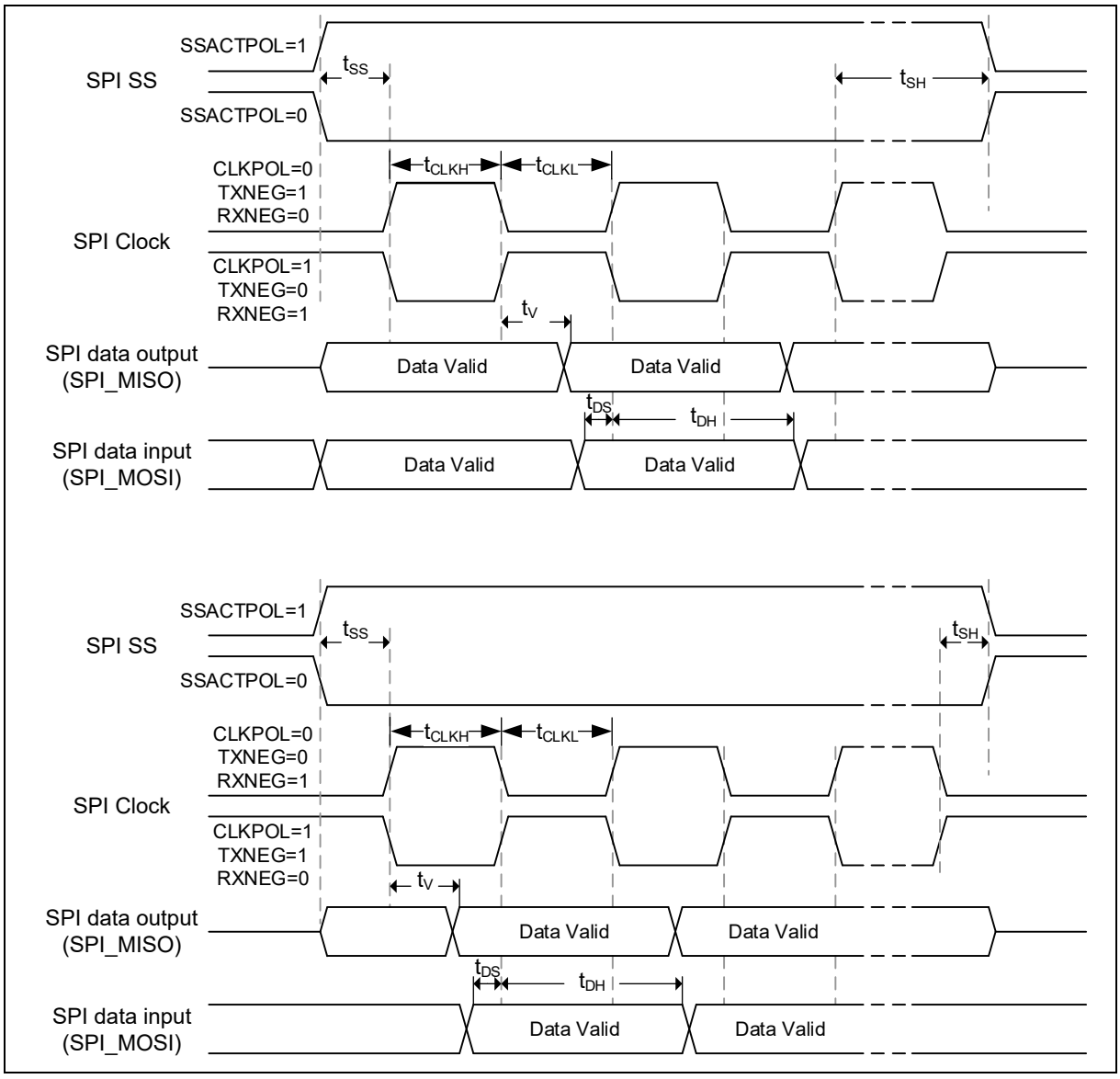


Figure 8.6-8 USCI-SPI Slave Mode Timing Diagram

8.6.6 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-8 USCI-I²C Characteristics

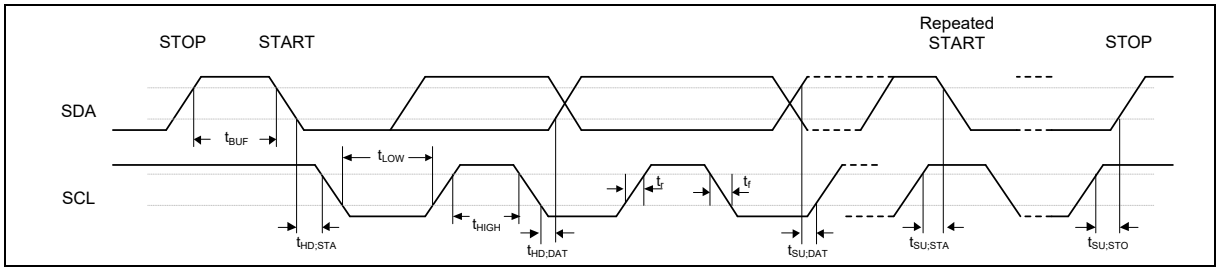


Figure 8.6-9 USCI-I²C Timing Diagram

8.6.7 CAN Characteristics

Symbol	Parameter	Min	Max [1]	Unit	Test Conditions
t_{CAN_TXD}	TXD output delay (Normal Slew Rate)	-	12.5	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	20		2.7 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CAN_RXD}	RXD input delay	-	2.8	nS	4.5 V ≤ VDD ≤ 5.5 V
		-	4.5		2.7 V ≤ VDD ≤ 5.5 V

Note:
1. Guaranteed by design, not tested in production.

Table 8.6-9 CAN Characteristics

8.6.8 USB Characteristics

8.6.8.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.7	-	5.5	V	
V_{BUS}	USB full speed transceiver operating voltage USB V_{BUS} voltage detection voltage	4.2	-	5.5	V	
V_{DD33}[2]	USB Internal power regulator output	3.0	3.3	3.6	V	
V_{IH}	Input high (driven)	2	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.1	0.2	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2	V	-
	Receiver hysteresis	150	200	350	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2	V	-
R_{PU}	Pull-up resistor	0.9	-	1.575	kΩ	-
R_{PD}	Pull-down resistor	14	-	25	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3	-	3.6	V	
Z_{DRV}[3]	Driver output resistance	8	8	25	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	50	pF	Pin to GND

Note:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 μF output capacitor, 1 uF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 43 Ω).

Table 8.6-10 USB Full-Speed Characteristics

8.6.8.2 USB Full-Speed PHY characteristics

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_{FR}	Rise time	4	-	20	nS	C_L=50 pF
T_{FF}	Fall time	4	-	20	nS	C_L=50 pF
T_{FRFF}	Rise and fall time matching	90	-	110	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-11 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[2]	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	14.5	-	ms+	T_A = 25℃
T_{PROG}	Program time	-	44	-	μS	
I_{DD1}	Read current	-	3.5	-	mA	
I_{DD2}	Program current	-	6.5	-	mA	
I_{DD3}	Erase current	-	4.5	-	mA	
N_{ENDUR}	Cycling Endurance	10,000	-	-	cycles[1]	T_J = -40℃~125℃
T_{RET}	Data retention	10	-	-	year	kcycle[1], T_J = 125℃

Note:

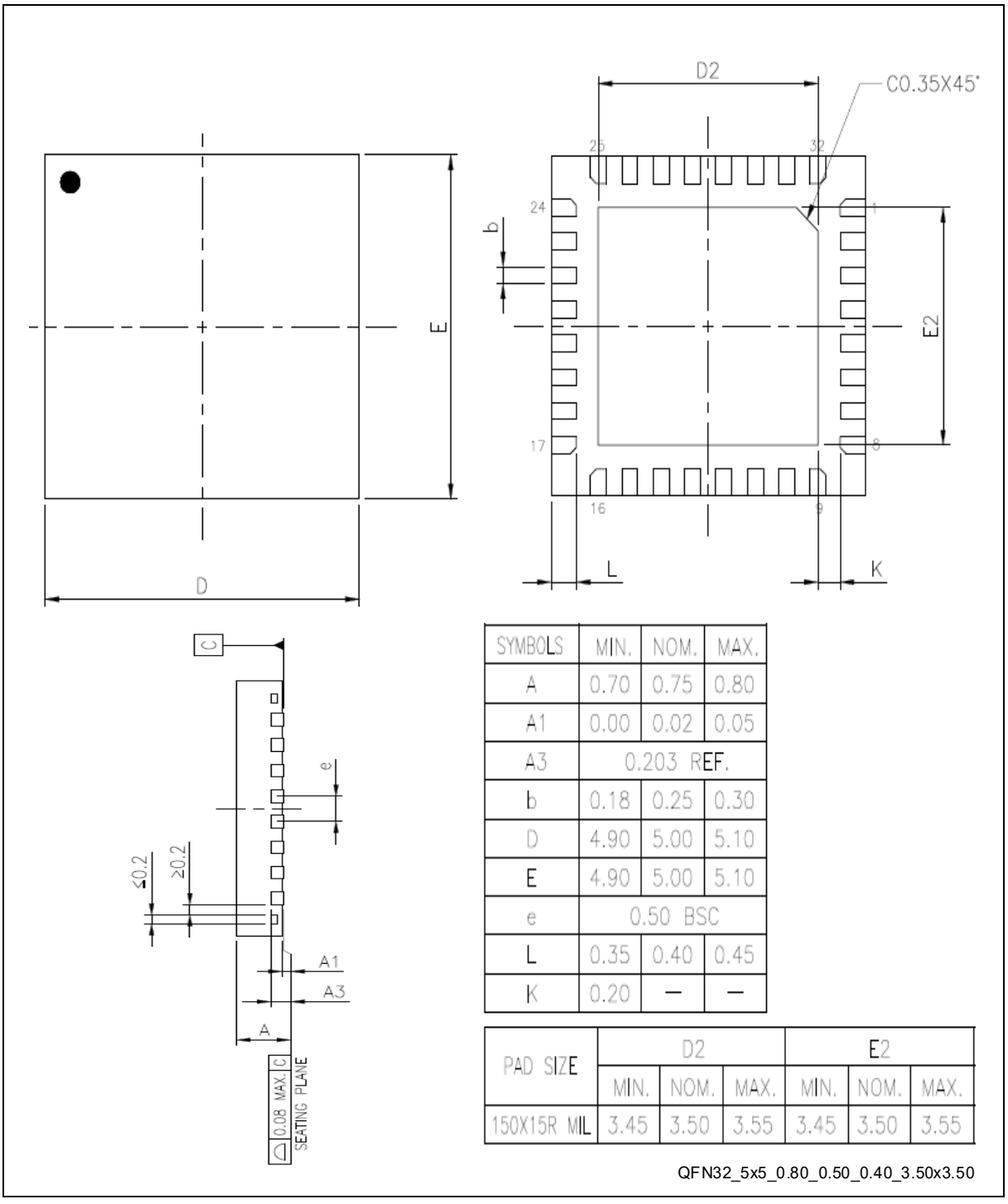
1. Number of program/erase cycles. Flash Data can only be programmed once at the same address after Flash erase.
2. Guaranteed by design, not tested in production.

Table 8.7-1 Flash DC Electrical Characteristics

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

9.1 QFN 33L (5x5x0.8 mm, Pitch 0.5 mm, Lead Length 0.4 mm)

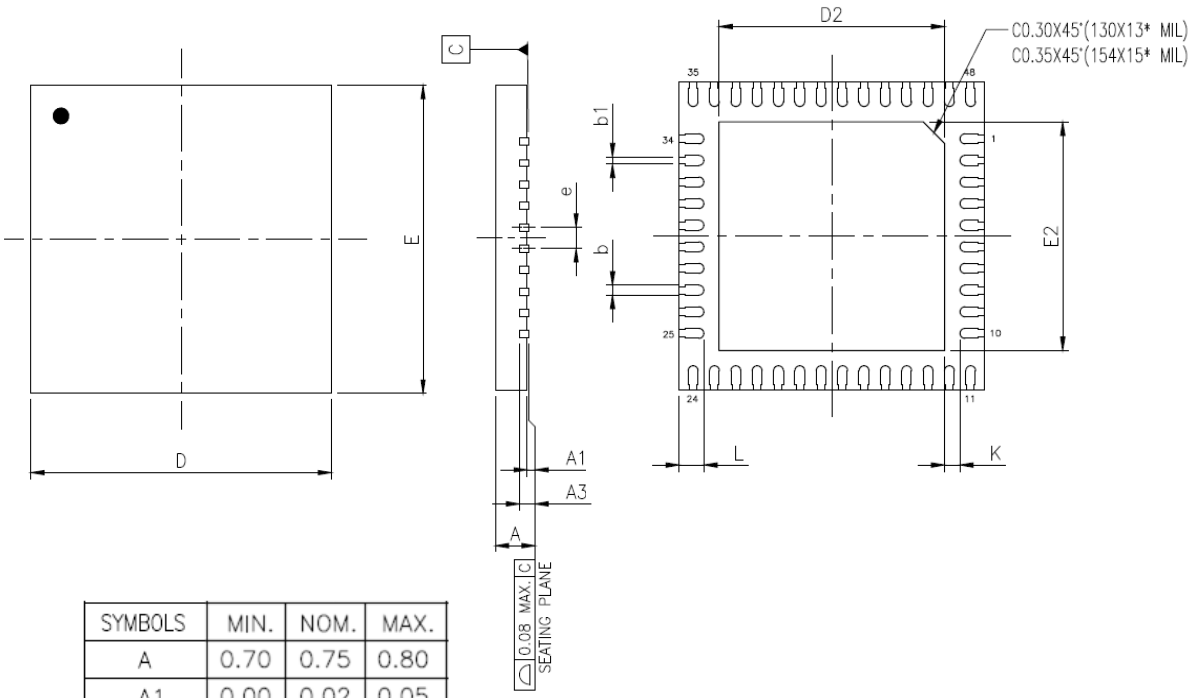


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
E	4.90	5.00	5.10
e		0.50 BSC	
L	0.35	0.40	0.45
K	0.20	—	—

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
150X15R MIL	3.45	3.50	3.55	3.45	3.50	3.55

QFN32_5x5_0.80_0.50_0.40_3.50x3.50

9.2 QFN 48L (5x5x0.8 mm, Pitch 0.35 mm, Lead Length 0.4 mm)

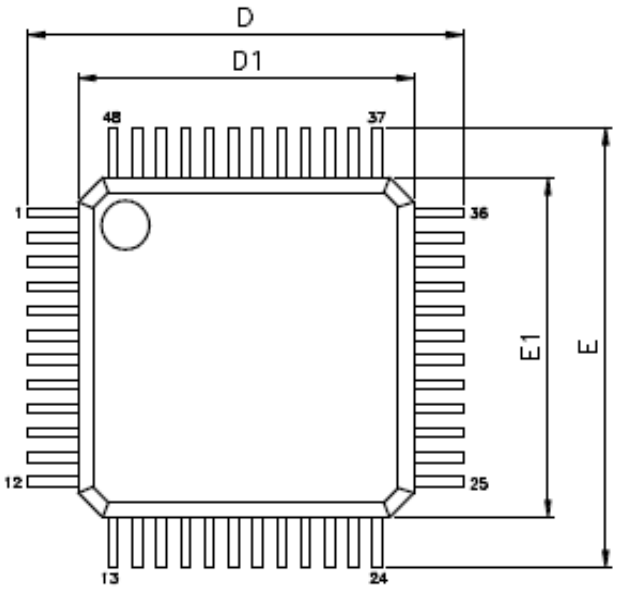


SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
130X13* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45
154X15* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45

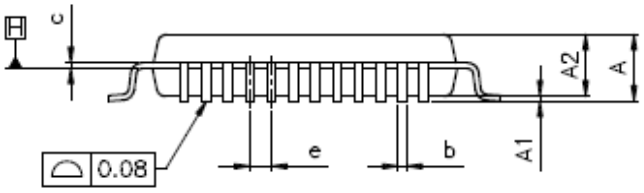
QFN48_5x5_0.80_0.35_0.40_3.70x3.70

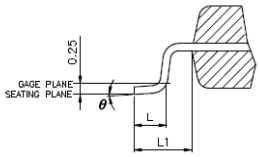
9.3 LQFP 48L (7x7x1.4 mm, Footprint 2.0mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

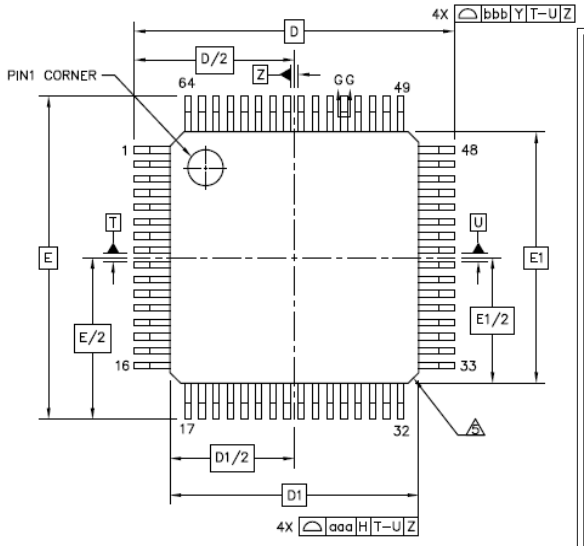
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°

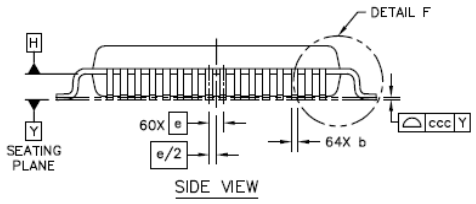


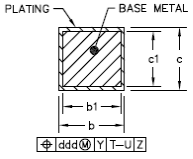


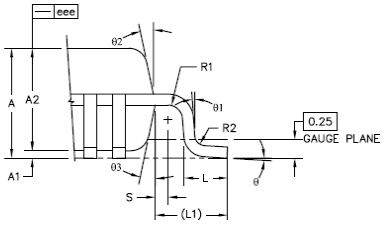
LQFP48_7X7_1.40_0.50_1.00

9.4 LQFP 64L (7x7x1.4 mm, Footprint 2.0 mm)





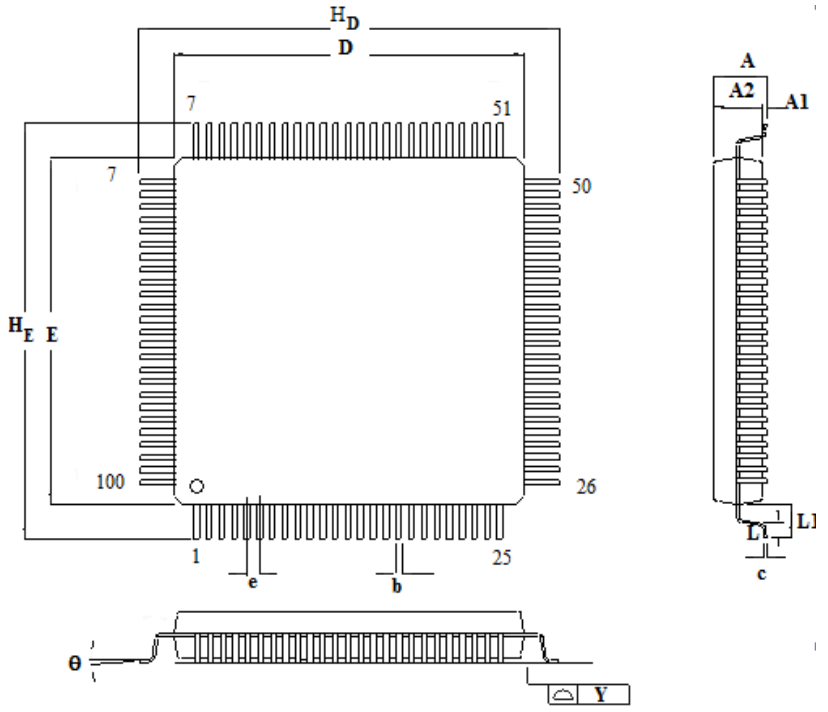




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	8.8	9	9.2
	Y	E	8.8	9	9.2
	X	D1	6.8	7	7.2
	Y	E1	6.8	7	7.2
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

LQFP64_7X7_1.40_0.40_1.00

9.5 LQFP 100L (14x14x1.4 mm, Footprint 2.0 mm)

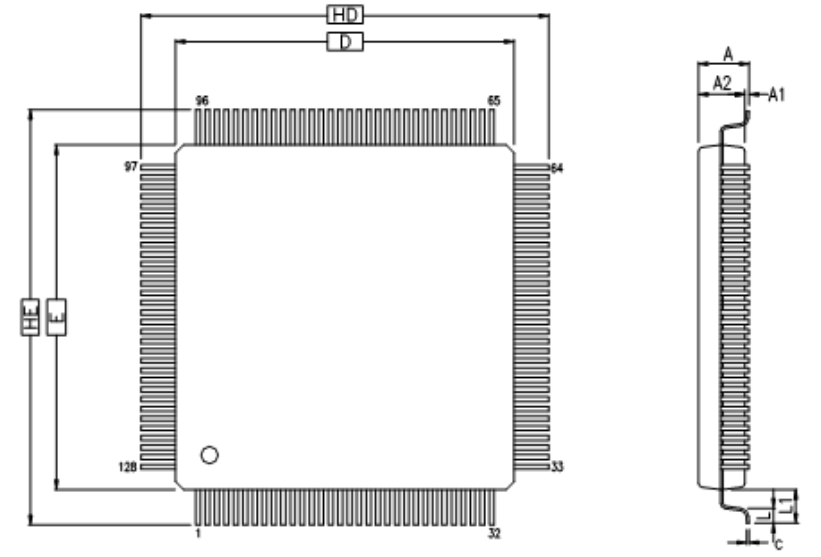


Controlling Dimension : Millimeters

SYMBOLS	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	-
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.10	0.15	0.20
D	13.90	14.00	14.10
E	13.90	14.00	14.10
e	-	0.50	-
HD	15.80	16.00	16.20
HE	15.80	16.00	16.20
L	0.45	0.60	0.75
L1	-	1	-
y	-	-	0.10
θ	0°	-	7°

LQFP100_14X14_1.40_0.50_1.00

9.6 LQFP 128L (14x14x1.4 mm, Footprint 2.0 mm)



SIDE VIEW

SYMBOL	MIN	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
HD	15.85	16.00	16.15
D	13.85	14.00	14.15
HE	15.85	16.00	16.15
E	13.85	14.00	14.15
b	0.13	0.16	0.23
e	-	0.40	-
θ°	0	3.5	7
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
Y	-	-	0.10

LQFP128_14X14_1.40_0.40_1.00

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2026.04.17	1.00	• Initial version.
2026.07.24	1.01	• Modified the table in section 3.1.1 M3351 Series • Fixed the typo M333x to M335x. • Modified the Table 8.1-4 EMC Characteristics as TBD.
2026.09.18	1.02	• Modified the table in the following sections of 8.1.4 EMC Characteristics 8.3.1 Supply Current Characteristics 8.3.3 Wakeup Time from Low-Power Modes 8.3.5 I/O DC Characteristics 8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC), 8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC), 8.5.2 Reset and Power Control Block Characteristics, 8.5.5 Digital to Analog Converter (DAC) 8.5.7 Internal Voltage Reference 8.5.8 Temperature Sensor

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