NuMicro® Family

Arm® Cortex®-M33-based Microcontroller

M3331 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro M3331 series is a 32-bit microcontroller powered by the Arm Cortex-M33 core. It integrates TrustZone® technology, a DSP instruction set, and a Floating-Point Unit (FPU). Designed for high-performance applications, it targets industrial control, smart factories, smart buildings, renewable energy, and consumer electronics. Operating at up to 180 MHz, the M3331 series supports 1.7V to 3.6V operating voltage and -40°C to +105°C wide operating temperature. It offers diverse packaging options and superior reliability, featuring high immunity with ESD HBM 4 kV and EFT 4.4 kV ratings.

Robust Memory and Security

The M3331 series provides up to 512 KB of Flash memory with Error Correction Code (ECC), 320 KB of SRAM (including 64 KB with hardware parity check), and an 8 KB user-defined loader (LDROM). To ensure robust security, it supports TrustZone technology, Secure Boot (Root of Trust, ROT), and Execute-Only Memory (XOM).

Enhanced Analog Features

The M3331 series integrates rich analog peripherals, including two analog comparators, up to 16 channels of 12-bit 4.2 Msps SAR ADC, multiple levels of internal voltage reference, a high-precision temperature sensor, low-voltage reset (LVR), and a brown-out detector (BOD) to reduce external components and form factors simultaneously.

Extensive Connectivity and Control Peripherals

The M3331 series supports a comprehensive range of peripherals, including one set of Enhanced LED Light Strip Interface (ELLSI) and 10 sets of LED Light Strip Interface (LLSI) for ARGB Gen1 and Gen2 LED control. It features up to 48 channels of 16-bit PWM, one I3C interface, two CAN FD controllers, and two Universal Serial Control Interfaces (USCI) configurable as UART, I²C, or SPI. Communication capabilities are further extended with five UARTs, three I²C, three SPI/I²S, one Quad-SPI, one SDH, and one USB High-Speed OTG/Device/Host controller with a built-in transceiver. Furthermore, the M3331 series incorporates one EQEI, one ECAP, one EBI, and a Real-Time Clock (RTC).

Supported packages include QFN 33-pin, QFN 48-pin, LQFP 48-pin, LQFP 64-pin, and LQFP 128-pin. Package is Halogen-free, RoHS-compliant and TSCA-compliant.

For the development, Nuvoton provides the NuMaker-M3334KI and NuMaker-M3333KI evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK Nuvoton Edition, IAR EWARM, VS Code are also supported.

Product Line	Core (MHz)	Flash (KB)	SRAM (KB)	Secure Boot	I3C	USB OTG	PWM	CAN FD	ELLSI	LLSI	USCI*	UART	I²C	SPI	EBI
M3334	180	512	320	√	1	HS x1	48	2	1	10	2	5+2	3+2	3+2	√
M3333	180	512	320	√	1	-	48	2	1	10	2	5+2	3+2	3+2	√
*USCI can be configured as UART/I²C/SPI.															

Table 2.1-1 NuMicro M3331 Series Key Features Support Table

The M3331 series is suitable for a wide range of applications such as:

- Industrial Control
- Smart Factories
- Smart Buildings
- Renewable Energy
- Consumer Electronics

2 FEATURES

2.1 M3331 Series Features

Core and System	
Arm Cortex-M33 with TrustZone®	• Arm Cortex-M33 processor, running up to 180 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports XOM feature with 4 regions • Supports DSP instruction set
Low power mode and current	• Low Power mode: – Idle mode • Power-down mode: – Normal Power-down mode 0 (NPD0) – Normal Power-down mode 1 (NPD1) – Normal Power-down mode 2 (NPD2) – Standby Power-down mode (SPD) – Deep Power-down mode (DPD)
Power supply and low voltage detect	• Built-in LDO for wide operating voltage from 1.7V to 3.6V • Core power voltage: 1.1V • Brown-out detector: – With 7 levels: 3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V – Supports Brown-out Interrupt and Reset option • Low Voltage Reset (LVR) with 1.5V threshold voltage level
Cyclic Redundancy Calculation Unit	• Supports four common polynomials CRC-8, CRC-16, and CRC-32 • Programmable seed value • Supports programmable order reverse setting for input data and CRC checksum • Supports programmable 1's complement setting for input data and CRC checksum • Supports 8/16/32-bit of data width

	• 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC • Supports Master mode
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Boot Loader	• Factory pre-loaded mask ROM for secure boot procedure and ISP procedure • Uses SHA-256 and ECDSA-P256 to validate data in APROM and LDROM • NuMicro ISP Programming Tool for firmware upgrade via UART, CAN FD, SPI, I^2C and high speed USB device
Flash Memory	• Up to 512 Kbytes on-chip Application ROM (APROM) • Dual bank 512 Kbytes APROM for Over-The-Air (OTA) upgrade • Four eXecute-Only-Memory (XOM) regions for code protection • Embedded with 4 Kbytes cache, with performance at zero wait cycle in continuous address read access • 8 Kbytes on-chip Flash for user-defined loader (LDROM) • 2 Kbytes One Time Programmable (OTP) ROM for data security • All on-chip Flash support 1 Kbytes page erase • Fast Flash programming verification with CRC32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 320 Kbytes on-chip SRAM includes: – 64 Kbytes SRAM located in bank 0 with programmable size of SPD retention; The first 64 Kbytes supports hardware parity check; Exception (NMI) generated upon a parity check error – 128 Kbytes SRAM located in bank 1 with SPD retention – 128 Kbytes SRAM located in bank 2 with SPD

	retention • Supports byte-, half-word- and word-access • PDMA operation
Peripheral DMA (PDMA)	• Up to 16 independent and configurable channels for automatic data transfer between memories and peripherals • Selectable 2 level of priority (fixed priority or round-robin priority) • Supports transfer data width of 8, 16, and 32 bits • Supports source and destination address increment size can be byte, half-word, word or no increment • Supports software and USB, UART, USCI, SPI, QSPI, ACMP, EINT, EPWM, I^2C, I^2S, Timer, and ADC request • Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table. • Supports single and burst transfer type • Supports time-out function on all of PDMA channels • Supports stride function from channel 0 to channel 5 • Supports enhanced stride function on channel 0 and channel 1
Clocks	
External Clock Source	• Built-in 4~32 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • Built-in 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• Built-in 48 MHz High-speed Internal RC oscillator (HIRC48) for crystal-less USB • Built-in 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Supports one PLL up to 180 MHz for high performance system operation, sourced from HIRC and HXT
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter • Independent clock source for each timer • Provides one-shot, periodic, toggle-output and continuous counting operation modes • 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0]) • Supports event counting function

	• Supports 3-bit capture input noise filter • 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0]) • Supports external capture pin event for interval measurement • Supports external capture pin event to reset 24-bit up counter • Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, EADC, EQEI and PDMA function • Supports internal capture triggered while internal ACMP output signal transition • Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event • Supports Inter-Timer trigger mode • Supports event counting source from ACMP or internal USB SOF signal • Supports internal capture triggered source from ACMP output, HXT, HIRC, LIRC and LXT • Supports over-capture flag **PWM** • Supports maximum clock frequency up to maximum PCLK • Supports independent mode for PWM generator with two output channels • Supports complementary mode for PWM generator with paired PWM output channel • Supports 12-bit prescale from 1 to 4096 • Supports 16-bit PWM counter • Supports mask function and tri-state enable for each PWM output pin • Supports brake function • Supports interrupt on the following events: – Supports PWM output accumulator event to trigger PDMA transfer – Supports PWM output accumulator event to stop PWM counting • Supports trigger EADC on the following events: – Supports External Pin event to trigger PWM counter action
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 180 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter • Supports dead time with maximum divided 12-bit prescale

	• Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Trigger EADC to start conversion after a short delay • Supports External Pin Trigger Function

Basic PWM (BPWM)	• Supports up to six BPWM modules; each module provides 6 output channels
	• Supports independent mode for BPWM output/Capture input channel
	• Supports 12-bit prescaler from 1 to 4096
	• Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
	  – Up, down and up/down counter operation type
	• Supports mask function and tri-state enable for each BPWM pin
	• Supports interrupt in the following events:
	  – BPWM counter matches 0, period value or compared value
	• Supports trigger EADC0/1/2 in the following events:
	  – BPWM counter matches 0, period value or compared value
	• Supports up to 12 capture input channels with 16-bit resolution
	• Supports rising or falling capture condition
	• Supports input rising/falling capture interrupt
	• Supports rising/falling capture with counter reload option

Watchdog	• 20-bit free running up counter for WDT time-out interval • Selectable time-out interval (24 ~ 220) * (1 / WDT_CLK) • System kept in reset state for a period of (1 / WDT_CLK) * 63 • Supports selectable WDT reset delay period, including 1026/130/18/3 WDT_CLK reset delay period • Supports to force Secure only WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register • Supports WDT time-out wake-up function only if WDT clock source is selected as 38.4kHz LIRC or LXT
RTC	• Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check • Supports alarm time (hour, minute, second) and calendar (year,

	month, day) settings in RTC_TALM and RTC_CALM • Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK • Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register • Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM • Supports Leap Year indication in RTC_LEAPYEAR register • Supports Day of the Week counter in RTC_WEEKDAY register • Frequency of RTC clock source compensate by RTC_FREQADJ register • All time and calendar message expressed in BCD format • Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second • Supports RTC Time Tick and Alarm Match interrupt • Supports 1 Hz clock output • Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated • Supports Daylight Saving Time software control in RTC_DSTCTL
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• Up to one set of 12-bit, 31-ch 4.5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and $AV_{DD}/4$. • Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC • Supports calibration function and calibration interrupt • Supports internal reference voltage VREF: 1.6V, 2V, 2.5V and 3V. • Supports power-down mode and ultra low frequency mode • Up to 19 sample modules • Averaging (2n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2n times, n=0~8) to support up to 16-bit result • Supports conversion results left-alignment • Supports PDMA transfer • Conversion Result Monitor by Compare Mode
Analog Comparator (ACMP)	• Up to four rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports programmable propagation speed and low power

	consumption • Supports power-down wake-up function • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 10mV, 20mV, 30mV and 40mV • Supports offset calibration
Internal Reference Voltage	• Internal reference voltage select: 1.6V, 2.0V, 2.5V, 3.0V for EADC, and CRV (comparator reference voltage) reference voltage • One built-in temperature sensor • Supported temperature range: –40°C to +105°C
Communication Interfaces	
UART	• Full-duplex asynchronous communications • Separates receive and transmit 16/16 bytes entry FIFO for data payloads • Supports hardware auto-flow control • Programmable receiver buffer trigger level • Supports programmable baud rate generator for each channel individually • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function • Supports 8-bit receiver buffer time-out detection function • Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8]) • Supports Auto-Baud Rate measurement and baud rate compensation function • Supports break error, frame error, parity error and receive/transmit buffer overflow detection function • Fully programmable serial-interface characteristics • Supports IrDA SIR function mode • Supports LIN function mode (UART0 with LIN function) • Supports RS-485 function mode • Supports PDMA transfer function • Supports Single-wire function mode
I^2C	• Supports up to three I^2C ports • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master)

	• Supports High speed mode 3.4Mbps • Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Arbitration between simultaneously transmitting masters without corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer • Built-in 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflow • Programmable clocks allow for versatile rate control • Supports 7-bit addressing and 10-bit addressing mode • Supports multiple address recognition (four slave address with mask option) • Supports Power-down wake-up function • Supports PDMA with one buffer capability • Supports setup/hold time programmable • Supports Bus Management (SM/PM compatible) function
Quad SPI	• Supports Master or Slave mode operation • Master mode up to 90 MHz (when chip works at V_{DD} = 2.7V~3.6V) • Slave mode up to 45 MHz (when chip works at V_{DD} = 2.7V~3.6V) • Supports 2-bit Transfer mode • Supports Dual and Quad I/O Transfer mode • Configurable bit length of a transaction word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports Transmit Double Transfer Rate Mode (TX DTR mode) • Supports receive-only mode
SPI/I^2S	• Up to three sets of SPI/I^2S controllers with Master/Slave mode **SPI** • Supports Master or Slave mode operation • Master mode up to 90 MHz (when chip works at V_{DD} = 2.7 ~ 3.6V) • Slave mode up to 45 MHz (when chip works at V_{DD} = 2.7 ~ 3.6V) • Configurable bit length of a transaction word from 4 to 32-bit

	• Provides separate 4-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports Master or Slave • Capable of handling 8-, 16-, 24- and 32-bit word sizes • Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving • Supports monaural and stereo audio data • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • Supports two PDMA requests, one for transmitting and the other for receiving
I²S	• Supports Master mode and Slave mode • Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel • Supports monaural and stereo audio data • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8 • Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving • Generates interrupt requests when buffer levels cross a programmable boundary • Supports two PDMA requests, one for transmitting and the other for receiving
Universal Serial Control Interface (USCI)	• Configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffer for data payload • Supports hardware auto flow control function • Supports programmable baud-rate generator

	• Supports 9-bit Data Transfer (Support 9-bit RS-485) • Baud rate detection possible by built-in capture event of baud rate generator • Supports PDMA transfer • Supports Wake-up function (Incoming Data and nCTS Wakeup) **SPI** • Supports Master or Slave mode operation (the maximum frequency -- Master = $f_{PCLK}/2$, Slave < $f_{PCLK}/5$) • Configurable bit length of a transfer word from 4 to 16-bit • Supports one transmit buffer and two receive buffers for data payload • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function by slave select signal in Slave mode • Supports one data channel half-duplex transfer **I^2C** • Full master and slave device capability • Supports of 7-bit addressing, as well as 10-bit addressing • Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s) • Supports multi-master bus • Supports one transmit buffer and two receive buffer for data payload • Supports 10-bit bus time-out capability • Supports bus monitor mode. • Supports Power down wake-up by START signal or address match • Supports setup/hold time programmable • Supports multiple address recognition (two slave addresses with mask option)
Controller Area Network with Feasibility Data Rate (CAN FD)	• Conform with CAN protocol version 2.0 part A, B and ISO 11898-1:2015 • CAN FD with up to 64 data bytes supported • CAN Error Logging • AUTOSAR and SAE J1939 support • Improved acceptance filtering • Two configurable Receive FIFOs • Separate signaling on reception of High Priority Messages • Configurable Transmit FIFO, Transmit Queue and Transmit Event FIFO

	• Direct Message RAM access for CPU • Programmable loop-back test mode • Maskable module interrupts • Two clock domains (CAN Core clock and AHB clock) • Power-down support
Secure Digital Host Controller (SDH)	• Compliant with SD Memory Card Specification Version 2.0 • Supports single DMA channel • Supports hardware Scatter-Gather function • Using single 128 Bytes shared buffer for data exchange between system memory and cards • Synchronous design for DMA with single clock domain, AHB bus clock (HCLK) • Interface with DMAC for register read/write and data transfer • Supports SD/SDHC card • Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock
External Bus Interface (EBI)	• Supports up to three memory banks • Supports dedicated external chip select pin with polarity control for each bank • Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out • Supports 8-/16-bit data width • Supports byte write in 16-bit data width mode • Supports Address/Data multiplexed Mode • Supports Timing parameters individual adjustment for each memory block • Supports LCD interface i80 mode • Supports PDMA mode • Supports variable external bus base clock (MCLK) which based on HCLK • Supports configurable idle cycle for different access conditions: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports address bus and data bus separate mode
LED Light Strip Interface (LLSI)	• 10 sets of LLSI channels with IDLE polarity control • Each LLSI has 4x32-bit TX FIFO • Configurable transfer period and frame reset length • Configurable T0H and T1H duty cycle • Supports RGB and GRB output format • Supports Software mode and PDMA base mode transfer

Enhanced LED Light Strip Interface (ELLSI)	• 1 set of ELLSI channels with IDLE polarity control • ELLSI has 4x32-bit TX FIFO • Configurable transfer period and frame reset length • Configurable T0H and T1H duty cycle • Supports RGB and GRB output format • Supports Software mode and PDMA base mode transfer • Supports LED advanced command mode (Feedback, TH20 Setting mode, Command mode) • Configurable advanced command pulse width
I3C	• Supports one I3C port • Supports Controller and Target mode • Static or Dynamic Target Device support • Built-in Hardware Dynamic Address Allocation support • Built-in CCC transfer handler • Auto Hot-Join request generation support • In-Band Interrupt request generation support • Adaptive mode of operation between I^2C and I3C depending on I3C bus traffic • Built-in TE0-TE5 Error Handling • Supports Power-down wake-up function • Supports PDMA mode for data transfer • Supports SDR mode, data rates up to 12.5 Mbps • Supports HDR-DDR mode, data rates up to 25 Mbps • Supports Secondary Controller mode • Supports Target Reset – basic V1.1.1 IP • Supports Set Static Address as Dynamic Address CCC – basic V1.1.1 IP • Supports Asynchronous Timing control (Mode 0) – basic V1.1.1 IP • Supports Grouped Addressing – basic V1.1.1 IP • Supports HDR-BT mode – basic V1.1.1 IP • Supports Composited / Virtual Targets – basic V1.1.1 IP
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O • Configurable I/O mode of all pins after reset default to Quasi-

	bidirection mode or input mode
Control Interfaces	
Enhanced Quadrature Encoder Interface (EQEI)	• One EQEI controller • Two EQEI phase inputs, QEA and QEB; One Index input. • One 32-bit up/down Quadrature Encoder Pulse Counter • Supports swap function for input signals QEA and QEB • Supports for detecting the occurrence of phase error from input signals QEA and QEB • Supports one times index signal reset function for Quadrature encoder pulse counter • Encoder Pulse Width measurement mode
Enhanced Capture (ECAP)	• One Input Capture Timer/Counter unit • Each unit has 3 input channels • Each unit has its own interrupt vector • Each input channel has its own capture counter hold register • 24-bit Input Capture up-counting timer/counter • With noise filter in front end of input ports • Captured events reset and/or reload capture counter • Supports compare-match function
Advanced Connectivity	
USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed OTG (On-The-Go)** • On-chip USB 2.0 high speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0 • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Built-in DMA **USB 2.0 High Speed Device Controller**

- Compliant with USB Revision 2.0 Specification
- Supports 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Maximum packet size up to 1024 bytes
- Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode
- Suspend, resume and remote wake-up capability
- Built-in DMA
- Supports Battery Charging 1.2 (BC1.2)
- Supports Link Power Management (LPM)

3 PARTS INFORMATION

3.1 M3331 Series Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	QFN33 (4x4mm)	QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)	LQFP128 (14x14mm)
M3334	M3334TIGAE M3334TGAAE	M3334YIGAE M3334YGAAE	M3334LIGAE M3334LGAAE	M3334SIGAE M3334SGAAE	M3334KIGAE
M3333	M3333TIGAE M3333TGAAE	M3333YIGAE M3333YGAAE	M3333LIGAE M3333LGAAE	M3333SIGAE M3333SGAAE	M3333KIGAE

3.2 M3331 Series Naming Rule

M33	31	K	I	G	A	E
Core	**Series**	**Package**	**Flash Size**	**SRAM Size**	**Revision**	**Temperature**
Cortex-33	34: USB HS 33: Base	K: LQFP128 (14x14 mm) S: LQFP64 (7x7 mm) L: LQFP48 (7x7 mm) Y: QFN48 (5x5 mm) T: QFN33 (4x4mm)	I: 512 KB G: 256 KB	G: 320 KB A: 96 KB	A	E: -40˚C to +105˚C

3.3 M3331 Series Selection Guide

3.3.1 M3334 Series

PART NUMBER		M3334				
		KIGAE	SIGAE	LIGAE	YIGAE	TIGAE
System Frequency (MHz)		180	180	180	180	180
Flash Memory (KB)		512	512	512	512	512
SRAM (KB)		320	320	320	320	320
LDROM (KB)		8	8	8	8	8
XOM (regions)		4	4	4	4	4
PDMA		16-ch	16-ch	16-ch	16-ch	16-ch
Secure Boot		√	√	√	√	√
I/O		102	46	34	34	21
32-bit Timer		4	4	4	4	4
16-bit EPWM		12	12	12	12	12
16-bit BPWM		36	33	28	28	17
Connectivity	I3C	1	1	1	1	1
	PDCI	-	-	-	-	-
	ELLSI	1	1	1	1	1
	LLSI	10	10	10	10	8
	UART	5	5	5	5	5
	SPI/I²S	3/3	3/3	3/3	3/3	2/2
	I²S	1	1	1	1	1
	I²C	3	3	3	3	3
	USCI (can be configured as UART/I²C/SPI)	2	2	2	2	2
	CAN FD	2	2	2	2	-
	SDH	1	1	1	1	1
	QSPI	1	1	1	1	1
LCD Parallel Data Bus (External Bus Interface)		√	√	-	-	-
USB High Speed with PHY		OTG	OTG	OTG	OTG	Device
12-bit ADC		16	16	12	12	10
Analog Comparator		2	2	2	2	2
EQEI		1	1	1	1	-
eCapture		1	1	1	1	-
RTC		√	√	√	√	√
Package		LQFP 128 (14x14mm)	LQFP 64 (7x7mm)	LQFP 48 (7x7mm)	QFN 48 (5x5mm)	QFN 33 (4x4mm)

PART NUMBER		M3334			
		SGAAE	LGAAE	YGAAE	TGAAE
System Frequency (MHz)		180	180	180	180
Flash Memory (KB)		256	256	256	256
SRAM (KB)		96	96	96	96
LDROM (KB)		8	8	8	8
XOM (regions)		4	4	4	4
PDMA		9-ch	9-ch	9-ch	9-ch
Secure Boot		√	√	√	√
I/O		46	34	34	21
32-bit Timer		4	4	4	4
16-bit EPWM		12	12	12	12
16-bit BPWM		12	12	12	12
Connectivity	I3C	-	-	-	-
	PDCI	28	24	24	16
	ELLSI	-	-	-	-
	LLSI	10	10	10	8
	UART	4	4	4	4
	SPI/I²S	2/1	2/1	2/1	2/1
	I²S	-	-	-	-
	I²C	2	2	2	2
	USCI (can be configured as UART/I²C/SPI)	1	1	1	1
	CAN FD	1	1	1	-
	SDH	-	-	-	-
	QSPI	1	1	1	1
LCD Parallel Data Bus (External Bus Interface)		-	-	-	-
USB High Speed with PHY		OTG	OTG	OTG	Device
12-bit ADC		16	12	12	10
Analog Comparator		-	-	-	-
EQEI		1	1	1	-
eCapture		1	1	1	-
RTC		√	√	√	√
Package		LQFP 64 (7x7mm)	LQFP 48 (7x7mm)	QFN 48 (5x5mm)	QFN 33 (4x4mm)

3.3.2 M3333 Series

PART NUMBER		M3333				
		KIGAE	SIGAE	LIGAE	YIGAE	TIGAE
System Frequency (MHz)		180	180	180	180	180
Flash Memory (KB)		512	512	512	512	512
SRAM (KB)		320	320	320	320	320
LDROM (KB)		8	8	8	8	8
XOM (regions)		4	4	4	4	4
PDMA		16-ch	16-ch	16-ch	16-ch	16-ch
Secure Boot		√	√	√	√	√
I/O		110	54	42	42	27
32-bit Timer		4	4	4	4	4
16-bit EPWM		12	12	12	12	12
16-bit BPWM		36	36	33	33	24
Connectivity	I3C	1	1	1	1	1
	PDCI	-	-	-	-	-
	ELLSI	1	1	1	1	1
	LLSI	10	10	10	10	10
	UART	5	5	5	5	5
	SPI/I²S	3/3	3/3	3/3	3/3	3/3
	I²S	1	1	1	1	1
	I²C	3	3	3	3	3
	USCI (can be configured as UART/I²C/SPI)	2	2	2	2	2
	CAN FD	2	2	2	2	1
	SDH	1	1	1	1	1
	QSPI	1	1	1	1	1
LCD Parallel Data Bus (External Bus Interface)		√	√	√	√	-
USB High Speed with PHY		-	-	-	-	-
12-bit ADC		16	16	12	12	10
Analog Comparator		2	2	2	2	2
EQEI		1	1	1	1	-
eCapture		1	1	1	1	-
RTC		√	√	√	√	√
Package		LQFP 128 (14x14mm)	LQFP 64 (7x7mm)	LQFP 48 (7x7mm)	QFN 48 (5x5mm)	QFN 33 (4x4mm)

PART NUMBER		M3333			
		SGAAE	LGAAE	YGAAE	TGAAE
System Frequency (MHz)		180	180	180	180
Flash Memory (KB)		256	256	256	256
SRAM (KB)		96	96	96	96
LDROM (KB)		8	8	8	8
XOM (regions)		4	4	4	4
PDMA		9-ch	9-ch	9-ch	9-ch
Secure Boot		√	√	√	√
I/O		46	34	34	21
32-bit Timer		4	4	4	4
16-bit EPWM		12	12	12	12
16-bit BPWM		12	12	12	12
Connectivity	I3C	-	-	-	-
	PDCI	28	24	24	16
	ELLSI	-	-	-	-
	LLSI	10	10	10	8
	UART	4	4	4	4
	SPI/I²S	2/1	2/1	2/1	2/1
	I²S	-	-	-	-
	I²C	2	2	2	2
	USCI (can be configured as UART/I²C/SPI)	1	1	1	1
	CAN FD	1	1	1	-
	SDH	-	-	-	-
	QSPI	1	1	1	1
LCD Parallel Data Bus (External Bus Interface)		-	-	-	-
USB High Speed with PHY		-	-	-	-
12-bit ADC		16	12	12	10
Analog Comparator		-	-	-	-
EQEI		1	1	1	-
eCapture		1	1	1	-
RTC		√	√	√	√
Package		LQFP 64 (7x7mm)	LQFP 48 (7x7mm)	QFN 48 (5x5mm)	QFN 33 (4x4mm)

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in the M3331 Series Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.2 Pin Diagram

4.2.1 QFN33-Pin Diagram

Corresponding Part Number: M3333TIGAE, M3333TGAAE

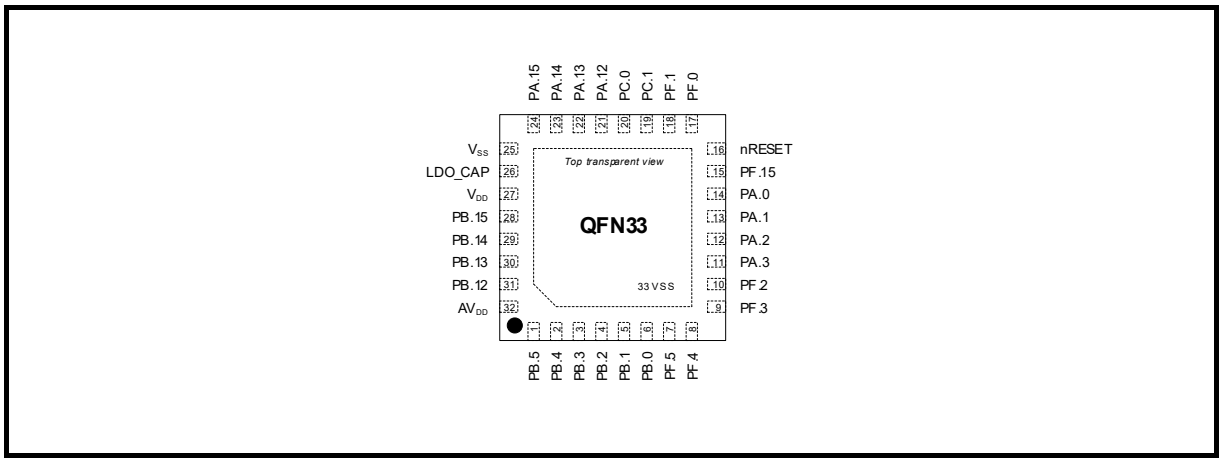


Figure 4.2-1 QFN33-Pin Diagram

4.2.2 UQFN33-Pin Diagram

Corresponding Part Number: M3334TIGAE, M3334TGAAE

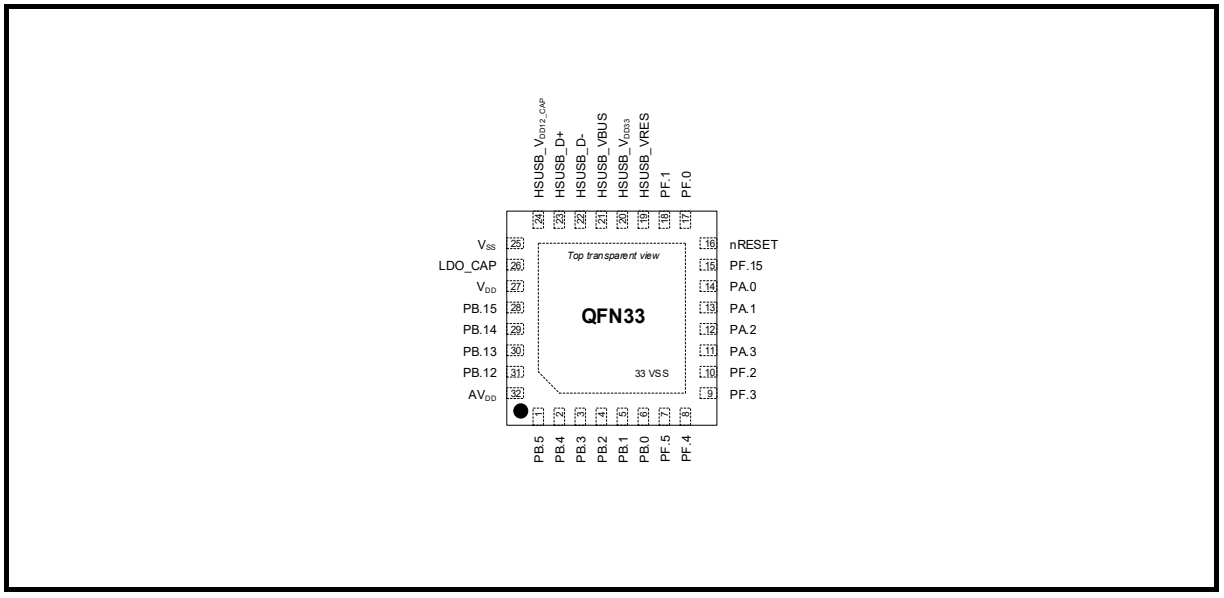


Figure 4.2-2 UQFN33-Pin Diagram

4.2.3 QFN48-Pin Diagram

Corresponding Part Number: M3333YIGAE, M3333YGAAE

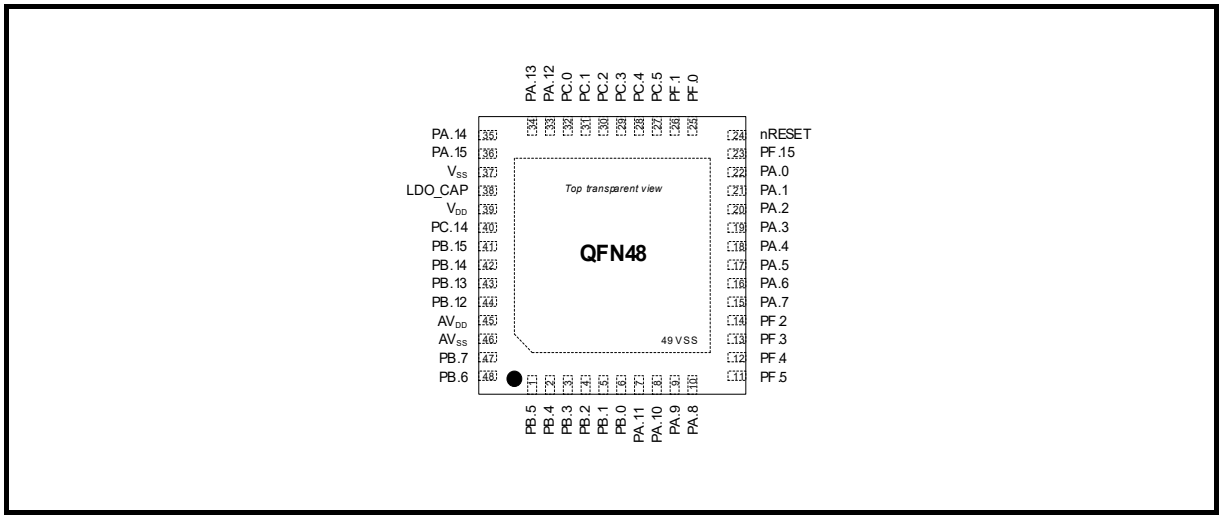


Figure 4.2-3 QFN48-Pin Diagram

4.2.4 UQFN48-Pin Diagram

Corresponding Part Number: M3334YIGAE, M3334YGAAE

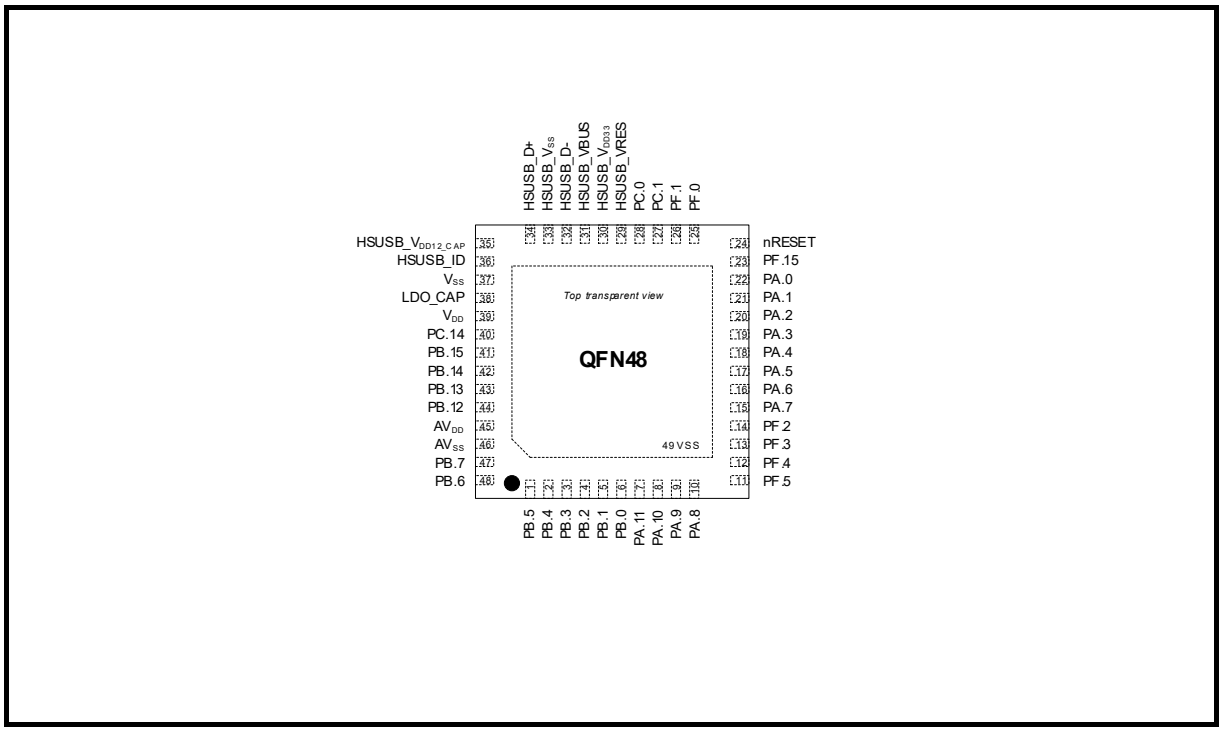


Figure 4.2-4 UQFN48-Pin Diagram

4.2.5 LQFP48-Pin Diagram

Corresponding Part Number: M3333LIGAE, M3333LGAAE

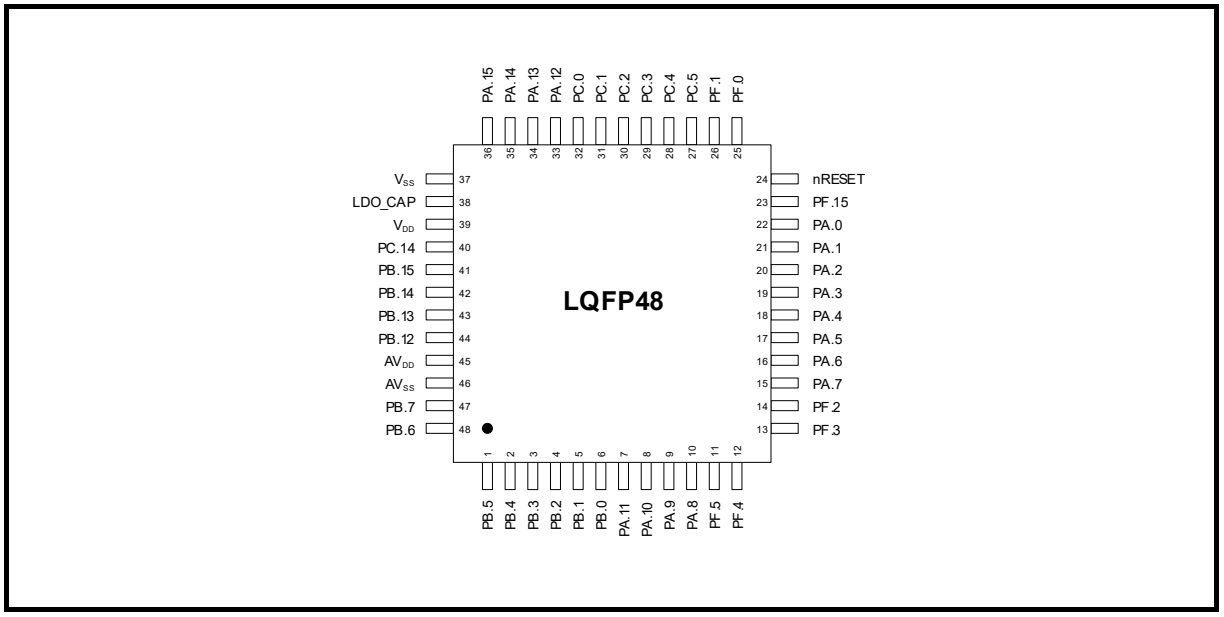


Figure 4.2-5 LQFP48-Pin Diagram

4.2.6 ULQFP48-Pin Diagram

Corresponding Part Number: M3334LIGAE, M3334LGAAE

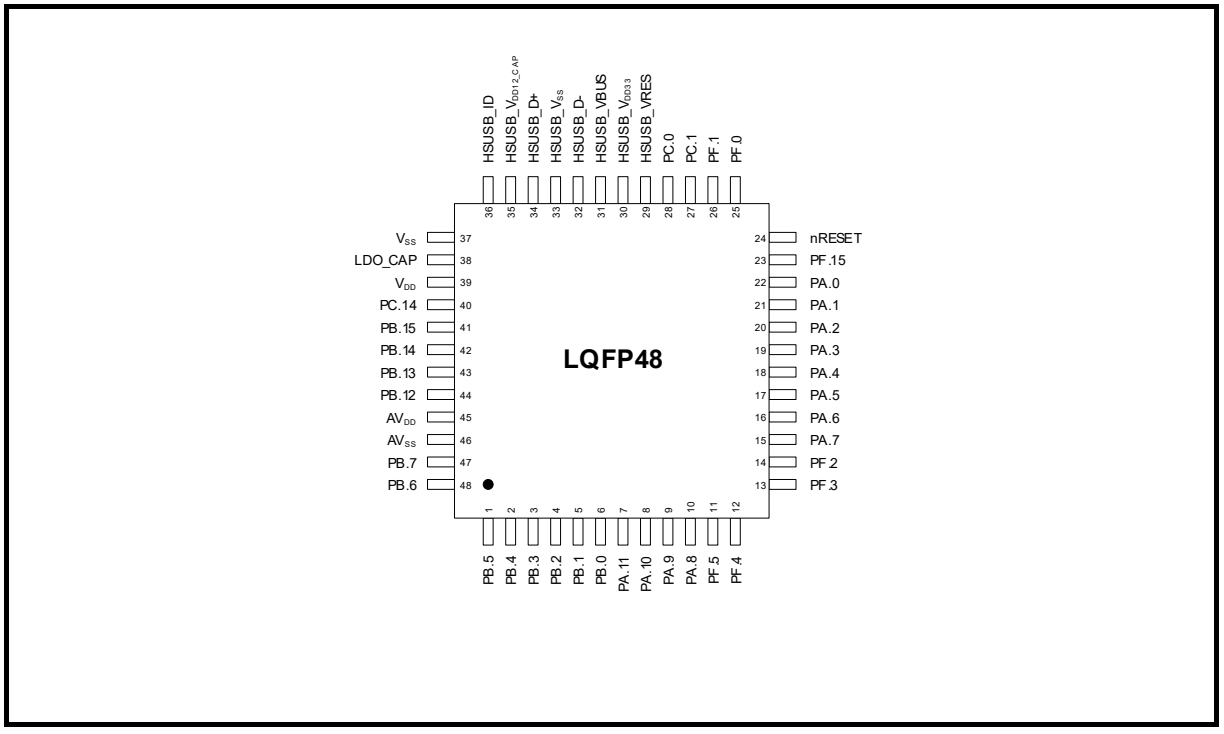


Figure 4.2-6 ULQFP48-Pin Diagram

4.2.7 LQFP64-Pin Diagram

Corresponding Part Number: M3333SIGAE, M3333SGAAE

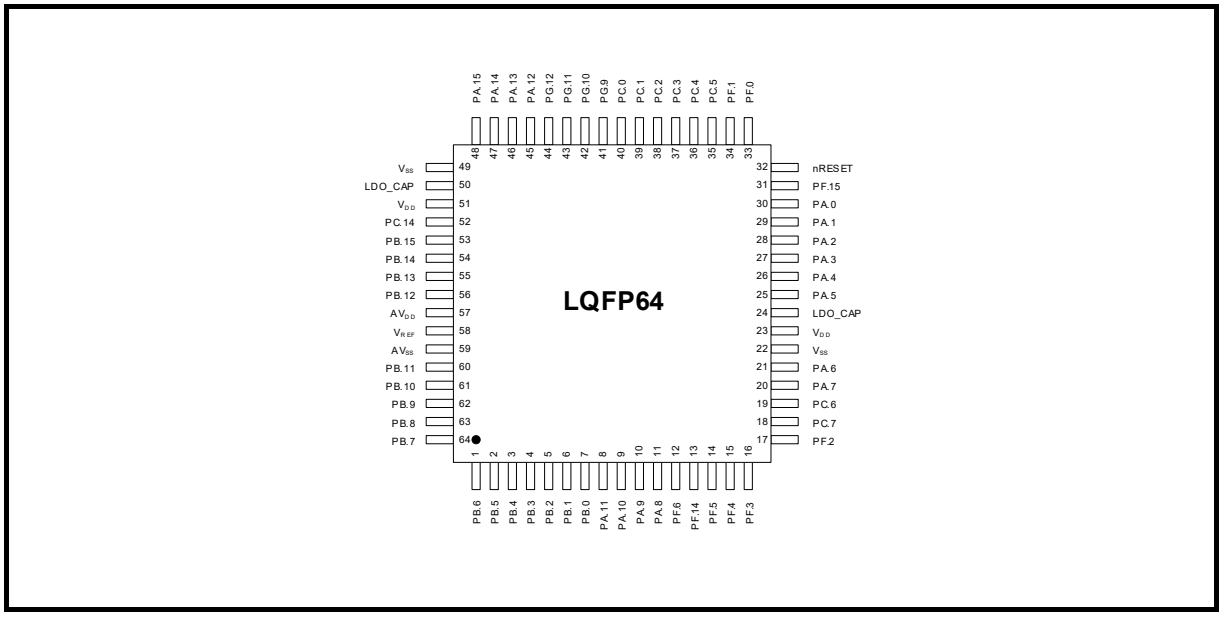


Figure 4.2-7 LQFP64-Pin Diagram

4.2.8 ULQFP64-Pin Diagram

Corresponding Part Number: M3334SIGAE, M3334SGAAE

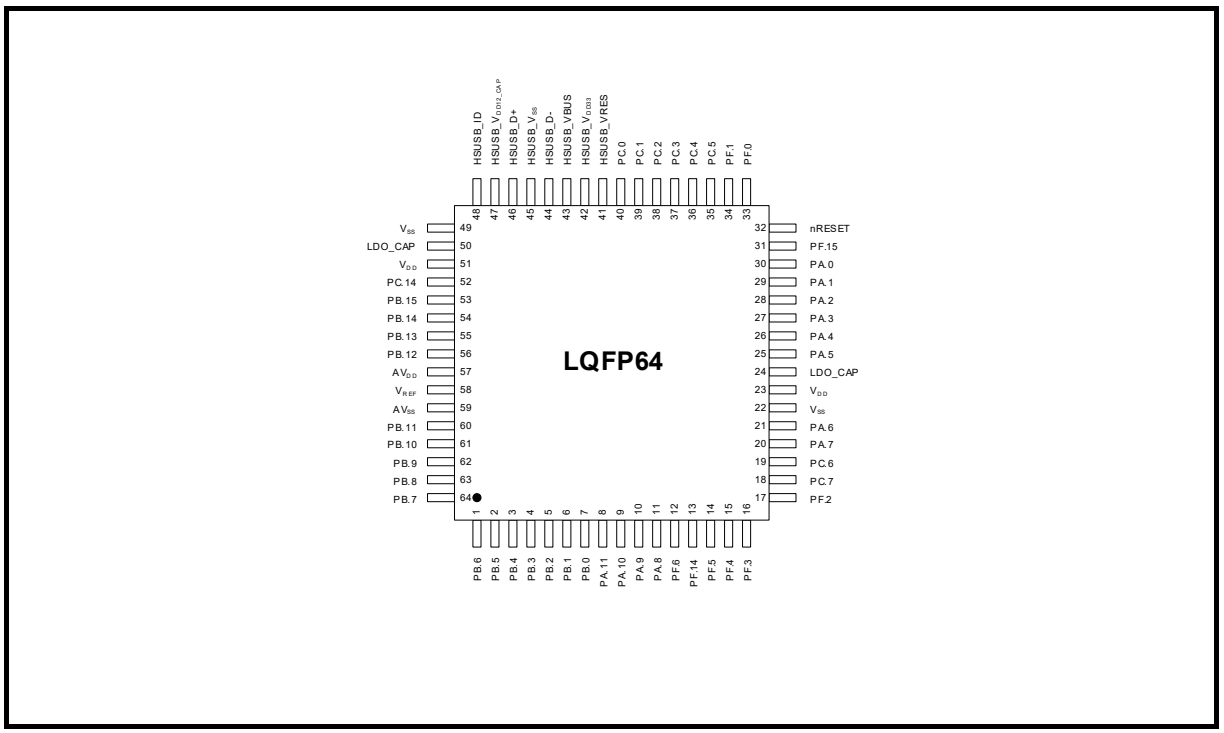


Figure 4.2-8 ULQFP64-Pin Diagram

4.2.9 LQFP128-Pin Diagram

Corresponding Part Number: M3333KIGAE

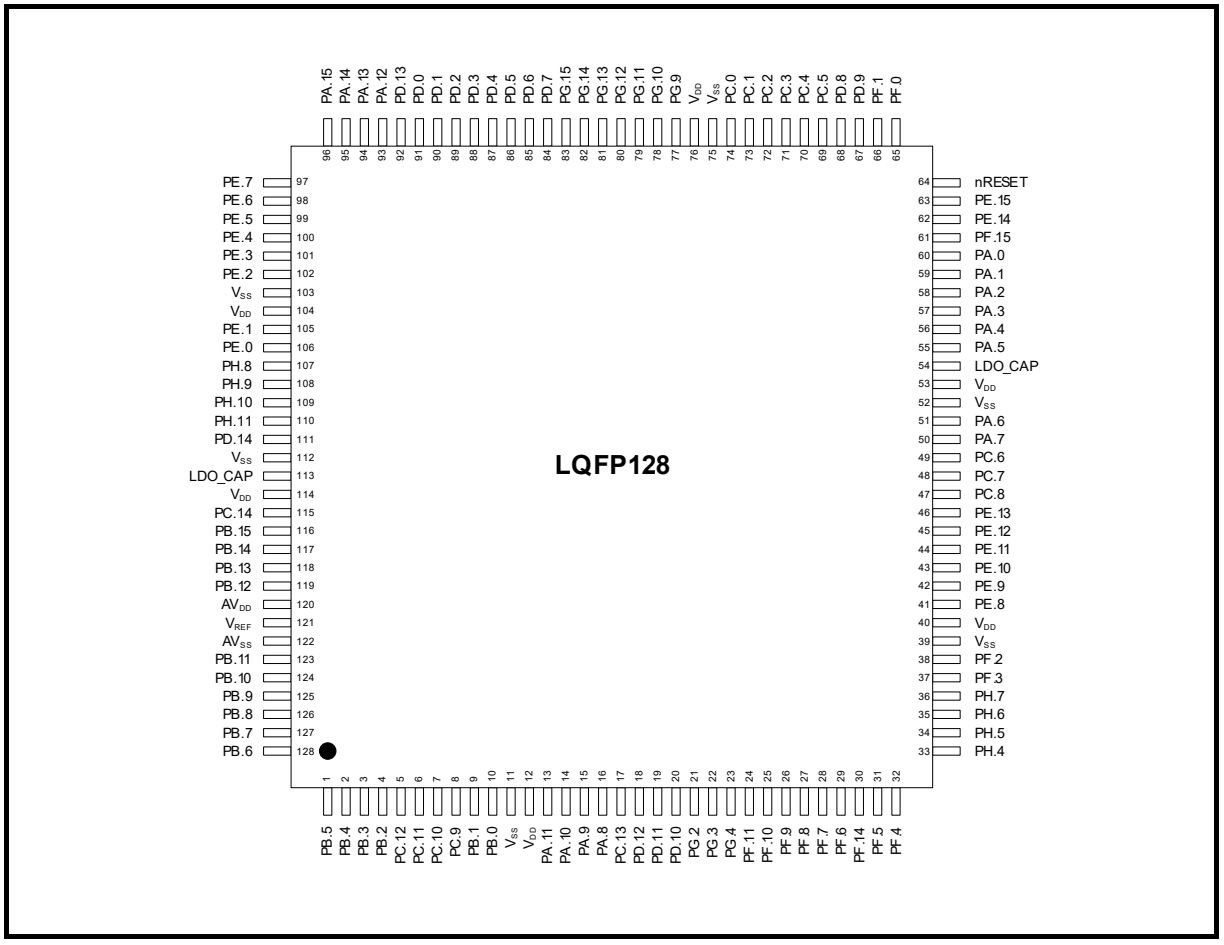


Figure 4.2-9 LQFP128-Pin Diagram

4.2.10 ULQFP128-Pin Diagram

Corresponding Part Number: M3334KIGAE

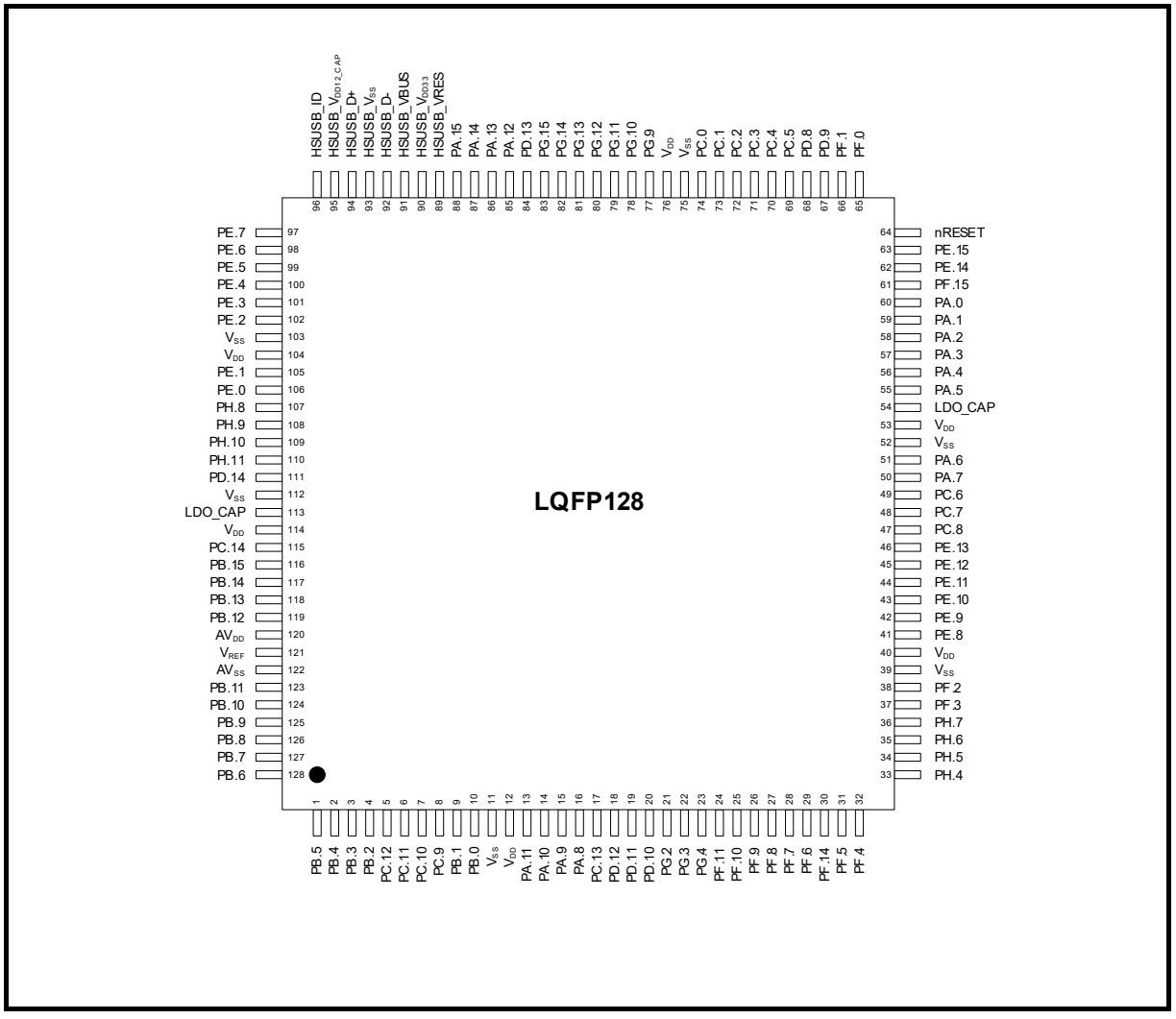


Figure 4.2-10 ULQFP128-Pin Diagram

4.3 Multi-function Pin Diagram

4.3.1 QFN33-Pin Multi-function Pin Diagram

Corresponding Part Number: M3333TIGAE

4.3.1.1 M3333TIGAE

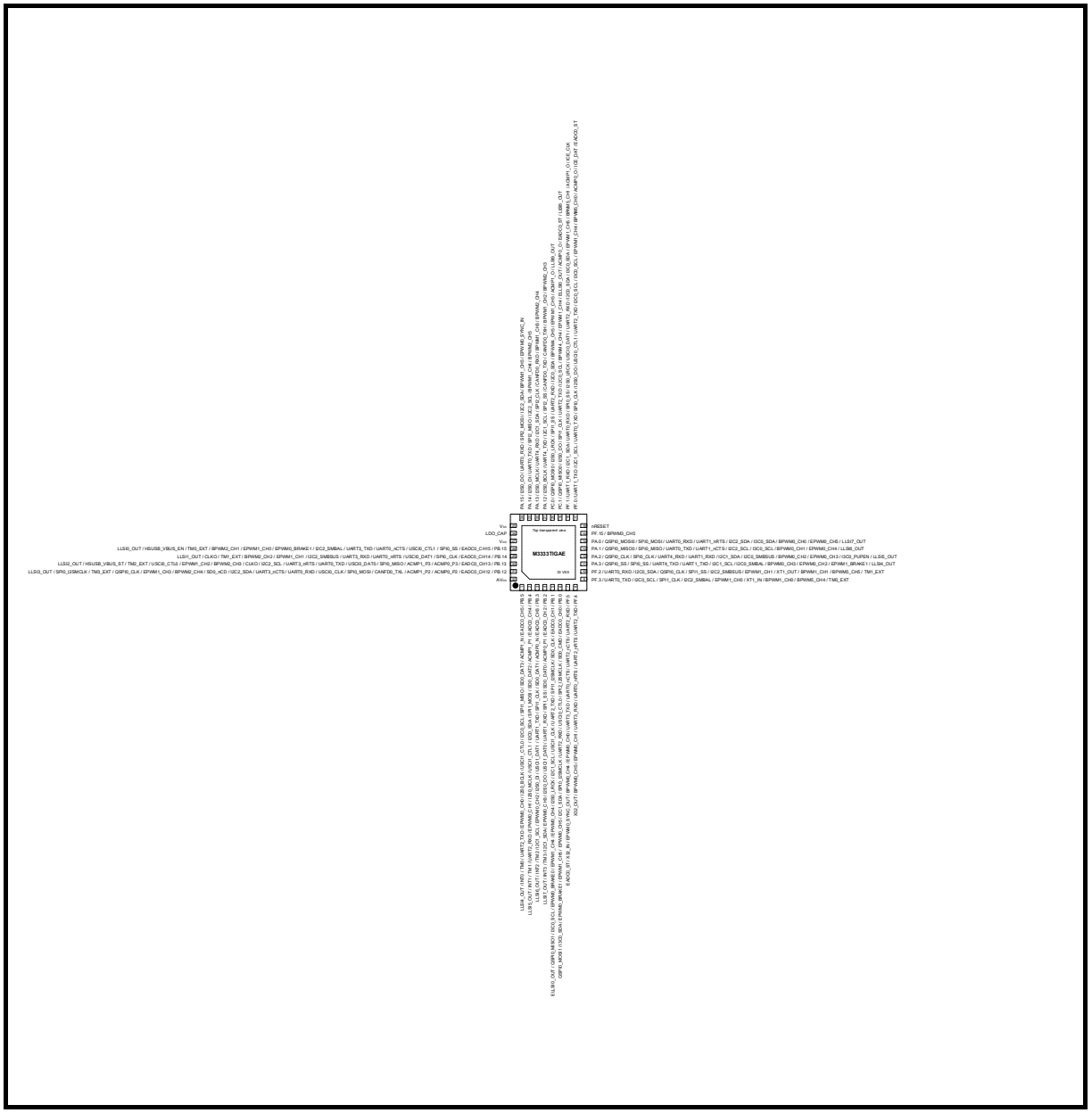


Figure 4.3-1 M3333TIGAE Multi-function Pin Diagram

Pin	Type	M3333TIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT

Pin	Type	M3333TIGAE Pin Function
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
8	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
9	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
10	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
11	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EPWM1_BRAKE1 / LLSI4_OUT
12	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
13	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
14	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
15	I/O	PF.15 / BPWM3_CH5
16	I	nRESET
17	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
18	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
19	I/O	PC.1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
20	I/O	PC.0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
21	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
22	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
23	I/O	PA.14 / I2S0_DI / UART0_TXD / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
24	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
25	P	V_{SS}

Pin	Type	M3333TIGAE Pin Function
26	A	LDO_CAP
27	P	V_{DD}
28	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
29	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
30	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
31	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
32	P	AV_{DD}
33	P	V_{SS}

Table 4.3-1 M3333TIGAE Multi-function Pin Table

4.3.1.2 M3333TGAAE

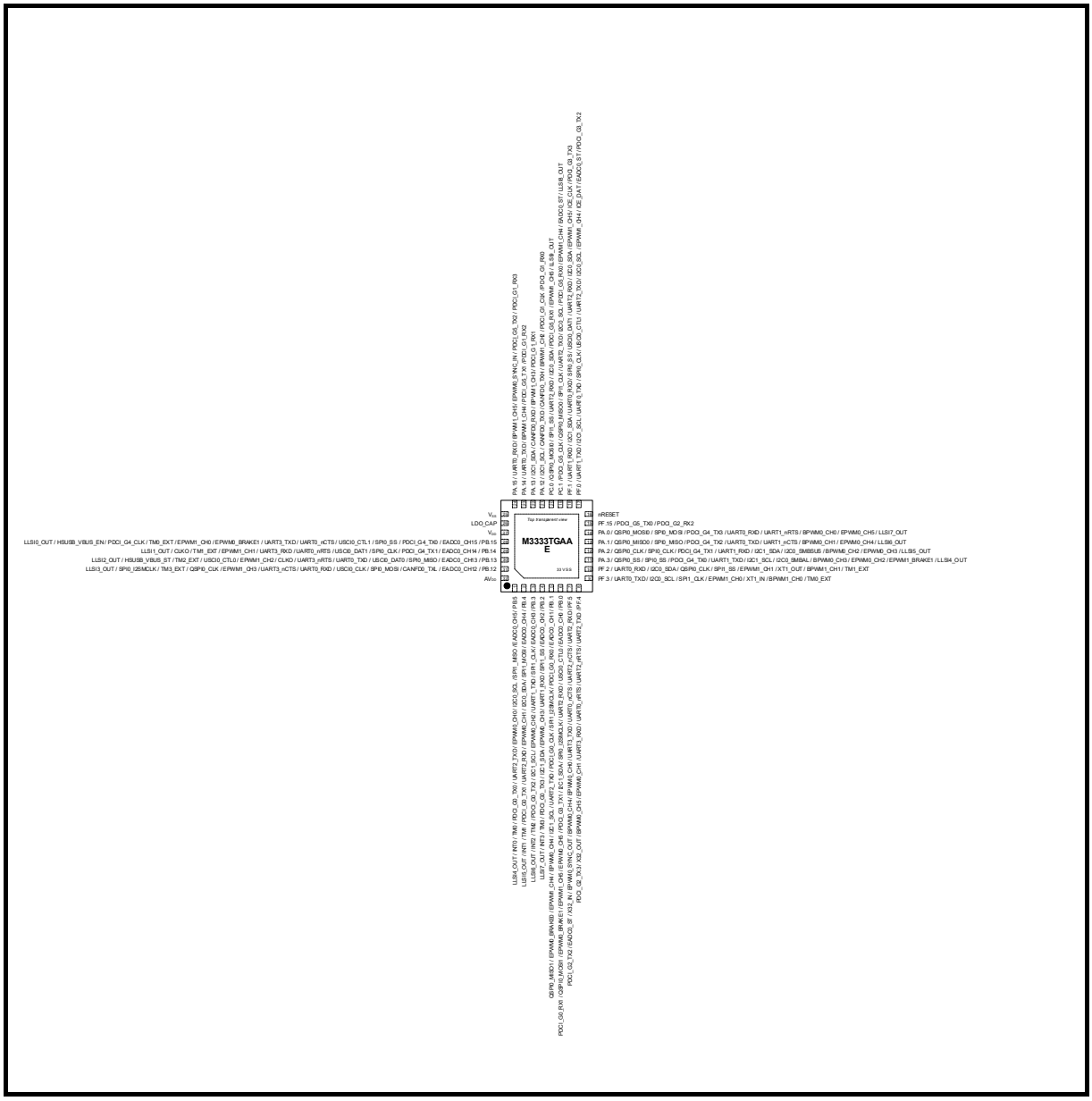


Figure 4.3-2 M3333TGAAE Multi-function Pin Diagram

Pin	Type	M3333TGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3333TGAAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
8	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
9	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
10	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
11	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EPWM1_BRAKE1 / LLSI4_OUT
12	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
13	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
14	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
15	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
16	I	nRESET
17	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
18	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
19	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
20	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT
21	I/O	PA.12 / I2C1_SCL / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / PDCI_G1_CLK / PDCI_G1_RX0
22	I/O	PA.13 / I2C1_SDA / CANFD0_RXD / BPWM1_CH3 / PDCI_G1_RX1
23	I/O	PA.14 / UART0_TXD / BPWM1_CH4 / PDCI_G5_TX1 / PDCI_G1_RX2
24	I/O	PA.15 / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / PDCI_G5_TX2 / PDCI_G1_RX3
25	P	V_{SS}
26	A	LDO_CAP
27	P	V_{DD}
28	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
29	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
30	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT

Pin	Type	M3333TGAAE Pin Function
31	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
32	P	AV_{DD}
33	P	V_{SS}

Table 4.3-2 M3333TGAAE Multi-function Pin Table

4.3.2 UQFN33-Pin Multi-function Pin Diagram

Corresponding Part Number: M3334TIGAE

4.3.2.1 M3334TIGAE

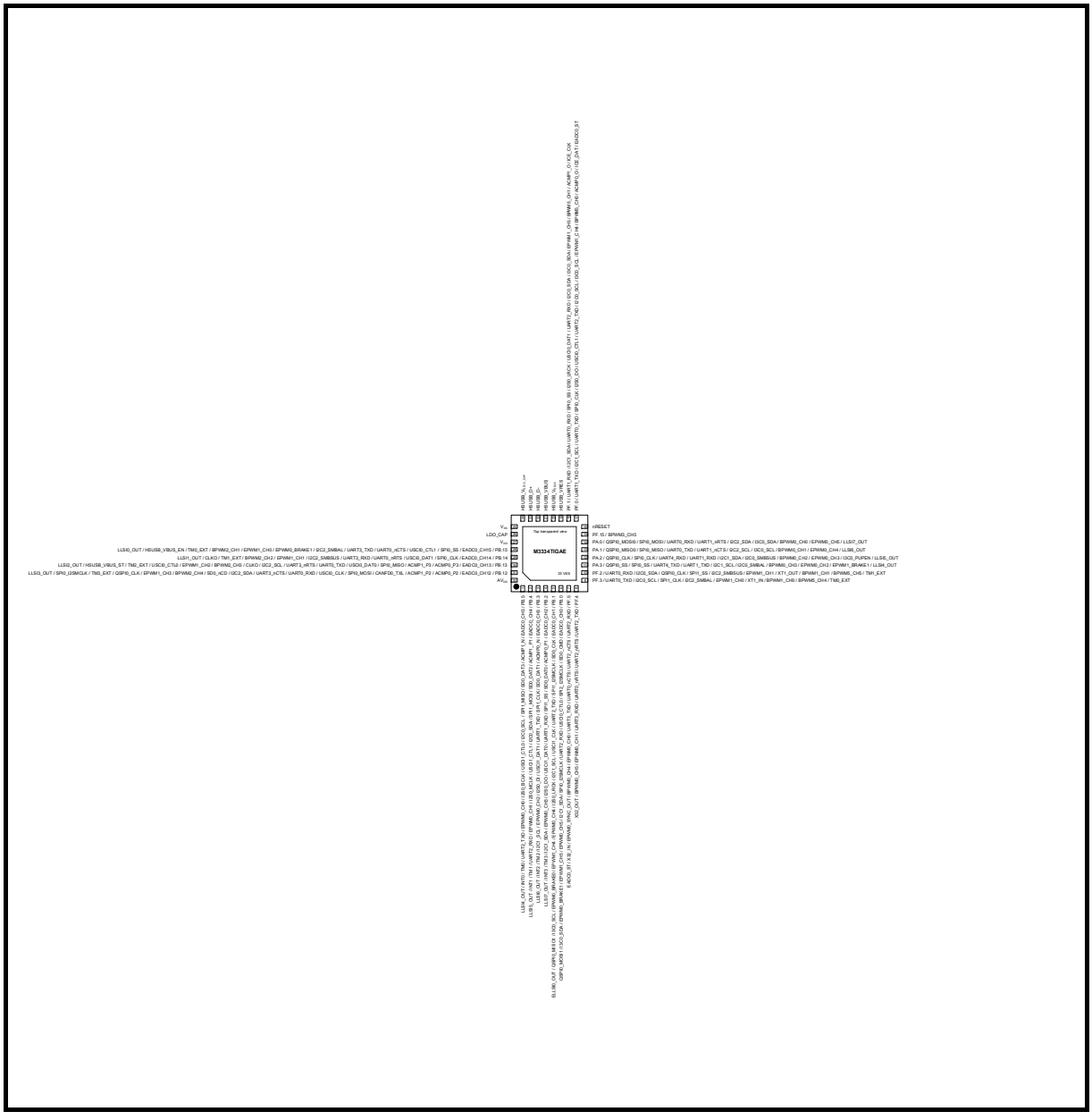


Figure -4.3-3 M3334TIGAE Multi-function Pin Diagram

Pin	Type	M3334TIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT

Pin	Type	M3334TIGAE Pin Function
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
8	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
9	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
10	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
11	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EPWM1_BRAKE1 / LLSI4_OUT
12	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
13	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
14	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
15	I/O	PF.15 / BPWM3_CH5
16	I	nRESET
17	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
18	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
19	A	HSUSB_VRES
20	P	HSUSB_VDD33
21	I/O	HSUSB_VBUS
22	A	HSUSB_D-
23	A	HSUSB_D+
24	A	HSUSB_VDD12_CAP
25	P	V_{SS}
26	A	LDO_CAP
27	P	V_{DD}
28	I/O	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT

Pin	Type	M3334TIGAE Pin Function
29	I/O	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
30	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
31	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
32	P	AV_{DD}
33	P	V_{SS}

Table 4.3-3 M3334TIGAE Multi-function Pin Table

4.3.2.2 M3334TGAAE

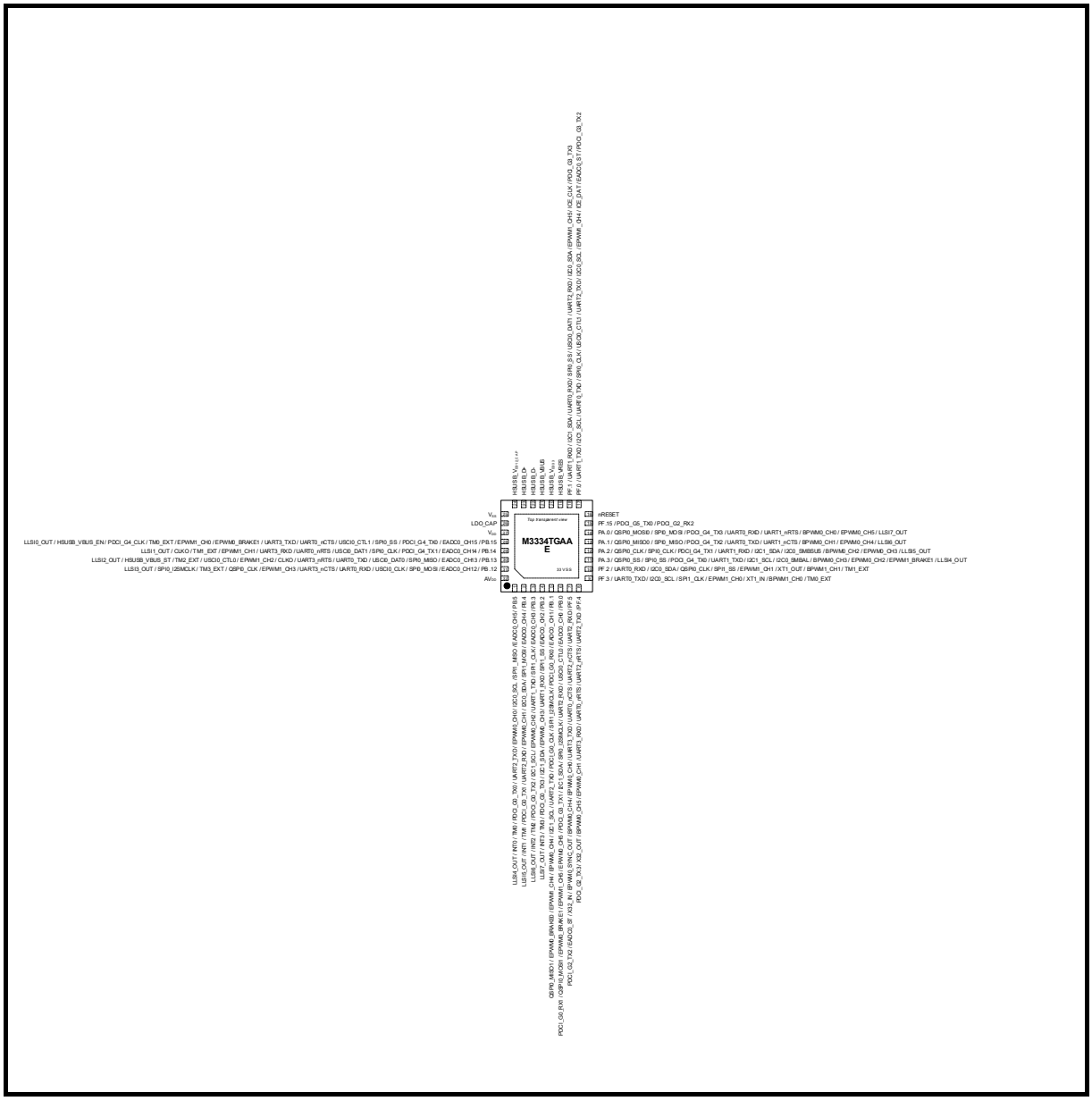


Figure 4.3-4 M3334TGAAE Multi-function Pin Diagram

Pin	Type	M3334TGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3334TGAAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
8	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
9	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
10	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
11	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EPWM1_BRAKE1 / LLSI4_OUT
12	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
13	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
14	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
15	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
16	I	nRESET
17	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
18	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
19	A	HSUSB_VRES
20	P	HSUSB_VDD33
21	I/O	HSUSB_VBUS
22	A	HSUSB_D-
23	A	HSUSB_D+
24	A	HSUSB_VDD12_CAP
25	P	V_{SS}
26	A	LDO_CAP
27	P	V_{DD}
28	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
29	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
30	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
31	I/O	PB.12 / EADC0_CH12 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 /

Pin	Type	M3334TGAAE Pin Function
		QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
32	P	AV_{DD}
33	P	V_{SS}

Table 4.3-4 M3334TGAAE Multi-function Pin Table

4.3.3 QFN48-Pin Multi-function Pin Diagram

Corresponding Part Number: M3333YIGAE

4.3.3.1 M3333YIGAE

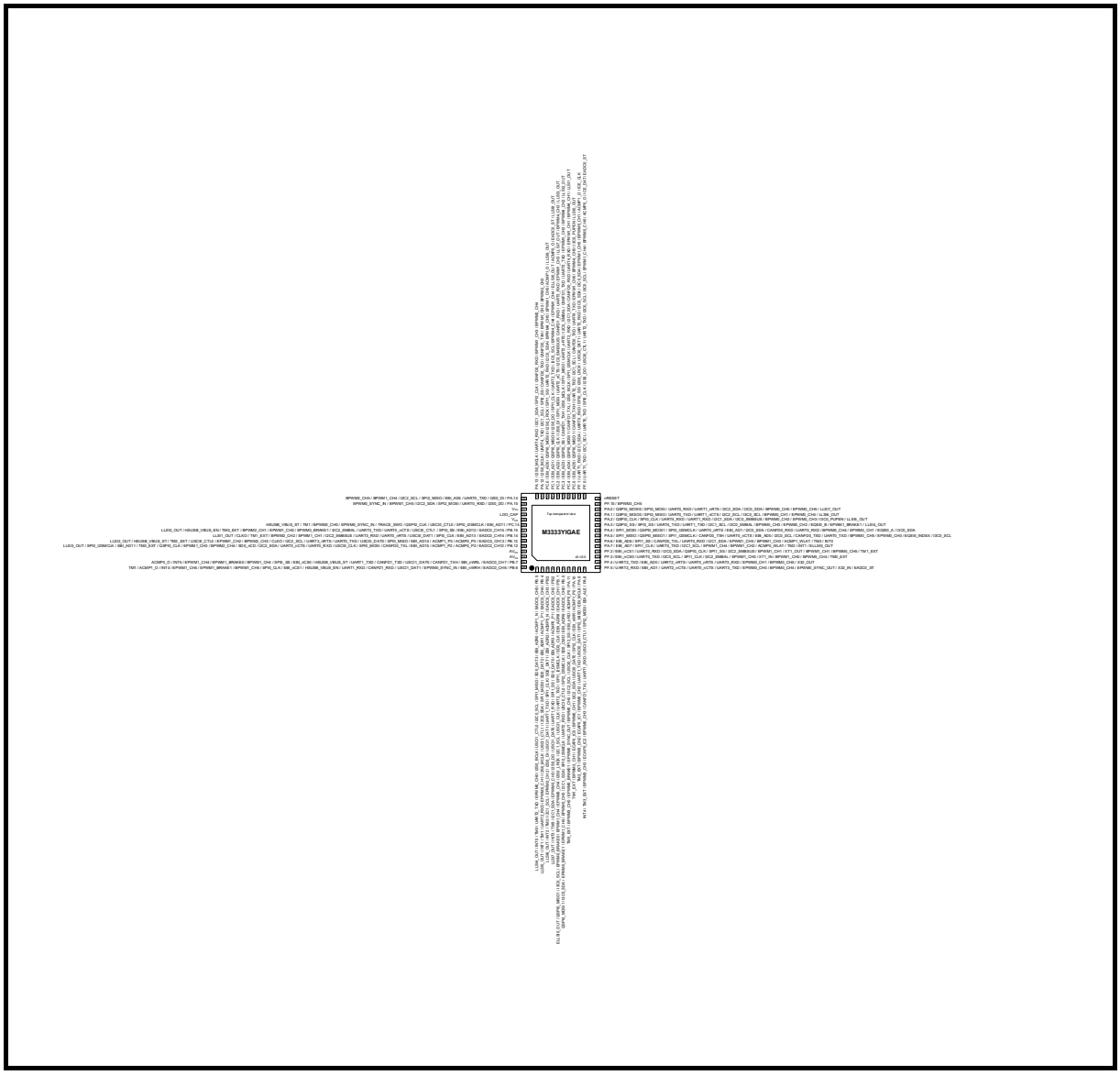


Figure 4.3-5 M3333YIGAE Multi-function Pin Diagram

Pin	Type	M3333YIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT

Pin	Type	M3333YIGAE Pin Function
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / BPWM3_CH5
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST

Pin	Type	M3333YIGAE Pin Function
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
27	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
28	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
29	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
30	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
31	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
32	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
33	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
34	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
35	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
36	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1

Pin	Type	M3333YIGAE Pin Function
49	P	V_{SS}

Table 4.3-5 M3333YIGAE Multi-function Pin Table

4.3.3.2 M3333YGAAE

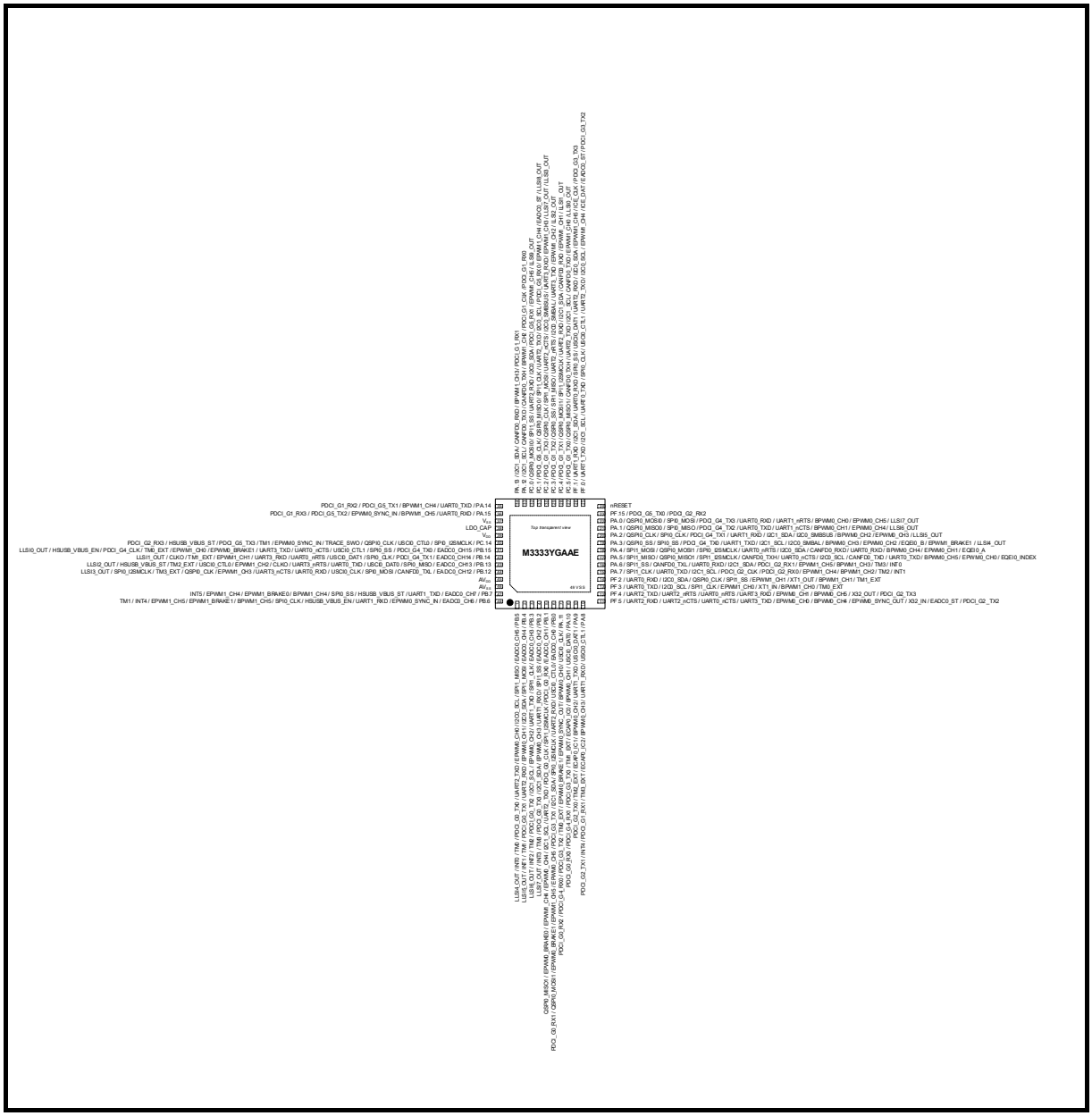


Figure 4.3-6 M3333YGAAE Multi-function Pin Diagram

Pin	Type	M3333YGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT

Pin	Type	M3333YGAAE Pin Function
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
8	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
10	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2

Pin	Type	M3333YGAAE Pin Function
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
27	I/O	PC.5 / PDCI_G1_TX0 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / EPWM1_CH0 / LLSI0_OUT
28	I/O	PC.4 / PDCI_G1_TX1 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / EPWM1_CH1 / LLSI1_OUT
29	I/O	PC.3 / PDCI_G1_TX2 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LLSI2_OUT
30	I/O	PC.2 / PDCI_G1_TX3 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / LLSI3_OUT
31	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
32	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT
33	I/O	PA.12 / I2C1_SCL / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / PDCI_G1_CLK / PDCI_G1_RX0
34	I/O	PA.13 / I2C1_SDA / CANFD0_RXD / BPWM1_CH3 / PDCI_G1_RX1
35	I/O	PA.14 / UART0_TXD / BPWM1_CH4 / PDCI_G5_TX1 / PDCI_G1_RX2
36	I/O	PA.15 / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / PDCI_G5_TX2 / PDCI_G1_RX3
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
41	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5
48	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1
49	P	V_{SS}

Table 4.3-6 M3333YGAAE Multi-function Pin Table

4.3.4 UQFN48-Pin Multi-function Pin Diagram

Corresponding Part Number: M3334YIGAE

4.3.4.1 M3334YIGAE

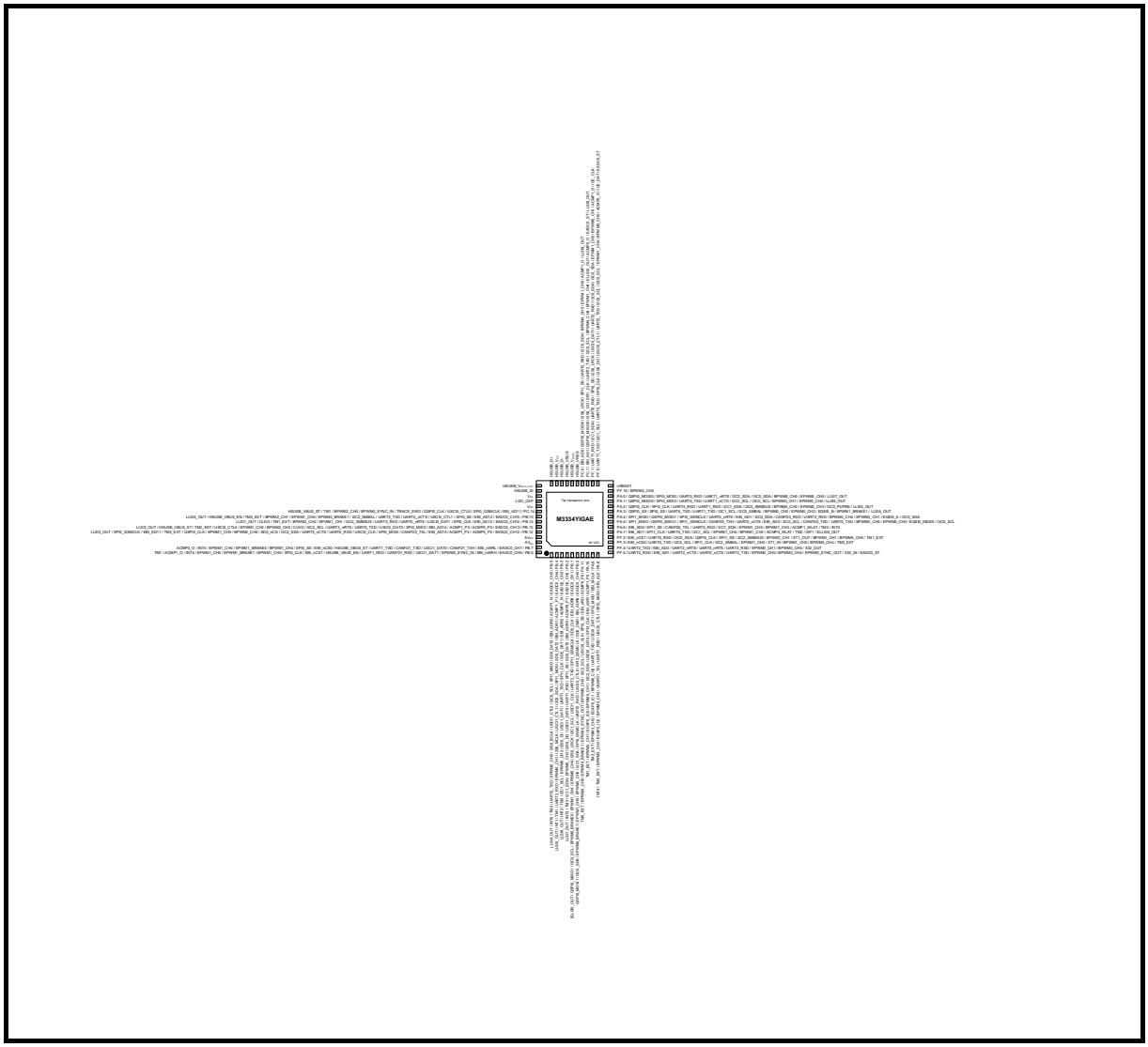


Figure 4.3-7 M3334YIGAE Multi-function Pin Diagram

Pin	Type	M3334YIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3334YIGAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / BPWM3_CH5
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK

Pin	Type	M3334YIGAE Pin Function
27	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
28	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
29	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
30	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
31	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
32	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
33	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
34	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
35	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
36	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1
49	P	V_{SS}

Table 4.3-7 M3334YIGAE Multi-function Pin Table

4.3.4.2 M3334YGAAE

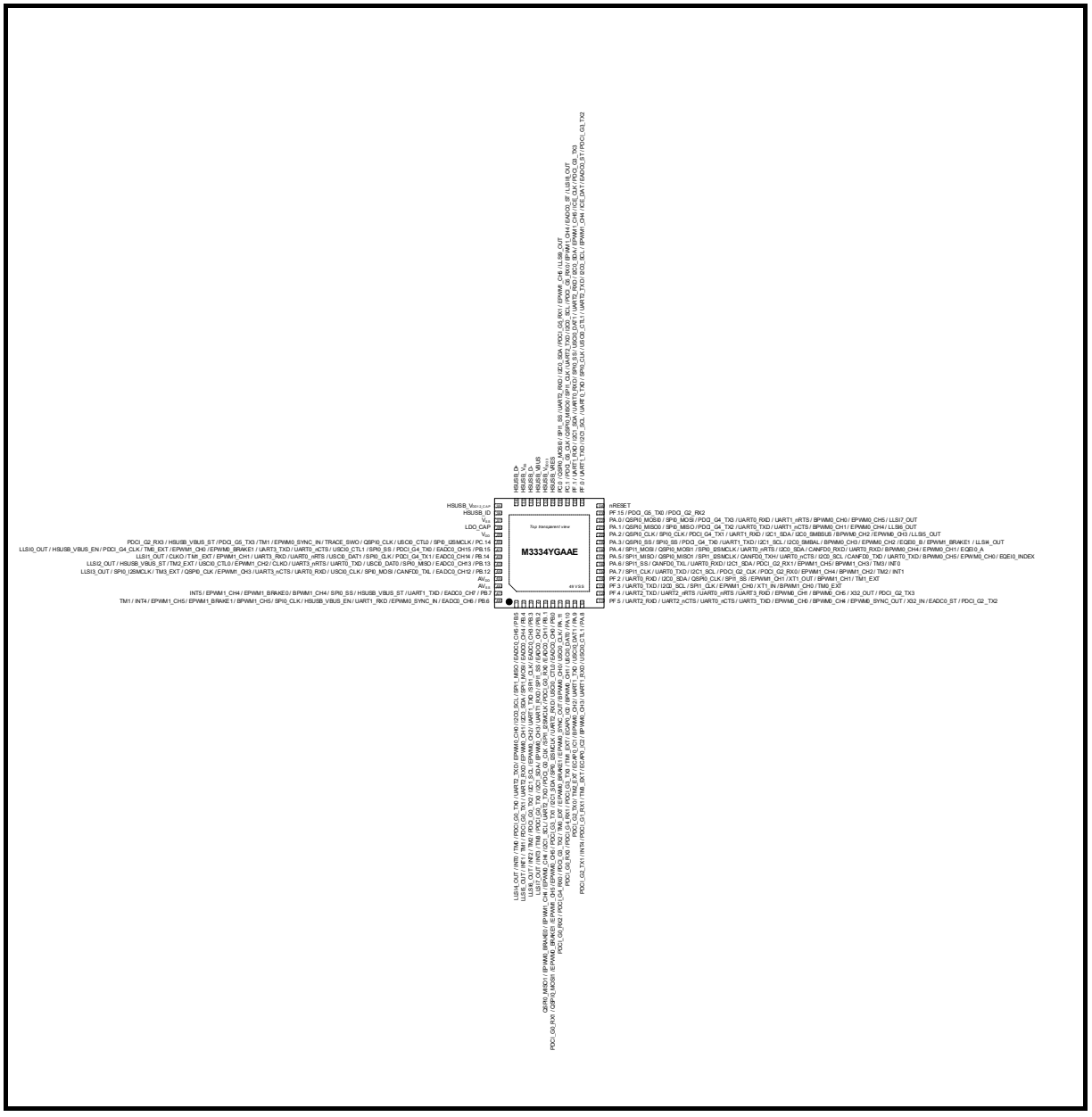


Figure 4.3-8 M3334YGAAE Multi-function Pin Diagram

Pin	Type	M3334YGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3334YGAAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
8	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
10	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
27	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
28	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT

Pin	Type	M3334YGAAE Pin Function
29	A	HSUSB_VRES
30	P	HSUSB_VDD33
31	I/O	HSUSB_VBUS
32	A	HSUSB_D-
33	P	HSUSB_VSS
34	A	HSUSB_D+
35	A	HSUSB_VDD12_CAP
36	I	HSUSB_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
41	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5
48	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1
49	P	V_{SS}

Table 4.3-8 M3334YGAAE Multi-function Pin Table

4.3.5 LQFP48-Pin Multi-function Pin Diagram

Corresponding Part Number: M3333LIGAE

4.3.5.1 M3333LIGAE

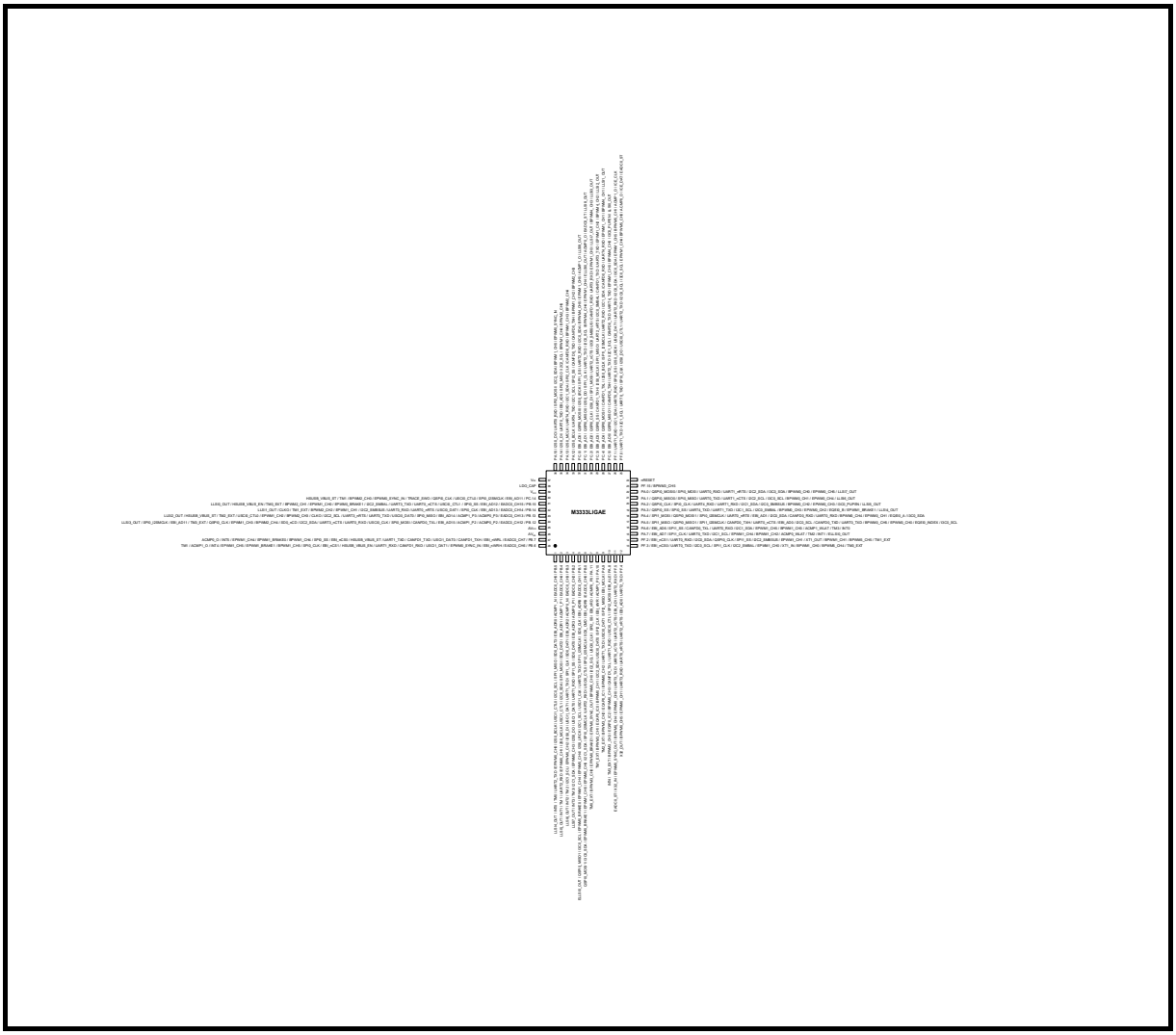


Figure 4.3-9 M3333LIGAE Multi-function Pin Diagram

Pin	Type	M3333LIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL /

Pin	Type	M3333LIGAE Pin Function
		QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / BPWM3_CH5
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
27	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT

Pin	Type	M3333LIGAE Pin Function
28	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
29	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
30	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
31	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
32	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
33	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
34	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
35	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
36	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1

Table 4.3-9 M3333LIGAE Multi-function Pin Table

4.3.5.2 M3333LGAAE

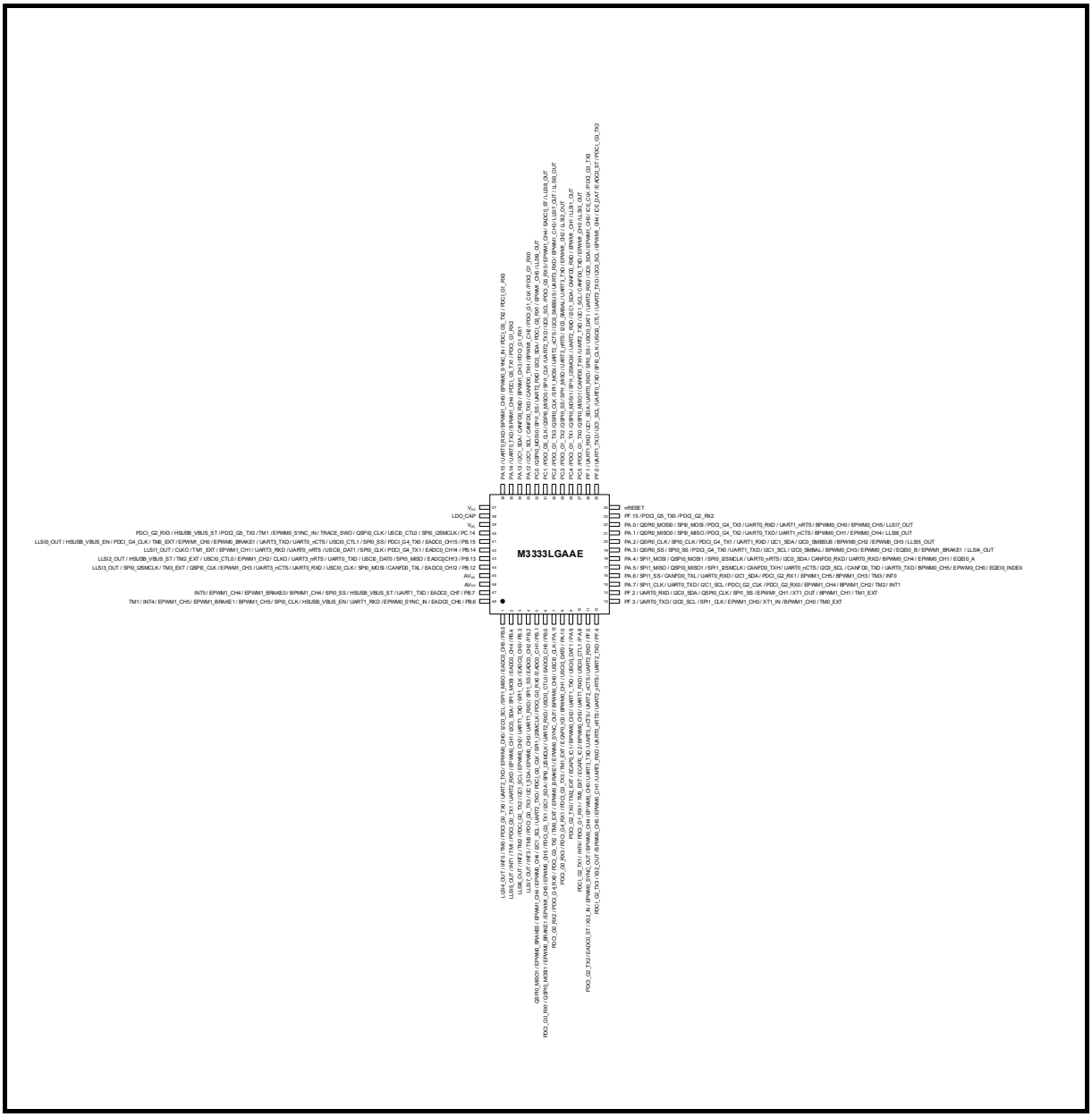


Figure4.3-10 M3333LGAAE Multi-function Pin Diagram

Pin	Type	M3333LGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3333LGAAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
8	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
10	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
27	I/O	PC.5 / PDCI_G1_TX0 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / EPWM1_CH0 / LLSI0_OUT
28	I/O	PC.4 / PDCI_G1_TX1 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / EPWM1_CH1 / LLSI1_OUT

Pin	Type	M3333LGAAE Pin Function
29	I/O	PC.3 / PDCI_G1_TX2 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LLSI2_OUT
30	I/O	PC.2 / PDCI_G1_TX3 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / LLSI3_OUT
31	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
32	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT
33	I/O	PA.12 / I2C1_SCL / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / PDCI_G1_CLK / PDCI_G1_RX0
34	I/O	PA.13 / I2C1_SDA / CANFD0_RXD / BPWM1_CH3 / PDCI_G1_RX1
35	I/O	PA.14 / UART0_TXD / BPWM1_CH4 / PDCI_G5_TX1 / PDCI_G1_RX2
36	I/O	PA.15 / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / PDCI_G5_TX2 / PDCI_G1_RX3
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
41	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5
48	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1

Table 4.3-10 M3333LGAAE Multi-function Pin Table

4.3.6 ULQFP48-Pin Multi-function Pin Diagram

Corresponding Part Number: M3334LIGAE

4.3.6.1 M3334LIGAE

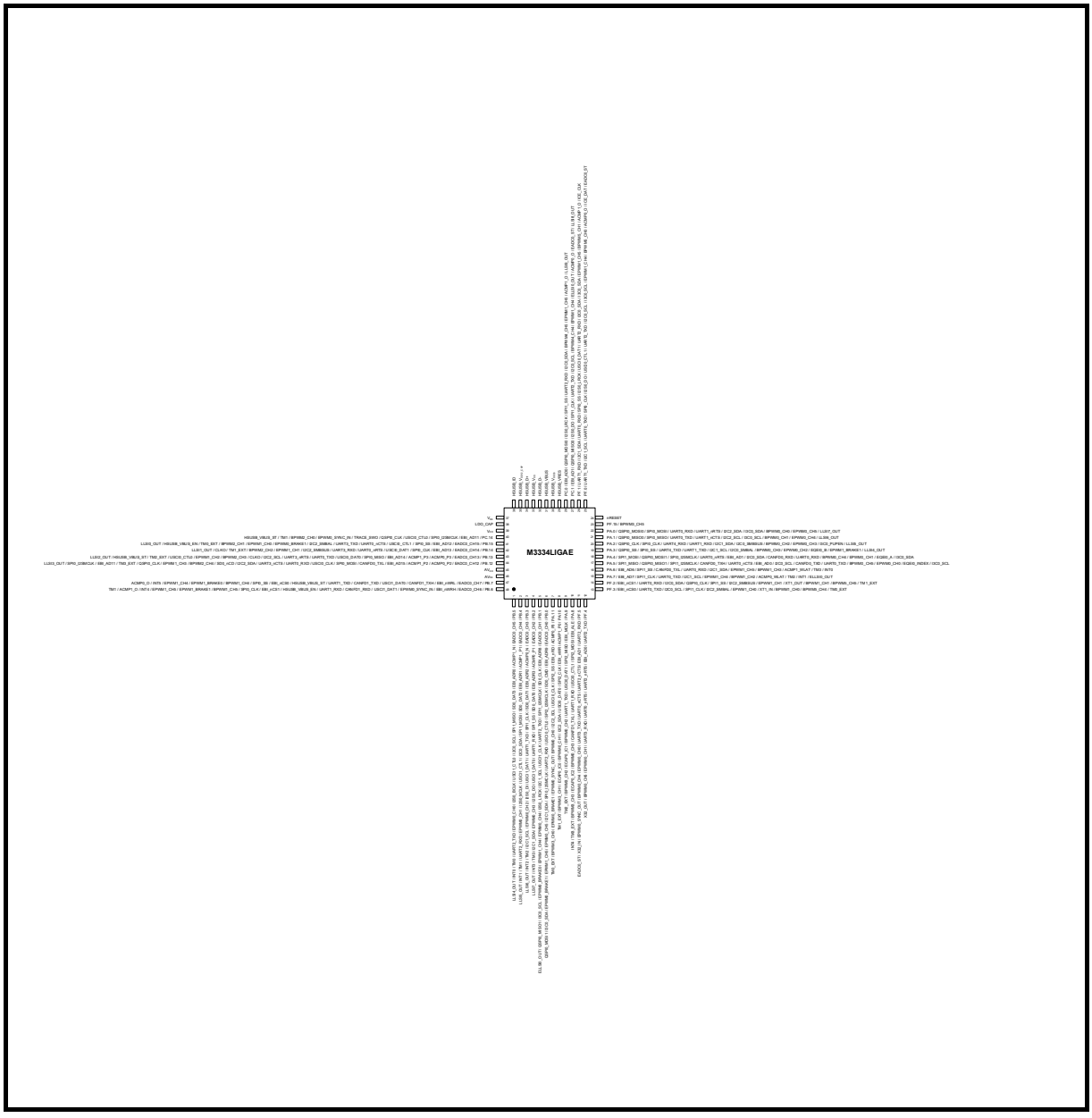


Figure4.3-11 M3334LIGAE Multi-function Pin Diagram

Pin	Type	M3334LIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT

Pin	Type	M3334LIGAE Pin Function
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / BPWM3_CH5
24	I	nRESET

Pin	Type	M3334LIGAE Pin Function
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
27	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
28	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
29	A	HSUSB_VRES
30	P	HSUSB_VDD33
31	I/O	HSUSB_VBUS
32	A	HSUSB_D-
33	P	HSUSB_VSS
34	A	HSUSB_D+
35	A	HSUSB_VDD12_CAP
36	I	HSUSB_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1

Table 4.3-11 M3334LIGAE Multi-function Pin Table

4.3.6.2 M3334LGAAE

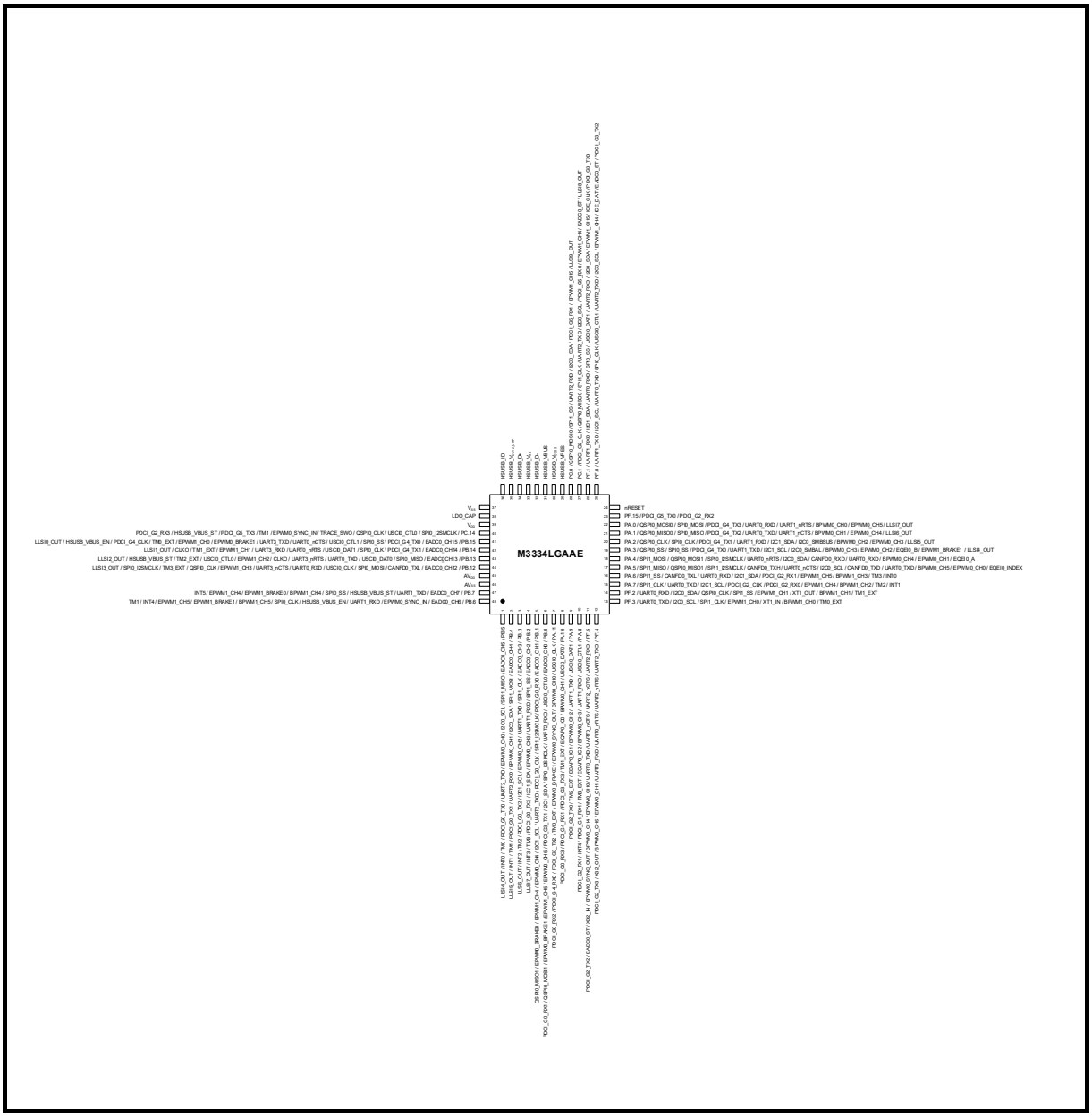


Figure4.3-12 M3334LGAAE Multi-function Pin Diagram

Pin	Type	M3334LGAAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT

Pin	Type	M3334LGAAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
6	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
7	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
8	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
9	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
10	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
11	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
12	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
13	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
14	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
15	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
16	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
17	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
23	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
27	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
28	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT

Pin	Type	M3334LGAAE Pin Function
29	A	HSUSB_VRES
30	P	HSUSB_VDD33
31	I/O	HSUSB_VBUS
32	A	HSUSB_D-
33	P	HSUSB_VSS
34	A	HSUSB_D+
35	A	HSUSB_VDD12_CAP
36	I	HSUSB_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
41	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
42	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
43	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
44	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5
48	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1

Table 4.3-12 M3334LGAAE Multi-function Pin Table

4.3.7 LQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M3333SIGAE

4.3.7.1 M3333SIGAE

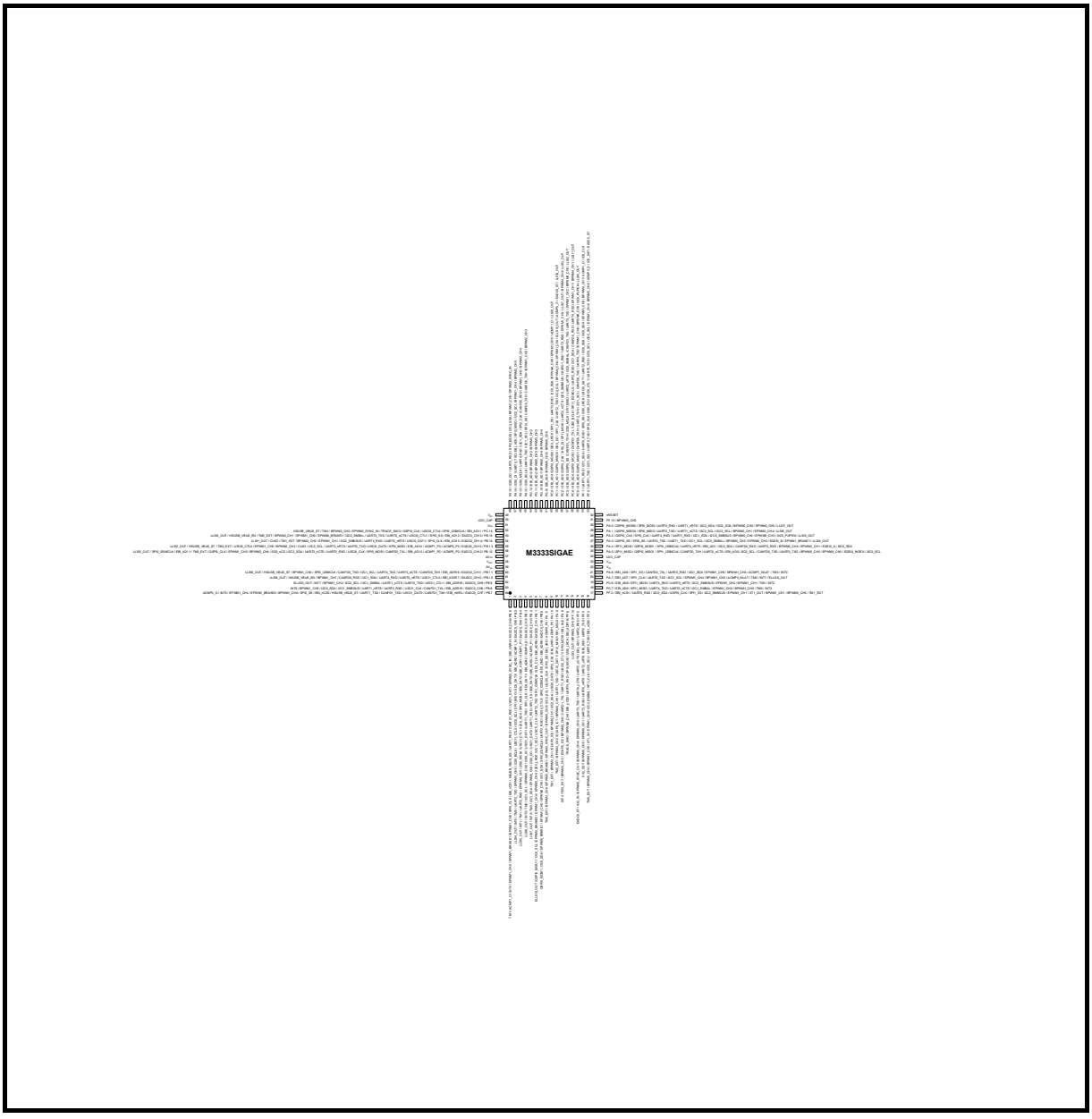


Figure 4.3-13 M3333SIGAE Multi-function Pin Diagram

Pin	Type	M3333SIGAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT

Pin	Type	M3333SIGAE Pin Function
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
6	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
7	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
8	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
10	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
11	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / BPWM3_CH4 / TRACE_SWO
13	I/O	PF.14 / BPWM3_CH5 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
18	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
21	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL

Pin	Type	M3333SIGAE Pin Function
26	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
31	I/O	PF.15 / BPWM3_CH5
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
35	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
36	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
37	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
38	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
39	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
40	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
41	I/O	PG.9 / EBI_AD0 / BPWM0_CH5 / BPWM5_CH5
42	I/O	PG.10 / EBI_AD1 / BPWM0_CH4 / BPWM5_CH4
43	I/O	PG.11 / EBI_AD2 / BPWM0_CH3 / BPWM5_CH3
44	I/O	PG.12 / EBI_AD3 / BPWM0_CH2 / BPWM5_CH2
45	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
46	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
47	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
48	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}

Pin	Type	M3333SIGAE Pin Function
52	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
53	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
54	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / CANFD0_TXH / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
61	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
62	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7 / ELLSI0_OUT
63	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
64	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O

Figure 4.3-14 M3333SIGAE Multi-function Pin Table

4.3.7.2 M3333SGAAE

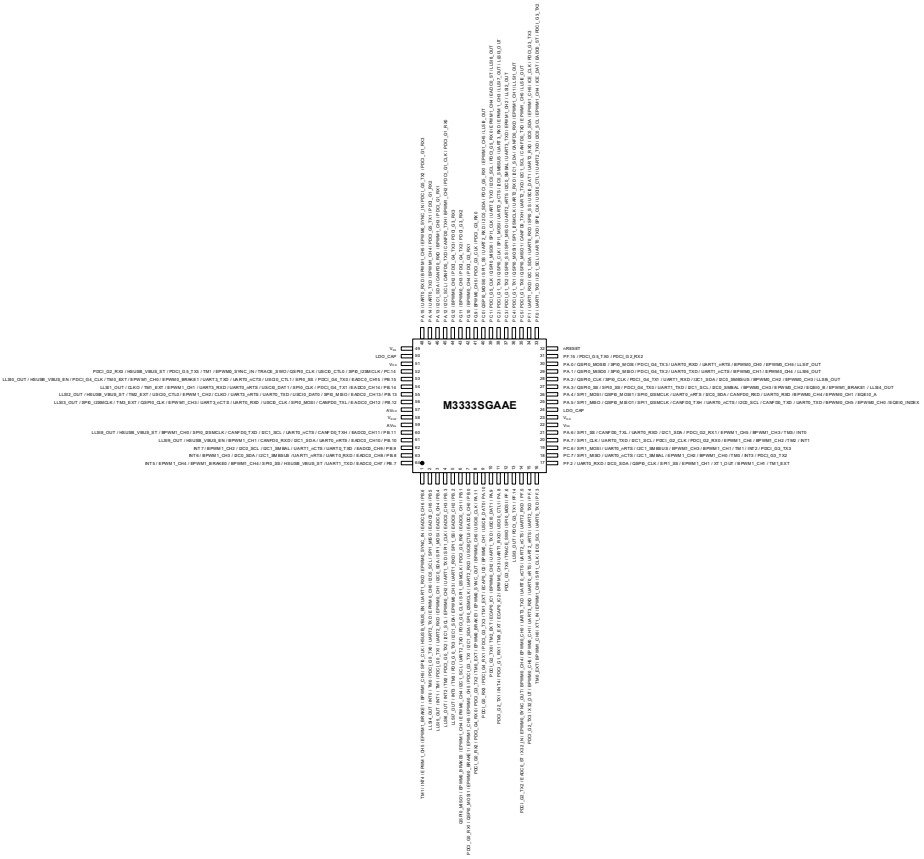


Figure 4.3-15 M3333SGAAE Multi-function Pin Diagram

Pin	Type	M3333SGAAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1
2	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
3	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
4	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT

Pin	Type	M3333SGAAE Pin Function
5	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT
6	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
7	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
8	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
9	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
12	I/O	PF.6 / SPI0_MOSI / TRACE_SWO / PDCI_G3_TX0
13	I/O	PF.14 / PDCI_G3_TX1 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
18	I/O	PC.7 / SPI1_MISO / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / PDCI_G3_TX2
19	I/O	PC.6 / SPI1_MOSI / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / PDCI_G3_TX3
20	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
26	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT

Pin	Type	M3333SGAAE Pin Function
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
31	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
35	I/O	PC.5 / PDCI_G1_TX0 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / EPWM1_CH0 / LLSI0_OUT
36	I/O	PC.4 / PDCI_G1_TX1 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / EPWM1_CH1 / LLSI1_OUT
37	I/O	PC.3 / PDCI_G1_TX2 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LLSI2_OUT
38	I/O	PC.2 / PDCI_G1_TX3 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / LLSI3_OUT
39	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
40	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT
41	I/O	PG.9 / BPWM0_CH5 / PDCI_G3_CLK / PDCI_G3_RX0
42	I/O	PG.10 / BPWM0_CH4 / PDCI_G3_RX1
43	I/O	PG.11 / BPWM0_CH3 / PDCI_G4_TX2 / PDCI_G3_RX2
44	I/O	PG.12 / BPWM0_CH2 / PDCI_G4_TX3 / PDCI_G3_RX3
45	I/O	PA.12 / I2C1_SCL / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / PDCI_G1_CLK / PDCI_G1_RX0
46	I/O	PA.13 / I2C1_SDA / CANFD0_RXD / BPWM1_CH3 / PDCI_G1_RX1
47	I/O	PA.14 / UART0_TXD / BPWM1_CH4 / PDCI_G5_TX1 / PDCI_G1_RX2
48	I/O	PA.15 / UART0_RXD / BPWM1_CH5 / EPWM0_SYNC_IN / PDCI_G5_TX2 / PDCI_G1_RX3
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
53	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
54	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
55	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
56	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT

Pin	Type	M3333SGAAE Pin Function
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / CANFD0_TXH / UART0_nCTS / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5

Table 4.3-13 M3333SGAAE Multi-function Pin Table

4.3.8 ULQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M3334SIGAE

4.3.8.1 M3334SIGAE

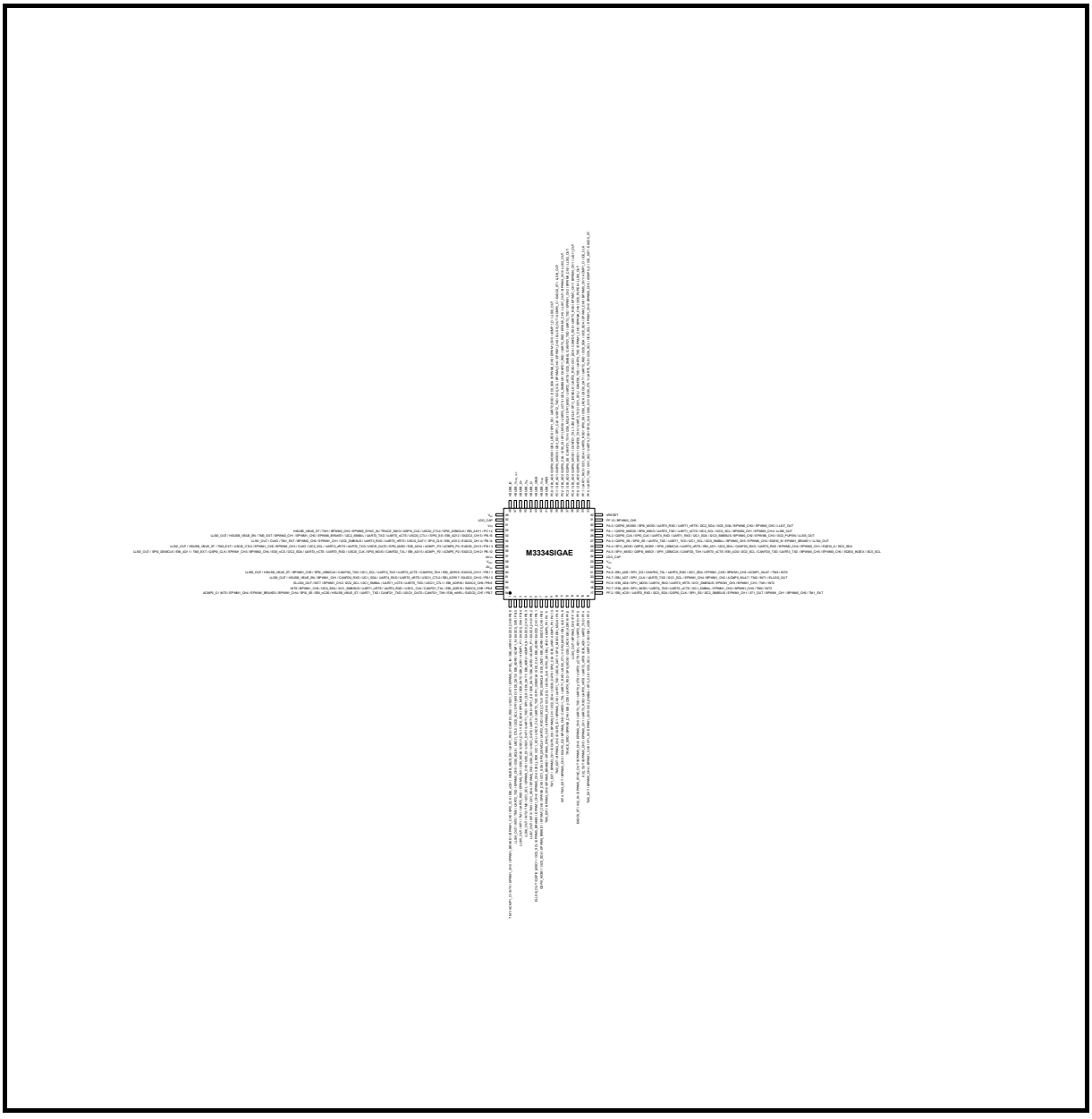


Figure 4.3-16 M3334SIGAE Multi-function Pin Diagram

Pin	Type	M3334SIGAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT

Pin	Type	M3334SIGAE Pin Function
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1 / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
6	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
7	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
8	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
10	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
11	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / BPWM3_CH4 / TRACE_SWO
13	I/O	PF.14 / BPWM3_CH5 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
15	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
18	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3
19	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2
20	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
21	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL

Pin	Type	M3334SIGAE Pin Function
26	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
31	I/O	PF.15 / BPWM3_CH5
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
35	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
36	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
37	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
38	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
39	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
40	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
41	A	HSUSB_VRES
42	P	HSUSB_VDD33
43	I/O	HSUSB_VBUS
44	A	HSUSB_D-
45	P	HSUSB_VSS
46	A	HSUSB_D+
47	A	HSUSB_VDD12_CAP
48	I	HSUSB_ID
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST

Pin	Type	M3334SIGAE Pin Function
53	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
54	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / CANFD0_TXH / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
61	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
62	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7 / ELLSI0_OUT
63	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
64	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O

Table 4.3-14 M3334SIGAE Multi-function Pin Table

4.3.8.2 M3334SGAAE

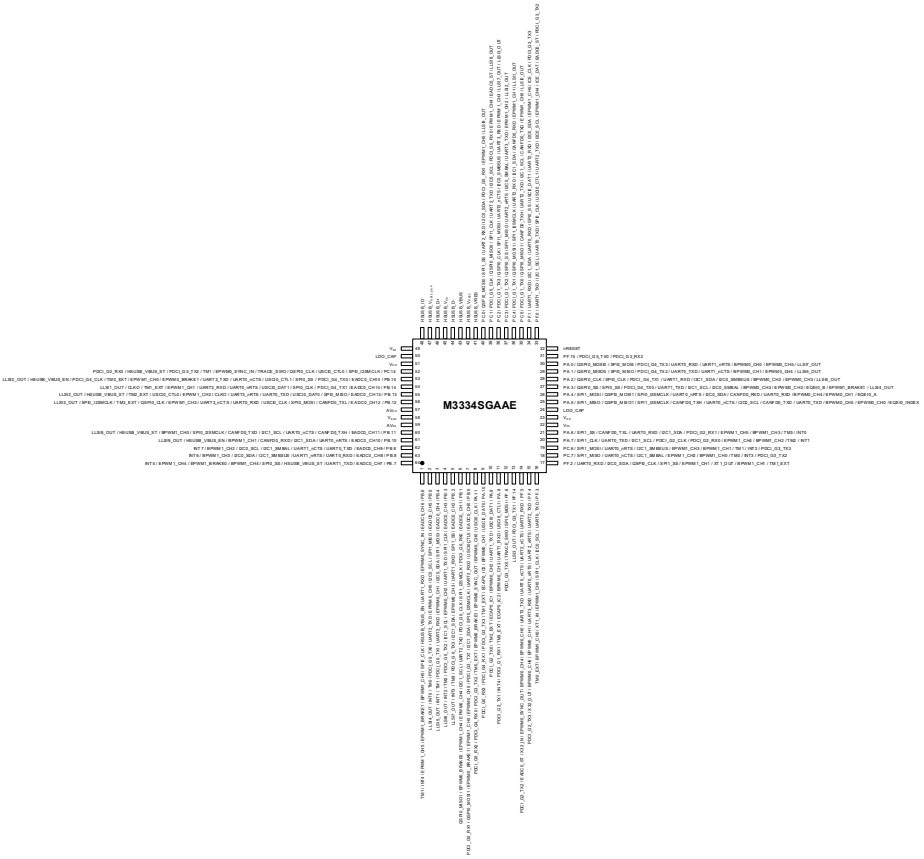


Figure 4.3-17 M3334SGAAE Multi-function Pin Diagram

Pin	Type	M3334SGAAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EPWM0_SYNC_IN / UART1_RXD / HSUSB_VBUS_EN / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / TM1
2	I/O	PB.5 / EADC0_CH5 / SPI1_MISO / I2C0_SCL / EPWM0_CH0 / UART2_TXD / PDCI_G0_TX0 / TM0 / INT0 / LLSI4_OUT
3	I/O	PB.4 / EADC0_CH4 / SPI1_MOSI / I2C0_SDA / EPWM0_CH1 / UART2_RXD / PDCI_G0_TX1 / TM1 / INT1 / LLSI5_OUT
4	I/O	PB.3 / EADC0_CH3 / SPI1_CLK / UART1_TXD / EPWM0_CH2 / I2C1_SCL / PDCI_G0_TX2 / TM2 / INT2 / LLSI6_OUT

Pin	Type	M3334SGAAE Pin Function
5	I/O	PB.2 / EADC0_CH2 / SPI1_SS / UART1_RXD / EPWM0_CH3 / I2C1_SDA / PDCI_G0_TX3 / TM3 / INT3 / LLSI7_OUT
6	I/O	PB.1 / EADC0_CH1 / PDCI_G0_RX0 / SPI1_I2SMCLK / PDCI_G0_CLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1
7	I/O	PB.0 / EADC0_CH0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / PDCI_G3_TX1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / PDCI_G0_RX1
8	I/O	PA.11 / USCI0_CLK / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / TM0_EXT / PDCI_G3_TX2 / PDCI_G4_RX0 / PDCI_G0_RX2
9	I/O	PA.10 / USCI0_DAT0 / BPWM0_CH1 / ECAP0_IC0 / TM1_EXT / PDCI_G3_TX3 / PDCI_G4_RX1 / PDCI_G0_RX3
10	I/O	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / TM2_EXT / PDCI_G2_TX0
11	I/O	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / ECAP0_IC2 / TM3_EXT / PDCI_G1_RX1 / INT4 / PDCI_G2_TX1
12	I/O	PF.6 / SPI0_MOSI / TRACE_SWO / PDCI_G3_TX0
13	I/O	PF.14 / PDCI_G3_TX1 / LLSI3_OUT
14	I/O	PF.5 / UART2_RXD / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / PDCI_G2_TX2
15	I/O	PF.4 / UART2_TXD / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / PDCI_G2_TX3
16	I/O	PF.3 / UART0_TXD / I2C0_SCL / SPI1_CLK / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / TM0_EXT
17	I/O	PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / TM1_EXT
18	I/O	PC.7 / SPI1_MISO / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / PDCI_G3_TX2
19	I/O	PC.6 / SPI1_MOSI / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / PDCI_G3_TX3
20	I/O	PA.7 / SPI1_CLK / UART0_TXD / I2C1_SCL / PDCI_G2_CLK / PDCI_G2_RX0 / EPWM1_CH4 / BPWM1_CH2 / TM2 / INT1
21	I/O	PA.6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / PDCI_G2_RX1 / EPWM1_CH5 / BPWM1_CH3 / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
26	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / I2C0_SDA / CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / PDCI_G4_TX0 / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / PDCI_G4_TX1 / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / LLSI5_OUT
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / PDCI_G4_TX2 / UART0_TXD / UART1_nCTS / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT

Pin	Type	M3334SGAAE Pin Function
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / PDCI_G4_TX3 / UART0_RXD / UART1_nRTS / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
31	I/O	PF.15 / PDCI_G5_TX0 / PDCI_G2_RX2
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / USCI0_CTL1 / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ICE_DAT / EADC0_ST / PDCI_G3_TX2
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / USCI0_DAT1 / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ICE_CLK / PDCI_G3_TX3
35	I/O	PC.5 / PDCI_G1_TX0 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / EPWM1_CH0 / LLSI0_OUT
36	I/O	PC.4 / PDCI_G1_TX1 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / EPWM1_CH1 / LLSI1_OUT
37	I/O	PC.3 / PDCI_G1_TX2 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / LLSI2_OUT
38	I/O	PC.2 / PDCI_G1_TX3 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / LLSI3_OUT
39	I/O	PC.1 / PDCI_G5_CLK / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / PDCI_G5_RX0 / EPWM1_CH4 / EADC0_ST / LLSI8_OUT
40	I/O	PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / PDCI_G5_RX1 / EPWM1_CH5 / LLSI9_OUT
41	A	HSUSB_VRES
42	P	HSUSB_VDD33
43	I/O	HSUSB_VBUS
44	A	HSUSB_D-
45	P	HSUSB_VSS
46	A	HSUSB_D+
47	A	HSUSB_VDD12_CAP
48	I	HSUSB_ID
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1 / PDCI_G5_TX3 / HSUSB_VBUS_ST / PDCI_G2_RX3
53	I/O	PB.15 / EADC0_CH15 / PDCI_G4_TX0 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PDCI_G4_CLK / HSUSB_VBUS_EN / LLSI0_OUT
54	I/O	PB.14 / EADC0_CH14 / PDCI_G4_TX1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EPWM1_CH1 / TM1_EXT / CLKO / LLSI1_OUT
55	I/O	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CLKO / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
56	I/O	PB.12 / EADC0_CH12 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / SPI0_I2SMCLK / LLSI3_OUT

Pin	Type	M3334SGAAE Pin Function
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / CANFD0_TXH / UART0_nCTS / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
61	I/O	PB.10 / EADC0_CH10 / UART0_nRTS / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
62	I/O	PB.9 / EADC0_CH9 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7
63	I/O	PB.8 / EADC0_CH8 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
64	I/O	PB.7 / EADC0_CH7 / UART1_TXD / HSUSB_VBUS_ST / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5

Table 4.3-15 M3334SGAAE Multi-function Pin Table

4.3.9 LQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M3333KIGAE

4.3.9.1 M3333KIGAE

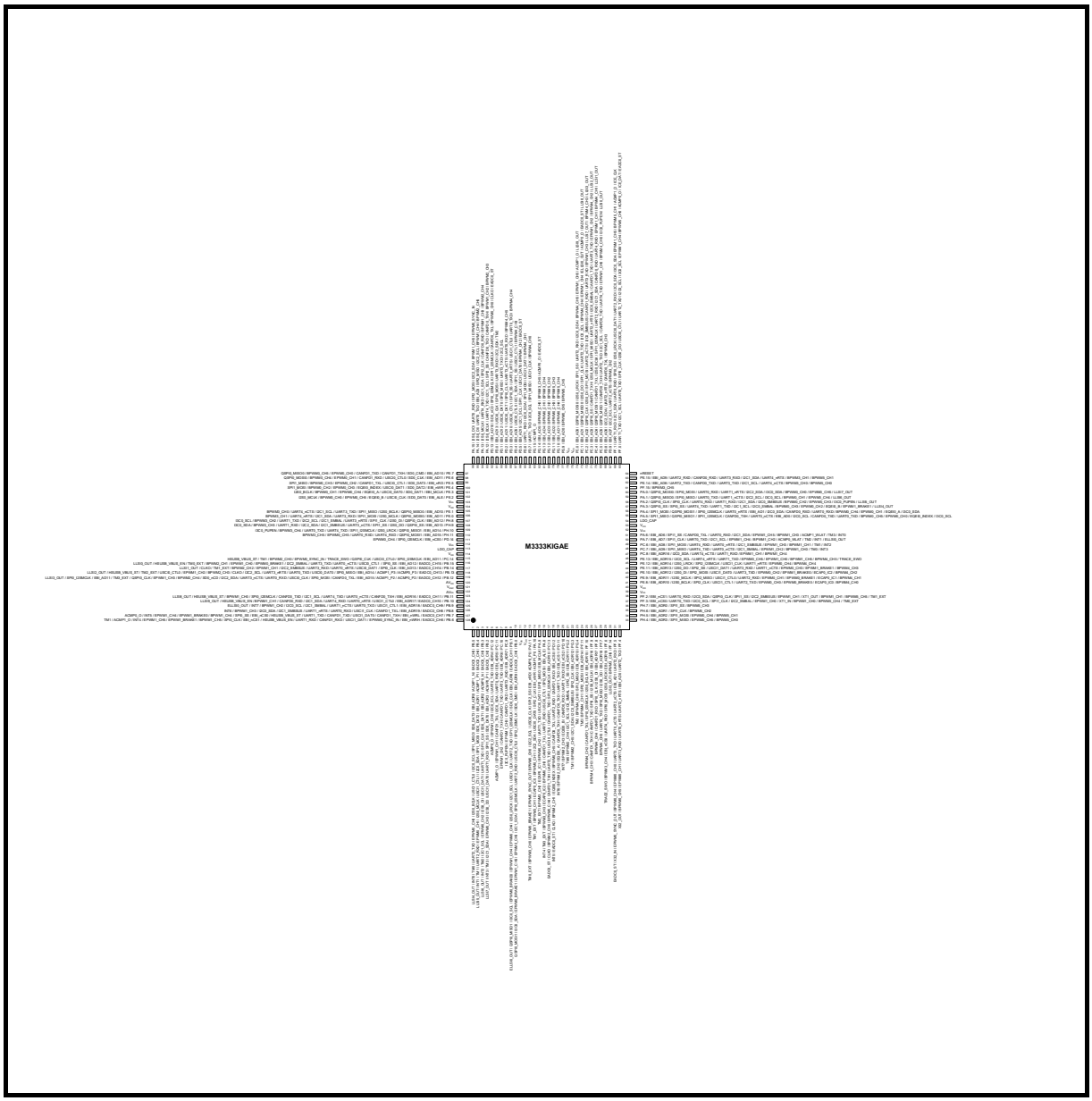


Figure 4.3-18 M3333KIGAE Multi-function Pin Diagram

Pin	Type	M3333KIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1

Pin	Type	M3333KIGAE Pin Function
		/ I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / CANFD1_TXL / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EPWM1_CH2
8	I/O	PC.9 / EBI_ADR7 / UART3_RXD / CANFD1_RXD / EPWM1_CH3 / I3C0_PUPEN
9	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
10	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
14	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
15	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
16	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
17	I/O	PC.13 / EBI_ADR10 / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / CANFD1_TXH / BPWM0_CH4 / BPWM2_CH0 / CLKO / EADC0_ST
18	I/O	PD.12 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / CANFD0_TXL / BPWM0_CH5 / EQEI0_INDEX / BPWM2_CH1 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / BPWM2_CH2 / INT6
20	I/O	PD.10 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / BPWM2_CH3 / INT7
21	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / BPWM2_CH4 / TM0
22	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / BPWM2_CH5 / TM1
23	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / BPWM4_CH0 / TM2
24	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / BPWM4_CH1 / TM3
25	I/O	PF.10 / EBI_ADR15 / I2S0_BCLK / SPI0_I2SMCLK / CANFD1_TXL / BPWM4_CH2
26	I/O	PF.9 / EBI_ADR16 / I2S0_MCLK / SPI0_SS / CANFD1_TXD / CANFD1_TXH / BPWM4_CH3
27	I/O	PF.8 / EBI_ADR17 / I2S0_DI / SPI0_CLK / CANFD1_RXD / BPWM4_CH4
28	I/O	PF.7 / EBI_ADR18 / I2S0_DO / SPI0_MISO / UART4_TXD / BPWM4_CH5
29	I/O	PF.6 / EBI_ADR19 / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / BPWM3_CH4 / TRACE_SWO
30	I/O	PF.14 / BPWM3_CH5 / LLSI3_OUT

Pin	Type	M3333KIGAE Pin Function
31	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / EPWM0_CH5 / BPWM5_CH0
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / EPWM0_CH4 / BPWM5_CH1
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / BPWM5_CH2
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / BPWM5_CH3
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / I2S0_BCLK / SPI2_CLK / USCI1_CTL1 / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / BPWM4_CH0
42	I/O	PE.9 / EBI_ADR11 / I2S0_MCLK / SPI2_MISO / USCI1_CTL0 / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / BPWM4_CH1
43	I/O	PE.10 / EBI_ADR12 / I2S0_DI / SPI2_MOSI / USCI1_DAT0 / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / BPWM4_CH2
44	I/O	PE.11 / EBI_ADR13 / I2S0_DO / SPI2_SS / USCI1_DAT1 / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / BPWM4_CH3
45	I/O	PE.12 / EBI_ADR14 / I2S0_LRCK / SPI2_I2SMCLK / USCI1_CLK / UART1_nRTS / EPWM0_CH4 / BPWM4_CH4
46	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / BPWM4_CH5 / TRACE_SWO
47	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4
48	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
51	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	A	LDO_CAP
55	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
56	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA /

Pin	Type	M3333KIGAE Pin Function
		CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
61	I/O	PF.15 / BPWM3_CH5
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART3_TXD / I2C1_SCL / UART4_nCTS / BPWM3_CH0 / BPWM5_CH0
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART3_RXD / I2C1_SDA / UART4_nRTS / BPWM3_CH1 / BPWM5_CH1
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / BPWM3_CH2
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / CANFD0_TXL / BPWM3_CH3
69	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
70	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
71	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
72	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
73	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
74	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
75	P	V_{SS}
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / BPWM0_CH5 / BPWM5_CH5
78	I/O	PG.10 / EBI_AD1 / BPWM0_CH4 / BPWM5_CH4
79	I/O	PG.11 / EBI_AD2 / BPWM0_CH3 / BPWM5_CH3
80	I/O	PG.12 / EBI_AD3 / BPWM0_CH2 / BPWM5_CH2
81	I/O	PG.13 / EBI_AD4 / BPWM0_CH1 / BPWM3_CH4
82	I/O	PG.14 / EBI_AD5 / BPWM0_CH0 / BPWM3_CH5 / ACMP0_O / EADC0_ST

Pin	Type	M3333KIGAE Pin Function
83	I/O	PG.15 / ACMP1_O
84	I/O	PD.7 / UART1_TXD / I2C0_SCL / SPI1_MISO / USCI1_CLK / BPWM4_CH0
85	I/O	PD.6 / UART1_RXD / I2C0_SDA / SPI1_MOSI / USCI1_DAT1 / BPWM4_CH1
86	I/O	PD.5 / EBI_AD15 / I2C1_SCL / SPI1_CLK / USCI1_DAT0 / BPWM4_CH2 / EADC0_ST
87	I/O	PD.4 / EBI_AD5 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / USCI1_CTL1 / BPWM4_CH3
88	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD / BPWM4_CH4
89	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / BPWM4_CH5
90	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL
91	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / TM2
92	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / CANFD0_TXL / BPWM0_CH0 / CLKO / EADC0_ST
93	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
94	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
95	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
96	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
97	I/O	PE.7 / EBI_AD10 / SD0_CMD / CANFD1_TXH / CANFD1_TXD / EPWM0_CH0 / BPWM0_CH5 / QSPI0_MISO0
98	I/O	PE.6 / EBI_AD11 / SD0_CLK / USCI0_CTL0 / CANFD1_RXD / EPWM0_CH1 / BPWM0_CH4 / QSPI0_MOSI0
99	I/O	PE.5 / EBI_nRD / SD0_DAT3 / USCI0_CTL1 / CANFD1_TXL / EPWM0_CH2 / BPWM0_CH3 / SPI1_MISO
100	I/O	PE.4 / EBI_nWR / SD0_DAT2 / USCI0_DAT1 / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / SPI1_MOSI
101	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / USCI0_DAT0 / EQEI0_A / EPWM0_CH4 / BPWM0_CH1 / I2S0_BCLK
102	I/O	PE.2 / EBI_ALE / SD0_DAT0 / USCI0_CLK / EQEI0_B / EPWM0_CH5 / BPWM0_CH0 / I2S0_MCLK
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / BPWM3_CH0
106	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / BPWM3_CH1
107	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / BPWM3_CH2 / I3C0_SCL
108	I/O	PH.9 / EBI_AD13 / QSPI0_SS / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / BPWM3_CH3 / I3C0_SDA
109	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / BPWM3_CH4 / I3C0_PUPEN

Pin	Type	M3333KIGAE Pin Function
110	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / BPWM3_CH5
111	I/O	PD.14 / EBI_nCS0 / SPI0_I2SMCLK / EPWM0_CH4
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
116	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
117	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / CANFD0_TXH / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
124	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
125	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7 / ELLSI0_OUT
126	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
127	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1

Table 4.3.9-2 M3333KIGAE Multi-function Pin Table

4.3.10 ULQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M3334KIGAE

4.3.10.1 M3334KIGAE

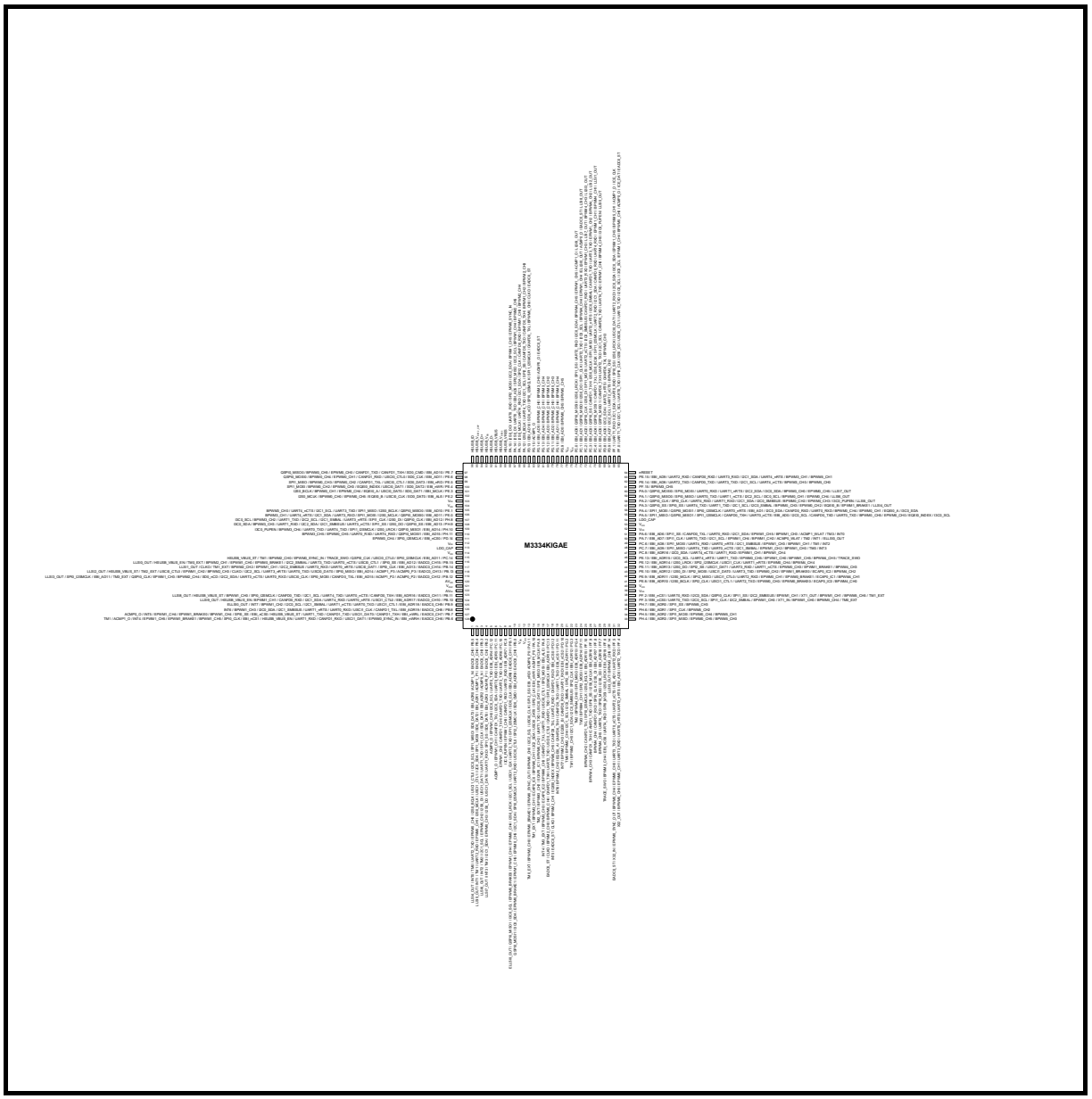


Figure-4.3-19 M3334KIGAE Multi-function Pin Diagram

Pin	Type	M3334KIGAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / USCI1_CTL0 / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LLSI4_OUT
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / USCI1_CTL1 / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LLSI5_OUT
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / USCI1_DAT1

Pin	Type	M3334KIGAE Pin Function
		/ I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / LLSI6_OUT
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / USCI1_DAT0 / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / LLSI7_OUT
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / CANFD1_TXL / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART3_TXD / CANFD1_TXD / CANFD1_TXH / EPWM1_CH2
8	I/O	PC.9 / EBI_ADR7 / UART3_RXD / CANFD1_RXD / EPWM1_CH3 / I3C0_PUPEN
9	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI1_I2SMCLK / UART2_TXD / USCI1_CLK / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / I3C0_SCL / QSPI0_MISO1 / ELLSI0_OUT
10	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / I3C0_SDA / QSPI0_MOSI1
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / BPWM0_CH0 / EPWM0_SYNC_OUT / EPWM0_BRAKE1 / BPWM3_CH0 / TM0_EXT
14	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / BPWM0_CH1 / ECAP0_IC0 / BPWM3_CH1 / TM1_EXT
15	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / ECAP0_IC1 / BPWM3_CH2 / TM2_EXT
16	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / CANFD1_TXL / BPWM0_CH3 / ECAP0_IC2 / BPWM3_CH3 / TM3_EXT / INT4
17	I/O	PC.13 / EBI_ADR10 / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / CANFD1_TXH / BPWM0_CH4 / BPWM2_CH0 / CLKO / EADC0_ST
18	I/O	PD.12 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / CANFD0_TXL / BPWM0_CH5 / EQEI0_INDEX / BPWM2_CH1 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / CANFD0_TXH / EQEI0_A / BPWM2_CH2 / INT6
20	I/O	PD.10 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / BPWM2_CH3 / INT7
21	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / BPWM2_CH4 / TM0
22	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / BPWM2_CH5 / TM1
23	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / BPWM4_CH0 / TM2
24	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / BPWM4_CH1 / TM3
25	I/O	PF.10 / EBI_ADR15 / I2S0_BCLK / SPI0_I2SMCLK / CANFD1_TXL / BPWM4_CH2
26	I/O	PF.9 / EBI_ADR16 / I2S0_MCLK / SPI0_SS / CANFD1_TXD / CANFD1_TXH / BPWM4_CH3
27	I/O	PF.8 / EBI_ADR17 / I2S0_DI / SPI0_CLK / CANFD1_RXD / BPWM4_CH4
28	I/O	PF.7 / EBI_ADR18 / I2S0_DO / SPI0_MISO / UART4_TXD / BPWM4_CH5
29	I/O	PF.6 / EBI_ADR19 / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / BPWM3_CH4 / TRACE_SWO
30	I/O	PF.14 / BPWM3_CH5 / LLSI3_OUT

Pin	Type	M3334KIGAE Pin Function
31	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / UART0_nCTS / UART3_TXD / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST
32	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / UART0_nRTS / UART3_RXD / EPWM0_CH1 / BPWM0_CH5 / X32_OUT
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / EPWM0_CH5 / BPWM5_CH0
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / EPWM0_CH4 / BPWM5_CH1
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / BPWM5_CH2
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / BPWM5_CH3
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / SPI1_CLK / I2C2_SMBAL / EPWM1_CH0 / XT1_IN / BPWM1_CH0 / BPWM5_CH4 / TM0_EXT
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / SPI1_SS / I2C2_SMBSUS / EPWM1_CH1 / XT1_OUT / BPWM1_CH1 / BPWM5_CH5 / TM1_EXT
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / I2S0_BCLK / SPI2_CLK / USCI1_CTL1 / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / BPWM4_CH0
42	I/O	PE.9 / EBI_ADR11 / I2S0_MCLK / SPI2_MISO / USCI1_CTL0 / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / BPWM4_CH1
43	I/O	PE.10 / EBI_ADR12 / I2S0_DI / SPI2_MOSI / USCI1_DAT0 / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / BPWM4_CH2
44	I/O	PE.11 / EBI_ADR13 / I2S0_DO / SPI2_SS / USCI1_DAT1 / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / BPWM4_CH3
45	I/O	PE.12 / EBI_ADR14 / I2S0_LRCK / SPI2_I2SMCLK / USCI1_CLK / UART1_nRTS / EPWM0_CH4 / BPWM4_CH4
46	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / BPWM4_CH5 / TRACE_SWO
47	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4
48	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3
49	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2
50	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / ELLSI0_OUT
51	I/O	PA.6 / EBI_AD6 / SPI1_SS / CANFD0_TXL / UART0_RXD / I2C1_SDA / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0
52	P	V_{SS}
53	P	V_{DD}
54	A	LDO_CAP
55	I/O	PA.5 / SPI1_MISO / QSPI0_MISO1 / SPI1_I2SMCLK / CANFD0_TXH / UART0_nCTS / EBI_AD0 / I2C0_SCL / CANFD0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / I3C0_SCL
56	I/O	PA.4 / SPI1_MOSI / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / EBI_AD1 / I2C0_SDA /

Pin	Type	M3334KIGAE Pin Function
		CANFD0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A / I3C0_SDA
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / LLSI4_OUT
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / I3C0_PUPEN / LLSI5_OUT
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / I3C0_SCL / BPWM0_CH1 / EPWM0_CH4 / LLSI6_OUT
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / I3C0_SDA / BPWM0_CH0 / EPWM0_CH5 / LLSI7_OUT
61	I/O	PF.15 / BPWM3_CH5
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART3_TXD / I2C1_SCL / UART4_nCTS / BPWM3_CH0 / BPWM5_CH0
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART3_RXD / I2C1_SDA / UART4_nRTS / BPWM3_CH1 / BPWM5_CH1
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SPI0_CLK / I2S0_DO / USCI0_CTL1 / UART2_TXD / I2C0_SCL / I3C0_SCL / EPWM1_CH4 / BPWM5_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI0_SS / I2S0_LRCK / USCI0_DAT1 / UART2_RXD / I2C0_SDA / I3C0_SDA / EPWM1_CH5 / BPWM5_CH1 / ACMP1_O / ICE_CLK
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / BPWM3_CH2
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / CANFD0_TXL / BPWM3_CH3
69	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / CANFD0_TXH / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / BPWM4_CH0 / I3C0_PUPEN / LLSI0_OUT
70	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / CANFD1_TXL / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / BPWM4_CH1 / LLSI1_OUT
71	I/O	PC.3 / EBI_AD3 / QSPI0_SS / CANFD1_TXH / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CANFD1_TXD / UART3_TXD / EPWM1_CH2 / BPWM4_CH2 / LLSI2_OUT
72	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CANFD1_RXD / UART3_RXD / EPWM1_CH3 / LLSI7_OUT / BPWM4_CH3 / LLSI3_OUT
73	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / BPWM4_CH4 / EPWM1_CH4 / ELLSI0_OUT / ACMP0_O / EADC0_ST / LLSI8_OUT
74	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / BPWM4_CH5 / EPWM1_CH5 / ACMP1_O / LLSI9_OUT
75	P	V_{SS}
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / BPWM0_CH5 / BPWM5_CH5
78	I/O	PG.10 / EBI_AD1 / BPWM0_CH4 / BPWM5_CH4
79	I/O	PG.11 / EBI_AD2 / BPWM0_CH3 / BPWM5_CH3
80	I/O	PG.12 / EBI_AD3 / BPWM0_CH2 / BPWM5_CH2
81	I/O	PG.13 / EBI_AD4 / BPWM0_CH1 / BPWM3_CH4
82	I/O	PG.14 / EBI_AD5 / BPWM0_CH0 / BPWM3_CH5 / ACMP0_O / EADC0_ST

Pin	Type	M3334KIGAE Pin Function
83	I/O	PG.15 / ACMP1_O
84	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / CANFD0_TXL / BPWM0_CH0 / CLKO / EADC0_ST
85	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD0_TXD / CANFD0_TXH / BPWM1_CH2 / BPWM2_CH3
86	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD0_RXD / BPWM1_CH3 / BPWM2_CH4
87	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / BPWM1_CH4 / BPWM2_CH5
88	I/O	PA.15 / I2S0_DO / UART0_RXD / SPI2_MOSI / I2C2_SDA / BPWM1_CH5 / EPWM0_SYNC_IN
89	A	HSUSB_VRES
90	P	HSUSB_VDD33
91	I/O	HSUSB_VBUS
92	A	HSUSB_D-
93	P	HSUSB_VSS
94	A	HSUSB_D+
95	A	HSUSB_VDD12_CAP
96	I	HSUSB_ID
97	I/O	PE.7 / EBI_AD10 / SD0_CMD / CANFD1_TXH / CANFD1_TXD / EPWM0_CH0 / BPWM0_CH5 / QSPI0_MISO0
98	I/O	PE.6 / EBI_AD11 / SD0_CLK / USCI0_CTL0 / CANFD1_RXD / EPWM0_CH1 / BPWM0_CH4 / QSPI0_MOSI0
99	I/O	PE.5 / EBI_nRD / SD0_DAT3 / USCI0_CTL1 / CANFD1_TXL / EPWM0_CH2 / BPWM0_CH3 / SPI1_MISO
100	I/O	PE.4 / EBI_nWR / SD0_DAT2 / USCI0_DAT1 / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / SPI1_MOSI
101	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / USCI0_DAT0 / EQEI0_A / EPWM0_CH4 / BPWM0_CH1 / I2S0_BCLK
102	I/O	PE.2 / EBI_ALE / SD0_DAT0 / USCI0_CLK / EQEI0_B / EPWM0_CH5 / BPWM0_CH0 / I2S0_MCLK
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / BPWM3_CH0
106	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / BPWM3_CH1
107	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / BPWM3_CH2 / I3C0_SCL
108	I/O	PH.9 / EBI_AD13 / QSPI0_SS / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / BPWM3_CH3 / I3C0_SDA
109	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / BPWM3_CH4 / I3C0_PUPEN

Pin	Type	M3334KIGAE Pin Function
110	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / BPWM3_CH5
111	I/O	PD.14 / EBI_nCS0 / SPI0_I2SMCLK / EPWM0_CH4
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / BPWM2_CH0 / TM1 / HSUSB_VBUS_ST
116	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / BPWM2_CH1 / TM0_EXT / HSUSB_VBUS_EN / LLSI0_OUT
117	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / BPWM2_CH2 / TM1_EXT / CLKO / LLSI1_OUT
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CLKO / BPWM2_CH3 / EPWM1_CH2 / USCI0_CTL0 / TM2_EXT / HSUSB_VBUS_ST / LLSI2_OUT
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / CANFD0_TXL / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / BPWM2_CH4 / EPWM1_CH3 / QSPI0_CLK / TM3_EXT / EBI_AD11 / SPI0_I2SMCLK / LLSI3_OUT
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / CANFD0_TXH / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / HSUSB_VBUS_ST / LLSI8_OUT
124	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD0_RXD / BPWM1_CH1 / HSUSB_VBUS_EN / LLSI9_OUT
125	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / I2C0_SCL / BPWM1_CH2 / INT7 / ELLSI0_OUT
126	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / CANFD1_TXL / USCI1_CLK / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / I2C0_SDA / BPWM1_CH3 / INT6
127	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CANFD1_TXH / USCI1_DAT0 / CANFD1_TXD / UART1_TXD / HSUSB_VBUS_ST / EBI_nCS0 / SPI0_SS / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O
128	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / EPWM0_SYNC_IN / USCI1_DAT1 / CANFD1_RXD / UART1_RXD / HSUSB_VBUS_EN / EBI_nCS1 / SPI0_CLK / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / TM1

Table 4.3-16 M3334KIGAE Multi-function Pin Table

4.4 Pin Mapping Table

4.4.1 M3333/M3334 Series Mapping Table

M3331 Series										
Pin Name	**33 Pin**	**33 Pin**	**48 Pin**	**48 Pin**	**48 Pin**	**48 Pin**	**64 Pin**	**64 Pin**	**128 Pin**	**128 Pin**
PB.5	1	1	1	1	1	1	2	2	1	1
PB.4	2	2	2	2	2	2	3	3	2	2
PB.3	3	3	3	3	3	3	4	4	3	3
PB.2	4	4	4	4	4	4	5	5	4	4
PC.12									5	5
PC.11									6	6
PC.10									7	7
PC.9									8	8
PB.1	5	5	5	5	5	5	6	6	9	9
PB.0	6	6	6	6	6	6	7	7	10	10
V_{SS}									11	11
V_{DD}									12	12
PA.11			7	7	7	7	8	8	13	13
PA.10			8	8	8	8	9	9	14	14
PA.9			9	9	9	9	10	10	15	15
PA.8			10	10	10	10	11	11	16	16
PC.13									17	17
PD.12									18	18
PD.11									19	19
PD.10									20	20
PG.2									21	21
PG.3									22	22
PG.4									23	23
PF.11									24	24
PF.10									25	25
PF.9									26	26
PF.8									27	27
PF.7									28	28
PF.6							12	12	29	29
PF.14							13	13	30	30

PF.5	7	7	11	11	11	11	14	14	31	31
PF.4	8	8	12	12	12	12	15	15	32	32
PH.4									33	33
PH.5									34	34
PH.6									35	35
PH.7									36	36
PF.3	9	9	13	13	13	13	16	16	37	37
PF.2	10	10	14	14	14	14	17	17	38	38
V_{SS}									39	39
V_{DD}									40	40
PE.8									41	41
PE.9									42	42
PE.10									43	43
PE.11									44	44
PE.12									45	45
PE.13									46	46
PC.8									47	47
PC.7							18	18	48	48
PC.6							19	19	49	49
PA.7			15	15	15	15	20	20	50	50
PA.6			16	16	16	16	21	21	51	51
V_{SS}							22	22	52	52
V_{DD}							23	23	53	53
LDO_CAP							24	24	54	54
PA.5			17	17	17	17	25	25	55	55
PA.4			18	18	18	18	26	26	56	56
PA.3	11	11	19	19	19	19	27	27	57	57
PA.2	12	12	20	20	20	20	28	28	58	58
PA.1	13	13	21	21	21	21	29	29	59	59
PA.0	14	14	22	22	22	22	30	30	60	60
PF.15	15	15	23	23	23	23	31	31	61	61
PE.14									62	62
PE.15									63	63
nRESET	16	16	24	24	24	24	32	32	64	64

PF.0	17	17	25	25	25	25	33	33	65	65
PF.1	18	18	26	26	26	26	34	34	66	66
PD.9									67	67
PD.8									68	68
PC.5			27		27		35	35	69	69
PC.4			28		28		36	36	70	70
PC.3			29		29		37	37	71	71
PC.2			30		30		38	38	72	72
PC.1	19		31	27	31	27	39	39	73	73
PC.0	20		32	28	32	28	40	40	74	74
V_{SS}									75	75
V_{DD}									76	76
PG.9							41		77	77
PG.10							42		78	78
PG.11							43		79	79
PG.12							44		80	80
PG.13									81	81
PG.14									82	82
PG.15									83	83
PD.7									84	
PD.6									85	
PD.5									86	
PD.4									87	
PD.3									88	
PD.2									89	
PD.1									90	
PD.0									91	
PD.13									92	84
PA.12	21		33		33		45		93	85
PA.13	22		34		34		46		94	86
PA.14	23		35		35		47		95	87
PA.15	24		36		36		48		96	88
HSUSB_V_{RES}		19		29		29		41		89
HSUSB_V_{DD33}		20		30		30		42		90

HSUSB_V_{BUS}		21		31		31		43		91
HSUSB_D-		22		32		32		44		92
HSUSB_V_{SS}		33		33		33		45		93
HSUSB_D+		23		34		34		46		94
HSUSB_V_{DD12_CAP}		24		35		35		47		95
HSUSB_ID				36		36		48		96
PE.7									97	97
PE.6									98	98
PE.5									99	99
PE.4									100	100
PE.3									101	101
PE.2									102	102
V_{SS}	25	25	37	37	37	37	49	49	103	103
V_{DD}									104	104
PE.1									105	105
PE.0									106	106
PH.8									107	107
PH.9									108	108
PH.10									109	109
PH.11									110	110
PD.14									111	111
V_{SS}									112	112
LDO_CAP	26	26	38	38	38	38	50	50	113	113
V_{DD}	27	27	39	39	39	39	51	51	114	114
PC.14			40	40	40	40	52	52	115	115
PB.15	28	28	41	41	41	41	53	53	116	116
PB.14	29	29	42	42	42	42	54	54	117	117
PB.13	30	30	43	43	43	43	55	55	118	118
PB.12	31	31	44	44	44	44	56	56	119	119
AV_{DD}	32	32	45	45	45	45	57	57	120	120
V_{REF}							58	58	121	121
AV_{SS}			46	46	46	46	59	59	122	122
PB.11							60	60	123	123
PB.10							61	61	124	124

PB.9							62	62	125	125
PB.8							63	63	126	126
PB.7			47	47	47	47	64	64	127	127
PB.6			48	48	48	48	1	1	128	128
V_{SS}	33	33	49	49						

4.5 Pin Functional Description

4.5.1 M3333/M3334 Series Summary Function Pin Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
BPWM2	BPWM2_CH0	I/O	BPWM2 channel 0 output/capture input.
	BPWM2_CH1	I/O	BPWM2 channel 1 output/capture input.
	BPWM2_CH2	I/O	BPWM2 channel 2 output/capture input.
	BPWM2_CH3	I/O	BPWM2 channel 3 output/capture input.

Group	Pin Name	Type	Description
	BPWM2_CH4	I/O	BPWM2 channel 4 output/capture input.
	BPWM2_CH5	I/O	BPWM2 channel 5 output/capture input.
BPWM3	BPWM3_CH0	I/O	BPWM3 channel 0 output/capture input.
	BPWM3_CH1	I/O	BPWM3 channel 1 output/capture input.
	BPWM3_CH2	I/O	BPWM3 channel 2 output/capture input.
	BPWM3_CH3	I/O	BPWM3 channel 3 output/capture input.
	BPWM3_CH4	I/O	BPWM3 channel 4 output/capture input.
	BPWM3_CH5	I/O	BPWM3 channel 5 output/capture input.
BPWM4	BPWM4_CH0	I/O	BPWM4 channel 0 output/capture input.
	BPWM4_CH1	I/O	BPWM4 channel 1 output/capture input.
	BPWM4_CH2	I/O	BPWM4 channel 2 output/capture input.
	BPWM4_CH3	I/O	BPWM4 channel 3 output/capture input.
	BPWM4_CH4	I/O	BPWM4 channel 4 output/capture input.
	BPWM4_CH5	I/O	BPWM4 channel 5 output/capture input.
BPWM5	BPWM5_CH0	I/O	BPWM5 channel 0 output/capture input.
	BPWM5_CH1	I/O	BPWM5 channel 1 output/capture input.
	BPWM5_CH2	I/O	BPWM5 channel 2 output/capture input.
	BPWM5_CH3	I/O	BPWM5 channel 3 output/capture input.
	BPWM5_CH4	I/O	BPWM5 channel 4 output/capture input.
	BPWM5_CH5	I/O	BPWM5 channel 5 output/capture input.
CANFD0	CANFD0_RXD	I	CANFD0 bus receiver input.
	CANFD0_TXD	O	CANFD0 bus transmitter output.
	CANFD0_TXH	O	CANFD0 bus transmitter high level line digital output.
	CANFD0_TXL	O	CANFD0 bus transmitter low level line digital output.
CANFD1	CANFD1_RXD	I	CANFD1 bus receiver input.
	CANFD1_TXD	O	CANFD1 bus transmitter output.
	CANFD1_TXH	O	CANFD1 bus transmitter high level line digital output.
	CANFD1_TXL	O	CANFD1 bus transmitter low level line digital output.
CLKO	CLKO	O	Clock Out.
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.

Group	Pin Name	Type	Description
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_ST	I	EADC0 external trigger input.
EBI	EBI_AD0	I/O	EBI address/data bus bit 0.
	EBI_AD1	I/O	EBI address/data bus bit 1.
	EBI_AD2	I/O	EBI address/data bus bit 2.
	EBI_AD3	I/O	EBI address/data bus bit 3.
	EBI_AD4	I/O	EBI address/data bus bit 4.
	EBI_AD5	I/O	EBI address/data bus bit 5.
	EBI_AD6	I/O	EBI address/data bus bit 6.
	EBI_AD7	I/O	EBI address/data bus bit 7.
	EBI_AD8	I/O	EBI address/data bus bit 8.
	EBI_AD9	I/O	EBI address/data bus bit 9.
	EBI_AD10	I/O	EBI address/data bus bit 10.
	EBI_AD11	I/O	EBI address/data bus bit 11.
	EBI_AD12	I/O	EBI address/data bus bit 12.
	EBI_AD13	I/O	EBI address/data bus bit 13.
	EBI_AD14	I/O	EBI address/data bus bit 14.
	EBI_AD15	I/O	EBI address/data bus bit 15.
	EBI_ADR0	O	EBI address bus bit 0.
	EBI_ADR1	O	EBI address bus bit 1.
	EBI_ADR2	O	EBI address bus bit 2.
	EBI_ADR3	O	EBI address bus bit 3.

Group	Pin Name	Type	Description
	EBI_ADR4	O	EBI address bus bit 4.
	EBI_ADR5	O	EBI address bus bit 5.
	EBI_ADR6	O	EBI address bus bit 6.
	EBI_ADR7	O	EBI address bus bit 7.
	EBI_ADR8	O	EBI address bus bit 8.
	EBI_ADR9	O	EBI address bus bit 9.
	EBI_ADR10	O	EBI address bus bit 10.
	EBI_ADR11	O	EBI address bus bit 11.
	EBI_ADR12	O	EBI address bus bit 12.
	EBI_ADR13	O	EBI address bus bit 13.
	EBI_ADR14	O	EBI address bus bit 14.
	EBI_ADR15	O	EBI address bus bit 15.
	EBI_ADR16	O	EBI address bus bit 16.
	EBI_ADR17	O	EBI address bus bit 17.
	EBI_ADR18	O	EBI address bus bit 18.
	EBI_ADR19	O	EBI address bus bit 19.
	EBI_ALE	O	EBI address latch enable output pin.
	EBI_MCLK	O	EBI external clock output pin.
	EBI_nCS0	O	EBI chip select 0 output pin.
	EBI_nCS1	O	EBI chip select 1 output pin.
	EBI_nCS2	O	EBI chip select 2 output pin.
	EBI_nRD	O	EBI read enable output pin.
	EBI_nWR	O	EBI write enable output pin.
	EBI_nWRH	O	EBI high byte write enable output pin
	EBI_nWRL	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
ELLSI0	ELLSI0_OUT	O	Enhanced LED Lighting Strip Interface 0 output pin.
EPWM0	EPWM0_BRAKE0	I	EPWM0 Brake 0 input pin.
	EPWM0_BRAKE1	I	EPWM0 Brake 1 input pin.
	EPWM0_CH0	I/O	EPWM0 channel 0 output/capture input.
	EPWM0_CH1	I/O	EPWM0 channel 1 output/capture input.

Group	Pin Name	Type	Description
	EPWM0_CH2	I/O	EPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	EPWM0 channel 3 output/capture input.
	EPWM0_CH4	I/O	EPWM0 channel 4 output/capture input.
	EPWM0_CH5	I/O	EPWM0 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	O	EPWM0 counter synchronous trigger output pin.
EPWM1	EPWM1_BRAKE0	I	EPWM1 Brake 0 input pin.
	EPWM1_BRAKE1	I	EPWM1 Brake 1 input pin.
	EPWM1_CH0	I/O	EPWM1 channel 0 output/capture input.
	EPWM1_CH1	I/O	EPWM1 channel 1 output/capture input.
	EPWM1_CH2	I/O	EPWM1 channel 2 output/capture input.
	EPWM1_CH3	I/O	EPWM1 channel 3 output/capture input.
	EPWM1_CH4	I/O	EPWM1 channel 4 output/capture input.
	EPWM1_CH5	I/O	EPWM1 channel 5 output/capture input.
EQEI0	EQEI0_A	I	EQEI0 phase A input.
	EQEI0_B	I	EQEI0 phase B input.
	EQEI0_INDEX	I	EQEI0 index input.
HSUSB	HSUSB_VBUS_EN	O	HSUSB external VBUS regulator enable pin.
	HSUSB_VBUS_ST	I	HSUSB external VBUS regulator status pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin.
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin.
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
	I2C2_SMBAL	O	I2C2 SMBus SMBALTER pin.
	I2C2_SMBSUS	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	O	I2S0 bit clock output pin.
	I2S0_DI	I	I2S0 data input pin.

Group	Pin Name	Type	Description
	I2S0_DO	O	I2S0 data output pin.
	I2S0_LRCK	O	I2S0 left right channel clock output pin.
	I2S0_MCLK	O	I2S0 master clock output pin.
I3C0	I3C0_PUPEN	O	I3C0 pull-up resistor enable pin.
	I3C0_SCL	I/O	I3C0 serial clock pin.
	I3C0_SDA	I/O	I3C0 serial data pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
INT6	INT6	I	External interrupt 6 input pin.
INT7	INT7	I	External interrupt 7 input pin.
LLSI0	LLSI0_OUT	O	LED Lighting Strip Interface 0 output pin.
LLSI1	LLSI1_OUT	O	LED Lighting Strip Interface 1 output pin.
LLSI2	LLSI2_OUT	O	LED Lighting Strip Interface 2 output pin.
LLSI3	LLSI3_OUT	O	LED Lighting Strip Interface 3 output pin.
LLSI4	LLSI4_OUT	O	LED Lighting Strip Interface 4 output pin.
LLSI5	LLSI5_OUT	O	LED Lighting Strip Interface 5 output pin.
LLSI6	LLSI6_OUT	O	LED Lighting Strip Interface 6 output pin.
LLSI7	LLSI7_OUT	O	LED Lighting Strip Interface 7 output pin.
LLSI8	LLSI8_OUT	O	LED Lighting Strip Interface 8 output pin.
LLSI9	LLSI9_OUT	O	LED Lighting Strip Interface 9 output pin.
PDCI	PDCI_G0_CLK	O	PDCI Group 0 Clock
	PDCI_G0_RX0	I	PDCI Group 0 RX 0 Pin
	PDCI_G0_RX1	I	PDCI Group 0 RX 1 Pin
	PDCI_G0_RX2	I	PDCI Group 0 RX 2 Pin
	PDCI_G0_RX3	I	PDCI Group 0 RX 3 Pin

Group	Pin Name	Type	Description
	PDCI_G0_TX0	I/O	PDCI Group 0 TX 0 Pin
	PDCI_G0_TX1	I/O	PDCI Group 0 TX 1 Pin
	PDCI_G0_TX2	I/O	PDCI Group 0 TX 2 Pin
	PDCI_G0_TX3	I/O	PDCI Group 0 TX 3 Pin
	PDCI_G1_CLK	O	PDCI Group 1 Clock
	PDCI_G1_RX0	I	PDCI Group 1 RX 0 Pin
	PDCI_G1_RX1	I	PDCI Group 1 RX 1 Pin
	PDCI_G1_RX2	I	PDCI Group 1 RX 2 Pin
	PDCI_G1_RX3	I	PDCI Group 1 RX 3 Pin
	PDCI_G1_TX0	I/O	PDCI Group 1 TX 0 Pin
	PDCI_G1_TX1	I/O	PDCI Group 1 TX 1 Pin
	PDCI_G1_TX2	I/O	PDCI Group 1 TX 2 Pin
	PDCI_G1_TX3	I/O	PDCI Group 1 TX 3 Pin
	PDCI_G2_CLK	O	PDCI Group 2 Clock
	PDCI_G2_RX0	I	PDCI Group 2 RX 0 Pin
	PDCI_G2_RX1	I	PDCI Group 2 RX 1 Pin
	PDCI_G2_RX2	I	PDCI Group 2 RX 2 Pin
	PDCI_G2_RX3	I	PDCI Group 2 RX 3 Pin
	PDCI_G2_TX0	I/O	PDCI Group 2 TX 0 Pin
	PDCI_G2_TX1	I/O	PDCI Group 2 TX 1 Pin
	PDCI_G2_TX2	I/O	PDCI Group 2 TX 2 Pin
	PDCI_G2_TX3	I/O	PDCI Group 2 TX 3 Pin
	PDCI_G3_CLK	O	PDCI Group 3 Clock
	PDCI_G3_RX0	I	PDCI Group 3 RX 0 Pin
	PDCI_G3_RX1	I	PDCI Group 3 RX 1 Pin
	PDCI_G3_RX2	I	PDCI Group 3 RX 2 Pin
	PDCI_G3_RX3	I	PDCI Group 3 RX 3 Pin
	PDCI_G3_TX0	I/O	PDCI Group 3 TX 0 Pin
	PDCI_G3_TX1	I/O	PDCI Group 3 TX 1 Pin
	PDCI_G3_TX2	I/O	PDCI Group 3 TX 2 Pin
	PDCI_G3_TX3	I/O	PDCI Group 3 TX 3 Pin
	PDCI_G4_CLK	O	PDCI Group 4 Clock
	PDCI_G4_RX0	I	PDCI Group 4 RX 0 Pin

Group	Pin Name	Type	Description
	PDCI_G4_RX1	I	PDCI Group 4 RX 1 Pin
	PDCI_G4_TX0	I/O	PDCI Group 4 TX 0 Pin
	PDCI_G4_TX1	I/O	PDCI Group 4 TX 1 Pin
	PDCI_G4_TX2	I/O	PDCI Group 4 TX 2 Pin
	PDCI_G4_TX3	I/O	PDCI Group 4 TX 3 Pin
	PDCI_G5_CLK	O	PDCI Group 5 Clock
	PDCI_G5_RX0	I	PDCI Group 5 RX 0 Pin
	PDCI_G5_RX1	I	PDCI Group 5 RX 1 Pin
	PDCI_G5_TX0	I/O	PDCI Group 5 TX 0 Pin
	PDCI_G5_TX1	I/O	PDCI Group 5 TX 1 Pin
	PDCI_G5_TX2	I/O	PDCI Group 5 TX 2 Pin
	PDCI_G5_TX3	I/O	PDCI Group 5 TX 3 Pin
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
SD0	SD0_CLK	O	SD/SDIO0 clock output pin
	SD0_CMD	I/O	SD/SDIO0 command/response pin
	SD0_DAT0	I/O	SD/SDIO0 data line bit 0.
	SD0_DAT1	I/O	SD/SDIO0 data line bit 1.
	SD0_DAT2	I/O	SD/SDIO0 data line bit 2.
	SD0_DAT3	I/O	SD/SDIO0 data line bit 3.
	SD0_nCD	I	SD/SDIO0 card detect input pin
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.

Group	Pin Name	Type	Description
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
SPI2	SPI2_CLK	I/O	SPI2 serial clock pin.
	SPI2_I2SMCLK	I/O	SPI2 I2S master clock output pin
	SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin.
	SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin.
	SPI2_SS	I/O	SPI2 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TRACE	TRACE_SWO	O	Trace Single Wire output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
UART4	UART4_RXD	I	UART4 data receiver input pin.

Group	Pin Name	Type	Description
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	I/O	USCI1 clock pin.
	USCI1_CTL0	I/O	USCI1 control 0 pin.
	USCI1_CTL1	I/O	USCI1 control 1 pin.
	USCI1_DAT0	I/O	USCI1 data 0 pin.
	USCI1_DAT1	I/O	USCI1 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
USB	HSUSB_D+	A	HSUSB differential signal D+.
	HSUSB_D-	A	HSUSB differential signal D-.
	HSUSB_ID	I	HSUSB identification.
	HSUSB_VBUS	I/O	HSUSB Power supply from USB host or HUB.
	HSUSB_VDD12_CAP	A	HSUSB Internal power regulator output 1.2V decoupling pin. Note: This pin needs to be connected with a 1μF capacitor.
	HSUSB_VDD33	P	Power supply for HSUSB VDD33.
	HSUSB_VRES	A	HSUSB module reference resister.
	HSUSB_VSS	P	Ground pin for HSUSB.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. Note: This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{REF}	A	ADC reference voltage input. Note: This pin needs to be connected with a 1μF capacitor.

Group	Pin Name	Type	Description
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. Note: It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.

5 BLOCK DIAGRAM

5.1 M3334 Series Block Diagram

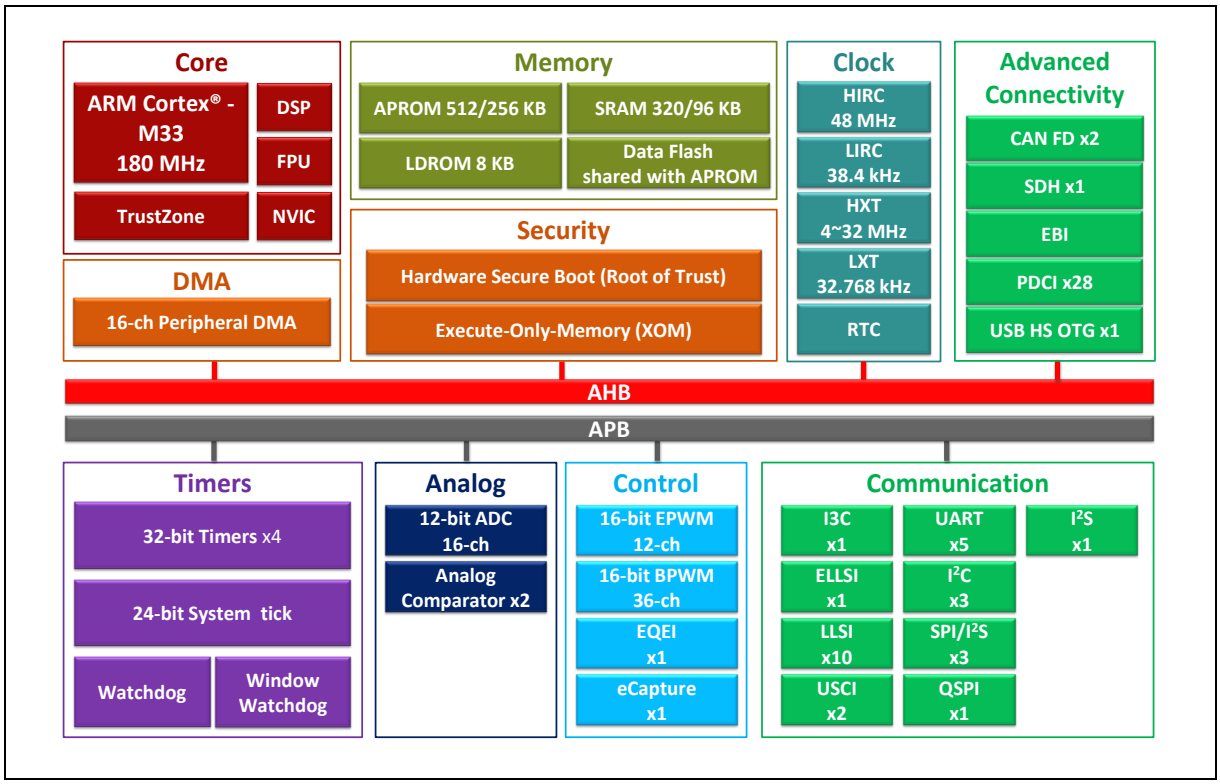


Figure 5.1-1 M3334 Series Block Diagram

5.2 M3333 Series Block Diagram

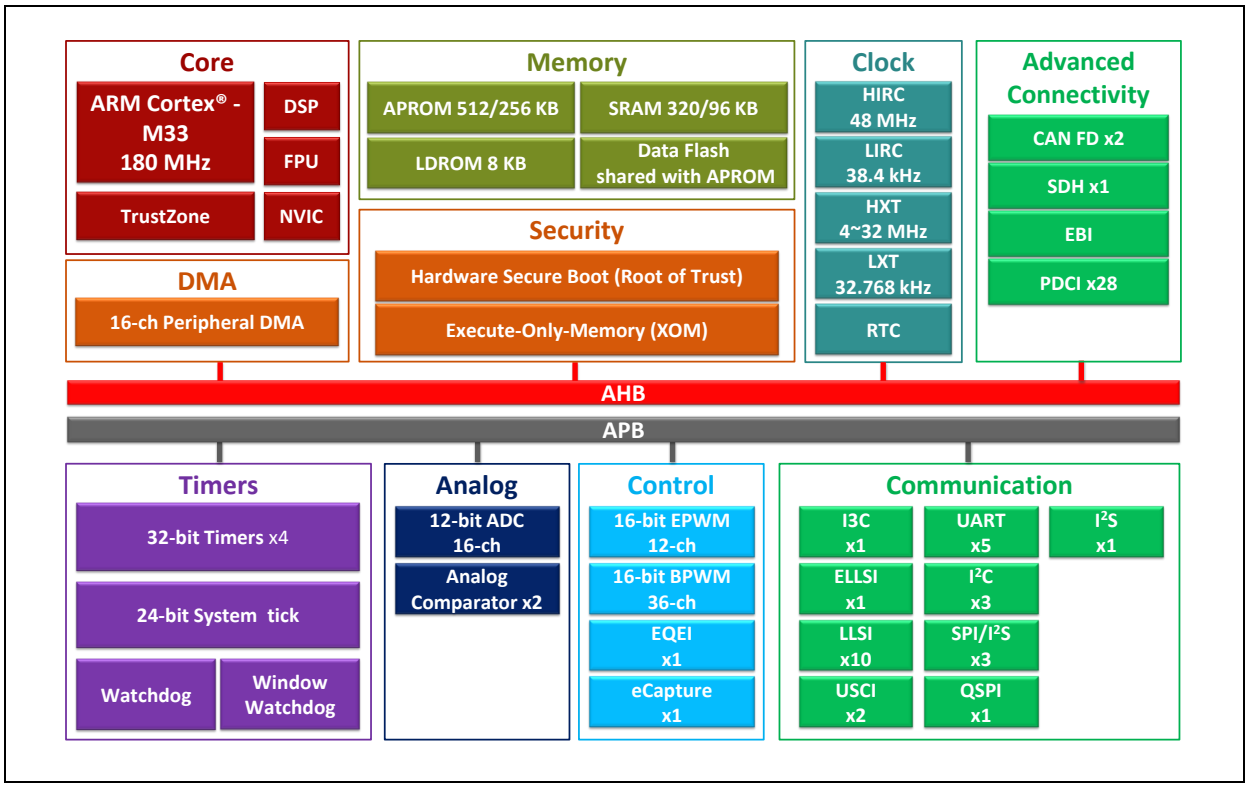


Figure 5.2-1 M3333 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM Cortex-M33 Core

The Cortex-M33 processor is a low gate count, highly energy efficient processor that is intended for microcontroller and deeply embedded applications. The processor is based on the Armv8-M architecture and is primarily for use in environments where security is an important consideration. TrustZone security for hardware-enforced isolation, memory-protection units (MPUs) and a floating-point unit (FPU). Figure 6.1-1shows the functional controller of the processor.

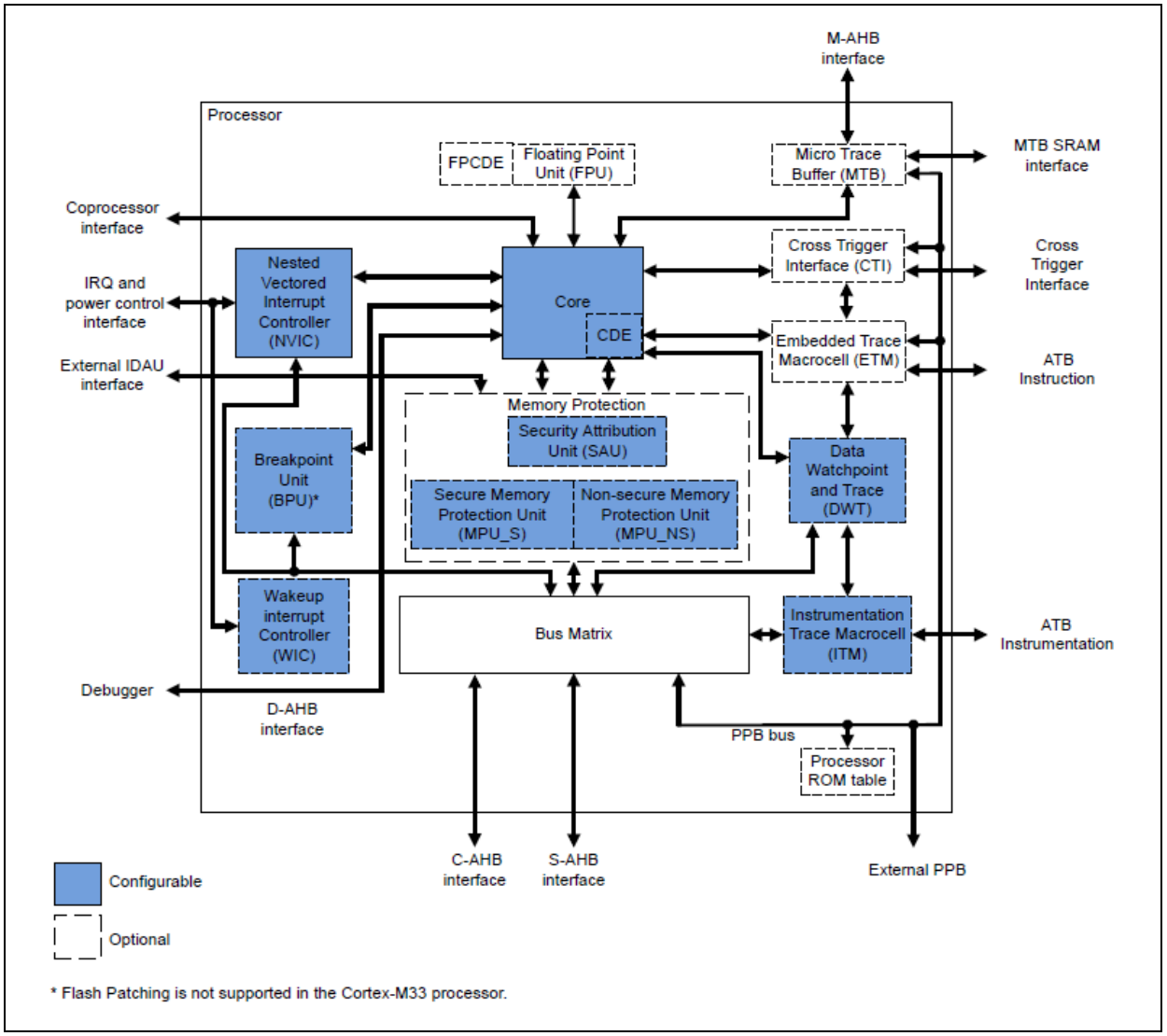


Figure 6.1-1 Cortex-M33 Block Diagram

Cortex-M33 processor features:

- The processor core provides:

  Limited dual-issue of common 16-bit instruction pairs

  Integer divide unit with support for operand-dependent early termination.

  Support for interrupted continuable load and store multiple operations.

Load and store operations that both support precise bus errors.

- Floating Point Unit (FPU) provides:

  Instructions for single-precision (C programming language float type) data-processing operations.

  Instructions for double-precision (C double type) load and store operations.

  Combined multiply-add instructions for increased precision (Fused MAC).

  Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root.

  Hardware support for denormals and all IEEE Standard 754-2008 rounding modes.

  32 32-bit single-precision registers or 16 64-bit double-precision registers.

  Lazy floating-point context save. Automated stacking of floating-point state is delayed until the ISR attempts to execute a floating-point instruction. This reduces the latency to enter the ISR and removes floating-point context save for ISRs that do not use floating-point.

- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Functions of the NVIC include:

  External interrupts, configurable from 1 to 480 using a contiguous or non-contiguous mapping. This is configured at implementation

  Configurable levels of interrupt priority from 8 to 256. This is configured at implementation.

  Dynamic reprioritization of interrupts.

  Priority grouping. This enables selection of preempting interrupt levels and non-preempting interrupt levels.

  Support for tail-chaining and late arrival of interrupts. This enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.

- Debug support

  Debug and trace components include a configurable Breakpoint Unit (BPU) for implementing breakpoints, and configurable Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data tracing, and system profiling.

- Bus interfaces:

  The System AHB (S-AHB) interface is used for any instruction fetch and data access to the memory-mapped SRAM, Peripheral, External RAM and External device, or Vendor_SYS regions of the Armv8-M memory map.

  The Code AHB (C-AHB) interface is used for any instruction fetch and data access to the Code region of the Armv8-M memory map.

  The External PPB (EPPB) APB interface enables access to CoreSight-compatible debug and trace components in a system connected to the processor.

  - The Debug AHB (D-AHB) slave interface allows a debugger access to registers, memory, and peripherals. The D-AHB interface provides debug access to the processor and the complete memory map.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M33 core only by writing 1 to CPURST (SYS_IPRST0[1])

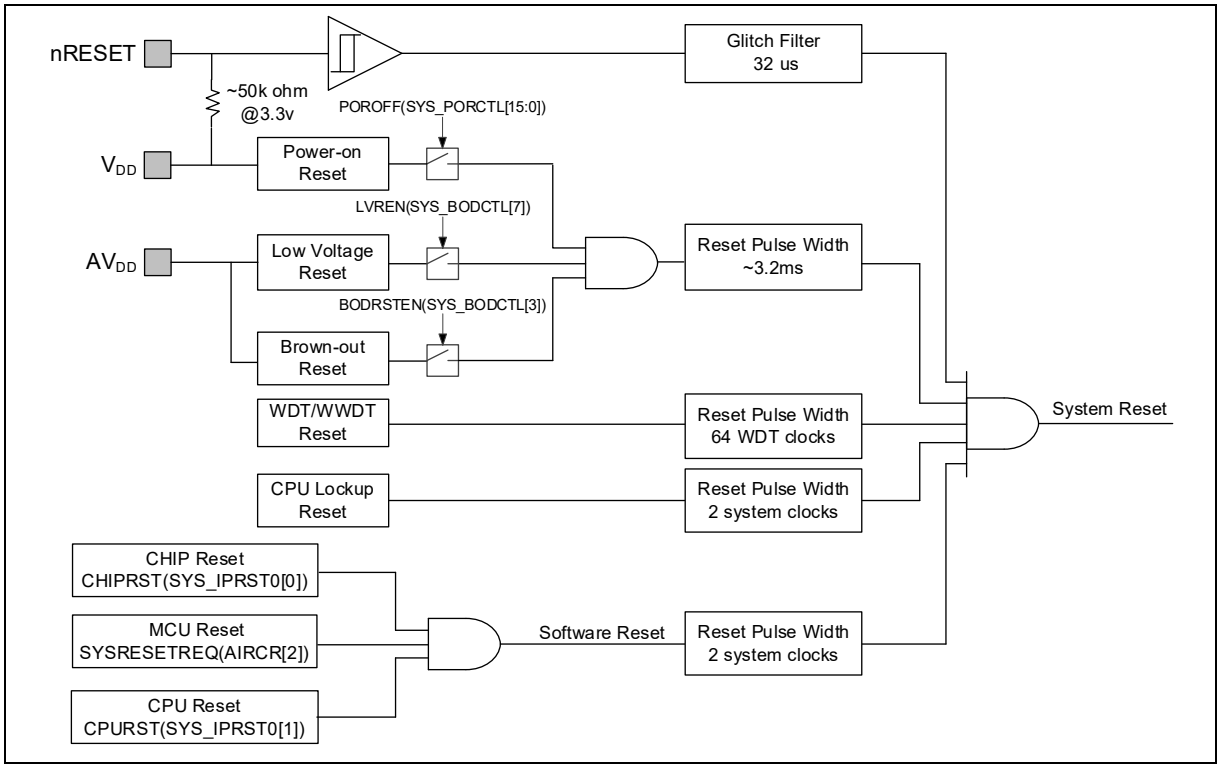


Figure 6.2-1 System Reset Sources

The Mask ROM which is built-in secure boot and ROM ISP function is the initial boot source after chip is powered on or cold reset. User can refer to Mask ROM application note for the detailed features and functions. System cold reset events include nRESET pin, WDT/WWDT, LVR, BOD, CHIP reset , Lockup reset and wake-up from Deep Power-down mode (DPD). Other reset events include MCU, CPU and wake-up from Standby Power-down mode (SPD) are defined as warm reset events. Figure 6.2-2 shows the Reset Event State Machine.

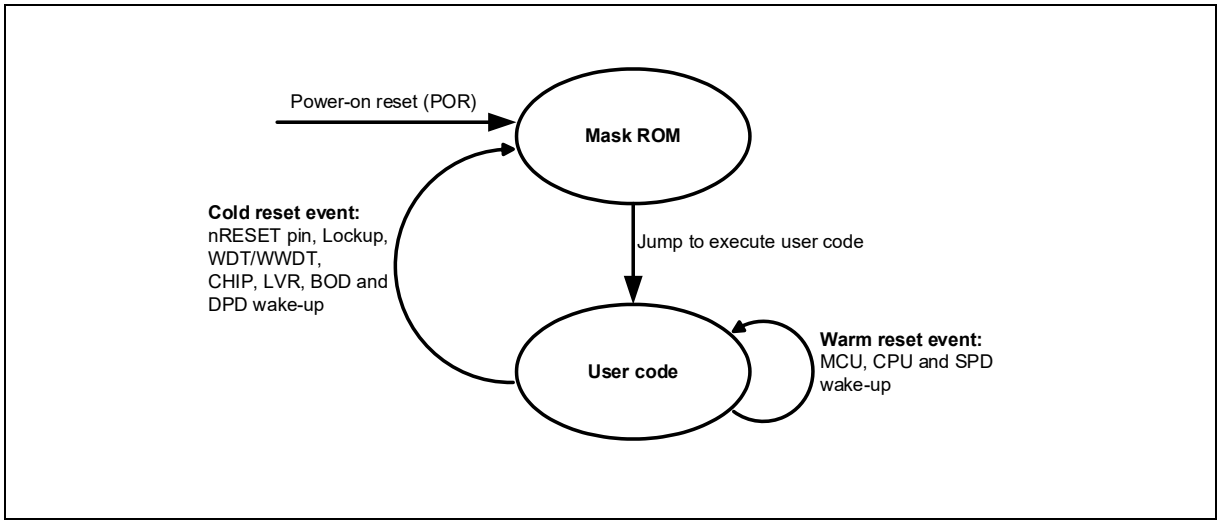


Figure 6.2-2 Reset Event State Machine

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M33 only; the other reset sources will reset Cortex-M33 and all peripherals. However, there are small

differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[19:16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	0x7 HIRC	-
CLK_PCLKDIV	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
CLK_PLLCTL	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	0x94426	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
HIRCSTB (CLK_STATUS[4])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PDMSEL (CLK_PMUCTL[2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									

WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	0x0800	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	-
FMC_CYCCTL	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

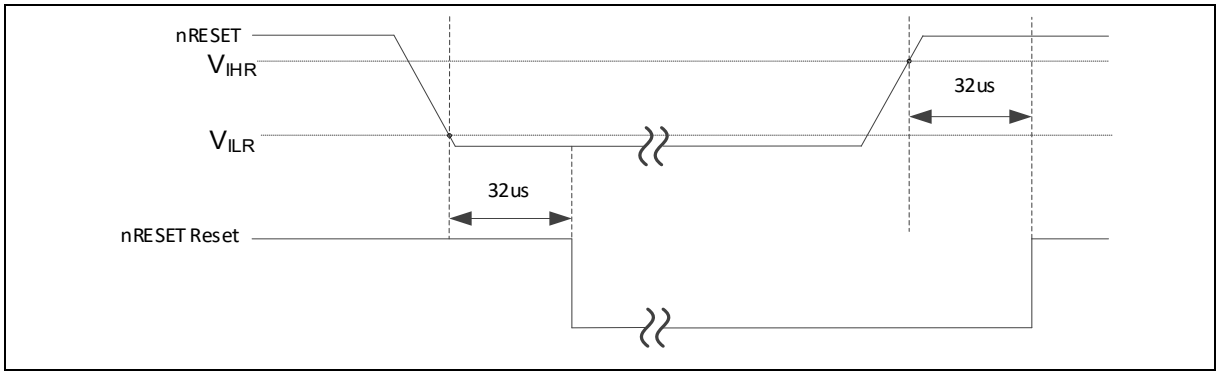


Figure 6.2-3 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-4 shows the power-on reset waveform.

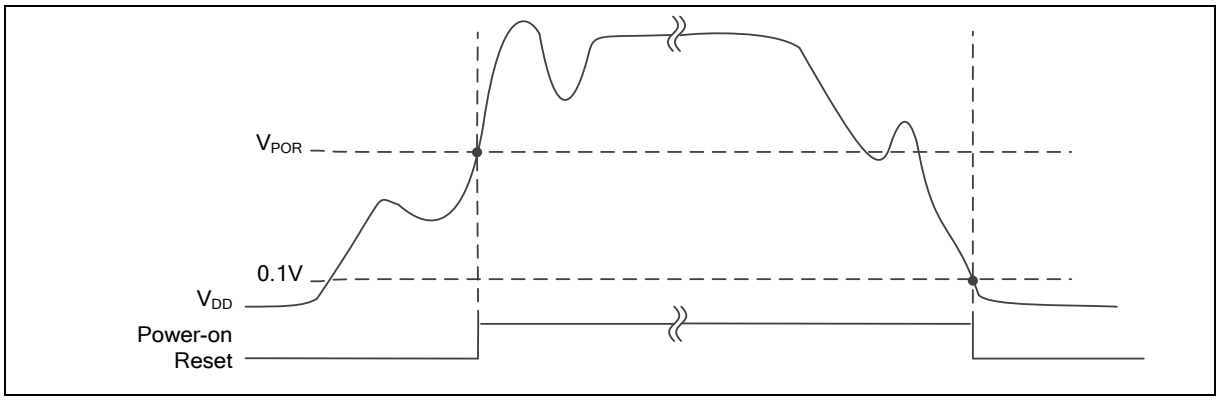


Figure 6.2-4 Power-on Reset (POR) Waveform

6.2.2.3 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 100us~200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-5 shows the Low Voltage Reset waveform.

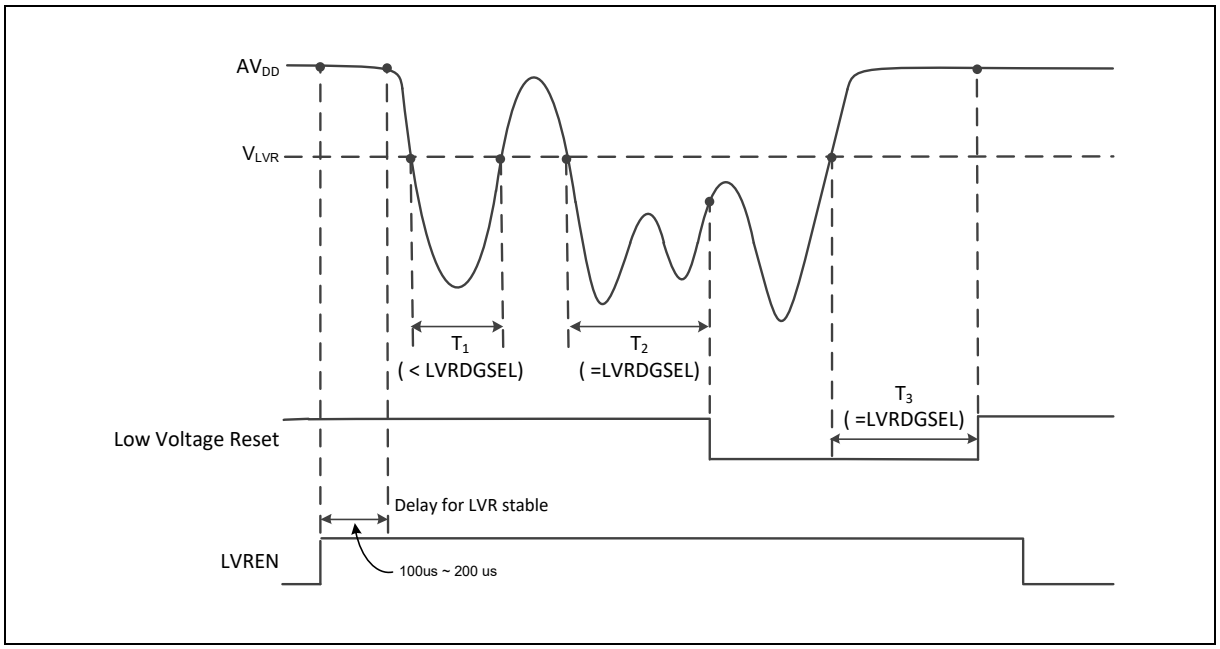


Figure 6.2-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 *Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[19:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD}

voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-6 shows the Brown-out Detector waveform.

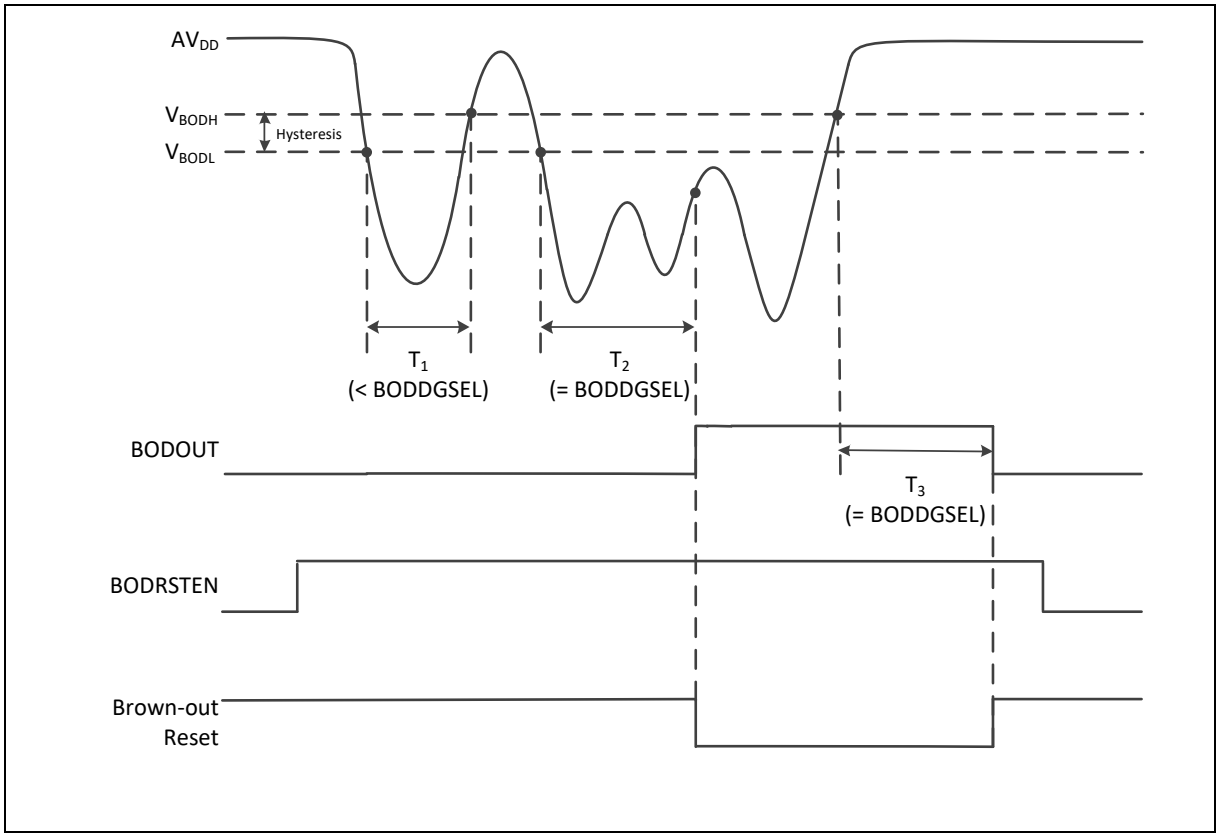


Figure 6.2-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex-M33 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and the Chip Booting Selection is automatically reloaded from CONFIG0[7] setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

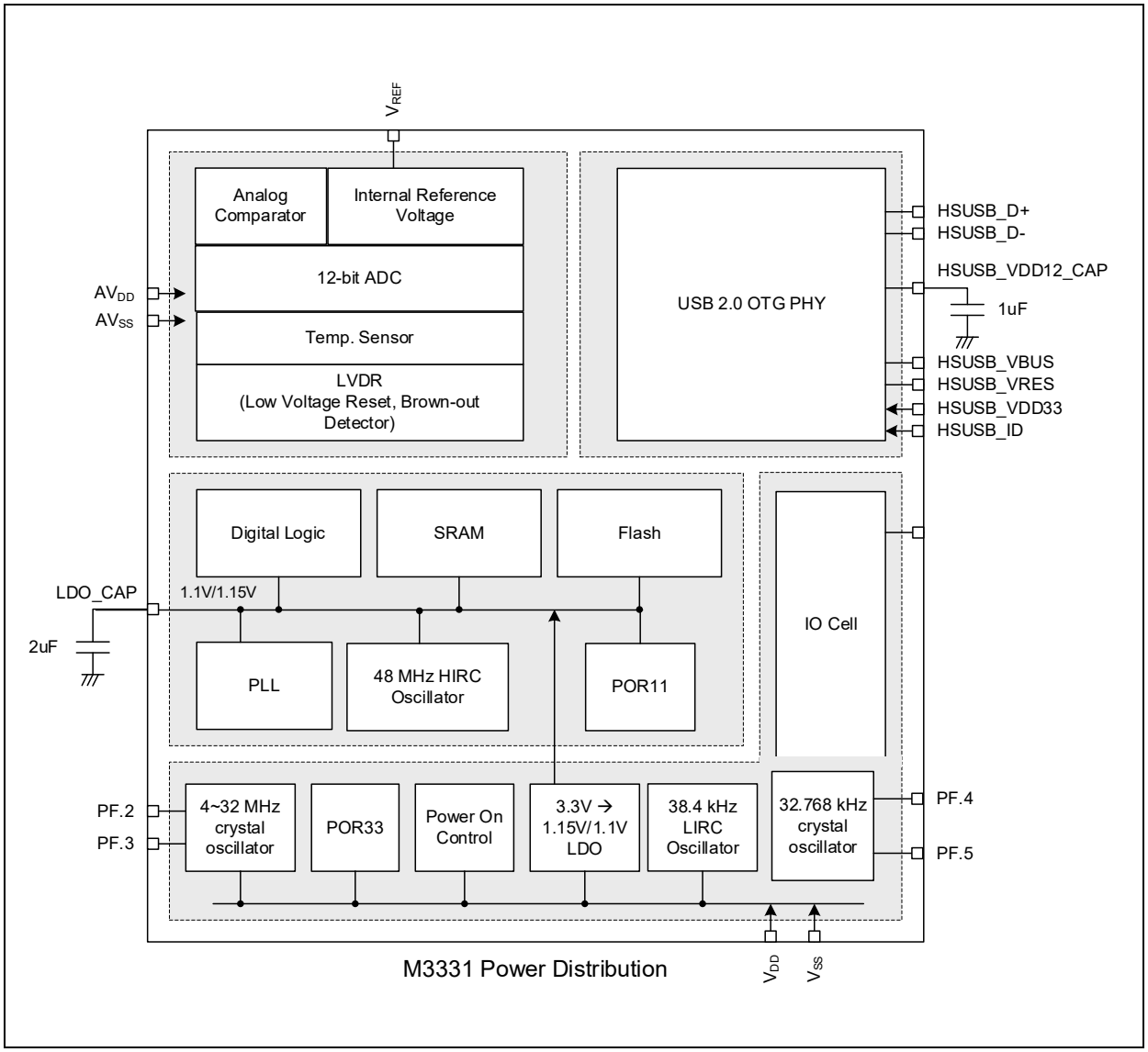
The MCU Reset is similar with CHIP Reset. The difference is that the Chip Booting Selection will not be reloaded from CBS(CONFIG0[7]) setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into five segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides power levels(PL0/PL1) for digital operation and I/O pins.
- USB 2.0 transceiver power from HSUSB_VDD33 offers the power for operating the USB transceiver.

The outputs of internal voltage regulator, LDO_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-7 shows the NuMicro M3331 power distribution.



M3331 Power Distribution

Figure 6.2-7 NuMicro M3331 Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M3331 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode at the M3331 series.

Mode	CPU Operating and HCLK Maximum Speed (MHz)	APB and PCLK Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode Power Level 1 (PL1)	160	80	1.1	All clocks are disabled by control register.
Turbo mode Power Level 0 (PL0)	180	90	1.15	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	CPU enter Sleep mode	1.1/1.15	Only CPU clock is disabled.

Normal Power-down mode 0 (NPD0)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.1/1.15	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode 1 (NPD1)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.1/1.15	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode 2 (NPD2)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	Power off	0.9	Only LIRC still enable for wake-up timer usage. Only LXT still enabled for RTC function usage.
Deep Power-down mode (DPD)	Power off	Power off	Floating	Only LIRC still enabled for wake-up timer usage. Only LXT still enabled for RTC function usage.

Table 6.2-2 Power Mode Table

There are different power mode entry setting for each power mode, with different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running at normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Normal Power-down mode 0	1	1	2	YES
Normal Power-down mode 1	1	1	0	YES
Normal Power-down mode 2	1	1	1	YES
Standby Power-down mode	1	1	4	YES
Deep Power-down mode	1	1	6	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retain.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, INT, SDH, USCI, ACMP, HSUSBD, HSUSBH, HSOTG, WKTMR and WKIO .

Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Definition Table

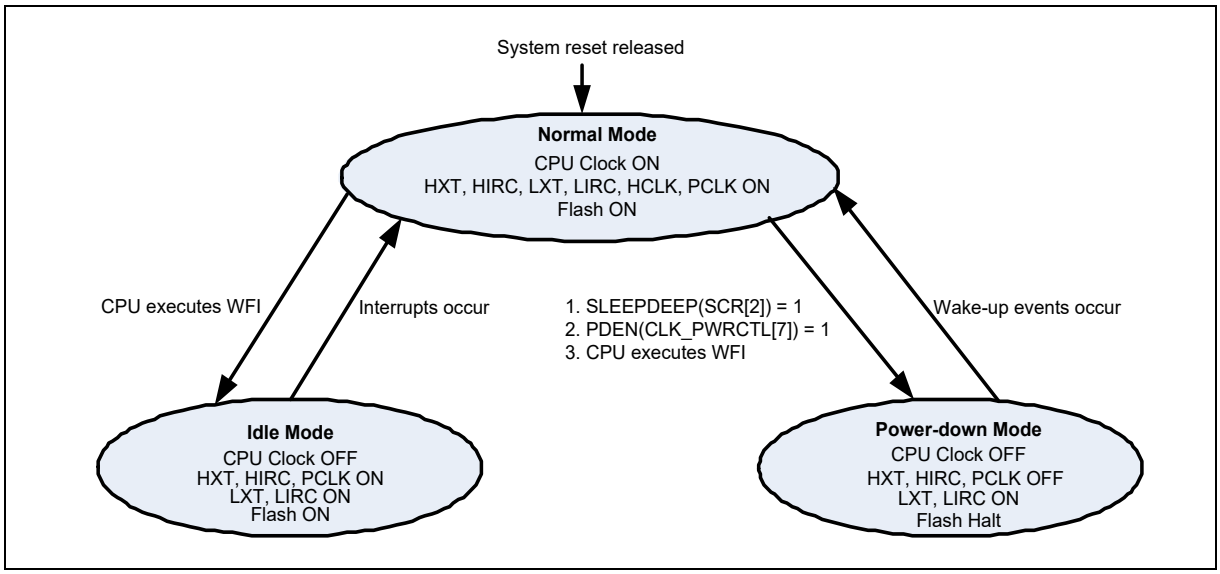


Figure 6.2-8 Power Mode State Machine

	Idle Mode	NPD0, NPD1, NPD2	SPD	DPD
HXT	ON	Halt	Halt	Halt
HIRC	ON	Halt	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]	ON/OFF[2,8]
PLL	ON	Halt	Halt	Halt
HCLK/PCLK	ON	Halt	Halt	Halt
CPU	Halt	Halt	Halt	Halt
SRAM retention	ON	ON	ON/OFF[7]	Halt
FLASH	ON	Halt	Halt	Halt
TIMER	ON	ON/OFF[3]	Halt	Halt
WDT	ON	ON/OFF[4]	Halt	Halt
RTC	ON	ON/OFF[5]	ON/OFF[9]	Halt
UART	ON	ON/OFF[6]	Halt	Halt
Others	ON	Halt	Halt	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on software setting in normal mode.

2. LIRC ON or OFF depends on software setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
5. If RTC clock source is selected as LIRC/LXT and LIRC/LXT is on.
6. If UART clock source is selected as LXT and LXT is on.
7. SRAM retention size depends on software setting in normal mode.
8. If timer wake-up function is disabled, LIRC will be disabled automatically when chip enters DPD mode for power saving.
9. If RTC clock source is selected as LXT and LXT is on.

Wake-up sources in Normal Power-down mode (NPD):

RTC, WDT, I²C, Timer, UART, USCI, BOD, GPIO, INT, SDH, ACMP, HSUSBD, HSUSBH, HSOTG, WKTMR and WKIO.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode			Re-Entering Power-Down Mode Condition
		NPD0/ NPD1/ NPD2	SPD	DPD	
BOD	Brown-Out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	V	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
RST pin	RST pin Reset	V	-	-	After software writes 1 to clear PINRF (SYS_RSTSTS[1]).
		-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RSTWK (CLK_PMUSTS[15]) when SPD or DPD mode is entered.
INT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
Wake-up I/O (WKIO)	rising or falling edge event	V	-	-	After software writes 1 to clear WKIOxxIF(CLK_PMUINTS[15:8]).
		-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear

					GPxWKx (CLK_PMUSTS[27:24] and CLK_PMUSTS[11:8]) when SPD mode is entered.
GPIO(PC.0/PB.0/PB.2/PB.12/PF.6) Wake-up pin	rising or falling edge event, 5-pin	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear PINWKx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD mode is entered.
VBUS(PA.12)	rising or falling edge event	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear VBUSWK (CLK_PMUSTS[7]) when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer (WKTMR)	Wakeup by wake-up timer time-out	V	-	-	After software writes 1 to clear WKTMRIF (CLK_PMUINTS[1]).
		-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
	Wakeup by RTC tick time	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).

I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
SDH	Card detection	V	-	-	Clear CDIF (SDH_INTSTS[8]) after SDH wake-up.
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMPx_STATUS[8]) and WKIF1 (ACMPx_STATUS[9])
	ACMPO status change	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWKx (CLK_PMUSTS[17:16]) when SPD mode is entered.
HSUSBD	1.V_{BUS} plug in/out 2.USB Resume/Reset	V	-	-	1. After software writes 1 to clear HSUSBD_BUSINTSTS[8](V_{BUS}) 2. After software writes 1 to clear HSUSBD_BUSINTSTS[2](Resume) or HSUSBD_BUSINTSTS[1](Reset)
HSUSBH	1. Remote-wakeup (while port in suspend state) 2. Connector plug-in detect 3. Connector plug-out detect (while port in suspend state) 4. Overcurrent detect	V	-	-	After software writes 1 to clear PCD (HSUSBH_USTSR[2])
HSOTG	ID pin state be change	V	-	-	After software writes 1 to set WKEN(HSOTG_CTL[5]).

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes and Power Level Transition

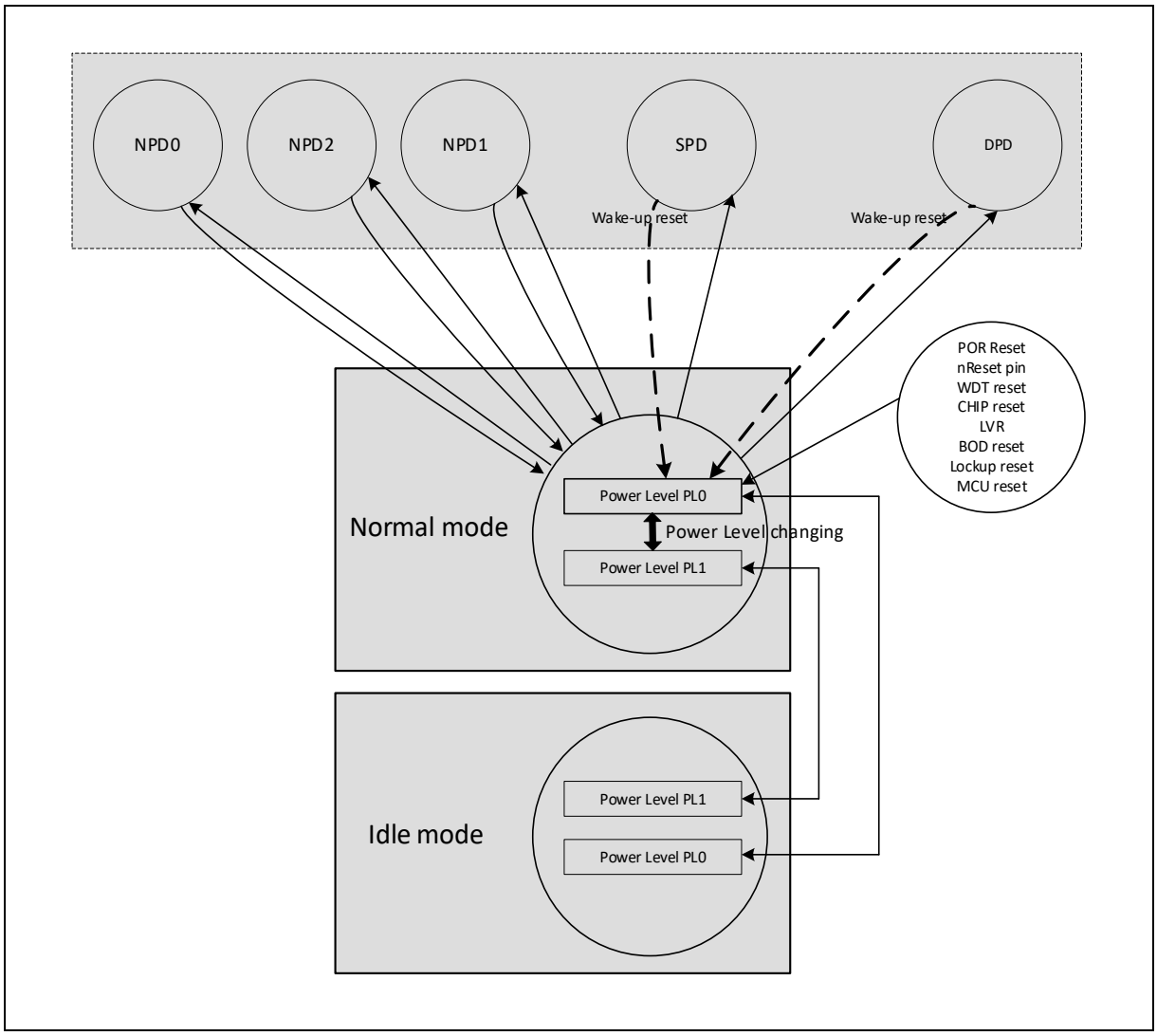


Figure 6.2-9 NuMicro M3331 Power Mode Transition

6.2.6 System Memory Map

The M3331 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M3331 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0007_FFFF	FLASH_BA	FLASH APROM Memory Space
0x0F10_0000 – 0x0F10_1FFF	FLASH_BA	FLASH LDROM Memory Space
0x0080_0000 – 0x0084_FFFF	SRAM_BA	SRAM Memory Space Remapping (320 Kbytes)
0x2000_0000 – 0x2004_FFFF	SRAM_BA	SRAM Memory Space (320 Kbytes)
0x6000_0000 – 0x602F_FFFF	EXTMEM_BA	External Memory Space (3 Mbytes)

Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA0 Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_8000 – 0x4001_8FFF	PDMA1_BA	Peripheral DMA1 Control Registers
0x4001_9000 – 0x4001_9FFF	HSUSBD_BA	HSUSBD Control Registers
0x4001_A000 – 0x4001_AFFF	HSUSBH _BA	HSUSBH Host Control Registers
0x4001_B000 – 0x4001_BFFF	PDCI_BA	Parallel Dimming Communication Interface Control Registers
0x4002_0000 – 0x4002_1FFF	CANFD0_BA	CANFD0 Control Registers
0x4002_4000 – 0x4002_5FFF	CANFD1_BA	CANFD1 Control Registers
0x4002_F000 – 0x4002_FFFF	SCU_BA	SCU Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT0_BA	Watchdog Timer 0 Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_2000 – 0x4004_2FFF	WDT1_BA	Watchdog Timer 1 Control Registers
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I2S0 Interface Control Registers
0x4004_F000 – 0x4004_FFFF	HSOTG_BA	HSOTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4005_C000 – 0x4005_CFFF	BPWM2_BA	BPWM2 Control Registers
0x4005_D000 – 0x4005_DFFF	BPWM3_BA	BPWM3 Control Registers
0x4005_E000 – 0x4005_EFFF	BPWM4_BA	BPWM4 Control Registers

0x4005_F000 – 0x4005_FFFF	BPWM5_BA	BPWM5 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I2C2 Control Registers
0x4008_4000 – 0x4008_4FFF	I3C0_BA	I3C0 Control Registers
0x4008_8000 – 0x4008_8FFF	LLSI0/2/4/6/8_BA	LLSI0/2/4/6/8 Control Registers
0x4008_9000 – 0x4008_9FFF	LLSI1/3/5/7/9_BA	LLSI1/3/5/7/9 Control Registers
0x4008_A000 – 0x4008_AFFF	ELLSI0_BA	ELLSI0 Control Registers
0x4009_6000 – 0x4009_9FFF	WWDT0_BA	Window Watchdog Timer 0 Control Registers
0x4009_8000 –0x4009_8FFF	WWDT1_BA	Window Watchdog Timer 1 Control Registers
0x400B_0000 – 0x400B_0FFF	EQEI0_BA	EQEI0 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 Implementation Defined Attribution Unit (IDAU)

6.2.7.1 Overview

ARMv8-M introduces TrustZone, which allows full isolation of two security levels – Secure and Non-Secure. The memory map security attribute is defined by the combination of:

- Security Attribution Unit (SAU).
- Implementation Defined Attribution Unit (IDAU).

These attribution units define the memory space into four type regions:

- Secure Region: contains Secure program code or data.
- Non-Secure Callable Region (NSC): contains entry functions for Non-Secure programs to access Secure functions.
- Non-Secure Region: contains Non-Secure program code or data.
- Exempt Region: exempt region will be exempted from security check.

Each memory region defined by the SAU and IDAU has a region number generated by the SAU or by the IDAU. Region number is used for determine a group of memory sharing the same security attribute. For testing security attributes and region numbers, a new instruction “TT” (Test Target) is introduced. By using a TT instruction on the start and end addresses of the memory range, and identifying that both reside in the same region number, user can determine the memory range is located entirely in the same range of attribute. For more details, please refer to the ARMv8-M Architecture Reference Manual. The M3331 IDAU memory map attributions and corresponding region numbers are shown in Figure 6.2-10. The address from 0xE000_0000 to 0xFFFF_FFFF is exempt regions and its region number is always not valid, that is, return data bit [23], IRVALID, of TT instruction is always 0.

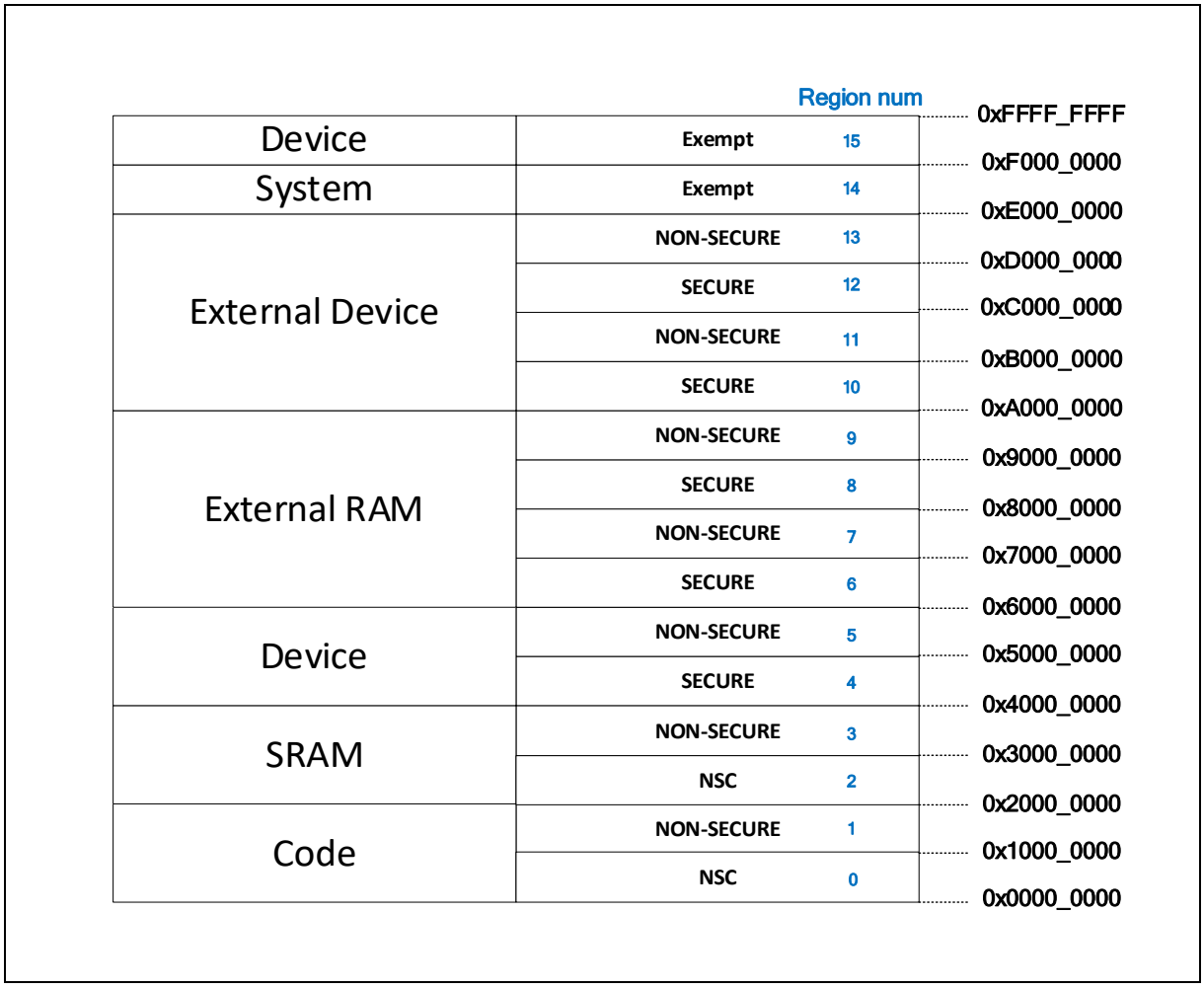


Figure 6.2-10 IDAU Memory Map

6.2.7.2 Block Diagram

The system block diagram is shown in Figure 6.2-11. IDAU is responsible to response the security

property of the address from processor, where the processor compares the security property of the IDAU and SAU, and takes the highest security attribute applied. There are four information IDAU can reply: Secure, Non-Secure Callable, Non-Secure and exempt region; after CPU gets the information of the region security, it will choose the right MPU to control accesses to the address space. The hierarchy of security levels from high to low is: Secure > NSC > Non-Secure.

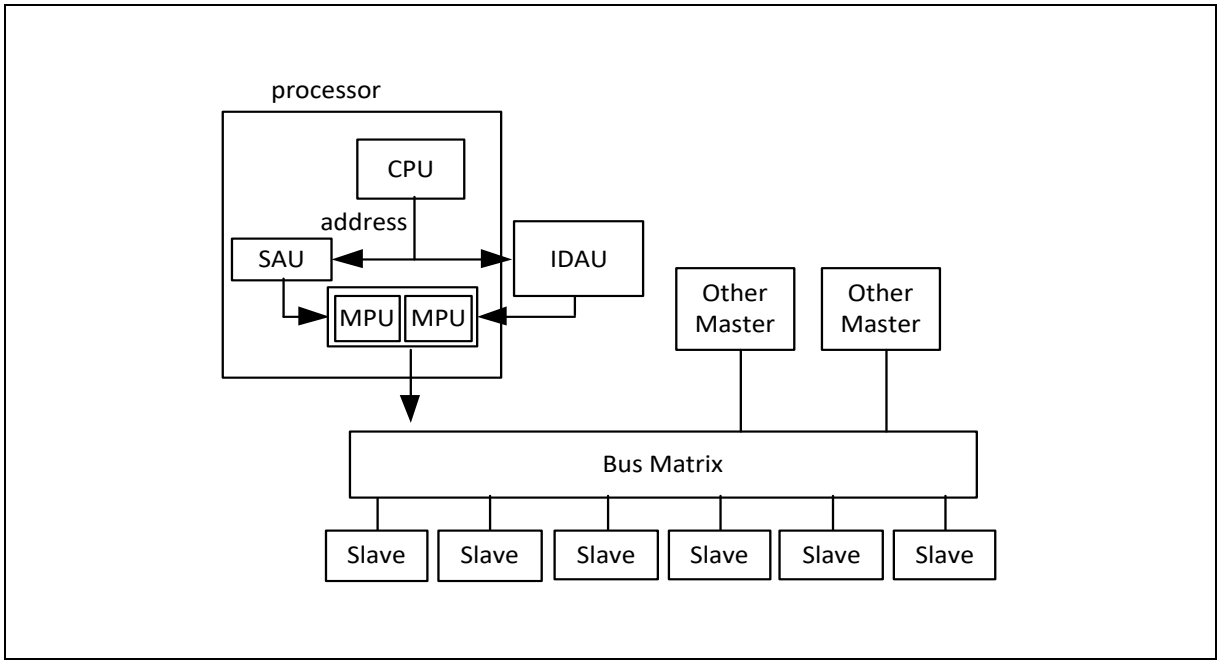


Figure 6.2-11 System Block Diagram

6.2.8 SRAM Memory Organization

The M3331 supports embedded SRAM with total up to 320 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0, SRAM bank1 and SRAM bank2. The first bank has 64 Kbytes address space, the second bank has 128 Kbytes address space and the third bank has 128 Kbytes address space. These three banks address space can be accessed simultaneously. The SRAM bank0 first 64 Kbytes supports parity error check to make sure chip operating more stable.

- Supports total up to 320 Kbytes SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0 first 64 Kbytes at 320 Kbytes device
- Supports oversize response error
- Supports remap address to 0x0080_0000

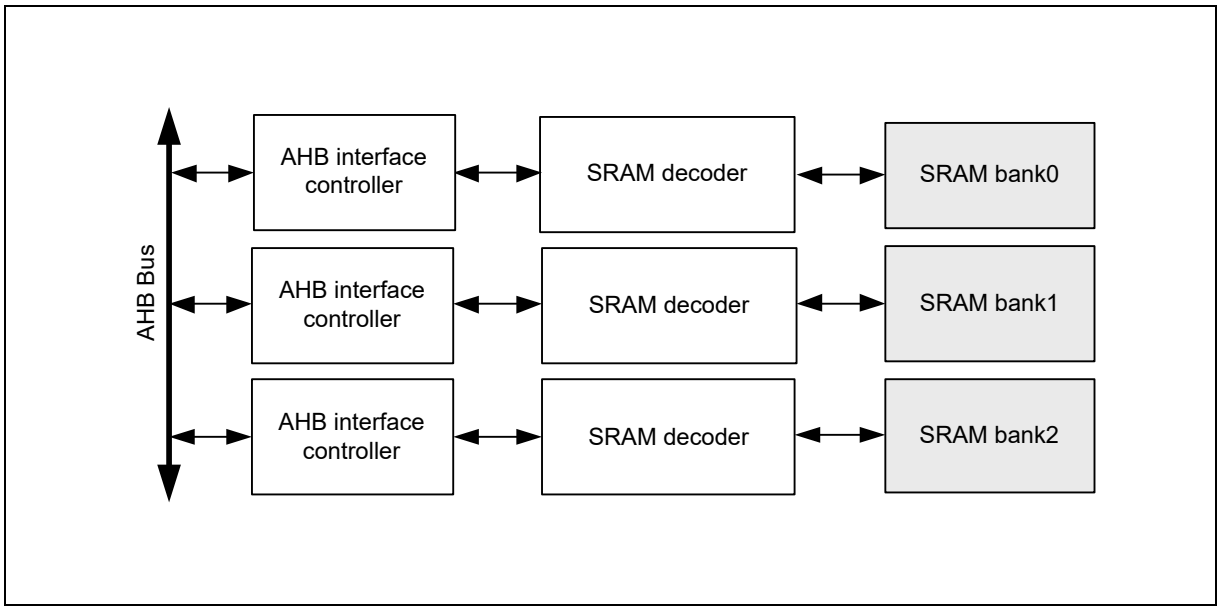


Figure 6.2-12 SRAM Block Diagram

Figure 6.2-12 shows the SRAM organization of M3331. There are three SRAM banks in the M3331. The bank0 is addressed to 64 Kbytes, bank1 is addressed to 128 Kbytes and the bank2 is addressed to 128 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_FFFF (Non-Secure Callable) or 0x3000_0000 to 0x3000_FFFF (Non-Secure). The bank1 address space is from 0x2001_0000 to 0x2002_FFFF (Non-Secure Callable) or 0x3001_0000 to 0x3002_FFFF (Non-Secure). The bank2 address space is from 0x2003_0000 to 0x2004_FFFF (Non-Secure Callable) or 0x3003_0000 to 0x3004_FFFF (Non-Secure). The address between 0x2005_0000 to 0x2FFF_FFFF (Non-Secure Callable) and 0x3005_0000 to 0x3FFF_FFFF (Non-Secure) is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x0080_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2000_FFFF or 0x0080_0000 to 0x0080_FFFF, and access SRAM bank1 through 0x2001_0000 to 0x2002_FFFF or 0x0081_0000 to 0x0082_FFFF and access SRAM bank2 through 0x2003_0000 to 0x2004_FFFF or 0x0083_0000 to 0x0084_FFFF.

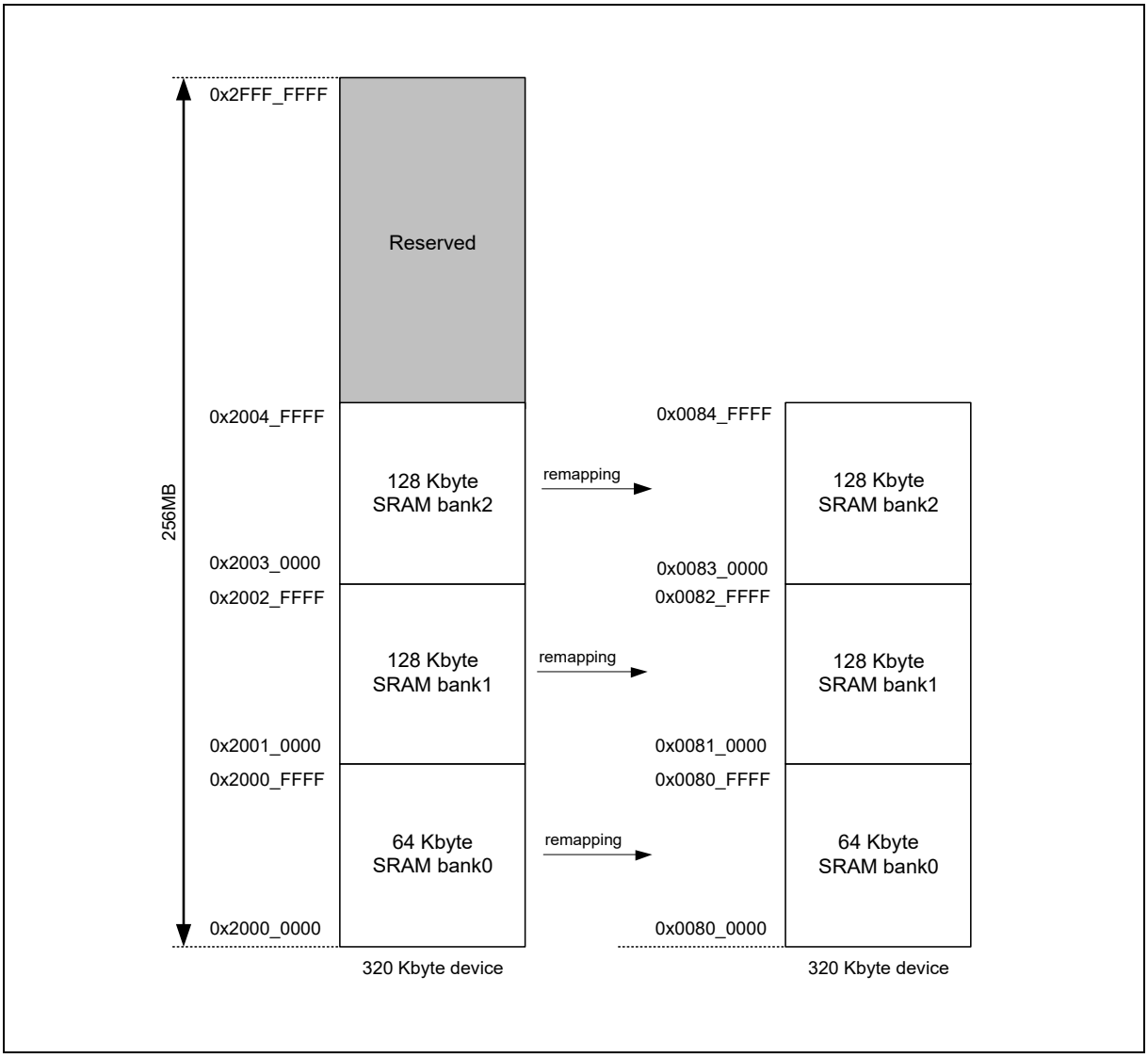


Figure 6.2-13 SRAM Memory Organization for 320 Kbytes Device

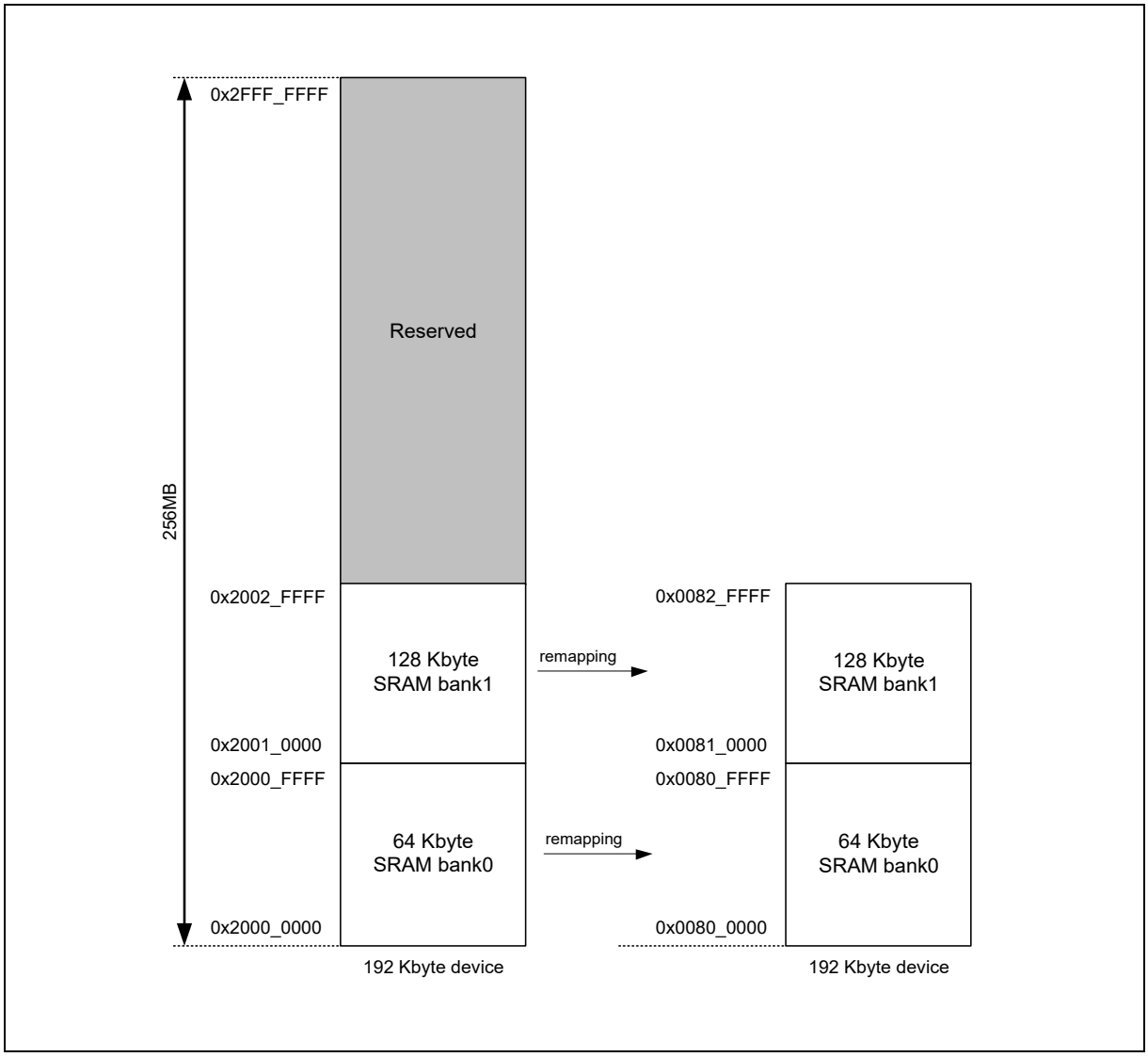


Figure 6.2-14 SRAM Memory Organization for 192 Kbytes Device

The SRAM bank0 first 64 Kbytes has byte parity error check function. When CPU is accessing the first 64 Kbytes of SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF will be asserted to 1 and the System SRAM Parity Error Address register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF bit.

For security consideration, all content in SRAM will be cleaned when chip execute FLASH mass erase.

6.2.9 Bus Matrix

The M3331 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex-M33 CPU as the highest bus priority.

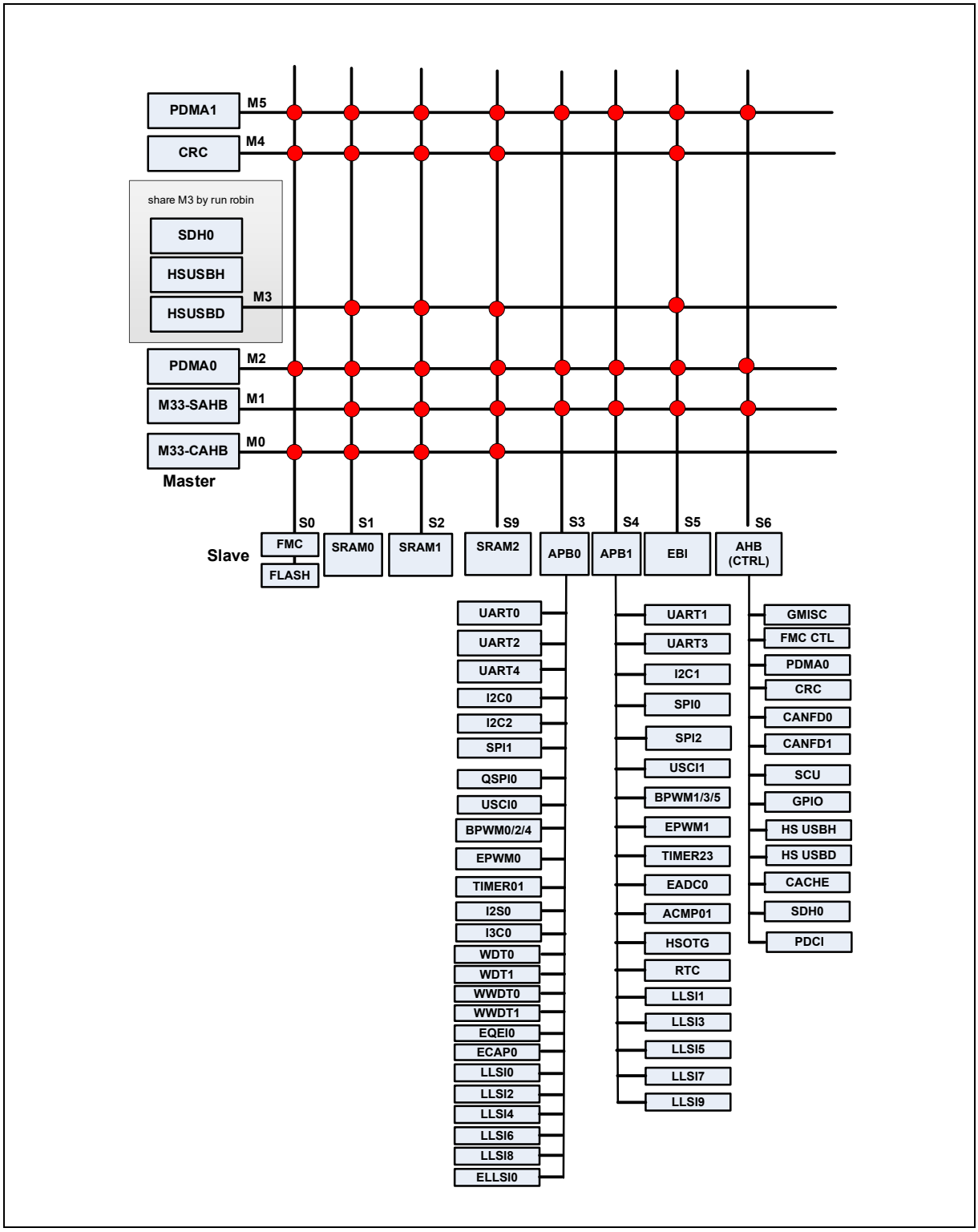


Figure 6.2-15 NuMicro M3331 Bus Matrix Diagram

6.2.10 HIRC Auto Trim

This chip supports auto-trim function: HIRC48M trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator), automatically gets accurate HIRC output frequency, 0.25 %

deviation within all temperature ranges.

In HIRC48M case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.11 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_BODCTL	address 0x4000_0018
SYS_PORCTL	address 0x4000_0024
SYS_VREFCTL	address 0x4000_0028
SYS_USBPHY	address 0x4000_002C
SYS_VTORSET	address 0x4000_00A8
SYS_SRAM_LSCTL	address 0x4000_00CC
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_PORDISAN	address 0x4000_01EC
SYS_PLCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_CLKDSTS	address 0x4000_0274
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
FMC_APWPROT0	address 0x4000_C110
FMC_APWPROT1	address 0x4000_C114
FMC_APWPKEEP	address 0x4000_C118
FMC_SCACT	address 0x4000_C11C
FMC_LDWPROT	address 0x4000_C120
FMC_LDWPKEEP	address 0x4000_C124

FMC_DFWPROT	address 0x4000_C128
FMC_DFWPKEEP	address 0x4000_C12C
FMC_ECCCTL	address 0x4000_C130
WDT_CTL	address 0x4004_0000/0x4004_2000
WDT_ALTCTL	address 0x4004_0004/0x4004_2004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170
TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8

EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC
EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC
BPWM_CTL0	address 0x4005_A000/0x4005_B000/0x4005_C000/0x4005_D000/0x4005_E000/0x4005_F000

6.2.12 Wake-up Timer (WKTMR) and Wake-up I/O (WKIO) Function

The WKTMR function can be enabled by WKTMREN (CLK_PMUCTL[8]), WKTMRMOD (CLK_PMUCTL[13]) and WKTMRIS (CLK_PMUCTL[12:9]). WKTMR can wake-up chip from NPD0/NPD1/NPD2/SPD/DPD modes.

When WKTMR wake-up event occurred in NPD0/NPD1/NPD2 modes, WKTMRIF (CLK_PMUINTS[0]) will be set, and if WKTMRIE (CLK_PMUINTC[0]) is set to 1, ETI interrupt will be triggered. When WKTMR wake-up event occurred in SPD/DPD modes, chip will be reset and re-run. Users can check wakeup flag from TMRWK (CLK_PMUSTS[1]).

The WKIO function can be enabled by CLK_PAPWCTL, CLK_PBPWCTL, CLK_PCPWCTL, CLK_PDPWCTL and CLK_PWDBCTL. WKIO can wakeup chip from NPD0/NPD1/NPD2/SPD modes.

When WKIO event occurred in NPD0/NPD1/NPD2 modes, WKIOxxIF(CLK_PMUINTS[15:8]

will be set, and if any of WKIO interrupt enable (CLK_PMUINTC[15:8]) is set to 1, ETI interrupt will be triggered. When WKIO wake-up event occurred in SPD modes, chip will be reset and re-run. Users can check wakeup flag from GPxWKx (CLK_PMUSTS[27:24], CLK_PMUSTS[11:8]).

6.2.13 System Timer (SysTick)

The Cortex-M33 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm Cortex-M33 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.2.14 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-480 interrupts.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.14.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by M3331 Series. Software can set 256 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xE0” (The 5-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000000 to 0xFFFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-4
NMI	2	0x00000008	-2
Secure HardFault when AIRCR.BFHFNMINS is 1	3	0x0000000C	-3
Secure HardFault when AIRCR.BFHFNMINS is 0			-1
Hard Fault			-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable

Usage Fault	6	0x00000018	Configurable
Secure Fault	7	0x0000001C	Configurable
Reserved	8 ~ 10	-	Reserved
SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13	-	Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt(IRQ0~IRQ142)	16 ~ 158	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	FMC_ISP_INT	FMC ISP interrupt
22	6	RTC_INT	Real time clock interrupt
23	7	Reserved	Reserved
24	8	WDT0_INT	Watchdog Timer 0 interrupt
25	9	WWDT0_INT	Window Watchdog 0 Timer interrupt
26	10	EINT0	External interrupt from INT0 pin
27	11	EINT1	External interrupt from INT1 pin
28	12	EINT2	External interrupt from INT2 pin
29	13	EINT3	External interrupt from INT3 pin
30	14	EINT4	External interrupt from INT4 pin
31	15	EINT5	External interrupt from INT5 pin
32	16	GPA_INT	External interrupt from PA pin
33	17	GPB_INT	External interrupt from PB pin
34	18	GPC_INT	External interrupt from PC pin
35	19	GPD_INT	External interrupt from PD pin

36	20	GPE_INT	External interrupt from PEpin
37	21	GPF_INT	External interrupt from PF pin
38	22	QSPI0_INT	QSPI0 interrupt
39	23	SPI0_INT	SPI0 interrupt
40	24	BRAKE0_INT	EPWM0 brake interrupt
41	25	EPWM0_P0_INT	EPWM0 pair 0 interrupt
42	26	EPWM0_P1_INT	EPWM0 pair 1 interrupt
43	27	EPWM0_P2_INT	EPWM0 pair 2 interrupt
44	28	BRAKE1_INT	EPWM1 brake interrupt
45	29	EPWM1_P0_INT	EPWM1 pair 0 interrupt
46	30	EPWM1_P1_INT	EPWM1 pair 1 interrupt
47	31	EPWM1_P2_INT	EPWM1 pair 2 interrupt
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA0_INT	PDMA0 interrupt
57	41	Reserved	Reserved
58	42	EADC0_INT0	EADC0 interrupt source 0
59	43	EADC0_INT1	EADC0 interrupt source 1
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	Reserved	Reserved
62	46	EADC0_INT2	EADC0 interrupt source 2
63	47	EADC0_INT3	EADC0 interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	UART3_INT	UART3 interrupt
66	50	Reserved	Reserved
67	51	SPI1_INT	SPI1 interrupt
68	52	SPI2_INT	SPI2 interrupt
69	53	Reserved	Reserved
70	54	USBH_INT	USB host interrupt

71	55	Reserved	Reserved
72	56	ETI_INT	External trigger interrupt
73	57	CRC_INT	CRC interrupt
74	58	Reserved	Reserved
75	59	NS_FMC_ISP_INT	Non-secure FMC ISP interrupt
76	60	SCU_INT	Security configuration unit interrupt
77	61	Reserved	Reserved
78	62	Reserved	Reserved
79	63	Reserved	Reserved
80	64	SDHOST0_INT	SD host 0 interrupt
81	65	HSUSBD_INT	HSUSBD interrupt
82	66	Reserved	Reserved
83	67	WDT1_INT	Watchdog Timer 1 interrupt
84	68	I2S0_INT	I2S0 interrupt
85	69	Reserved	Reserved
86	70	Reserved	Reserved
87	71	Reserved	Reserved
88	72	GPG_INT	External interrupt from PG pin
89	73	EINT6	External interrupt from INT6 pin
90	74	UART4_INT	UART4 interrupt
91	75	Reserved	Reserved
92	76	USCI0_INT	USCI0 interrupt
93	77	USCI1_INT	USCI1 interrupt
94	78	BPWM0_INT	BPWM0 interrupt
95	79	BPWM1_INT	BPWM1 interrupt
96	80	Reserved	Reserved
97	81	Reserved	Reserved
98	82	I2C2_INT	I2C2 interrupt
99	83	Reserved	Reserved
100	84	EQEI0_INT	EQEI0 interrupt
101	85	Reserved	Reserved
102	86	ECAP0_INT	ECAP0 interrupt
103	87	Reserved	Reserved
104	88	GPH_INT	External interrupt from PH pin

105	89	EINT7	External interrupt from INT7 pin
106	90	Reserved	Reserved
107	91	WWDT1_INT	Window Watchdog 1 Timer interrupt
108	92	HSUSBH_INT	HSUSBH interrupt
109	93	HSOTG_INT	HSOTG interrupt
110	94	Reserved	Reserved
111	95	Reserved	Reserved
112	96	NS_SRAM_PERR	Non-secure SRAM parity check error interrupt
113	97	Reserved	Reserved
114	98	PDMA1_INT	PDMA1 interrupt
115	99	Reserved	Reserved
116	100	Reserved	Reserved
117	101	Reserved	Reserved
118	102	Reserved	Reserved
119	103	Reserved	Reserved
120	104	Reserved	Reserved
121	105	Reserved	Reserved
122	106	Reserved	Reserved
123	107	Reserved	Reserved
124	108	I3C0_INT	I3C0 interrupt
125	109	Reserved	Reserved
126	110	Reserved	Reserved
127	111	Reserved	Reserved
128	112	CANFD0_INT0	CANFD0 interrupt source 0
129	113	CANFD0_INT1	CANFD0 interrupt source 1
130	114	CANFD1_INT0	CANFD1 interrupt source 0
131	115	CANFD1_INT1	CANFD1 interrupt source 1
132	116	Reserved	Reserved
133	117	Reserved	Reserved
134	118	Reserved	Reserved
135	119	PDCI_INT	PDCI interrupt
136	120	Reserved	Reserved
137	121	Reserved	Reserved
138	122	Reserved	Reserved
139	123	Reserved	Reserved

140	124	Reserved	Reserved
141	125	Reserved	Reserved
142	126	Reserved	Reserved
143	127	Reserved	Reserved
144	128	LLSI0_INT	LED Light Strip Interface interrupt source 0
145	129	LLSI1_INT	LED Light Strip Interface interrupt source 1
146	130	LLSI2_INT	LED Light Strip Interface interrupt source 2
147	131	LLSI3_INT	LED Light Strip Interface interrupt source 3
148	132	LLSI4_INT	LED Light Strip Interface interrupt source 4
149	133	LLSI5_INT	LED Light Strip Interface interrupt source 5
150	134	LLSI6_INT	LED Light Strip Interface interrupt source 6
151	135	LLSI7_INT	LED Light Strip Interface interrupt source 7
152	136	LLSI8_INT	LED Light Strip Interface interrupt source 8
153	137	LLSI9_INT	LED Light Strip Interface interrupt source 9
154	138	ELLSI0_INT	Enhanced LED Light Strip Interface interrupt source 0
155	139	BPWM2_INT	BPWM2 interrupt
156	140	BPWM3_INT	BPWM3 interrupt
157	141	BPWM4_INT	BPWM4 interrupt
158	142	BPWM5_INT	BPWM5 interrupt

Table 6.2-9 Interrupt Number Table

6.2.14.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.15 System Control Register

The Cortex-M33 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex-M33 interrupt priority and Cortex-M33 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm Cortex-M33 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex-M33 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC) and PLL to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

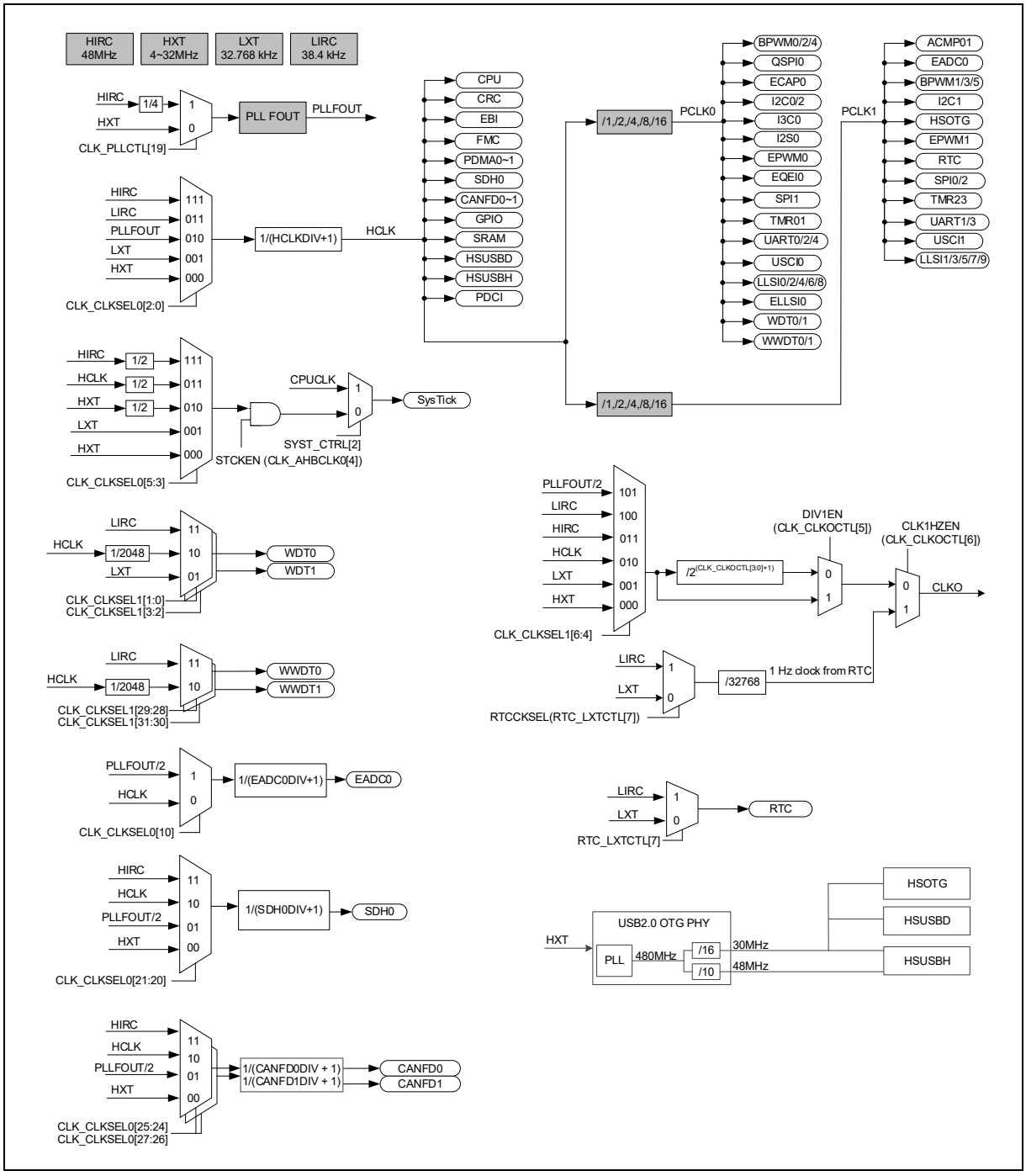


Figure 6.3-1 Clock Generator Global View Diagram (1/2)

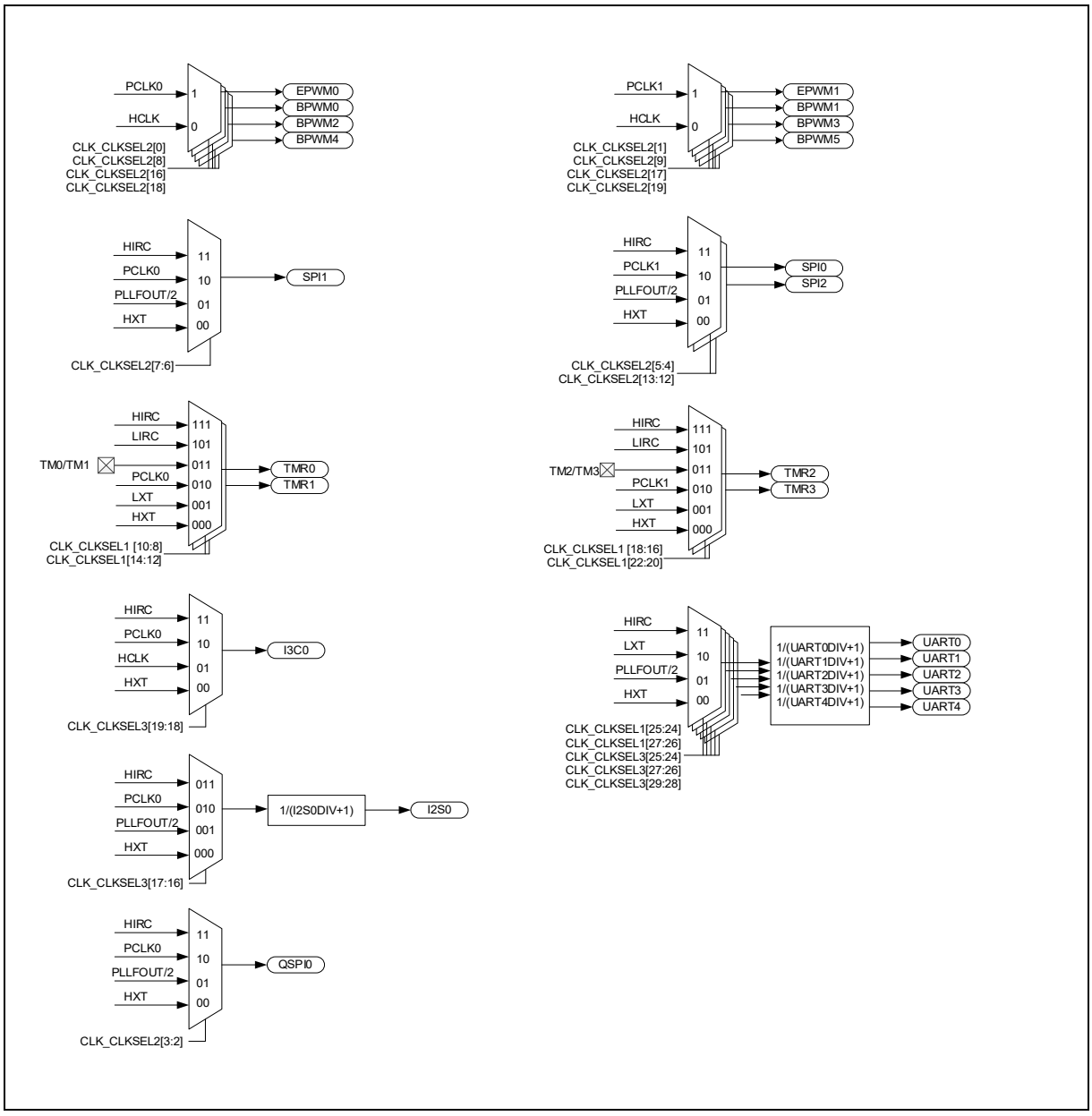


Figure 6.3-2 Clock Generator Global View Diagram (2/2)

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~32 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator (HIRC)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index is set to 1 after stable counter value reach a define value as shown in Table 6.3-1.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-2 will auto clear when user disables the clock source.

Besides, the clock stable index of HXT, HIRC and PLL will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clocks	341.33us for 12 MHz
LXT	16384 LXT clocks	500ms for 32.768 kHz
PLL	1200 PLL source clocks (CLK_PLLCTL[23]=0) 2400 PLL source clocks (CLK_PLLCTL[23]=1)	100us for 12 MHz 200us for 12 MHz
LIRC	1 LIRC clock	26.04us for 38.4 kHz
HIRC	256 HIRC clocks (CLK_PWRCTL[17:16]=0x0) 128 HIRC clocks (CLK_PWRCTL[17:16]=0x1)	5.33us for 48 MHz 2.67us for 48 MHz

Table 6.3-1 Clock Stable Count Value Table

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
HXT	HXTEN(CLK_PWRCTL[0])	HXTSTB(CLK_STATUS[0])
LXT	LXTEN(CLK_PWRCTL[1])	LXTSTB(CLK_STATUS[1])
PLL	PD(CLK_PLLCTL[16])	PLLSTB(CLK_STATUS[2])
LIRC	LIRCEN(CLK_PWRCTL[3])	LIRCSTB(CLK_STATUS[3])
HIRC	HIRCEN(CLK_PWRCTL[2])	HIRCSTB(CLK_STATUS[4])

Table 6.3-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table

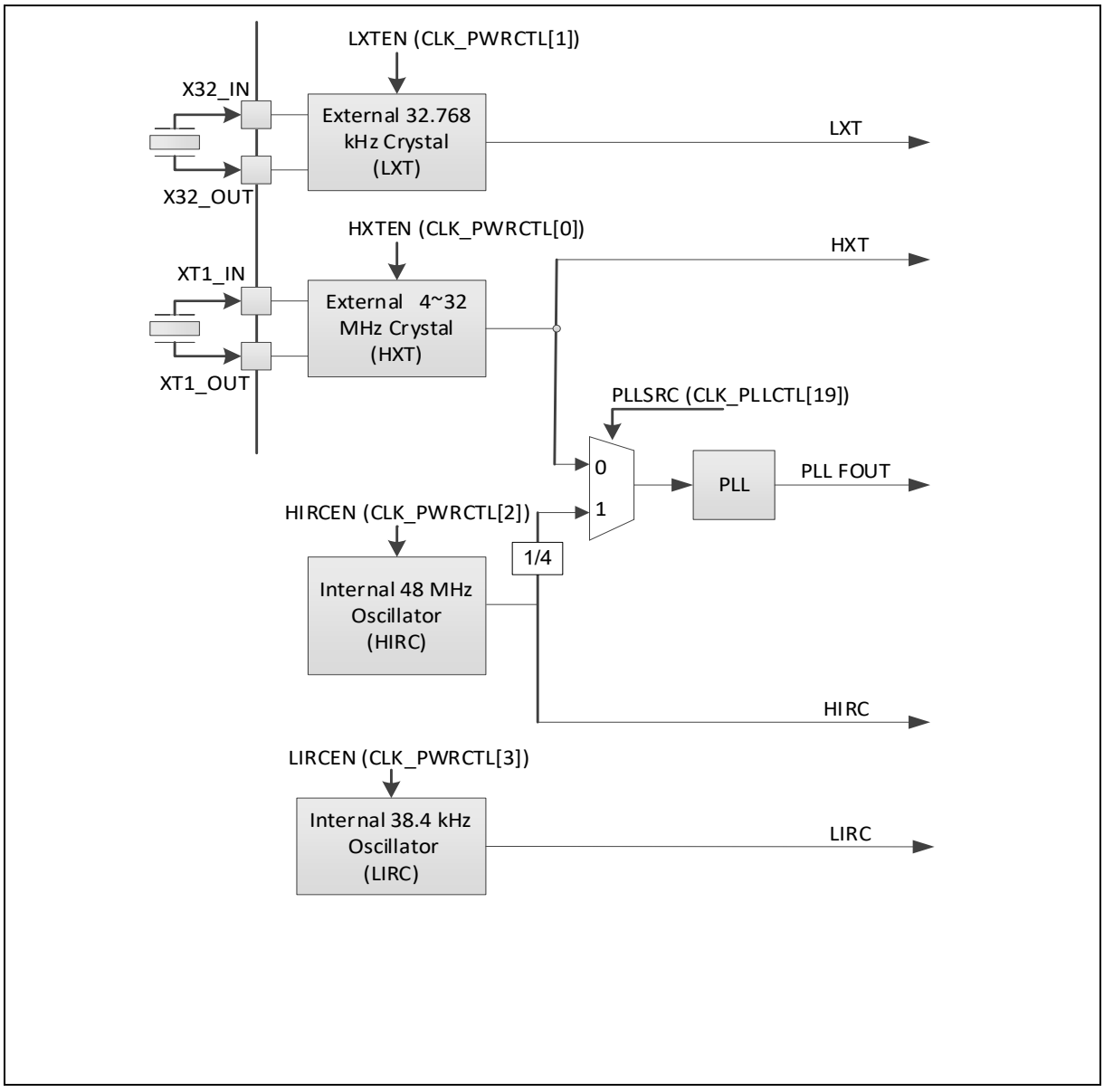


Figure 6.3-3 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-4.

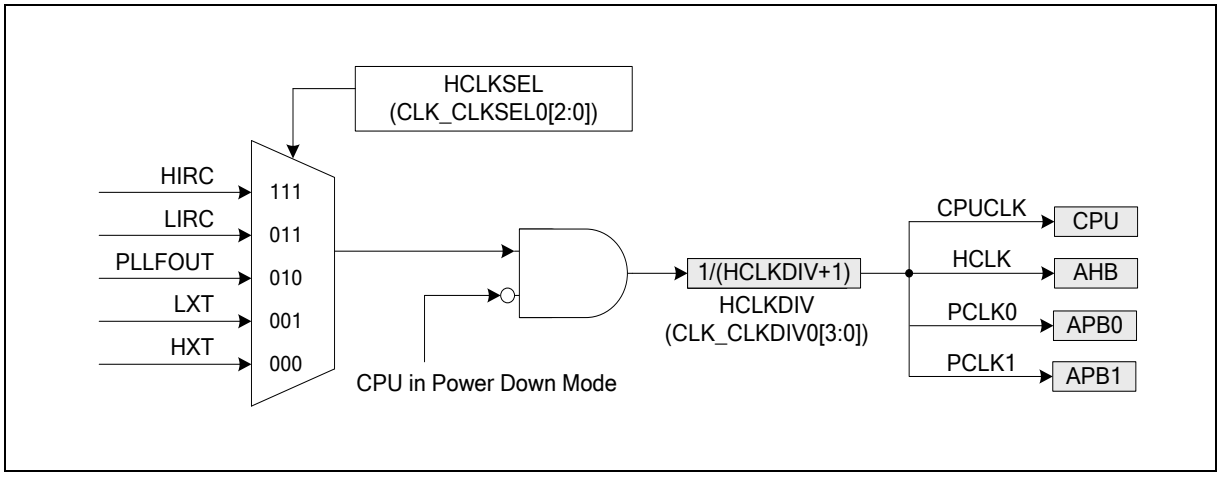


Figure 6.3-4 System Clock Block Diagrams

The clock source of SysTick in Cortex-M33 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

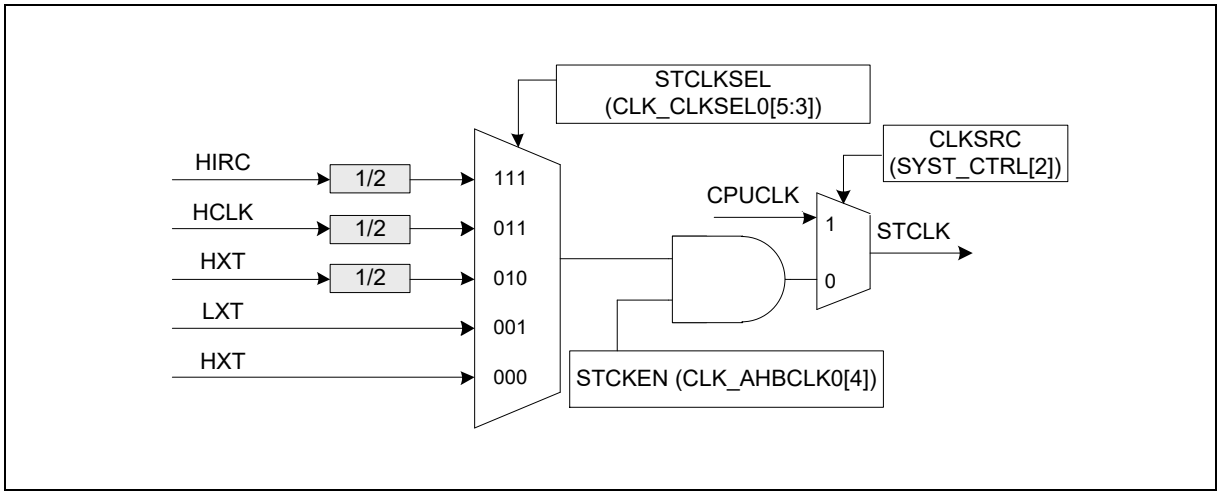


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Clock Fail Detection

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-6 shows that the HXT clock stops detection and system clock switches to HIRC procedure.

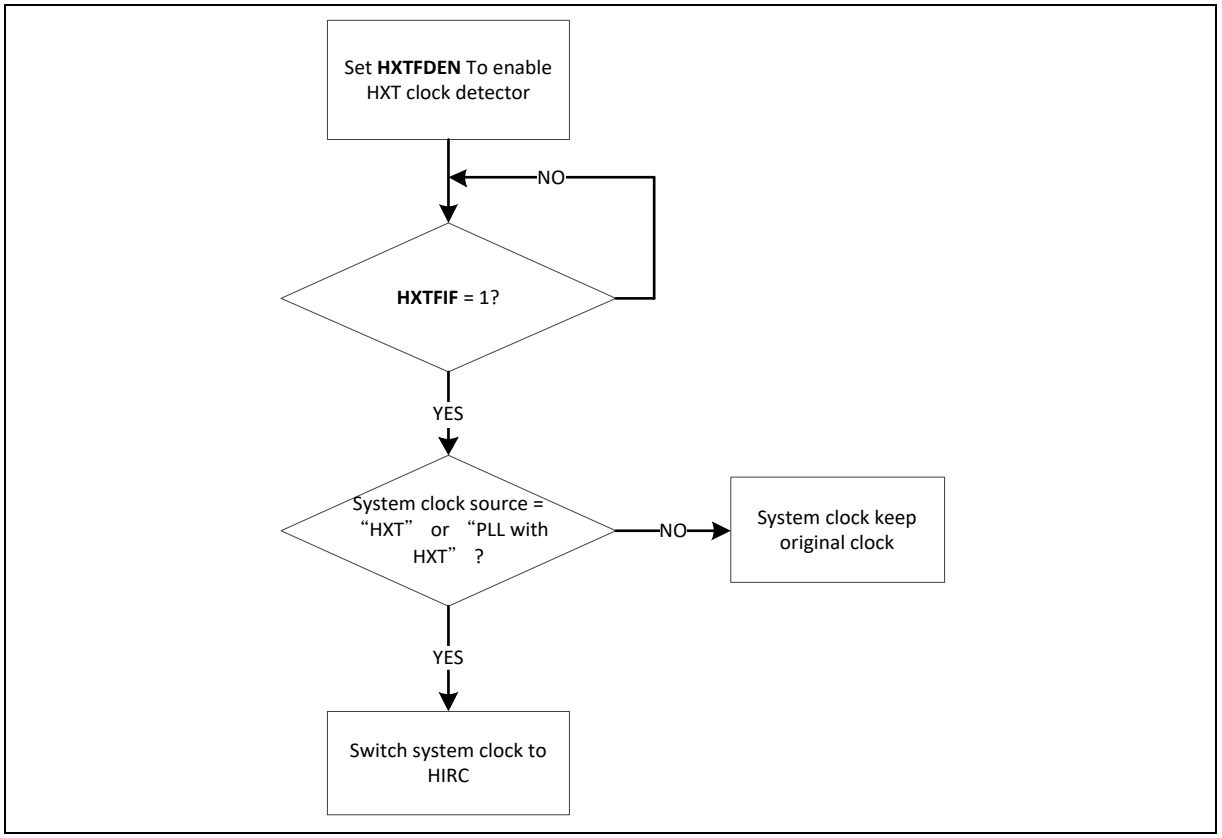


Figure 6.3-6 HXT Stop Protect Procedure

Besides, User can also monitor HXT CLK frequency range by HIRC clock. User can set UPERBD (CLK_CDUPB[10:0]) and LOWERBD (CLK_CDLOWB[10:0]) to decide monitoring frequency window.

The formula of UPERBD and LOWERBD is listed below.

HIRC_period* 1024 < HXT_period* UPERBD

HIRC_period* 1024 > HXT_period* LOWERBD

6.3.5 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 register.

6.3.6 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.7 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT or LIRC.

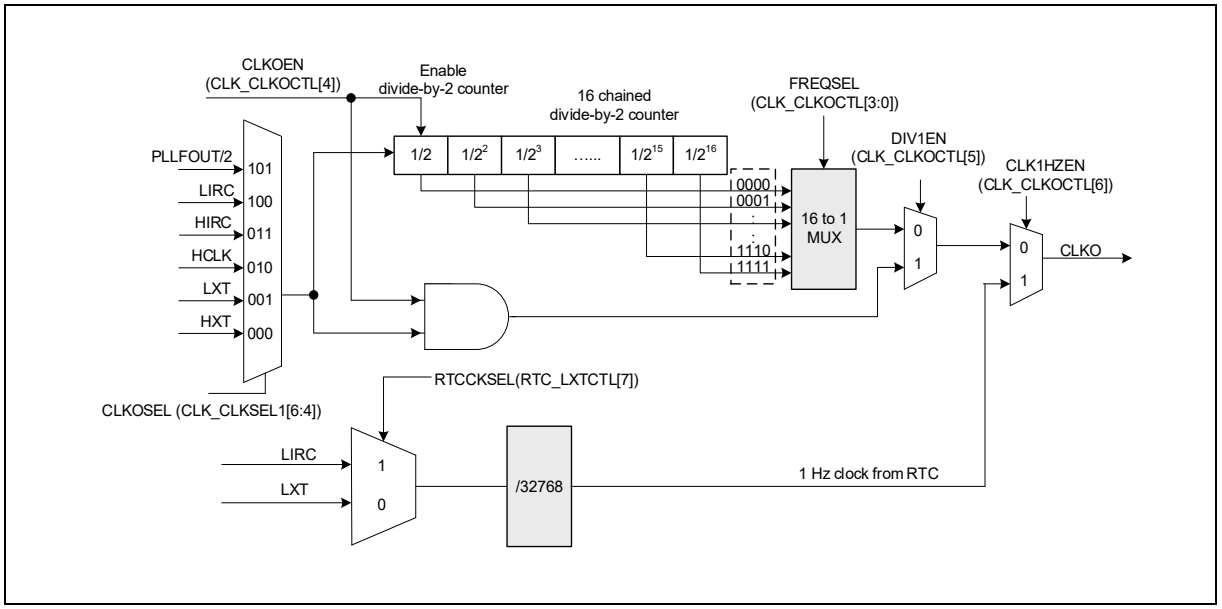


Figure 6.3-7 Clock Output Block Diagram

6.3.8 Share Registers

The clock controller shares part of register information to non-secure world with enable bits in SYSSIAEN (SCU_SINFAEN[1]) register. Shared registers are enabled by default.

Shared Register Access	Clock Controller

R/W	NA
Read only	CLK_PWRCTL, CLK_AHBCLK0, CLK_APBCLK0, CLK_APBCLK1, CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3, CLK_CLKDIV0, CLK_CLKDIV1, CLK_PCLKDIV, CLK_PLLCTL, CLK_STATUS
Write only	NA

Table 6.3-3 Clock Controller Share Register list

6.3.9 USB Clock Source

The clock sources of USB 2.0 systems are generated from USB2.0 PHY clock. The generated clocks are shown in Figure 6.3-8.

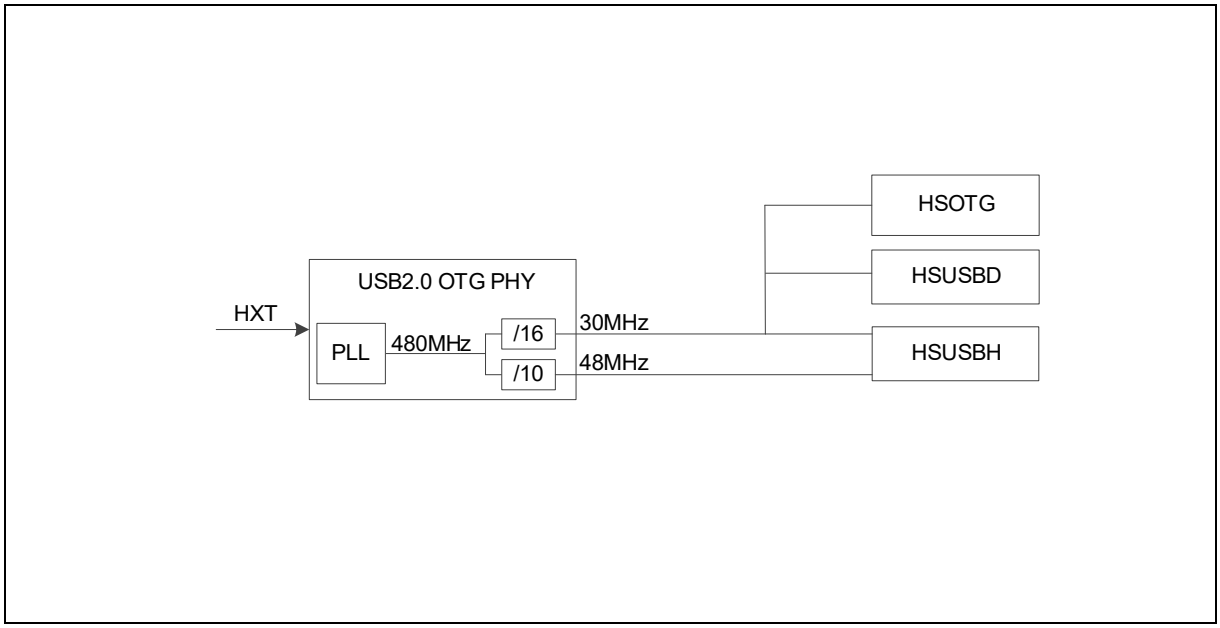


Figure 6.3-8 USB Clock Source

6.4 Security Configuration Unit (SCU)

6.4.1 Overview

Security configuration unit is designed for Arm® TrustZone®, and used to configure the security attribution of SRAM, GPIO as well as all other peripherals. SCU also collects AHB slaves' security violation response and generates SCU interrupt. SCU is also equipped with a timer to monitor the duration of the core processor in non-secure state.

Note: For details on Arm® TrustZone®, refer to the section "Arm® TrustZone®"

6.4.2 Features

- Configure SRAM's security attribution block by block
- Configure GPIOs' security attribution port by port and EINT's security attribution separately
- Configure peripherals' security attribution
- Generate secure violation interrupt
- Equipped with a 24-bit timer as a non-secure state monitor

6.5 Cache Controller (CACHE)

6.5.1 Overview

The Cache Controller is introduced on C-AHB bus of Cortex-M33 processor to improve memory access performance and reduce power consumption.

6.5.2 Features

- Supports one 32-bit AHB slave port
- Supports one 32-bit AHB master port
- Supports zero wait state on cache hits
- Supports LRU replacement (least recently used)
- Supports write-through policy
- Supports 32-bit hit monitor counter
- Supports 16-bit miss monitor counter
- Supports critical-word-first refill policy

Feature	CACHE
Number of ways	2
Cache size	4 Kbytes
Cache line width	8 bytes
Data width of AHB slave port	32 bits
Data width of AHB master port	32 bits

Table 6.5-1 CACHE Features

6.6 External Bus Interface (EBI)

6.6.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.6.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplex mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.7 Flash Memory Controller (FMC)

6.7.1 Overview

The FMC is equipped with 256/512 Kbytes on-chip embedded Flash for application. A 4 Kbytes Data Flash to store some application dependent data. A User Configuration block provides for system initiation. A 8 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 32 Kbytes Boot Loader consists of native ISP functions and secure boot function. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.7.2 Features

- Supports Bank Remap
- Supports 256/512 Kbytes application ROM (APROM)
- Supports 8 Kbytes loader ROM (LDROM)
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM
- Supports 4 Kbytes Data Flash
- Supports User Configuration block to control system initiation
- Supports 1 Kbyte page erase for all embedded Flash
- Supports Error Correction Code for APROM, LDROM and Data Flash
- Supports bank erase for APROM, except if XOM regions is set
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for code integrity and authenticity
- Supports 32-bit Flash programming function
- Supports 64-bit Flash programming function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

This chip has up to 110 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB and PE has 16 pins on port. PC and PD has 15 pins on port. PF has 14 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of these pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Please refer to the Datasheet for detailed pin operation voltage information about V_{DD}, V_{DDIO} and V_{BAT} electrical characteristics.

6.8.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports EINT0~7 edge detect and trigger function

6.9 PDMA Controller (PDMA)

6.9.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. Each PDMA channel can perform transfer between memory and peripherals or between memory and memory. Devices with 512 KB APROM implement one PDMA controller (PDMA0) with 16 channels. Devices with 256 KB APROM implement two PDMA controllers (PDMA0 and PDMA1) with 9 channels.

6.9.2 Features

- Supports 9/16 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and PDCI, ELLSI, LLSI, USB, UART, USCI, SPI, QSPI, ACMP, EINT, EPWM, I^2C, I3C, I^2S, Timer, and EADC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on all channels
- Supports stride function from channel 0 to channel 5
- Supports enhanced stride function on channel 0 and channel1

6.10 Timer Controller (TMR)

6.10.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.10.2 Features

6.10.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- Supports 3-bit capture input noise filter
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, EADC and PDMA function
- Supports Timer0 ~ Timer3 time-out interrupt signal forced output to EQEI in the M3331GA series
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP or internal USB SOF signal
- Supports internal capture triggered source from ACMP output, HXT, HIRC, LIRC and LXT.
- Supports over-capture flag

6.10.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale

- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error, FMC ECC double error detection and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports PWM output accumulator event to trigger PDMA transfer
- Supports PWM output accumulator event to stop PWM counting
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events
- Supports External Pin event to trigger PWM counter action

6.11 Basic PWM Generator and Capture Timer (BPWM)

6.11.1 Overview

The chip provides six BPWM generators. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.11.2 Features

6.11.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum HCLK frequency.
- Supports up to six BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.11.2.2 Capture Function Features

- Supports up to 36 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.12 EPWM Generator and Capture Timer (EPWM)

6.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.12.2 Features

6.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum HCLK frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion independent control with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator, EADC and system safety events (clock failed, SRAM parity error, Brown-out detection, FMC ECC Double error and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value
  - Supports EPWM trigger EADC event prescaler feature
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect function
- Supports External Pin Trigger Function

6.12.2.2 Capture Function Features

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.13 Enhanced Input Capture Timer (ECAP)

6.13.1 Overview

The chip provides up to one unit of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.13.2 Features

- Up to one Input Capture Timer/Counter unit, CAP0
- Each unit has 3 input channels
- Each unit has its own interrupt vector
- Each input channel has its own capture counter hold register
- 24-bit Input Capture up-counting timer/counter
- With noise filter in front end of input ports
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter
- Supports compare-match function

6.14 Enhanced Quadrature Encoder Interface (EQEI)

6.14.1 Overview

There is one EQEI controller in this device. The Enhanced Quadrature Encoder Interface (EQEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.14.2 Features

6.14.2.1 Enhanced Quadrature Encoder Interface (EQEI) Features

- Up to one EQEI controller, EQEI0.
- Two EQEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (EQEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (EQEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (EQEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (EQEI_CNTCMP) with a Pre-set Maximum Count Register (EQEI_CNTMAX)
- A 32-bit up count Unit Timer Pulse Counter (EQEI_UTCNT)
- A 32-bit Unit Timer Pulse Counter Compare Register (EQEI_UTCMP)
- One EQEI control register (EQEI_CTL) and one EQEI Status Register (EQEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Supports X4 free-counting mode
  - Supports X2 free-counting mode
  - Supports X4 compare-counting mode
  - Supports X2 compare-counting mode
- Two Quadrature encoder phase counter operation modes:
  - Supports X1 1-phase 2 input compare-counting mode
  - Supports X2 1-phase 2 input compare-counting mode
- Two Quadrature encoder directional counter operation modes:
  - Supports X1 1-phase 1 input compare-counting mode
  - Supports X2 1-phase 1 input compare-counting mode
- Supports swap function for input signals QEA and QEB
- Supports for detecting the occurrence of phase error from input signals QEA and QEB
- Supports one times index signal reset function for Quadrature encoder pulse counter
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clock/8

6.15 Watchdog Timer (WDT)

6.15.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.15.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.42 ms ~ 27.306 s if WDT_CLK = 38.4 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force Secure only WDT (WDT0) enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.16 Window Watchdog Timer (WWDT)

6.16.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.16.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.17 Real Time Clock (RTC)

6.17.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.17.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.

6.18 UART Interface Controller (UART)

6.18.1 Overview

The chip provides five channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports eleven types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.18.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode

UART Feature	UART0	UART1 ~ UART4	USCI-UART
FIFO	16 Bytes	16 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	√	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-
Received Data FIFO reached threshold Time-out Wake-up	√	√	-
Baud Rate Compensation	√	√	-
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.18-1 M3331 Series UART Features

6.19 I²S Controller (I²S)

6.19.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.19.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.20 Secure Digital Host Controller (SDH)

6.20.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SD host can support SD/SDHC and cooperate with DMAC to provide a fast data transfer between system memory and cards.

6.20.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write
- Supports single DMA channel
- Supports hardware Scatter-Gather function
- Using single 128 bytes shared buffer for data exchange between system memory and cards
- Synchronous design for DMA with single clock domain, AHB bs clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock; note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.21 I²C Serial Interface Controller (I²C)

6.21.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are three sets of I²C controllers which support Power-down wake-up function.

6.21.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Up to three I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable
- Supports pin swap function
- Supports Bus Management (SM/PM compatible) function compatible with the SMBUS specification rev 2.0 (http://smbus.org/specs/) and PMBUS specification rev 1.2 (http://pmbus.org/)

6.22 I3C Serial Interface Controller (I3C)

6.22.1 Overview

I3C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The Improved Inter Integrated Circuit (I3C) is part of a group of communication protocols defined by the MIPI Alliance. This specification is developed to ease sensor system design architectures in mobile wireless products by providing a fast, low cost, low power, two-wire digital interface for sensors.

The I3C controller is dual role device and meets the requirement of I3C protocol and I^2C protocol as specified by the MIPI I3C Specification. The specific reference documents is:

- MIPI Alliance Specification for I3C Basic Specification Version 1.1.1

6.22.2 Features

- Supports one I3C port
- Supports Controller and Target mode
- Static or Dynamic Target Device support
- Built-in Hardware Dynamic Address Allocation support
- Built-in CCC transfer handler
- Auto Hot-Join request generation support
- In-Band Interrupt request generation support
- Adaptive mode of operation between I2C and I3C depending on I3C bus traffic
- Built-in TE0-TE5 Error Handling
- Supports Power-down wake-up function
- Supports PDMA mode for data transfer
- Supports SDR mode, data rates up to 12.5 Mbps
- Supports HDR-DDR mode, data rates up to 25 Mbps
- Supports Secondary Controller mode
- Supports Set Static Addess as Dymamic Address CCC
- Supports Target Reset
- Supports Asynchronous Timing Control (Modes 0)
- Supports Grouped Addressing
- Supports HDR-BT mode
- Supports Virtual Targets

6.23 LED Light Strip Interface (LLSI)

6.23.1 Overview

The LLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There are ten sets of LLSI that can be used.

6.23.2 Features

- 10 sets of LLSI channels with IDLE polarity control
- Each LLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer

6.24 Enhanced LED Light Strip Interface (ELLSI)

6.24.1 Overview

The ELLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There is one set of ELLSI that can be used.

The ELLSI also supports LED strip advavanced command protocol, including Set ID Command (SET_ID), Clear ID Command (CLR_ID), Check ID Command (CHK_ID), Specify ID Command (SPE_ID), Feedback Command and TH20 SET Command (TH20_SET), etc.

6.24.2 Features

- One set of ELLSI channels with IDLE polarity control
- ELLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer
- Supports LED advanced command mode (Feedback, TH20 SET Mode, Command mode)
- Configurable advanced command pulse width

6.25 Serial Peripheral Interface (SPI)

6.25.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to 3 sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.25.2 Features

- SPI Mode
  - Up to 3 sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 90 MHz (when chip works at V_{DD} = 2.7V~3.6V)
  - Slave mode up to 45 MHz (when chip works at V_{DD} = 2.7V~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Up to 3 sets of I^2S controllers
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.26 Quad Serial Peripheral Interface (QSPI)

6.26.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains a QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.26.2 Features

- Supports Master or Slave mode operation
- Master mode up to 90 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Slave mode up to 45 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.27 USCI - Universal Serial Control Interface Controller (USCI)

6.27.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.27.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I2C

6.28 USCI – UART Mode

6.28.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.28.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup)

6.29 USCI - SPI Mode

6.29.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

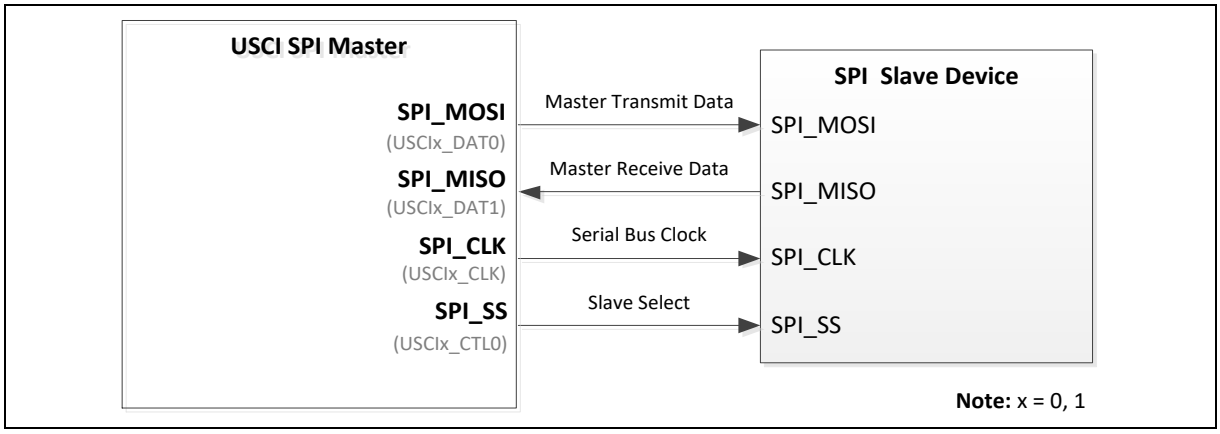


Figure 6.29-1 SPI Master Mode Application Block Diagram

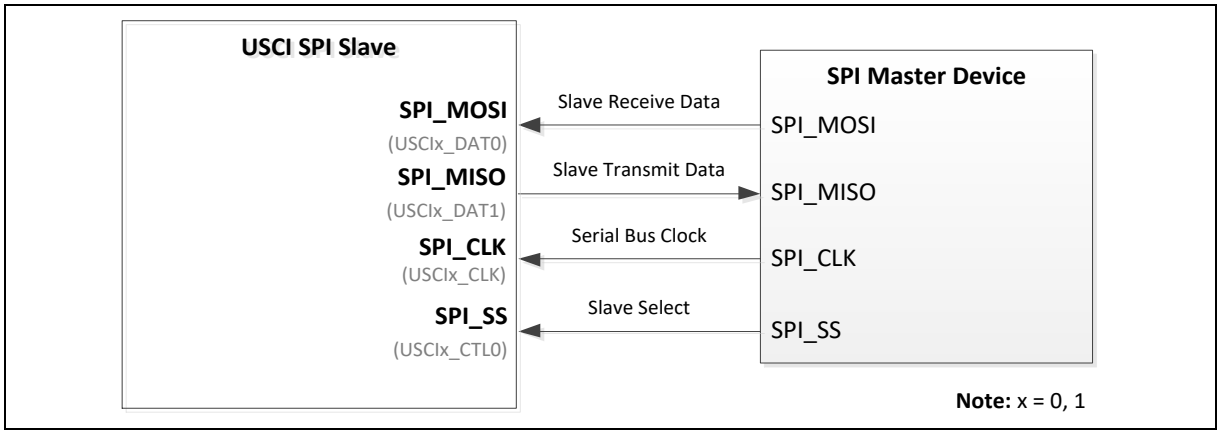


Figure 6.29-2 SPI Slave Mode Application Block Diagram

6.29.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function

- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.30 USCI - I²C Mode

6.30.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.30-1 for more detailed I²C BUS Timing.

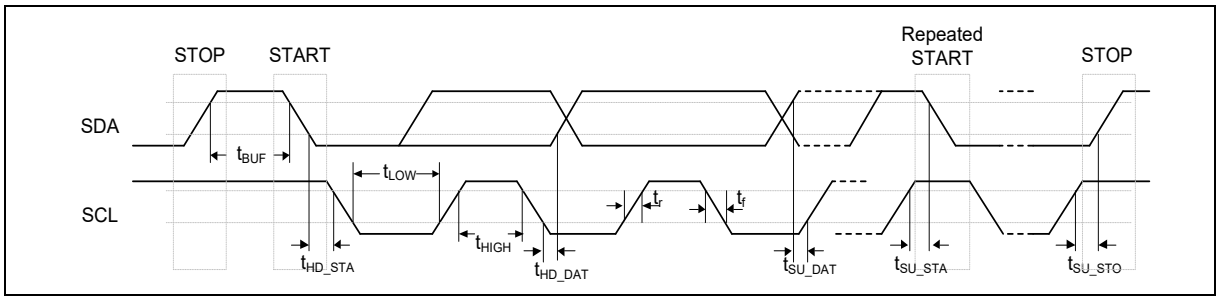


Figure 6.30-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.30.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.31 High Speed USB 2.0 Device Controller (HSUSBD)

6.31.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is compliant with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.31.2 Features

- USB Specification revision 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- Supports Endpoint Maximum Packet Size up to 1024 bytes
- Supports VBUS / Resume wakeup from system power-down mode
- Supports Link Power Management (LPM) feature
- Supports Battery Charging 1.2 (BC1.2) feature

6.32 High Speed USB 2.0 and USB 1.1 Host Controller (HSUSBH and USBH)

6.32.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.32.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.33 High Speed USB 2.0 On-The-Go (HSOTG)

6.33.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in HSUSBROLE (SYS_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID dependent mode, USB frame can be USB Host or USB device depends on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

6.33.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The USB frame can act as USB Host (USB_ID pin is at low) or USB Device (USB_ID pin is at high) only depending on USB_ID pin state. HNP or SRP protocol is not supported.
  - OTG device: It can be A-device (USB_ID pin state is at low) or B-device (USB_ID pin state is at high) depending on USB_ID pin state. HNP and SRP protocols are supported.

6.34 Controller Area Network with Flexible Data-Rate (CAN FD)

6.34.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and need be connected to additional transceiver hardware for the physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.34.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.35 CRC Controller (CRC)

6.35.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with three common polynomials CRC-8, CRC-16, CRC-32 mode and 32-bits programmable polynomials settings.

6.35.2 Features

- Supports three common polynomials CRC-8, CRC-16, and CRC-32 mode
- Programmable seed value
- Programmable polynomials settings
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation
- Supports Master mode

6.36 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.36.1 Overview

The chip contains three 12-bit successive approximation analog-to-digital converters (SAR EADC converter) with 16 external input channels and 3 internal channels. The EADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0~5 triggers, Timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger, external pin (EADC0_ST) input signal, and ACMP0~1 triggers.

6.36.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), and $AV_{DD}/4$.
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 100 MHz for EADC
- Up to 4.5 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage VREF: 1.6V, 2V, 2.5V and 3V.
- Supports power-down mode
- Up to 19 sample modules
  - Sample modules 0~15 is configurable for EADC converter channel (EADC_CH0~15) and trigger source for each EADC
  - Sample module 16~18 is fixed for channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and $AV_{DD}/4$.
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay

counter

- ACMP0 and ACMP1 interrupt pulse triggers

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

6.37 Analog Comparator Controller (ACMP)

6.37.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.37.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV, 10mV, 20mV, 30mV, 40mV,
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 3 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage (V_{BG})
- ACMP1 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 3 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage (V_{BG})
- Shares one ACMP interrupt vector for two comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode
- Supports offset calibration
- Supports ACMP0 event, ACMP1 event be as PDMA request source
- Supports ACMP0 event, ACMP1 event be as EADC trigger source
- Supports ACMP0 output, ACMP1 output be as Timer, ECAP and EPWM trigger source

6.38 Parallel Dimming Communication Interface (PDCI)

6.38.1 Overview

The design purpose of this controller is to realize the function of Biphase Mark Coding (BMC) encoding. This controller contains a total of 24 PDCI channels. Every 4 channels are classified as a group, so there are a total of 6 groups of PDCI channels that can be activated independently.

In order for the system to achieve better application functions, in addition to the delay time and the output channel group location can be adjusted as needed before each channel sends a preamble period can be set by the user. The bit width relationship between data level 0 and data level 1 can be adjusted by the user.

6.38.2 Features

- Supports 24-channel Biphase Mark Coding (BMC) encoding
- 24-channel encoder supports Half Duplex Mode
- Supports 16-channel decoding
- Supports BMC decoding in 4-bit, 5-bit modes
- Supports deglitch filter for decoder
- Implements basic CRC16 using the polynomial X^16 + X^15 + X^2 +1
- Supports PDMA for data transmission
- Configurable preamble bit length
- Configurable delay time before the preamble period
- Configurable channel group output location

6.39 Peripherals Interconnection

6.39.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

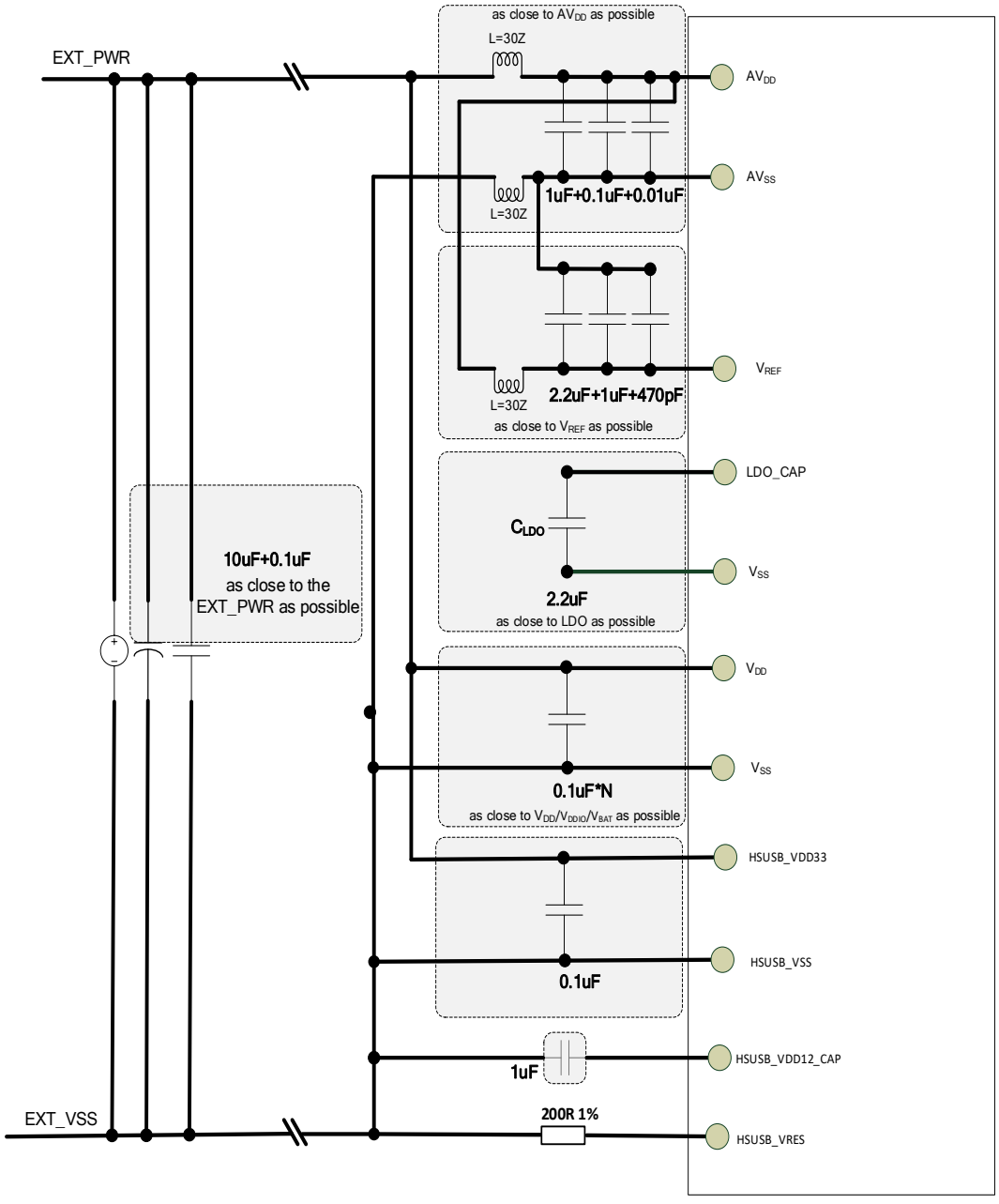
6.39.2 Peripherals Interconnect Matrix Table

Source		Destination									
		EADC	ACMP		TMR	EPWM	BPWM	SYSTEM	ECAP	EQEI	CANFD
		EADC	ACMP	ACMP_CRV	Timer	EPWM	BPWM	HIRCTRIM	ECAP	EQEI	CANFD
ACMP	ACMP	√	-	-	√	√	-	-	√	-	√
	ACMP_CRV	-	√	-	-	-	-	-	-	-	-
CLKCTL	HXT clock fail	-	-	-	√	-	-	-	-	-	-
EADC	EADC	-	-	-	-	√	-	-	-	-	-
EPWM	EPWM	√	-	-	-	√	√	-	-	-	-
EQEI	EQEI	-	-	-	-	-	-	-	√	-	-
GPIO	EINT	-	-	-	√	√	-	-	-	-	-
BPWM	BPWM	√	-	-	-	√	√	-	-	-	-
SYSTEM	LXT	-	-	-	√	-	-	√	-	-	-
	T. Sensor	√	-	-	-	-	-	-	-	-	-
	V_{BG}	√	√	-	-	-	-	-	-	-	-
	Internal V_{REF}	√	-	√	-	-	-	-	-	-	-
	HXT	-	-	-	√	-	-		-	-	-
	HIRC48	-	-	-	√	-	-	-	-	-	-
	LIRC38.4K	-	-	-	√	-	-	-	-	-	-
	BOD	-	-	-	√	√	-	-	-	-	-
	CPU Lockup	-	-	-	√	√	-	-	-	-	-
	SRAM parity error	-	-	-	√	√	-	-	-	-	-
	FMC double ECC detect	-	-	-	√	√	-	-	-	-	-
TMR	Timer	√	-	-	√	√	√	-	-	√	-

Table 6.39-1 Peripherals Interconnect Matrix Table

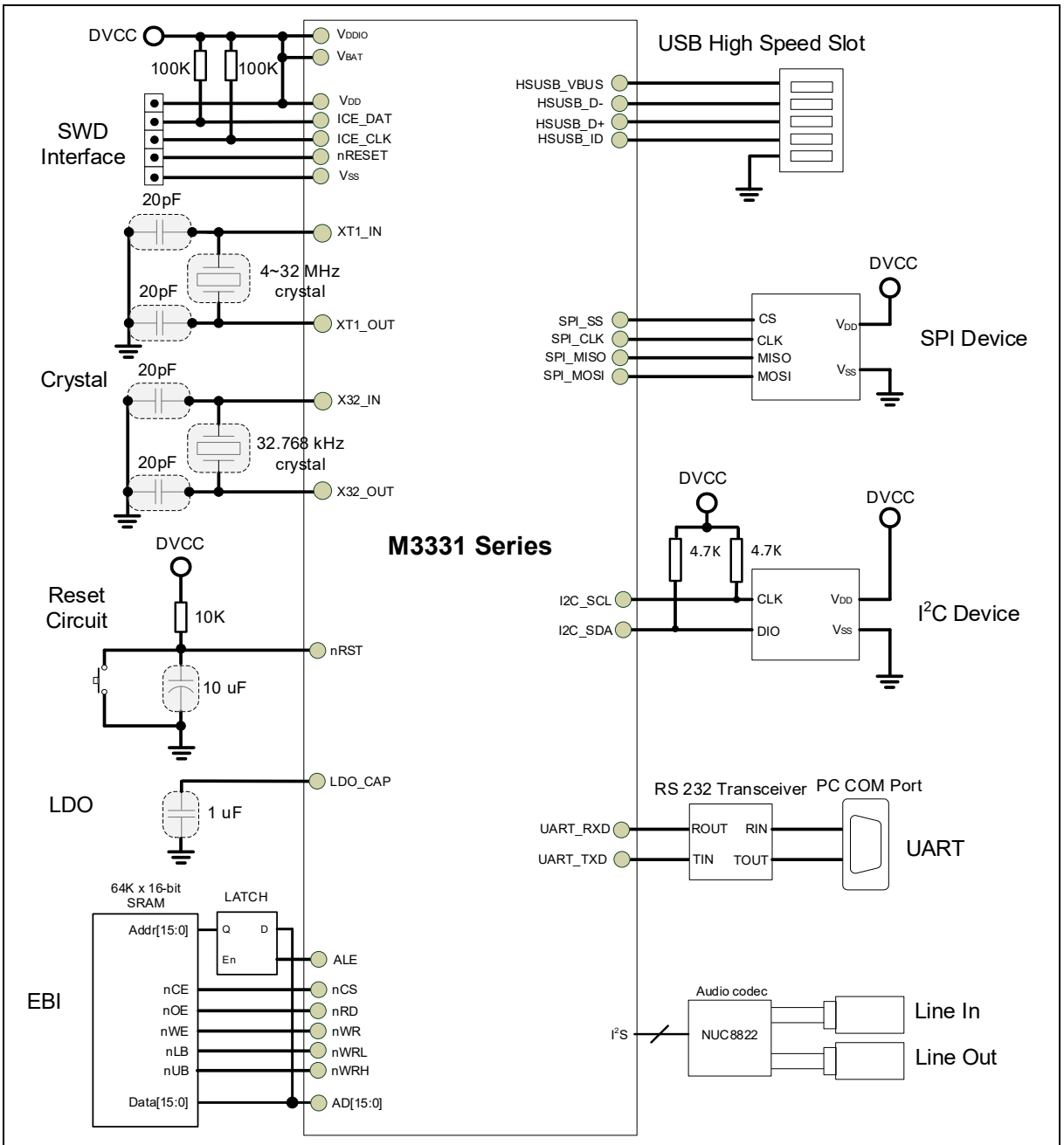
7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



Note: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

7.2 Peripheral Application Scheme

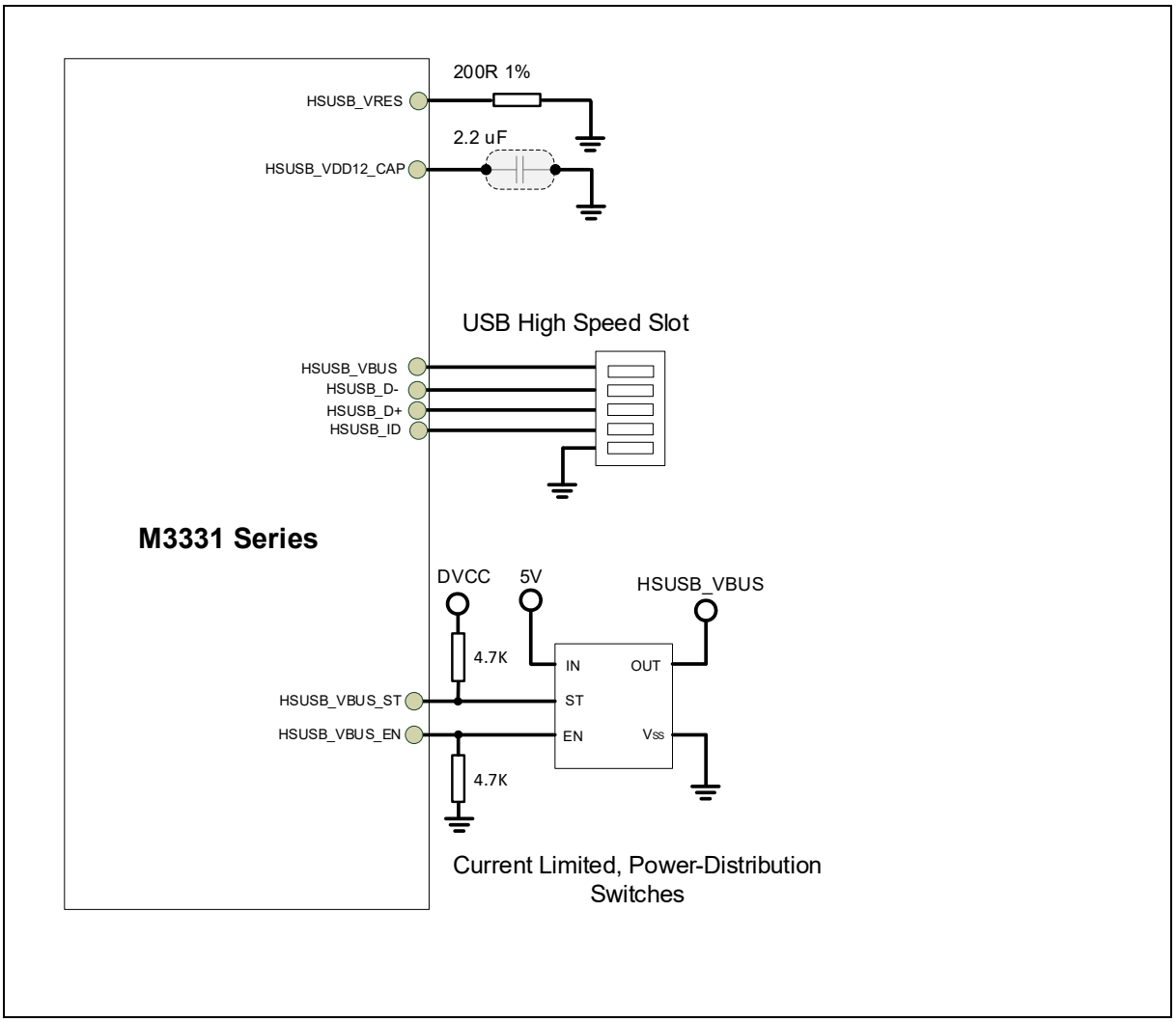


Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

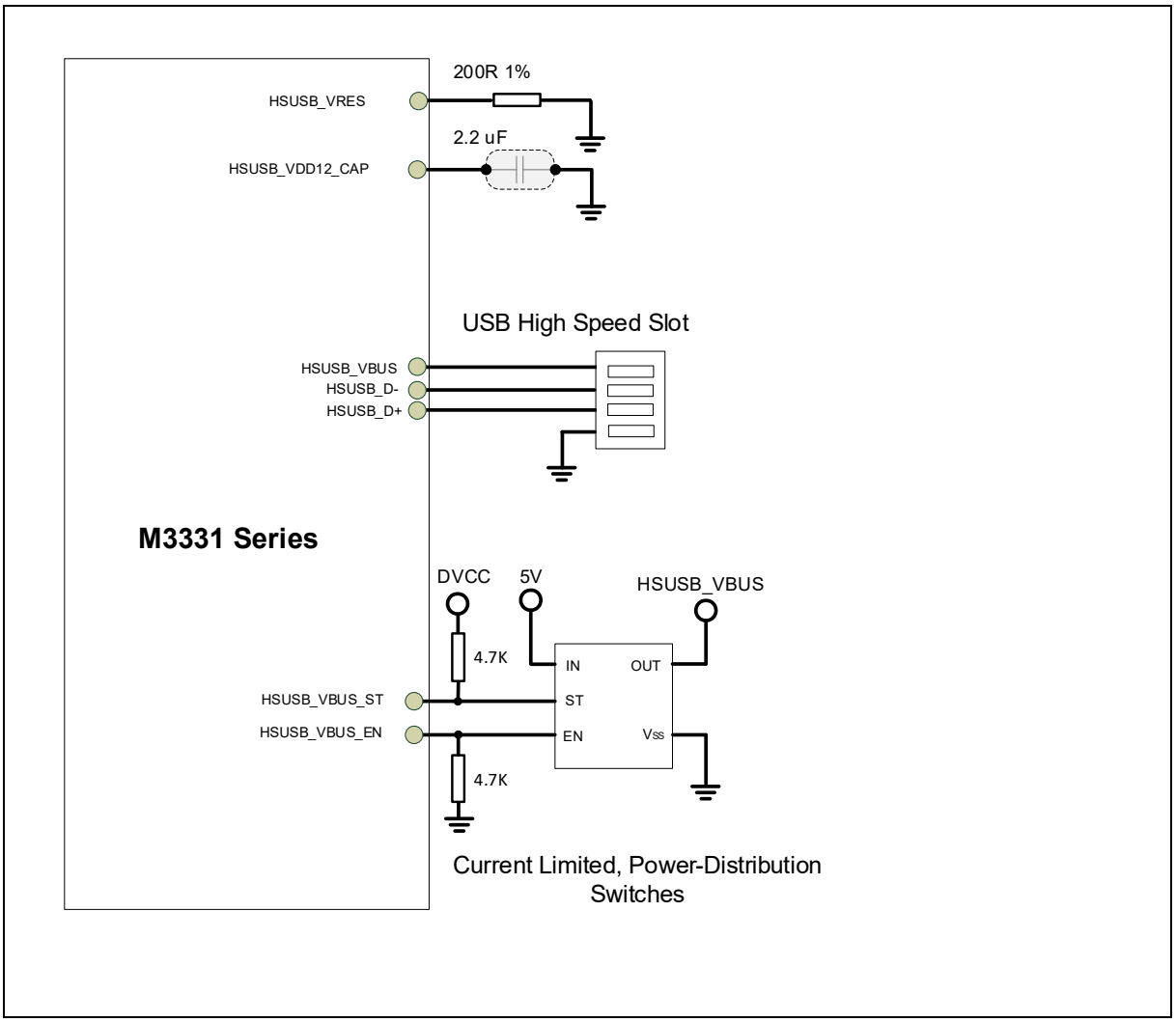
Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 μF capacitor on nRESET pin.

Note 3: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

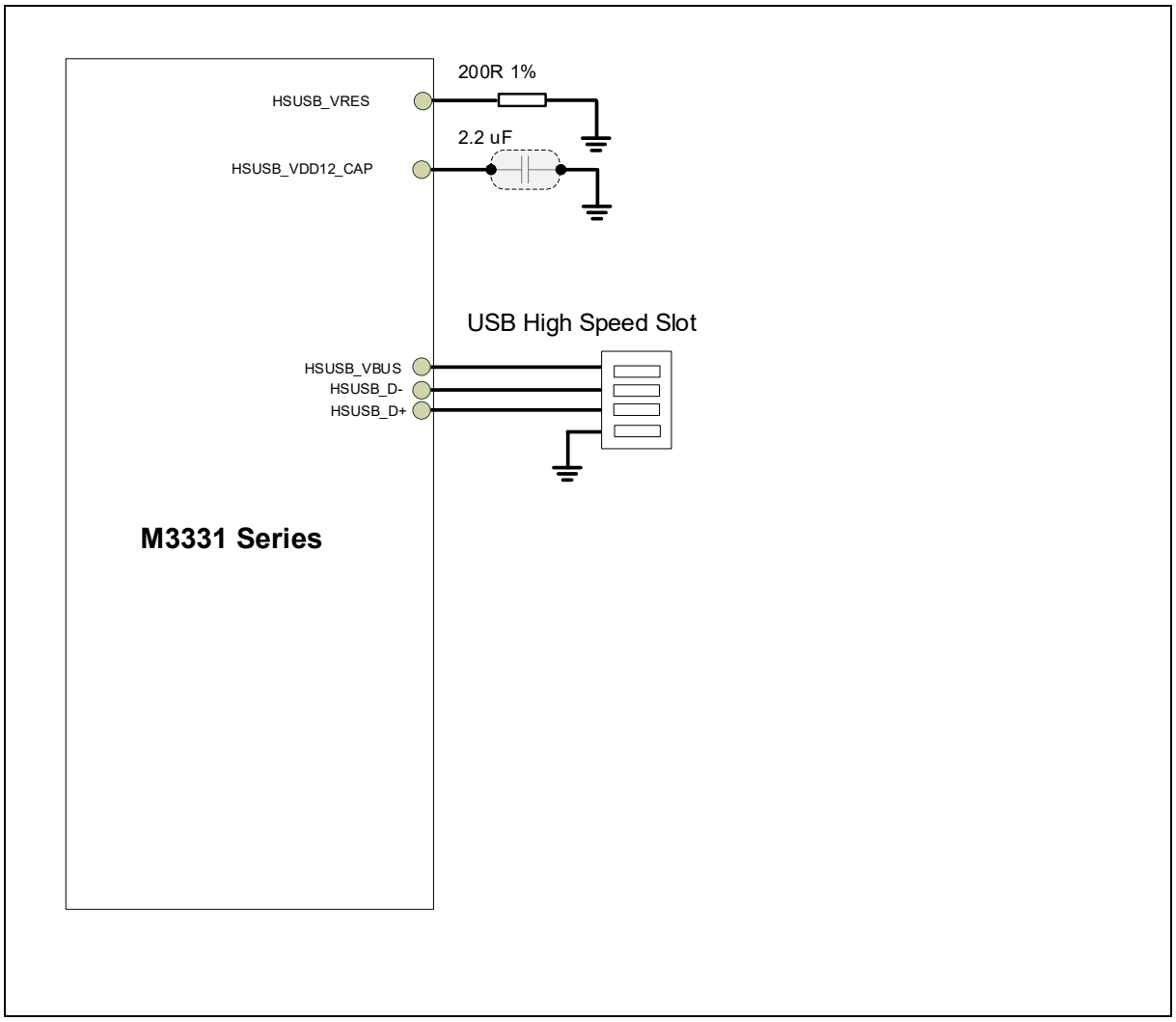
7.3 High speed USB OTG mode Application Scheme



7.4 High speed USB HOST mode Application Scheme



7.5 High speed USB HOST mode Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[1]	DC power supply	-0.3	4.0	V
V_{BUS}-V_{SS}[1]	V_{BUS} Power Supply	0	5.25	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV

Notes:

1. All main power (V_{DD}, AV_{DD}, V_{REF}, V_{BUS}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[2]	-	100	
	Maximum current sourced by total I/O Pins[2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- θ_{JC} = thermal resistance junction-case (°C /Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1]	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)	-	50	-	°C/Watt
	Thermal resistance junction-ambient 48-pin QFN(5x5 mm)	-	37.8	-	°C/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	°C/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	°C/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	38.5	-	°C/Watt
θ_{JC}[1]	Thermal resistance junction-case 33-pin QFN(4x4 mm)	-	7	-	°C/Watt
	Thermal resistance junction-case 48-pin QFN(5x5 mm)	-	5	-	°C/Watt
	Thermal resistance junction-case 48-pin LQFP(7x7 mm)	-	19.6	-	°C/Watt
	Thermal resistance junction-case 64-pin LQFP(7x7 mm)	-	17	-	°C/Watt
	Thermal resistance junction-case 128-pin LQFP(14x14 mm)	-	10	-	°C/Watt

Note:
1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	-4K	-	4K	V
V_{CDM}[2]	Electrostatic discharge,charge device model	-450	-	450	
V_{MM}	Electrostatic discharge,machine model	-200	-	200	
LU[3]	Pin current for latch-up[3] Class I for room temperature Class II for max. T_A temperature	-250(class I) -100(class II)	-	250(class I) 100(class II)	mA
V_{EFT}[4]	Fast transient voltage burst	-4.4	-	4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.

Table 8.1-4 EMC characteristics

8.2 General Operating Conditions

(V_{DD} - V_{SS} = 1.7 ~ 3.6 V, T_A = 25°C, HCLK = 180 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	180	MHz	
V_{DD}	Operation voltage	1.7	-	3.6	V	
AV_{DD}[1]	Analog operation voltage	V_{DD}				Except ADC and ACMP[4]
V_{REF}	Analog reference voltage	1.7	-	AV_{DD}		Except ADC[4]
V_{LDO}	LDO output voltage	-	1.15	-		
V_{BG}	Band-gap voltage	1.15	1.2	1.3	V	
T_{VBG_ADC}[3]	ADC sampling time when reading the band-gap voltage	-	8	10	µs	
C_{LDO}[2]	LDO regulator output capacitor	2.2			µF	
I_{RUSH}[3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	200	350	mA	
E_{RUSH}[3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.42	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 40 mA for 60 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, CLDO must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General operating conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.7 ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}/2$
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT, LIRC or LXT clock. clock	180 MHz	16.32	TBD	TBD	TBD	mA
	Normal run mode with PL1 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT, LIRC or LXT clock.	160 MHz	14.06	TBD	TBD	TBD	
		144 MHz	12.80	TBD	TBD	TBD	
		120 MHz	10.88	TBD	TBD	TBD	
		96 MHz	9.34	TBD	TBD	TBD	
		84 MHz	8.31	TBD	TBD	TBD	
		72 MHz	7.28	TBD	TBD	TBD	
		60 MHz	6.25	TBD	TBD	TBD	
		50 MHz	5.39	TBD	TBD	TBD	
		48 MHz	4.51	TBD	TBD	TBD	
		32 MHz	5.94	TBD	TBD	TBD	
		24 MHz	2.69	TBD	TBD	TBD	
		12 MHz	1.78	TBD	TBD	TBD	
		6 MHz	1.32	TBD	TBD	TBD	
		3 MHz	1.10	TBD	TBD	TBD	
		32.768 kHz	0.42	TBD	TBD	TBD	
		38 kHz	0.42	TBD	TBD	TBD	

	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock. clock	180 MHz	37.02	TBD	TBD	TBD	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock.	160 MHz	31.73	TBD	TBD	TBD	
		144 MHz	28.72	TBD	TBD	TBD	
		120 MHz	24.18	TBD	TBD	TBD	
		96 MHz	20.01	TBD	TBD	TBD	
		84 MHz	17.67	TBD	TBD	TBD	
		72 MHz	17.48	TBD	TBD	TBD	
		60 MHz	14.78	TBD	TBD	TBD	
		50 MHz	12.52	TBD	TBD	TBD	
		48 MHz	11.54	TBD	TBD	TBD	
		32 MHz	11.14	TBD	TBD	TBD	
		24 MHz	6.47	TBD	TBD	TBD	
		12 MHz	3.93	TBD	TBD	TBD	
		6 MHz	2.66	TBD	TBD	TBD	
		3 MHz	2.03	TBD	TBD	TBD	
		32.768 kHz	0.43	TBD	TBD	TBD	
		38 kHz	0.43	TBD	TBD	TBD	

Notes:

5. When analog peripheral blocks such as USB, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
6. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_IDLE}	Idle mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT, LIRC or LXT clock. clock	180 MHz	5.19	TBD	TBD	TBD	mA
	Idle mode with PL1 (PLSEL = 00), executed from Flash, all peripherals disable HIRC, PLL, HXT, LIRC or	160 MHz	4.54	TBD	TBD	TBD	
		144 MHz	4.20	TBD	TBD	TBD	
		120 MHz	3.68	TBD	TBD	TBD	
		96 MHz	3.56	TBD	TBD	TBD	

	LXT clock.	84 MHz	3.25	TBD	TBD	TBD	
		72 MHz	2.93	TBD	TBD	TBD	
		60 MHz	2.63	TBD	TBD	TBD	
		50 MHz	2.37	TBD	TBD	TBD	
		48 MHz	1.60	TBD	TBD	TBD	
		32 MHz	4.00	TBD	TBD	TBD	
		24 MHz	1.24	TBD	TBD	TBD	
		12 MHz	1.05	TBD	TBD	TBD	
		6 MHz	0.96	TBD	TBD	TBD	
		3 MHz	0.91	TBD	TBD	TBD	
		32.768 kHz	0.42	TBD	TBD	TBD	
		38 kHz	0.42	TBD	TBD	TBD	
	Idle mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock. clock	180 MHz	25.52	TBD	TBD	TBD	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT, LIRC or LXT clock.	160 MHz	21.88	TBD	TBD	TBD	
		144 MHz	19.82	TBD	TBD	TBD	
		120 MHz	16.73	TBD	TBD	TBD	
		96 MHz	14.02	TBD	TBD	TBD	
		84 MHz	12.42	TBD	TBD	TBD	
		72 MHz	12.97	TBD	TBD	TBD	
		60 MHz	11.01	TBD	TBD	TBD	
		50 MHz	9.37	TBD	TBD	TBD	
		48 MHz	8.51	TBD	TBD	TBD	
		32 MHz	9.12	TBD	TBD	TBD	
		24 MHz	4.94	TBD	TBD	TBD	
		12 MHz	3.16	TBD	TBD	TBD	
		6 MHz	2.26	TBD	TBD	TBD	
		3 MHz	1.82	TBD	TBD	TBD	
		32.768 kHz	0.42	TBD	TBD	TBD	
		38 kHz	0.42	TBD	TBD	TBD	

Notes:

1. When analog peripheral blocks such as USB, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	Power Level	LXT[1] 32.768 kHz	LIRC 38.4 kHz	Typ[2]			Max[3][4]				Unit
					T_A= 25 °C			T_A = 25 °C	T_A = 55 °C	T_A = 85 °C	T_A = 105 °C	
					1.7 V	3.3 V	3.6 V	3.6 V	3.6 V	3.6 V	3.6 V	
I_{DD_DPD}	DPD mode, all peripherals disable	-	-	-	0.52	0.62	0.75	TBD	TBD	TBD	TBD	µA
	DPD mode, all peripherals disable (DPDHOLDEN=1)	-	-	-	0.54	0.87	1.15	TBD	TBD	TBD	TBD	
I_{DD_SPD}	SPD mode, all peripherals disable without SRAM retention	-	-	-	4.35	4.93	5.34	TBD	TBD	TBD	TBD	µA
	SPD mode, all peripherals disable with 64KB SRAM retention	-	-	-	5.28	5.85	6.26	TBD	TBD	TBD	TBD	
	SPD mode, all peripherals disable with 192KB SRAM retention	-	-	-	6.91	7.48	7.89	TBD	TBD	TBD	TBD	
	SPD mode, all peripherals disable with 320KB SRAM retention	-	-	-	8.54	9.11	9.53	TBD	TBD	TBD	TBD	
	SPD mode without SRAM retention, RTC enable and run	-	V	-	4.79	5.40	5.82	TBD	TBD	TBD	TBD	
	SPD mode without SRAM retention, wake-up timer enable and run	-	-	V	4.57	5.21	5.63	TBD	TBD	TBD	TBD	
I_{DD_NPD2}	NPD2 mode, all peripherals disable	-	-	-	188.88	189.89	191.50	TBD	TBD	TBD	TBD	µA
	NPD2 mode, WDT/Timer/UART/RTC enable and run	-	V	-	190.07	191.12	192.73	TBD	TBD	TBD	TBD	
	NPD2 mode, RTC/WDT/Timer enable and run	-	-	V	189.57	190.66	192.28	TBD	TBD	TBD	TBD	
	NPD2 mode, WDT/Timer use LIRC, RTC /UART use LXT	-	V	V	190.43	191.53	193.18	TBD	TBD	TBD	TBD	
I_{DD_NPD1}	NPD1 mode, all	PL0	-	-	391.62	392.81	394.42	TBD	TBD	TBD	TBD	µA

	peripherals disable	PL1	-	-	339.40	340.86	342.55	TBD	TBD	TBD	TBD	
	NPD1 mode, all peripherals disable (LVR disable)	PL0	-	-	391.38	392.50	394.11	TBD	TBD	TBD	TBD	
		PL1	-	-	339.15	340.65	342.31	TBD	TBD	TBD	TBD	
	NPD1 mode, RTC enable and run	PL0	V	-	392.00	393.18	394.82	TBD	TBD	TBD	TBD	
		PL1	V	-	339.85	341.37	343.03	TBD	TBD	TBD	TBD	
	NPD1 mode, WDT/Timer/UART/RTC enable and run	PL0	V	-	393.21	394.42	395.97	TBD	TBD	TBD	TBD	
		PL1	V	-	340.98	342.51	344.14	TBD	TBD	TBD	TBD	
	NPD1 mode, RTC/WDT/Timer enable and run	PL0	-	V	392.49	393.65	395.25	TBD	TBD	TBD	TBD	
		PL1	-	V	340.32	341.90	343.55	TBD	TBD	TBD	TBD	
	NPD1 mode, WDT/Timer/UART/RTC enable and run, WDT/Timer use LIRC, UART/RTC use LXT	PL0	V	V	393.55	394.85	396.47	TBD	TBD	TBD	TBD	
		PL1	V	V	341.47	343.04	344.68	TBD	TBD	TBD	TBD	
I_{DD_NPD0}	NPD0 mode, all peripherals disable	PL0	-	-	456.46	451.09	452.87	TBD	TBD	TBD	TBD	μA
		PL1	-	-	404.22	397.96	399.68	TBD	TBD	TBD	TBD	
	NPD0 mode, WDT/Timer/UART/RTC enable and run	PL0	V	-	458.80	452.21	454.05	TBD	TBD	TBD	TBD	
		PL1	V	-	404.93	398.92	400.68	TBD	TBD	TBD	TBD	
	NPD0 mode, RTC/WDT/Timer enable and run	PL0	-	V	457.98	451.61	453.47	TBD	TBD	TBD	TBD	
		PL1	-	V	404.09	398.45	400.24	TBD	TBD	TBD	TBD	
	NPD0 mode, WDT/Timer/UART/RTC enable and run, WDT/Timer use LIRC, UART/RTC use LXT	PL0	V	V	459.44	452.89	454.75	TBD	TBD	TBD	TBD	
		PL1	V	V	404.84	399.67	401.44	TBD	TBD	TBD	TBD	

Table 8.3-3 Chip Current Consumption in Power-down mode

Symbol	Test Conditions	Typ[1]				Max[2]				Unit
		25°C	55°C	85°C	105°C	25°C	55°C	85°C	105°C	
I_{DD_SRAM}	SRAM 64 KB static consumption	0.92	3.23	11.52	25.30	TBD	TBD	TBD	TBD	μA
	SRAM 192 KB static consumption	2.55	8.82	31.13	68.30	TBD	TBD	TBD	TBD	
	SRAM 320 KB static consumption	4.18	14.44	50.84	111.30	TBD	TBD	TBD	TBD	

Notes:

1. Tested in SPD mode.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-4 SRAM Static Current Consumption in Power-down mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = PLL180 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2 (PCLK keeps default value).
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[1]	Unit
PDMA0	380	μA
ISP	1	
EBI	74	
ST	181	
SDH0	811	
CRC	65	
CANFD0	687	
CANFD1	702	
HSUSBD[4]	603	
FMCIDLE	86	
USBH[4]	866	
CANRAM0	41	
CANRAM1	39	
TRACE	0	
GPA	20	
GPB	17	
GPC	24	
GPD	19	
GPE	23	
GPF	21	
GPG	20	
GPH	22	
WDT0	157	
RTC	34	
TMR0	243	
TMR1	241	
TMR2	224	

TMR3	217	
CLKO	317	
ACMP01[3]	148	
I2C0	61	
I2C1	37	
I2C2	60	
I3C0	838	
QSPI0	384	
SPI0	371	
SPI1	396	
SPI2	370	
UART0	462	
UART1	416	
UART2	414	
UART3	422	
UART4	413	
WWDT0	155	
WWDT1	155	
EADC0[2]	533	
I2S0	351	
HSOTG[4]	311	
WDT1	157	
USCI0	68	
USCI1	45	
EPWM0	159	
EPWM1	129	
BPWM0	106	
BPWM1	87	
EQEI0	56	
ECAP0	59	
BPWM2	134	
BPWM3	340	
BPWM4	178	
BPWM5	213	
LLSI0	64	

LLSI1	41	
LLSI2	65	
LLSI3	41	
LLSI4	62	
LLSI5	40	
LLSI6	64	
LLSI7	41	
LLSI8	63	
LLSI9	41	
ELLSI0	117	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.

Table 8.3-5 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode	12	TBD	cycles
t_{WU_DPD}[1][2]	Wakeup from DPD mode	2400	TBD	μs
t_{WU_SPD}[1][2]	Wakeup from SPD mode	207	TBD	
t_{WU_NPD2}[1][2]	Wakeup from NPD2 mode running in flash	57	TBD	
t_{WU_NPD1}[1][2]	Wakeup from NPD1 mode running in flash	12	TBD	
t_{WU_NPD0}[1][2]	Wakeup from NPD0 mode running in flash	9	TBD	
t_{ET_IDLE}[1]	Enter to IDLE mode	5	TBD	cycles
t_{ET_DPD}[1]	Enter to DPD mode	12	TBD	μs
t_{ET_SPD}[1]	Enter to SPD mode	6	TBD	
t_{ET_NPD2}[1]	Enter to NPD2 mode	0.6	TBD	
t_{ET_NPD1}[1]	Enter to NPD1 mode	0.6	TBD	
t_{ET_NPD0}[1]	Enter to NPD0 mode	0.3	TBD	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-6 Low-power mode wakeup timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	-		Injected current on any 5V tolerance I/O except analog input pin
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-7 I/O current injection characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	V_{DD} = 1.7 ~ 3.6V
	Input low voltage (TTL trigger)	0	-	0.7		V_{DD} = 2.7 V
		0	-	0.4		V_{DD} = 1.7 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	V_{DD} = 1.7 ~ 3.6V
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 3.6 V
		1.2	-	V_{DD}		V_{DD} = 1.8 V
V_{HY}[1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	V_{DD} = 1.7 ~ 3.6V
I_{LK}[2]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 3.6 V, Open-drain or input only mode on any other 5V tolerance pins
R_{PU}[1]	Pull up resistor	40	51	61	kΩ	V_{DD} = 1.7 ~ 3.6V
R_{PD}[1]	Pull down resistor	40	51	61	kΩ	V_{DD} = 1.7 ~ 3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-8 I/O input characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2] [3]	Source current for quasi-bidirectional mode and high level	-6.0		-10.0	μA	V_{DD} = 3.6 V V_{IN} = (V_{DD} - 0.4) V
		-6.0		-8.5	μA	V_{DD} = 2.7 V V_{IN} = (V_{DD} - 0.4) V
		-6.0		-8.5	μA	V_{DD} = 1.8 V V_{IN} = (V_{DD} - 0.4) V
		-6.0		-8.5	μA	V_{DD} = 1.7 V V_{IN} = (V_{DD} - 0.4) V
	Source current for push-pull mode and high level	-11.0		-21.0	mA	V_{DD} = 3.6 V V_{IN} = (V_{DD} - 0.4) V
		-8.0		-20.5	mA	V_{DD} = 2.7 V V_{IN} = (V_{DD} - 0.4) V
		-7.0		-14.0	mA	V_{DD} = 1.8 V V_{IN} = (V_{DD} - 0.4) V
		-7.0		-12.5	mA	V_{DD} = 1.7 V V_{IN} = (V_{DD} - 0.4) V
I_{SK}[1] [2] [4]	Sink current for push-pull mode and low level	11.0		24.0	mA	V_{DD} = 3.6 V V_{IN} = 0.4 V
		8.5		22.5	mA	V_{DD} = 2.7 V V_{IN} = 0.4 V
		6.0		16.0	mA	V_{DD} = 1.8 V V_{IN} = 0.4 V
		6.0		14.5	mA	V_{DD} = 1.7 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance		5		pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.
3. The range of output high level voltage (V_{OH}) is from V_{DD}-0.4 to V_{DD} based on minimum value of source current (I_{SR}).
4. The range of output low level voltage (V_{OL}) is from 0 to 0.4 based on minimum value of sink current (I_{SK}).

Table 8.3-9 I/O output characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	

V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	40	50	60	kΩ	V_{DD} = 1.7~3.6V
t_{RP}[1]	Minimum nRESET pulse width	34	-	-	μs	Normal run and Idle mode
		38	-	-		FWPD mode
		40	-	-		NPD mode
		40	-	-		LLNPD mode
		0.5	-	-		SPD mode
		0.5	-	-		DPD mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10 μF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-10 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

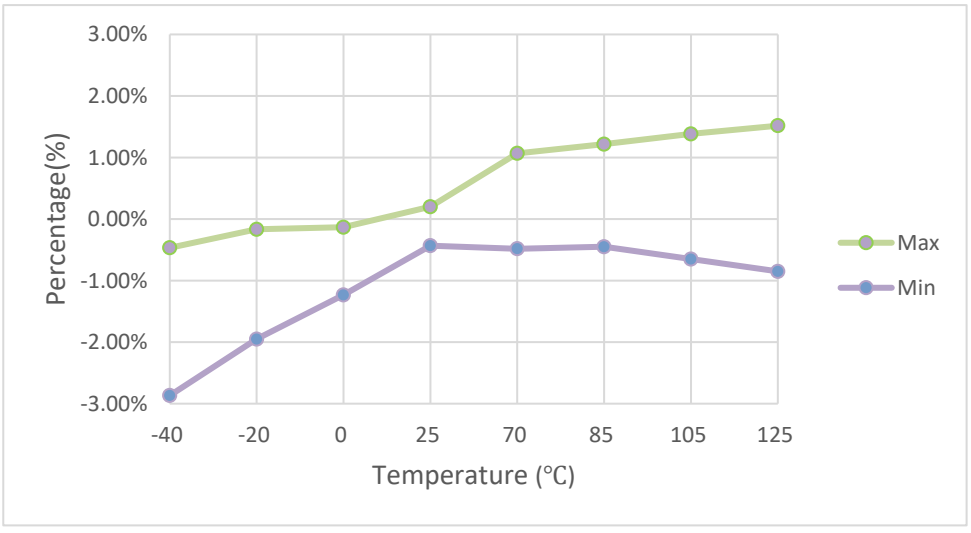
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operating voltage	1.7	-	3.6	V	
f_{HIRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[1]	-	2[1]	%	T_A = 25 ~ +105 °C, V_{DD} = 3.3V
		-3[1]	-	3[1]	%	T_A = -40 ~ +105 °C, V_{DD} = 1.7 ~ 3.6V
I_{HIRC}[1]	Operating current	-	200	-	μA	
T_S[2]	Stable time	-	5	-	μs	T_A = -40°C ~ +105 °C, V_{DD} = 1.7 ~ 3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-1.

Figure 8.4-1 HIRC vs. Temperature

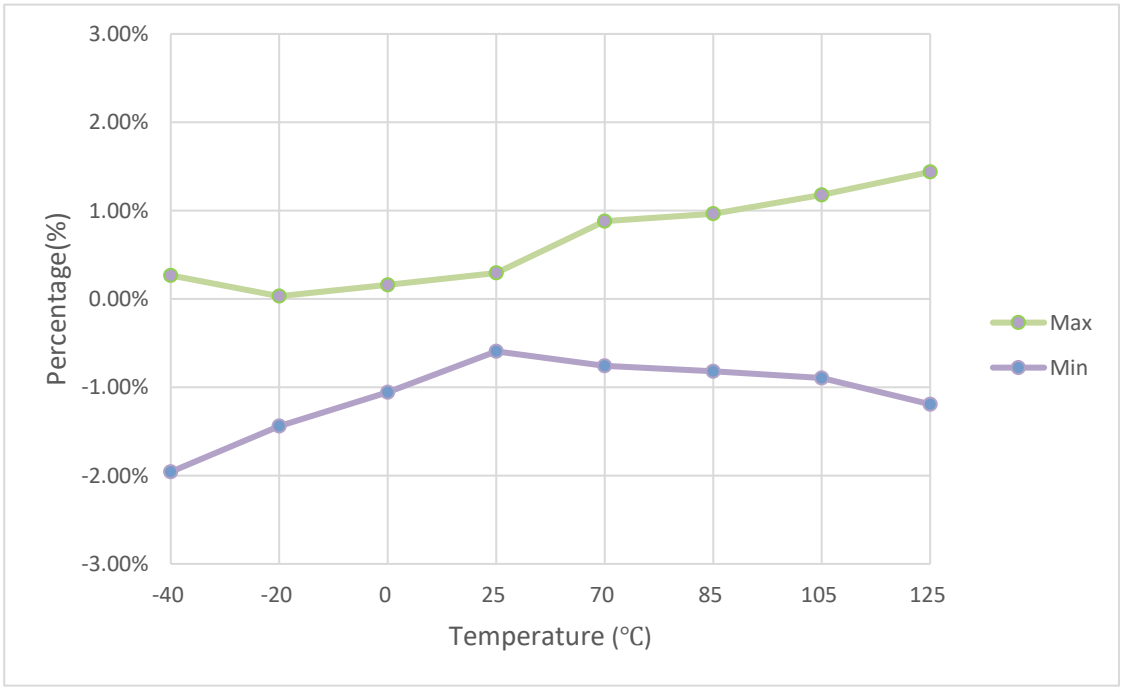
8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operating voltage	1.7	-	3.6	V	
F_{LIRC}	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3 V
		-1.5[1]	-	1.5[1]	%	T_A = 25 ~ 105 °C V_{DD} = 1.7 ~ 3.6 V
		-2.5[1]	-	2.5[1]	%	T_A = -40 ~ 105 °C V_{DD} = 1.7 ~ 3.6 V
I_{LIRC}	Operating current	-	0.23	-	μA	V_{DD} = 3.3 V
T_S [2]	Stable time	-	500	-	μs	T_A = -40 ~ 105 °C V_{DD} = 1.7 ~ 3.6 V

Notes:

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-2 32 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-2.

Figure 8.4-2 LIRC vs. Temperature

8.4.3 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
R_f	Internal feedback resister	-	0.2	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT_INV}	Current consumption	-	400	-	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	2600	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	3200	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	5000	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	6000	-		32 MHz, Gain = L4, C_L = 12.5 pF
I_{HXT_GM}	Current consumption	-	350	-	μA	4 MHz, Gain = L0, C_L = 12.5 pF
		-	700	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	950	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	2300	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	2500	-		32 MHz, Gain = L4, C_L = 12.5 pF
T_{S_INV}	Stable time	-	3200	-	μs	4 MHz, Gain = L0, C_L = 12.5 pF
		-	3000	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2600	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	1500	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	650	-		32 MHz, Gain = L4, C_L = 12.5 pF
T_{S_GM}	Stable time	-	3700	-	μs	4 MHz, Gain = L0, C_L = 12.5 pF
		-	2400	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	2100	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	1100	-		24 MHz, Gain = L3, C_L = 12.5 pF
		-	650	-		32 MHz, Gain = L4, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1.6	-	V	4 MHz, Gain = L0, C_L = 12.5 pF
		-	1.4	-		12 MHz, Gain = L1, C_L = 12.5 pF
		-	1.6	-		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	1.7	-		24 MHz, Gain = L3, C_L = 12.5 pF

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
		-	1.9	-		32 MHz, Gain = L4, C_L = 12.5 pF

Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	150	Ω	4 MHz, Gain = L0, C_L = 12.5 pF
		-	-	120		12 MHz, Gain = L1, C_L = 12.5 pF
		-	-	100		16 Mhz, Gain = L2, C_L = 12.5 pF
		-	-	80		24 MHz, Gain = L3, C_L = 12.5 pF
		-	-	50		32 MHz, Gain = L4, C_L = 12.5 pF

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

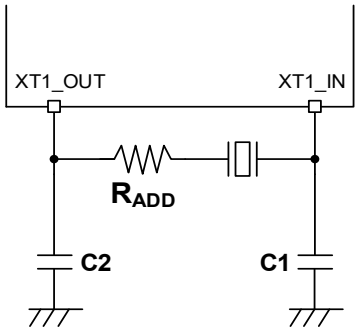


Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics

8.4.3.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 20 pF	10 ~ 20 pF	without

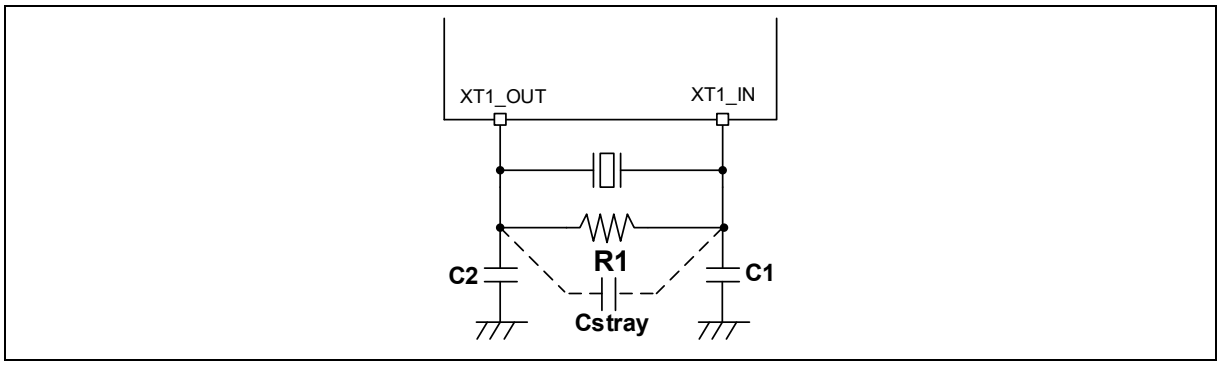
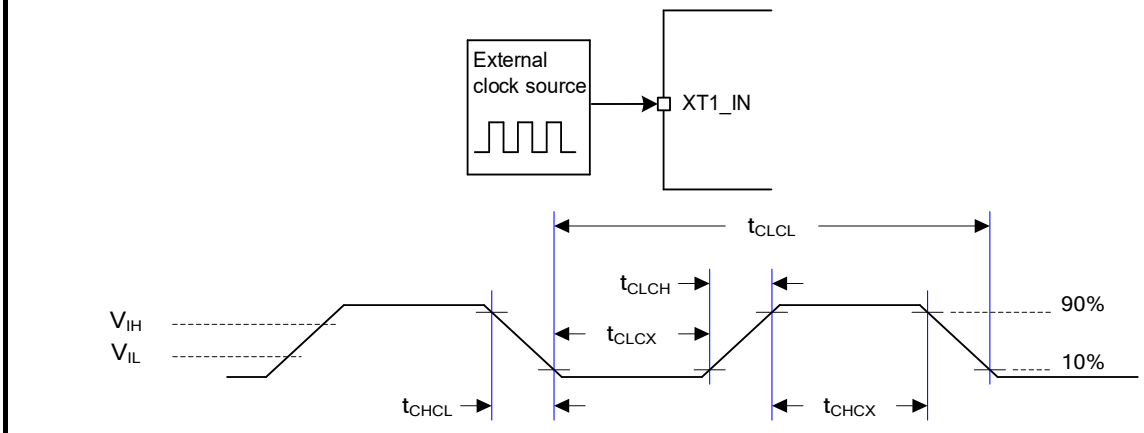


Figure 8.4-3 Typical Crystal Application Circuit

8.4.4 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The XT1_IN is set as schmitt trigger input mode.
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The XT1_IN is set as schmitt trigger input mode.



Notes:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~32 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{DD}	Operation voltage	1.7	3	3.6	V	
R_f	Internal feedback resistor	-	12	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	400	-	nA	ESR = 50 kΩ, C_L = 6 pF, Gain = L0
		-	700	-		ESR = 50 kΩ, C_L = 12.5 pF, Gain = L1
		-	850	-		ESR = 70 kΩ, C_L = 12.5 pF, Gain = L2
		-	1100	-		ESR = 90 kΩ, C_L = 12.5 pF, Gain = L3
Ts_{LXT}	Stable time	-	1	-	s	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.3	-	-	V	

Notes:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (Sf) must be higher than 5 for LXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the LXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

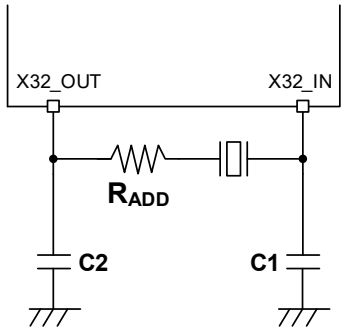


Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	50	90	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.2 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 5 pF ~ 20 pF range, designed for RTC applications, and selected to match the requirements of the crystal. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 90 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

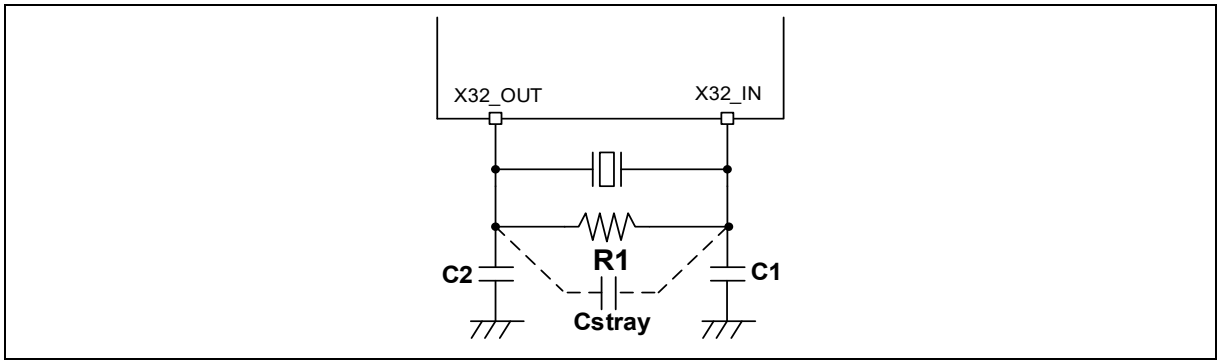
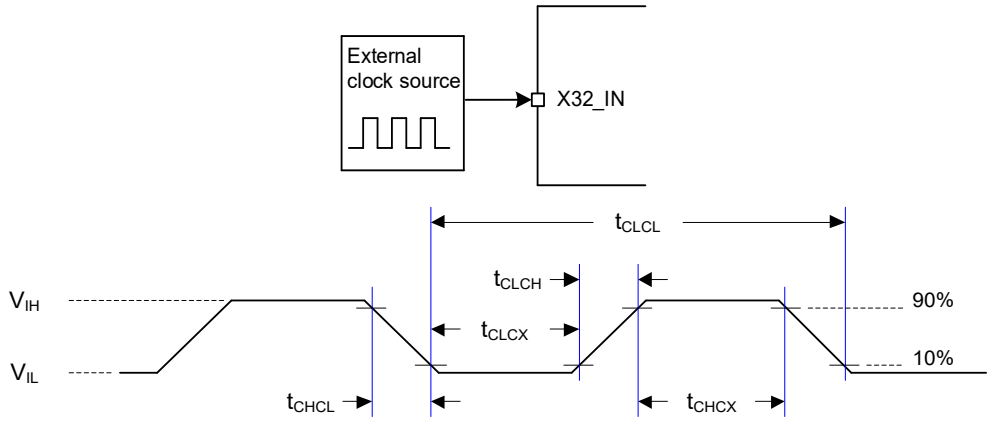


Figure 8.4-4 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
V_{IH}	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	V_{DD} The X32_IN is set as schmitt trigger input mode.
V_{IL}	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	V_{DD} The X32_IN is set as schmitt trigger input mode.



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{PLL_in}	PLL input clock	1	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	25	-	180	MHz	
f_{PLL_REF}	PLL reference clock	1	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	100	-	360	MHz	
T_L	PLL locking time	-	100	300	μs	
Jitter[2]	Cycle-to-cycle Jitter	-	400	600	ps	
I_{DD}	Power consumption	-	2	2.6	mA	f_{PLL_VCO} = 360 MHz

Notes:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-9 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	8.52	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	5.74		C_L = 10 pF, V_{DD} = 3.6 V
		-	10.16		C_L = 30 pF, V_{DD} >= 2.7 V
		-	6.93		C_L = 10 pF, V_{DD} >= 2.7 V
		-	14.78		C_L = 30 pF, V_{DD} >= 1.7 V
		-	10.22		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	5.14		C_L = 30 pF, V_{DD} = 3.6 V
		-	3.23		C_L = 10 pF, V_{DD} = 3.6 V
		-	6.12		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3.82		C_L = 10 pF, V_{DD} >= 2.7 V
		-	9.27		C_L = 30 pF, V_{DD} >= 1.7 V
		-	5.63		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (Fast Slew Rate)	-	3.42	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	1.67		C_L = 10 pF, V_{DD} = 3.6 V
		-	4.17		C_L = 30 pF, V_{DD} >= 2.7 V
		-	2.04		C_L = 10 pF, V_{DD} >= 2.7 V
		-	6.91		C_L = 30 pF, V_{DD} >= 1.7 V
		-	3.38		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (Ultra-Fast Slew Rate)	-	2.75	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	1.35		C_L = 10 pF, V_{DD} = 3.6 V
		-	3.36		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.65		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5.57		C_L = 30 pF, V_{DD} >= 1.7 V
		-	2.74		C_L = 10 pF, V_{DD} >= 1.7 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	7.99	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	5.53		C_L = 10 pF, V_{DD} = 3.6 V
		-	9.66		C_L = 30 pF, V_{DD} >= 2.7 V
		-	6.74		C_L = 10 pF, V_{DD} >= 2.7 V

		-	14.08		C_L = 30 pF, V_{DD} >= 1.7 V
		-	9.83		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	4.93	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	3.15		C_L = 10 pF, V_{DD} = 3.6 V
		-	5.98		C_L = 30 pF, V_{DD} >= 2.7 V
		-	3.80		C_L = 10 pF, V_{DD} >= 2.7 V
		-	9.29		C_L = 30 pF, V_{DD} >= 1.7 V
		-	5.69		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (Fast Slew Rate)	-	3.03	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	1.57		C_L = 10 pF, V_{DD} = 3.6 V
		-	3.88		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.99		C_L = 10 pF, V_{DD} >= 2.7 V
		-	6.86		C_L = 30 pF, V_{DD} >= 1.7 V
		-	3.47		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (Ultra-Fast Slew Rate)	-	2.48	ns	C_L = 30 pF, V_{DD} = 3.6 V
		-	1.31		C_L = 10 pF, V_{DD} = 3.6 V
		-	3.17		C_L = 30 pF, V_{DD} >= 2.7 V
		-	1.67		C_L = 10 pF, V_{DD} >= 2.7 V
		-	5.58		C_L = 30 pF, V_{DD} >= 1.7 V
		-	2.88		C_L = 10 pF, V_{DD} >= 1.7 V
$f_{max(IO)out}$[*3]	I/O maximum frequency[5] (Normal Slew Rate)	-	30.28	MHz	C_L = 30 pF, V_{DD} = 3.6 V
		-	44.37		C_L = 10 pF, V_{DD} = 3.6 V
		-	25.23		C_L = 30 pF, V_{DD} >= 2.7 V
		-	36.58		C_L = 10 pF, V_{DD} >= 2.7 V
		-	17.33		C_L = 30 pF, V_{DD} >= 1.7 V
		-	24.94		C_L = 10 pF, V_{DD} >= 1.7 V
	I/O maximum frequency[5] (High Slew Rate)	-	49.65	MHz	C_L = 30 pF, V_{DD} = 3.6 V
		-	78.37		C_L = 10 pF, V_{DD} = 3.6 V
		-	41.32		C_L = 30 pF, V_{DD} >= 2.7 V
		-	65.62		C_L = 10 pF, V_{DD} >= 2.7 V

		-	26.94		C_L = 30 pF, V_{DD} >= 1.7 V
		-	44.17		C_L = 10 pF, V_{DD} >= 1.7 V
	I/O maximum frequency[4] (Fast Slew Rate)	-	77.52	MHz	C_L = 30 pF, V_{DD} = 3.6 V
		-	154.32		C_L = 10 pF, V_{DD} = 3.6 V
		-	62.11		C_L = 30 pF, V_{DD} >= 2.7 V
		-	124.07		C_L = 10 pF, V_{DD} >= 2.7 V
		-	36.31		C_L = 30 pF, V_{DD} >= 1.7 V
		-	72.99		C_L = 10 pF, V_{DD} >= 1.7 V
	I/O maximum frequency[4] (Ultra-Fast Slew Rate)	-	95.60	MHz	C_L = 30 pF, V_{DD} = 3.6 V
		-	180.00		C_L = 10 pF, V_{DD} = 3.6 V
		-	76.57		C_L = 30 pF, V_{DD} >= 2.7 V
		-	150.60		C_L = 10 pF, V_{DD} >= 2.7 V
		-	44.84		C_L = 30 pF, V_{DD} >= 1.7 V
		-	88.97		C_L = 10 pF, V_{DD} >= 1.7 V

Notes:

1. Guaranteed by design result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$
4. Maximum output frequency is achieved if ((T_R + T_F) ≤ 1/2) T and if the ducy cycle is (45%-55%) when loaded by the specified capacitance but the maximum system frequency is limited to CPU.

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	105	°C	
V_{DD}	Power supply	1.7	-	3.6	V	
V_{LDO}	Output voltage	-	1.15	-	V	MCU @ PL0
V_{LDO}	Output voltage	-	1.1	-	V	MCU @ PL1
V_{LDO}	Output voltage	-	0.9	-	V	MCU @ NPD2 or SPD1

Notes:

1. It is recommended a 0.1 μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a C_{LDO} capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.
3. V_{LDO} is only used to supply internal power.

Table 8.5-1 LDO characteristics

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
I_{POR}[1]	POR operating current	-	10	20	μA	V_{DD} = AV_{DD} = 3.6 V
I_{LVR}[1]	LVR operating current	-	0.45	0.65		V_{DD} = AV_{DD} = 3.6 V
I_{BOD}[1]	BOD operating current	-	10	15		V_{DD} = AV_{DD} = 3.6 V, Normal mode
		-	-	1.5		V_{DD} = AV_{DD} = 3.6 V, Low Power mode
V_{POR}	POR reset voltage (Rising edge)	1.45	1.50	1.55	V	
	POR reset voltage (Falling edge)	1.40	1.45	1.50		
V_{LVR}	LVR reset voltage (Rising edge)	1.525	1.625	1.725		
	LVR reset voltage (Falling edge)	1.45	1.55	1.65		
V_{BOD}	BOD brown-out detect voltage (Rising edge)	1.575	1.675	1.775		BODVL = 8
		1.775	1.875	1.975		BODVL = 9
		1.95	2.075	2.175		BODVL = 10
		2.175	2.275	2.375		BODVL = 11
		2.375	2.475	2.575		BODVL = 12
		2.575	2.675	2.775		BODVL = 13

		2.775	2.875	2.975		BODVL = 14
		2.975	3.075	3.175		BODVL = 15
	BOD brown-out detect voltage (Falling edge)	1.5	1.6	1.7		BODVL = 8
		1.7	1.8	1.9		BODVL = 9
		1.9	2	2.1		BODVL = 10
		2.1	2.2	2.2		BODVL = 11
		2.3	2.4	2.5		BODVL = 12
		2.5	2.6	2.7		BODVL = 13
		2.7	2.8	2.9		BODVL = 14
		2.9	3	3.1		BODVL = 15
T_{LVR_SU}[1]	LVR startup time	-	-	2250	μs	-
T_{LVR_RE}[1]	LVR respond time	-	15	30		LVRDGSEL = 0
T_{BOD_SU}[1]	BOD startup time	-	-	300		BOD Normal mode
		-	-	350		BOD Low Power mode
T_{BOD_RE}[1]	BOD respond time	-	5	10		Normal mode BODDGSEL = 3
		-	-	3500		Low Power mode BODDGSEL = 3
R_{VDDR}[1]	VDD rise time rate	10	-	-	μs/V	POR Enabled
R_{VDDF}[1]	VDD fall time rate	10	-	-		POR Enabled
		150	-	-		LVR Enabled
		50	-	-		BOD 1.55V Enabled, Normal mode
		40	-	-		BOD 1.6V Enabled, Normal mode
		22.22	-	-		BOD 1.8V Enabled, Normal mode
		15.38	-	-		BOD 2.0V Enabled, Normal mode
		11.76	-	-		BOD 2.2V Enabled, Normal mode
		9.52	-	-		BOD 2.4V Enabled, Normal mode
		8	-	-		BOD 2.6V Enabled, Normal mode
		6.89	-	-		BOD 2.8V Enabled, Normal mode
		6.06	-	-		BOD 3.0V Enabled, Normal mode
		17500	-	-		BOD 1.55V Enabled, Low Power mode

		14000	-	-		BOD 1.6V Enabled, Low Power mode
		7777.7	-	-		BOD 1.8V Enabled, Low Power mode
		5384.6	-	-		BOD 2.0V Enabled, Low Power mode
		4117.6	-	-		BOD 2.2V Enabled, Low Power mode
		3333.3	-	-		BOD 2.4V Enabled, Low Power mode
		2800	-	-		BOD 2.6V Enabled, Low Power mode
		2413.7	-	-		BOD 2.8V Enabled, Low Power mode
		2121.2	-	-		BOD 3.0V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-2 Reset and Power Control Unit

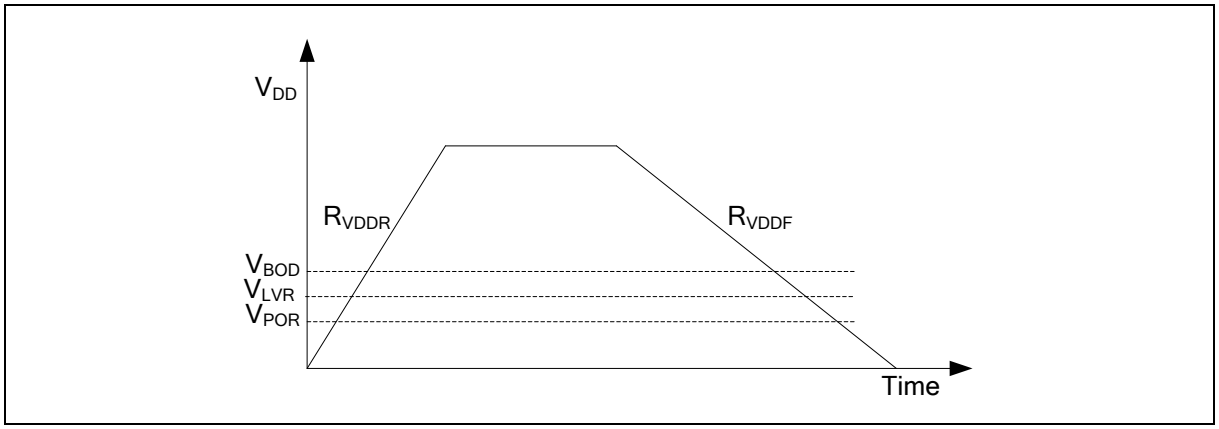


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	278		µA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 90 MHz F_{SPS} = 4285 * kSPS
		-	57		µA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 12. MHz F_{SPS} = 571 * kSPS
N_R	Resolution	12			Bit	
F_{ADC}[1] $1/T_{ADC}$	ADC Clock frequency	12	-	90	MHz	
T_{SMP}[1]	Sampling Time	0	-	255	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	21	-		$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 21 * T_{ADC}$
F_{SPS}[1]	Sampling Rate	571	-	4285	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}[1]	Enable to ready time	5	-	-	$1/F_{ADC}$	
INL[1]	Integral Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
DNL[1]	Differential Non-Linearity Error	-2	-	+2	LSB	$V_{REF} = AV_{DD}$,
E_G[1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
E_O[1]	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
E_A[1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$,
ENOB[1]	Effective number of bits	-	10	-	bits	F_{ADC} = 90. MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[1]	Signal-to-noise and distortion ratio	-	62	-	dB	
SNR[1]	Signal-to-noise ratio	-	63	-		
THD[1]	Total harmonic distortion	-	-64	-		
C_{IN}[2]	Internal Capacitance	-	3.6	-	pF	
R_{IN}[2]	Internal Switch Resistance	-	-	0.72	kΩ	
R_{EX}	External input impedance at room temperature [1] [3]	0.39	-	10	kΩ	F_{ADC} = 90 MHz $T_{CONV} = T_{SMP} + 21 * T_{ADC}$ $C_{EX} = C_{IO}$ = 5 pF T_J = 25 °C

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

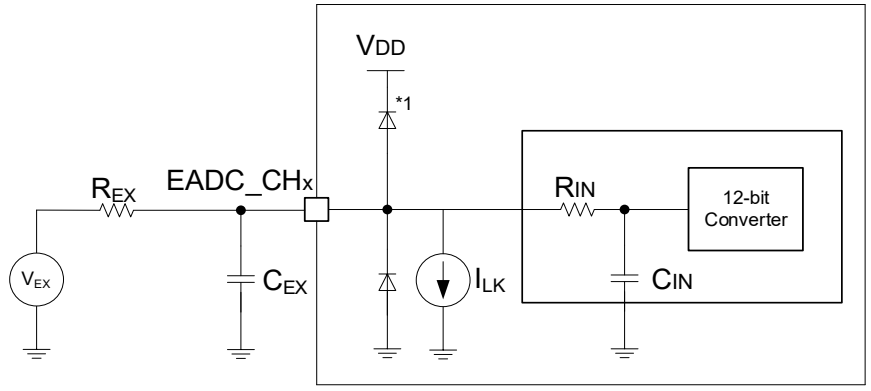
Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design, not tested in production.
3. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resolution) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

4. The signal voltage is affected by IO leakage and internal ADC leakage. When ADC is running at high temperature, the R_{EX} should be lower to decrease IR voltage drop effect.

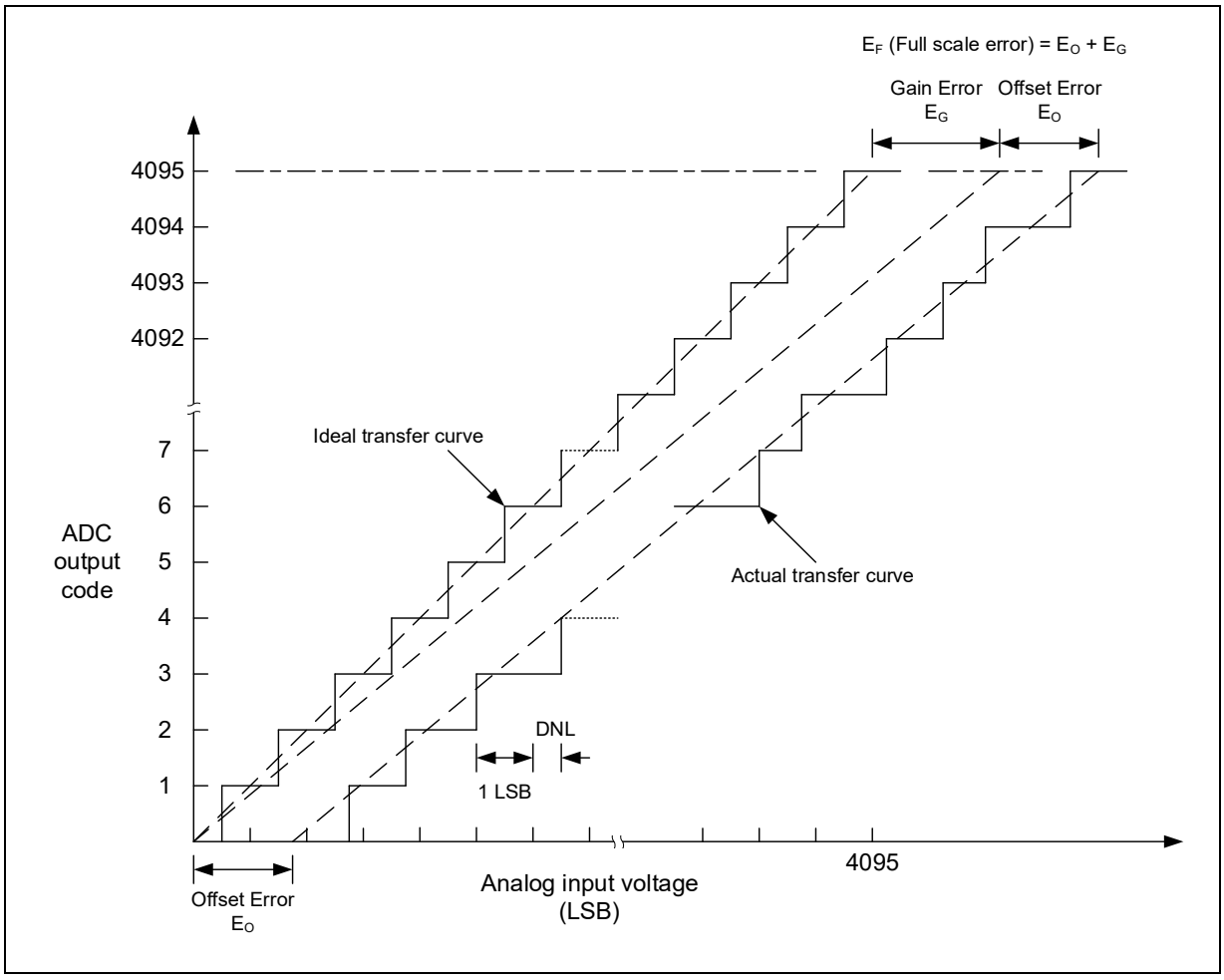
Table 8.5-3 ADC Characteristics



Notes:

1. The internal ESD diode doesn't be supported between IO and V_{DD} at 5V tolerence IO pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Analog Comparator (ACMP)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog supply voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
I_{ACMP}[2]	ACMP operating current	-	70	-	μA	MODESEL = 11
		-	35	-		MODESEL = 10
		-	2	-		MODESEL = 01
		-	1	-		MODESEL = 00
V_{CM}[2]	Input common mode voltage range	0	-	AV_{DD}	V	
V_{offset}[2]	Input offset voltage	-	±5	±10	mV	MODESEL = 11 Hysteresis disable (HYSSEL = 00)
			±10	±20		MODESEL = 00~10 Hysteresis disable (HYSSEL = 00)
			±15	±30		Without trim
V_{hys}[2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	60		HYSSEL = 100
A_v[1]	DC voltage Gain	51	70	-	dB	
T_d[2]	Propagation delay	-	50	75	ns	MODESEL = 11
		-	100	150		MODESEL = 10
		-	1	3	μs	MODESEL = 01
		-	2	6		MODESEL = 00
T_{Setup}[2]	Setup time	-	-	1	μs	MODESEL = 10~11
				30		MODESEL = 00~01
A_{CRV}[2]	CRV output voltage absolute accuracy	-1	-	1	LSB	AV_{DD} x (CRV_SEL[5:0]/63)
T_{SETUP_CRV}[2]	Setup time	-	-	0.6	μs	CRV output voltage settle to ±5%
I_{DD_CRV}[2]	Operating current	-	30	50	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-4 ACMP Characteristics

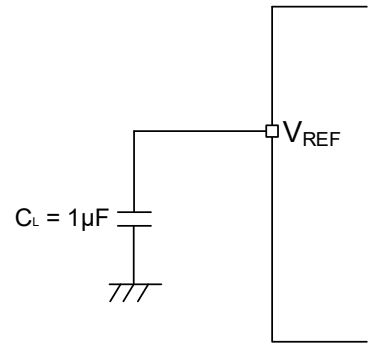
8.5.5 Internal Voltage Reference

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{REF_INT}	Internal reference voltage	TBD	1.6	TBD	V	AV_{DD} >= 2.0 V
		TBD	2.048	TBD		AV_{DD} >= 2.3 V
		TBD	2.5	TBD		AV_{DD} >= 2.8 V
		TBD	3.072	TBD		AV_{DD} >= 3.3 V
T_s[1]	Stable time	-	-	0.96	ms	C_L = 2.2 µF, V_{REF} initial = 0 V, Preload is enabled.
		-	-	6	ms	C_L = 2.2 µF, V_{REF} initial = 3.6 V, Preload is enabled.
		-	-	2	ms	C_L = 4.7 µF, V_{REF} initial = 0 V, Preload is enabled.
		-	-	15	ms	C_L = 4.7 µF, V_{REF} initial = 3.6 V, Preload is enabled.
I_{VREF_INT}[1]	V_{REF_INT} operating current	-	140	200	µA	
I_{VREF_LOAD}[1]	V_{REF_INT} output loading current	-	-	TBD	mA	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.5-5 Internal V_{REF} Characteristics



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.6 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
V_{TEMP_OS}[1]	Temperature sensor offset voltage	815	879	939	mV	CTAT T_A = 0°C
T_C[1]	Temperature Coefficient	|-2.32|	|-2.5|	|-2.68|	mV/°C	CTAT
T_S[2]	Stable time	-	2	5	µs	
T_{TEMP_ADC}[1]	ADC sampling time when reading the temperature	-	10	15	µs	
I_{TEMP}[1]	Temperature sensor operating current	-	5	8	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Table 8.5-6 Temperture Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	75	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	40		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	
t_V	Data output valid time	-	-	1	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	1	ns	1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Table 8.6-1 SPI Master Mode Characteristics

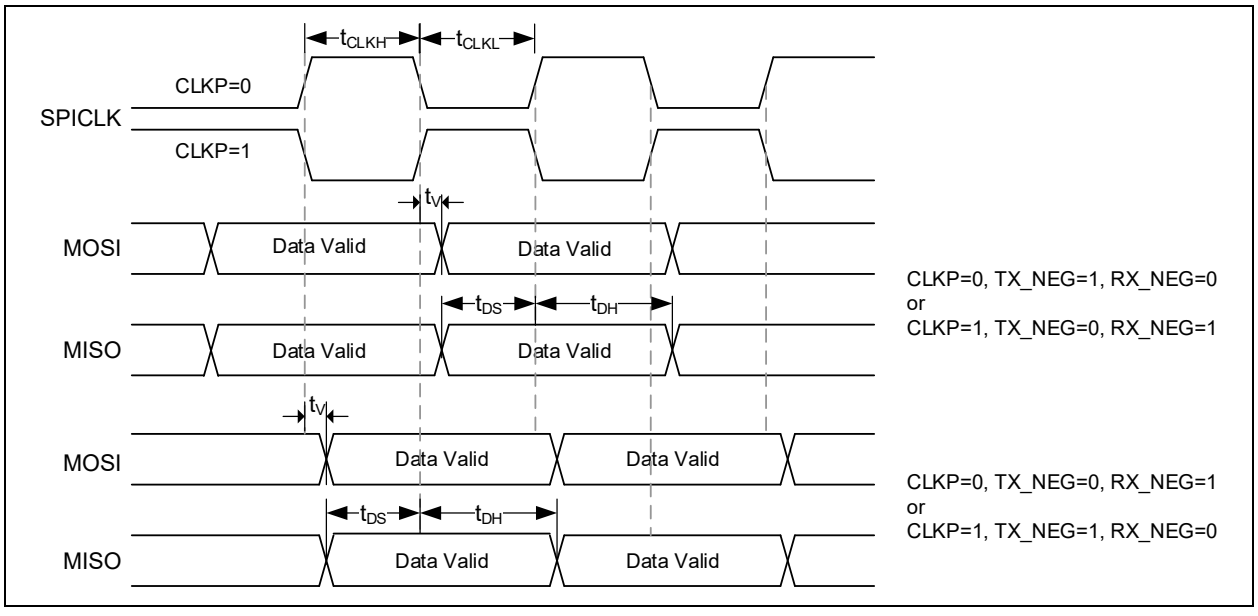


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	17	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	12.5		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 3	-	-		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		2	-	-		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_V	Data output valid time	-	-	29	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	40		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-2 SPI Slave Mode Characteristics

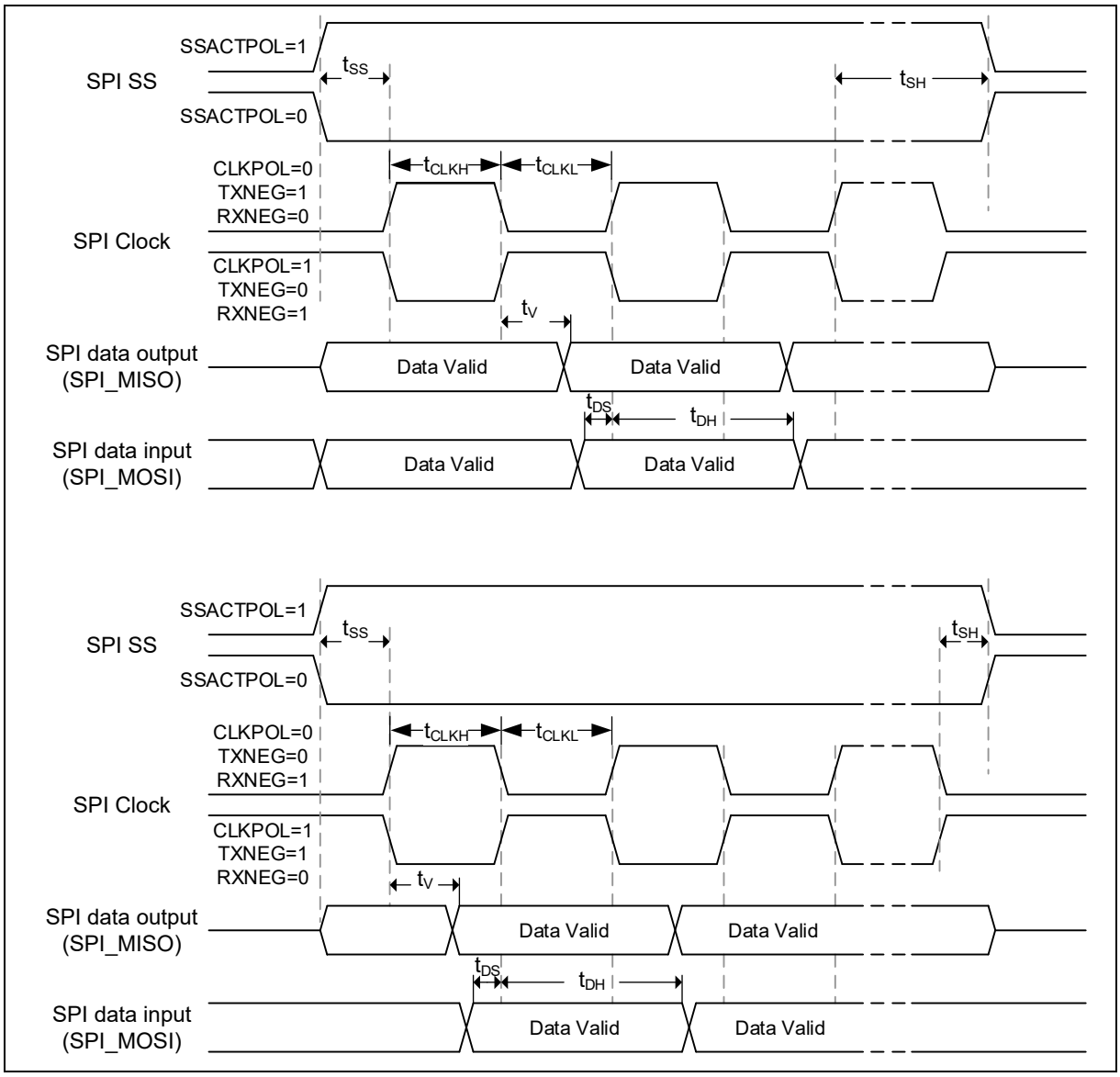


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 I²C Characteristics

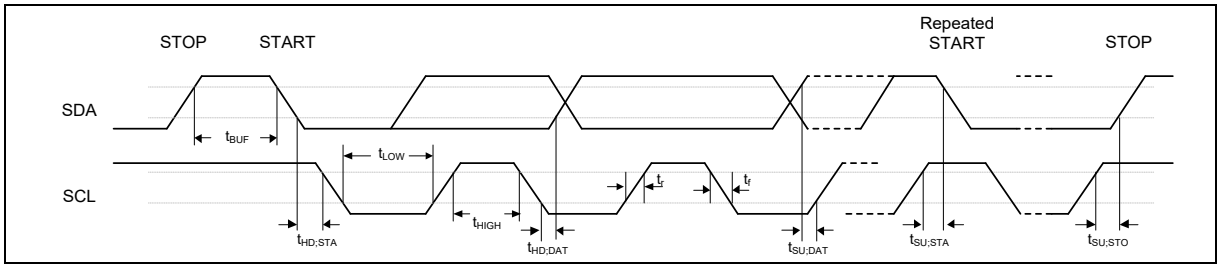


Figure 8.6-3 I²C Timing Diagram

8.6.3 I3C Dynamic Characteristics

Symbol	Parameter		I²C Mode		I3C Mode				Unit
			Open Drain		Open Drain		Push-Pull		
			Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock frequency		0.01	1	-	-	0.01	12.5	MHz
t_{LOW}	SCL Clock Low Period		500	-	-	-	32	-	ns
t_{HIGH}	SCL Clock High Period		260	-	-	-	32	-	ns
t_{cr}	SCL Clock Rise Time		-	120	-	-	-	13	ns
t_{cf}	SCL Clock Fall Time		-	120	-	-	-	13	ns
t_{SU_DAT}	Data setup time		50	-	3	-	3	-	ns
t_{HD_DAT}	Data hold time	Master	-	-	-	-	15	-	ns
		Slave	-	-	-	-	0	-	
t_{SCO}	Clock in to Data Out for Slave		-	-	-	-	-	13	ns
t_{CAS}	Clock After START(S) Condition		260 n	-	38.4 n	ENTAS0: 1 µ ENTAS1: 100 µ ENTAS2: 2 m ENTAS3: 50 m	19.2 n	-	s
t_{CBP}	Clock Before STOP(P) Condition		260 n	-	19.2 n	-	19.2 n	-	s
t_{CBSr}	Clock Before Repeated START (Sr) Condition		-	-	-	-	19.2	-	ns
t_{BUF}	Time between Stop Condition and next Start Condition		500	-	500	-	-	-	ns
t_{AVAIL}	Bus Available Condition		-	-	1	-	-	-	µs
t_{IDLE}	Bus Idle Condition		-	-	200	-	-	-	µs

Notes:

1. Guaranteed by characteristic, not tested in production.
2. I3C clock source must be greater than 125 MHz to achieve the maximum SCL Clock frequency.
3. Slave that do not support the optional ENTASx CCCs shall use the tCAS Max value *shown for ENTAS3*

Table 8.6-4 I³C Characteristics

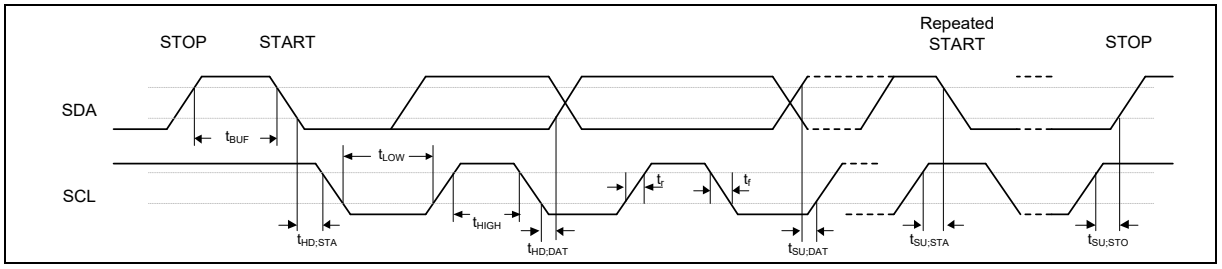


Figure 8.6-4 I³C Timing Diagram

8.6.4 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max[*1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	f_{PCLK} / 2	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	f_{PCLK} / 2		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	
t_V	Data output valid time	-	-	1	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	1	ns	1.71 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-5 USCI-SPI Master Mode Characteristics

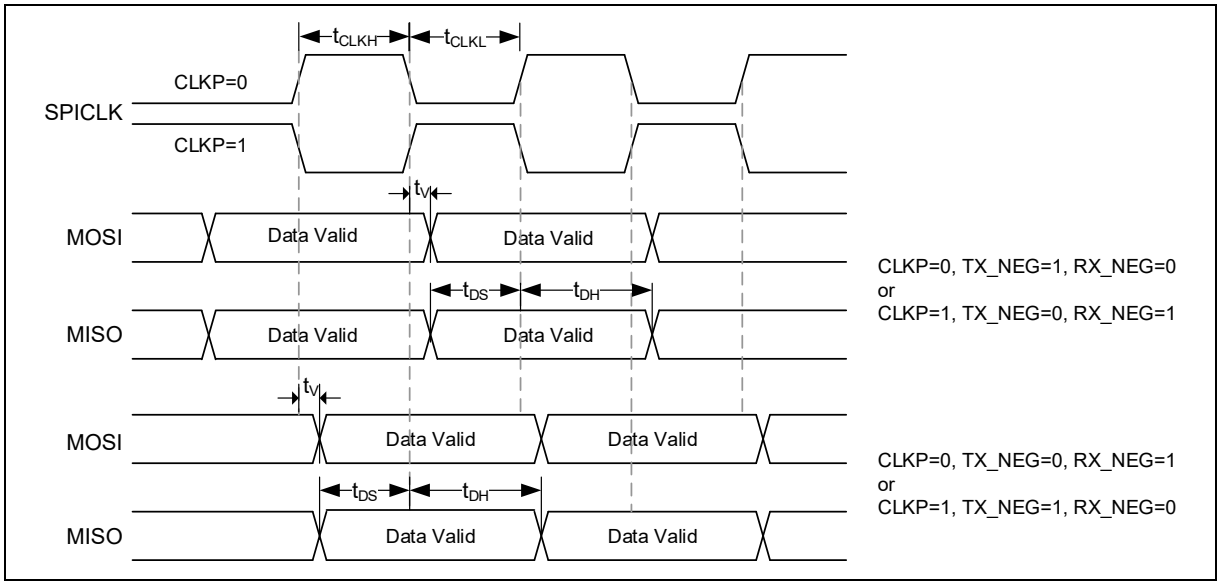


Figure 8.6-5 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	9.7	MHz	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	8		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2	-	-	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		1 T_{SPICLK} + 3	-	-		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	0	-	-	ns	
t_{DH}	Data input hold time	2	-	-	ns	
t_V	Data output valid time	-	-	51	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	-	61		1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-6 USCI-SPI Slave Mode Characteristics

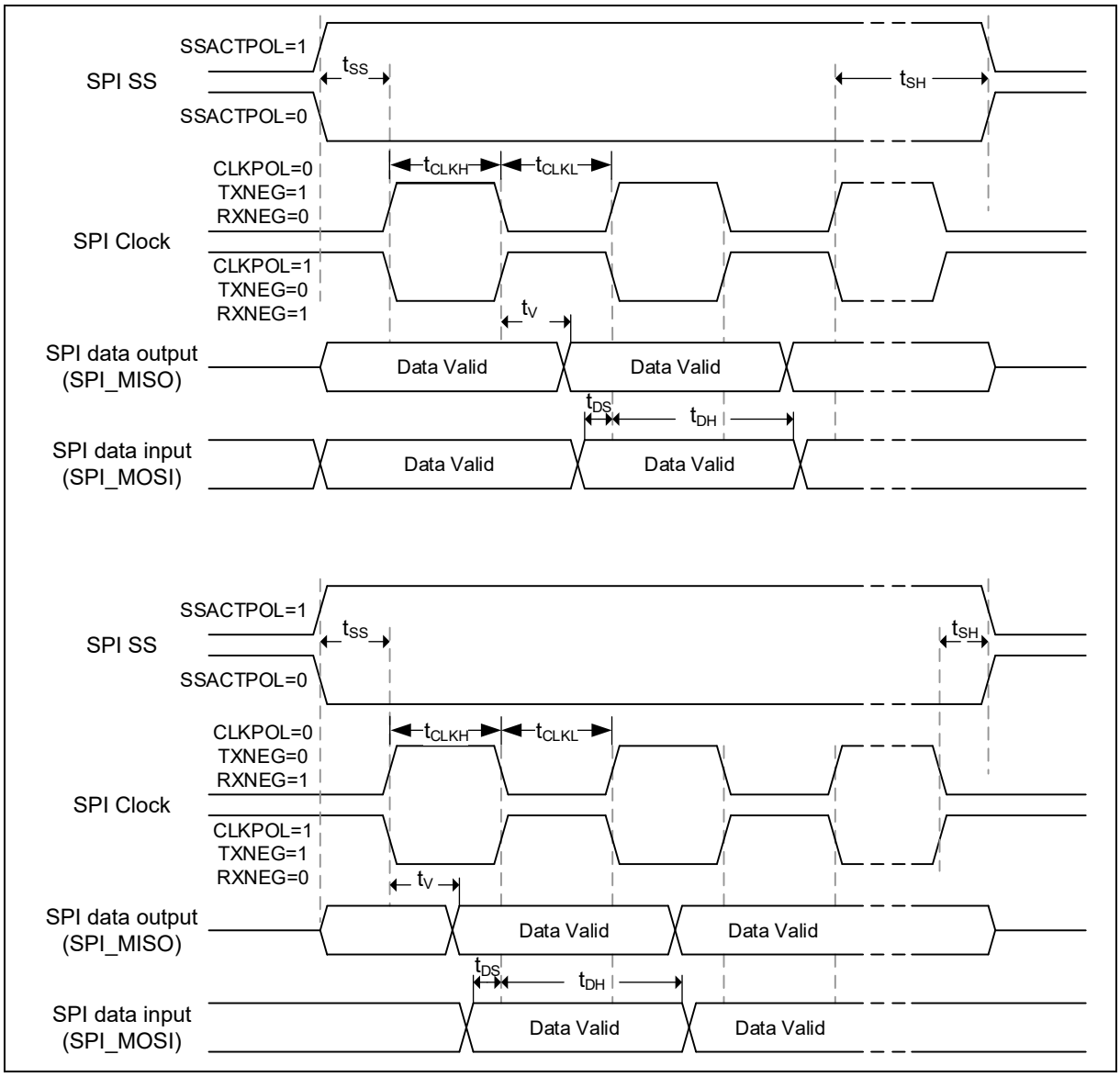


Figure 8.6-6 USCI-SPI Slave Mode Timing Diagram

8.6.5 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-7 USCI-I²C Characteristics

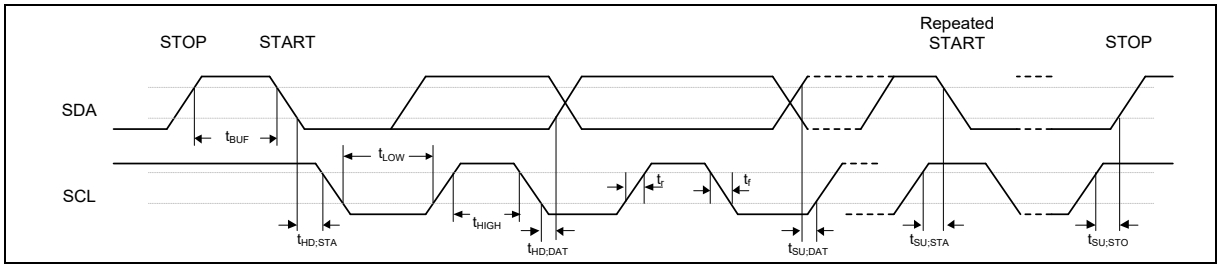


Figure 8.6-7 USCI-I²C Timing Diagram

8.6.6 CAN Characteristics

Symbol	Parameter	Min	Max [*1]	Unit	Test Conditions
t_{CAN_TXD}	TXD output delay (Normal Slew Rate)	-	16.5	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	26.5	ns	1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
t_{CAN_RXD}	RXD input delay	-	5.0	ns	2.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF
		-	6.0	ns	1.7 V ≤ V_{DD} ≤ 3.6 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-8 CAN Characteristics

8.6.7 USB Characteristics

8.6.7.1 USB High-Speed PHY characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	High Speed Driver rise time	400	-	-	ps	C_L = 5 pF
T_{FF}	High Speed Driver fall time	400	-	-	ps	C_L = 5 pF
T_{FRFF}	Rise and Fall Time Matching	90		111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-9 USB High-Speed PHY Characteristics

8.6.8 SDIO Characteristics

8.6.8.1 SDIO Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P_SD_CLK_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H_SD_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-10 SDIO Default Mode Timing

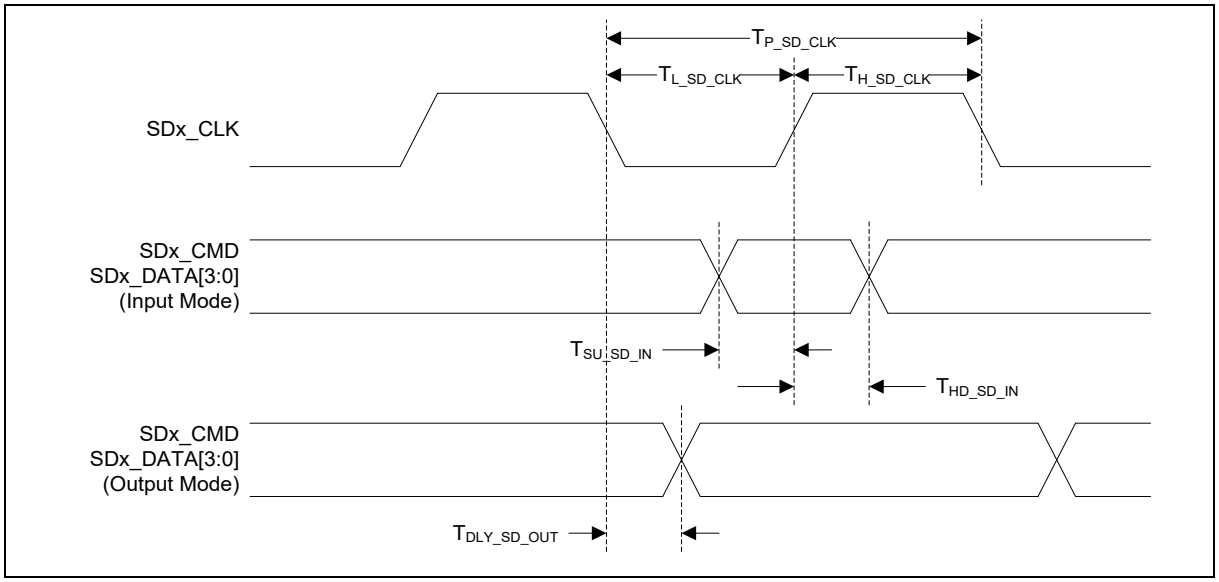


Table 8.6-11 SDIO Default Mode

8.6.8.2 SDIO Dynamic characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H_SD_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD_SD_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-12 SDIO Dynamic Characteristics

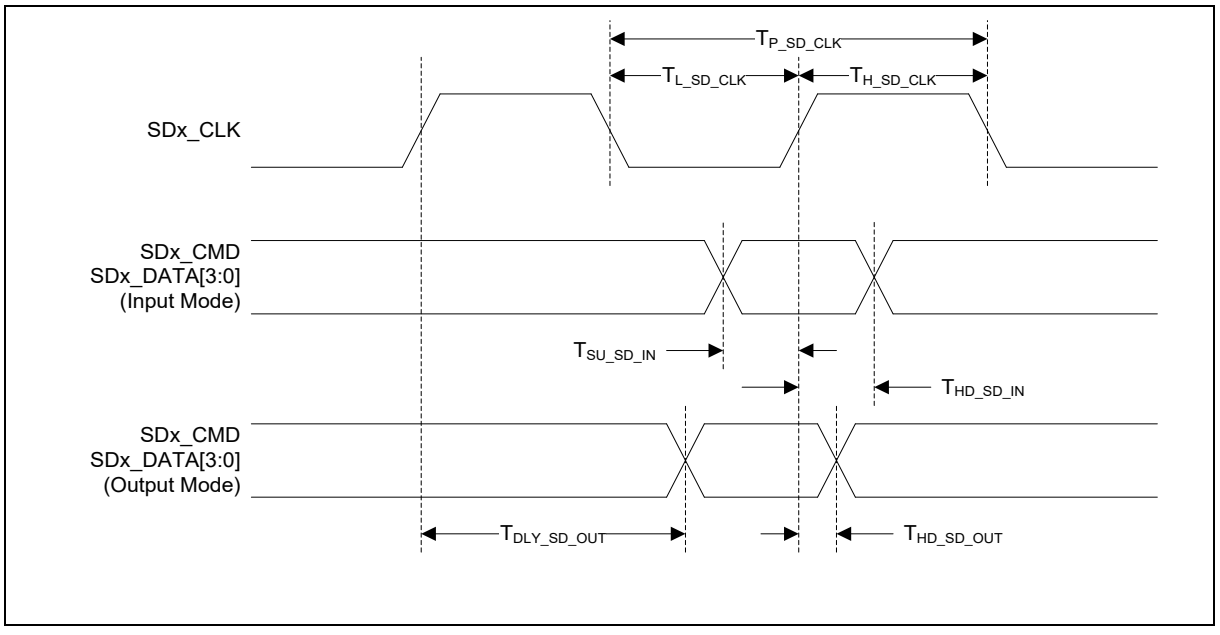


Table 8.6-13 SDIO High-speed Mode

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	0.99	1.1	1.21	V	T_A = 25°C
T_{ERASE}	Page erase time	8	12.1	20	ms	
T_{PROG}	Program time	47	57.5	66	µs	
I_{DD1}	Read current	-	-	4	mA	
I_{DD2}	Program current	-	5	-	mA	
I_{DD3}	Erase current	-	4	-	mA	
N_{ENDUR}	Cycling Endurance	100,000	-	-	cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	10	-	-	year	100 kcycle[2] , T_J = 25°C

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The Flash data can only be programmed once at the same address after Flash erase.
3. Guaranteed by design.

Table 8.7-1 Flash DC Electrical Characteristics

9 ABBREVIATIONS

9.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
CCAP	Camera Capture Interface
DAP	Debug Access Port
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
ECAP	Enhanced Capture
EHCI	Enhanced Host Controller Interface
EPWM	Enhanced Pulse Width Modulation
ELLSI	Enhanced LED Light Strip Interface
EQEI	Enhanced Quadrature Encoder Interface
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	48 MHz Internal High Speed RC Oscillator
HXT	4~32 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	38.4 kHz internal low speed RC oscillator (LIRC)
LLSI	LED Light Strip Interface
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller

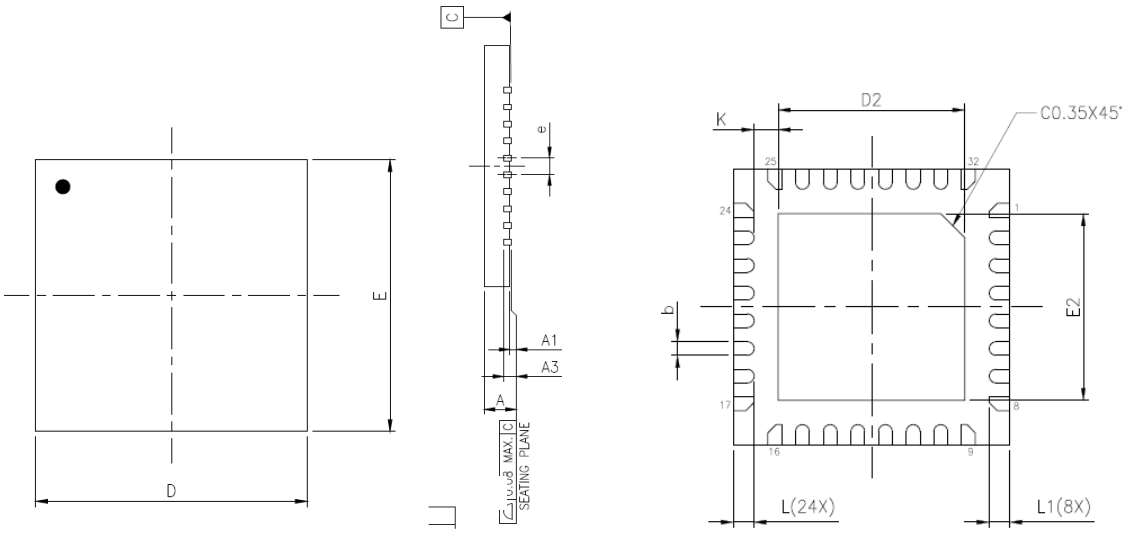
OHCI	Open Host Controller Interface
PCLK	The Clock of Advanced Peripheral Bus
PDCI	Parallel Dimming Communication Interface
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
EQEI	Enhanced Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPBC	Serial Parallel Broadcastt Controller
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 9.1-1 List of Abbreviations

10 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

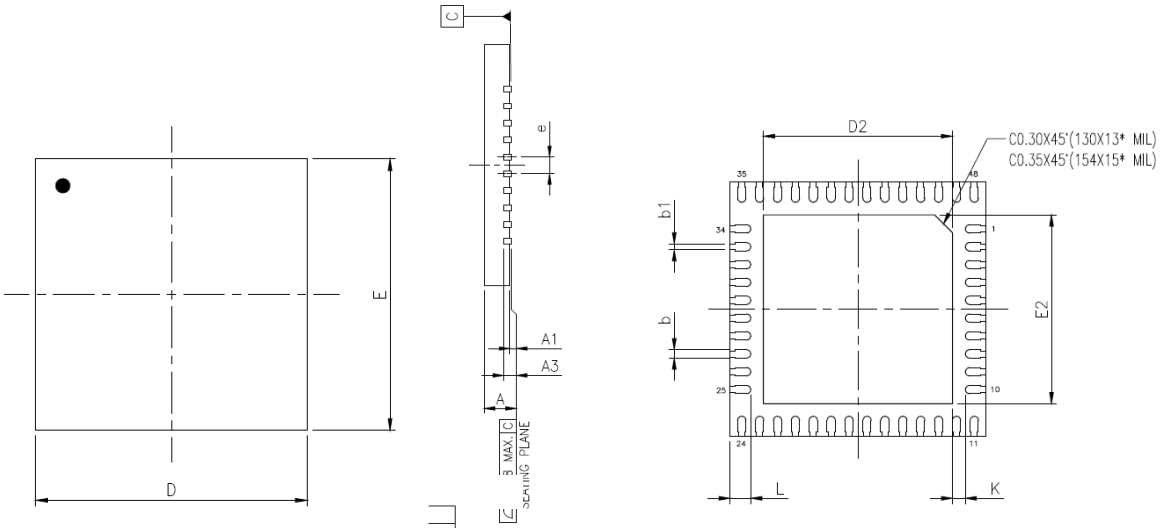
10.1 QFN32L 4x4mm, Thickness 0.80mm, Lead_Pitch 0.40mm, Lead_Length 0.30mm, EP Size 2.70x2.70mm



PKG CODE	WQFN(X432)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
e	0.40 BSC		
L	0.25	0.30	0.35
L1	0.23	0.28	0.33
K	0.20	—	—

PAD SIZE	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
122X12R MIL	2.65	2.70	2.75	2.65	2.70	2.75

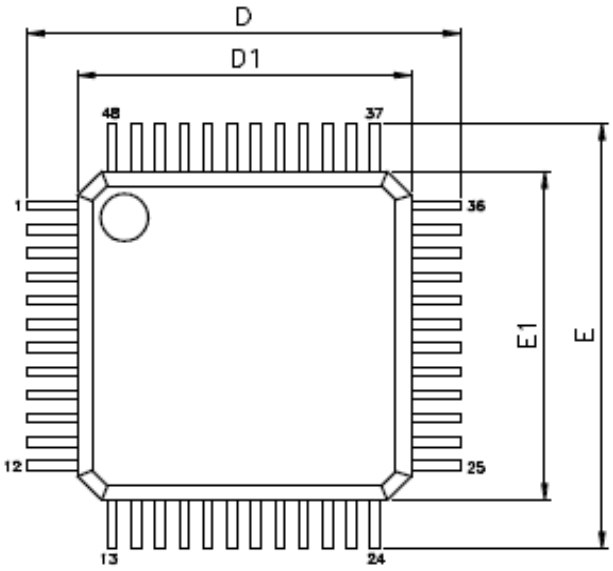
10.2 QFN48L 5x5mm, Thickness 0.80mm, Lead_Pitch 0.35mm, Lead_Length 0.40mm, EP Size 3.70x3.70mm



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—

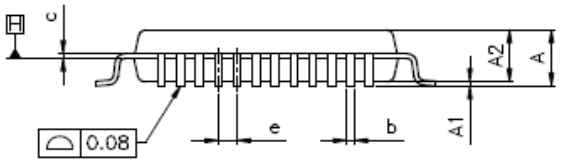
PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
130X13* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45
154X15* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45

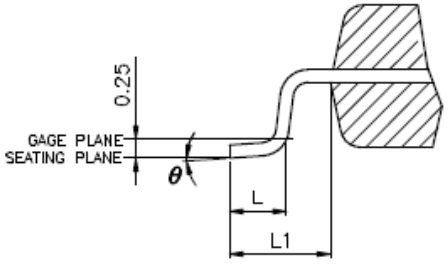
10.3 LQFP48L 7x7mm, Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm



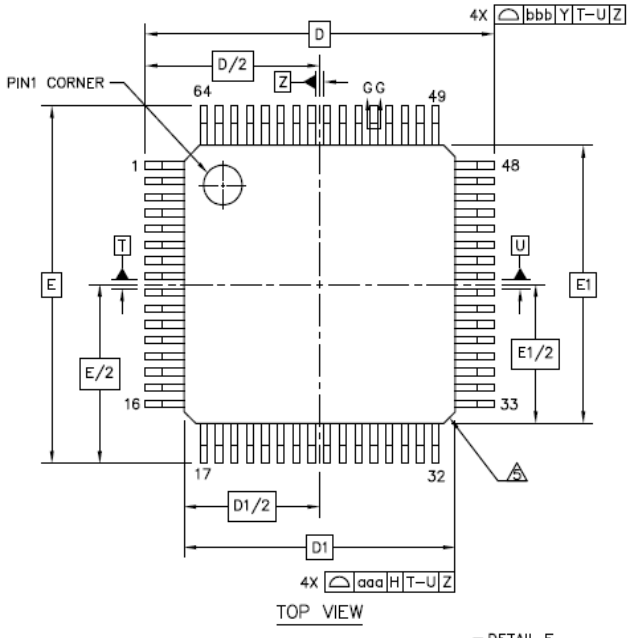
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

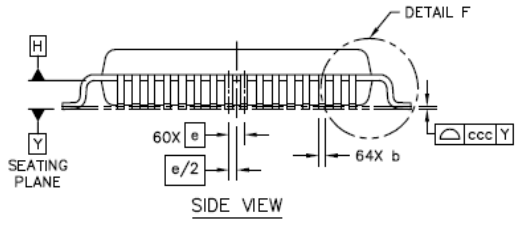
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°

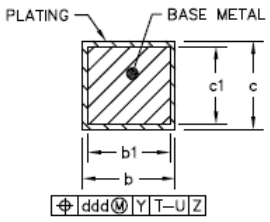




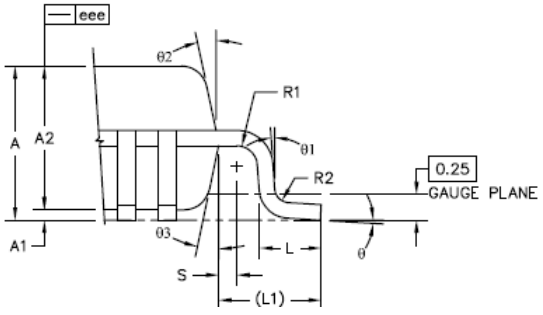
10.4 LQFP64L 7x7mm, Thickness 1.40mm, Lead_Pitch 0.40mm, Lead_Length 1.00mm



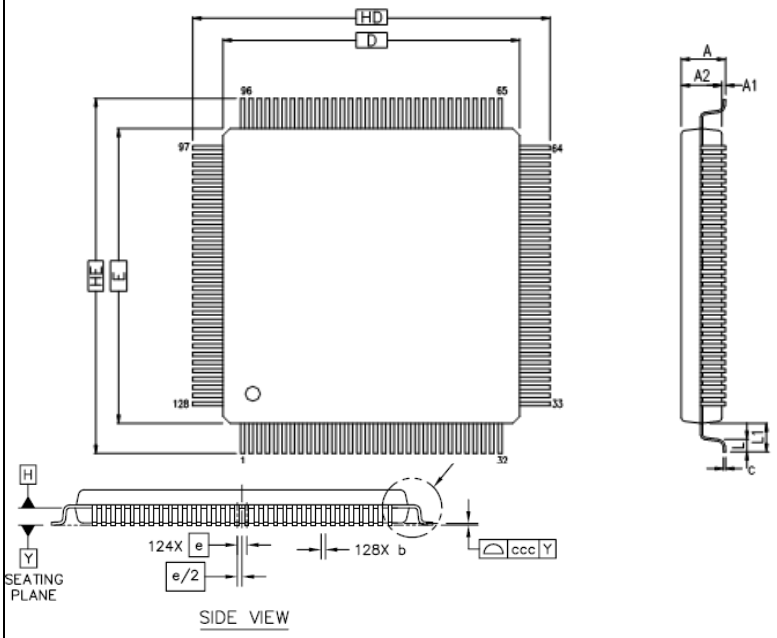




		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



10.5 LQFP128L 14x14mm, Thickness 1.40mm, Lead_Pitch 0.40mm, Lead_Length 1.00mm



SIDE VIEW

SYMBOL	MIN	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
HD	15.85	16.00	16.15
D	13.85	14.00	14.15
HE	15.85	16.00	16.15
E	13.85	14.00	14.15
b	0.13	0.16	0.23
e	-	0.40	-
θ°	0	3.5	7
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
Y	-	-	0.10

11 REVISION HISTORY

Date	Revision	Description
2026.03.17	1.00	Initial version

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