## NuMicro® Family

## Arm® Cortex®-M23-based Microcontroller

# M2L31 Series
# Datasheet

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# 1 GENERAL DESCRIPTION

The NuMicro® M2L31 series is based on Arm Cortex-M23 core at Armv8-M architecture with a single-cycle hardware multiplier/divider. It runs up to 72 MHz and features 64 to 512 Kbytes ReRAM, 40 to 168 Kbytes SRAM, 1.71V to 3.6V operating voltage, -40°C to 105°C wide operating temperature, a variety of packages choices, and excellent high immunity characteristics by 4 KV ESD HBM and 4.4 KV EFT. The dual bank design of 512 Kbytes ReRAM supports firmware update through the Over-The-Air (FOTA) process. The M2L31 series supports Execute-Only Memory (XOM) function to protect confidential program code information from being stolen in the run-time.

**ReRAM (Resistive Random-Access Memory)**

A type of non-volatile memory achieves digital data storage by altering the resistance state of its components through the application of an external voltage. It boasts three major characteristics: fast read/write speeds, low power consumption, and superior durability, making it hailed as the next-generation embedded universal memory. Unlike embedded Flash memory, ReRAM doesn't require a page erase operation before writing, resulting in faster write speeds and a more straightforward and speedy operation similar to EEPROM. Furthermore, ReRAM consumes less energy for storing each bit compared to what is needed in Flash memory. Additionally, because each storage unit can be individually set or reset, it offers greater endurance than Flash memory.

**Enhanced Analog Features**

The M2L31 series provides up to three Programmable Gain Amplifiers (PGA) to amplify the small voltage changed by amplification factors of 1, 2, 4, 8, 16, and 32, three comparators in conjunction with PWM to ensure cycle-by-cycle over current limiting for increased application safety and robustness, one 24-ch high-speed 3.6 MSPS 12-bit SAR ADC, up to two 12-bit 1 MSPS DAC to provide precise voltage reference to other analog device, and up to 24-ch 16-bit PWM for precise modulation and optimized for controlling half bridge or H-bridge motor drive circuits. It is eligible for motor control, industrial automation, home appliance.

**USB 2.0 Type-C Power Delivery 3.0 Controller**

The M2L31 series includes one controller compliant with USB Type-C Rev. 2.1 and USB Power Delivery Rev. 3.0 specifications. The controller featuring USB Type-C pull-up and pull-down resistors, Dead battery and fast role swap supported, and flexible Power Delivery along with data transmission over a single cable.

**Low-Power Technology**

The M2L31 series provides low power consumption in Normal Run mode 60 μA/MHz at 72 MHz, 33 μA/MHz in idle run mode. It supports 6 core power-down levels, including Fast Wake-up Power-down, Normal Power-down, Low Leakage Power-down, Ultra Low Leakage Power-down, Standby Power-down, and Deep Power-down mode. Beside LIRC/LXT can be operated in Low Leakage Power-down mode, the MIRC can also work for operation of high precision sensors by shorten stable time of clock; in Ultra Low Leakage Power-down mode the M2L31 series provides Auto-operation mode to process the sensor data through low power serial interface with low power DMA and 8KB standalone low power SRAM without interrupting CPU. The current consumption of Standby Power-down modes with RAM retention is 3.2uA, and Deep Power-down mode is less than 0.5 μA.

**Enhanced Security Levels**

The M2L31 series supports eXecute-Only-Memory (XOM) to protect the intelligent property of developers. It is also equipped with rich functions to improve system security. The Secure Bootloader supports system-boot feature to protect cerificated firmware from being replaced with malware in the upgrade processing. The hardware crypto accelerators, including AES, PRNG, and TRNG, support encryption and decryption operations to offload the main processor's computing power and ensure data transmission in secure. Beside the configureration words and register setting for write protection, the M2L31 series is also equipped with one hardware PIN Lock function to conduct dual function protect protection. One of the major challenges for IoT devices that are connected to cloud services is security, so the IoT devices must meet some security requirements to secure assets from being stolen or modified by an attacker.

**Rich peripherals for comprehensive product application scenarios**

The M2L31 series provides plenty of peripherals such as Timers, Watchdog Timers, RTC with independent $V_{BAT}$ pin, up to 16 channels of PDMA, up to 16 independent capacitive touch key sensing function with single-scan or programmable periodic key-scans modes, up to 2 sets of CAN FD controller with internal 12Kbytes SRAM, USB 2.0 FS OTG Host and device controllers, up to 8 sets of UART, up to 4 sets of I2C, up to 4 sets of SPI/I2S,1 set of QSPI, and 2 sets of Universal Serial Control Interfaces (USCI); moreover, it supports enhanced control interfaces such as Voltage adjustable interface (VAI), External Bus Interface (EBI), eCAP and QEI interface to detect the motor spinning position.

Supported packages include WLCSP 25 (2.5 mm x 2.5 mm), QFN32 (5 mm x 5 mm), LQFP48 (7 mm x 7 mm), QFN 48 (5 mm x 5 mm), WLCSP 49 (3.0 mm x 3.0 mm), LQFP64 (7 mm x 7 mm), and LQFP128 (14 mm x 14 mm).

For the development, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclipse IDE with GNU GCC compilers are also supported.

USCI*: supports UART, SPI or $I^2C$

| Product Line | UART | $I^2C$ | SPI/$I^2S$ | USCI* | USB OTG | CAN FD | Timer | PDMA | PGA | ADC | DAC | ACMP | PWM |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| M2L31 | 8 | 4 | 4 | 2 | 1 | 2 | 4 | 16 | 3 | 24 | 2 | 3 | 24 |

Table 6.2-1 NuMicro M2L31 Series Key Features Support Table

The M2L31 series is suitable for a wide range of applications such as:

- Motor Control
- PC Peripherals
- Industrial Automatic Related Products
- Battery Management System

# 2 FEATURES

## 2.1 M2L31 Series Features

| *Core and System* | |
|---|---|
| **Arm Cortex-M23 without TrustZone** | Arm Cortex-M23 core, running up to 72 MHz when VDD = 1.71V ~ 3.6V<br>Built-in PMSAv8 Memory Protection Unit (MPU)<br>Built-in Nested Vectored Interrupt Controller (NVIC)<br>32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider<br>24-bit system tick timer<br>Supports Programmable and maskable interrupt<br>Supports Low Power Sleep mode by WFI and WFE instructions<br>Supports single cycle I/O access<br>Supports XOM feature with 4 regions |
| **Low power mode and current** | Low Power mode:<br>– Idle mode<br>Power-down mode:<br>– Normal Power-down mode (NPD)<br>– Standby Power-down mode (SPD)<br>– Deep Power-down mode (DPD) |
| **Wake-up source and wakeup time** | EINT, USCI, RTC, WDT, I²C, Timer, UART, BOD, LVR, POR, GPIO, USBD, USBH, USBOTP, ACMP, LPTMR, TTMR, OPA, LPUART, LPI²C, LPSPI, LPPDMA, LPADC, TouchKey, UPTPD, Debug interface, WKTMR, WKIO, Reset pin from NPD0~NPD2<br>RTC, WDT, BOD, LVR, POR, ACMP, LPTMR, TTMR, OPA, LPUART, LPI²C, LPSPI, LPPDMA, LPADC, Debug interface, WKTMR, WKIO, Reset pin from NPD3~NPD4<br>RTC, BOD, LVR, POR, ACMP, WKTMR, WKIO, Reset pin from NPD5, SPD0~SPD2<br>RTC, WKTMR, POR, Wake-up pins, Tamper from DPD0~DPD1 |
| **Power supply and low voltage detect** | Built-in LDO for wide operating voltage from 1.71V to 3.6V<br>Core power voltage: 1.1V<br>Brown-out detector<br>– With 7 levels: 3.0V/2.8V/2.6V/2.4V/2.2V/2.0V/1.8V/1.6V<br>– Supports Brown-out Interrupt and Reset option<br>Low Voltage Reset (LVR) with 1.5V threshold voltage level |
| **Cyclic Redundancy Calculation Unit** | Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 |

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| | Programmable order reverse setting for input data and CRC checksum<br>Programmable 1's complement setting for input data and CRC checksum<br>Supports 8-/16-/32-bit of data width<br>Programmable seed value<br>8-bit write mode: 1-AHB clock cycle operation<br>16-bit write mode: 2-AHB clock cycle operation<br>32-bit write mode: 4-AHB clock cycle operation<br>Supports using PDMA to write data to perform CRC operation |
| **Voltage Adjustable Interface** | Supports up to 6 VAI pins<br>User Configurable 1.71V ~ 3.6V I/O Interface with a dedicated power input ($V_{DDIO}$)<br>Supports CAN FD, UART, QSPI, SPI, $I^2C$, LPUART, LPSPI and LPI2C interface |
| **Security** | 96-bit Unique ID (UID)<br>128-bit Unique Customer ID (UCID) |
| ***Memories*** | |
| **Boot Loader** | Factory pre-loaded mask ROM for secure boot procedure and ISP procedure<br>Uses SHA-256 and ECDSA-P256 to validate data in APROM and LDROM<br>NuMicro ISP Programming Tool for firmware upgrade via UART, CAN FD, SPI, $I^2C$ and high speed USB device |
| **ReRAM** | Up to 512 KB on-chip Application ROM (APROM)<br>Dual bank 512 Kbytes APROM for Over-The-Air (OTA) upgrade<br>Four eXecute-Only-Memory (XOM) regions for code protection<br>Embedded with 4 Kbytes cache, with performance at zero wait cycle in continuous address read access<br>8 Kbytes on-chip user-defined loader (LDROM)<br>3 Kbytes One Time Programmable (OTP) ROM for data security<br>32-bit ReRAM programming function.<br>Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded ReRAM memory<br>Supports CRC-32 checksum calculation function<br>Hardware external read protection of whole ReRAM memory by Security Lock Bit<br>2-wired ICP ReRAM updating through SWD interface |
| **SRAM** | Up to 168 KB embedded SRAM |

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| | – 40 Kbytes SRAM located in bank 0 with programmable size of SPD retention The total 40 Kbytes supports hardware parity check; Exception (NMI) generated upon a parity check error<br>– 128 Kbytes SRAM located in bank 1 with SPD retention<br>Supports byte-, half-word- and word-access<br>Supports PDMA mode |
| **Peripheral DMA (PDMA)** | Up to 16 independent configurable channels for automatic data transfer between memories and peripherals<br>Channel 0, 1 support time-out function<br>Basic and Scatter-Gather Transfer modes<br>Each channel supports circular buffer management using Scatter-Gather Transfer mode<br>Two types of priorities modes: Fixed-priority and Round-robin modes<br>Transfer data width of 8, 16, and 32 bits<br>Single and burst transfer type<br>Source and destination address can be increment or fixed<br>PDMA transfer count up to 65536<br>Request source form software, SPI/I²S, UART, USCI, EADC, DAC, PWM capture event or TIMER |
| ***Clocks*** | |
| **External Clock Source** | Built-in 4~32 MHz external high speed crystal oscillator (HXT) for precise timing operation<br>Built-in 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation<br>Supports clock failure detection for high/low speed external crystal oscillator<br>HXT clock frequency accuracy detector |
| **Internal Clock Source** | Built-in 12 MHz internal high speed RC oscillator (HIRC) for system operation<br>Built-in 48 MHz internal high speed RC oscillator (HIRC48M) for system operation<br>Built-in 1/2/4/8 MHz internal high speed RC oscillator (MIRC) for system operation<br>Built-in 32 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation.<br>Supports one PLL up to 144 MHz for high performance system operation, sourced from HIRC and HXT |
| ***Timers*** | |
| **32-bit Timer** | **TIMER mode**<br>4 sets of 32-bit timers with 24-bit up counters and 8-bit prescale |

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| | counters |
| | Independent clock source for each timer |
| | One-shot, Periodic, Toggle and Continuous Counting operation modes |
| | Event counting function to count the event from external pin |
| | Input capture function to capture or reset counter value |
| | External capture pin event for interval measurement |
| | External capture pin event to reset 24-bit up counter |
| | Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated |
| | Timer interrupt flag or external capture interrupt flag to trigger EPWM, PWM, EADC, LPADC, DAC and PDMA |
| | Internal capture triggered source from ACMP output |
| | Inter-Timer trigger capture mode |
| | **PWM mode** |
| | 16-bit compare register and period register |
| | Double buffer for period register and compare register |
| | Supports inverse in PWM output |
| | PWM interrupt wake-up from system Power-down mode |
| **Enhanced PWM (EPWM)** | Twelve 16-bit counters with 12-bit clock prescale for twelve 144 MHz PWM output channels |
| | Up to 12 independent input capture channels with 16-bit resolution counter |
| | Supports dead time with maximum divided 12-bit prescale |
| | Up, down or up-down PWM counter type |
| | Supports complementary mode for 3 complementary paired PWM output channels |
| | Synchronous function for phase control |
| | Counter synchronous start function |
| | Brake function with auto recovery mechanism |
| | Mask function and tri-state output for each PWM channel |
| | Trigger EADC or DAC to start conversion immediately |
| | Trigger EADC to start conversion after a short delay |
| | Supports External Pin Trigger function |
| **PWM** | Supports maximum clock frequency up to 72 MHz |
| | Up to two PWM modules; each module provides 6 output channels. |
| | Supports independent mode for PWM output/Capture input channel |
| | Supports complementary mode for 3 complementary paired PWM output channels: |

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| | – Dead-time insertion with 12-bit resolution<br>Two compared values during one period<br>Supports 12-bit prescaler from 1 to 4096<br>Supports 16-bit resolution PWM counter:<br>– Up, down or up/down counter operation type<br>Supports mask function and tri-state enable for each PWM pin<br>Supports brake function:<br>– Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)<br>– Noise filter for brake source from pin<br>– Edge detect brake source to control brake state until brake interrupt cleared<br>– Level detect brake source to auto recover function after brake condition removed<br>Supports interrupt on the following events:<br>PWM counter match 0, period value or compared value<br>Brake condition happened<br>Supports trigger ADC on the following events:<br>PWM counter match 0, period value or compared value<br>Capture Function Features:<br>– Up to 12 capture input channels with 16-bit resolution<br>– Supports rising or falling capture condition<br>– Supports input rising/falling capture interrupt<br>– Supports rising/falling capture with counter reload option<br>Supports PDMA transfer function for all PWM channels |
| **Watchdog** | 20-bit free running up counter for WDT time-out interval<br>Clock sources from LIRC (default), HCLK/2048 or LXT<br>9 selectable time-out periods<br>Able to wake up from Power-down or Idle mode<br>Interrupt or reset selectable on watchdog time-out<br>Selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period<br>Force WDT enabled after chip power on or reset<br>WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT |
| **Window Watchdog** | Clock sources from HCLK/2048 (default) or LIRC<br>Window set by 6-bit down counter with 11-bit prescaler<br>WWDT counter suspends in Idle/Power-down mode |

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| | Supports Interrupt |
| **RTC** | Supports external power pin $V_{BAT}$ |
| | Software compensation by setting frequency compensate register (FCR),compensated clock accuracy reaches ±5ppm within 5 seconds |
| | RTC counter (second, minute, hour) and calendar counter (day, month, year) |
| | Alarm registers (second, minute, hour, day, month, year) |
| | Selectable 12-hour or 24-hour mode |
| | Automatic leap year recognition |
| | Day of the Week counter |
| | Daylight Saving Time software control |
| | Periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 or 1 second |
| | 1 Hz clock output for RTC calibration |
| | Wake-up from idle mode and Power-down mode |
| | 32 kHz oscillator gain control |
| | RTC Time Tick and Alarm Match interrupt |
| **Tamper** | 20 bytes spare registers and 3 tamper pins to clear the content of these spare registers |
| | Selectable spare register erase function |
| | Supports Timestamp function |
| ***Analog Interfaces*** | |
| **Enhanced Analog-to-Digital Converter (EADC)** | Up to one set of 12-bit, 31-ch 3.42 MSPS SAR EADC with up to 24 single-ended input channels or 12 differential input pairs; 10-bit accuracy is guaranteed |
| | Seven internal channels for $V_{BAT}$, $AV_{DD}$, OPA0/1/2 output, band-gap VBG input and Temperature sensor input |
| | Supports external $V_{REF}$ pin or internal reference voltage |
| | Supports Power-down mode |
| | Supports calibration capability |
| | Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse or EPWM/PWM |
| | Configurable EADC sampling time |
| | Up to 31 sample modules |
| | Double data buffers for sample module 0~3 |
| | PDMA operation |
| | Supports Averageing mode and Oversampling mode, where Oversampling mode provides up to 16-bit precision |
| | Supports early interrupt with delay counter feature |

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| **Digital-to-Analog Converter (DAC)** | Up to one 12-bit 1 MSPS voltage type DAC<br>Analog output voltage: 0~$V_{REF}$ ($AV_{DD}$)<br>Supports 8-bit and 12-bit mode<br>Rail to rail settle time 6us<br>Reference voltage selects from internal reference voltage, $AV_{DD}$ or $V_{REF}$ pin<br>Max. output voltage $AV_{DD}$ -0.2V in buffer mode<br>Conversion started by software enable, Timer interrupt flag(TIF) or PDMA trigger<br>Voltage output buffer mode and bypass voltage output buffer mode<br>Supports PDMA mode |
| **Analog Comparator (ACMP)** | Up to three rail-to-rail analog comparators<br>4 multiplexed I/O pins at positive node<br>Negative node:<br>– One I/O pin<br>– Band-gap (VBG)<br>– DAC0 output<br>– Comparator Reference Voltage (CRV)<br>Programmable propagation speed and low power consumption<br>Interrupts generated when compare results change (Interrupt event condition programmable)<br>Supports Power-down Wake-up<br>Supports triggers for break events and cycle-by-cycle control for PWM<br>Supports window compare mode and window latch mode<br>Supports programmable hysteresis window:<br>– 0 mV, 20 mV or 40 mV<br>Supports offset calibration |
| **OPA** | Analog input voltage: 0~$AV_{DD}$<br>Up to three operational amplifier<br>Supports to use schmitt trigger buffer output for simple comparator function<br>Supports schmitt trigger buffer output interrupts |
| **Internal Reference Voltage** | Internal reference voltage select: 1.6V, 2.0V, 2.5V, 3.0V for EADC, DAC and CRV (comparator reference voltage) reference voltage |
| ***Communication Interfaces*** | |
| **UART** | Supports up to 8 UARTs: UART0~7<br>UART baud rate clock from LXT(32.768 kHz) with 9600bps in Power- |

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| | down mode<br>Baud rate up to 10 Mbps<br>Full-duplex asynchronous communications<br>Supports one-wire half-duplex communications<br>Separates receive and transmit 16/16 bytes FIFO<br>Programmable receiver buffer trigger level<br>Hardware auto-flow control (CTS and RTS)<br>IrDA (SIR) function:<br>– Supports 3/16 bit duration for normal mode<br>RS-485 9-bit mode and direction control<br>UART0/1 supports LIN function:<br>– LIN master/slave mode<br>– Programmable break generation function for transmitter<br>– Break detection function for receiver<br>Programmable baud-rate generator up to 1/16 system clock<br>8-bit receiver FIFO time-out detection function<br>Programmable transmitting data delay time between the last stop and the next start bit<br>Auto-Baud Rate measurement and baud rate compensation function<br>Break error, frame error, parity error and receive/transmit FIFO overflow detection function<br>Supports RS-485 mode:<br>– RS-485 9-bit mode<br>– Hardware or software enables to program nRTS pin to control RS-485 transmission direction<br>– nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in Power-down mode.<br>– Hardware or software enables to program nRTS pin to control RS-485 transmission direction<br>Fully programmable serial-interface:<br>– Programmable number of data bit, 5-, 6-, 7-, 8- bit character<br>– Programmable parity bit, even, odd, no parity or stick parity bit generation and detection<br>– Programmable stop bit, 1, 1.5, or 2 stop bit generation<br>Supports PDMA mode |
| **Quad SPI** | Supports one set of Quad SPI with Master/Slave mode<br>Master mode up to 36 MHz ($V_{DD}$ = 2.7V ~ 3.6V)<br>Slave mode up to 18 MHz ($V_{DD}$ = 2.7V ~ 3.6V) |

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| | Supports Dual and Quad I/O Transfer mode |
| | Supports one data channel half-duplex transfer |
| | Supports double data rate mode (Master TX DIR Mode Only) |
| | Supports receive-only mode |
| | Configurable bit length of a transfer word from 8 to 32-bit |
| | Provides separate 8-level depth transmit and receive FIFO buffers |
| | Supports MSB first or LSB first transfer sequence |
| | Supports the byte reorder function |
| | Supports Byte or Word Suspend mode |
| | Supports 3-wired, no slave select signal, bi-direction interface |
| | PDMA operation |
| **$I^2C$** | Up to 4 sets of $I^2C$ devices |
| | Master/Slave mode |
| | Bidirectional data transfer between masters and slaves |
| | Multi-master bus (no central master) |
| | 7-bit and 10-bit addressing mode |
| | Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) |
| | Arbitration between simultaneously transmitting masters without corruption of serial data on the bus |
| | Serial clock synchronization allows devices with different bit rates to communicate via one serial bus |
| | Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer |
| | Supports 14-bit time-out counter requesting the $I^2C$ interrupt if the $I^2C$ bus hangs up and timer-out counter overflows |
| | Programmable clocks allow versatile rate control |
| | Multiple address recognition (four slave address with mask option) |
| | Supports setup/hold time programmable |
| | Supports SMBus and PMBus |
| | Multi-address Power-down wake-up function |
| | Supports PDMA transfer |
| SPI/$I^2S$ | Up to four sets of SPI/I2S controllers with Master/Slave mode |
| | Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers |
| | **SPI** |
| | Master mode up to 36 MHz ($V_{DD}$ = 2.7V ~ 3.6V) |
| | Slave mode up to 18 MHz ($V_{DD}$ = 2.7V ~ 3.6V) |

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| | Configurable bit length of a transfer word from 4 to 32-bit |
| | MSB first or LSB first transfer sequence |
| | Byte reorder function |
| | Supports Byte or Word Suspend mode |
| | Supports one data channel half-duplex transfer |
| | Supports receive-only mode |
| | **I²S** |
| | Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes |
| | Supports PCM mode A, PCM mode B, I2S and MSB justified data format |
| | PDMA operation |
| **Universal Serial Control Interface (USCI)** | Up to 2 sets of USCI: USCI0 and USCI1 |
| | Supports UART, SPI and I²C function |
| | Single byte TX and RX buffer mode |
| | **USCI_UART** |
| | One transmit buffer and two receive buffer for data payload |
| | Hardware auto flow control function and programmable flow control trigger level |
| | Programmable baud-rate generator |
| | Supports 9-bit data transfer |
| | Baud rate detection by built-in capture event of baud rate generator |
| | Supports Wake-up function (Data and nCTS Wakeup Only) |
| | Supports PDMA transfer |
| | **USCI_SPI** |
| | Master or Slave mode operation |
| | Configurable bit length of a transfer word from 4 to 16-bit |
| | One transmit buffer and two receive buffer for data payload |
| | MSB first or LSB first transfer sequence |
| | Word suspend function |
| | Supports PDMA transfer |
| | Supports 3-wire, no slave select signal, bi-direction interface |
| | Wake-up function: input slave select transition |
| | Supports one data channel half-duplex transfer |
| | **USCI_I2C** |
| | Full master and slave device capability |
| | 7-bit/10-bit addressing mode |
| | Communication in Standard mode (100 kbps), Fast mode (up to 400 |

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| | kbps) and Fast mode plus (1 Mbps)<br>Multi-master bus<br>One transmit buffer and two receive buffer for data payload<br>10-bit bus time out capability<br>Supports Bus monitor mode<br>Wake-up by data toggle or address match in Power-down mode<br>Multiple address recognition<br>Setup/hold time programmable |
| **External Bus Interface (EBI)** | Supports up to three memory banks<br>Supports dedicated external chip select pin with polarity control for each bank<br>Accessible space up to 1 Mbytes for each bank<br>Byte write in 16-bit data width mode<br>Address/Data multiplexed and separate mode<br>Timing parameters individual adjustment for each memory block<br>Supports LCD interface i80 mode<br>Supports Continuous Data Access mode<br>Supports PDMA mode |
| **Controller Area Network with Feasibility Data Rate (CAN FD)** | Up to four sets of CAN FD controllers<br>Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015<br>Compliant with CAN FD version 1.0 with up to 64 data bytes supported<br>Supports CAN Error logging, AUTOSAR and SAE J1938<br>Built-in 1.5K word (32-bit) Message SRAM for each CAN FD controller |
| **GPIO** | Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode<br>Selectable TTL/Schmitt trigger input<br>Configured as interrupt source with edge/level trigger setting<br>Supports independent pull-up/pull-down control<br>Supports software selectable slew rate control<br>Supports 5V-tolerance function except analog I/O<br>Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode |
| ***Control Interfaces*** | |
| **Enhanced Quadrature Encoder Interface (EQEI)** | • Two EQEI phase inputs (EQEI_A, EQEI_B) and one Index input (EQEI_INDEX)<br>• Supports 2/4 times free-counting mode and 2/4 compare-counting |

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| | mode<br>• Supports encoder pulse width measurement mode with ECAP<br>• Supports swap function for input signals (EQEI_A, EQEI_B)<br>• Supports for detecting the occurrence of phase error<br>• Supports one times index signal reset function |
| **Enhanced Capture (ECAP)** | • Up to four sets of Enhanced input Capture units<br>• Supports three input channels with independent capture counter hold register<br>• 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter<br>• Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports<br>• Supports compare-match function |
| ***Advanced Connectivity*** | |
| **USB 2.0 Full Speed with on-chip transceiver** | USB 2.0 Full Speed OTG (On-The-Go)<br>• On-chip USB 2.0 full speed OTG transceiver<br>• Compliant with USB OTG Supplement 2.0<br>• Configurable as host-only, device-only, ID-dependent or OTG device<br>**USB 2.0 Full Speed Host Controller**<br>• Compliant with USB Revision 1.1 Specification<br>• Compatible with OHCI (Open Host Controller Interface) Revision 1.0<br>• Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices<br>• Supports Control, Bulk, Interrupt, Isochronous and Split transfers<br>• Integrated a port routing logic to route full/low speed device to OHCI controller<br>• Supports an integrated Root Hub<br>• Supports port power control and port overcurrent detection<br>• Built-in DMA<br>**USB 2.0 Full Speed Device Controller**<br>• Compliant with USB Revision 2.0 Specification<br>• Supports suspend function when no bus activity exists for 3 ms<br>• 25 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types<br>• 1.5 Kbytes configurable RAM for endpoint buffer<br>• Remote wake-up capability<br>• Start of Frame (SOF) locked clock pulse generation for crystal-less feature<br>• Supports double buffer function |

# 3 PARTS INFORMATION

## 3.1 M2L31 Series Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

| Part No. | WLCSP25 (2.5x2.5mm) | WLCSP49 (3x3mm) | QFN33 (5x5mm) | QFN48 (5x5mm) | LQFP48 (7x7mm) | LQFP64 (7x7mm) | LQFP128 (14x14mm) |
|---|---|---|---|---|---|---|---|
| **M2L31** | M2L31XD4AE | M2L31CIDAE<br>M2L31CGDAE | M2L31ZE4AE<br>M2L31ZD4AE | M2L31YIDAE<br>M2L31YGDAE<br>M2L31YG4AE<br>M2L31YE4AE<br>M2L31YD4AE | M2L31LIDAE<br>M2L31LGDAE<br>M2L31LG4AE<br>M2L31LE4AE<br>M2L31LD4AE | M2L31SIDAE<br>M2L31SGDAE<br>M2L31SG4AE<br>M2L31SE4AE | M2L31KIDAE<br>M2L31KGDAE |

## 3.2 M2L31 Series Naming Rule

| M2 | L31 | K | I | D | A | E |
|---|---|---|---|---|---|---|
| **Core** | **Line** | **Package** | **ReRAM** | **SRAM** | **Reserve** | **Temperature** |
| Cortex-M23 | L31: Low Power line | K: LQFP128 (14x14 mm)<br>S: LQFP64 (7x7 mm)<br>L: LQFP48 (7x7 mm)<br>Y: QFN48 (5x5 mm)<br>Z: QFN33 (5x5 mm)<br>C: WLCSP49<br>X: WLCSP25 | D: 64 KB<br>E: 128 KB<br>G: 256 KB<br>I: 512 KB | 4: 40 KB<br>D: 168 KB | A | E:-40°C ~ 105°C |

## 3.3 M2L31 Series Selection Guide

| PART NO. | M2L31XD4AE | M2L31ZD4AE | M2L31ZE4AE | M2L31YD4AE | M2L31YE4AE | M2L31YG4AE | M2L31YGDAE | M2L31YIDAE | M2L31LD4AE | M2L31LE4AE | M2L31LG4AE | M2L31LGDAE | M2L31LIDAE | M2L31CIDAE | M2L31CGDAE | M2L31SE4AE | M2L31SG4AE | M2L31SGDAE | M2L31SIDAE | M2L31KGDAE | M2L31KIDAE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ReRAM (KB) | 64 | 64 | 128 | 64 | 128 | 256 | 256 | 512 | 64 | 128 | 256 | 256 | 512 | 512 | 256 | 128 | 256 | 256 | 512 | 256 | 512 |
| SRAM (KB) | 40 | 40 | 40 | 40 | 40 | 40 | 168 | 168 | 40 | 40 | 40 | 168 | 168 | 168 | 168 | 40 | 40 | 168 | 168 | 168 | 168 |
| Low Power SRAM (KB) | 4 | 4 | 4 | 4 | 4 | 4 | 8 | 8 | 4 | 4 | 4 | 8 | 8 | 8 | 8 | 4 | 4 | 8 | 8 | 8 | 8 |
| LDROM (KB) | 8 | | | | | | | | | | | | | | | | | | | | |
| 32-bit Timer 16-bit PWM | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 | 4 |
| WDT/WWDT | √ | | | | | | | | | | | | | | | | | | | | |
| LXT | √ | | | | | | | | | | | | | | | | | | | | |
| RTC | √ | | | | | | | | | | | | | | | | | | | | |
| 16-bit EPWM | 12 | | | | | | | | | | | | | | | | | | | | |
| 16-bit PWM | - | - | - | - | - | - | 12 | 12 | - | - | - | 12 | 12 | 12 | 12 | - | - | 12 | 12 | 12 | 12 |
| Connectivity USCI* | - | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 |
| Connectivity UART | 5 | 6 | 6 | 6 | 6 | 6 | 8 | 8 | 6 | 6 | 6 | 8 | 8 | 8 | 8 | 6 | 6 | 8 | 8 | 8 | 8 |
| Connectivity QSPI | - | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| Connectivity SPI/I²S | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 2 | 2 | 2 | 4 | 4 | 4 | 4 | 2 | 2 | 4 | 4 | 4 | 4 |
| Connectivity I²C | 2 | 2 | 2 | 2 | 2 | 2 | 4 | 4 | 2 | 2 | 2 | 4 | 4 | 4 | 4 | 2 | 2 | 4 | 4 | 4 | 4 |
| Connectivity CAN FD | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 |
| Connectivity USB-C PD | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| Connectivity VAI | - | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| USB 2.0 FS OTG | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ | √ |
| LCD Parallel Data (External Bus Interface) | - | - | - | - | - | - | √ | √ | - | - | - | √ | √ | √ | √ | - | - | √ | √ | √ | √ |
| PDMA | 10 | 10 | 10 | 10 | 10 | 10 | 16 | 16 | 10 | 10 | 10 | 16 | 16 | 16 | 16 | 10 | 10 | 16 | 16 | 16 | 16 |
| EQEI | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| ECAP | 1 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 | 2 |
| CRC | √ | | | | | | | | | | | | | | | | | | | | |
| Crypto | AES-256 | | | | | | | | | | | | | | | | | | | | |
| TRNG | - | - | - | - | - | - | √ | √ | - | - | - | √ | √ | √ | √ | - | - | √ | √ | √ | √ |
| PRNG | - | - | - | - | - | - | √ | √ | - | - | - | √ | √ | √ | √ | - | - | √ | √ | √ | √ |
| PLL(MHz) | √ | | | | | | | | | | | | | | | | | | | | |
| ISO-60730 | √ | | | | | | | | | | | | | | | | | | | | |
| Touchkey (ch) | - | - | - | - | - | - | 11 | 11 | - | - | - | 11 | 11 | 11 | 11 | - | - | 16 | 16 | 17 | 17 |
| ACMP | 2 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 | 3 |
| OP Amplifier | - | 2 | 2 | 2 | 2 | 2 | 3 | 3 | 2 | 2 | 2 | 3 | 3 | 3 | 3 | 2 | 2 | 3 | 3 | 3 | 3 |
| 12-bit 1MSPS DAC | 1 | 1 | 1 | 1 | 1 | 1 | 2 | 2 | 1 | 1 | 1 | 2 | 2 | 2 | 2 | 1 | 1 | 2 | 2 | 2 | 2 |
| 12-bit ADC | 6 | 10 | | 16 | | | | | 16 | | | | | 16 | | 20 | | | | 24 | |
| GPIO | 18 | 26 | | 41 | | | | | 41 | | | | | 40 | | 53 | | | | 109 | |
| Package | WLCSP25 | QFN32 | | QFN48 | | | | | LQFP48 | | | | | WLCSP49 | | LQFP64 | | | | LQFP 128 | |

USCI*: supports UART, SPI or I²C

## 3.4 M2L31xxDAE/M2L31xx4AE Features Comparison Table

| Section | Sub-section | M2L31xxDAE | M2L31xx4AE |
|---|---|---|---|
| **RMC Features** | Dual-bank RRAM macro | ● | |

# 4 PIN CONFIGURATION

## 4.1 Pin Configuration

Users can find pin configuration information in the Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

## 4.2 M2L31 Series Pin Diagram

### 4.2.1 QFN33-Pin Diagram

Corresponding Part Number: M2L31ZE4AE, M2L31ZD4AE

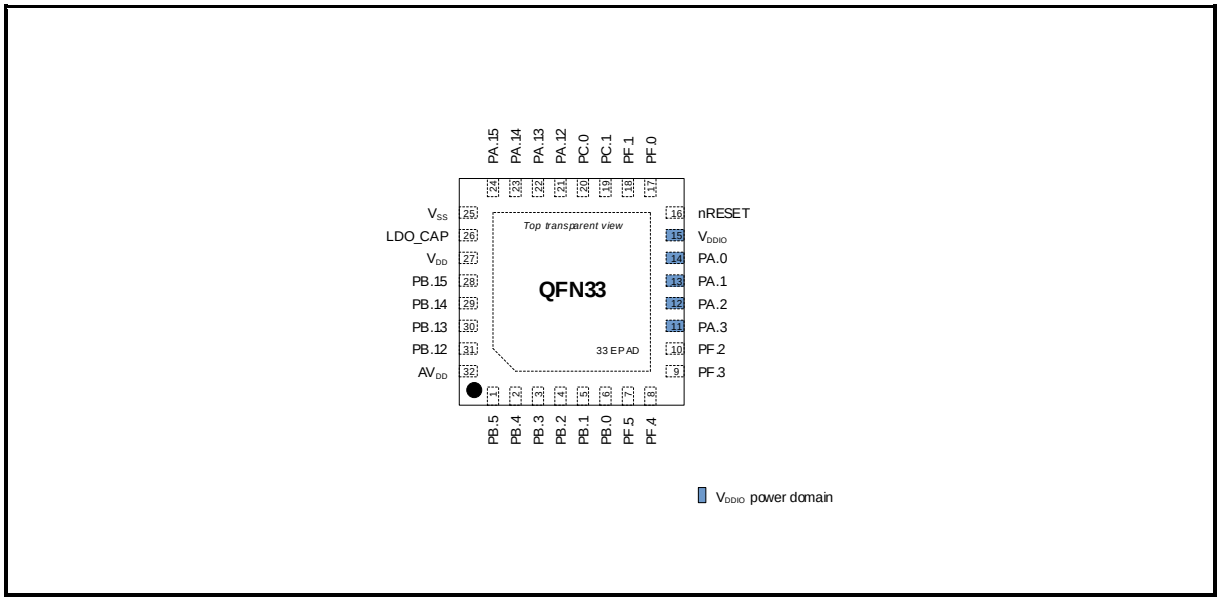



Figure 6.2-1 QFN33-Pin Diagram

### 4.2.2 QFN48-Pin Diagram

Corresponding Part Number: M2L31YG4AE, M2L31YE4AE, M2L31YD4AE, M2L31YIDAE, M2L31YGDAE

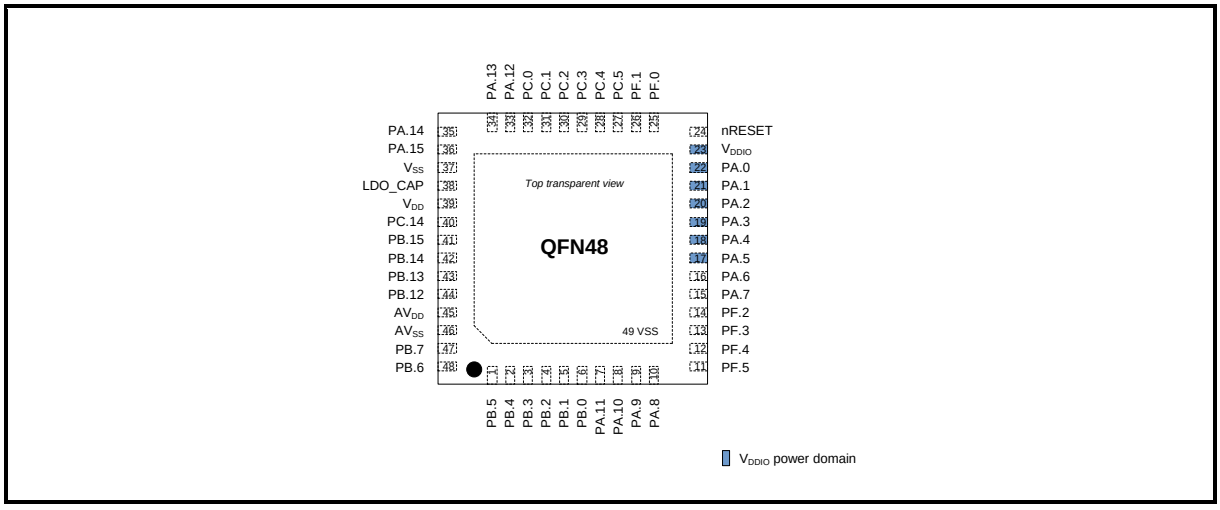



Figure 6.2-2 QFN48-Pin Diagram

### 4.2.3 LQFP48-Pin Diagram

Corresponding Part Number: M2L31LE4AE, M2L31LG4AE, M2L31LD4AE, M2L31LIDAE, M2L31LGDAE

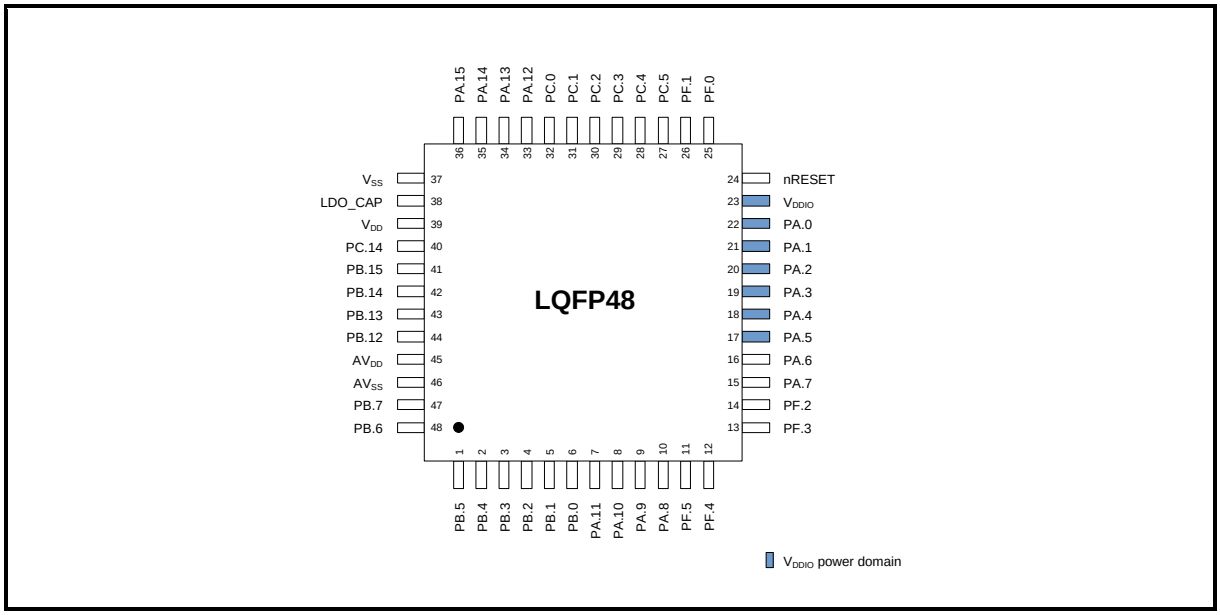



Figure 6.2-3 LQFP48-Pin Diagram

### 4.2.4 LQFP64-Pin Diagram

Corresponding Part Number: M2L31SG4AE, M2L31SE4AE, M2L31SIDAE, M2L31SGDAE

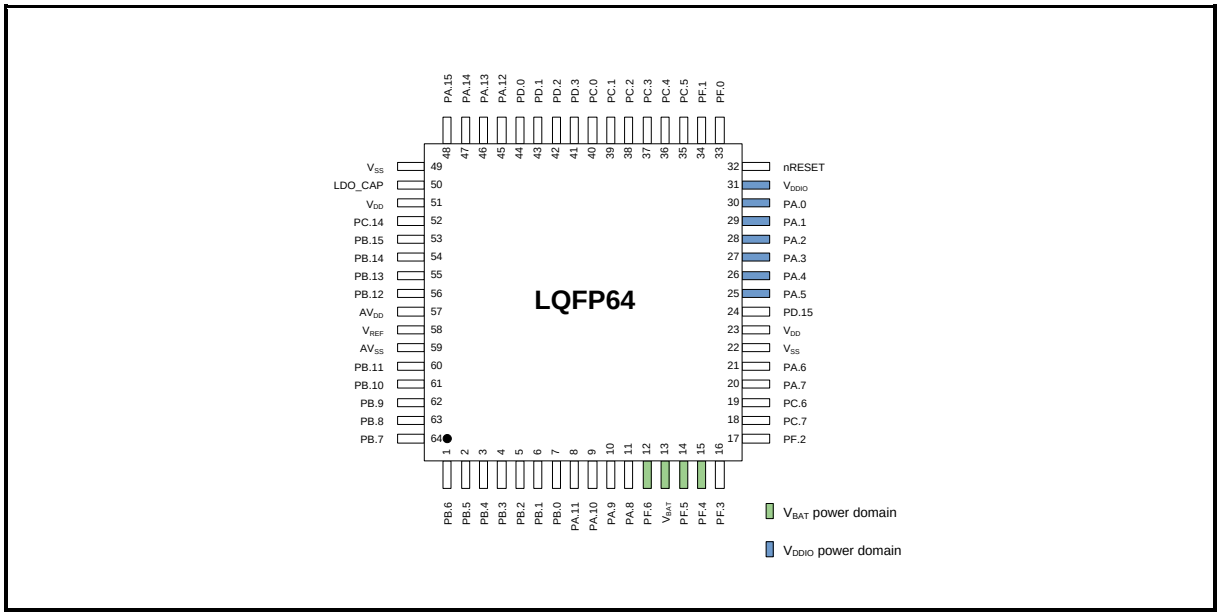



Figure 6.2-4 LQFP64-Pin Diagram

### 4.2.5 LQFP128-Pin Diagram

Corresponding Part Number: M2L31KIDAE, M2L31KGDAE

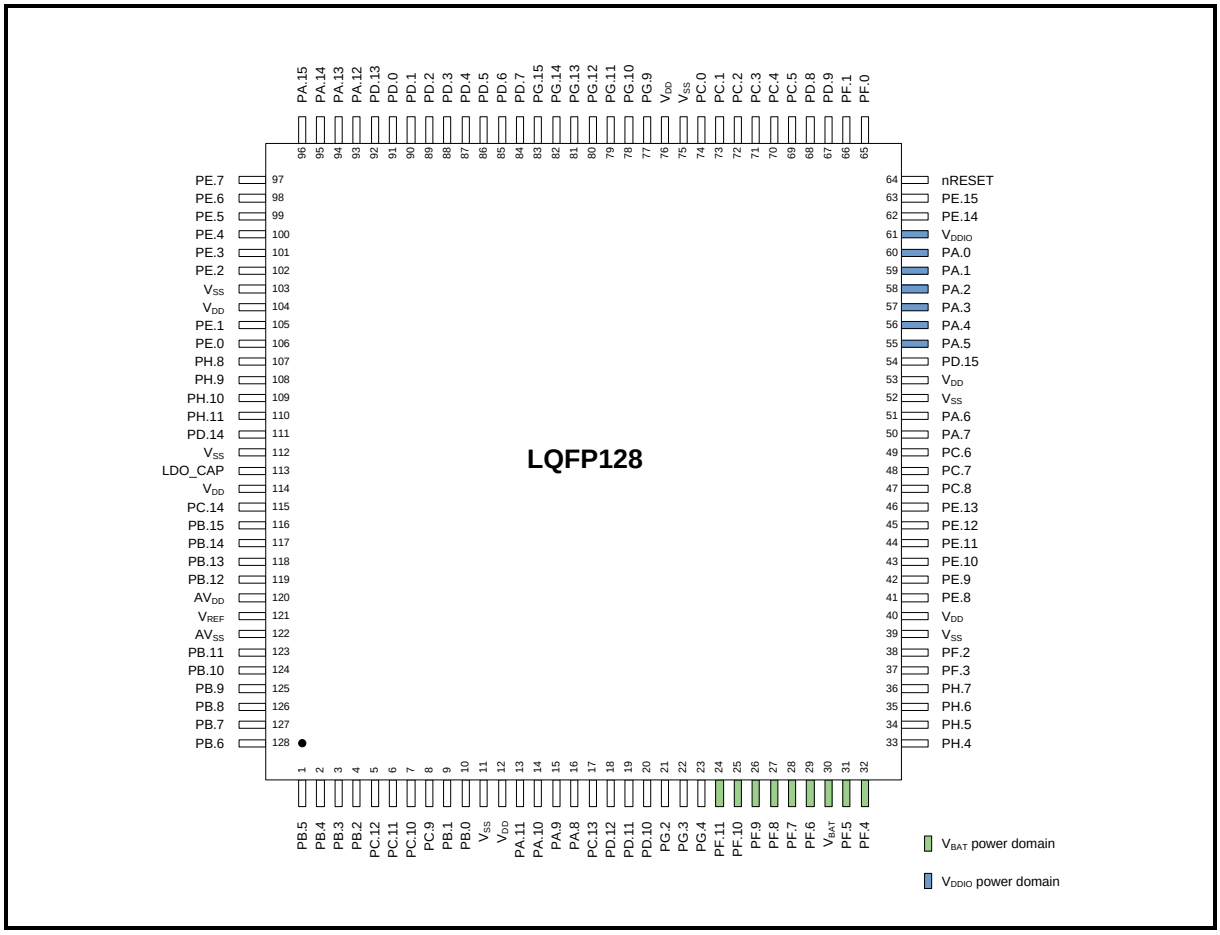



Figure 6.2-5 LQFP128-Pin Diagram

## 4.3 M2L31 Series Multi-function Diagram

### 4.3.1 QFN33-Pin Multi-function Diagram

Corresponding Part Number: M2L31ZE4AE, M2L31ZD4AE

#### *4.3.1.1 M2L31ZE4AE*

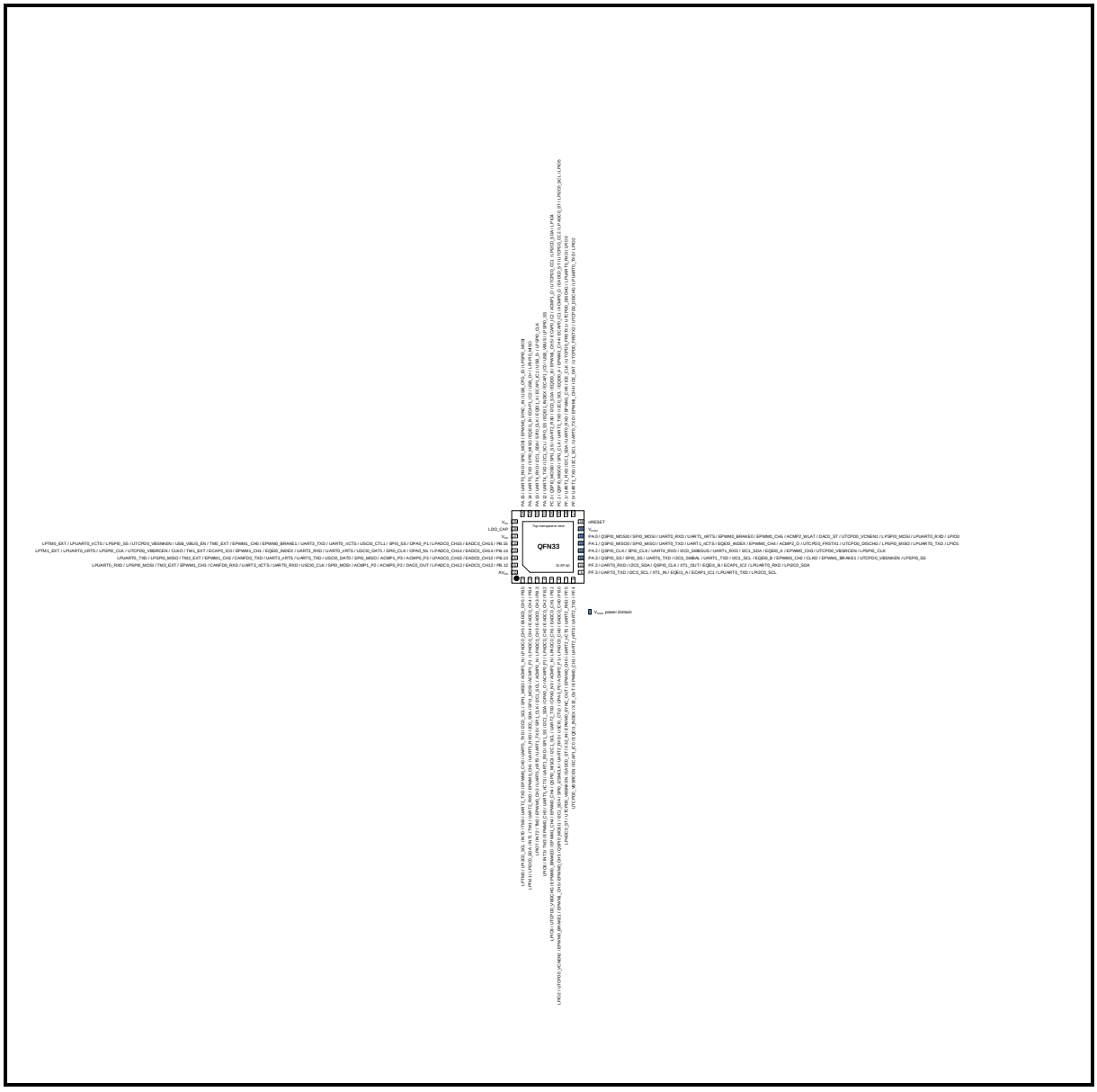



Figure 6.2-6 M2L31ZE4AE Multi-function Pin Diagram

| Pin | Type | M2L31ZE4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |

| Pin | Type | M2L31ZE4AE Pin Function |
|---|---|---|
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 8 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 9 | I/O | PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 10 | I/O | PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 11 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 12 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 13 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 14 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 15 | P | $V_{DDIO}$ |
| 16 | I | nRESET |
| 17 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 18 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 19 | I/O | PC.1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPADC0_ST / LPI2C0_SCL / LPIO5 |
| 20 | I/O | PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 21 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 22 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 23 | I/O | PA.14 / UART0_TXD / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 24 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 25 | P | $V_{SS}$ |
| 26 | A | LDO_CAP |
| 27 | P | $V_{DD}$ |
| 28 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / |

| Pin | Type | M2L31ZE4AE Pin Function |
|---|---|---|
| | | UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 29 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 30 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 31 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 32 | P | $AV_{DD}$ |
| 33 | P | $V_{SS}$ |

Table 6.2-1 M2L31ZE4AE Multi-function Pin Table

#### 4.3.1.2 M2L31ZD4AE

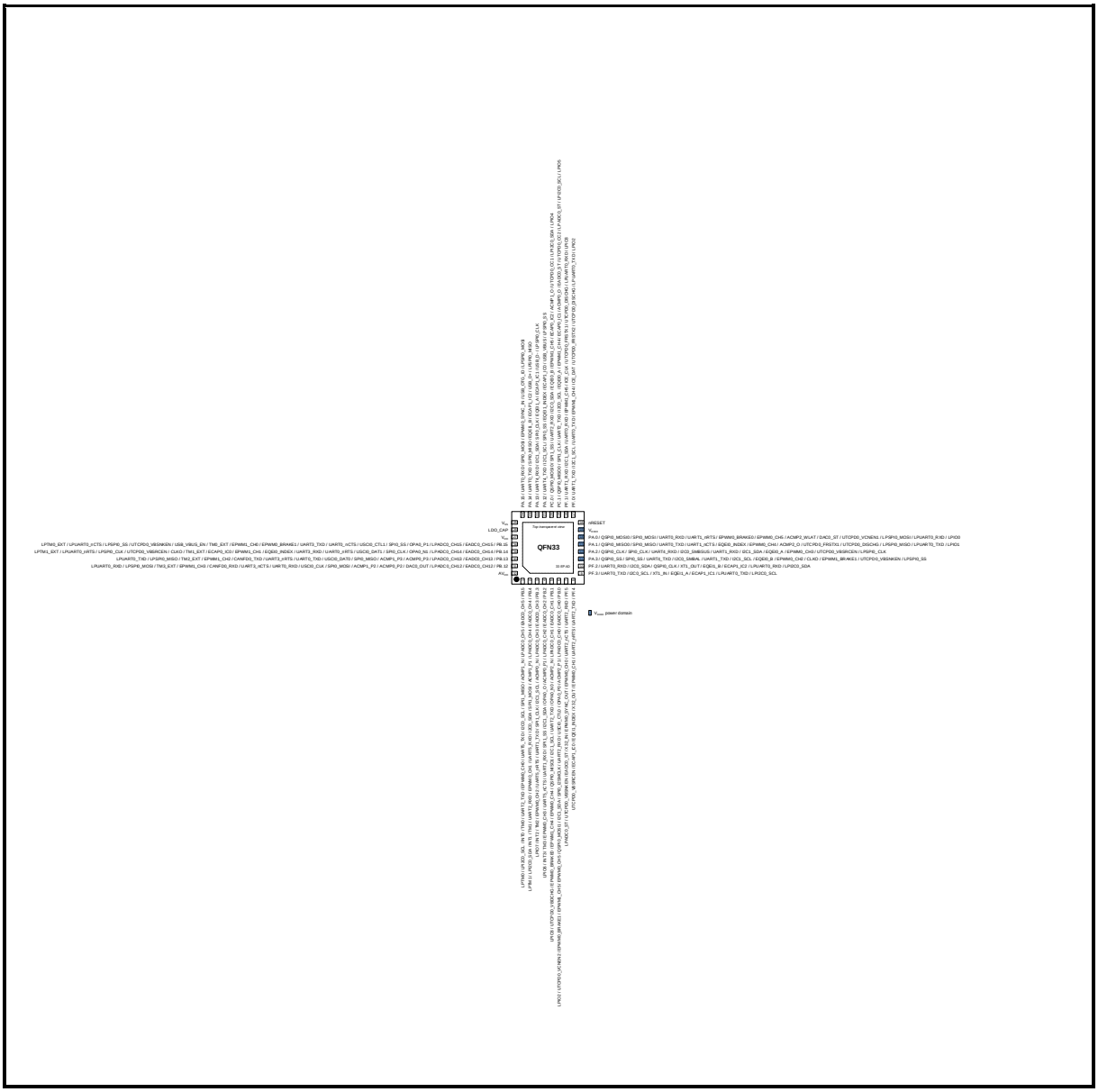



Figure 6.2-7 M2L31ZD4AE Multi-function Pin Diagram

| Pin | Type | M2L31ZD4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |

| Pin | Type | M2L31ZD4AE Pin Function |
|---|---|---|
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 8 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 9 | I/O | PF.3 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 10 | I/O | PF.2 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 11 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 12 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 13 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 14 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 15 | P | $V_{DDIO}$ |
| 16 | I | nRESET |
| 17 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 18 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 19 | I/O | PC.1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPADC0_ST / LPI2C0_SCL / LPIO5 |
| 20 | I/O | PC.0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 21 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 22 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 23 | I/O | PA.14 / UART0_TXD / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 24 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 25 | P | $V_{SS}$ |
| 26 | A | LDO_CAP |
| 27 | P | $V_{DD}$ |
| 28 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 29 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 30 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / |

| Pin | Type | M2L31ZD4AE Pin Function |
|---|---|---|
| | | LPSPI0_MISO / LPUART0_TXD |
| 31 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 32 | P | $AV_{DD}$ |
| 33 | P | $V_{SS}$ |

Table 6.2-2 M2L31ZD4AE Multi-function Pin Table

### 4.3.2 QFN48-Pin Multi-function Diagram

Corresponding Part Number: M2L31YG4AE, M2L31YE4AE, M2L31YD4AE, M2L31YIDAE, M2L31YGDAE

#### *4.3.2.1 M2L31YG4AE*

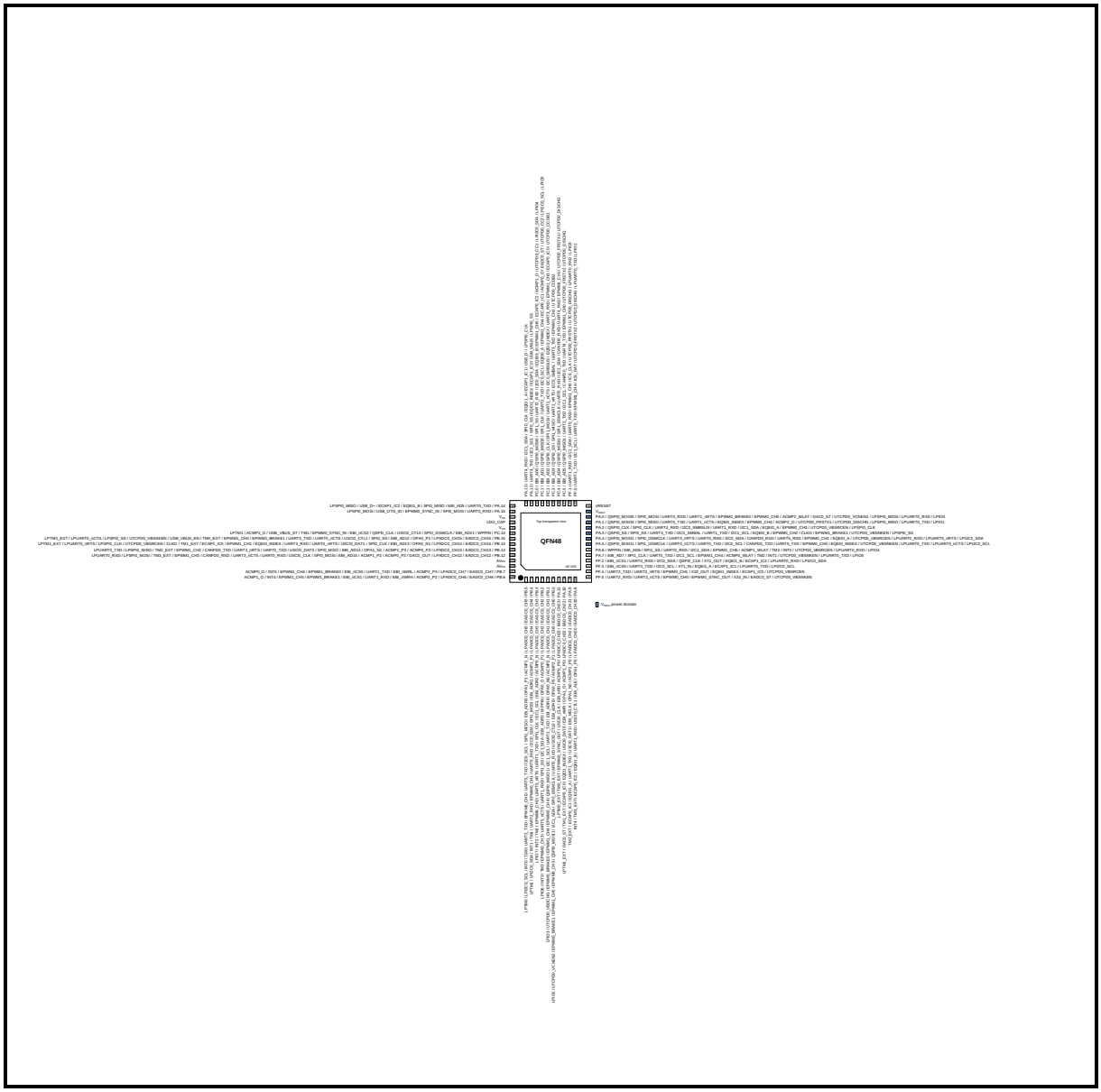



Figure 6.2-8 M2L31YG4AE Multi-function Pin Diagram

| Pin | Type | M2L31YG4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |

| Pin | Type | M2L31YG4AE Pin Function |
|---|---|---|
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |

| Pin | Type | M2L31YG4AE Pin Function |
|---|---|---|
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-3 M2L31YG4AE Multi-function Pin Table

#### 4.3.2.2 M2L31YE4AE

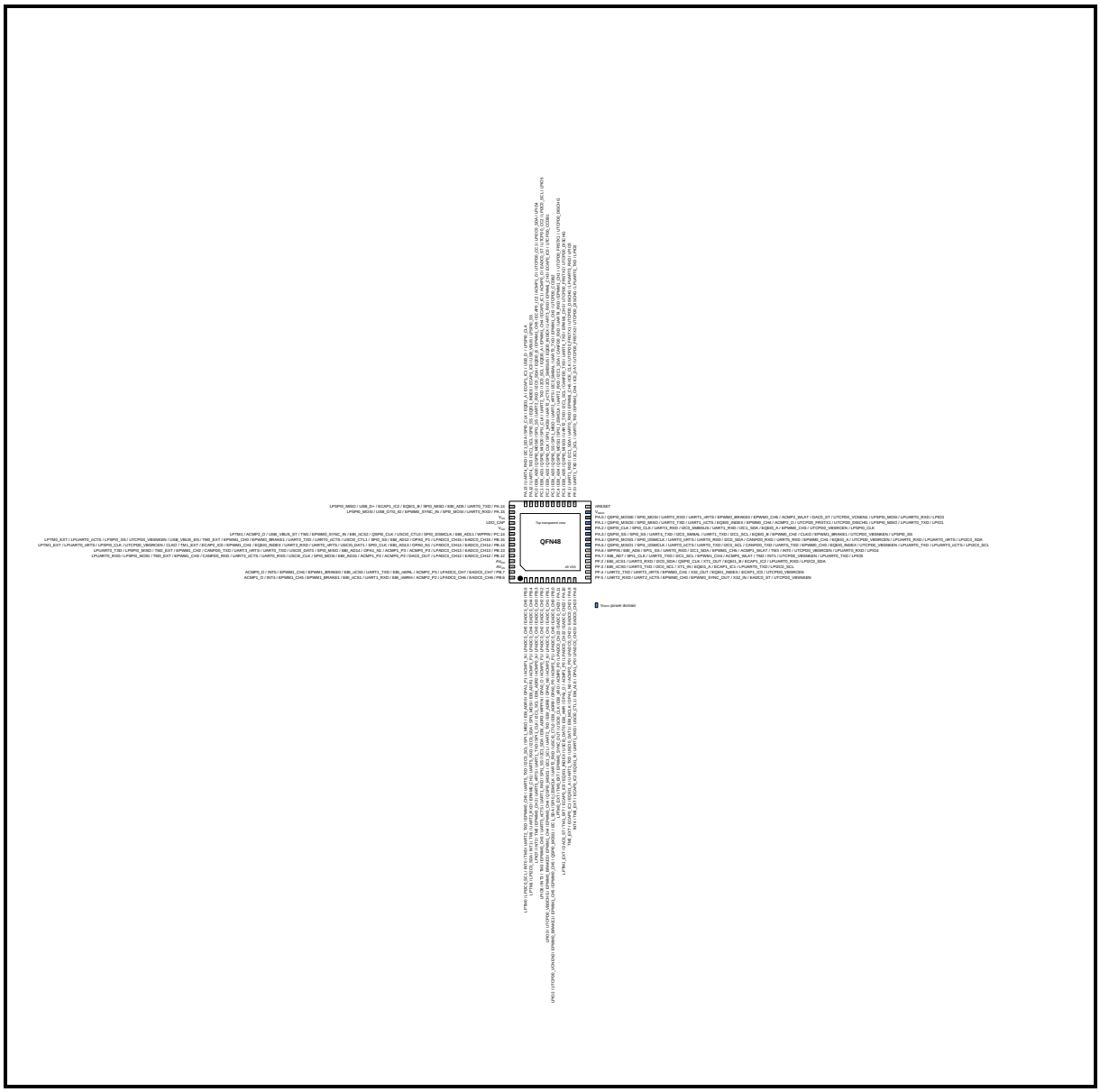



Figure 6.2-9 M2L31YE4AE Multi-function Pin Diagram

| Pin | Type | M2L31YE4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |

| Pin | Type | M2L31YE4AE Pin Function |
|---|---|---|
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |

| Pin | Type | M2L31YE4AE Pin Function |
|---|---|---|
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-4 M2L31YE4AE Multi-function Pin Table

#### 4.3.2.3 M2L31YD4AE

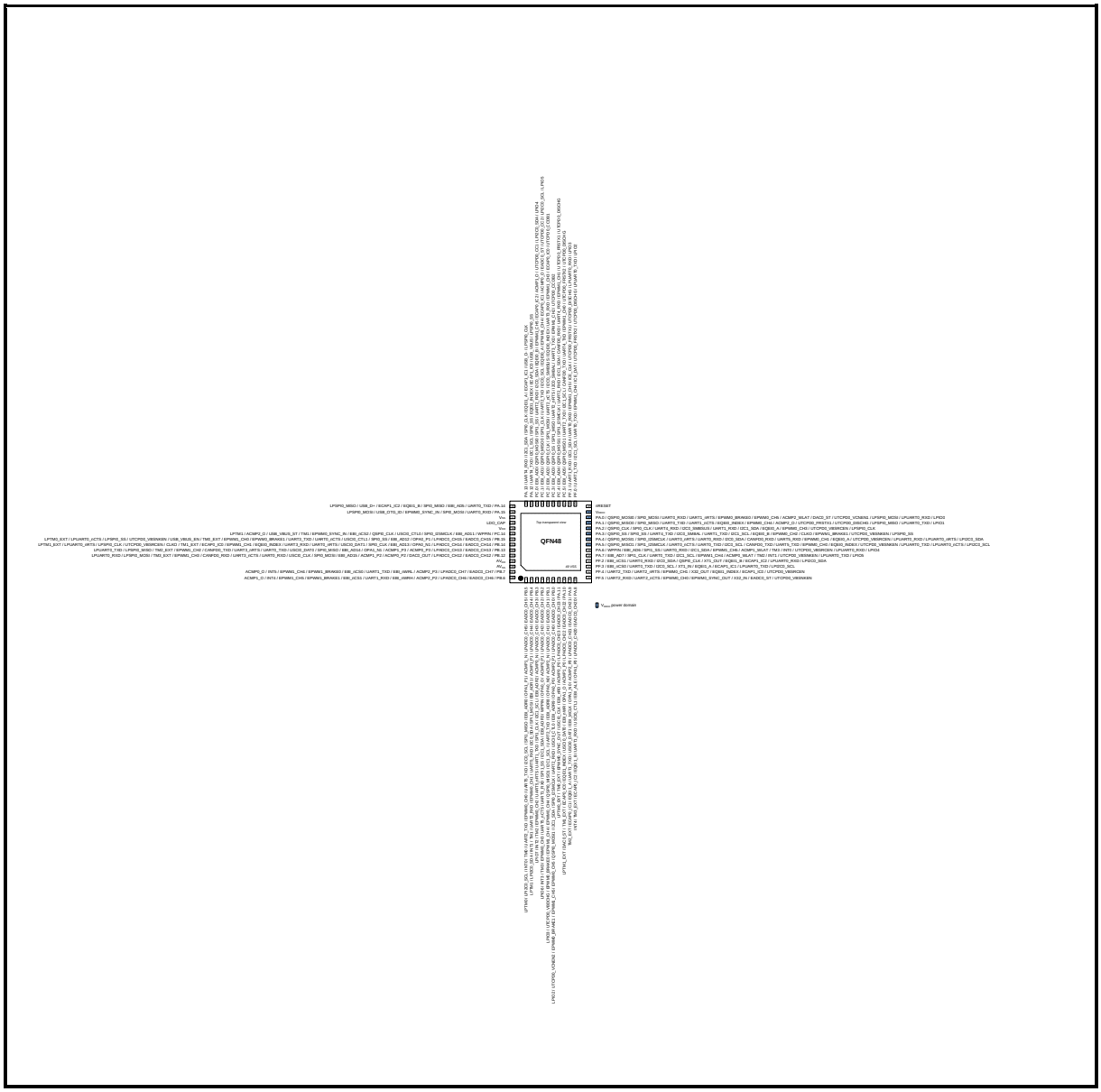



Figure 6.2-10 M2L31YD4AE Multi-function Pin Diagram

| Pin | Type | M2L31YD4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |

| Pin | Type | M2L31YD4AE Pin Function |
|---|---|---|
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |

| Pin | Type | M2L31YD4AE Pin Function |
|---|---|---|
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-5 M2L31YD4AE Multi-function Pin Table

#### 4.3.2.4 M2L31YIDAE

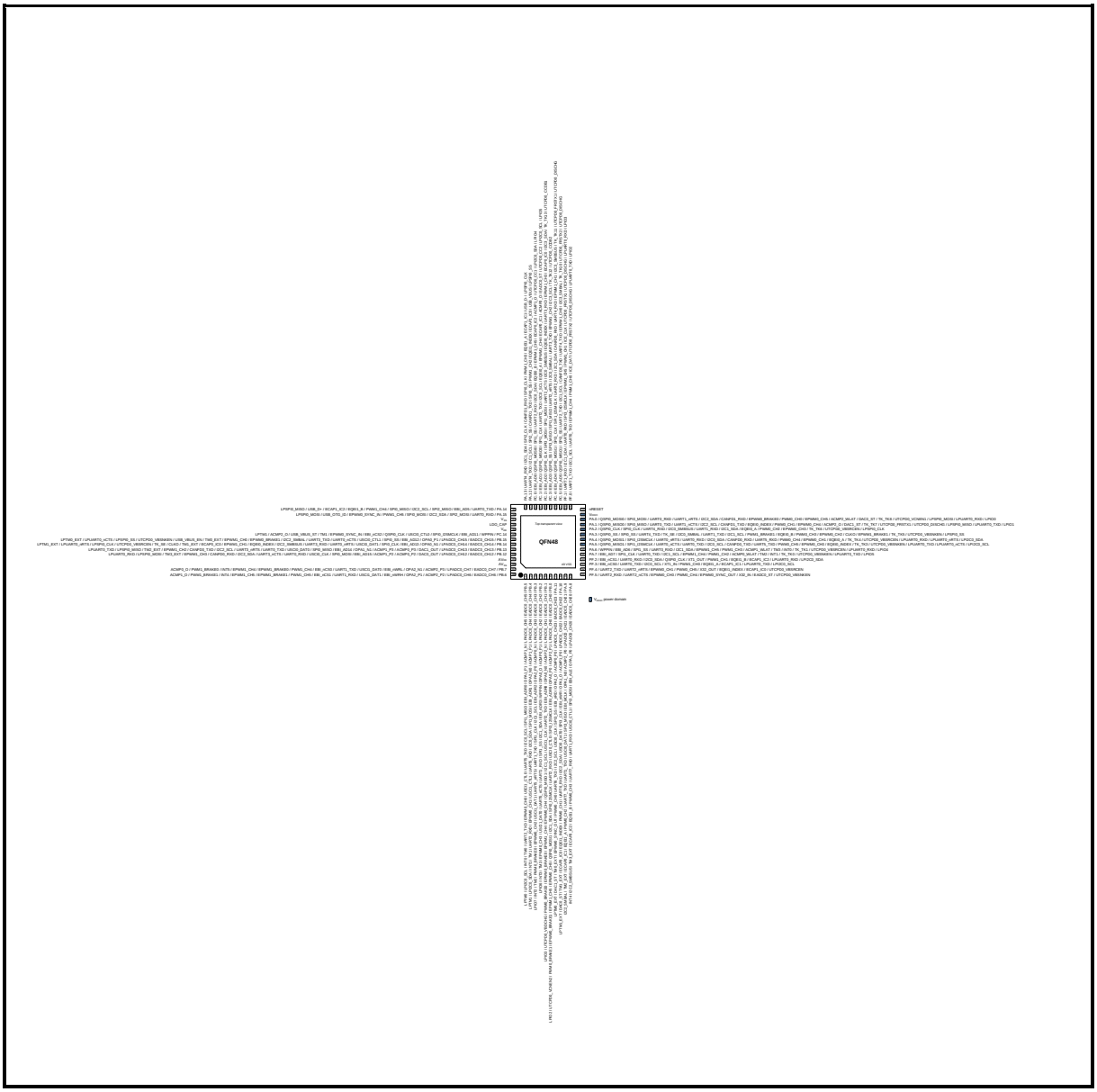



Figure 6.2-11 M2L31YIDAE Multi-function Pin Diagram

| Pin | Type | M2L31YIDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / |

| Pin | Type | M2L31YIDAE Pin Function |
|---|---|---|
| | | UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |

| Pin | Type | M2L31YIDAE Pin Function |
|---|---|---|
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |

| Pin | Type | M2L31YIDAE Pin Function |
|---|---|---|
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-6 M2L31YIDAE Multi-function Pin Table

#### 4.3.2.5 M2L31YGDAE

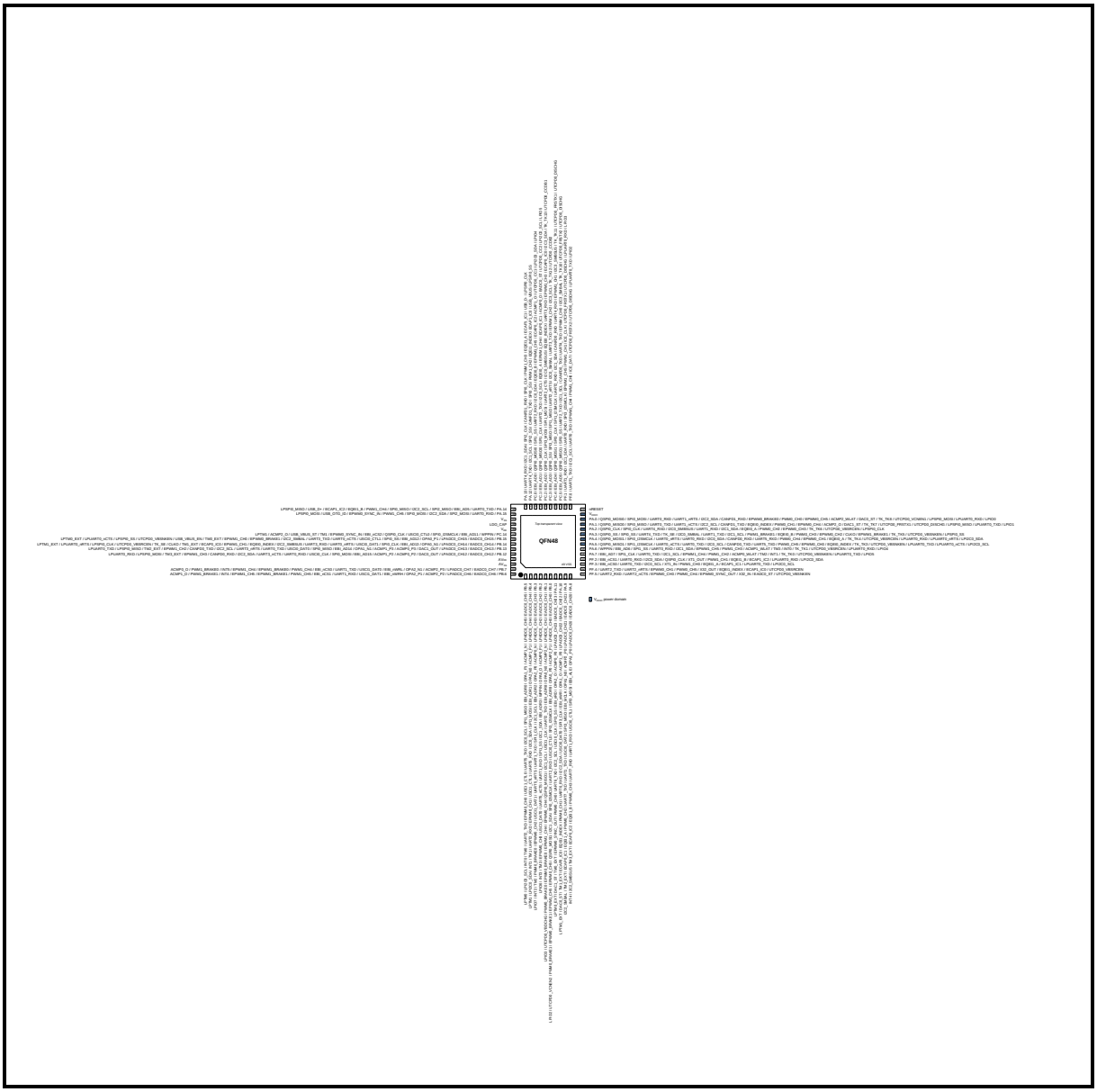



Figure 6.2-12 M2L31YGDAE Multi-function Pin Diagram

| Pin | Type | M2L31YGDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |

| Pin | Type | M2L31YGDAE Pin Function |
|---|---|---|
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |

| Pin | Type | M2L31YGDAE Pin Function |
|---|---|---|
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 |

| Pin | Type | M2L31YGDAE Pin Function |
|---|---|---|
| | | / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-7 M2L31YGDAE Multi-function Pin Table

### 4.3.3 LQFP48-Pin Multi-function Diagram

Corresponding Part Number: M2L31LE4AE, M2L31LG4AE, M2L31LD4AE, M2L31LIDAE, M2L31LGDAE

#### *4.3.3.1 M2L31LE4AE*

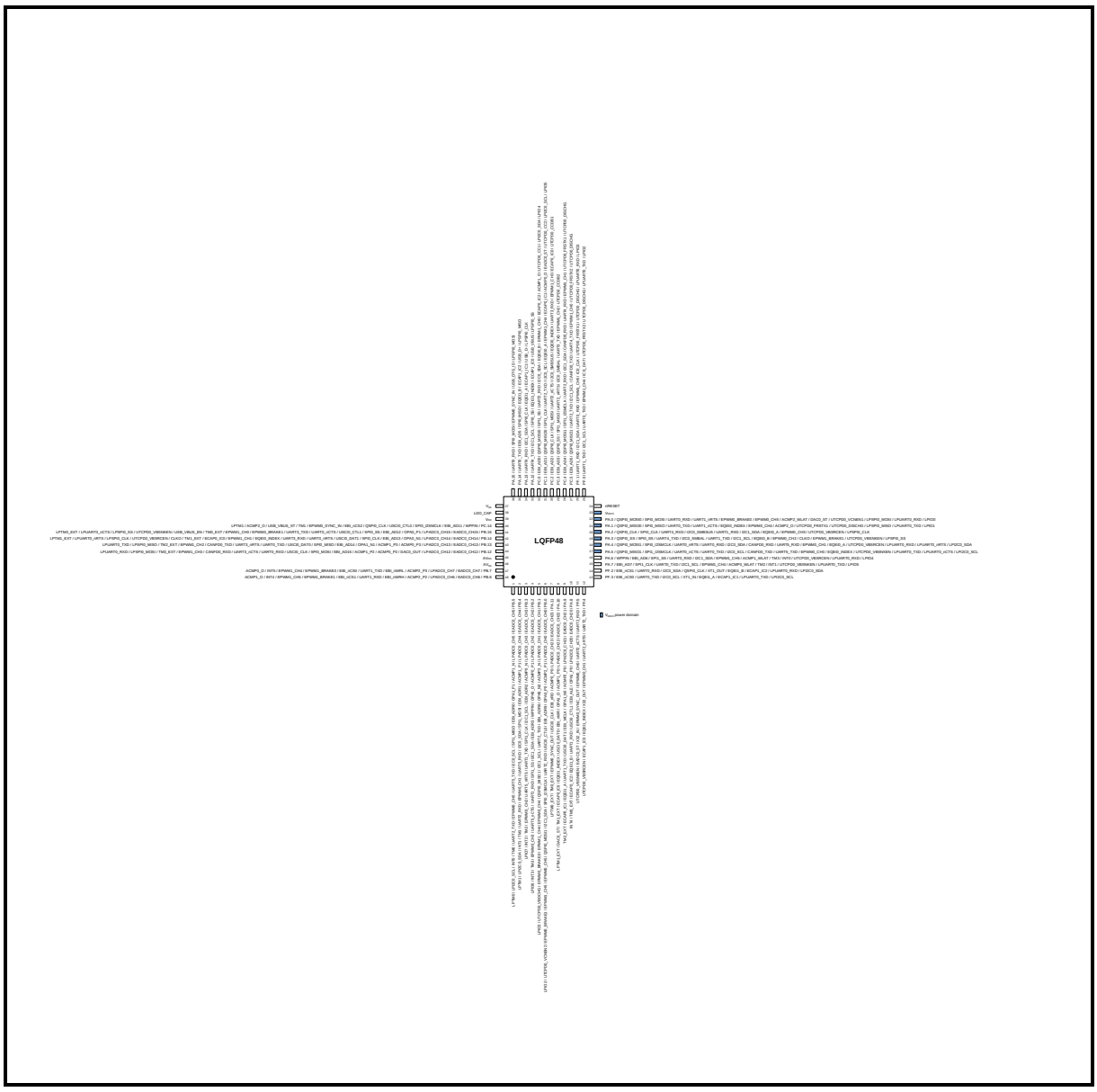



Figure 6.2-13 M2L31LE4AE Multi-function Pin Diagram

| Pin | Type | M2L31LE4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |

| Pin | Type | M2L31LE4AE Pin Function |
|---|---|---|
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |

| Pin | Type | M2L31LE4AE Pin Function |
|---|---|---|
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-8 M2L31LE4AE Multi-function Pin Table

#### 4.3.3.2 M2L31LG4AE

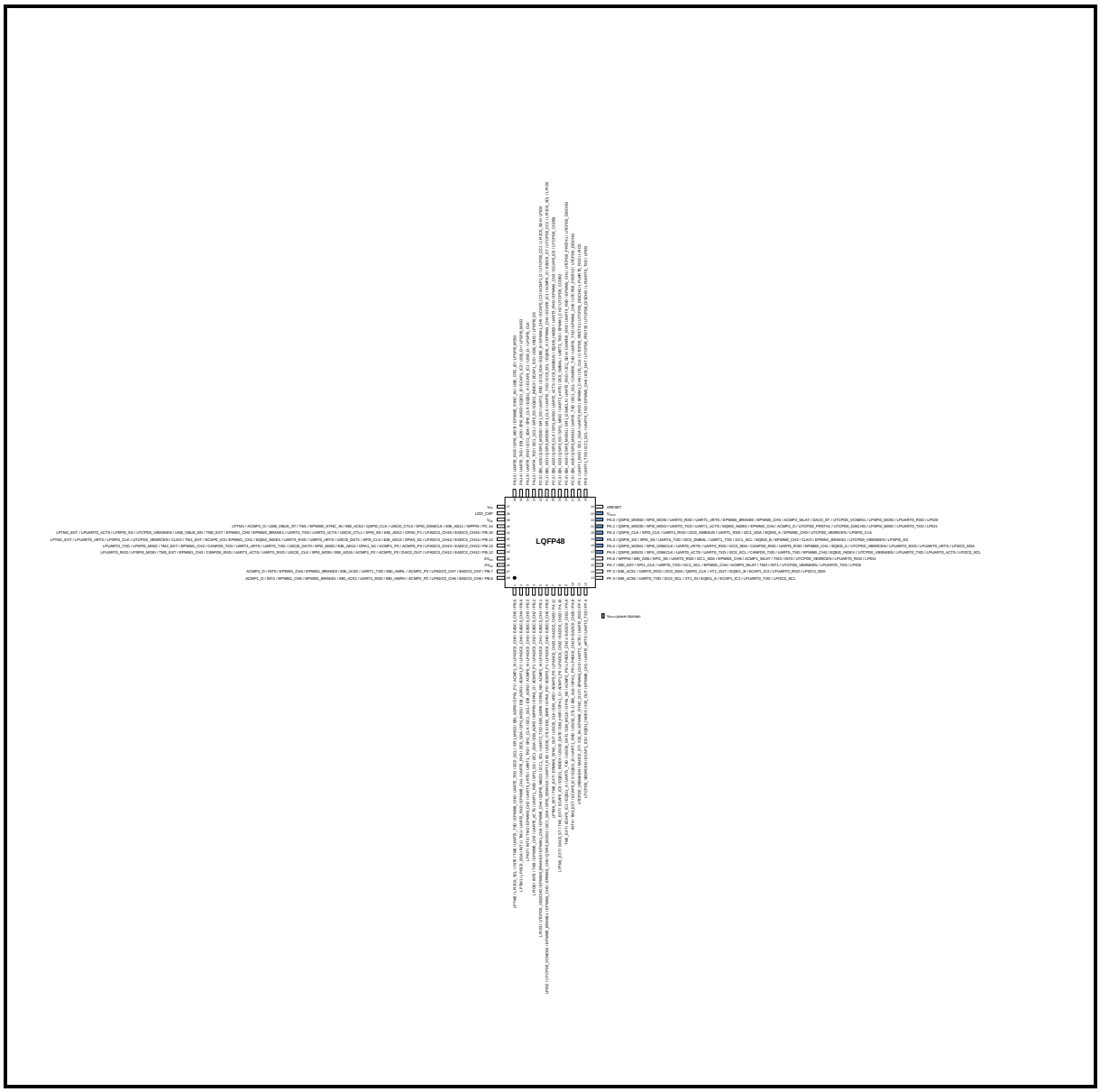



Figure 6.2-14 M2L31LG4AE Multi-function Pin Diagram

| Pin | Type | M2L31LG4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |

| Pin | Type | M2L31LG4AE Pin Function |
|---|---|---|
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |

| Pin | Type | M2L31LG4AE Pin Function |
|---|---|---|
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-9 M2L31LG4AE Multi-function Pin Table

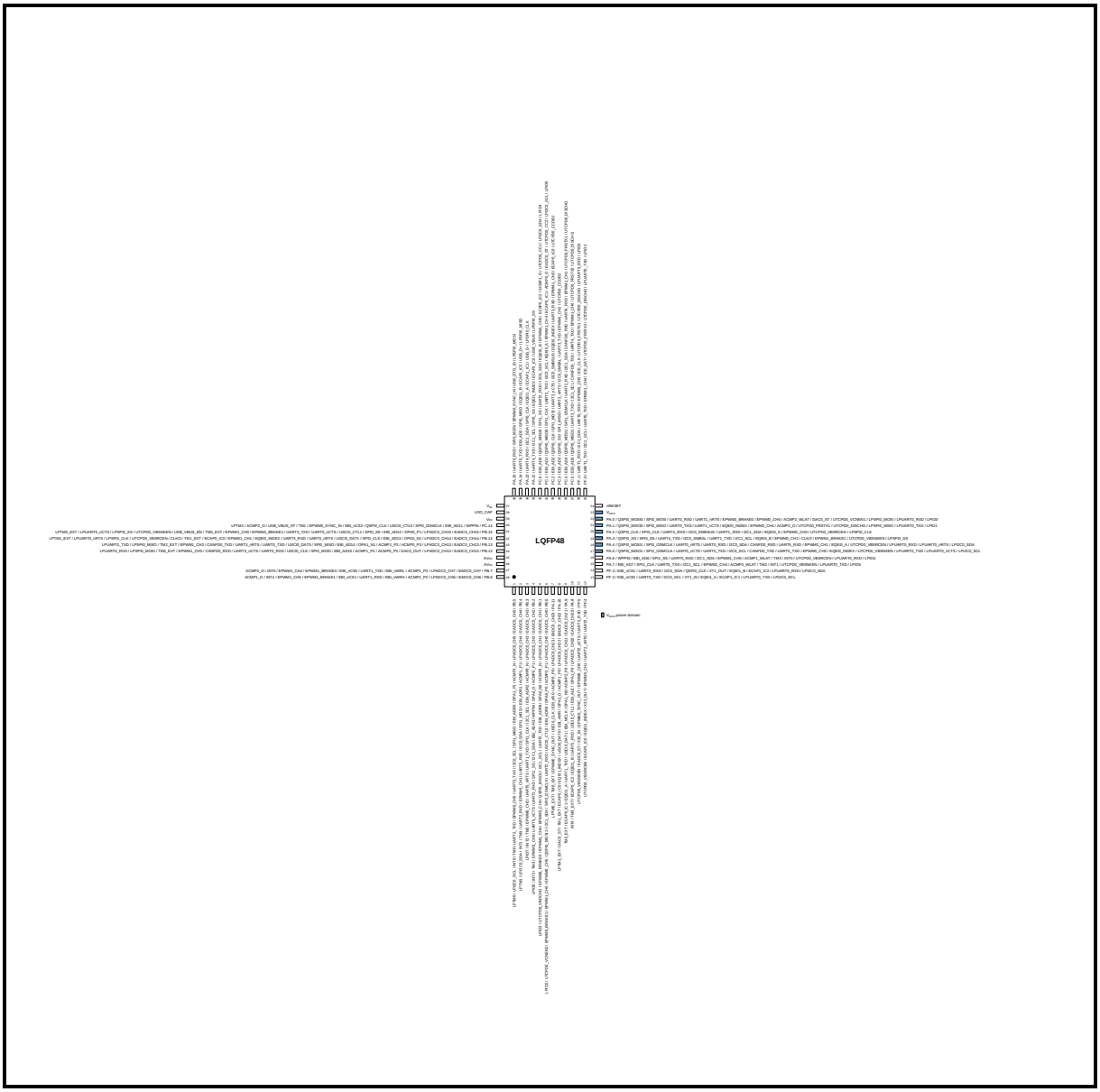



Figure 6.2-15 M2L31LD4AE Multi-function Pin Diagram

| Pin | Type | M2L31LD4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / |

| Pin | Type | M2L31LD4AE Pin Function |
|---|---|---|
| | | UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |

| Pin | Type | M2L31LD4AE Pin Function |
|---|---|---|
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |

Table 6.2-10 M2L31LD4AE Multi-function Pin Table

#### 4.3.3.3 M2L31LIDAE

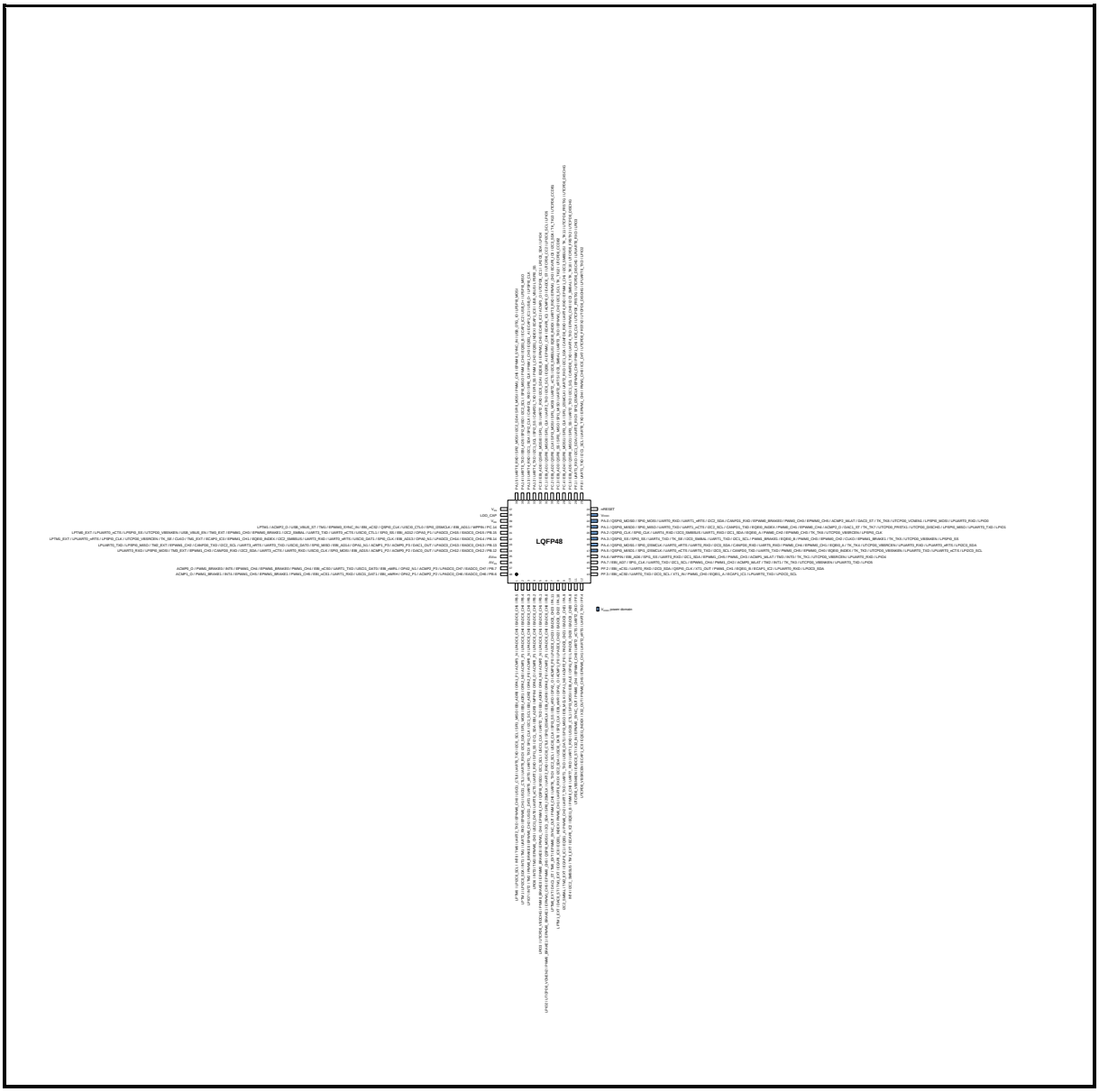



Figure 6.2-16 M2L31LIDAE Multi-function Pin Diagram

| Pin | Type | M2L31LIDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / |

| Pin | Type | M2L31LIDAE Pin Function |
|---|---|---|
| | | UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |

| Pin | Type | M2L31LIDAE Pin Function |
|---|---|---|
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |

| Pin | Type | M2L31LIDAE Pin Function |
|---|---|---|
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-11 M2L31LIDAE Multi-function Pin Table

#### 4.3.3.4 M2L31LGDAE

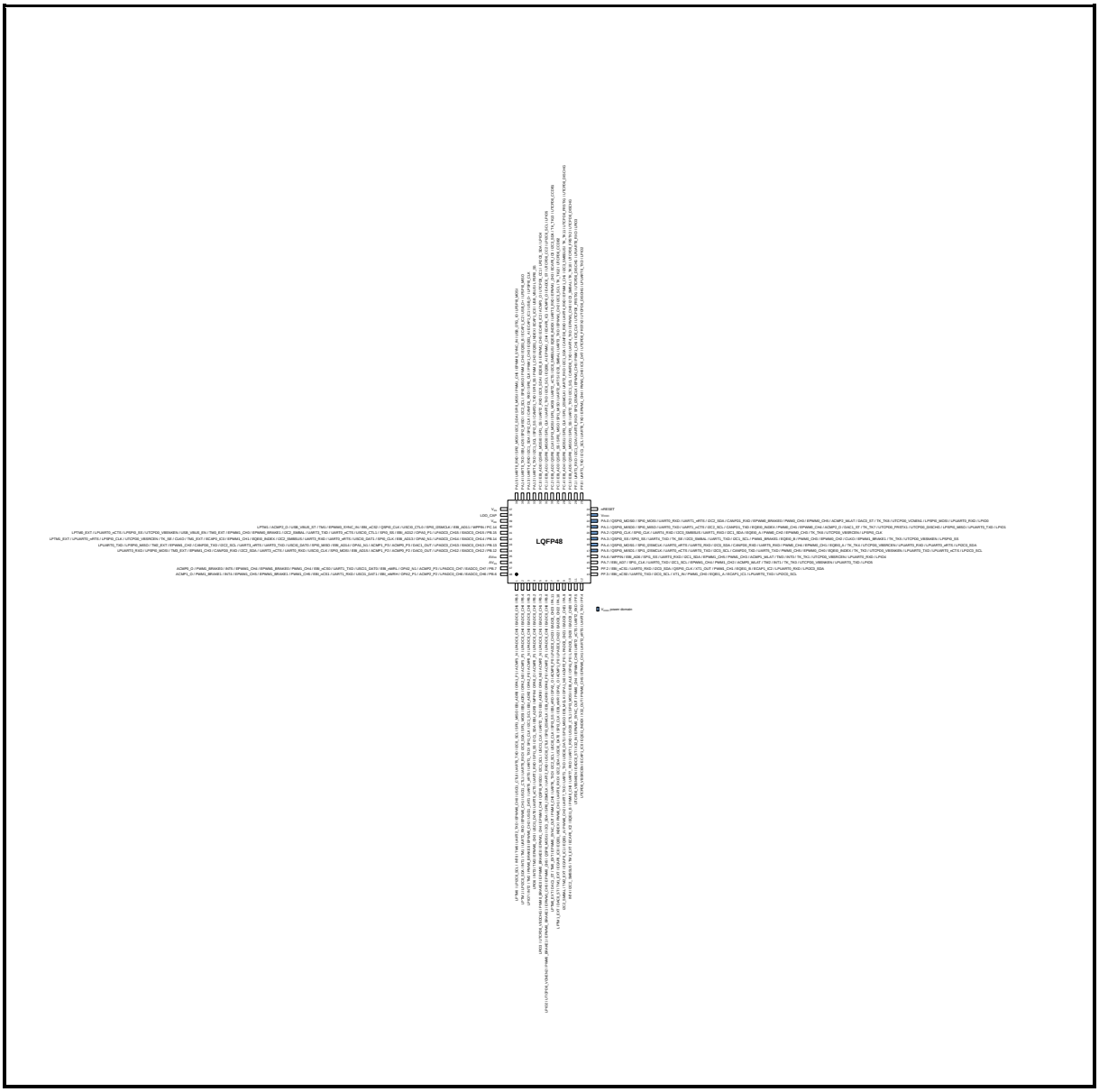



Figure 6.2-17 M2L31LGDAE Multi-function Pin Diagram

| Pin | Type | M2L31LGDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / |

| Pin | Type | M2L31LGDAE Pin Function |
|---|---|---|
| | | UTCPD0_VBDCHG / LPIO3 |
| 6 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 7 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 8 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 9 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 10 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 11 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 12 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 13 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 14 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 15 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 16 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 17 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 18 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 19 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 20 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 21 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 22 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 23 | P | $V_{DDIO}$ |
| 24 | I | nRESET |
| 25 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |

| Pin | Type | M2L31LGDAE Pin Function |
|---|---|---|
| 26 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 27 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 28 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 29 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 30 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 31 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 32 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 33 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 34 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 35 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 36 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 37 | P | $V_{SS}$ |
| 38 | A | LDO_CAP |
| 39 | P | $V_{DD}$ |
| 40 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 41 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 42 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 43 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 44 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 45 | P | $AV_{DD}$ |
| 46 | P | $AV_{SS}$ |
| 47 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |

| Pin | Type | M2L31LGDAE Pin Function |
|---|---|---|
| 48 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-12 M2L31LGDAE Multi-function Pin Table

### 4.3.4 LQFP64-Pin Multi-function Diagram

Corresponding Part Number: M2L31SG4AE, M2L31SE4AE, M2L31SIDAE, M2L31SGDAE

#### *4.3.4.1 M2L31SG4AE*

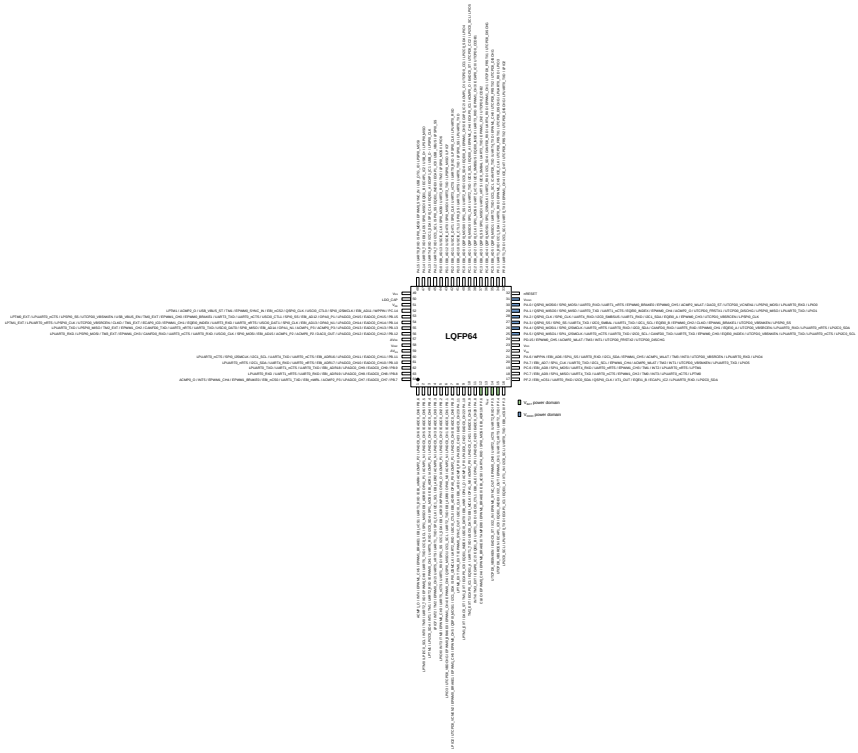



Figure 6.2-18 M2L31SG4AE Multi-function Pin Diagram

| Pin | Type | M2L31SG4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |
| 2 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 3 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |

| Pin | Type | M2L31SG4AE Pin Function |
|---|---|---|
| 4 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |
| 5 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 6 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 7 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 8 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 9 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 10 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 11 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 12 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / CLKO |
| 13 | P | $V_{BAT}$ |
| 14 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 15 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 16 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 17 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 18 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / EPWM1_CH2 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 19 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / EPWM1_CH3 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 20 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 21 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 22 | P | $V_{SS}$ |
| 23 | P | $V_{DD}$ |
| 24 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 25 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 26 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |

| Pin | Type | M2L31SG4AE Pin Function |
|---|---|---|
| 27 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 28 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 29 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 30 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 31 | P | $V_{DDIO}$ |
| 32 | I | nRESET |
| 33 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 34 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 35 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 36 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 37 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 38 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 39 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 40 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 41 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / UART0_TXD / LPSPI0_SS / LPUART0_TXD |
| 42 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / LPSPI0_CLK / LPUART0_RXD |
| 43 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / LPSPI0_MISO / LPIO7 |
| 44 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / LPSPI0_MOSI / LPIO6 |
| 45 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 46 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 47 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 48 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 49 | P | $V_{SS}$ |
| 50 | A | LDO_CAP |
| 51 | P | $V_{DD}$ |
| 52 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 53 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / |

| Pin | Type | M2L31SG4AE Pin Function |
|---|---|---|
| | | UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 54 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 55 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 56 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 57 | P | $AV_{DD}$ |
| 58 | A | $V_{REF}$ |
| 59 | P | $AV_{SS}$ |
| 60 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / SPI0_I2SMCLK / LPUART0_nCTS |
| 61 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / UART0_nRTS / UART4_RXD / I2C1_SDA / LPUART0_nRTS |
| 62 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / UART0_TXD / UART1_nCTS / LPUART0_TXD |
| 63 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / UART0_RXD / UART1_nRTS / LPUART0_RXD |
| 64 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |

Table 6.2-13 M2L31SG4AE Multi-function Pin Table

#### 4.3.4.2 M2L31SE4AE

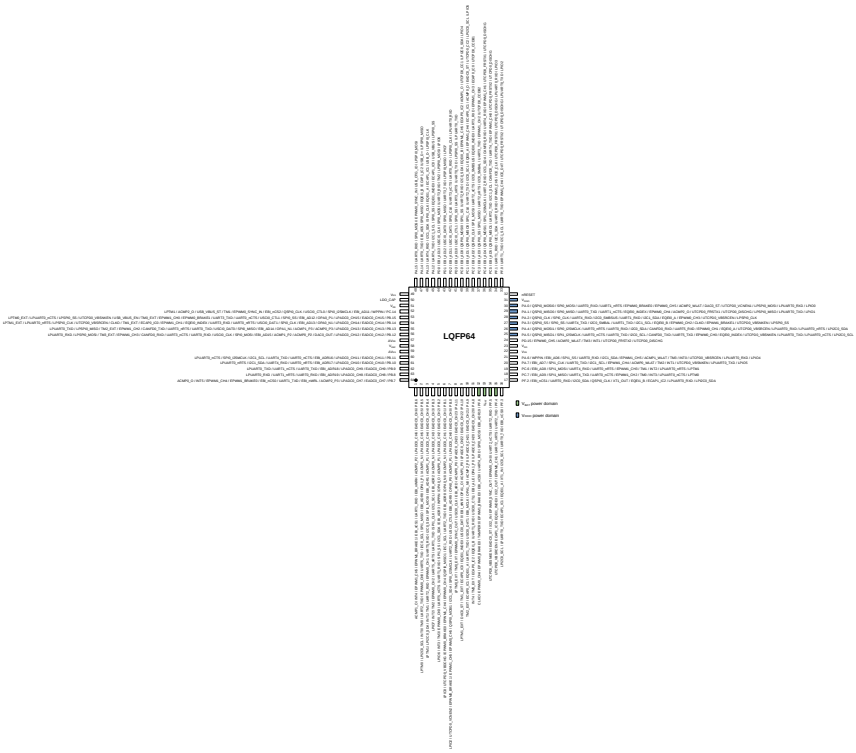



Figure 6.2-19 M2L31SE4AE Multi-function Pin Diagram

| Pin | Type | M2L31SE4AE Pin Function |
|---|---|---|
| 1 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / EBI_nWRH / UART1_RXD / EBI_nCS1 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O |
| 2 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 3 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 4 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / EPWM0_CH2 / TM2 / INT2 / LPIO7 |

| Pin | Type | M2L31SE4AE Pin Function |
|---|---|---|
| 5 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 6 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 7 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 8 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / EBI_nRD / USCI0_CLK / EPWM0_SYNC_OUT / TM0_EXT / LPTM0_EXT |
| 9 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / USCI0_DAT0 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 10 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / USCI0_DAT1 / UART1_TXD / EQEI1_A / ECAP0_IC1 / TM2_EXT |
| 11 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / USCI0_CTL1 / UART1_RXD / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4 |
| 12 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / CLKO |
| 13 | P | $V_{BAT}$ |
| 14 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 15 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 16 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 17 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 18 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / EPWM1_CH2 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 19 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / EPWM1_CH3 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 20 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / ACMP0_WLAT / TM2 / INT1 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 21 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / ACMP1_WLAT / TM3 / INT0 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 22 | P | $V_{SS}$ |
| 23 | P | $V_{DD}$ |
| 24 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 25 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / EPWM0_CH0 / EQEI0_INDEX / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 26 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / EPWM0_CH1 / EQEI0_A / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 27 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / I2C0_SMBAL / UART1_TXD / I2C1_SCL / EQEI0_B / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / UTCPD0_VBSNKEN / LPSPI0_SS |

| Pin | Type | M2L31SE4AE Pin Function |
|---|---|---|
| 28 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / EPWM0_CH3 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 29 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / EQEI0_INDEX / EPWM0_CH4 / ACMP2_O / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 30 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / EPWM0_BRAKE0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 31 | P | $V_{DDIO}$ |
| 32 | I | nRESET |
| 33 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 34 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / EPWM1_CH5 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 35 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 36 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 37 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / UTCPD0_CCDB2 |
| 38 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / UTCPD0_CCDB1 |
| 39 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 40 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 41 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / UART0_TXD / LPSPI0_SS / LPUART0_TXD |
| 42 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / LPSPI0_CLK / LPUART0_RXD |
| 43 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / LPSPI0_MISO / LPIO7 |
| 44 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / LPSPI0_MOSI / LPIO6 |
| 45 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI0_SS / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 46 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI0_CLK / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 47 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI0_MISO / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 48 | I/O | PA.15 / UART0_RXD / SPI0_MOSI / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 49 | P | $V_{SS}$ |
| 50 | A | LDO_CAP |
| 51 | P | $V_{DD}$ |
| 52 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 53 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |

| Pin | Type | M2L31SE4AE Pin Function |
|---|---|---|
| 54 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 55 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 56 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 57 | P | $AV_{DD}$ |
| 58 | A | $V_{REF}$ |
| 59 | P | $AV_{SS}$ |
| 60 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / SPI0_I2SMCLK / LPUART0_nCTS |
| 61 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / UART0_nRTS / UART4_RXD / I2C1_SDA / LPUART0_nRTS |
| 62 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / UART0_TXD / UART1_nCTS / LPUART0_TXD |
| 63 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / UART0_RXD / UART1_nRTS / LPUART0_RXD |
| 64 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / EBI_nWRL / UART1_TXD / EBI_nCS0 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O |

Table 6.2-14 M2L31SE4AE Multi-function Pin Table

#### 4.3.4.3 M2L31SIDAE

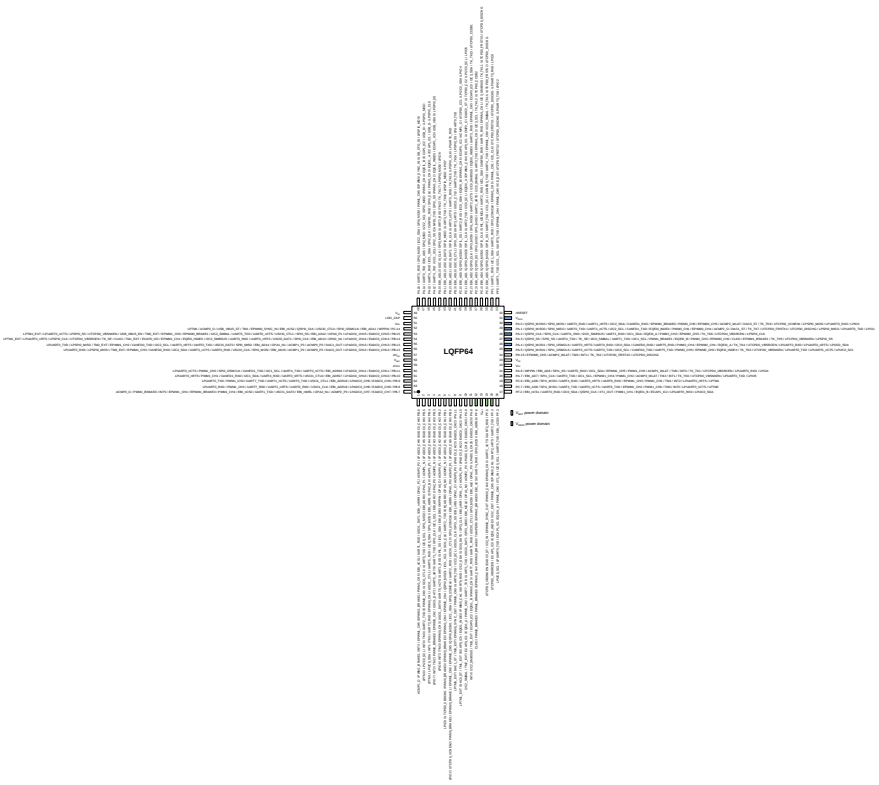



Figure 6.2-20 M2L31SIDAE Multi-function Pin Diagram

| Pin | Type | M2L31SIDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |
| 2 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 3 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 4 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / |

| Pin | Type | M2L31SIDAE Pin Function |
|---|---|---|
| | | UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 5 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 6 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 7 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 8 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 9 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 10 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 11 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 12 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / PWM1_BRAKE0 / PWM0_BRAKE0 / CLKO |
| 13 | P | $V_{BAT}$ |
| 14 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 15 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 16 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 17 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 18 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / UART6_TXD / EPWM1_CH2 / PWM1_CH0 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 19 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / UART6_RXD / EPWM1_CH3 / PWM1_CH1 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 20 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 21 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 22 | P | $V_{SS}$ |
| 23 | P | $V_{DD}$ |
| 24 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / TK_TK2 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 25 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |

| Pin | Type | M2L31SIDAE Pin Function |
|---|---|---|
| 26 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 27 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 28 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 29 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 30 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 31 | P | $V_{DDIO}$ |
| 32 | I | nRESET |
| 33 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 34 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 35 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 36 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 37 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 38 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 39 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 40 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 41 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD / TK_TK14 / LPSPI0_SS / LPUART0_TXD |
| 42 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / TK_TK15 / LPSPI0_CLK / LPUART0_RXD |
| 43 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / TK_TK16 / LPSPI0_MISO / LPIO7 |
| 44 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / TK_TK17 / LPSPI0_MOSI / LPIO6 |
| 45 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 46 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 47 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |

| Pin | Type | M2L31SIDAE Pin Function |
|---|---|---|
| 48 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 49 | P | $V_{SS}$ |
| 50 | A | LDO_CAP |
| 51 | P | $V_{DD}$ |
| 52 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 53 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 54 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 55 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 56 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 57 | P | $AV_{DD}$ |
| 58 | A | $V_{REF}$ |
| 59 | P | $AV_{SS}$ |
| 60 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD1_TXD / SPI0_I2SMCLK / PWM1_CH0 / LPUART0_nCTS |
| 61 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD1_RXD / PWM1_CH1 / LPUART0_nRTS |
| 62 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART7_TXD / PWM1_CH2 / LPUART0_TXD |
| 63 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / UART7_RXD / PWM1_CH3 / LPUART0_RXD |
| 64 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |

Table 6.2-15 M2L31SIDAE Multi-function Pin Table

#### 4.3.4.4 M2L31SGDAE

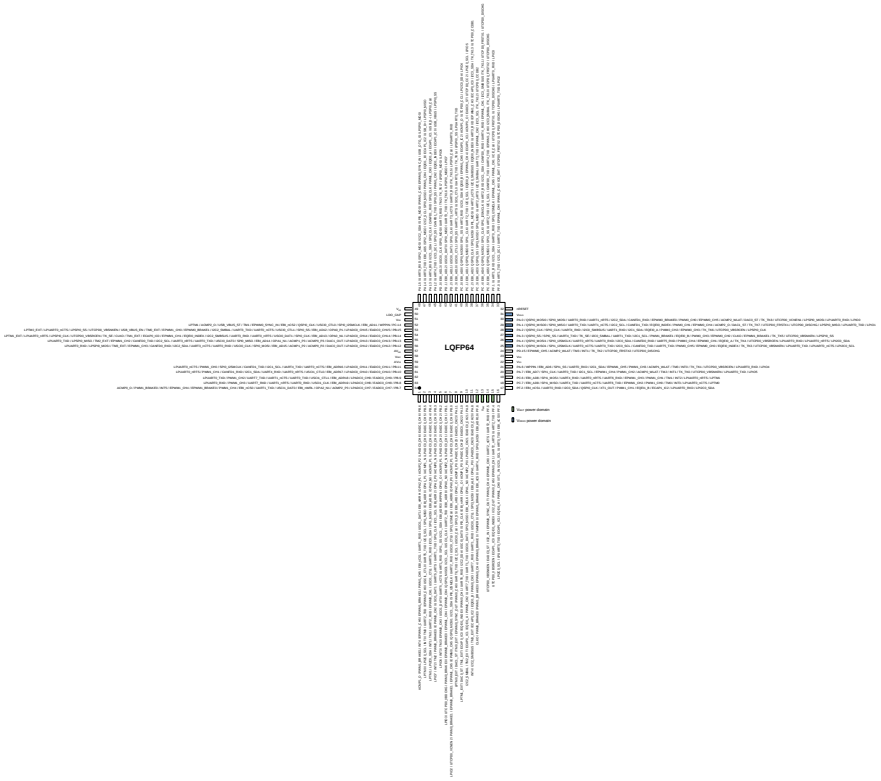



Figure 6.2-21 M2L31SGDAE Multi-function Pin Diagram

| Pin | Type | M2L31SGDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |
| 2 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 3 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 4 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 5 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / |

| Pin | Type | M2L31SGDAE Pin Function |
|---|---|---|
| | | SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 6 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 7 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 8 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 9 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 10 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 11 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 12 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / PWM1_BRAKE0 / PWM0_BRAKE0 / CLKO |
| 13 | P | $V_{BAT}$ |
| 14 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 15 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 16 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 17 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 18 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / UART6_TXD / EPWM1_CH2 / PWM1_CH0 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 19 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / UART6_RXD / EPWM1_CH3 / PWM1_CH1 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 20 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 21 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 22 | P | $V_{SS}$ |
| 23 | P | $V_{DD}$ |
| 24 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / TK_TK2 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 25 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 26 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |

| Pin | Type | M2L31SGDAE Pin Function |
|---|---|---|
| 27 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 28 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 29 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 30 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 31 | P | $V_{DDIO}$ |
| 32 | I | nRESET |
| 33 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 34 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 35 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 36 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 37 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 38 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 39 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 40 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 41 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD / TK_TK14 / LPSPI0_SS / LPUART0_TXD |
| 42 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / TK_TK15 / LPSPI0_CLK / LPUART0_RXD |
| 43 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / TK_TK16 / LPSPI0_MISO / LPIO7 |
| 44 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / TK_TK17 / LPSPI0_MOSI / LPIO6 |
| 45 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 46 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 47 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 48 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 49 | P | $V_{SS}$ |

| Pin | Type | M2L31SGDAE Pin Function |
|---|---|---|
| 50 | A | LDO_CAP |
| 51 | P | $V_{DD}$ |
| 52 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 53 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 54 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 55 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 56 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 57 | P | $AV_{DD}$ |
| 58 | A | $V_{REF}$ |
| 59 | P | $AV_{SS}$ |
| 60 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD1_TXD / SPI0_I2SMCLK / PWM1_CH0 / LPUART0_nCTS |
| 61 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD1_RXD / PWM1_CH1 / LPUART0_nRTS |
| 62 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART7_TXD / PWM1_CH2 / LPUART0_TXD |
| 63 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / UART7_RXD / PWM1_CH3 / LPUART0_RXD |
| 64 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |

Table 6.2-16 M2L31SGDAE Multi-function Pin Table

### 4.3.5 LQFP128-Pin Multi-function Diagram

Corresponding Part Number: M2L31KIDAE, M2L31KGDAE

#### *4.3.5.1 M2L31KIDAE*

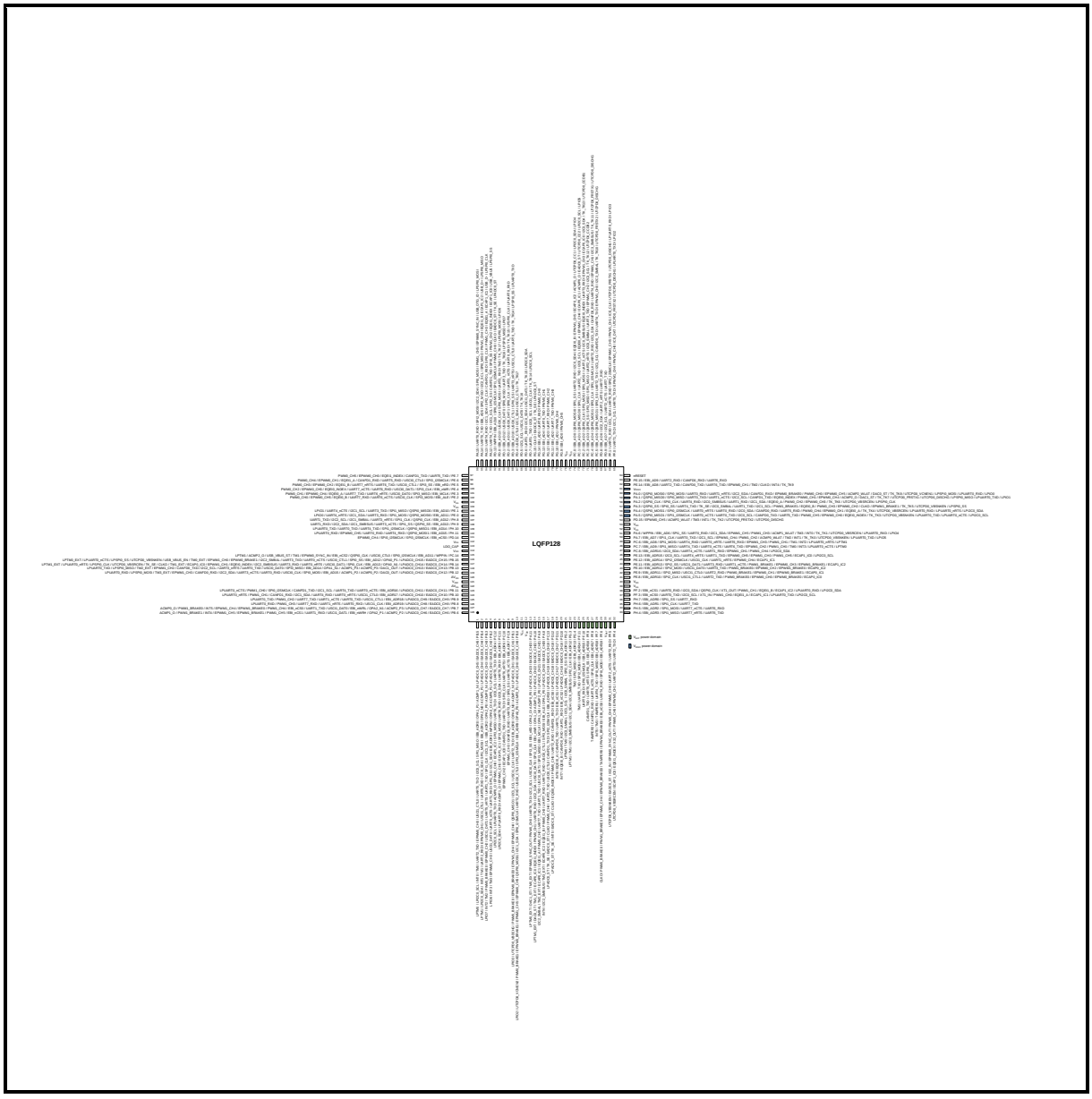



Figure 6.2-22 M2L31KIDAE Multi-function Pin Diagram

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O / LPUART0_TXD / LPI2C0_SCL |
| 6 | I/O | PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O / LPUART0_RXD / LPI2C0_SDA |
| 7 | I/O | PC.10 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CANFD1_TXD / ECAP1_IC0 / EPWM1_CH2 |
| 8 | I/O | PC.9 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CANFD1_RXD / EPWM1_CH3 |
| 9 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 10 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 11 | P | $V_{SS}$ |
| 12 | P | $V_{DD}$ |
| 13 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 14 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 15 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 16 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 17 | I/O | PC.13 / EADC0_CH19 / LPADC0_CH19 / EBI_ADR10 / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / PWM0_CH4 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 18 | I/O | PD.12 / EADC0_CH18 / LPADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / PWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5 / TK_SE / LPADC0_ST |
| 19 | I/O | PD.11 / EADC0_CH17 / LPADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / EQEI0_A / INT6 |
| 20 | I/O | PD.10 / EADC0_CH16 / LPADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7 |
| 21 | I/O | PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / I2C3_SMBAL / TM0 / LPTM0 |
| 22 | I/O | PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / I2C3_SMBSUS / TM1 / LPTM1 |
| 23 | I/O | PG.4 / EBI_ADR13 / SPI2_MISO / TM2 |
| 24 | I/O | PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / TM3 |
| 25 | I/O | PF.10 / EBI_ADR15 / SPI0_I2SMCLK / UART5_RXD |
| 26 | I/O | PF.9 / EBI_ADR16 / SPI0_SS / UART5_nRTS / CANFD1_TXD |
| 27 | I/O | PF.8 / EBI_ADR17 / SPI0_CLK / UART5_nCTS / CANFD1_RXD / TAMPER2 |
| 28 | I/O | PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD / TAMPER1 / TM3 / INT5 |

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| 29 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / PWM1_BRAKE0 / PWM0_BRAKE0 / CLKO |
| 30 | P | $V_{BAT}$ |
| 31 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 32 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 33 | I/O | PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD |
| 34 | I/O | PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD |
| 35 | I/O | PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD |
| 36 | I/O | PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD |
| 37 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 38 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 39 | P | $V_{SS}$ |
| 40 | P | $V_{DD}$ |
| 41 | I/O | PE.8 / EBI_ADR10 / SPI2_CLK / USCI1_CTL1 / UART2_TXD / PWM0_BRAKE0 / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 |
| 42 | I/O | PE.9 / EBI_ADR11 / SPI2_MISO / USCI1_CTL0 / UART2_RXD / PWM0_BRAKE1 / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 |
| 43 | I/O | PE.10 / EBI_ADR12 / SPI2_MOSI / USCI1_DAT0 / UART3_TXD / PWM1_BRAKE0 / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 |
| 44 | I/O | PE.11 / EBI_ADR13 / SPI2_SS / USCI1_DAT1 / UART3_RXD / UART1_nCTS / PWM1_BRAKE1 / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 |
| 45 | I/O | PE.12 / EBI_ADR14 / SPI2_I2SMCLK / USCI1_CLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 |
| 46 | I/O | PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / PWM1_CH5 / ECAP1_IC0 / LPI2C0_SCL |
| 47 | I/O | PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / PWM1_CH4 / LPI2C0_SDA |
| 48 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / UART6_TXD / EPWM1_CH2 / PWM1_CH0 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 49 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / UART6_RXD / EPWM1_CH3 / PWM1_CH1 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 50 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 51 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 52 | P | $V_{SS}$ |
| 53 | P | $V_{DD}$ |
| 54 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / TK_TK2 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 55 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / |

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| | | UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 56 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 57 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 58 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 59 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 60 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 61 | P | $V_{DDIO}$ |
| 62 | I/O | PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD / EPWM0_CH1 / TM2 / CLKO / INT4 / TK_TK9 |
| 63 | I/O | PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD |
| 64 | I | nRESET |
| 65 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 66 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 67 | I/O | PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD |
| 68 | I/O | PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD |
| 69 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 70 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 71 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 72 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 73 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 74 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 75 | P | $V_{SS}$ |
| 76 | P | $V_{DD}$ |
| 77 | I/O | PG.9 / EBI_AD0 / PWM0_CH5 |
| 78 | I/O | PG.10 / EBI_AD1 / PWM0_CH4 |

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| 79 | I/O | PG.11 / EBI_AD2 / UART7_TXD / PWM0_CH3 |
| 80 | I/O | PG.12 / EBI_AD3 / UART7_RXD / PWM0_CH2 |
| 81 | I/O | PG.13 / EBI_AD4 / UART6_TXD / PWM0_CH1 |
| 82 | I/O | PG.14 / EBI_AD5 / UART6_RXD / PWM0_CH0 |
| 83 | I/O | PG.15 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 84 | I/O | PD.7 / UART1_TXD / I2C0_SCL / USCI1_CLK / TK_TK14 / LPI2C0_SCL |
| 85 | I/O | PD.6 / UART1_RXD / I2C0_SDA / USCI1_DAT1 / TK_TK15 / LPI2C0_SDA |
| 86 | I/O | PD.5 / I2C1_SCL / USCI1_DAT0 / TK_TK16 |
| 87 | I/O | PD.4 / USCI0_CTL0 / I2C1_SDA / USCI1_CTL1 / TK_TK17 |
| 88 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD / TK_TK14 / LPSPI0_SS / LPUART0_TXD |
| 89 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / TK_TK15 / LPSPI0_CLK / LPUART0_RXD |
| 90 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / TK_TK16 / LPSPI0_MISO / LPIO7 |
| 91 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / TK_TK17 / LPSPI0_MOSI / LPIO6 |
| 92 | I/O | PD.13 / WPPIN / EBI_AD10 / SPI0_I2SMCLK / SPI1_I2SMCLK / PWM0_CH0 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 93 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 94 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 95 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 96 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 97 | I/O | PE.7 / UART5_TXD / CANFD1_TXD / EQEI1_INDEX / EPWM0_CH0 / PWM0_CH5 |
| 98 | I/O | PE.6 / SPI3_I2SMCLK / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / EPWM0_CH1 / PWM0_CH4 |
| 99 | I/O | PE.5 / EBI_nRD / SPI3_SS / USCI0_CTL1 / UART6_TXD / UART7_nRTS / EQEI1_B / EPWM0_CH2 / PWM0_CH3 |
| 100 | I/O | PE.4 / EBI_nWR / SPI3_CLK / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / EPWM0_CH3 / PWM0_CH2 |
| 101 | I/O | PE.3 / EBI_MCLK / SPI3_MISO / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / EPWM0_CH4 / PWM0_CH1 |
| 102 | I/O | PE.2 / EBI_ALE / SPI3_MOSI / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / EPWM0_CH5 / PWM0_CH0 |
| 103 | P | $V_{SS}$ |
| 104 | P | $V_{DD}$ |
| 105 | I/O | PE.1 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / LPIO1 |
| 106 | I/O | PE.0 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / LPIO0 |
| 107 | I/O | PH.8 / EBI_AD12 / QSPI0_CLK / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / |

| Pin | Type | M2L31KIDAE Pin Function |
|---|---|---|
| | | UART1_TXD |
| 108 | I/O | PH.9 / EBI_AD13 / QSPI0_SS / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD |
| 109 | I/O | PH.10 / EBI_AD14 / QSPI0_MISO1 / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / LPUART0_TXD |
| 110 | I/O | PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / LPUART0_RXD |
| 111 | I/O | PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SPI0_I2SMCLK / EPWM0_CH4 |
| 112 | P | $V_{SS}$ |
| 113 | A | LDO_CAP |
| 114 | P | $V_{DD}$ |
| 115 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 116 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 117 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 118 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 119 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 120 | P | $AV_{DD}$ |
| 121 | A | $V_{REF}$ |
| 122 | P | $AV_{SS}$ |
| 123 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD1_TXD / SPI0_I2SMCLK / PWM1_CH0 / LPUART0_nCTS |
| 124 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD1_RXD / PWM1_CH1 / LPUART0_nRTS |
| 125 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART7_TXD / PWM1_CH2 / LPUART0_TXD |
| 126 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / UART7_RXD / PWM1_CH3 / LPUART0_RXD |
| 127 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |
| 128 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-17 M2L31KIDAE Multi-function Pin Table

#### 4.3.5.2 M2L31KGDAE

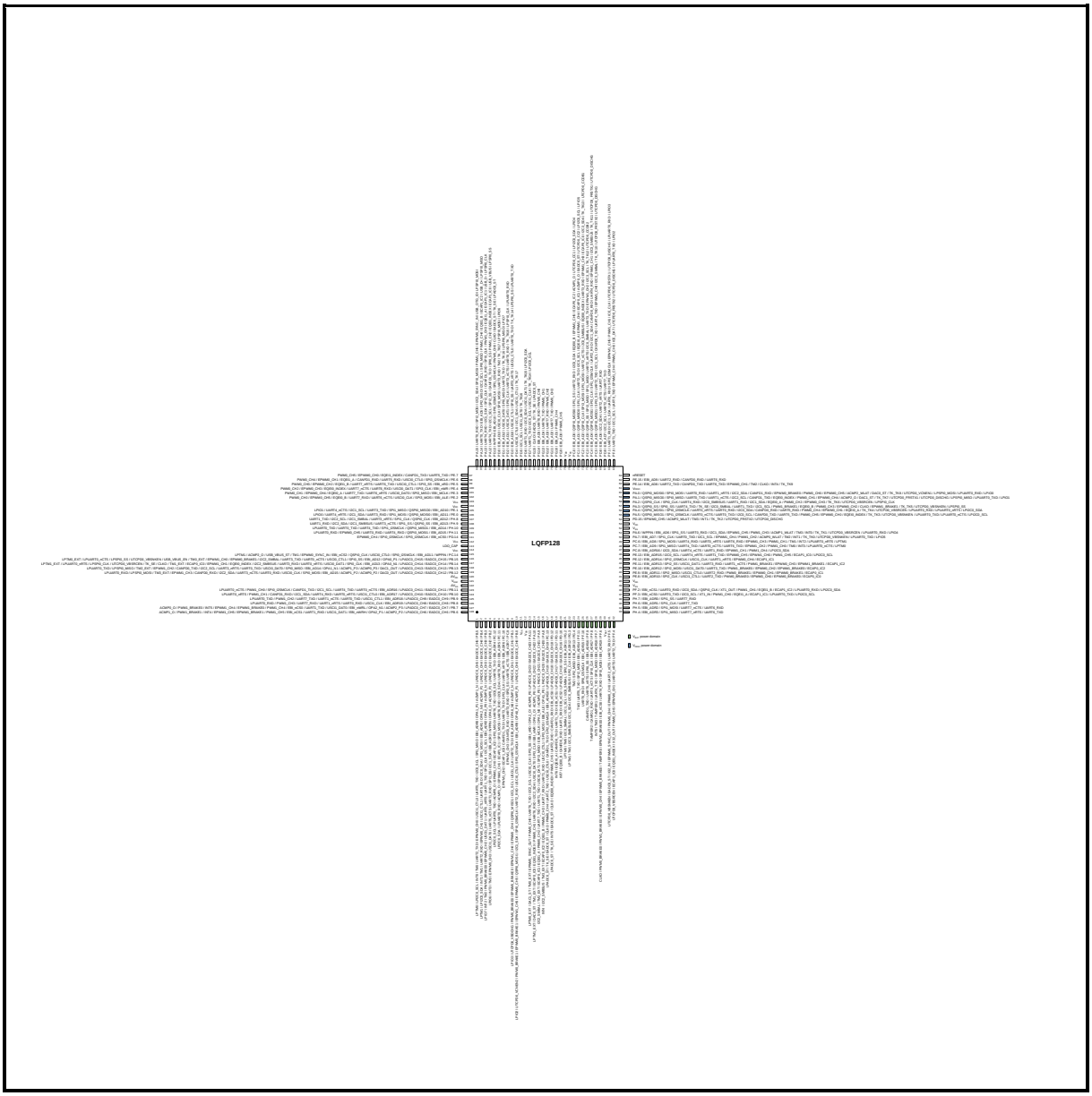



Figure 6.2-23 M2L31KGDAE Multi-function Pin Diagram

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| 1 | I/O | PB.5 / EADC0_CH5 / LPADC0_CH5 / ACMP1_N / OPA1_P1 / EBI_ADR0 / SPI1_MISO / I2C0_SCL / UART5_TXD / USCI1_CTL0 / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / LPI2C0_SCL / LPTM0 |
| 2 | I/O | PB.4 / EADC0_CH4 / LPADC0_CH4 / ACMP1_P1 / OPA2_N0 / EBI_ADR1 / SPI1_MOSI / I2C0_SDA / UART5_RXD / USCI1_CTL1 / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / LPI2C0_SDA / LPTM1 |
| 3 | I/O | PB.3 / EADC0_CH3 / LPADC0_CH3 / ACMP0_N / OPA2_P0 / EBI_ADR2 / I2C1_SCL / SPI1_CLK / UART1_TXD / UART5_nRTS / USCI1_DAT1 / EPWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2 / LPIO7 |
| 4 | I/O | PB.2 / EADC0_CH2 / LPADC0_CH2 / ACMP0_P1 / OPA0_O / WPPIN / EBI_ADR3 / I2C1_SDA / SPI1_SS / UART1_RXD / UART5_nCTS / USCI1_DAT0 / EPWM0_CH3 / TM3 / INT3 / LPIO6 |
| 5 | I/O | PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / ECAP1_IC2 / |

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| | | EPWM1_CH0 / ACMP0_O / LPUART0_TXD / LPI2C0_SCL |
| 6 | I/O | PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O / LPUART0_RXD / LPI2C0_SDA |
| 7 | I/O | PC.10 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CANFD1_TXD / ECAP1_IC0 / EPWM1_CH2 |
| 8 | I/O | PC.9 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CANFD1_RXD / EPWM1_CH3 |
| 9 | I/O | PB.1 / EADC0_CH1 / LPADC0_CH1 / ACMP2_N / OPA0_N0 / EBI_ADR8 / UART2_TXD / USCI1_CLK / I2C1_SCL / QSPI0_MISO1 / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / PWM0_BRAKE0 / UTCPD0_VBDCHG / LPIO3 |
| 10 | I/O | PB.0 / EADC0_CH0 / LPADC0_CH0 / ACMP2_P1 / OPA0_P0 / EBI_ADR9 / SPI3_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / QSPI0_MOSI1 / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / PWM0_BRAKE1 / UTCPD0_VCNEN2 / LPIO2 |
| 11 | P | $V_{SS}$ |
| 12 | P | $V_{DD}$ |
| 13 | I/O | PA.11 / EADC0_CH23 / LPADC0_CH23 / ACMP0_P0 / OPA2_O / EBI_nRD / SPI3_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / PWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / DAC1_ST / LPTM0_EXT |
| 14 | I/O | PA.10 / EADC0_CH22 / LPADC0_CH22 / ACMP1_P0 / OPA1_O / EBI_nWR / SPI3_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / PWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / DAC0_ST / LPTM1_EXT |
| 15 | I/O | PA.9 / EADC0_CH21 / LPADC0_CH21 / ACMP2_P0 / OPA1_N0 / EBI_MCLK / SPI3_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / PWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT / I2C2_SMBAL |
| 16 | I/O | PA.8 / EADC0_CH20 / LPADC0_CH20 / OPA1_P0 / EBI_ALE / SPI3_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / PWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / I2C2_SMBSUS / INT4 |
| 17 | I/O | PC.13 / EADC0_CH19 / LPADC0_CH19 / EBI_ADR10 / SPI2_I2SMCLK / CANFD1_TXD / USCI0_CTL0 / UART2_TXD / PWM0_CH4 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 18 | I/O | PD.12 / EADC0_CH18 / LPADC0_CH18 / EBI_nCS0 / CANFD1_RXD / UART2_RXD / PWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5 / TK_SE / LPADC0_ST |
| 19 | I/O | PD.11 / EADC0_CH17 / LPADC0_CH17 / EBI_nCS1 / UART1_TXD / CANFD0_TXD / EQEI0_A / INT6 |
| 20 | I/O | PD.10 / EADC0_CH16 / LPADC0_CH16 / EBI_nCS2 / UART1_RXD / CANFD0_RXD / EQEI0_B / INT7 |
| 21 | I/O | PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / I2C3_SMBAL / TM0 / LPTM0 |
| 22 | I/O | PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / I2C3_SMBSUS / TM1 / LPTM1 |
| 23 | I/O | PG.4 / EBI_ADR13 / SPI2_MISO / TM2 |
| 24 | I/O | PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / TM3 |
| 25 | I/O | PF.10 / EBI_ADR15 / SPI0_I2SMCLK / UART5_RXD |
| 26 | I/O | PF.9 / EBI_ADR16 / SPI0_SS / UART5_nRTS / CANFD1_TXD |
| 27 | I/O | PF.8 / EBI_ADR17 / SPI0_CLK / UART5_nCTS / CANFD1_RXD / TAMPER2 |
| 28 | I/O | PF.7 / EBI_ADR18 / SPI0_MISO / UART4_TXD / TAMPER1 / TM3 / INT5 |
| 29 | I/O | PF.6 / EBI_ADR19 / SPI0_MOSI / UART4_RXD / EBI_nCS0 / EPWM1_BRAKE0 / TAMPER0 / EPWM0_BRAKE0 / EPWM0_CH4 / PWM1_BRAKE0 / PWM0_BRAKE0 / CLKO |
| 30 | P | $V_{BAT}$ |

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| 31 | I/O | PF.5 / UART2_RXD / UART2_nCTS / EPWM0_CH0 / PWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / UTCPD0_VBSNKEN |
| 32 | I/O | PF.4 / UART2_TXD / UART2_nRTS / EPWM0_CH1 / PWM0_CH5 / X32_OUT / EQEI1_INDEX / ECAP1_IC0 / UTCPD0_VBSRCEN |
| 33 | I/O | PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD |
| 34 | I/O | PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD |
| 35 | I/O | PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD |
| 36 | I/O | PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD |
| 37 | I/O | PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / PWM1_CH0 / EQEI1_A / ECAP1_IC1 / LPUART0_TXD / LPI2C0_SCL |
| 38 | I/O | PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / PWM1_CH1 / EQEI1_B / ECAP1_IC2 / LPUART0_RXD / LPI2C0_SDA |
| 39 | P | $V_{SS}$ |
| 40 | P | $V_{DD}$ |
| 41 | I/O | PE.8 / EBI_ADR10 / SPI2_CLK / USCI1_CTL1 / UART2_TXD / PWM0_BRAKE0 / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 |
| 42 | I/O | PE.9 / EBI_ADR11 / SPI2_MISO / USCI1_CTL0 / UART2_RXD / PWM0_BRAKE1 / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 |
| 43 | I/O | PE.10 / EBI_ADR12 / SPI2_MOSI / USCI1_DAT0 / UART3_TXD / PWM1_BRAKE0 / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 |
| 44 | I/O | PE.11 / EBI_ADR13 / SPI2_SS / USCI1_DAT1 / UART3_RXD / UART1_nCTS / PWM1_BRAKE1 / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 |
| 45 | I/O | PE.12 / EBI_ADR14 / SPI2_I2SMCLK / USCI1_CLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 |
| 46 | I/O | PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / PWM1_CH5 / ECAP1_IC0 / LPI2C0_SCL |
| 47 | I/O | PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / PWM1_CH4 / LPI2C0_SDA |
| 48 | I/O | PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / UART6_TXD / EPWM1_CH2 / PWM1_CH0 / TM0 / INT3 / LPUART0_nCTS / LPTM0 |
| 49 | I/O | PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / UART6_RXD / EPWM1_CH3 / PWM1_CH1 / TM1 / INT2 / LPUART0_nRTS / LPTM1 |
| 50 | I/O | PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / EPWM1_CH4 / PWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / TK_TK0 / UTCPD0_VBSNKEN / LPUART0_TXD / LPIO5 |
| 51 | I/O | PA.6 / WPPIN / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / EPWM1_CH5 / PWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / TK_TK1 / UTCPD0_VBSRCEN / LPUART0_RXD / LPIO4 |
| 52 | P | $V_{SS}$ |
| 53 | P | $V_{DD}$ |
| 54 | I/O | PD.15 / EPWM0_CH5 / ACMP2_WLAT / TM3 / INT1 / TK_TK2 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 55 | I/O | PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART0_TXD / I2C0_SCL / CANFD0_TXD / UART5_TXD / PWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX / TK_TK3 / UTCPD0_VBSNKEN / LPUART0_TXD / LPUART0_nCTS / LPI2C0_SCL |
| 56 | I/O | PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_RXD / UART5_RXD / PWM0_CH4 / EPWM0_CH1 / EQEI0_A / TK_TK4 / UTCPD0_VBSRCEN / |

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| | | LPUART0_RXD / LPUART0_nRTS / LPI2C0_SDA |
| 57 | I/O | PA.3 / QSPI0_SS / SPI0_SS / UART4_TXD / TK_SE / I2C0_SMBAL / UART1_TXD / I2C1_SCL / PWM1_BRAKE1 / EQEI0_B / PWM0_CH3 / EPWM0_CH2 / CLKO / EPWM1_BRAKE1 / TK_TK5 / UTCPD0_VBSNKEN / LPSPI0_SS |
| 58 | I/O | PA.2 / QSPI0_CLK / SPI0_CLK / UART4_RXD / I2C0_SMBSUS / UART1_RXD / I2C1_SDA / EQEI0_A / PWM0_CH2 / EPWM0_CH3 / TK_TK6 / UTCPD0_VBSRCEN / LPSPI0_CLK |
| 59 | I/O | PA.1 / QSPI0_MISO0 / SPI0_MISO / UART0_TXD / UART1_nCTS / I2C2_SCL / CANFD1_TXD / EQEI0_INDEX / PWM0_CH1 / EPWM0_CH4 / ACMP2_O / DAC1_ST / TK_TK7 / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPSPI0_MISO / LPUART0_TXD / LPIO1 |
| 60 | I/O | PA.0 / QSPI0_MOSI0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / I2C2_SDA / CANFD1_RXD / EPWM0_BRAKE0 / PWM0_CH0 / EPWM0_CH5 / ACMP2_WLAT / DAC0_ST / TK_TK8 / UTCPD0_VCNEN1 / LPSPI0_MOSI / LPUART0_RXD / LPIO0 |
| 61 | P | $V_{DDIO}$ |
| 62 | I/O | PE.14 / EBI_AD8 / UART2_TXD / CANFD0_TXD / UART6_TXD / EPWM0_CH1 / TM2 / CLKO / INT4 / TK_TK9 |
| 63 | I/O | PE.15 / EBI_AD9 / UART2_RXD / CANFD0_RXD / UART6_RXD |
| 64 | I | nRESET |
| 65 | I/O | PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / EPWM1_CH4 / PWM1_CH0 / ICE_DAT / UTCPD0_FRSTX2 / UTCPD0_DISCHG / LPUART0_TXD / LPIO2 |
| 66 | I/O | PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SPI3_I2SMCLK / EPWM1_CH5 / PWM1_CH1 / ICE_CLK / UTCPD0_FRSTX1 / UTCPD0_DISCHG / LPUART0_RXD / LPIO3 |
| 67 | I/O | PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD |
| 68 | I/O | PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD |
| 69 | I/O | PC.5 / EBI_AD5 / QSPI0_MISO1 / SPI3_SS / UART2_TXD / I2C1_SCL / CANFD0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL / TK_TK10 / UTCPD0_FRSTX2 / UTCPD0_DISCHG |
| 70 | I/O | PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI3_CLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CANFD0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS / TK_TK11 / UTCPD0_FRSTX1 / UTCPD0_DISCHG |
| 71 | I/O | PC.3 / EBI_AD3 / QSPI0_SS / SPI3_MISO / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / UART3_TXD / EPWM1_CH2 / I2C3_SCL / TK_TK12 / UTCPD0_CCDB2 |
| 72 | I/O | PC.2 / EBI_AD2 / QSPI0_CLK / SPI3_MOSI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / EQEI0_INDEX / UART3_RXD / EPWM1_CH3 / ECAP0_IC0 / I2C3_SDA / TK_TK13 / UTCPD0_CCDB1 |
| 73 | I/O | PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EQEI0_A / EPWM1_CH4 / ECAP0_IC1 / ACMP0_O / EADC0_ST / UTCPD0_CC2 / LPI2C0_SCL / LPIO5 |
| 74 | I/O | PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EQEI0_B / EPWM1_CH5 / ECAP0_IC2 / ACMP1_O / UTCPD0_CC1 / LPI2C0_SDA / LPIO4 |
| 75 | P | $V_{SS}$ |
| 76 | P | $V_{DD}$ |
| 77 | I/O | PG.9 / EBI_AD0 / PWM0_CH5 |
| 78 | I/O | PG.10 / EBI_AD1 / PWM0_CH4 |
| 79 | I/O | PG.11 / EBI_AD2 / UART7_TXD / PWM0_CH3 |
| 80 | I/O | PG.12 / EBI_AD3 / UART7_RXD / PWM0_CH2 |
| 81 | I/O | PG.13 / EBI_AD4 / UART6_TXD / PWM0_CH1 |

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| 82 | I/O | PG.14 / EBI_AD5 / UART6_RXD / PWM0_CH0 |
| 83 | I/O | PG.15 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 84 | I/O | PD.7 / UART1_TXD / I2C0_SCL / USCI1_CLK / TK_TK14 / LPI2C0_SCL |
| 85 | I/O | PD.6 / UART1_RXD / I2C0_SDA / USCI1_DAT1 / TK_TK15 / LPI2C0_SDA |
| 86 | I/O | PD.5 / I2C1_SCL / USCI1_DAT0 / TK_TK16 |
| 87 | I/O | PD.4 / USCI0_CTL0 / I2C1_SDA / USCI1_CTL1 / TK_TK17 |
| 88 | I/O | PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / USCI1_CTL0 / UART0_TXD / TK_TK14 / LPSPI0_SS / LPUART0_TXD |
| 89 | I/O | PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / UART0_RXD / TK_TK15 / LPSPI0_CLK / LPUART0_RXD |
| 90 | I/O | PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / TK_TK16 / LPSPI0_MISO / LPIO7 |
| 91 | I/O | PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / TM2 / TK_TK17 / LPSPI0_MOSI / LPIO6 |
| 92 | I/O | PD.13 / WPPIN / EBI_AD10 / SPI0_I2SMCLK / SPI1_I2SMCLK / PWM0_CH0 / CLKO / EADC0_ST / TK_SE / LPADC0_ST |
| 93 | I/O | PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CANFD1_TXD / SPI0_SS / PWM1_CH2 / EQEI1_INDEX / ECAP1_IC0 / USB_VBUS / LPSPI0_SS |
| 94 | I/O | PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CANFD1_RXD / SPI0_CLK / PWM1_CH3 / EQEI1_A / ECAP1_IC1 / USB_D- / LPSPI0_CLK |
| 95 | I/O | PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / PWM1_CH4 / EQEI1_B / ECAP1_IC2 / USB_D+ / LPSPI0_MISO |
| 96 | I/O | PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / PWM1_CH5 / EPWM0_SYNC_IN / USB_OTG_ID / LPSPI0_MOSI |
| 97 | I/O | PE.7 / UART5_TXD / CANFD1_TXD / EQEI1_INDEX / EPWM0_CH0 / PWM0_CH5 |
| 98 | I/O | PE.6 / SPI3_I2SMCLK / USCI0_CTL0 / UART5_RXD / CANFD1_RXD / EQEI1_A / EPWM0_CH1 / PWM0_CH4 |
| 99 | I/O | PE.5 / EBI_nRD / SPI3_SS / USCI0_CTL1 / UART6_TXD / UART7_nRTS / EQEI1_B / EPWM0_CH2 / PWM0_CH3 |
| 100 | I/O | PE.4 / EBI_nWR / SPI3_CLK / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / EPWM0_CH3 / PWM0_CH2 |
| 101 | I/O | PE.3 / EBI_MCLK / SPI3_MISO / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / EPWM0_CH4 / PWM0_CH1 |
| 102 | I/O | PE.2 / EBI_ALE / SPI3_MOSI / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / EPWM0_CH5 / PWM0_CH0 |
| 103 | P | $V_{SS}$ |
| 104 | P | $V_{DD}$ |
| 105 | I/O | PE.1 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / LPIO1 |
| 106 | I/O | PE.0 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / LPIO0 |
| 107 | I/O | PH.8 / EBI_AD12 / QSPI0_CLK / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD |
| 108 | I/O | PH.9 / EBI_AD13 / QSPI0_SS / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD |
| 109 | I/O | PH.10 / EBI_AD14 / QSPI0_MISO1 / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / LPUART0_TXD |

| Pin | Type | M2L31KGDAE Pin Function |
|---|---|---|
| 110 | I/O | PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / LPUART0_RXD |
| 111 | I/O | PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SPI0_I2SMCLK / EPWM0_CH4 |
| 112 | P | $V_{SS}$ |
| 113 | A | LDO_CAP |
| 114 | P | $V_{DD}$ |
| 115 | I/O | PC.14 / WPPIN / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / EBI_nCS2 / EPWM0_SYNC_IN / TM1 / USB_VBUS_ST / ACMP2_O / LPTM1 |
| 116 | I/O | PB.15 / EADC0_CH15 / LPADC0_CH15 / OPA0_P1 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / USB_VBUS_EN / UTCPD0_VBSNKEN / LPSPI0_SS / LPUART0_nCTS / LPTM0_EXT |
| 117 | I/O | PB.14 / EADC0_CH14 / LPADC0_CH14 / OPA0_N1 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EQEI0_INDEX / EPWM1_CH1 / ECAP0_IC0 / TM1_EXT / CLKO / TK_SE / UTCPD0_VBSRCEN / LPSPI0_CLK / LPUART0_nRTS / LPTM1_EXT |
| 118 | I/O | PB.13 / EADC0_CH13 / LPADC0_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / OPA1_N1 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CANFD0_TXD / EPWM1_CH2 / TM2_EXT / LPSPI0_MISO / LPUART0_TXD |
| 119 | I/O | PB.12 / EADC0_CH12 / LPADC0_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / CANFD0_RXD / EPWM1_CH3 / TM3_EXT / LPSPI0_MOSI / LPUART0_RXD |
| 120 | P | $AV_{DD}$ |
| 121 | A | $V_{REF}$ |
| 122 | P | $AV_{SS}$ |
| 123 | I/O | PB.11 / EADC0_CH11 / LPADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CANFD1_TXD / SPI0_I2SMCLK / PWM1_CH0 / LPUART0_nCTS |
| 124 | I/O | PB.10 / EADC0_CH10 / LPADC0_CH10 / EBI_ADR17 / USCI1_CTL0 / UART0_nRTS / UART4_RXD / I2C1_SDA / CANFD1_RXD / PWM1_CH1 / LPUART0_nRTS |
| 125 | I/O | PB.9 / EADC0_CH9 / LPADC0_CH9 / EBI_ADR18 / USCI1_CTL1 / UART0_TXD / UART1_nCTS / UART7_TXD / PWM1_CH2 / LPUART0_TXD |
| 126 | I/O | PB.8 / EADC0_CH8 / LPADC0_CH8 / EBI_ADR19 / USCI1_CLK / UART0_RXD / UART1_nRTS / UART7_RXD / PWM1_CH3 / LPUART0_RXD |
| 127 | I/O | PB.7 / EADC0_CH7 / LPADC0_CH7 / ACMP2_P3 / OPA2_N1 / EBI_nWRL / USCI1_DAT0 / UART1_TXD / EBI_nCS0 / PWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / PWM1_BRAKE0 / ACMP0_O |
| 128 | I/O | PB.6 / EADC0_CH6 / LPADC0_CH6 / ACMP2_P2 / OPA2_P1 / EBI_nWRH / USCI1_DAT1 / UART1_RXD / EBI_nCS1 / PWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / PWM1_BRAKE1 / ACMP1_O |

Table 6.2-18 M2L31KGDAE Multi-function Pin Table

## 4.4 Pin Mapping Table

### 4.4.1 M2L31 Series Mapping Table

| | M231 Series | | | | |
|---|---|---|---|---|---|
| Pin Name | M2L31ZxAE | M2L31YxAE | M2L31LxAE | M2L31SxAE | M2L31KxAE |
| PB.5 | 1 | 1 | 1 | 2 | 1 |
| PB.4 | 2 | 2 | 2 | 3 | 2 |
| PB.3 | 3 | 3 | 3 | 4 | 3 |
| PB.2 | 4 | 4 | 4 | 5 | 4 |
| PC.12 | | | | | 5 |
| PC.11 | | | | | 6 |
| PC.10 | | | | | 7 |
| PC.9 | | | | | 8 |
| PB.1 | 5 | 5 | 5 | 6 | 9 |
| PB.0 | 6 | 6 | 6 | 7 | 10 |
| $V_{SS}$ | | | | | 11 |
| $V_{DD}$ | | | | | 12 |
| PA.11 | | 7 | 7 | 8 | 13 |
| PA.10 | | 8 | 8 | 9 | 14 |
| PA.9 | | 9 | 9 | 10 | 15 |
| PA.8 | | 10 | 10 | 11 | 16 |
| PC.13 | | | | | 17 |
| PD.12 | | | | | 18 |
| PD.11 | | | | | 19 |
| PD.10 | | | | | 20 |
| PG.2 | | | | | 21 |
| PG.3 | | | | | 22 |
| PG.4 | | | | | 23 |
| PF.11 | | | | | 24 |
| PF.10 | | | | | 25 |
| PF.9 | | | | | 26 |
| PF.8 | | | | | 27 |
| PF.7 | | | | | 28 |
| PF.6 | | | | 12 | 29 |
| $V_{BAT}$ | | | | 13 | 30 |

| | | | | | |
|---|---|---|---|---|---|
| PF.5 | 7 | 11 | 11 | 14 | 31 |
| PF.4 | 8 | 12 | 12 | 15 | 32 |
| PH.4 | | | | | 33 |
| PH.5 | | | | | 34 |
| PH.6 | | | | | 35 |
| PH.7 | | | | | 36 |
| PF.3 | 9 | 13 | 13 | 16 | 37 |
| PF.2 | 10 | 14 | 14 | 17 | 38 |
| $V_{SS}$ | | | | | 39 |
| $V_{DD}$ | | | | | 40 |
| PE.8 | | | | | 41 |
| PE.9 | | | | | 42 |
| PE.10 | | | | | 43 |
| PE.11 | | | | | 44 |
| PE.12 | | | | | 45 |
| PE.13 | | | | | 46 |
| PC.8 | | | | | 47 |
| PC.7 | | | | 18 | 48 |
| PC.6 | | | | 19 | 49 |
| PA.7 | | 15 | 15 | 20 | 50 |
| PA.6 | | 16 | 16 | 21 | 51 |
| $V_{SS}$ | | | | 22 | 52 |
| $V_{DD}$ | | | | 23 | 53 |
| PD.15 | | | | 24 | 54 |
| PA.5 | | 17 | 17 | 25 | 55 |
| PA.4 | | 18 | 18 | 26 | 56 |
| PA.3 | 11 | 19 | 19 | 27 | 57 |
| PA.2 | 12 | 20 | 20 | 28 | 58 |
| PA.1 | 13 | 21 | 21 | 29 | 59 |
| PA.0 | 14 | 22 | 22 | 30 | 60 |
| $V_{DDIO}$ | 15 | 23 | 23 | 31 | 61 |
| PE.14 | | | | | 62 |
| PE.15 | | | | | 63 |
| nRESET | 16 | 24 | 24 | 32 | 64 |
| PF.0 | 17 | 25 | 25 | 33 | 65 |

| | | | | | |
|---|---|---|---|---|---|
| PF.1 | 18 | 26 | 26 | 34 | 66 |
| PD.9 | | | | | 67 |
| PD.8 | | | | | 68 |
| PC.5 | | 27 | 27 | 35 | 69 |
| PC.4 | | 28 | 28 | 36 | 70 |
| PC.3 | | 29 | 29 | 37 | 71 |
| PC.2 | | 30 | 30 | 38 | 72 |
| PC.1 | 19 | 31 | 31 | 39 | 73 |
| PC.0 | 20 | 32 | 32 | 40 | 74 |
| $V_{SS}$ | | | | | 75 |
| $V_{DD}$ | | | | | 76 |
| PG.9 | | | | | 77 |
| PG.10 | | | | | 78 |
| PG.11 | | | | | 79 |
| PG.12 | | | | | 80 |
| PG.13 | | | | | 81 |
| PG.14 | | | | | 82 |
| PG.15 | | | | | 83 |
| PD.7 | | | | | 84 |
| PD.6 | | | | | 85 |
| PD.5 | | | | | 86 |
| PD.4 | | | | | 87 |
| PD.3 | | | | 41 | 88 |
| PD.2 | | | | 42 | 89 |
| PD.1 | | | | 43 | 90 |
| PD.0 | | | | 44 | 91 |
| PD.13 | | | | | 92 |
| PA.12 | 21 | 33 | 33 | 45 | 93 |
| PA.13 | 22 | 34 | 34 | 46 | 94 |
| PA.14 | 23 | 35 | 35 | 47 | 95 |
| PA.15 | 24 | 36 | 36 | 48 | 96 |
| PE.7 | | | | | 97 |
| PE.6 | | | | | 98 |
| PE.5 | | | | | 99 |
| PE.4 | | | | | 100 |

| | | | | | |
|---|---|---|---|---|---|
| PE.3 | | | | | 101 |
| PE.2 | | | | | 102 |
| $V_{SS}$ | 25 | 37 | 37 | 49 | 103 |
| $V_{DD}$ | | | | | 104 |
| PE.1 | | | | | 105 |
| PE.0 | | | | | 106 |
| PH.8 | | | | | 107 |
| PH.9 | | | | | 108 |
| PH.10 | | | | | 109 |
| PH.11 | | | | | 110 |
| PD.14 | | | | | 111 |
| $V_{SS}$ | | | | | 112 |
| LDO_CAP | 26 | 38 | 38 | 50 | 113 |
| $V_{DD}$ | 27 | 39 | 39 | 51 | 114 |
| PC.14 | | 40 | 40 | 52 | 115 |
| PB.15 | 28 | 41 | 41 | 53 | 116 |
| PB.14 | 29 | 42 | 42 | 54 | 117 |
| PB.13 | 30 | 43 | 43 | 55 | 118 |
| PB.12 | 31 | 44 | 44 | 56 | 119 |
| $AV_{DD}$ | 32 | 45 | 45 | 57 | 120 |
| $V_{REF}$ | | | | 58 | 121 |
| $AV_{SS}$ | | 46 | 46 | 59 | 122 |
| PB.11 | | | | 60 | 123 |
| PB.10 | | | | 61 | 124 |
| PB.9 | | | | 62 | 125 |
| PB.8 | | | | 63 | 126 |
| PB.7 | | 47 | 47 | 64 | 127 |
| PB.6 | | 48 | 48 | 1 | 128 |
| $V_{SS}$ | 33 | 49 | | | |

## 4.5 Pin Functional Description

### 4.5.1 M2L31 Series Summary Function Pin Description

| Group | Pin Name | Type | Description |
|---|---|---|---|
| ACMP0 | ACMP0_N | A | Analog comparator 0 negative input pin. |
| | ACMP0_O | O | Analog comparator 0 output pin. |
| | ACMP0_P0 | A | Analog comparator 0 positive input 0 pin. |
| | ACMP0_P1 | A | Analog comparator 0 positive input 1 pin. |
| | ACMP0_P2 | A | Analog comparator 0 positive input 2 pin. |
| | ACMP0_P3 | A | Analog comparator 0 positive input 3 pin. |
| | ACMP0_WLAT | I | Analog comparator 0 window latch input pin |
| ACMP1 | ACMP1_N | A | Analog comparator 1 negative input pin. |
| | ACMP1_O | O | Analog comparator 1 output pin. |
| | ACMP1_P0 | A | Analog comparator 1 positive input 0 pin. |
| | ACMP1_P1 | A | Analog comparator 1 positive input 1 pin. |
| | ACMP1_P2 | A | Analog comparator 1 positive input 2 pin. |
| | ACMP1_P3 | A | Analog comparator 1 positive input 3 pin. |
| | ACMP1_WLAT | I | Analog comparator 1 window latch input pin |
| ACMP2 | ACMP2_N | A | Analog comparator 2 negative input pin. |
| | ACMP2_O | O | Analog comparator 2 output pin. |
| | ACMP2_P0 | A | Analog comparator 2 positive input 0 pin. |
| | ACMP2_P1 | A | Analog comparator 2 positive input 1 pin. |
| | ACMP2_P2 | A | Analog comparator 2 positive input 2 pin. |
| | ACMP2_P3 | A | Analog comparator 2 positive input 3 pin. |
| | ACMP2_WLAT | I | Analog comparator 2 window latch input pin |
| CANFD0 | CANFD0_RXD | I | CANF bus receiver input. |
| | CANFD0_TXD | O | CANF bus transmitter output. |
| CANFD1 | CANFD1_RXD | I | CANF bus receiver input. |
| | CANFD1_TXD | O | CANF bus transmitter output. |
| CLKO | CLKO | O | Clock Out |
| DAC0 | DAC0_OUT | A | DAC0 channel analog output. |
| | DAC0_ST | I | DAC0 external trigger input. |
| DAC1 | DAC1_OUT | A | DAC1 channel analog output. |
| | DAC1_ST | I | DAC1 external trigger input. |
| EADC0 | EADC0_CH0 | A | EADC0 channel 0 analog input. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | EADC0_CH1 | A | EADC0 channel 1 analog input. |
| | EADC0_CH2 | A | EADC0 channel 2 analog input. |
| | EADC0_CH3 | A | EADC0 channel 3 analog input. |
| | EADC0_CH4 | A | EADC0 channel 4 analog input. |
| | EADC0_CH5 | A | EADC0 channel 5 analog input. |
| | EADC0_CH6 | A | EADC0 channel 6 analog input. |
| | EADC0_CH7 | A | EADC0 channel 7 analog input. |
| | EADC0_CH8 | A | EADC0 channel 8 analog input. |
| | EADC0_CH9 | A | EADC0 channel 9 analog input. |
| | EADC0_CH10 | A | EADC0 channel 10 analog input. |
| | EADC0_CH11 | A | EADC0 channel 11 analog input. |
| | EADC0_CH12 | A | EADC0 channel 12 analog input. |
| | EADC0_CH13 | A | EADC0 channel 13 analog input. |
| | EADC0_CH14 | A | EADC0 channel 14 analog input. |
| | EADC0_CH15 | A | EADC0 channel 15 analog input. |
| | EADC0_CH16 | A | EADC0 channel 16 analog input. |
| | EADC0_CH17 | A | EADC0 channel 17 analog input. |
| | EADC0_CH18 | A | EADC0 channel 18 analog input. |
| | EADC0_CH19 | A | EADC0 channel 19 analog input. |
| | EADC0_CH20 | A | EADC0 channel 20 analog input. |
| | EADC0_CH21 | A | EADC0 channel 21 analog input. |
| | EADC0_CH22 | A | EADC0 channel 22 analog input. |
| | EADC0_CH23 | A | EADC0 channel 23 analog input. |
| | EADC0_ST | I | EADC0 external trigger input. |
| EBI | EBI_AD0 | I/O | EBI address/data bus bit 0. |
| | EBI_AD1 | I/O | EBI address/data bus bit 1. |
| | EBI_AD2 | I/O | EBI address/data bus bit 2. |
| | EBI_AD3 | I/O | EBI address/data bus bit 3. |
| | EBI_AD4 | I/O | EBI address/data bus bit 4. |
| | EBI_AD5 | I/O | EBI address/data bus bit 5. |
| | EBI_AD6 | I/O | EBI address/data bus bit 6. |
| | EBI_AD7 | I/O | EBI address/data bus bit 7. |
| | EBI_AD8 | I/O | EBI address/data bus bit 8. |
| | EBI_AD9 | I/O | EBI address/data bus bit 9. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | EBI_AD10 | I/O | EBI address/data bus bit 10. |
| | EBI_AD11 | I/O | EBI address/data bus bit 11. |
| | EBI_AD12 | I/O | EBI address/data bus bit 12. |
| | EBI_AD13 | I/O | EBI address/data bus bit 13. |
| | EBI_AD14 | I/O | EBI address/data bus bit 14. |
| | EBI_AD15 | I/O | EBI address/data bus bit 15. |
| | EBI_ADR0 | O | EBI address bus bit 0. |
| | EBI_ADR1 | O | EBI address bus bit 1. |
| | EBI_ADR2 | O | EBI address bus bit 2. |
| | EBI_ADR3 | O | EBI address bus bit 3. |
| | EBI_ADR4 | O | EBI address bus bit 4. |
| | EBI_ADR5 | O | EBI address bus bit 5. |
| | EBI_ADR6 | O | EBI address bus bit 6. |
| | EBI_ADR7 | O | EBI address bus bit 7. |
| | EBI_ADR8 | O | EBI address bus bit 8. |
| | EBI_ADR9 | O | EBI address bus bit 9. |
| | EBI_ADR10 | O | EBI address bus bit 10. |
| | EBI_ADR11 | O | EBI address bus bit 11. |
| | EBI_ADR12 | O | EBI address bus bit 12. |
| | EBI_ADR13 | O | EBI address bus bit 13. |
| | EBI_ADR14 | O | EBI address bus bit 14. |
| | EBI_ADR15 | O | EBI address bus bit 15. |
| | EBI_ADR16 | O | EBI address bus bit 16. |
| | EBI_ADR17 | O | EBI address bus bit 17. |
| | EBI_ADR18 | O | EBI address bus bit 18. |
| | EBI_ADR19 | O | EBI address bus bit 19. |
| | EBI_ALE | O | EBI address latch enable output pin. |
| | EBI_MCLK | O | EBI external clock output pin. |
| | EBI_nCS0 | O | EBI chip select 0 output pin. |
| | EBI_nCS1 | O | EBI chip select 1 output pin. |
| | EBI_nCS2 | O | EBI chip select 2 output pin. |
| | EBI_nRD | O | EBI read enable output pin. |
| | EBI_nWR | O | EBI write enable output pin. |
| | EBI_nWRH | O | EBI high byte write enable output pin |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | EBI_nWRL | O | EBI low byte write enable output pin. |
| ECAP0 | ECAP0_IC0 | I | Enhanced capture unit 0 input 0 pin. |
| | ECAP0_IC1 | I | Enhanced capture unit 0 input 1 pin. |
| | ECAP0_IC2 | I | Enhanced capture unit 0 input 2 pin. |
| ECAP1 | ECAP1_IC0 | I | Enhanced capture unit 1 input 0 pin. |
| | ECAP1_IC1 | I | Enhanced capture unit 1 input 1 pin. |
| | ECAP1_IC2 | I | Enhanced capture unit 1 input 2 pin. |
| EPWM0 | EPWM0_BRAKE0 | I | EPWM0 Brake 0 input pin. |
| | EPWM0_BRAKE1 | I | EPWM0 Brake 1 input pin. |
| | EPWM0_CH0 | I/O | EPWM0 channel 0 output/capture input. |
| | EPWM0_CH1 | I/O | EPWM0 channel 1 output/capture input. |
| | EPWM0_CH2 | I/O | EPWM0 channel 2 output/capture input. |
| | EPWM0_CH3 | I/O | EPWM0 channel 3 output/capture input. |
| | EPWM0_CH4 | I/O | EPWM0 channel 4 output/capture input. |
| | EPWM0_CH5 | I/O | EPWM0 channel 5 output/capture input. |
| | EPWM0_SYNC_IN | I | EPWM0 counter synchronous trigger input pin. |
| | EPWM0_SYNC_OUT | O | EPWM0 counter synchronous trigger output pin. |
| EPWM1 | EPWM1_BRAKE0 | I | EPWM1 Brake 0 input pin. |
| | EPWM1_BRAKE1 | I | EPWM1 Brake 1 input pin. |
| | EPWM1_CH0 | I/O | EPWM1 channel 0 output/capture input. |
| | EPWM1_CH1 | I/O | EPWM1 channel 1 output/capture input. |
| | EPWM1_CH2 | I/O | EPWM1 channel 2 output/capture input. |
| | EPWM1_CH3 | I/O | EPWM1 channel 3 output/capture input. |
| | EPWM1_CH4 | I/O | EPWM1 channel 4 output/capture input. |
| | EPWM1_CH5 | I/O | EPWM1 channel 5 output/capture input. |
| EQEI0 | EQEI0_A | I | EQEI0 phase A input. |
| | EQEI0_B | I | EQEI0 phase B input. |
| | EQEI0_INDEX | I | EQEI0 index input. |
| EQEI1 | EQEI1_A | I | EQEI1 phase A input. |
| | EQEI1_B | I | EQEI1 phase B input. |
| | EQEI1_INDEX | I | EQEI1 index input. |
| I2C0 | I2C0_SCL | I/O | I2C0 clock pin. |
| | I2C0_SDA | I/O | I2C0 data input/output pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | I2C0_SMBAL | O | I2C0 SMBus SMBALTER pin |
| | I2C0_SMBSUS | O | I2C0 SMBus SMBSUS pin (PMBus CONTROL pin) |
| I2C1 | I2C1_SCL | I/O | I2C1 clock pin. |
| | I2C1_SDA | I/O | I2C1 data input/output pin. |
| | I2C1_SMBAL | O | I2C1 SMBus SMBALTER pin |
| | I2C1_SMBSUS | O | I2C1 SMBus SMBSUS pin (PMBus CONTROL pin) |
| I2C2 | I2C2_SCL | I/O | I2C2 clock pin. |
| | I2C2_SDA | I/O | I2C2 data input/output pin. |
| | I2C2_SMBAL | O | I2C2 SMBus SMBALTER pin |
| | I2C2_SMBSUS | O | I2C2 SMBus SMBSUS pin (PMBus CONTROL pin) |
| I2C3 | I2C3_SCL | I/O | I2C3 clock pin. |
| | I2C3_SDA | I/O | I2C3 data input/output pin. |
| | I2C3_SMBAL | O | I2C3 SMBus SMBALTER pin |
| | I2C3_SMBSUS | O | I2C3 SMBus SMBSUS pin (PMBus CONTROL pin) |
| ICE | ICE_CLK | I | Serial wired debugger clock pin.<br>**Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin. |
| | ICE_DAT | I/O | Serial wired debugger data pin.<br>**Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin. |
| INT0 | INT0 | I | External interrupt 0 input pin. |
| INT1 | INT1 | I | External interrupt 1 input pin. |
| INT2 | INT2 | I | External interrupt 2 input pin. |
| INT3 | INT3 | I | External interrupt 3 input pin. |
| INT4 | INT4 | I | External interrupt 4 input pin. |
| INT5 | INT5 | I | External interrupt 5 input pin. |
| INT6 | INT6 | I | External interrupt 6 input pin. |
| INT7 | INT7 | I | External interrupt 7 input pin. |
| LPADC0 | LPADC0_CH0 | A | Low Power ADC0 channel 0 analog input. |
| | LPADC0_CH1 | A | Low Power ADC0 channel 1 analog input. |
| | LPADC0_CH2 | A | Low Power ADC0 channel 2 analog input. |
| | LPADC0_CH3 | A | Low Power ADC0 channel 3 analog input. |
| | LPADC0_CH4 | A | Low Power ADC0 channel 4 analog input. |
| | LPADC0_CH5 | A | Low Power ADC0 channel 5 analog input. |
| | LPADC0_CH6 | A | Low Power ADC0 channel 6 analog input. |
| | LPADC0_CH7 | A | Low Power ADC0 channel 7 analog input. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | LPADC0_CH8 | A | Low Power ADC0 channel 8 analog input. |
| | LPADC0_CH9 | A | Low Power ADC0 channel 9 analog input. |
| | LPADC0_CH10 | A | Low Power ADC0 channel 10 analog input. |
| | LPADC0_CH11 | A | Low Power ADC0 channel 11 analog input. |
| | LPADC0_CH12 | A | Low Power ADC0 channel 12 analog input. |
| | LPADC0_CH13 | A | Low Power ADC0 channel 13 analog input. |
| | LPADC0_CH14 | A | Low Power ADC0 channel 14 analog input. |
| | LPADC0_CH15 | A | Low Power ADC0 channel 15 analog input. |
| | LPADC0_ST | I | Low Power ADC0 external trigger input pin. |
| LPI2C0 | LPI2C0_SCL | I/O | Low Power I2C0 clock pin. |
| | LPI2C0_SDA | I/O | Low Power I2C0 data input/output pin. |
| LPIO0 | LPIO0 | I | Low Power I/O 0 input pin. |
| LPIO1 | LPIO1 | I | Low Power I/O 1 input pin. |
| LPIO2 | LPIO2 | I | Low Power I/O 2 input pin. |
| LPIO3 | LPIO3 | I | Low Power I/O 3 input pin. |
| LPIO4 | LPIO4 | I | Low Power I/O 4 input pin. |
| LPIO5 | LPIO5 | I | Low Power I/O 5 input pin. |
| LPIO6 | LPIO6 | I | Low Power I/O 6 input pin. |
| LPIO7 | LPIO7 | I | Low Power I/O 7 input pin. |
| LPSPI0 | LPSPI0_CLK | I/O | Low Power SPI0 serial clock pin. |
| | LPSPI0_MISO | I/O | Low Power SPI0 MISO (Master In, Slave Out) pin. |
| | LPSPI0_MOSI | I/O | Low Power SPI0 MOSI (Master Out, Slave In) pin. |
| | LPSPI0_SS | I/O | Low Power SPI0 slave select pin. |
| LPTM0 | LPTM0 | I/O | Low Power Timer0 event counter input/toggle output pin. |
| | LPTM0_EXT | I/O | Low Power Timer0 external capture input/toggle output pin. |
| LPTM1 | LPTM1 | I/O | Low Power Timer1 event counter input/toggle output pin. |
| | LPTM1_EXT | I/O | Low Power Timer1 external capture input/toggle output pin. |
| LPUART0 | LPUART0_RXD | I | Low Power UART0 data receiver input pin. |
| | LPUART0_TXD | O | Low Power UART0 data transmitter output pin. |
| | LPUART0_nCTS | I | Low Power UART0 clear to Send input pin. |
| | LPUART0_nRTS | O | Low Power UART0 request to Send output pin. |
| OPA0 | OPA0_N0 | A | Operational amplifier 0 negative 0 input pin. |
| | OPA0_N1 | A | Operational amplifier 0 negative 1 input pin. |
| | OPA0_O | A | Operational amplifier 0 output pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | OPA0_P0 | A | Operational amplifier 0 positive 0 input pin. |
| | OPA0_P1 | A | Operational amplifier 0 positive 1 input pin. |
| OPA1 | OPA1_N0 | A | Operational amplifier 1 negative 0 input pin. |
| | OPA1_N1 | A | Operational amplifier 1 negative 1 input pin. |
| | OPA1_O | A | Operational amplifier 1 output pin. |
| | OPA1_P0 | A | Operational amplifier 1 positive 0 input pin. |
| | OPA1_P1 | A | Operational amplifier 1 positive 1 input pin. |
| OPA2 | OPA2_N0 | A | Operational amplifier 2 negative 0 input pin. |
| | OPA2_N1 | A | Operational amplifier 2 negative 1 input pin. |
| | OPA2_O | A | Operational amplifier 2 output pin. |
| | OPA2_P0 | A | Operational amplifier 2 positive 0 input pin. |
| | OPA2_P1 | A | Operational amplifier 2 positive 1 input pin. |
| PWM0 | PWM0_BRAKE0 | I | PWM0 Brake 0 input pin. |
| | PWM0_BRAKE1 | I | PWM0 Brake 1 input pin. |
| | PWM0_CH0 | I/O | PWM0 channel 0 output/capture input. |
| | PWM0_CH1 | I/O | PWM0 channel 1 output/capture input. |
| | PWM0_CH2 | I/O | PWM0 channel 2 output/capture input. |
| | PWM0_CH3 | I/O | PWM0 channel 3 output/capture input. |
| | PWM0_CH4 | I/O | PWM0 channel 4 output/capture input. |
| | PWM0_CH5 | I/O | PWM0 channel 5 output/capture input. |
| PWM1 | PWM1_BRAKE0 | I | PWM1 Brake 0 input pin. |
| | PWM1_BRAKE1 | I | PWM1 Brake 1 input pin. |
| | PWM1_CH0 | I/O | PWM1 channel 0 output/capture input. |
| | PWM1_CH1 | I/O | PWM1 channel 1 output/capture input. |
| | PWM1_CH2 | I/O | PWM1 channel 2 output/capture input. |
| | PWM1_CH3 | I/O | PWM1 channel 3 output/capture input. |
| | PWM1_CH4 | I/O | PWM1 channel 4 output/capture input. |
| | PWM1_CH5 | I/O | PWM1 channel 5 output/capture input. |
| QSPI0 | QSPI0_CLK | I/O | Quad SPI0 serial clock pin. |
| | QSPI0_MISO0 | I/O | Quad SPI0 MISO0 (Master In, Slave Out) pin. |
| | QSPI0_MISO1 | I/O | Quad SPI0 MISO1 (Master In, Slave Out) pin. |
| | QSPI0_MOSI0 | I/O | Quad SPI0 MOSI0 (Master Out, Slave In) pin. |
| | QSPI0_MOSI1 | I/O | Quad SPI0 MOSI1 (Master Out, Slave In) pin. |
| | QSPI0_SS | I/O | Quad SPI0 slave select pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| SPI0 | SPI0_CLK | I/O | SPI0 serial clock pin. |
| | SPI0_I2SMCLK | I/O | SPI0 I2S master clock output pin |
| | SPI0_MISO | I/O | SPI0 MISO (Master In, Slave Out) pin. |
| | SPI0_MOSI | I/O | SPI0 MOSI (Master Out, Slave In) pin. |
| | SPI0_SS | I/O | SPI0 slave select pin. |
| SPI1 | SPI1_CLK | I/O | SPI1 serial clock pin. |
| | SPI1_I2SMCLK | I/O | SPI1 I2S master clock output pin |
| | SPI1_MISO | I/O | SPI1 MISO (Master In, Slave Out) pin. |
| | SPI1_MOSI | I/O | SPI1 MOSI (Master Out, Slave In) pin. |
| | SPI1_SS | I/O | SPI1 slave select pin. |
| SPI2 | SPI2_CLK | I/O | SPI2 serial clock pin. |
| | SPI2_I2SMCLK | I/O | SPI2 I2S master clock output pin |
| | SPI2_MISO | I/O | SPI2 MISO (Master In, Slave Out) pin. |
| | SPI2_MOSI | I/O | SPI2 MOSI (Master Out, Slave In) pin. |
| | SPI2_SS | I/O | SPI2 slave select pin. |
| SPI3 | SPI3_CLK | I/O | SPI3 serial clock pin. |
| | SPI3_I2SMCLK | I/O | SPI3 I2S master clock output pin |
| | SPI3_MISO | I/O | SPI3 MISO (Master In, Slave Out) pin. |
| | SPI3_MOSI | I/O | SPI3 MOSI (Master Out, Slave In) pin. |
| | SPI3_SS | I/O | SPI3 slave select pin. |
| TAMPER0 | TAMPER0 | I/O | TAMPER detector loop pin 0. |
| TAMPER1 | TAMPER1 | I/O | TAMPER detector loop pin 1. |
| TAMPER2 | TAMPER2 | I/O | TAMPER detector loop pin 2. |
| TK | TK_SE | I/O | Touch key (shielding electrode) |
| | TK_TK0 | I/O | Touch key 0 |
| | TK_TK1 | I/O | Touch key 1 |
| | TK_TK2 | I/O | Touch key 2 |
| | TK_TK3 | I/O | Touch key 3 |
| | TK_TK4 | I/O | Touch key 4 |
| | TK_TK5 | I/O | Touch key 5 |
| | TK_TK6 | I/O | Touch key 6 |
| | TK_TK7 | I/O | Touch key 7 |
| | TK_TK8 | I/O | Touch key 8 |
| | TK_TK9 | I/O | Touch key 9 |

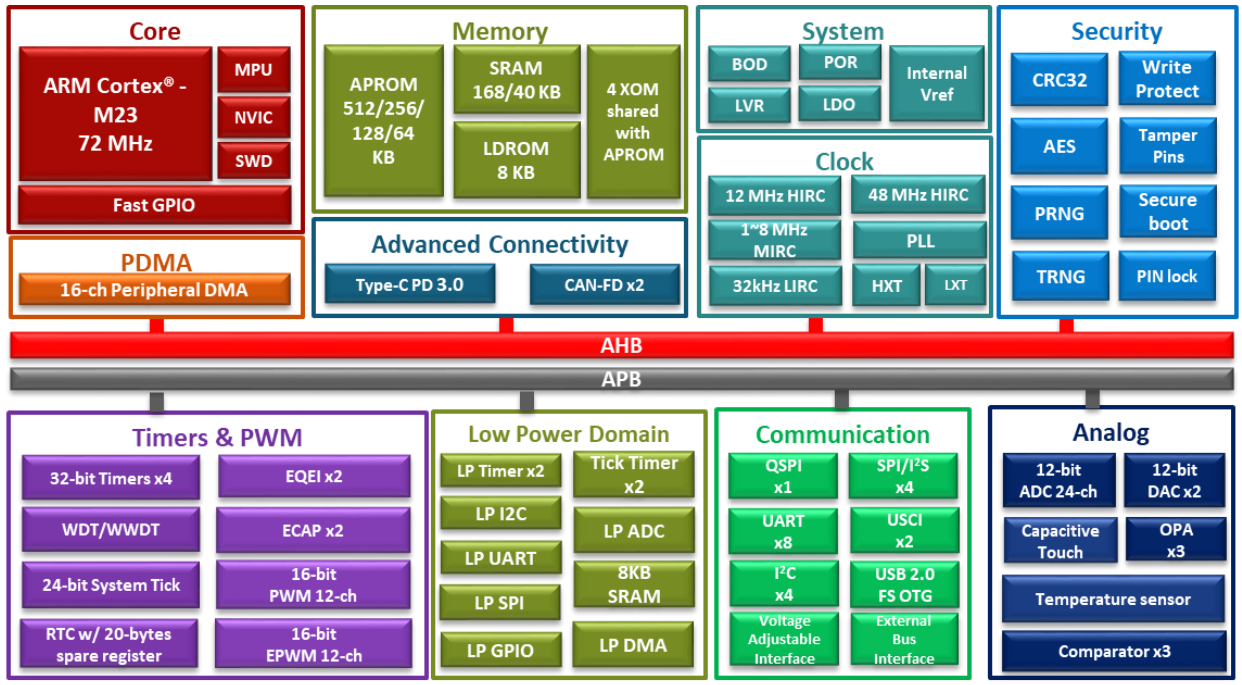
| Group | Pin Name | Type | Description |
|---|---|---|---|
| | TK_TK10 | I/O | Touch key 10 |
| | TK_TK11 | I/O | Touch key 11 |
| | TK_TK12 | I/O | Touch key 12 |
| | TK_TK13 | I/O | Touch key 13 |
| | TK_TK14 | I/O | Touch key 14 |
| | TK_TK15 | I/O | Touch key 15 |
| | TK_TK16 | I/O | Touch key 16 |
| | TK_TK17 | I/O | Touch key 17 |
| TM0 | TM0 | I/O | Timer0 event counter input/toggle output pin. |
| | TM0_EXT | I/O | Timer0 external capture input/toggle output pin. |
| TM1 | TM1 | I/O | Timer1 event counter input/toggle output pin. |
| | TM1_EXT | I/O | Timer1 external capture input/toggle output pin. |
| TM2 | TM2 | I/O | Timer2 event counter input/toggle output pin. |
| | TM2_EXT | I/O | Timer2 external capture input/toggle output pin. |
| TM3 | TM3 | I/O | Timer3 event counter input/toggle output pin. |
| | TM3_EXT | I/O | Timer3 external capture input/toggle output pin. |
| UART0 | UART0_RXD | I | UART0 data receiver input pin. |
| | UART0_TXD | O | UART0 data transmitter output pin. |
| | UART0_nCTS | I | UART0 clear to Send input pin. |
| | UART0_nRTS | O | UART0 request to Send output pin. |
| UART1 | UART1_RXD | I | UART1 data receiver input pin. |
| | UART1_TXD | O | UART1 data transmitter output pin. |
| | UART1_nCTS | I | UART1 clear to Send input pin. |
| | UART1_nRTS | O | UART1 request to Send output pin. |
| UART2 | UART2_RXD | I | UART2 data receiver input pin. |
| | UART2_TXD | O | UART2 data transmitter output pin. |
| | UART2_nCTS | I | UART2 clear to Send input pin. |
| | UART2_nRTS | O | UART2 request to Send output pin. |
| UART3 | UART3_RXD | I | UART3 data receiver input pin. |
| | UART3_TXD | O | UART3 data transmitter output pin. |
| | UART3_nCTS | I | UART3 clear to Send input pin. |
| | UART3_nRTS | O | UART3 request to Send output pin. |
| UART4 | UART4_RXD | I | UART4 data receiver input pin. |
| | UART4_TXD | O | UART4 data transmitter output pin. |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | UART4_nCTS | I | UART4 clear to Send input pin. |
| | UART4_nRTS | O | UART4 request to Send output pin. |
| UART5 | UART5_RXD | I | UART5 data receiver input pin. |
| | UART5_TXD | O | UART5 data transmitter output pin. |
| | UART5_nCTS | I | UART5 clear to Send input pin. |
| | UART5_nRTS | O | UART5 request to Send output pin. |
| UART6 | UART6_RXD | I | UART6 data receiver input pin. |
| | UART6_TXD | O | UART6 data transmitter output pin. |
| | UART6_nCTS | I | UART6 clear to Send input pin. |
| | UART6_nRTS | O | UART6 request to Send output pin. |
| UART7 | UART7_RXD | I | UART7 data receiver input pin. |
| | UART7_TXD | O | UART7 data transmitter output pin. |
| | UART7_nCTS | I | UART7 clear to Send input pin. |
| | UART7_nRTS | O | UART7 request to Send output pin. |
| USB | USB_D+ | A | USB differential signal D+. |
| | USB_D- | A | USB differential signal D-. |
| | USB_OTG_ID | I | USB_ identification. |
| | USB_VBUS | P | Power supply from USB host or HUB. |
| | USB_VBUS_EN | O | USB external VBUS regulator enable pin. |
| | USB_VBUS_ST | I | USB external VBUS regulator status pin. |
| USCI0 | USCI0_CLK | I/O | USCI0 clock pin. |
| | USCI0_CTL0 | I/O | USCI0 control 0 pin. |
| | USCI0_CTL1 | I/O | USCI0 control 1 pin. |
| | USCI0_DAT0 | I/O | USCI0 data 0 pin. |
| | USCI0_DAT1 | I/O | USCI0 data 1 pin. |
| USCI1 | USCI1_CLK | I/O | USCI1 clock pin. |
| | USCI1_CTL0 | I/O | USCI1 control 0 pin. |
| | USCI1_CTL1 | I/O | USCI1 control 1 pin. |
| | USCI1_DAT0 | I/O | USCI1 data 0 pin. |
| | USCI1_DAT1 | I/O | USCI1 data 1 pin. |
| UTCPD0 | UTCPD0_CC1 | A | UTCPD0 USB Type-C Configuration Channel pin 1 |
| | UTCPD0_CC2 | A | UTCPD0 USB Type-C Configuration Channel pin 2 |
| | UTCPD0_CCDB1 | A | UTCPD0 USB Type-C Configuration Channel pin D |
| | UTCPD0_CCDB2 | A | UTCPD0 USB Type-C Configuration Channel pin D |

| Group | Pin Name | Type | Description |
|---|---|---|---|
| | UTCPD0_DISCHG | O | UTCPD0 VCONN Discharge Enable output pin |
| | UTCPD0_FRSTX1 | O | UTCPD0 CC1 Fast Role Swap Transmit output pin |
| | UTCPD0_FRSTX2 | O | UTCPD0 CC2 Fast Role Swap Transmit output pin |
| | UTCPD0_VBDCHG | O | UTCPD0 VBUS Discharge Enable output pin |
| | UTCPD0_VBSNKEN | O | UTCPD0 VBUS Sink Enable output pin |
| | UTCPD0_VBSRCEN | O | UTCPD0 VBUS Source Enable output pin |
| | UTCPD0_VCNEN1 | O | UTCPD0 CC1 VCONN Enable output pin |
| | UTCPD0_VCNEN2 | O | UTCPD0 CC2 VCONN Enable output pin |
| X32 | X32_IN | I | External 32.768 kHz crystal input pin. |
| | X32_OUT | O | External 32.768 kHz crystal output pin. |
| XT1 | XT1_IN | I | External 4~24 MHz (high speed) crystal input pin. |
| | XT1_OUT | O | External 4~24 MHz (high speed) crystal output pin. |
| Power | $AV_{DD}$ | P | Power supply for internal analog circuit. |
| | $AV_{SS}$ | P | Ground pin for analog circuit. |
| | LDO_CAP | A | LDO output pin.<br>**Note:** This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet. |
| | $V_{BAT}$ | P | Power supply by batteries for RTC. |
| | $V_{DD}$ | P | Power supply for I/O ports and LDO source for internal PLL and digital circuit. |
| | $V_{DDIO}$ | P | Power supply for PA.0~PA.5. |
| | $V_{REF}$ | A | ADC reference voltage input.<br>**Note:** This pin needs to be connected with a 1uF capacitor. |
| | $V_{SS}$ | P | Ground pin for digital circuit. |
| | nRESET | I | External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.<br>**Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin. |

# 5 BLOCK DIAGRAM

## 5.1 M2L31 Series Block Diagram



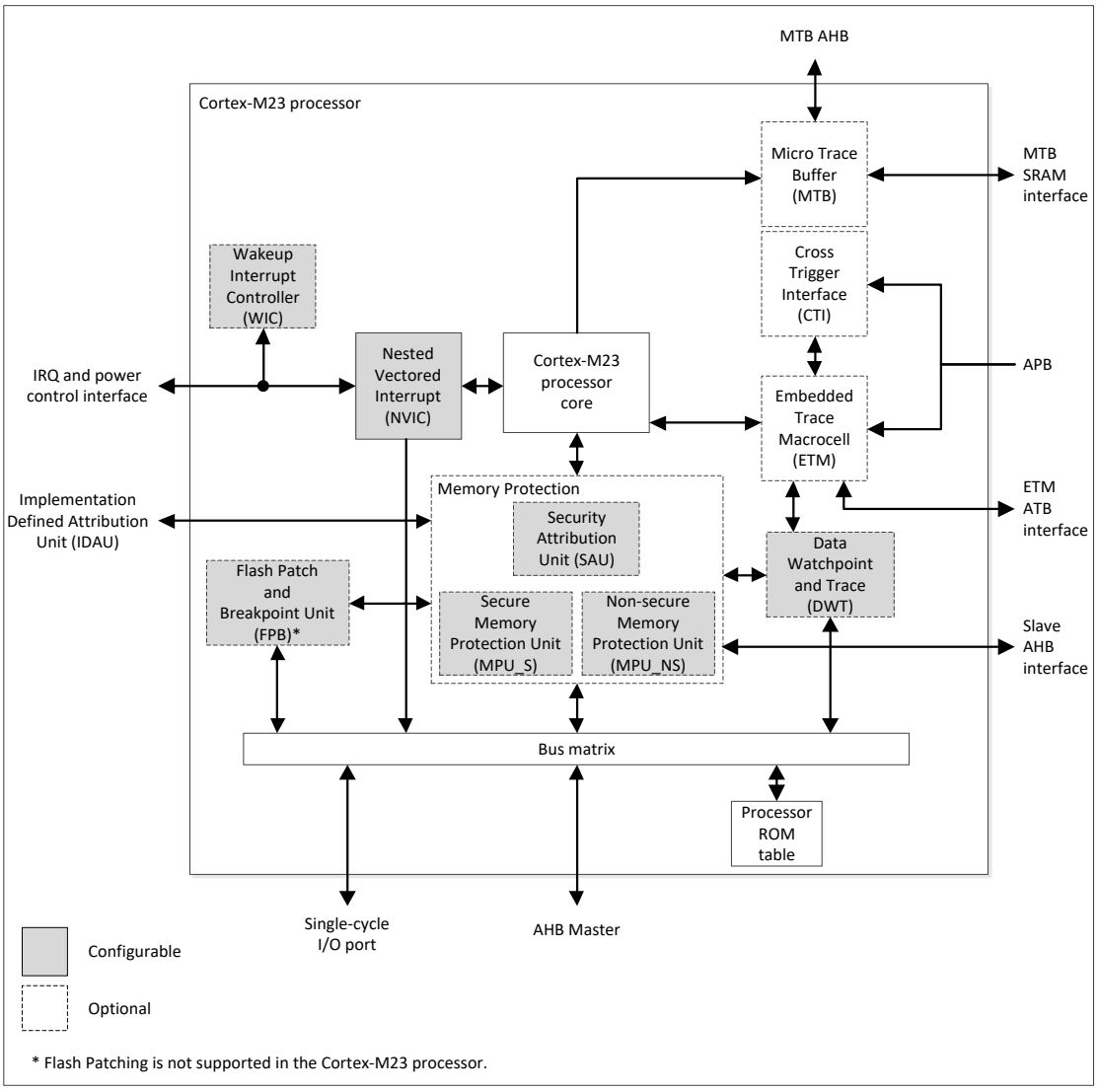

Please refer to the selection guide in section 4.2 for detailed information.

Figure 6.2-1 M2L31 Series Block Diagram

# 6 FUNCTIONAL DESCRIPTION

## 6.1 Arm Cortex-M23 Core

The Cortex-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro M2L31 is embedded with Cortex-M23 processor.Figure 6.2-1 shows the functional controller of the processor.




**Note:** The M2L31 does not support security attribution unit, ETM, CTI and MTB function.

Figure 6.2-1 Cortex-M23 Block Diagram

***Cortex-M23 processor features:***

- Armv8-M Baseline architecture.
- Armv8-M Baseline Thumb-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced ReRAM and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Protected Memory System Architecture (PMSAv8) Memory Protection Units (MPUs) for both Secure and Non-secure states.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

## 6.2 System Manager

### 6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

### 6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M23 core only by writing 1 to CPURST (SYS_IPRST0[1])

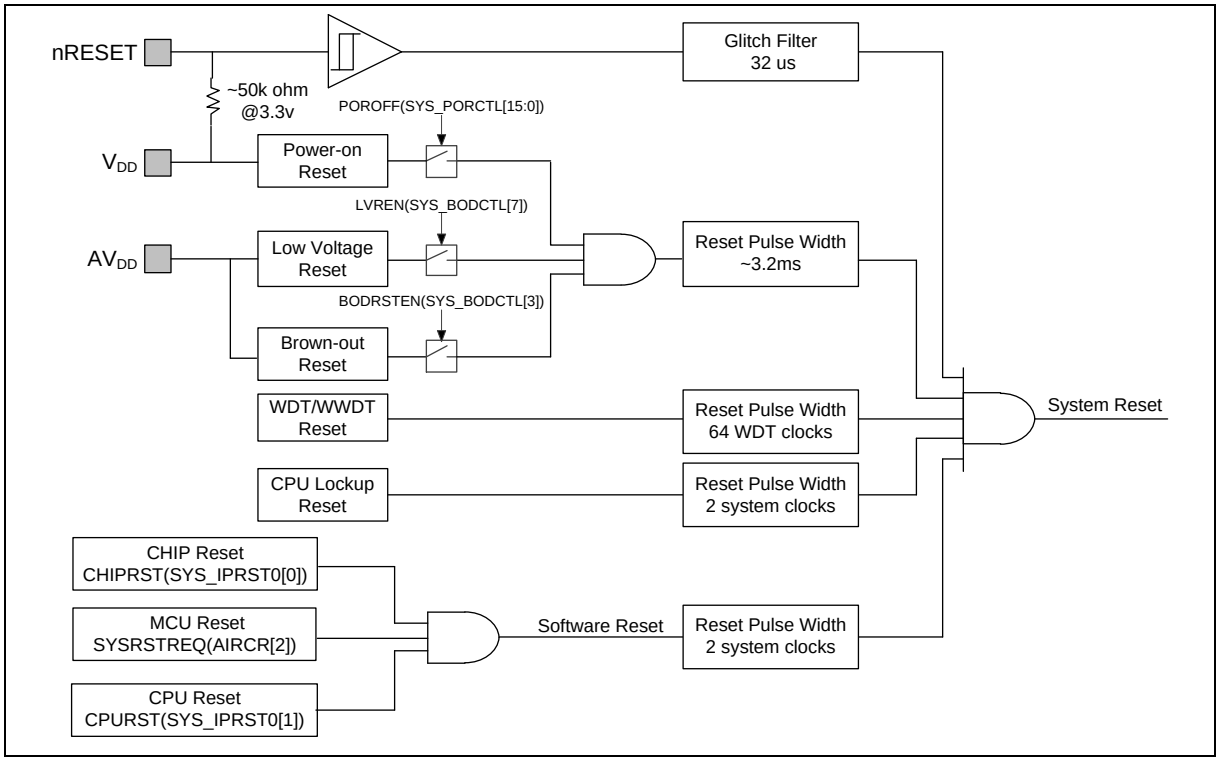



Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M23 only; the other reset sources will reset Cortex-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

| Reset Sources<br>Register | POR | nRESET | WDT | LVR | BOD | Lockup | CHIP | MCU | CPU |
|---|---|---|---|---|---|---|---|---|---|
| SYS_RSTSTS | Bit 0 = 1 | Bit 1 = 1 | Bit 2 = 1 | Bit 3 = 1 | Bit 4 = 1 | Bit 8 = 1 | Bit 0 = 1 | Bit 5 = 1 | Bit 7 = 1 |
| CHIPRST<br>(SYS_IPRST0[0]) | 0x0 | - | - | - | - | - | - | - | - |
| BODEN<br>(SYS_BODCTL[0]) | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - |
| BODVL<br>(SYS_BODCTL[2:1]) | | | | | | | | | |
| BODRSTEN<br>(SYS_BODCTL[3]) | | | | | | | | | |
| LXTEN<br>(CLK_PWRCTL[1]) | 0x0 | - | - | - | - | - | - | - | - |
| WDTCKEN<br>(CLK_APBCLK0[0]) | 0x1 | - | 0x1 | - | - | - | 0x1 | - | - |
| WDTSEL<br>(CLK_CLKSEL1[1:0]) | 0x3 | 0x3 | - | - | - | - | - | - | - |
| HXTSTB | 0x0 | - | - | - | - | - | - | - | - |

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| (CLK_STATUS[0]) | | | | | | | | | |
| LXTSTB<br>(CLK_STATUS[1]) | 0x0 | - | - | - | - | - | - | - | - |
| PLLSTB<br>(CLK_STATUS[2]) | 0x0 | - | - | - | - | - | - | - | - |
| HIRCSTB<br>(CLK_STATUS[4]) | 0x0 | - | - | - | - | - | - | - | - |
| CLKSFAIL<br>(CLK_STATUS[7]) | 0x0 | 0x0 | - | - | - | - | - | - | - |
| RSTEN<br>(WDT_CTL[1])<br>WDTEN<br>(WDT_CTL[7]) | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| WDT_CTL<br>except bit 1 and bit 7. | 0x0700 | 0x0700 | 0x0700 | 0x0700 | 0x0700 | - | 0x0700 | - | - |
| WDT_ALTCTL | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| WWDT_RLDCNT | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| WWDT_CTL | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | 0x3F0800 | - | 0x3F0800 | - | - |
| WWDT_STATUS | 0x0000 | 0x0000 | 0x0000 | 0x0000 | 0x0000 | - | 0x0000 | - | - |
| WWDT_CNT | 0x3F | 0x3F | 0x3F | 0x3F | 0x3F | - | 0x3F | - | - |
| BS<br>(RMC_ISPCTL[1]) | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| DFBA<br>(RMC_DFBA[31:0]) | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | Reload from CONFIG1 | - | Reload from CONFIG1 | - | - |
| CBS<br>(RMC_ISPSTS[2]) | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | Reload from CONFIG0 | - | Reload from CONFIG0 | - | - |
| VECMAP<br>(RMC_ISPSTS[23:9]) | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | Reload base on CONFIG0 | - | Reload base on CONFIG0 | - | - |
| SCACT<br>(RMC_SCACT[0]) | 0x0 | 0x0 | 0x0 | 0x0 | 0x0 | - | 0x0 | - | - |
| Other Peripheral Registers | Reset Value | | | | | | | | - |
| RMC Registers | Reset Value | | | | | | | | |
| **Note:** '-' means that the value of register keeps original setting. | | | | | | | | | |

Table 6.2-1 Reset Value of Registers

### *6.2.2.1 nRESET Reset*

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an

asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.3 $V_{DD}$ and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 $V_{DD}$ and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

**Note:** Please refer to the datasheet for $T_{RP}$ value.

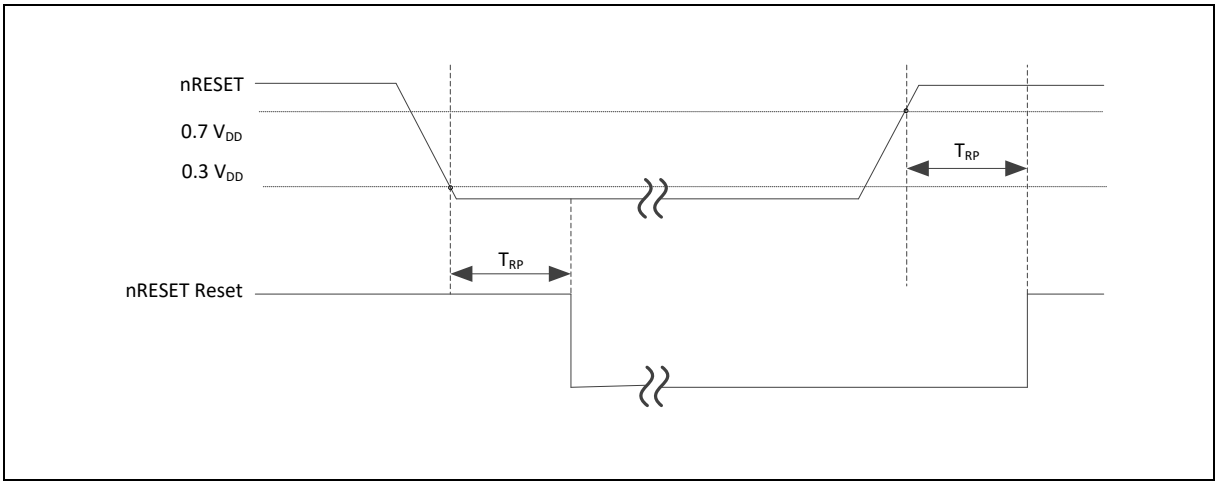



Figure 6.2-2 nRESET Reset Waveform

### *6.2.2.2 Power-on Reset (POR)*

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

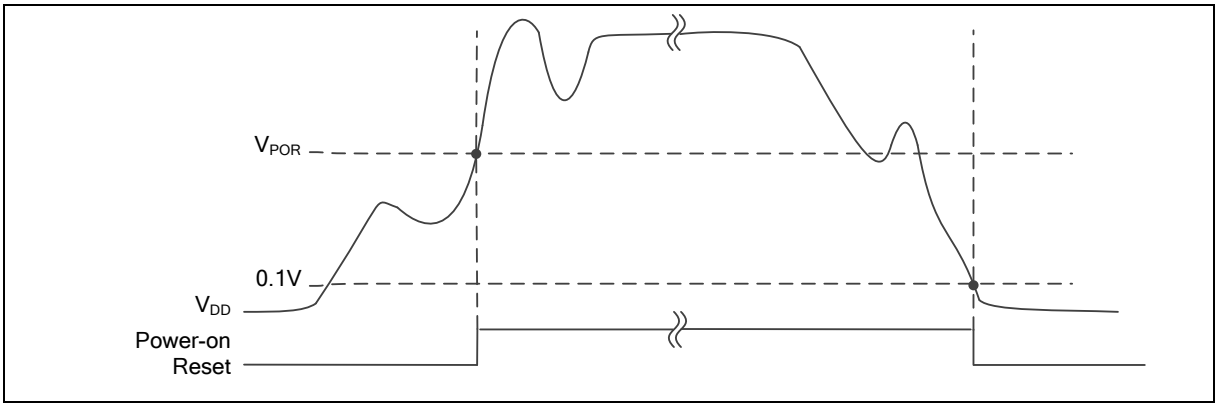



Figure 6.2-3 Power-on Reset (POR) Waveform

### *6.2.2.3 Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN

(SYS_BODCTL[7]) to 1, after 100us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the $AV_{DD}$ voltage rises above $V_{LVR}$ and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

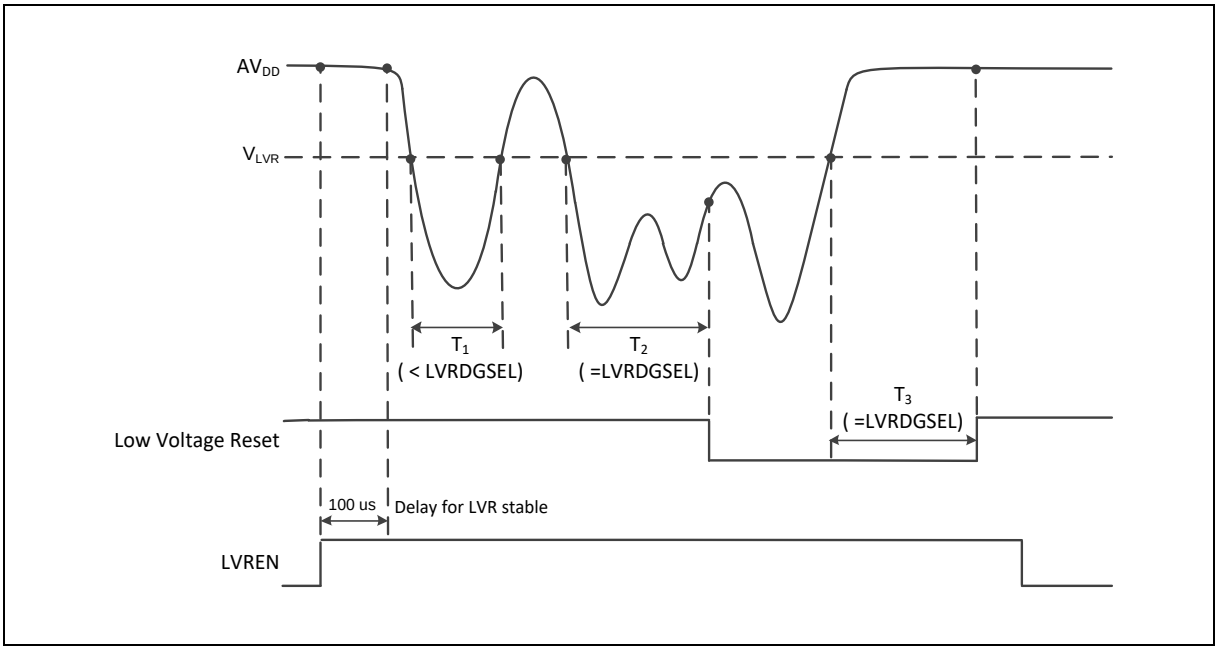



Figure 6.2-4 Low Voltage Reset (LVR) Waveform

### *6.2.2.4 Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect $AV_{DD}$ during system operation. When the $AV_{DD}$ voltage is lower than $V_{BOD}$ which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the $AV_{DD}$ voltage rises above $V_{BOD}$ and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by RRAM controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

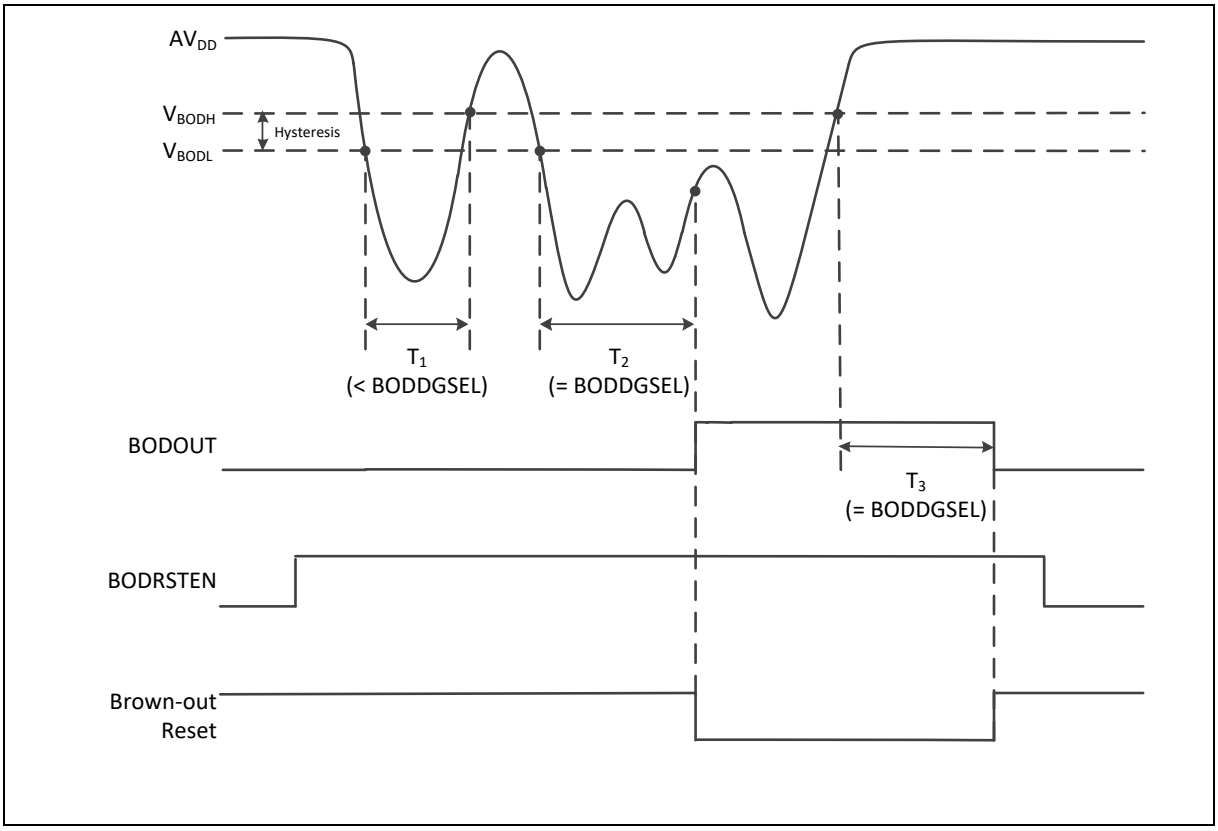



Figure 6.2-5 Brown-out Detector (BOD) Waveform

#### *6.2.2.5 Watchdog Timer Reset (WDT)*

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

#### *6.2.2.6 CPU Lockup Reset*

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

#### *6.2.2.7 CPU Reset, CHIP Reset and MCU Reset*

The CPU Reset means only Cortex-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(RMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(RMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

### 6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from $AV_{DD}$ and $AV_{SS}$ provides the power for analog components operation.
- Digital power from $V_{DD}$ and $V_{SS}$ supplies the power to the internal regulator for digital operation and I/O pins.
- I/O power from $V_{DDIO}$ supplies the power for PA.0 ~ PA.5
- RTC power from $V_{BAT}$ provides the power for RTC and 80 bytes backup registers.

The output of internal voltage regulators, LDO_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power ($AV_{DD}$) should be the same voltage level of the digital power ($V_{DD}$). Figure 6.2-6 shows the NuMicro M2L31 power distribution. In Figure 6.2-6, the block of Low Power Digital Logic includes LPPDMA, LPGPIO, LPADC, LPI2C, LPSPI, LPUART, LPTMR, TTMR, WDT and OPA peripherals.

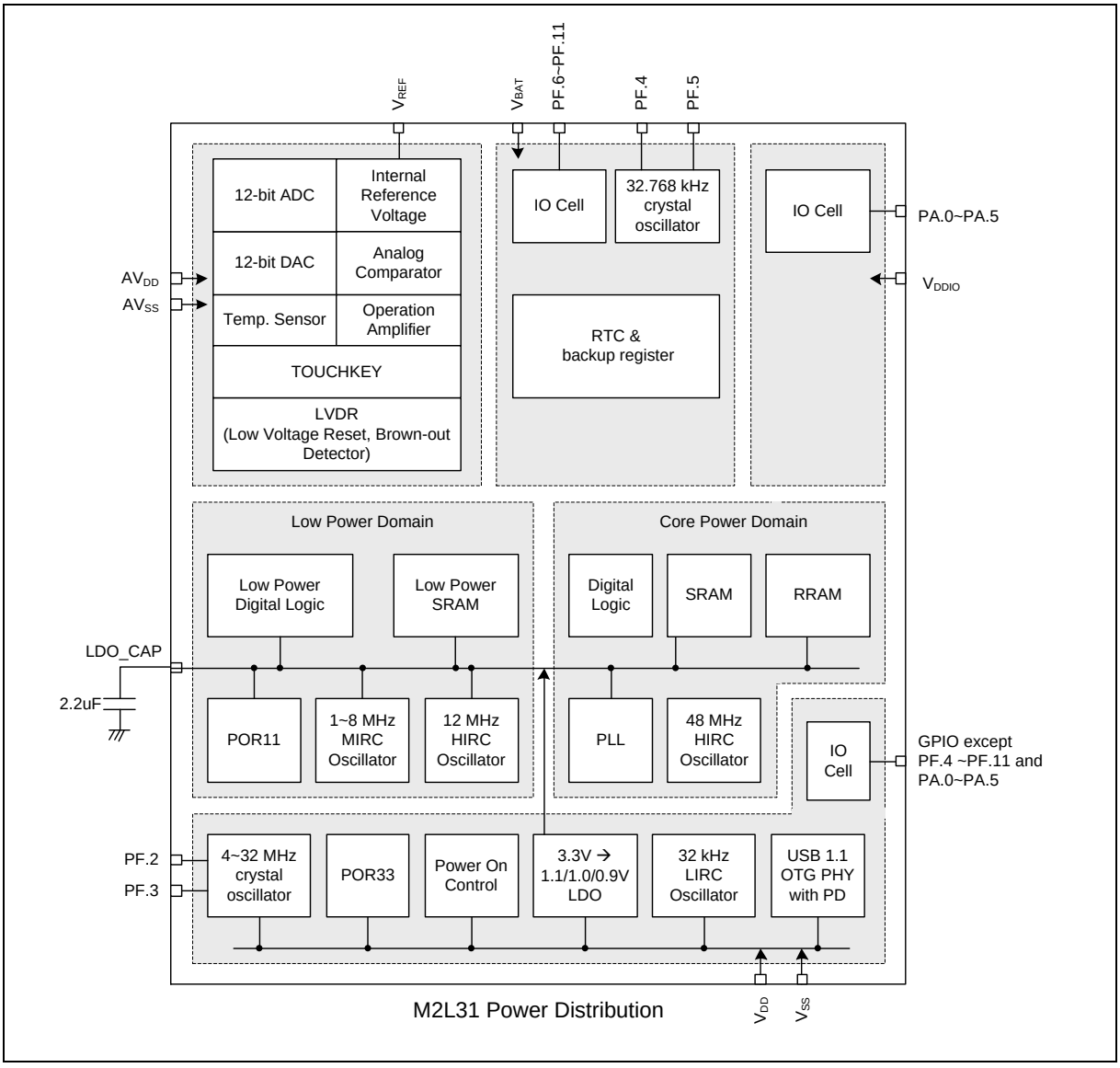



Figure 6.2-6 NuMicro M2L31 Power Distribution Diagram

### 6.2.4 Power Modes and Wake-up Sources

The NuMicro M2L31 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode at NuMicro M2L31 series.

| Mode | CPU Status | LDO_CAP (V) | Clock Status |
|---|---|---|---|
| PL1 run mode | Normal Run | 1.1 | All clocks can be disabled by control register. |
| Idle mode | Sleep mode | 1.1 | Only CPU clock is disabled. |
| Normal Power-down mode 0 (NPD0) | Deep Sleep mode | 1.1 | Most clocks are disabled except HIRC/MIRC/LIRC/LXT.<br>RTC, TMR, UART and low power domain peripherals could be active if HIRC/MIRC/LIRC/LXT are selected as clock sources. |
| Normal Power-down mode 1 (NPD1) | Deep Sleep mode | 1.1 | Most clocks are disabled except HIRC/MIRC/LIRC/LXT.<br>RTC, TMR, UART and low power domain peripherals could be active if HIRC/MIRC/LIRC/LXT are selected as clock sources. |
| Normal Power-down mode 2 (NPD2) | Deep Sleep mode | 0.9 | Most clocks are disabled except HIRC/MIRC/LIRC/LXT.<br>RTC, TMR, UART and low power domain peripherals could be active if HIRC/MIRC/LIRC/LXT are selected as clock sources. |
| Normal Power-down mode 3 (NPD3) | Power off | 1.1 | Most clocks are disabled except HIRC/MIRC/LIRC/LXT.<br>RTC and low power domain peripherals could be active if HIRC/MIRC/LIRC/LXT are selected as clock sources. |
| Normal Power-down mode 4 (NPD4) | Power off | 0.9 | Most clocks are disabled except HIRC/MIRC/LIRC/LXT.<br>RTC and low power domain peripherals could be active if HIRC/MIRC/LIRC/LXT are selected as clock sources. |
| Normal Power-down mode 5 (NPD5) | Power off | 0.7 | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |
| Standby Power-down mode 0 (SPD0) | Power off | 1.1 | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |
| Standby Power-down mode 1 (SPD1) | Power off | 0.9 | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |
| Standby Power-down mode 2 (SPD2) | Power off | 0.7 | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |
| Deep Power-down mode 0 (DPD0) | Power off | Floating | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |
| Deep Power-down mode 1 (DPD1) | Power off | Floating | LXT is enabled for RTC function and LIRC is enabled for wake-up timer usage. |

Table 6.2-2 Power Mode Table

| Mode | Core Power Domain AHB/APB Bus Maximum Speed (MHz (HCLK0/PCLK0/PCLK1) | Low Power Domain AHB/APB Bus Maximum Speed (MHz) (HCLK1/PCLK2) |
|---|---|---|
| PL1 run mode | 72 | 24 |
| NPD0 mode | Off | 12 |
| NPD1 mode | Off | 12 |
| NPD2 mode | Off | 4 |
| NPD3 mode | Off | 12 |
| NPD4 mode | Off | 4 |
| NPD5 mode | Off | Off |

Table 6.2-3 AHB/APB Bus maximum speed under different Power Modes

Table 6.2-3 shows the maximum speed of AHB/APB bus in Core Power and Low Power domain, different power mode.

There are different power mode entry setting. For each power mode, they have different entry setting and leaving condition. Table 6.2-4 shows the entry setting for each power mode. When chip power-on, chip is running at normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

| Register/Instruction Mode | SLEEPDEEP (SCR[2]) | PDEN (CLK_PWRCTL[7]) | PDMSEL (CLK_PMUCTL[2:0]) | CPU Run WFI Instruction |
|---|---|---|---|---|
| Normal mode | 0 | 0 | 0 | NO |
| Idle mode | 0 | 0 | 0 | YES |
| Normal Power-down mode 0 (NPD0) | 1 | 1 | 0 | YES |
| Normal Power-down mode 1 (NPD1) | 1 | 1 | 1 | YES |
| Normal Power-down mode 2 (NPD2) | 1 | 1 | 2 | YES |
| Normal Power-down mode 3 (NPD3) | 1 | 1 | 3 | YES |
| Normal Power-down mode 4 (NPD4) | 1 | 1 | 4 | YES |
| Normal Power-down mode 5 (NPD5) | 1 | 1 | 5 | YES |
| Standby Power-down mode 0 (SPD0) | 1 | 1 | 8 | YES |
| Standby Power-down mode 1 (SPD1) | 1 | 1 | 9 | YES |
| Standby Power-down mode 2 (SPD2) | 1 | 1 | 10 | YES |
| Deep Power-down mode 0 (DPD0) | 1 | 1 | 12 | YES |
| Deep Power-down mode 1 (DPD1) | 1 | 1 | 13 | YES |

Table 6.2-4 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-5 lists the available clocks for each power mode. When chip wake-up from standby Power-down mode 0/1/2 (SPD0/1/2) or deep Power-down mode 0/1 (DPD0/1), the CPU will be reset and start running.

| Power Mode | Normal Mode | Idle Mode | Power-Down Mode |
|---|---|---|---|
| Definition | CPU is in active state | CPU is in sleep state | CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended. |
| Entry Condition | Chip is in normal mode after system reset released | CPU executes WFI instruction. | CPU sets sleep mode enable and power down enable and executes WFI instruction. |
| Wake-up Sources | N/A | All interrupts | RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI, USBD, ACMP and BOD. |
| Available Clocks | All | All except CPU clock | LXT and LIRC |
| After Wake-up | N/A | CPU back to normal mode | CPU back to normal mode |

Table 6.2-5 Power Mode Definition Table

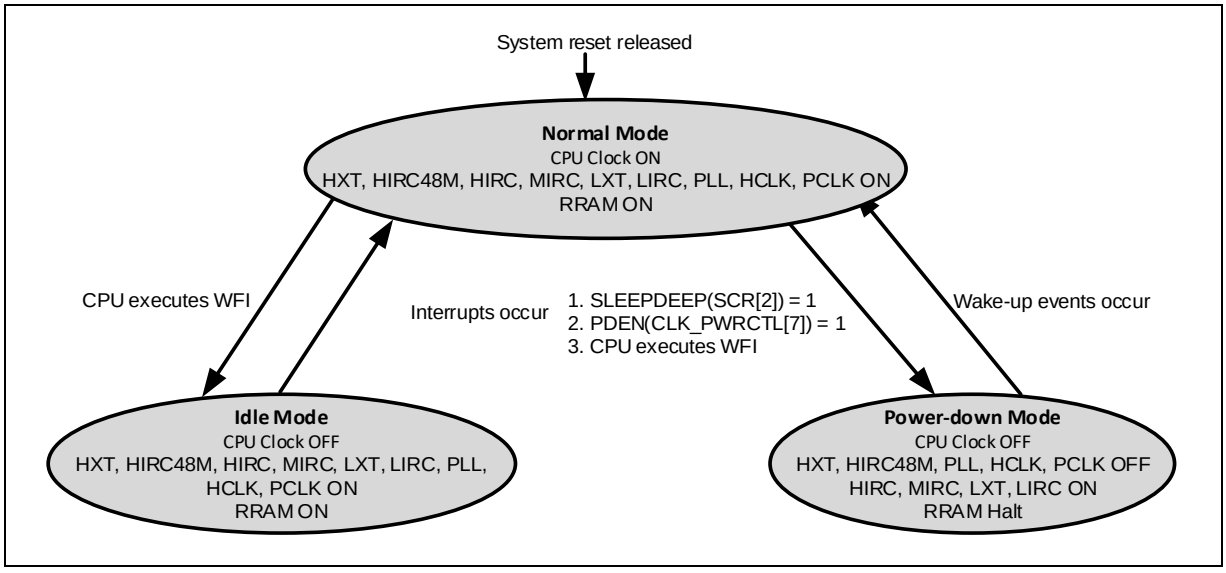



Figure 6.2-7 Power Mode State Machine

| Clocks | Idle Mode | NPD0, NPD1,NPD2 | NPD3, NPD4 | NPD5, SPD0~2 | DPD0, DPD1 |
|---|---|---|---|---|---|
| HXT | ON/OFF | Halt | Halt | Halt | Halt |
| HIRC48M | ON/OFF | Halt | Halt | Halt | Halt |
| HIRC | ON/OFF | ON/OFF[1] | ON/OFF[1] | Halt | Halt |
| MIRC | ON/OFF | ON/OFF[1] | ON/OFF[1] | Halt | Halt |
| LXT | ON/OFF | ON/OFF[1] | ON/OFF[1] | ON/OFF[1] | ON/OFF[1] |
| LIRC | ON/OFF | ON/OFF[1] | ON/OFF[1] | ON/OFF[1] | ON/OFF[1],[6] |
| PLL | ON/OFF | Halt | Halt | Halt | Halt |
| HCLK0/PCLK0/PCLK1 | ON | Halt | Halt | Halt | Halt |
| HCLK1/PCLK2 | ON/OFF | ON/OFF | ON/OFF | Halt | Halt |
| CPU | Halt | Halt | Halt | Halt | Halt |
| SRAM | ON | Halt | Halt | Halt | Halt |
| LPSRAM | ON/OFF | ON/OFF | ON/OFF | Halt | Halt |
| RRAM | ON | Halt | Halt | Halt | Halt |
| TIMER | ON | ON/OFF[2] | Halt | Halt | Halt |
| WDT | ON | ON/OFF[3] | ON/OFF[3] | Halt | Halt |
| RTC | ON | ON/OFF[4] | ON/OFF[4] | ON/OFF[4] | ON/OFF[4] |
| UART | ON | ON/OFF[5] | Halt | Halt | Halt |
| Low power domain peripherals | ON | ON/OFF[7] | ON/OFF[7] | Halt | Halt |
| Others | ON | Halt | Halt | Halt | Halt |

Table 6.2-6 Clocks in Power Modes

**Note:**

1. HIRC, MIRC, LXT, LIRC ON or OFF depends on SOFTWARE setting in normal mode.
2. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is enabled.
3. If WDT clock source is selected as LIRC and LIRC is enabled.
4. If RTC clock source is selected as LXT and LXT is enabled.
5. If UART clock source is selected as LXT and LXT is enabled.
6. If timer wake up function is disabled, LIRC will be disabled automatically when chip enter DPD0~1 mode for power saving.
7. If low power domain peripherals clock sources are selected as HIRC/MIRC/LIRC/LXT and HIRC/MIRC/LIRC/LXT are enabled.

***Wake-up/Reset-Wake-up sources in each power-down mode :***

After chip enters power down, the following wake-up sources can wake up chip to normal mode. Table 6.2-7 lists the condition about how to enter Power-down mode again for each peripheral. User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

| Wake-Up/ Reset-Wake-up Source | Wake-Up/ Reset-Wake-up Condition | Power-Down Mode | | | | Re-Entering Power-Down Mode Condition |
|---|---|---|---|---|---|---|
| | | NPD0/ NPD1/ NPD2 | NPD3/ NPD4 | NPD5/ SPD0/ SPD1/ SPD2 | DPD0/ DPD1 | |
| RST pin (Reset-Wake-up) | RST pin Reset 3x us debounce | V | - | - | - | After software writes 1 to clear PINF (SYS_RSTSTS[1]) |
| | RST pin Reset 300ns debounce | - | V | V | V | After software writes 1 (CLK_PMUSTS[31]) to clear RSTWK (CLK_PMUSTS[15]) when NPD3 or NPD4 or NPD5 or SPD0~2 or DPD0~1 mode is entered. |
| RTC | Wakeup by RTC alarm | V | V | V | V | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD0~1 or SPD0~2 mode is entered. |
| | Wakeup by RTC tick time | V | V | V | V | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD0~1 or SPD0~2 mode is entered. |
| | Wakeup by tamper event | V | V | V | V | After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD0~1 or SPD0~2 mode is entered. |
| WKTMR | Wakeup by wake-up timer time-out | V | V | V | V | After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when power down mode is entered. |
| BOD (Wake-up/ Reset-Wake-up) | Brown-Out Detector Reset / Interrupt | V | - | - | - | After software writes 1 to clear BODIF (SYS_BODCTL[4]). |
| | Brown-Out Detector Reset / Wake-up | - | V | V | - | After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD0~2 mode is entered. |
| LVR (Reset-Wake-up) | LVR Reset | V | - | - | - | After software writes 1 to clear LVRF (SYS_RSTSTS[3]) |
| | | - | V | V | - | After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD0~2 mode is entered. |
| POR (Reset-Wake-up) | POR Reset | V | V | V | V | After software writes 1 to clear PORF (SYS_RSTSTS[0]) |
| ACMP | Comparator Power-Down Wake-Up Interrupt | V | V | - | - | After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]) and WKIF2 (ACMP_STATUS2[8]) |
| | ACMPO status change | - | - | V | - | After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWK (CLK_PMUSTS[18:16]) when SPD0~2 mode is entered. |
| OPA | Digital output change state | V | V | - | - | After software writes 1 to clear OPDOWKFx (OPA_STATUS [10:8]) and OPDOIFx |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | | | | (OPA_STATUS [6:4]). |
| GPIO | GPIO Interrupt | V | - | - | - | After software write 1 to clear the Px_INTSRC[n] bit. |
| WKIOx (PA~PD) | rising or falling edge event, 64-pin | V | V | V | - | After software writes 1 (CLK_PMUSTS[31]) to clear GPxWKx (CLK_PMUSTS[27:24], CLK_PMUSTS[11:8) when NPD0~5/SPD0~2 mode is entered. |
| WKPINx (PC.0/PB.0/PB.2 /PB.12/PF.6/PA.12 ) | rising or falling edge event, 6-pins | - | - | - | V | After software writes 1 (CLK_PMUSTS[31]) to clear WKPINx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD0~1 mode is entered. |
| EINT | GPIO Interrupt | V | - | - | - | After software write 1 to clear the Px_INTSRC[n] bit. |
| WDT (Wake-up/ Reset-Wake-up) | WDT Wake-up with Interrupt/ Reset-Wake-up | V | V | - | - | After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect). |
| TIMER | Timer Interrupt | V | - | - | - | After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]). |
| | PWM PIF Interrupt | V | | | | After software writes 1 to clear PWMINTWKF (TIMERx_PWMSTATUS[8]) and PIF (TIMERx_PWMINTSTS0[1]). |
| | PWM CMPUIF Interrupt | V | | | | After software writes 1 to clear PWMINTWKF (TIMERx_PWMSTATUS[8]) and CMPUIF (TIMERx_PWMINTSTS0[2]). |
| | PWM Interrupt Accumulator | V | | | | After software writes 1 to clear PWMINTWKF (TIMERx_PWMSTATUS[8]) and IFAIF (TIMERx_PWMAINTSTS[0]). |
| LPTIMER | Timer Interrupt | V | V | - | - | After software writes 1 to clear TWKF (LPTMRx_INTSTS[1]) and TIF (LPTMRx_INTSTS[0]). |
| | PWM PIF Interrupt | V | V | | | After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and PIF (LPTMRx_PWMINTSTS0[1]). |
| | PWM CMPUIF Interrupt | V | V | | | After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and CMPUIF (LPTMRx_PWMINTSTS0[2]). |
| | PWM Interrupt Accumulator | V | V | | | After software writes 1 to clear PWMINTWKF (LPTMRx_PWMSTATUS[8]) and IFAIF (LPTMRx_PWMAINTSTS[0]). |
| TTMR | Timer Time-out Interrupt | V | V | - | - | After software writes 1 to clear TWKF (TTMRx_INTSTS[1]) and TIF (TTMRx_INTSTS[0]). |
| UART | nCTS wake-up | V | - | - | - | After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]). |
| | RX Data wake-up | V | - | - | - | After software writes 1 to clear DATWKF (UARTx_WKSTS[1]). |
| | Received FIFO Threshold Wake-up | V | - | - | - | After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]). |
| | RS-485 AAD Mode Wake-up | V | - | - | - | After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]). |
| | Received FIFO Threshold Time-out | V | - | - | - | After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]). |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Wake-up | | | | | |
| LPUART | nCTS wake-up | V | V | - | - | After software writes 1 to clear CTSWKF (LPUARTx_WKSTS[0]). |
| | RX Data wake-up | V | V | - | - | After software writes 1 to clear DATWKF (LPUARTx_WKSTS[1]). |
| | Received FIFO Threshold Wake-up | V | V | - | - | After software writes 1 to clear RFRTWKF (LPUARTx_WKSTS[2]). |
| | RS-485 AAD Mode Wake-up | V | V | - | - | After software writes 1 to clear RS485WKF (LPUARTx_WKSTS[3]). |
| | Received FIFO Threshold Time-out Wake-up | V | V | - | - | After software writes 1 to clear TOUTWKF (LPUARTx_WKSTS[4]). |
| | Bus idle time-out | V | V | - | - | After software writes 1 to clear AOTOWKF (LPUARTx_AUTOSTS[0]). |
| USCI UART | CTS Toggle | V | - | - | - | After software writes 1 to clear WKF (UUART_WKSTS[0]). |
| | Data Toggle | V | - | - | - | After software writes 1 to clear WKF (UUART_WKSTS[0]). |
| USCI $I^2C$ | Data toggle | V | - | - | - | After software writes 1 to clear WKF (UI2C_WKSTS[0]). |
| | Address match | V | - | - | - | After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]). |
| USCI SPI | SS Toggle | V | - | - | - | After software writes 1 to clear WKF (USPI_WKSTS[0]). |
| $I^2C$ | Address match wake-up | V | - | - | - | After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]). |
| LPI$^2C$ | Address match wake-up | V | V | - | - | After software writes 1 to clear WKAKDONE (LPI2C_WKSTS[1]). Then software writes 1 to clear WKIF(LPI2C_WKSTS[0]). |
| | Master: Transfer data count match TX/RX count | V | V | - | - | After software writes 1 to clear RXWKF (LPI2C_AUTOSTS[1]) or TXWKF (LPI2C_AUTOSTS[0]) |
| | Master: Receive NACK in address phase (address + r/w) | V | V | - | - | After software writes 1 to clear NACKWKF (LPI2C_AUTOSTS[2]) |
| LPSPI | Master: TCNT[7:0] count match wake-up | V | V | - | - | Master: after software write 1 to clear CNTWKF (LPSPI_AUTOSTS[3]) |
| | Slave: SS active wake-up | V | V | - | - | Slave: after software write 1 to clear SSWKF (LPSPI_AUTOSTS[1]) |
| TOUCHKEY | TK Sensing Result Data Match Threshold | V | - | - | - | After software writes 1 to clear SCIF (TK_STA[1]). Then software writes 1 to clear TKIFx (TK_STA[6]~TK_STA[24] and TK_STA1[0]). |
| UTCPD | Force VBUS off event(from EINT0~5) | V | - | - | - | After software writes 1 to clear FOFFVB (UTCPD_FUTSTS[6]). Then software writes 1 to clear FUTIS (UTCPD_IS[9] |
| | Connection detected | V | - | - | - | After software writes 1 to clear CCSCHIS (UTCPD_IS[0]) |
| USBOTG | ID pin state be change | V | - | - | - | After software writes 1 to set WKEN(OTG_CTL[5]). |

| | | | | | | |
|---|---|---|---|---|---|---|
| USBH | USE remote wakeup (K-state detected) | V | - | - | - | After USBH engine clock active |
| | USB connector plug-in/Plug-out (D+/D- state changed) | V | - | - | - | After CCS (HcRhPortStatus1[0]) is 1 for Plug-in while after CCS (HcRhPortStatus1[0]) is 0 for Plug-out. |
| | Overcurrent MFP pin input state change | V | - | - | - | After POCI (HcRhPortStatus1[3]) is 1. |
| USBD | Plug-in Wakeup | V | - | - | - | After software writes 1 to clear BUSIF (USBD_INTSTS[0]). |
| | Resume Wakeup | V | - | - | - | After software writes 1 to clear BUSIF (USBD_INTSTS[0]). |
| LPPDMA | Transfer Done | V | V | - | - | After software writes 1 to clear WKF (LPPDMAx_INTSTS [3]) and TDIF (LPPDMAx_TDSTS). |
| | Address don't alignment | V | V | - | - | After software writes 1 to clear WKF (LPPDMAx_INTSTS [3]) and ALIGNIF (LPPDMAx_ALIGN) . |
| | Bus response error | V | V | - | - | After software writes 1 to clear WKF (LPPDMAx_INTSTS [3]) and ABTIF(LPPDMAx_ABTSTS). |
| LPADC | ADC Conversion End | V | V | - | - | After software writes 1 to clear ADWKF (LPADC_AUTOSTS[0]). |
| | Conversion Result Monitor | V | V | - | - | After software writes 1 to clear CMP0WKF (LPADC_AUTOSTS[1]) and CMP1WKF (LPADC_AUTOSTS [2]). |
| Debug interface | Wakeup by ICE | V | - | - | - | - |

Table 6.2-7 Re-Entering Power-down Mode Condition

The NuMicro M2L31 series has two startup methods: Cold Boot and Warm Boot. Cold Boot is the process of re-excuting security boot, and Warm Boot does not re-excute security boot. Table 6.2-8 lists the difference and functional relationships between Cold-boot and Warm-boot.

| | **Normal-Run/ Power-down mode** | **Wake-up/ Resrt-Wake-up Source** | **BootFlag (Re-Security-Boot/ BootFlag value)** | **Vector Map (Function/ Setting)** | **GPIO (I/O-State/ control-by)** | **VTOR (Function/ Setting)** | |
|---|---|---|---|---|---|---|---|
| Cold Boot | DPDx | POR, nRESET | Yes/ 1 | No/ Reset | Tri-state/ NA | No/ Reset | |
| | SPDx | POR, nRESET, LVR, BOD Reset | Yes/ 1 | No/ Reset | Tri-state/ NA | No/ Reset | |
| | NPDx | POR, nRESET, LVR, BOD Reset, WDT reset | Yes/ 1 | No/ Reset | Tri-state/ NA | No/ Reset | |
| | Normal Run | POR, nRESET, LVR, BOD Reset, WDT reset | Yes/ 1 | No/ Reset | Tri-state/ NA | No/ Reset | |
| | Normal Run | SYS_IPRST0[0], AIRCR[2] | Yes/ 1 | No/ Reset | Tri-state/ NA | No/ Reset | |
| Warm Boot | DPDx | RTC, WKTMR, WKPIN | No/ 1 | Yes/ Keep | Keep/ GPIO_HOLD (At CLK_IOPDCTL[8] =1) | No/ Reset | |
| | SPDx | RTC, WKTMR, WKIO, ACMP, BOD wakeup | No/ 1 | Yes/ Keep | Keep/ GPIO_HOLD | Yes/ Reset | |
| | NPDx | Reference Wake-up source table | No/ 1 | Yes/ Keep | Keep/ IP of GPIO | Yes/ Keep | |
| | Normal Run | SYS_IPRST0[1] | No/ 1 | Yes/ Keep | Keep/ IP of GPIO | Yes/ Keep | |

Table 6.2-8 Function relationship with Cold-boot and warm-boot

### 6.2.5 Power Modes and Power Level Transition

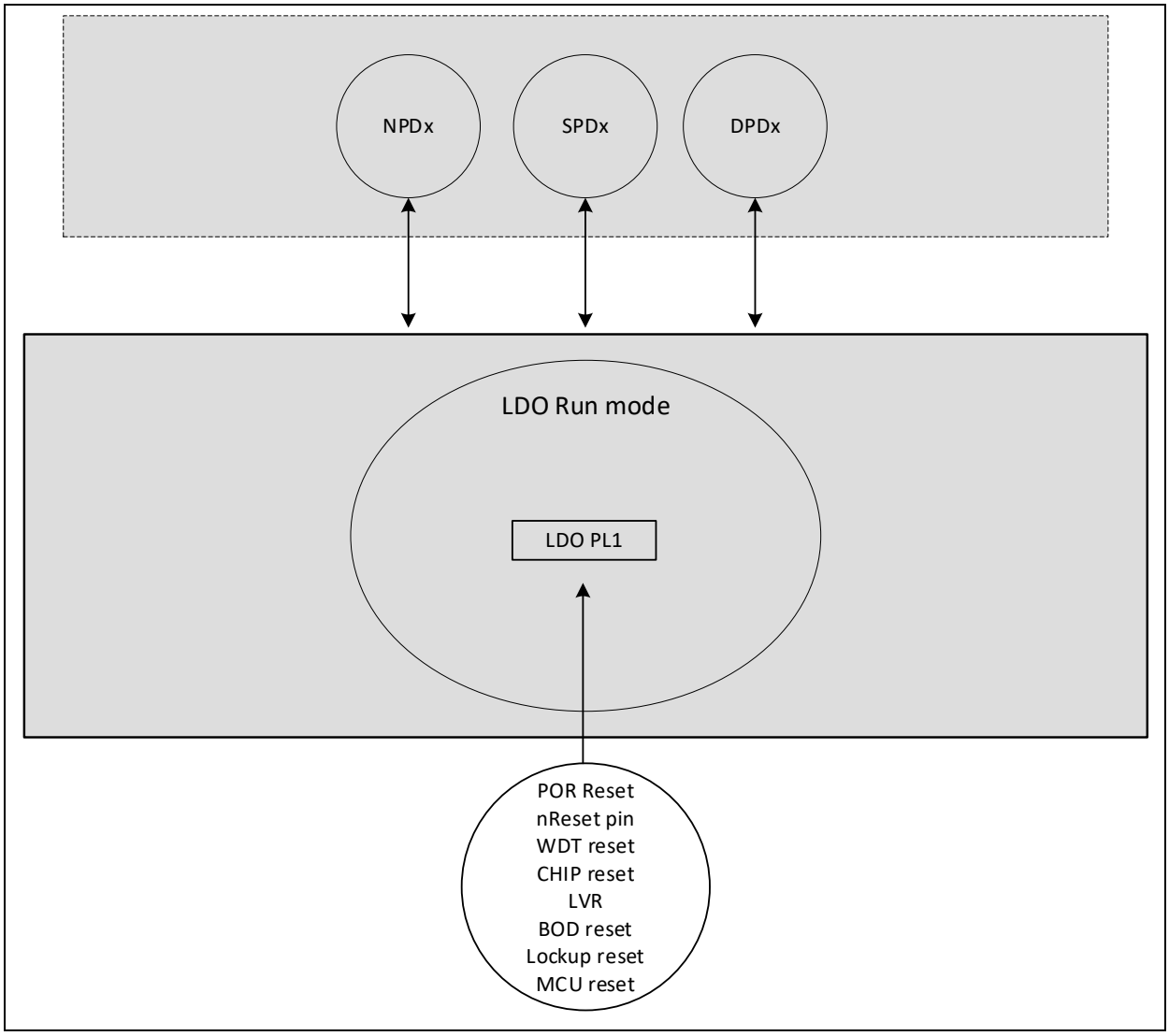



Figure 6.2-8 NuMicro M2L31 Power Mode Transition

### 6.2.6 System Memory Map

The NuMicro M2L31 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-9. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro M2L31 series only supports little-endian data format.

| Address Space | Token | Controllers |
|---|---|---|
| RRAM and SRAM Memory Space | | |
| 0x0000_0000 – 0x0007_FFFF | RRAM_BA | RRAM Memory Space (512 Kbytes) |
| 0x2000_0000 – 0x2000_9FFF | SRAM0_BA | SRAM Memory Space (40 Kbytes) |
| 0x2000_A000 – 0x2002_9FFF | SRAM1_BA | SRAM Memory Space (128 Kbytes) |
| 0x2800_0000 – 0x2800_1FFF | LPSRAM_BA | Low power SRAM Memory Space (8 Kbytes) |
| 0x6000_0000 – 0x6FFF_FFFF | EXTMEM_BA | External Memory Space (256 Mbytes) |
| Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF) | | |
| 0x4000_0000 – 0x4000_01FF<br>0x4000_0500 – 0x4000_0FFF | SYS_BA | System Control Registers |
| 0x4000_0200 – 0x4000_02FF | CLK_BA | Clock Control Registers |
| 0x4000_0300 – 0x4000_03FF | NMI_BA | NMI Control Registers |
| 0x4000_4000 – 0x4000_4FFF | GPIO_BA | GPIO Control Registers |
| 0x4000_8000 – 0x4000_8FFF | PDMA0_BA | Peripheral DMA0 Control Registers |
| 0x4000_9000 – 0x4000_9FFF | USBH_BA | USB Host Control Registers |
| 0x4000_C000 – 0x4000_CFFF | RMC_BA | RRAM Memory Control Registers |
| 0x4001_0000 – 0x4001_0FFF | EBI_BA | External Bus Interface Control Registers |
| 0x4002_0000 – 0x4002_1FFF | CANFD0_BA | CANFD0 Control Registers |
| 0x4002_4000 – 0x4002_5FFF | CANFD1_BA | CANFD1 Control Registers |
| 0x4003_1000 – 0x4003_1FFF | CRC_BA | CRC Generator Registers |
| 0x4003_2000 – 0x4003_4FFF | CRYP_BA | Cryptographic Accelerator Registers |
| 0x4003_5000 – 0x4003_5FFF | KS_BA | Key Store Registers |
| 0x4003_8000 – 0x4003_8FFF | LPSCC_BA | Low Power System and Clock Control Registers |
| 0x4003_9000 – 0x4003_9FFF | LPPDMA0_BA | Low Power Peripheral DMA0 Control Registers |
| 0x4003_A000 – 0x4003_AFFF | LPGPIO_BA | Low Power GPIO Control Registers |
| APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF) | | |
| 0x4004_0000 – 0x4004_0FFF | WDT_BA | Watchdog Timer Control Registers |
| 0x4004_1000 – 0x4004_1FFF | RTC_BA | Real Time Clock (RTC) Control Register |
| 0x4004_3000 – 0x4004_3FFF | EADC0_BA | Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers |
| 0x4004_5000 – 0x4004_5FFF | ACMP01_BA | Analog Comparator 0/ 1 Control Registers |
| 0x4004_6000 – 0x4004_6FFF | OPA_BA | OP Amplifier Control Registers |
| 0x4004_7000 – 0x4004_7FFF | DAC_BA | DAC Control Registers |

| | | |
|---|---|---|
| 0x4004_D000 – 0x4004_DFFF | OTG_BA | OTG Control Registers |
| 0x4005_0000 – 0x4005_0FFF | TMR01_BA | Timer0/Timer1 Control Registers |
| 0x4005_1000 – 0x4005_1FFF | TMR23_BA | Timer2/Timer3 Control Registers |
| 0x4005_8000 – 0x4005_8FFF | EPWM0_BA | EPWM0 Control Registers |
| 0x4005_9000 – 0x4005_9FFF | EPWM1_BA | EPWM1 Control Registers |
| 0x4005_C000 – 0x4005_CFFF | PWM0_BA | PWM0 Control Registers |
| 0x4005_D000 – 0x4005_DFFF | PWM1_BA | PWM1 Control Registers |
| 0x4006_0000 – 0x4006_0FFF | QSPI0_BA | QSPI0 Control Registers |
| 0x4006_1000 – 0x4006_1FFF | SPI0_BA | SPI0 Control Registers |
| 0x4006_2000 – 0x4006_2FFF | SPI1_BA | SPI1 Control Registers |
| 0x4006_3000 – 0x4006_3FFF | SPI2_BA | SPI2 Control Registers |
| 0x4006_4000 – 0x4006_4FFF | SPI3_BA | SPI3 Control Registers |
| 0x4007_0000 – 0x4007_0FFF | UART0_BA | UART0 Control Registers |
| 0x4007_1000 – 0x4007_1FFF | UART1_BA | UART1 Control Registers |
| 0x4007_2000 – 0x4007_2FFF | UART2_BA | UART2 Control Registers |
| 0x4007_3000 – 0x4007_3FFF | UART3_BA | UART3 Control Registers |
| 0x4007_4000 – 0x4007_4FFF | UART4_BA | UART4 Control Registers |
| 0x4007_5000 – 0x4007_5FFF | UART5_BA | UART5 Control Registers |
| 0x4007_6000 – 0x4007_6FFF | UART6_BA | UART6 Control Registers |
| 0x4007_7000 – 0x4007_7FFF | UART7_BA | UART7 Control Registers |
| 0x4008_0000 – 0x4008_0FFF | I2C0_BA | I2C0 Control Registers |
| 0x4008_1000 – 0x4008_1FFF | I2C1_BA | I2C1 Control Registers |
| 0x4008_2000 – 0x4008_2FFF | I2C2_BA | I2C2 Control Registers |
| 0x4008_3000 – 0x4008_3FFF | I2C3_BA | I2C3 Control Registers |
| 0x4009_6000 – 0x4009_6FFF | WWDT_BA | WWDT Control Registers |
| 0x400B_0000 – 0x400B_0FFF | EQEI0_BA | EQEI0 Control Registers |
| 0x400B_1000 – 0x400B_1FFF | EQEI1_BA | EQEI1 Control Registers |
| 0x400B_4000 – 0x400B_4FFF | ECAP0_BA | ECAP0 Control Registers |
| 0x400B_5000 – 0x400B_5FFF | ECAP1_BA | ECAP1 Control Registers |
| 0x400B_9000 – 0x400B_9FFF | TRNG_BA | TRNG Control Registers |
| 0x400C_0000 – 0x400C_0FFF | USBD_BA | USB Device Control Register |
| 0x400C_4000 – 0x400C_4FFF | TK_BA | Touchkey Control Register |
| 0x400C_6000 – 0x400C_6FFF | UTCPD_BA | UTCPD Control Register |
| 0x400C_9000 – 0x400C_9FFF | ACMP2_BA | Analog Comparator 2 Control Registers |
| 0x400D_0000 – 0x400D_0FFF | USCI0_BA | USCI0 Control Registers |

| | | |
|---|---|---|
| 0x400D_1000 – 0x400D_1FFF | USCI1_BA | USCI1 Control Registers |
| 0x400E_0000 – 0x400E_0FFF | LPUART0_BA | LPUART0 Control Registers |
| 0x400E_1000 – 0x400E_1FFF | LPSPI0_BA | LPSPI0 Control Registers |
| 0x400E_2000 – 0x400E_2FFF | LPI2C0_BA | LPI2C0 Control Registers |
| 0x400E_3000 – 0x400E_3FFF | LPADC0_BA | LPADC0 Control Registers |
| 0x400E_4000 – 0x400E_4FFF | LPTMR01_BA | LPTMR01 Control Registers |
| 0x400E_5000 – 0x400E_5FFF | TTMR01_BA | TTMR01 Control Registers |
| System Controllers Space (0xE000_E000 ~ 0xE000_EFFF) | | |
| 0xE000_E010 – 0xE000_E0FF | SCS_BA | System Timer Control Registers |
| 0xE000_E100 – 0xE000_ECFF | SCS_BA | External Interrupt Controller Control Registers |
| 0xE000_ED00 – 0xE000_ED8F | SCS_BA | System Control Registers |

Table 6.2-9 Address Space Assignments for On-Chip Controllers

### 6.2.7 SRAM Memory Orginization

The M2L31 supports embedded SRAM up to 168 Kbytes size and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1. The first bank has 40 Kbytes address space, the second bank has 128 Kbyte address space. These two banks address space can be accessed simultaneously. The SRAM bank0 supports parity error check to make sure chip operating more stable.

- Supports up to 168 Kbytes SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0
- Supports oversize response error
-

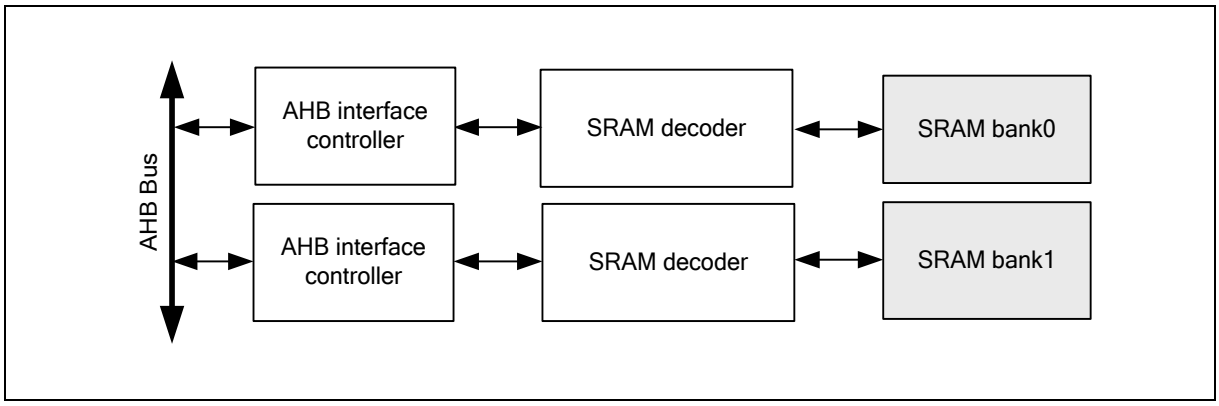



Figure 6.2-9 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization of M2L31. There are two SRAM banks in M2L31. The bank0 is addressed to 40 Kbytes and the bank1 is addressed to 128 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_9FFF. The bank1 address space is from 0x2000_A000 to 0x2002_9FFF. The address between 0x2002_A000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

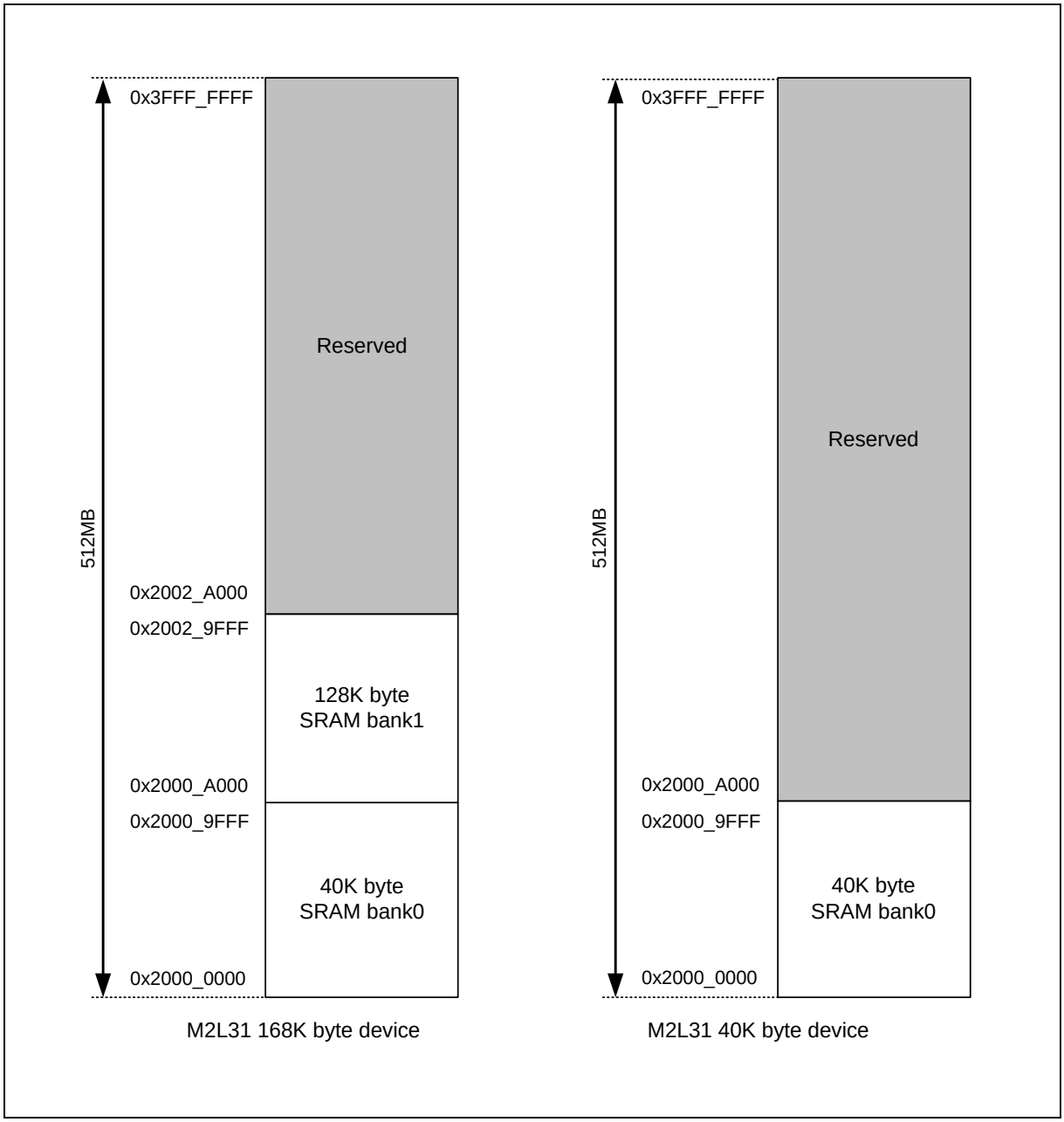



Figure 6.2-10 SRAM Memory Organization

### *6.2.7.1 SRAM Parity Error Check*

SRAM bank0 has byte parity error check function. Users must initialize SRAM before CPU accessing SRAM bank0. The parity error check is excuting while SRAM being read. As parity error occured, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occured, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

### *6.2.7.2 SRAM Power Control*

The SRAM bank0 and bank1 have marco retention and shut down function. Each SRAM marco can be configured to retention or shut down mode independently by SRAMxPMn(SYS_SRAMPC0 and SYS_SRAMPC1, x=0-1 n=0-7). Figure 6.2-11 shows the SRAM marco number in bank0 and bank1.

When chip wake-up from Power-down mode, the SRAM marcos wake up in the order of marco number, from SRAM marco0 to SRAM marco6.

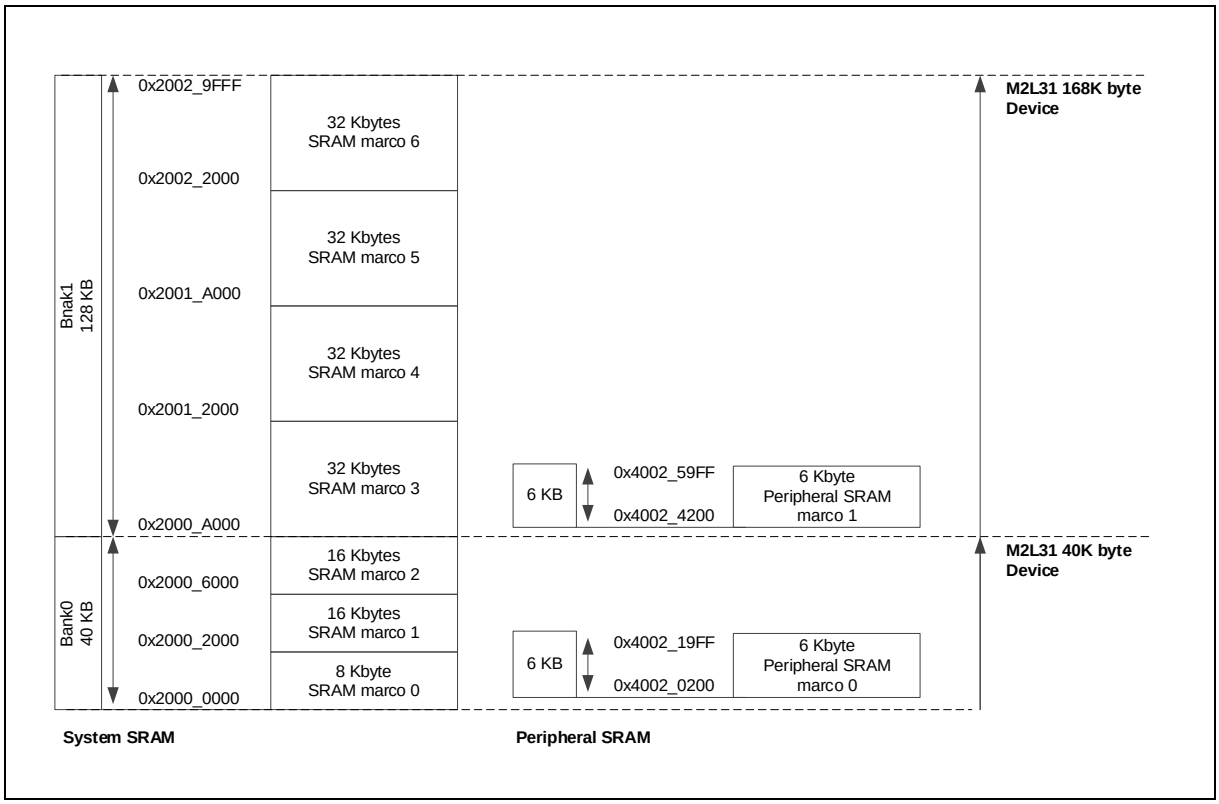



Figure 6.2-11 SRAM Marco Organization

For system SRAM (bank0 and bank1), if the SRAM power mode is set to normal mode, it automatically changes to retention mode when system enters NPD0~5/SPD0~2 Power-down mode, and then changes back to normal mode after wake-up. System SRAM power mode do not change when system enters NPD0 Power-down mode. When system enters DPD0~1 Power-down mode, system SRAM is always operating in shut down mode and reset to normal mode after wake-up.

For other peripheral SRAM, when system enters NPD0~5/SPD0~2 Power-down mode, if peripheral SRAM power mode is set to normal mode, the peripheral SRAM power mode automatically changes to retention mode, and then changes back to normal mode after wake-up, too.

But if entering SPD0~2 Power-down mode, peripheral SRAM resets to default power mode after wake-up.

When system enters DPD0~1 Power-down mode, peripheral SRAM is always operating in shut down mode and reset to default power mode after wake-up. Peripheral SRAM power mode does not change when system enters NPD0 Power-down mode.

| SRAM | Power-Down Mode | SRAM Power Mode Before and After Wake-Up |
|---|---|---|
| System SRAM bank0/1 | NPD0~2 | 1.If SRAM power mode is set to normal mode, it changes to retention mode after entering Power-down Mode, and changes back to normal mode after wake-up.<br>2.If SRAM power mode is set to retention or shut down mode, it keeps power mode setting. |
| | NPD3~5 | 1.If SRAM power mode is set to normal mode and is selected within retention size, it changes to retention mode after entering Power-down Mode, and changes back to normal mode after wake-up.<br>2.If SRAM power mode is set to normal mode and is not selected within retention size, |

| | | |
|---|---|---|
| | | it changes to shut down mode after entering Power-down Mode, and changes back to normal mode after wake-up.<br>3.If SRAM power mode is set to retention or shut down mode, it keeps power mode setting. |
| | SPD0~2 | 1.If SRAM power mode is set to normal mode and is selected within retention size, it changes to retention mode after entering Power-down Mode, and changes back to normal mode after wake-up.<br>2.If SRAM power mode is set to normal mode and is not selected within retention size, it changes to shut down mode after entering Power-down Mode, and changes back to normal mode after wake-up.<br>3.If SRAM power mode is set to retention or shut down mode, it keeps power mode setting after entering Power-down Mode, and changes back to normal mode after wake-up. |
| | DPD0~1 | No matter what SRAM power mode is set, SRAM will change to shut down mode after entering Power-down Mode, and changes back to normal mode after wake-up. |
| Peripheral SRAM bank0/1 | NPD0~2 | SRAM keep normal mode before/after entring Power-down Mode and wake-up. |
| | NPD3~5,<br>SPD0~2,<br>DPD0~1 | SRAM will enter shut down mode after entering Power-down Mode, and changes back to normal mode after wake-up. |

Table 6.2-10 SRAM Power Mode Behavior

### 6.2.8 Low Power SRAM Memory Orginization

The M2L31 supports embedded low power SRAM up to 8 Kbytes size. The low power SRAM located in low power domain and operating under HCLK1 clock speed. The low power SRAM can co-work with LPPDMA and the IP which in low power domain to do data transfer. The CPU and PDMA also can access low power SRAM, and it takes four HCLK0 clock and four HCLK1 clock for write data. For read data, it takse three HCLK0 clock and four HCLK1 clock.

- Supports up to 8 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

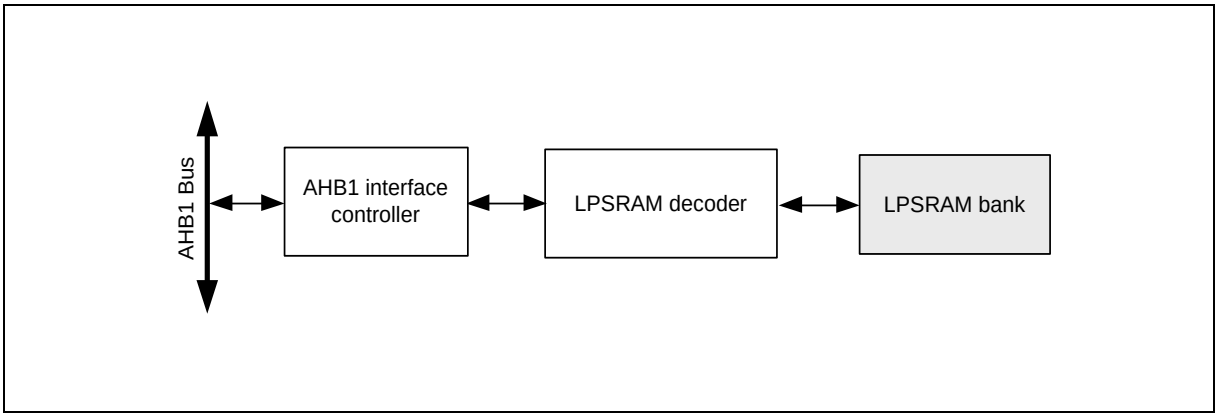



Figure 6.2-12 LPSRAM Block Diagram

### 6.2.9 Bus Matrix

The M2L31 supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex-M23 CPU as the highest bus priority.

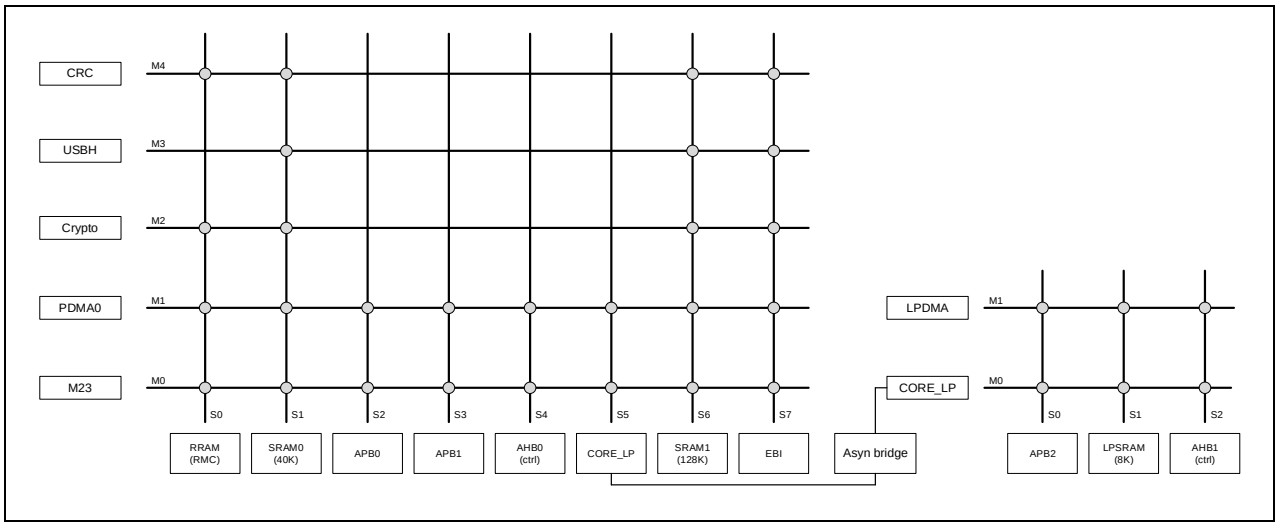



Figure 6.2-13 NuMicro M2L31 Bus Matrix Diagram

**Note**: The RRAM, SRAM0/1, LPSRAM, CRC and EBI transfers must be aligned to the address boundry which equal to the transfer size (Word/HalfWord/Byte). Other AHB and APB slaves must be word-aligned to the address boundry with transfer size in Word.

### 6.2.10 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator), HIRC trim (48 MHz RC oscillator) and MIRC trim (1 MHz RC oscillator) according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % /0.5% /0.75% /1% selected by ACCURSEL (SYS_HIRCTCTL[3:2]/ SYS_IRCTCTL[3:2]/ SYS_MIRCTCTL[3:2]) deviation within all temperature ranges.

For some application needs an accurate 12 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_IRCTCTL[3:2]) set.

For some application needs an accurate 48 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_HIRCTCTL[3:2]) set.

For some application needs an accurate 1 MHz clock. In such case, if neither using PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_MIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_MIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_MIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within the deviation ACCURSEL(SYS_MIRCTCTL[3:2]) set.

### 6.2.11 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

| Protected Register | Location |
|---|---|
| SYS_IPRST0 | Address 0x4000_0008 |
| SYS_BODCTL | address 0x4000_0018 |
| SYS_VREFCTL | address 0x4000_0028 |
| SYS_USBPHY | address 0x4000_002C |
| SYS_SRAM_BISTCTL | address 0x4000_00D0 |
| SYS_PORDISAN | address 0x4000_01EC |
| SYS_PLCTL | address 0x4000_01F8 |
| CLK_PWRCTL | address 0x4000_0200 |
| CLK_APBCLK0 | address 0x4000_0208 |
| CLK_CLKSEL0 | address 0x4000_0210 |
| CLK_CLKSEL1 | address 0x4000_0214 |
| CLK_PLLCTL | address 0x4000_0240 |
| CLK_PMUCTL | address 0x4000_0290 |
| NMIEN | address 0x4000_0300 |
| AHBMCTL | address 0x4000_0400 |
| RMC_FTCTL | address 0x4000_5018 |
| RMC_ICPCMD | address 0x4000_501C |
| RMC_ISPCTL | address 0x4000_C000 |
| RMC_ISPTRG | address 0x4000_C010 |
| RMC_ISPSTS | address 0x4000_C040 |
| RMC_CYCCTL | address 0x4000_C04C |
| RMC_KPKEYTRG | address 0x4000_C05C |
| RMC_KPKEYSTS | address 0x4000_C060 |
| WDT_CTL | address 0x4004_0000 |
| WDT_ALTCTL | address 0x4004_0004 |
| TIMER0_CTL | address 0x4005_0000 |
| TIMER1_CTL | address 0x4005_0100 |
| TIMER2_CTL | address 0x4005_1000 |
| TIMER3_CTL | address 0x4005_1100 |

| | |
|---|---|
| TIMER0_PWMCTL | address 0x4005_0040 |
| TIMER1_PWMCTL | address 0x4005_0140 |
| TIMER2_PWMCTL | address 0x4005_1040 |
| TIMER3_PWMCTL | address 0x4005_1140 |
| TIMER0_PWMDTCTL | address 0x4005_0058 |
| TIMER1_PWMDTCTL | address 0x4005_0158 |
| TIMER2_PWMDTCTL | address 0x4005_1058 |
| TIMER3_PWMDTCTL | address 0x4005_1158 |
| TIMER0_PWMBRKCTL | address 0x4005_0070 |
| TIMER1_PWMBRKCTL | address 0x4005_0170 |
| TIMER2_PWMBRKCTL | address 0x4005_1070 |
| TIMER3_PWMBRKCTL | address 0x4005_1170 |
| TIMER0_PWMSWBRK | address 0x4005_007C |
| TIMER1_PWMSWBRK | address 0x4005_017C |
| TIMER2_PWMSWBRK | address 0x4005_107C |
| TIMER3_PWMSWBRK | address 0x4005_117C |
| TIMER0_PWMINTEN1 | address 0x4005_0084 |
| TIMER1_PWMINTEN1 | address 0x4005_0184 |
| TIMER2_PWMINTEN1 | address 0x4005_1084 |
| TIMER3_PWMINTEN1 | address 0x4005_1184 |
| TIMER0_PWMINTSTS1 | address 0x4005_008C |
| TIMER1_PWMINTSTS1 | address 0x4005_018C |
| TIMER2_PWMINTSTS1 | address 0x4005_108C |
| TIMER3_PWMINTSTS1 | address 0x4005_118C |
| EPWM_CTL0 | address 0x4005_8000/0x4005_9000 |
| EPWM_CTL1 | address 0x4005_8000/0x4005_9000 |
| EPWM_DTCTL0_1 | address 0x4005_8070/0x4005_9070 |
| EPWM_DTCTL2_3 | address 0x4005_8074/0x4005_9074 |
| EPWM_DTCTL4_5 | address 0x4005_8078/0x4005_9078 |
| EPWM_BRKCTL0_1 | address 0x4005_80C8/0x4005_90C8 |
| EPWM_BRKCTL2_3 | address 0x4005_80CC/0x4005_90CC |
| EPWM_BRKCTL4_5 | address 0x4005_80D0/0x4005_90D0 |
| EPWM_SWBRK | address 0x4005_80DC/0x4005_90DC |
| EPWM_INTEN1 | address 0x4005_80E4/0x4005_90E4 |
| EPWM_INTSTS1 | address 0x4005_80EC/0x4005_90EC |

| | |
|---|---|
| BPWM_CTL0 | address 0x4005_A000/0x4005_B000 |
| SYST_VAL | address 0xE000_E018 |

Table 6.2-11 Protected Registers

### 6.2.12 Deep Power Down Wakeup Pin

When chip enter deep Power-down mode (DPD0/DPD1), the chip can be wake-up by six wake-up pins. These pins are WKPIN0 (PC.0), WKPIN1 (PB.0), WKPIN2 (PB.2), WKPIN3 (PB.12), WKPIN4 (PF.6) and WKPIN5 (PA.12). User can set WKPINEN0 (CLK_PMUWKCTL[17:16]) to select WKPIN0 trigger edge or disable WKPIN0 wake-up function. In the same way, user can set WKPINEN1 (CLK_PMUWKCTL[19:18]) to select WKPIN1 trigger edge or disable WKPIN1 wake-up function, set WKPINEN2 (CLK_PMUWKCTL[21:20]) to select WKPIN2 trigger edge or disable WKPIN2 wake-up function, set WKPINEN3 (CLK_PMUWKCTL[23:22]) to select WKPIN3 trigger edge or disable WKPIN3 wake-up function, set WKPINEN4 (CLK_PMUWKCTL[25:24]) to select WKPIN4 trigger edge or disable WKPIN4 wake-up function and set WKPINEN5 (CLK_PMUWKCTL[27:26]) to select WKPIN5 trigger edge or disable WKPIN5 wake-up function.

### 6.2.13 Wake-up Timer (WKTMR) and Wake-up IO (WKIO) Function

The WKTMR function can be enabled by WKTMREN (CLK_PMUWKCTL[0]), WKTMRMOD (CLK_PMUWKCTL[1]) and WKTMRIS (CLK_PMUWKCTL[11:8]). WKTMR can wake-up chip from NPD0~5/SPD0~2/DPD0~1 modes.

When WKTMR wake-up event occurred in NPD0~5 modes, TMRWK (CLK_PMUSTS[1]) will be set, and if WKTMRIE (CLK_PMUINTC[0]) is set to 1, WKTMRIF (CLK_PMUINTS[0]) will be set and ETI interrupt will be triggered. When WKTMR wake-up event occurred in SPD0~2/DPD0~1 modes, chip will be reset and re-run. Users can check wakeup flag from TMRWK (CLK_PMUSTS[1]).

The WKIO function can be enabled by CLK_PAPWCTL, CLK_PBPWCTL, CLK_PCPWCTL, CLK_PDPWCTL and CLK_PWDBCTL. WKIO can wakeup chip from NPD0~5/SPD0~2 modes.

When WKIO event occurred in NPD0~5 modes, GPXWKx(CLK_PMUSTS[27:24], CLK_PMUSTS[11:8]) will be set, and if any of WKIO interrupt enable (CLK_PMUINTC[15:8]) is set to 1, WKIO interrupt flag (CLK_PMUINTS[15:8]) will be set and ETI interrupt will be triggered. When WKIO wake-up event occurred in SPD0~2 modes, chip will be reset and re-run. Users can check wakeup flag from GPXWKx (CLK_PMUSTS[27:24], CLK_PMUSTS[11:8]).

### 6.2.14 Low Power Domain System Clock

The low power domain system clock include HCLK1 and PCLK2. HCLK1 has five clock sources, which can be selected by HCLK1SEL (CLK_CLKSEL0[7:6]). PCLK2 is generated from HCLK1, can be HCLK1 divided by 1/2/4/8/16. The block diagram is shown in Figure 6.2-14.

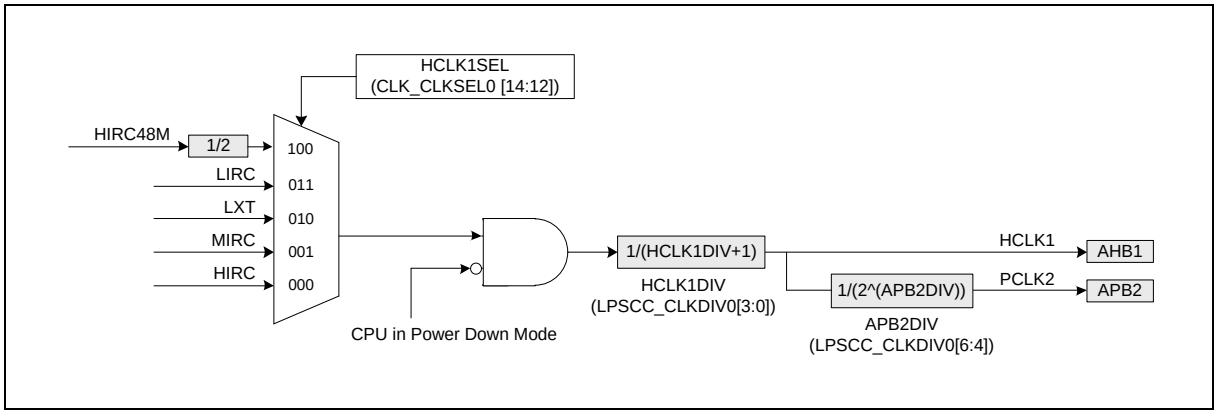



Figure 6.2-14 Low Power Domain System Clock Block Diagrams

### 6.2.15 System Timer (SysTick)

The Cortex-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm Cortex-M23 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

### 6.2.16 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

#### *6.2.16.1 Exception Model and System Interrupt Map*

Table 6.2-12 lists the exception model supported by M2L31 Series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

| Exception Type | Vector Number | Vector Address | Priority |
|---|---|---|---|
| Reset | 1 | 0x00000004 | -3 |
| NMI | 2 | 0x00000008 | -2 |
| Hard Fault | 3 | 0x0000000C | -1 |
| Memory Manager Fault | 4 | 0x00000010 | Configurable |
| Bus Fault | 5 | 0x00000014 | Configurable |
| Usage Fault | 6 | 0x00000018 | Configurable |
| Reserved | 7 ~ 10 | | Reserved |

| | | | |
|---|---|---|---|
| SVCall | 11 | 0x0000002C | Configurable |
| Reserved | 12~13 | | Reserved |
| PendSV | 14 | 0x00000038 | Configurable |
| SysTick | 15 | 0x0000003C | Configurable |
| Interrupt (IRQ0 ~ IRQ) | 16 ~ 159 | 0x00000000 + (Vector Number)*4 | Configurable |

Table 6.2-12 Exception Model

| Vector Number | Interrupt Number (Bit In Interrupt Registers) | Interrupt Name | Interrupt Description |
|---|---|---|---|
| 0 ~ 15 | - | - | System exceptions |
| 16 | 0 | BODOUT | Brown-Out low voltage detected interrupt |
| 17 | 1 | IRC_INT | IRC TRIM interrupt |
| 18 | 2 | PWRWU_INT | Clock controller interrupt for chip wake-up from power-down state |
| 19 | 3 | SRAM_PERR | SRAM parity check error interrupt |
| 20 | 4 | CLKFAIL | Clock fail detected interrupt |
| 21 | 5 | RMC_INT | RRAM Memory Controller interrupt |
| 22 | 6 | RTC_INT | Real time clock interrupt |
| 23 | 7 | TAMPER_INT | Backup register tamper interrupt |
| 24 | 8 | WDT_INT | Watchdog Timer interrupt |
| 25 | 9 | WWDT_INT | Window Watchdog Timer interrupt |
| 26 | 10 | EINT0 | External interrupt from INT0 pins |
| 27 | 11 | EINT1 | External interrupt from INT1 pins |
| 28 | 12 | EINT2 | External interrupt from INT2 pin |
| 29 | 13 | EINT3 | External interrupt from INT3 pin |
| 30 | 14 | EINT4 | External interrupt from INT4 pin |
| 31 | 15 | EINT5 | External interrupt from INT5 pin |
| 32 | 16 | GPA_INT | External interrupt from PA[15:0] pin |
| 33 | 17 | GPB_INT | External interrupt from PB[15:0] pin |
| 34 | 18 | GPC_INT | External interrupt from PC[15:0] pin |
| 35 | 19 | GPD_INT | External interrupt from PD[15:0] pin |
| 36 | 20 | GPE_INT | External interrupt from PE[15:0] pin |
| 37 | 21 | GPF_INT | External interrupt from PF[15:0] pin |
| 38 | 22 | QSPI0_INT | QSPI0 interrupt |
| 39 | 23 | SPI0_INT | SPI0 interrupt |

| | | | |
|---|---|---|---|
| 40 | 24 | EBRAKE0_INT | EPWM0 brake interrupt |
| 41 | 25 | EPWM0_P0_INT | EPWM0 pair 0 interrupt |
| 42 | 26 | EPWM0_P1_INT | EPWM0 pair 1 interrupt |
| 43 | 27 | EPWM0_P2_INT | EPWM0 pair 2 interrupt |
| 44 | 28 | EBRAKE1_INT | EPWM1 brake interrupt |
| 45 | 29 | EPWM1_P0_INT | EPWM1 pair 0 interrupt |
| 46 | 30 | EPWM1_P1_INT | EPWM1 pair 1 interrupt |
| 47 | 31 | EPWM1_P2_INT | EPWM1 pair 2 interrupt |
| 48 | 32 | TMR0_INT | Timer 0 interrupt |
| 49 | 33 | TMR1_INT | Timer 1 interrupt |
| 50 | 34 | TMR2_INT | Timer 2 interrupt |
| 51 | 35 | TMR3_INT | Timer 3 interrupt |
| 52 | 36 | UART0_INT | UART0 interrupt |
| 53 | 37 | UART1_INT | UART1 interrupt |
| 54 | 38 | I2C0_INT | I2C0 interrupt |
| 55 | 39 | I2C1_INT | I2C1 interrupt |
| 56 | 40 | PDMA0_INT | PDMA0 interrupt |
| 57 | 41 | DAC_INT | DAC interrupt |
| 58 | 42 | EADC0_INT0 | EADC0 interrupt source 0 |
| 59 | 43 | EADC0_INT1 | EADC0 interrupt source 1 |
| 60 | 44 | ACMP01_INT | ACMP0 and ACMP1 interrupt |
| 61 | 45 | ACMP2_INT | ACMP2 interrupt |
| 62 | 46 | EADC0_INT2 | EADC0 interrupt source 2 |
| 63 | 47 | EADC0_INT3 | EADC0 interrupt source 3 |
| 64 | 48 | UART2_INT | UART2 interrupt |
| 65 | 49 | UART3_INT | UART3 interrupt |
| 66 | 50 | Reserved | Reserved |
| 67 | 51 | SPI1_INT | SPI1 interrupt |
| 68 | 52 | SPI2_INT | SPI2 interrupt |
| 69 | 53 | USBD_INT | USB device interrupt |
| 70 | 54 | USBH_INT | USB host interrupt |
| 71 | 55 | USBOTG_INT | USB OTG interrupt |
| 72 | 56 | ETI_INT | External Trigger Interface interrupt |
| 73 | 57 | CRC0_INT | CRC0 interrupt |
| 74 | 58 | Reserved | Reserved |

| | | | |
|---|---|---|---|
| 75 | 59 | Reserved | Reserved |
| 76 | 60 | Reserved | Reserved |
| 77 | 61 | Reserved | Reserved |
| 78 | 62 | SPI3_INT | SPI3 interrupt |
| 79 | 63 | TK_INT | Touchkey interrupt |
| 80 | 64 | Reserved | Reserved |
| 81 | 65 | Reserved | Reserved |
| 82 | 66 | Reserved | Reserved |
| 83 | 67 | Reserved | Reserved |
| 84 | 68 | Reserved | Reserved |
| 85 | 69 | Reserved | Reserved |
| 86 | 70 | OPA_INT | Analog OPA interrupt |
| 87 | 71 | CRYPTO | Crypto interrupt |
| 88 | 72 | GPG_INT | External interrupt from PG[15:0] pin |
| 89 | 73 | EINT6 | External interrupt from INT6 pin |
| 90 | 74 | UART4_INT | UART4 interrupt |
| 91 | 75 | UART5_INT | UART5 interrupt |
| 92 | 76 | USCI0_INT | USCI0 interrupt |
| 93 | 77 | USCI1_INT | USCI1 interrupt |
| 94 | 78 | Reserved | Reserved |
| 95 | 79 | Reserved | Reserved |
| 96 | 80 | Reserved | Reserved |
| 97 | 81 | Reserved | Reserved |
| 98 | 82 | I2C2_INT | I2C2 interrupt |
| 99 | 83 | I2C3_INT | I2C3 interrupt |
| 100 | 84 | EQEI0_INT | EQEI0 interrupt |
| 101 | 85 | EQEI1_INT | EQEI1 interrupt |
| 102 | 86 | ECAP0_INT | ECAP0 interrupt |
| 103 | 87 | ECAP1_INT | ECAP1 interrupt |
| 104 | 88 | GPH_INT | External interrupt from PH[15:0] pin |
| 105 | 89 | EINT7 | External interrupt from INT7 pin |
| 106 | 90 | Reserved | Reserved |
| 107 | 91 | Reserved | Reserved |
| 108 | 92 | Reserved | Reserved |
| 109 | 93 | Reserved | Reserved |

| | | | |
|---|---|---|---|
| 110 | 94 | Reserved | Reserved |
| 111 | 95 | Reserved | Reserved |
| 112 | 96 | Reserved | Reserved |
| 113 | 97 | Reserved | Reserved |
| 114 | 98 | LPPDMA0_INT | LPPDMA0 interrupt |
| 115 | 99 | Reserved | Reserved |
| 116 | 100 | Reserved | Reserved |
| 117 | 101 | TRNG_INT | TRNG interrupt |
| 118 | 102 | UART6_INT | UART6 interrupt |
| 119 | 103 | UART7_INT | UART7 interrupt |
| 120 | 104 | Reserved | Reserved |
| 121 | 105 | Reserved | Reserved |
| 122 | 106 | Reserved | Reserved |
| 123 | 107 | Reserved | Reserved |
| 124 | 108 | UTCPD_INT | UTCPD interrupt |
| 125 | 109 | Reserved | Reserved |
| 126 | 110 | Reserved | Reserved |
| 127 | 111 | Reserved | Reserved |
| 128 | 112 | CANFD00 | CANFD00 interrupt |
| 129 | 113 | CANFD01 | CANFD01 interrupt |
| 130 | 114 | CANFD10 | CANFD10 interrupt |
| 131 | 115 | CANFD11 | CANFD11 interrupt |
| 132 | 116 | Reserved | Reserved |
| 133 | 117 | Reserved | Reserved |
| 134 | 118 | Reserved | Reserved |
| 135 | 119 | Reserved | Reserved |
| 136 | 120 | Reserved | Reserved |
| 137 | 121 | Reserved | Reserved |
| 138 | 122 | Reserved | Reserved |
| 139 | 123 | Reserved | Reserved |
| 140 | 124 | Reserved | Reserved |
| 141 | 125 | Reserved | Reserved |
| 142 | 126 | Reserved | Reserved |
| 143 | 127 | Reserved | Reserved |
| 144 | 128 | BRAKE0_INT | PWM0 brake interrupt |

| | | | |
|---|---|---|---|
| 145 | 129 | PWM0_P0_INT | PWM0 pair 0 interrupt |
| 146 | 130 | PWM0_P1_INT | PWM0 pair 1 interrupt |
| 147 | 131 | PWM0_P2_INT | PWM0 pair 2 interrupt |
| 148 | 132 | BRAKE1_INT | PWM1 brake interrupt |
| 149 | 133 | PWM1_P0_INT | PWM1 pair 0 interrupt |
| 150 | 134 | PWM1_P1_INT | PWM1 pair 1 interrupt |
| 151 | 135 | PWM1_P2_INT | PWM1 pair 2 interrupt |
| 152 | 136 | LPADC0_INT | LPADC0 interrupt |
| 153 | 137 | LPUART0_INT | LPUART0 interrupt |
| 154 | 138 | LPI2C0_INT | LPI2C0 interrupt |
| 155 | 139 | LPSPI0_INT | LPSPI0 interrupt |
| 156 | 140 | LPTMR0_INT | LPTMR0 interrupt |
| 157 | 141 | LPTMR1_INT | LPTMR1 interrupt |
| 158 | 142 | TTMR0_INT | TTMR0 interrupt |
| 159 | 143 | TTMR1_INT | TTMR1 interrupt |

Table 6.2-13 Interrupt Number Table

#### *6.2.16.2 Operation Description*

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

### 6.2.17 System Control Register

The Cortex-M23 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex-M23 interrupt priority and Cortex-M23 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm Cortex-M23 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

## 6.3 Clock Controller

### 6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 12 MHz internal high speed RC oscillator (HIRC), 48 MHz internal high speed RC oscillator (HIRC48M) and 1/2/4/8 MHz internal multiple speed RC oscillator (MIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

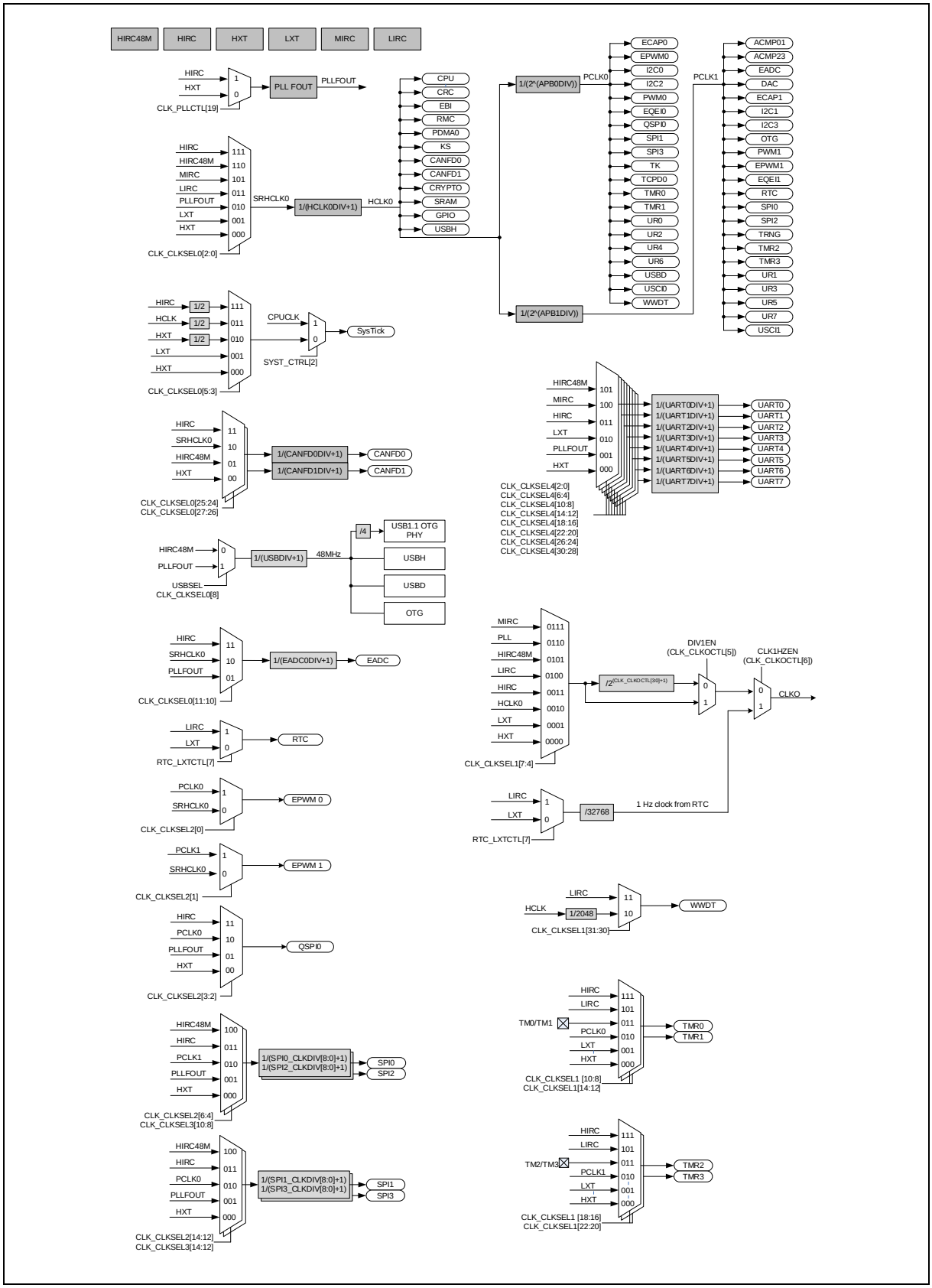



Figure 6.3-1 Clock Generator Global View Diagram

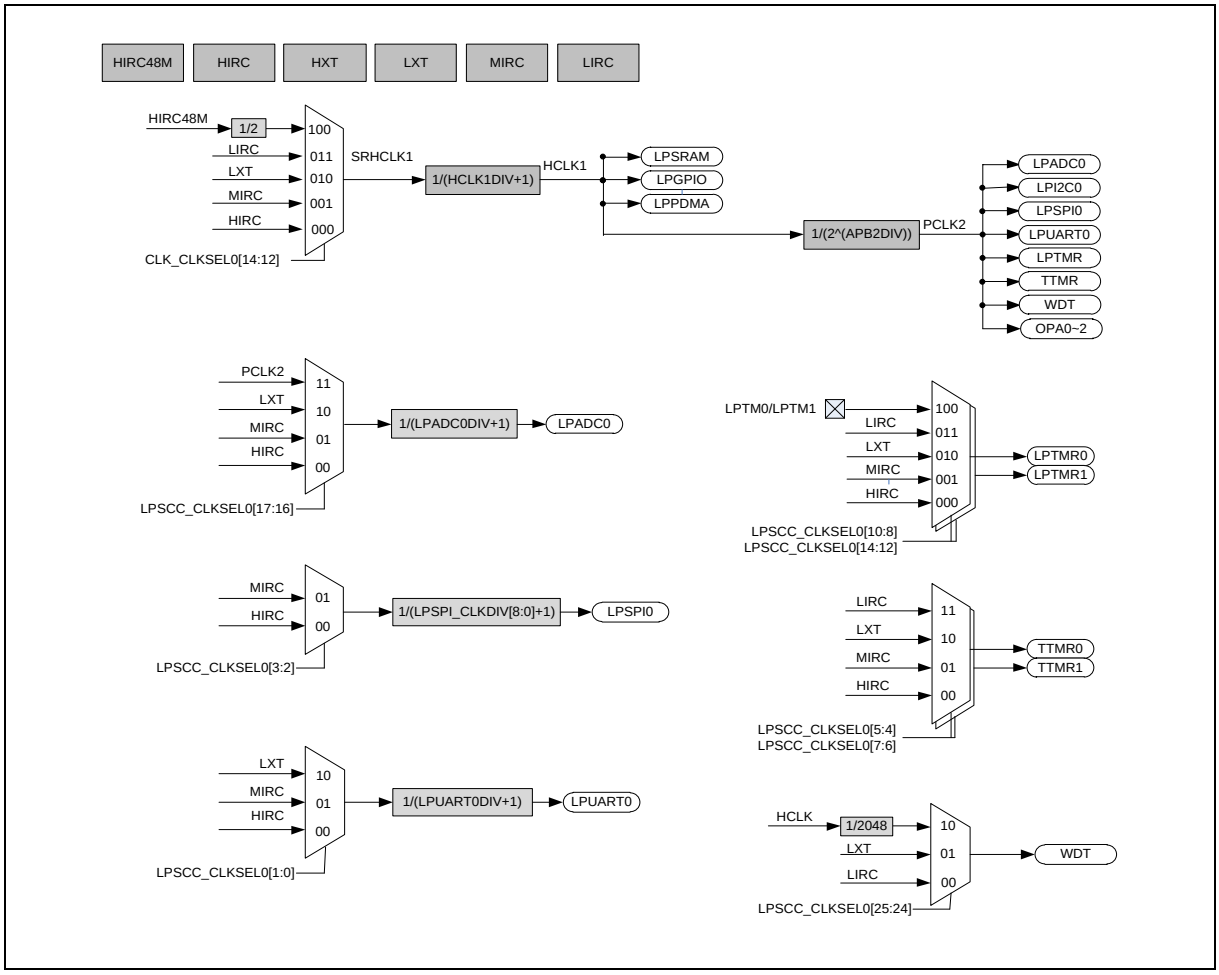



Figure 6.3-2 Low Power Domain Clock Generator Global View Diagram

### 6.3.2 Clock Generator

The clock generator consists of seven clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~32 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- 12 MHz internal high speed RC oscillator (HIRC)
- 32 kHz internal low speed RC oscillator (LIRC)
- 48 MHz internal high speed RC oscillator (HIRC48M)
- 1/2/4/8 MHz internal multiple speed RC oscillator (MIRC)
-

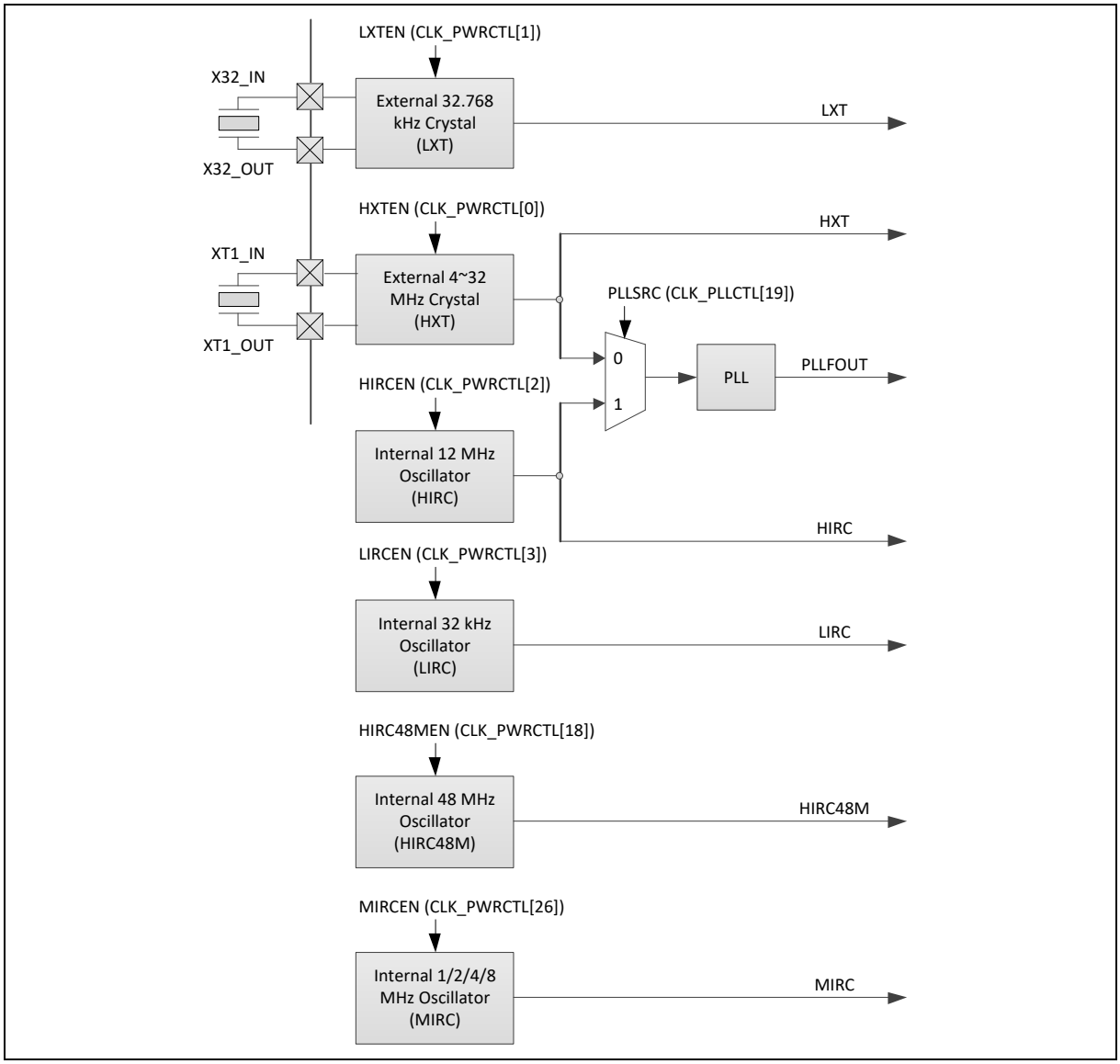



Figure 6.3-3 Clock Generator Block Diagram

### 6.3.3 Internal Multiple Speed RC Oscillator (MIRC)

The chip has a built-in internal multiple speed RC oscillator (MIRC) for a variable clock frequency with lower power consumption. Setting MIRCFSEL (CLK_PWRCTL[30:28]) can select MIRC output clock frequency to 1/2/4/8 MHz. The frequency setting of MIRC cannot be changed during MIRC is enabled. Before changing the MIRC frequency of MIRC, MIRC should be disabled and check MIRCSTB (CLK_STATUS[5]) flag go low. After changing clock frequency setting, users can enable MIRC and wait MIRCSTB (CLK_STATUS[5]) flag go high, then, MIRC can be used by system or peripherals clock source.

### 6.3.4 System Clock

The system clock include CPUCLK, HCLK0, HCLK1, PCLK0, PCLK1 and PCLK2. HCLK0 has seven clock sources, which can be selected by HCLK0SEL (CLK_CLKSEL0[2:0]). HCLK1 has five clock sources, which can be selected by HCLK1SEL (CLK_CLKSEL0[7:6]). PCLK0 and PCLK1 are generated from HCLK0, can be HCLK0 divided by 1/2/4/8/16. PCLK2 is generated from HCLK1, can be HCLK1 divided by 1/2/4/8/16. The block diagram is shown in Figure 6.3-4.

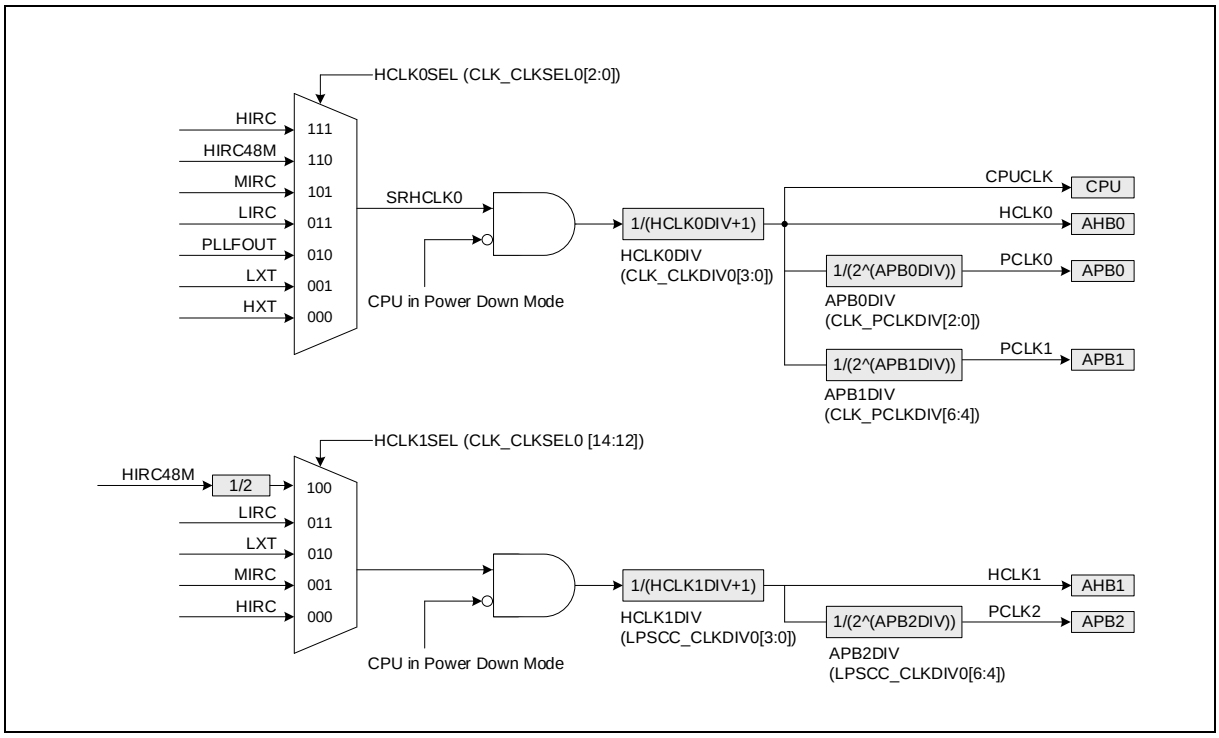



Figure 6.3-4 System Clock Block Diagrams

The clock source of SysTick in Cortex-M23 core can use CPU clock or external clock (SYST_CTL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

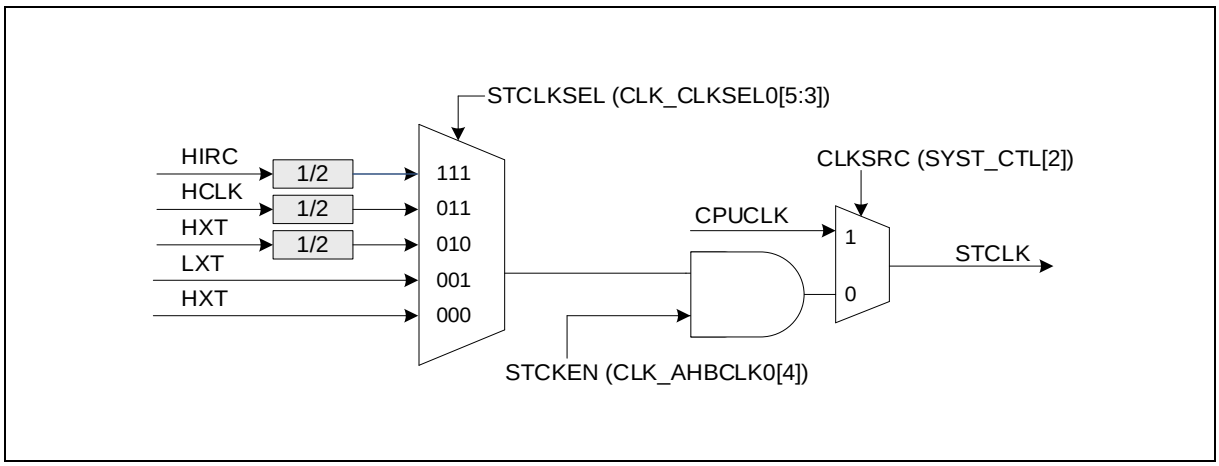



Figure 6.3-5 SysTick Clock Control Block Diagram

### 6.3.5 Clock Fail Detection

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

When LXT clock detector is enabled, the system clock will auto switch to LIRC if LXT clock stop is detected and system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIEN (CLK_CLKDCTL[13]) is set to 1. User can try to recover LXT by disabling LXT and enabling LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recovered to oscillate after re-enable action and user can switch system clock to LXT again.

Figure 6.3-6 shows The HXT clock stops detection and system clock switches to HIRC procedure

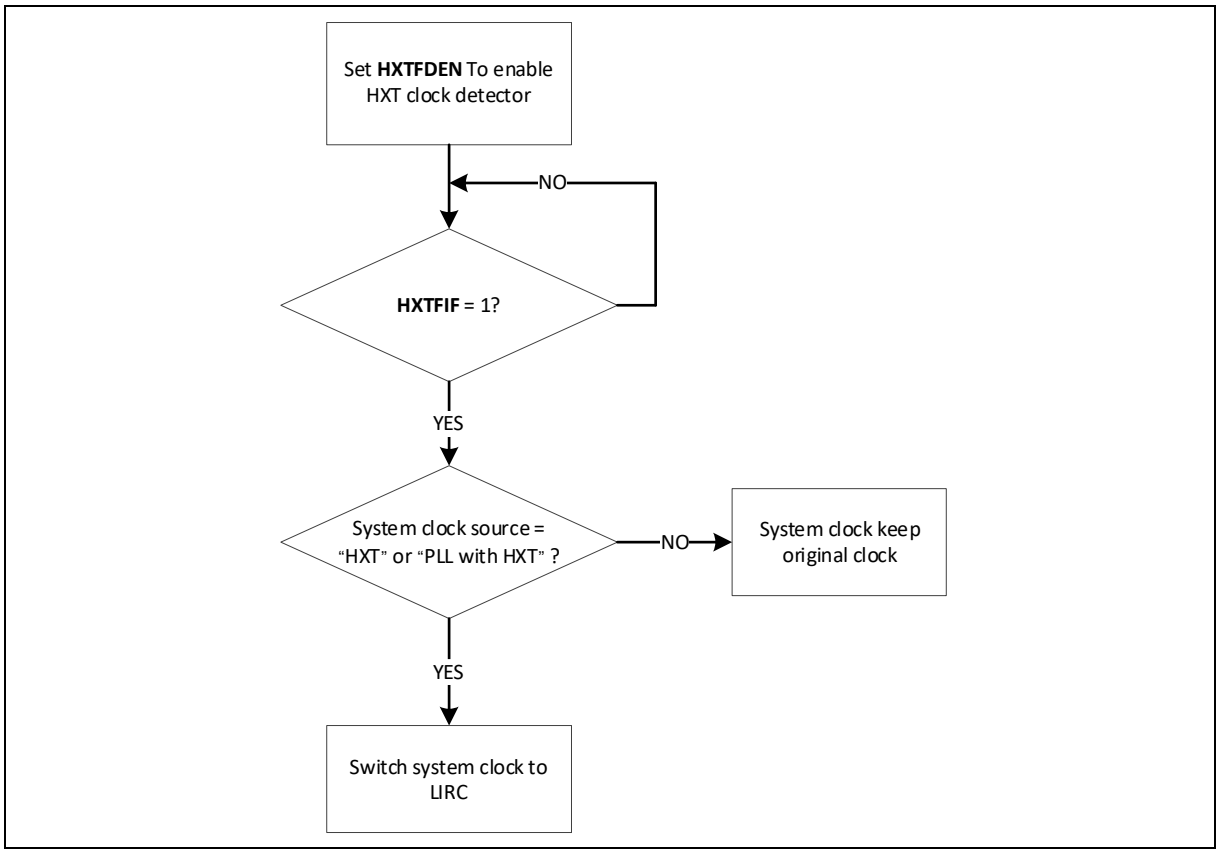



Figure 6.3-6 HXT Stop Protect Procedure

Figure 6.3-7 shows that the LXT clock stops detection and system clock switches to HIRC procedure.

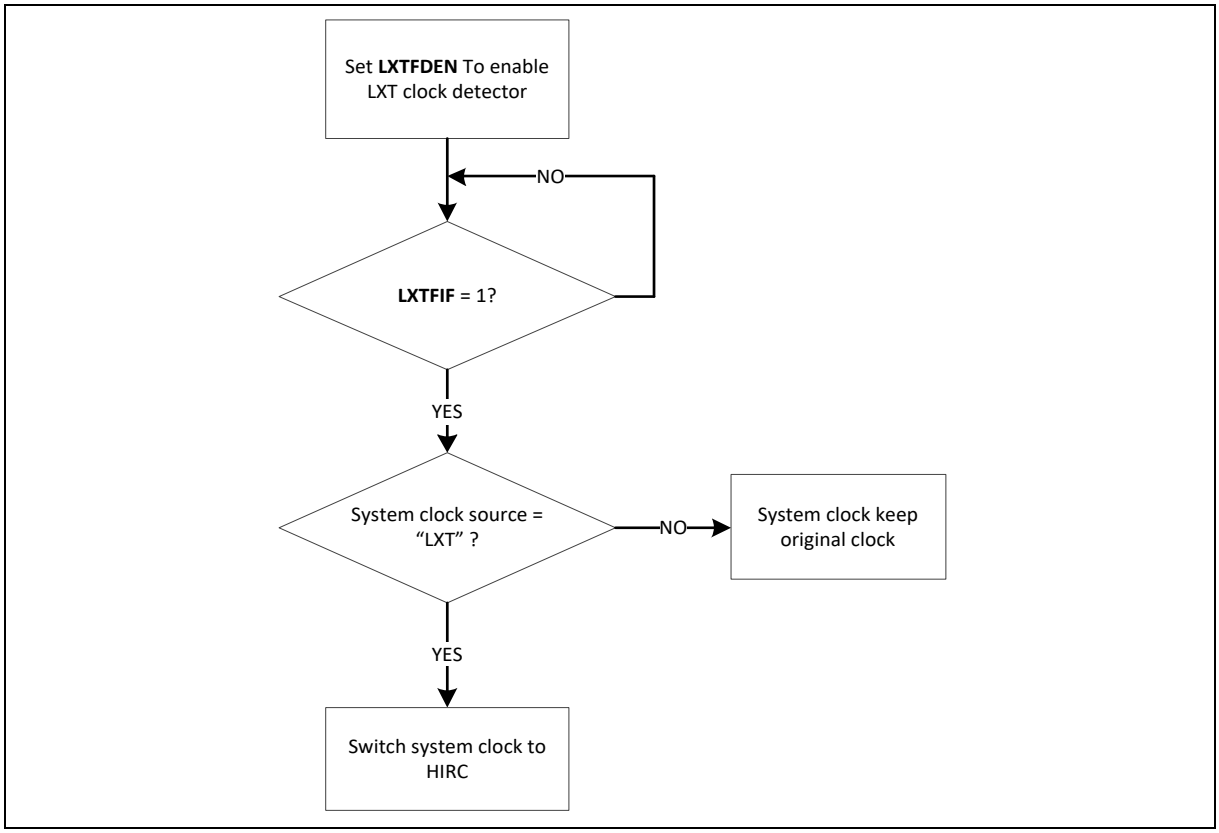



Figure 6.3-7 LXT Stop Protect Procedure

### 6.3.6 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3 and CLK_CLKSEL4 register.

### 6.3.7 Power-down Mode Clock

When entering Power-down mode, the system clocks, some of clock sources and peripheral clocks are disabled. But some of clock sources and peripheral clocks are still active in Power-down mode.

The clocks which are still active in Power-down mode are listed below:

- Clock Generator
  - 32 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
  - 12 MHz internal high speed RC oscillator (HIRC) clock if needed
  - 1/2/4/8 MHz internal multiple speed RC oscillator (MIRC) clock if needed
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)
- Peripherials Clock in which in low power domain

### 6.3.8 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where $F_{in}$ is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where $F_{in}$ is the input clock frequency, $F_{out}$ is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state. When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT.

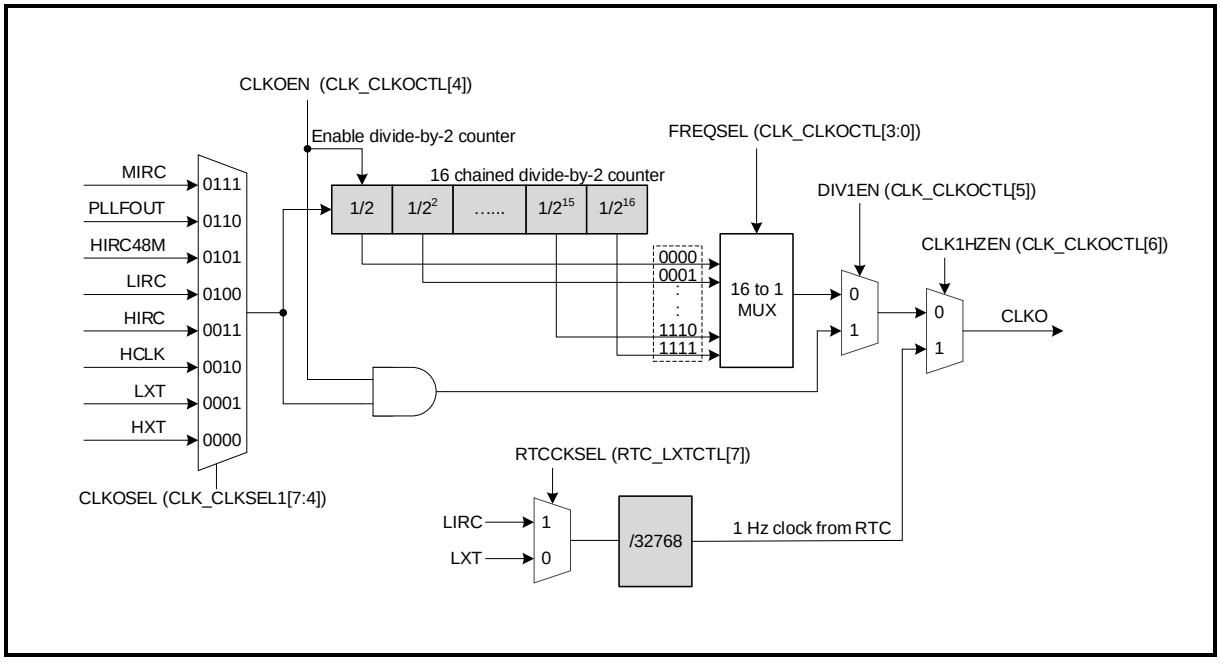



Figure 6.3-8 Clock Output Block Diagram

### 6.3.9 USB Clock Source

The clock sources of USB 1.1 and 2.0 systems are generated from USB2.0 PHY clock or programmable PLL output. The generated clocks are shown in Figure 6.3-9.

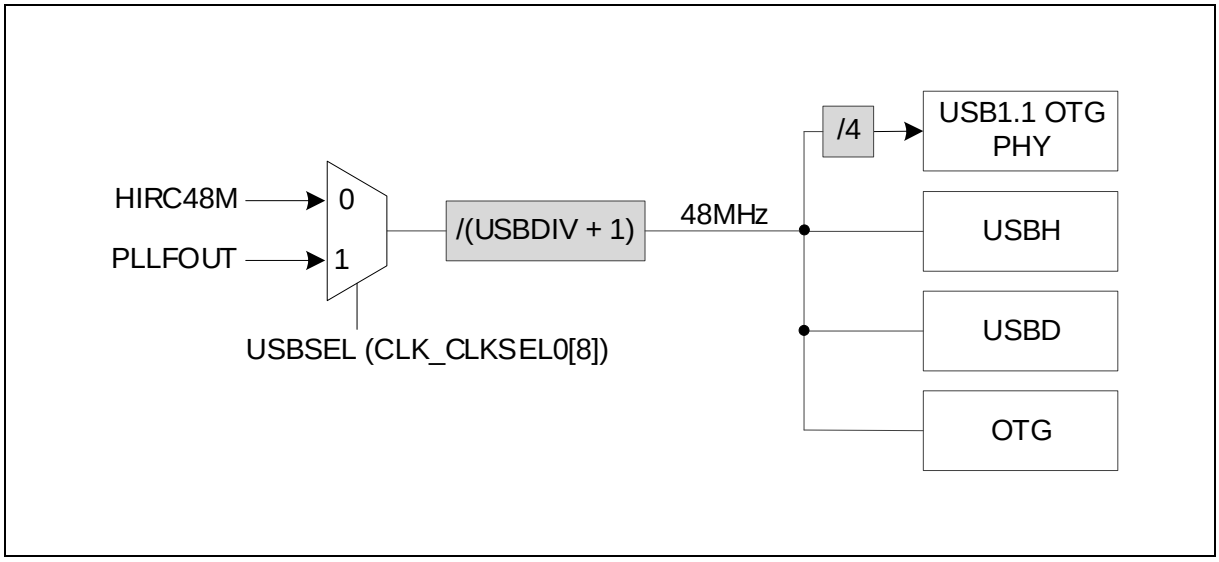



Figure 6.3-9 USB Clock Block Diagram

## 6.4 True Random Number Generator (TRNG)

### 6.4.1 Overview

This is a True Random Number Generator (TRNG) consists of an entropy source from analog macro and a CTR_DRBG. It can generate true random number by analog macro. There is a calibration mechanism of internal TRNG for randomness of generating true random number. Besides, there is a CTR_DRBG design in this TRNG for the DRBG (deterministic random bit generator) of SP800-90A and the NRBG (non-deterministic random bit generator) of SP800-90C.

### 6.4.2 Features

- Up to 10Mbit/s data rate for entropy source
- Pass NIST SP800-22A standard
- Include NIST SP800-90A known answer test for DRBG and NIST SP800-90B health test for entropy source (Start-up test, Repetition count test, Adaptive proportion test).
- Provides the true random number seed for PRNG

## 6.5 RRAM Memory Controller (RMC)

### 6.5.1 Overview

The RRAM memory controller (RMC) is equipped with 512/256/128/64 Kbytes on-chip embedded RRAM for application and configurable Data RRAM to store some application dependent data. Thus, the total size of application rom (APROM) is 512/256/128/64 Kbytes. This chip supports Dual-bank RRAM macro for safe firmware upgrade. A User Configuration block provides for system initiation. A 8 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 16 Kbytes Bootloader consists of native ISP functions and secure boot function. A 2 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data. 4 Kbytes cache with zero wait cycle is used to improve RRAM access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded RRAM is updated.

### 6.5.2 Features

- Supports Dual-bank RRAM macro for safe firmware upgrade
- Supports Dual-bank remapping
- Supports 512/256/128/64 Kbytes application ROM (APROM)
- Supports 8 Kbytes loader ROM (LDROM)
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM
- Supports Data RRAM with configurable memory size
- Supports 256 bytes User Configuration block to control system initiation
- Supports 2 Kbytes one-time-program ROM (OTP)
- Supports Bootloader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for code integrity and authenticity
- Supports 32-bit and word line RRAM programming function
- Supports CRC32 checksum calculation function
- Supports RRAM all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded RRAM memory
- Supports cache memory to improve RRAM access performance and reduce power consumption

| RMC Features | M2L31xxDAE | M2L31xx4AE |
|---|---|---|
| Dual-bank RRAM macro | ● | |

Table 6.5-1 RMC Features Comparison Table at Different Chip

## 6.6 General Purpose I/O (GPIO)

### 6.6.1 Overview

This chip has up to 109 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 109 pins are arranged in 8 ports named as PA, PB, PC, PD, PE, PF, PG and PH. PA, PB, PD and PE has 16 pins on port. PC has 15 pins on port. PF has 12 pins on port. PG has 10 pins on port. PH has 8 pins on port. Each of the 109 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode.

### 6.6.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function

## 6.7 Low Power General Purpose I/O (LPGPIO)

### 6.7.1 Overview

This chip has up to 8 Low Power General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 8 pins are named as LPIO0, LPIO1, LPIO2, LPIO3, LPIO4, LPIO5, LPIO6 and LPIO7. Each of the 8 pins is independent and has the corresponding register bits to control the pin function and data. These 8 pins also support output data set/reset registers to allow individual set/reset bitwise control.

### 6.7.2 Features

- Supports function operating in NPD0/1/2/3/4
- Two I/O modes:
  - Push-Pull Output mode
  - Input only with high impendence mode
- Supports pin output data individual bit set/reset

## 6.8 PDMA Controller (PDMA)

### 6.8.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. PDMA can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. PDMA has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

### 6.8.2 Features

- Supports 16 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and USB, UART, USCI, SPI, QSPI, ACMP, PWM, EINT, EPWM, $I^2C$, Timer, EADC, and DAC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports 2 time-out function channels

## 6.9 Low Power PDMA Controller (LPPDMA)

### 6.9.1 Overview

The low power peripheral direct memory access (LPPDMA) controller is used to provide high-speed data transfer. LPPDMA can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. LPPDMA has a total of 4 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

### 6.9.2 Features

- Supports 4 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and LPUART, LPSPI, LPI$^2$C, LPTIMER, TTIMER, LPADC and ACMP request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type

## 6.10 External Bus Interface (EBI)

### 6.10.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

### 6.10.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplex mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

## 6.11 Timer Controller (TMR)

### 6.11.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (TMx or TMx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

### 6.11.2 Features

*6.11.2.1 Timer Function Features*

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC, MIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, PWM, EADC, LPADC, DAC, EQEI, and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP0 output, ACMP1 output, ACMP2 output or internal USB SOF signal
- Supports Timer0~3 time-out interrupts signal (TIF) to trigger Touch-Key scan.
- Supports internal capture triggered source from ACMP0 output, ACMP1 output, ACMP2 output, HXT, HIRC, LIRC, MIRC and LXT.

*6.11.2.2 PWM Function Features*

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256

- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels
- Supports interrupt on the following events:
  - PWM period point, up-count compared point events
- Supports wake-up when interrupt occurs when clock source is LXT or LIRC
- PWM can generate output in Power-down mode
- Supports trigger EADC, LPADC, PDMA, and DAC on the following events:
  - PWM period point and up-count compared point events
- Supports PWM output accumulator event to trigger PDMA transfer and EADC
- Supports PWM output accumulator event to stop PWM counting

## 6.12 Low Power Timer Controller (LPTMR)

### 6.12.1 Overview

The low power timer controller includes two 32-bit timers, LPTMR0 ~ LPTMR1, allowing user to easily implement a timer control for applications. The low power can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The low power timer controller also provides two PWM generators. Each PWM generator supports one PWM output and two selectable PWM output channels (LPTMRx or LPTMRx_EXT). The output state of PWM output pin can be control by polarity control, output enable control and output channel select.

### 6.12.2 Features

*6.12.2.1 Low Power Timer Function Features*

- Two sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (LPTMRx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (LPTMRx_CAP[23:0])
- Supports external capture pin (LPTMRx_EXT) event for interval measurement
- Supports external capture pin (LPTMRx_EXT) event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt signal or capture interrupt signal to trigger LPADC0, , LPI2C0, LPSPI0, LPUART, , and LPPDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports event counting source from ACMP0 output, ACMP1 output or ACMP2 output
- Supports internal capture triggered source from ACMP0 output, ACMP1 output and ACMP2 output

*6.12.2.2 PWM Function Features*

- Supports PWM generator with two selectable output channels
- Supports 16-bit PWM counter
  - Up count operation type
  - One-shot or auto-reload counter operation mode
- Supports 8-bit prescale from 1 to 256
- Supports 16-bit compare register and period register and double buffer for period register and compare register
- Supports tri-state enable and polarity control for each PWM selectable output channels
- Supports interrupt on the following events:
  - PWM period point, up-count compared point events

- Supports wake-up when interrupt occurs when clock source is LXT or LIRC
- PWM can generate output in Power-down mode
  - Supports trigger LPADC, LPPDMA, and on the following events:
  - PWM period point and up-count compared point events
- Supports PWM output accumulator event to trigger LPPDMA transfer and LPADC
- Supports PWM output accumulator event to stop PWM counting
- Support automatic operation mode

## 6.13 Tick Timer Controller (TTMR)

### 6.13.1 Overview

The tick timer controller includes two 32-bit timers, TTMR0 ~ TTMR1, allowing user to easily implement a timer control for applications. The tick timer can perform functions, such as, delay timing,.

### 6.13.2 Features

#### *6.13.2.1 Tick Timer Function Features*

- Two sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TTMRx_CNT[23:0])
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports time-out interrupt signal to trigger LPADC0, LPI2C0, LPSPI0, LPUART, , and LPPDMA function

## 6.14 PWM Generator and Capture Timer (PWM)

### 6.14.1 Overview

The chip provides two PWM generators — PWM0 and PWM1. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for EADC, LPADC and DAC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

### 6.14.2 Features

#### *6.14.2.1 PWM Function Features*

- Supports maximum clock frequency up to maximum 72MHz frequency
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin, analog comparator, UTCPD, EADC result monitor and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/LPADC/DAC on the following events:
  - PWM counter matches 0, period value or compared value
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports PWM output accumulator stop counter mode
- Support External Pin Trigger Function

#### *6.14.2.2 Capture Function Features*

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

## 6.15 EPWM Generator and Capture Timer (EPWM)

### 6.15.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events are used to generate EPWM pulse, interrupt and trigger signal for EADC, LPADC and DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC/LPADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also supports PDMA to transfer captured data to memory.

### 6.15.2 Features

#### *6.15.2.1 EPWM Function Features*

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion independent control with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator, UTCPD, EADC0 result monitor and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed

- Supports interrupt on the following events:
  - EPWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger EADC/LPADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC/LPADC)
  - Supports EPWM trigger EADC/LPADC event prescaler feature
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect function
- Supports External Pin Trigger Function

#### *6.15.2.2 Capture Function Features*

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

## 6.16 Enhanced Quadrature Encoder Interface (EQEI)

### 6.16.1 Overview

There are two EQEI controllers in this device. The Enhanced Quadrature Encoder Interface (EQEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

### 6.16.2 Features

*6.16.2.1 Enhanced Quadrature Encoder Interface (EQEI) Features*

- Up to two EQEI controllers, EQEI0 and EQEI1.
- Two EQEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (EQEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (EQEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (EQEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (EQEI_CNTCMP) with a Pre-set Maximum Count Register (EQEI_CNTMAX)
- A 32-bit up count Unit Timer Pulse Counter (EQEI_UTCNT)
- A 32-bit Unit Timer Pulse Counter Compare Register (EQEI_UTCMP)
- Two EQEI control registers (EQEI_CTL and QEI_CTL2) and one EQEI Status Register (EQEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Supports X4 free-counting mode
  - Supports X2 free-counting mode
  - Supports X4 compare-counting mode
  - Supports X2 compare-counting mode
- Two Quadrature encoder phase counter operation modes:

  - Supports X1 1-phase 2 input compare-counting mode

  - Supports X2 1-phase 2 input compare-counting mode
- Two Quadrature encoder directional counter operation modes:

  - Supports X1 1-phase 1 input compare-counting mode

  - Supports X2 1-phase 1 input compare-counting mode
- Supports swap function for input signals QEA and QEB
- Supports for detecting the occurrence of phase error from input signals QEA and QEB
- Supports one times index signal reset function for Quadrature encoder pulse counter
- Encoder Pulse Width measurement mode by ECAP
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clock/8

## 6.17 Enhanced Input Capture Timer (ECAP)

### 6.17.1 Overview

The chip provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

### 6.17.2 Features

- Up to two Input Capture Timer/Counter units, CAP0 and CAP1.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

## 6.18 Watchdog Timer (WDT)

### 6.18.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

### 6.18.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval ($2^4$ ~ $2^{20}$) and the time-out interval is 0.5 ms ~ 32.768 s if WDT_CLK = 32 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

## 6.19 Window Watchdog Timer (WWDT)

### 6.19.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

### 6.19.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

## 6.20 Real Time Clock (RTC)

### 6.20.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

### 6.20.2 Features

- Supports external power pin $V_{BAT}$.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up to 3 individual tamper pins.
- Supports 20 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports RRAM mass erase operate will also clear the 20 bytes spare registers content.

## 6.21 I²C Serial Interface Controller (I²C)

### 6.21.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are four sets of I²C controllers which support Power-down Wake-up function.

### 6.21.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to four I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable
- Add pin swap function
- Supports Bus Management (SM/PM compatible) function Compatible with the SMBUS Specification Rev 2.0 (http://smbus.org/specs/) and PMBUS Specification Rev 1.2 (http://pmbus.org/)

## 6.22 Low Power I²C Serial Interface Controller (LPI2C)

### 6.22.1 Overview

LPI2C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices.

There is one set of LPI2C controller which supports Power-down Wake-up function.

### 6.22.2 Features

The LPI2C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of LPI2C bus include:

- Supports one LPI2C port
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) when clock source is greater than 20 MHz
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the LPI2C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports LPPDMA with one buffer capability
- Supports setup/hold time programmable
- Add pin swap function
- Supports auto-operation mode
- Supports trigger source from LPTMR0/1, TTMR0/1 and WKIOA/B/C/D rising/falling edge event

## 6.23 USCI - Universal Serial Control Interface Controller (USCI)

### 6.23.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or $I^2C$ functional protocol.

### 6.23.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- $I^2C$

## 6.24 USCI – UART Mode

### 6.24.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

### 6.24.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

## 6.25 USCI - SPI Mode

### 6.25.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

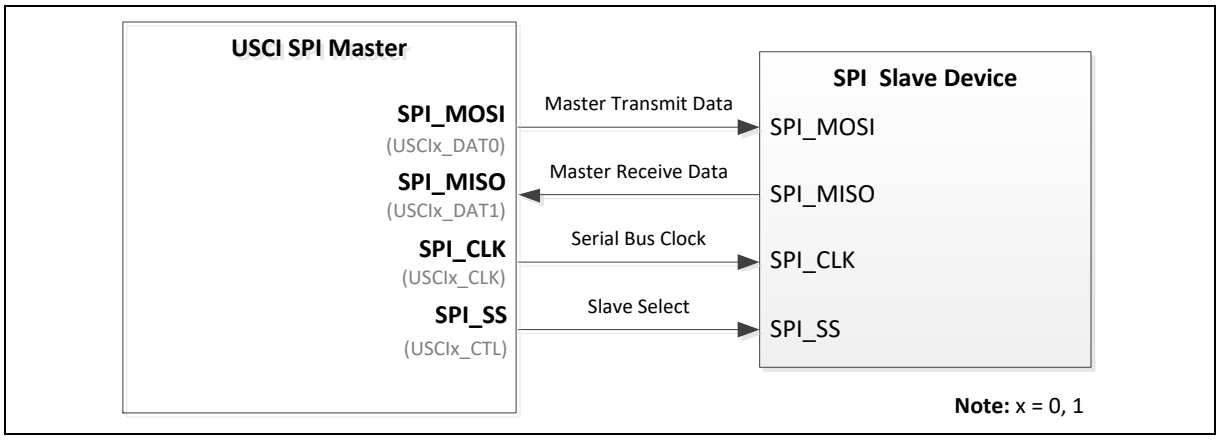



Figure 6.25-1 SPI Master Mode Application Block Diagram

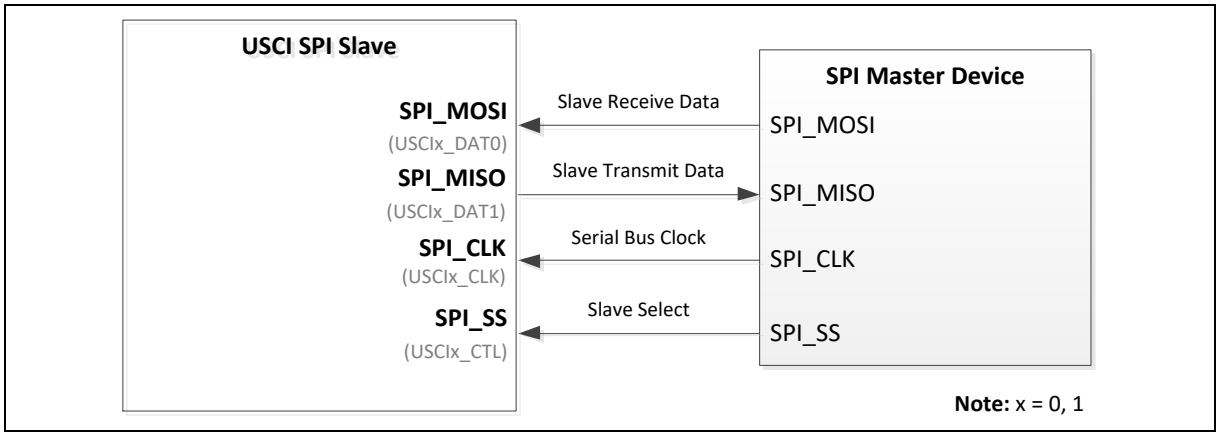



Figure 6.25-2 SPI Slave Mode Application Block Diagram

### 6.25.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < $f_{PCLK}$ / 2, Slave < $f_{PCLK}$ / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function

- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

## 6.26 USCI - I²C Mode

### 6.26.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.26-1 for more detailed I²C BUS Timing.

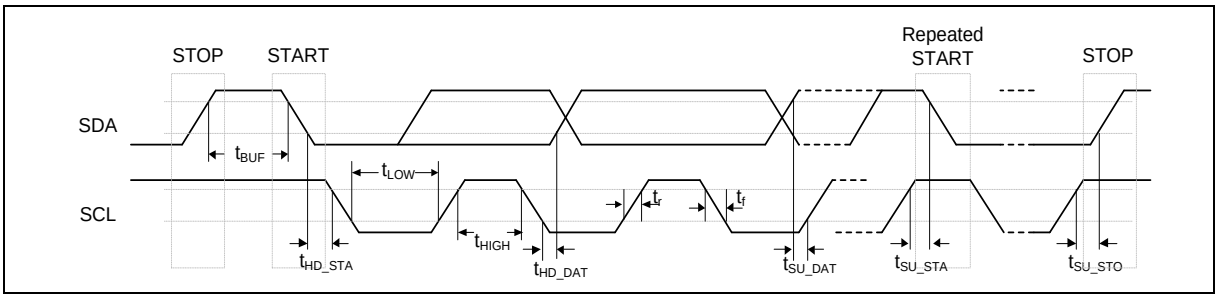



Figure 6.26-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

**Note:** Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

### 6.26.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

## 6.27 UART Interface Controller (UART)

### 6.27.1 Overview

The chip provides eight channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports eleven types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

### 6.27.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

| UART Feature | UART0/ UART1 | UART2 ~ UART7 | USCI-UART |
|---|---|---|---|
| FIFO | 16 Bytes | 16 Bytes | TX: 1byte<br>RX: 2byte |
| Auto Flow Control (CTS/RTS) | √ | √ | √ |
| IrDA | √ | √ | - |
| LIN | √ | - | - |
| RS-485 Function Mode | √ | √ | √ |
| nCTS Wake-up | √ | √ | √ |
| Incoming Data Wake-up | √ | √ | √ |
| Received Data FIFO reached threshold Wake-up | √ | √ | - |
| RS-485 Address Match (AAD mode) Wake-up | √ | √ | - |
| Received Data FIFO reached threshold Time-out Wake-up | √ | √ | - |
| Baud Rate Compensation | √ | √ | - |
| Auto-Baud Rate Measurement | √ | √ | √ |
| STOP bit Length | 1, 1.5, 2 bit | 1, 1.5, 2 bit | 1, 2 bit |
| Word Length | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 6~13 bits |
| Even / Odd Parity | √ | √ | √ |
| Stick Bit | √ | √ | - |

Table 6.27-1 M2L31 Series UART Features

## 6.28 Low Power UART Interface Controller (LPUART)

### 6.28.1 Overview

The chip provides one channel of Low Power Universal Asynchronous Receiver/Transmitters (LPUART). The LPUART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each LPUART controller channel supports ten types of interrupts. The LPUART controller supports flow control function. The LPUART controller also supports RS-485 and Single-wire function modes and auto-baud rate measuring function.

### 6.28.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (LPUART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for LPUART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enabled to program nRTS pin to control RS-485 transmission direction
- Supports LPPDMA transfer function
- Supports Single-wire function mode.
- Supports Automatic Operation

| LPUART Feature | LPUART0 | UART0/ UART1 | UART2 ~ UART7 | USCI-UART |
|---|---|---|---|---|
| FIFO | 16 Bytes | 16 Bytes | 16 Bytes | TX: 1byte<br>RX: 2byte |
| Automatic Operation | √ | - | - | - |

| | | | | |
|---|---|---|---|---|
| Auto Flow Control (CTS/RTS) | √ | √ | √ | √ |
| RS-485 Function Mode | √ | √ | √ | √ |
| nCTS Wake-up | √ | √ | √ | √ |
| Incoming Data Wake-up | √ | √ | √ | √ |
| Received Data FIFO reached threshold Wake-up | √ | √ | √ | - |
| RS-485 Address Match (AAD mode) Wake-up | √ | √ | √ | - |
| Received Data FIFO reached threshold Time-out Wake-up | √ | √ | √ | - |
| Baud Rate Compensation | √ | √ | √ | - |
| Auto-Baud Rate Measurement | √ | √ | √ | √ |
| STOP bit Length | 1, 1.5, 2 bit | 1, 1.5, 2 bit | 1, 1.5, 2 bit | 1, 2 bit |
| Word Length | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 5, 6, 7, 8 bits | 6~13 bits |
| Even / Odd Parity | √ | √ | √ | √ |
| Stick Bit | √ | √ | √ | - |

Table 6.28-1 M2L31 Series LPUART Features

## 6.29 Serial Peripheral Interface (SPI)

### 6.29.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports $I^2S$ mode to connect external audio CODEC.

### 6.29.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 72 MHz (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Slave mode up to 36 MHz (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- $I^2S$ Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, $I^2S$ and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

## 6.30 Low Power Serial Peripheral Interface (LPSPI)

### 6.30.1 Overview

The Low Power Serial Peripheral Interface (LPSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of LPSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The LPSPI controller can be configured as a master device and supports the PDMA function to access the data buffer, or configured as a slave device and monitor the signal level change of SS to wake up system.

### 6.30.2 Features

- SPI Mode
  - One set of LPSPI controller
  - Supports Master or Slave mode operation
  - Master mode up to 12 MHz (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Slave mode up to 6 MHz when SPI master device supports adjustment function of RX data sampling clock (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Slave mode up to 6 MHz when SPI master device does not support adjustment function of RX data sampling clock (when chip works at $V_{DD}$ = 2.7~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
  - Supports automatic operation mode

## 6.31 Quad Serial Peripheral Interface (QSPI)

### 6.31.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one QSPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

### 6.31.2 Features

- Supports Master or Slave mode operation
- Master mode up to 36 MHz (when chip works at $V_{DD}$ = 2.7V~3.6V)
- Slave mode up to 24 MHz (when chip works at $V_{DD}$ = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

## 6.32 USB 2.0 Full-Speed Device Controller (USBD)

### 6.32.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbyte sizes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SIE. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEG0~18).

There are 19 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are four different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, like IN ACK, OUT ACK and BUS events, like suspend and resume. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0~3) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

### 6.32.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBDET, USB, BUS and SOF)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 19 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbyte buffer size
- Provides remote wake-up capability
- Supports double buffer function

## 6.33 USB 1.1 Host Controller (USBH)

### 6.33.1 Overview

This chip is equipped with a USB 1.1 Host Controller (USBH) that supports Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

### 6.33.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 1.1.
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports both full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt and Isochronous transfers.
- Supports an integrated Root Hub.
- Supports a USB host port shared with USB device (OTG function).
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

## 6.34 USB On-The-Go (OTG)

### 6.34.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of a USB 1.1 host controller and a USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

A USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, the USB frame acts as USB host. The USB frame can support both full-speed and low-speed transfer. In Device-only mode, the USB frame acts as USB device. USB device support full-speed transfer. In ID dependent mode, the USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. OTG specification support full-speed transfer whether OTG device acts as a host or peripheral.

### 6.34.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The role of USB frame is only dependent on USB_ID pin value--as USB Host (USB_ID pin is low) or USB Device (USB_ID pin is high). HNP or SRP protocol is not supported.
  - OTG device: dependent on USB_ID pin status to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). HNP and SRP protocols are supported.

## 6.35 USB Type C Power Delivery Controller (UTCPD)

### 6.35.1 Overview

The UTCPD is a USB Type-C Power Delivery controller. UTCPD integrates a Power Delivery PHY with BMC encoding and decoding, protocol layer function and USB Type-C Configuration Channel (CC) logic to fulfill USB Type-C CC sensing and control and USB PD message delivery function.

UTCPD is compliant with USB Type-C 1.2 and USB Power Delivery3.0.

### 6.35.2 Features

- Basic Functionality
  - Compliant with USB Type-C Cable and Connector Specification Rev1.2 (TYPE-C)
  - Supports UFP, DFP and DRD data roles
  - Supports Sink, Source and DRP power roles
  - Dual-Role Power functionality with Autonomous DRP toggle
  - Supports CC1 and CC2 signals
    - Internal Rp and Rd
    - Default, 1.5A and 3A current sourcing advertising
    - Support dead battery
    - Detects cable orientation
    - Transmits and receives BMC encoded, PD messages
    - Transmits and receives Fast Role Swap (FRS) requests
    - Detects $V_{BUS}$ presence
  - Monitors $V_{BUS}$ voltage,using system EADC
  - Debounces attachment detection on either $V_{BUS}$ or CCx signals
  - Detects connection removal via either $V_{BUS}$ or CC*x* signals
- Power Delivery Functionality
  - Compliant with USB Power Delivery Specification Rev3.0, V1.2 (PD)
  - Transmits and receives serial data via CC*x* signals:
    - Limits the slew rate of the transmitted signal
    - Filters the received signal
  - Supports Power Delivery PHY Layer
    - Performs BMC and 4b5b encoding/decoding of the transmitted and received data bits stream
    - Generates and decodes Preamble, SOP and EOP
    - Appends and checks CRC
    - Generates and receives Hard Reset
    - Generates and receives Cable Reset
    - Supports Carrier Mode 2 and Test data, BIST modes
  - Supports Power Delivery Protocol Layer

- Supports SOP', SOP" and SOP messages
- Implements and checks the MessageID counter
- Supports Control messages ：Automatically generates GoodCRC response
- Supports Control messages ：Generates Hard Reset
- Supports Data messages with up to 30 data bytes：Supports Vendor Defined Messages (VDM)
- Supports Data messages with up to 30 data bytes：Supports long messages via Chunking
- Has separate transmit and receive buffers
- Supports up to three automatic retries
- Supports Data role, power role and $V_{CONN}$ swapping
- Implements the timing critical functions of the PD protocol, such as waiting for a GoodCRC response

- System Control and Monitoring
  - Provides controls for $V_{BUS}$ both "force" and "bleed" bulk capacitors discharge
    - Discharge signal is controlled by monitoring the actual VBus voltage level
- Wake-up from Idle mode and NPD0~2

## 6.36 Controller Area Network with Flexible DataRate (CAN FD)

### 6.36.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and need be connected to additional transceiver hardware for the physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock (HCLK). In order to achieve a stable function of the CAN FD controller, the AHB clock must always be faster than or equal to the CAN core clock.

### 6.36.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Up to 64/32 Receive buffers/Transmit Buffers
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

## 6.37 Key Store (KS)

### 6.37.1 Overview

The Key Store (KS) is a key management device for key storage. The Key Store is capable of providing a crypto engine to access or store the key while encryption, decryption and generation. The Key Store supports revoke key operation if key is unused. The Key Store is able to protect the key by integrity checking and auto verifying.

### 6.37.2 Features

- Supports programming interface for key management
- Supports key size 256-bit required for Cryptography engine
- Supports 2 OTP keys, maximum key size is 256-bit
- Supports crypto engine access Key Store directly
- Supports revoke operation
- Supports revoke key in OTP while tamper detected
- Supports integrity checking
- Supports auto verify function
- Supports lock function

## 6.38 Cryptographic Accelerator (CRYPTO)

### 6.38.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255, and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, and CBC-CS3 mode.

| Section | M2L31xxDAE | M2L31xx4AE |
|---|---|---|
| Cryptographic Accelerator | ● | - |

Table 6.38-1 Cryptographic Features Comparison Table at Different Chip

### 6.38.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255, and 256 bits random number generation
  - Able to take the true random number seed from TRNG
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports key expander for key expansion in FIPS NIST 197

## 6.39 Touch Key (TK)

### 6.39.1 Overview

The capacitive touch key sensing controller supports several programmable sensitivity levels for different applications to detect the finger touched or near the electrode covered by dielectric. It supports up to 16 touch keys with single-scan or programmable periodic key-scans, and system can be woken up by any key for low power applications.

### 6.39.2 Features

- Supports up to 16 touch keys
- Supports flexible reference pad and shielding electrode channel setting; at least 1 reference pad channel and 1 shielding electrode channel are needed
- Programmable sensitivity levels for each channel
- Programmable scanning speed for different applications
- Supports any touch key wake-up for low-power applications
- Supports single key-scan and programmable periodic key-scan
- Programmable interrupt options for key-scan complete with or without threshold control
- Supports independent reference capacitor bank(CB) registers for each channels
- Supports Timer0~3 time-out interrupts signal(TIF) to trigger touch key scan
- Supports RTC tick event to trigger touch key scan

## 6.40 CRC Controller (CRC)

### 6.40.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with three common polynomials CRC-8, CRC-16, CRC-32, and 32-bit programmable polynomials settings.

### 6.40.2 Features

- Supports three common polynomials CRC-8, CRC-16, and CRC-32
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports Master mode

## 6.41 Analog Comparator Controller (ACMP)

### 6.41.1 Overview

The chip provides three comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

### 6.41.2 Features

- Analog input voltage range: 0 ~ $AV_{DD}$ (voltage of $AV_{DD}$ pin)
- Up to three rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV,-, 20mV,-, 40mV,
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 7 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, ACMP0_P3, OPA0_int_OUT, OPA1_int_OUT or OPA2_int_OUT
  - 5 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage ($V_{BG}$)
    - DAC0 output (DAC0_OUT)
    - DAC1 output (DAC1_OUT)
- ACMP1 supports:
  - 7 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, ACMP1_P3, OPA0_int_OUT, OPA1_int_OUT or OPA2_int_OUT
  - 5 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage ($V_{BG}$)
    - DAC0 output (DAC0_OUT)
    - DAC1 output (DAC1_OUT)
- ACMP2 supports:
  - 7 multiplexed I/O pins at positive sources:
    - ACMP2_P0, ACMP2_P1, ACMP2_P2, ACMP2_P3, OPA0_int_OUT, OPA1_int_OUT or OPA2_int_OUT
  - 5 negative sources:
    - ACMP2_N

- Supports Comparator Reference Voltage (CRV2)
- Internal band-gap voltage ($V_{BG}$)
- DAC0 output (DAC0_OUT)
- DAC1 output (DAC1_OUT)

- ACMP0 and ACMP1 share one ACMP interrupt vector, and ACMP2 use one ACMP interrupt vector
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode
- Supports offset calibration
- Supports ACMP0 event, ACMP1 event, ACMP2 event be as PDMA request source
- Supports ACMP0 event, ACMP1 event, ACMP2 event be as EADC trigger source
- Supports ACMP0 output, ACMP1 output, ACMP2 output be as Timer, LPTimer, ECAP,LPADC, PWM and EPWM trigger source
- Supports ACMP0 interrupt flag, ACMP1 interrupt flag, ACMP2 interrupt flag be as UTCPD trigger source

## 6.42 Enhanced 12-bit Analog-to-Digital Converter (EADC)

### 6.42.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR EADC converter) with 24 external input channels and 7 internal channels. The EADC converter can be started by software trigger, EPWM0/1 triggers, PWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger, external pin (EADC0_ST) input signal, and ACMP0~2 triggers.

### 6.42.2 Features

- Analog input voltage range: 0~ $V_{REF}$ (Max to 3.6V)
- Reference voltage from $V_{REF}$ pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 24 single-end analog external input channels or 8 pair differential analog input channels
- Up to 7 internal channels, they are AN_OPA0_OUT, AN_OPA1_OUT, AN_OPA2_OUT, $AV_{DD}/4$, band-gap voltage ($V_{BG}$), temperature sensor ($V_{TEMP}$), and battery power/4 ($V_{BAT}/4$).
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 72 MHz for EADC
- Up to 3.42 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage $V_{REF}$: 1.6V, 2V, 2.5V and 3V.
- Supports power-down mode
- Up to 31 sample modules
  - Sample module 0~26 is configurable for EADC converter channel (EADC_CH0~23, AN_OPA0_OUT, AN_OPA1_OUT, AN_OPA2_OUT) and trigger source for each EADC.
  - Sample module 27~30 are fixed for input sources $AV_{DD}/4$, band-gap voltage, temperature sensor, and battery power/4 ($V_{BAT}/4$), respectively.
  - Double buffer for sample control logic module 0~3.
  - Configurable sampling time for each sample module.
  - Conversion results are held in 31 data registers with valid and overrun indicators.
- Averaging ($2^n$ times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, ($2^n$ times, n=0~8) to support up to 16-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~30)
  - External pin EADC0_ST trigger
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/PWM triggers

  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay counter
  - ACMP0, ACMP1, and ACMP2 interrupt pulse triggers
- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode

## 6.43 Low Power Analog-to-Digital Converter (LPADC)

### 6.43.1 Overview

LPADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 24 input channels. The A/D converter supports four operation modes: Single, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (LPADC0_ST), Timer 0~3 overflow pulse trigger, EPWM trigger, PWM trigger and ACMP0_O/ACMP1_O/ACMP2_O edge event. The A/D converter can also be triggered to start by software write 1 to SWTRIG (LPADC_AUTOSTRG[0]), Low power timer 0/1, Tick timer, Wake-up I/O or ACMP at auto-operation mode

### 6.43.2 Features

- Operating voltage: 1.8V~3.6V
- Analog input voltage: 0 ~ $AV_{DD}$
- Supports external reference voltage from $V_{REF}$ pin.
- 12-bit resolution and 10-bit accuracy guaranteed
- Up to 24 single-end analog input channels or 12 differential analog input channels
- Maximum LPADC peripheral clock (LPADC_CLK) frequency is 12 MHz
- Up to 571 KSPS sampling rate
- Scan on enabled channels
- Threshold voltage detection
- Three operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (LPADC0_ST)
  - Timer 0~3 overflow pulse trigger
  - EPWM trigger
  - PWM trigger
  - ACMP0_O/ ACMP1_O/ ACMP2_O edge event
- Supports auto-operation mode with A/D conversion that can be started by:
  - Software Write 1 to SWTRIG bit
  - Low power Timer 0/1
  - Tick Timer 0/1
  - ACMP analog ouput 0/1(ACMPS0/ ACMPS1) edge event
- Each conversion result held in data register of each channel with valid and overrun indicators

- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~16383 LPADC clock)
- Seven internal channels from band-gap voltage ($V_{BG}$), temperature sensor ($V_{TEMP}$), $V_{BAT}$ voltage divided by 4, $AV_{DD}$ voltage divided by 4 and three OPAs.
- Supports LPPDMA transfer mode
- Supports Calibration mode
- Supports Floating Detect Function

**Note 1:** LPADC sampling rate = (LPADC peripheral clock frequency) / (total LPADC conversion cycle)

**Note 2:** If the internal channel for band-gap voltage is active, the maximum sampling rate will be 100 KSPS.

**Note 3:** LPADC peripheral clock frequency must be slower than or equal to PCLK2.

## 6.44 Digital to Analog Converter (DAC)

### 6.44.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

### 6.44.2 Features

- Analog output voltage range: 0~$AV_{DD}$.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), $V_{REF}$ pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, PWM0, PWM1 and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

## 6.45 OP Amplifier (OPA)

### 6.45.1 Overview

This device is equipped with three operational amplifiers. Users can enable each of them individually by their application purpose.These three OP amplifier circuits can also be used in the application of Programmable Gain Amplifier (PGA) or OPA mode, unit-gain mode.

### 6.45.2 Features

- Analog input voltage range: 0~$V_{DD}$.
- Supports up to 3 operational amplifiers
- Supports to use Schmitt trigger buffer output for simple comparator function
- Supports Schmitt trigger buffer output interrupts.
- Supports wake-up function
- PGA with non-inverting gain setting:
  - 2x, 4x, 8x, 16x, 32x
- PGA with inverting gain setting:
  - -1x, -3x, -7x, -15x, -31x
- 8 MHz gain bandwidth product

## 6.46 Peripherals Interconnection

### 6.46.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

### 6.46.2 Peripherals Interconnect Matrix Table

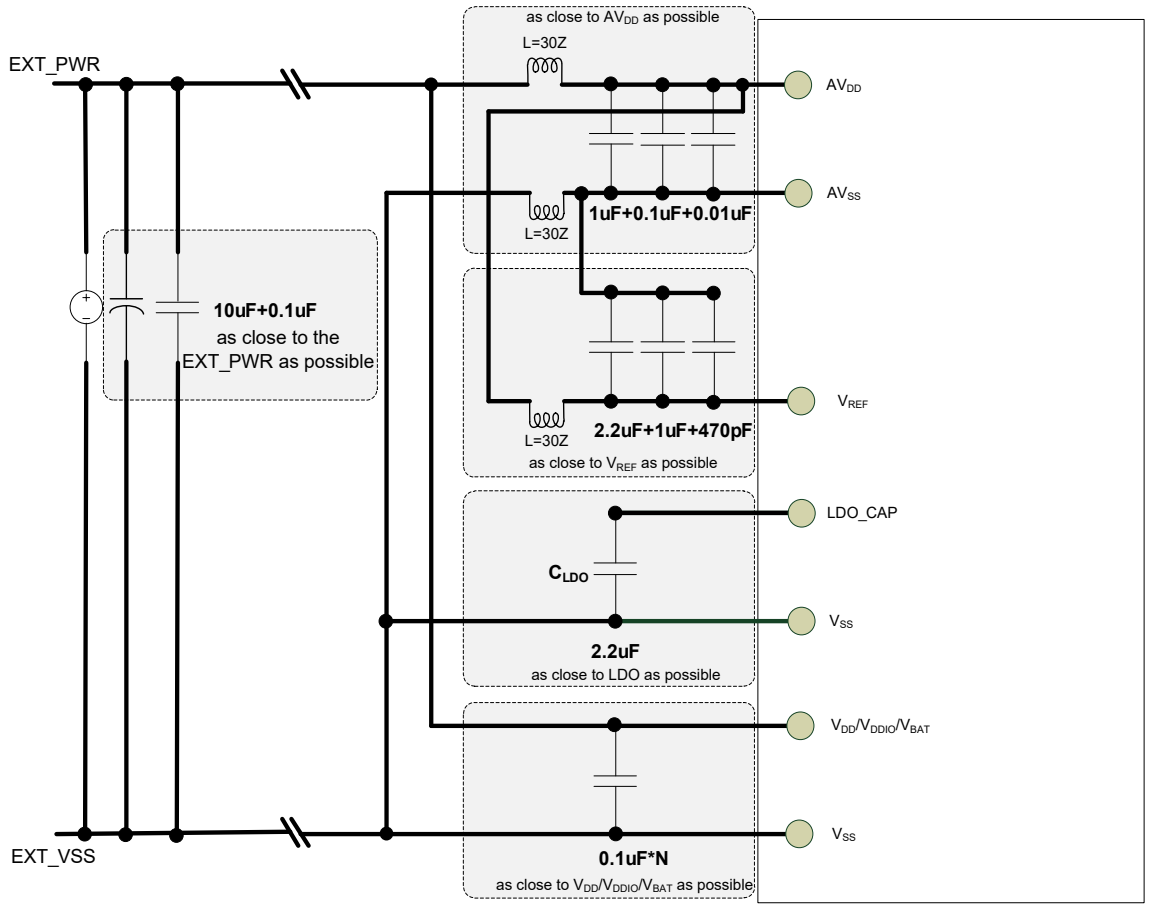
Please refer to the relative Technical Reference Manual for detailed functional description about the peripherals interconnection.

| Source | | Destination | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | EADC | LPADC | ACMP | | DAC | OPA | TMR | EPWM | PWM | SYSTEM | ECAP | EQEI | TK | UTCPD | LPTMR | LPUART | LPI2C | LPSPI | LPDMA |
| | | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ | ↘ |
| ACMP | √ | √ | √ | - | - | - | - | √ | √ | √ | - | √ | - | - | √ | √ | - | - | - | - |
| | √ | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| CLKCTL | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| DAC | √ | - | - | √ | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - |
| EADC | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | √ | - | - | - | - | - |
| EPWM | √ | √ | √ | - | - | √ | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| EQEI | √ | - | - | - | - | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - |
| GPIO | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | √ | - | - | - | - | - |
| LPADC | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | √ |
| LPI2C | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | √ |
| LPSPI | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | √ |
| LPTMR | √ | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | √ | √ | √ | √ |
| LPUART | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | √ |
| OPA | √ | √ | √ | √ | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - |
| PWM | √ | √ | √ | - | - | √ | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| RTC | √ | √ | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | √ | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | - | - | - | - | - | - | √ | - | - | - | - | - | - |
| SYSTEM | √ | √ | √ | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | √ | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | √ | √ | - | √ | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | √ | - | - | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |
| | √ | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | √ | √ | √ | - |
| TMR | √ | √ | √ | - | - | √ | - | √ | √ | √ | - | - | √ | √ | - | - | - | - | - | - |
| TTMR | √ | - | √ | - | - | - | - | - | - | - | - | - | - | - | - | - | √ | √ | √ | √ |
| USB1 | √ | - | - | - | - | - | - | √ | - | - | √ | - | - | - | - | - | - | - | - | - |
| UTCPD | √ | - | - | - | - | - | - | - | √ | √ | - | - | - | - | - | - | - | - | - | - |

Table 6.45-1 Peripherals Interconnect Matrix Table

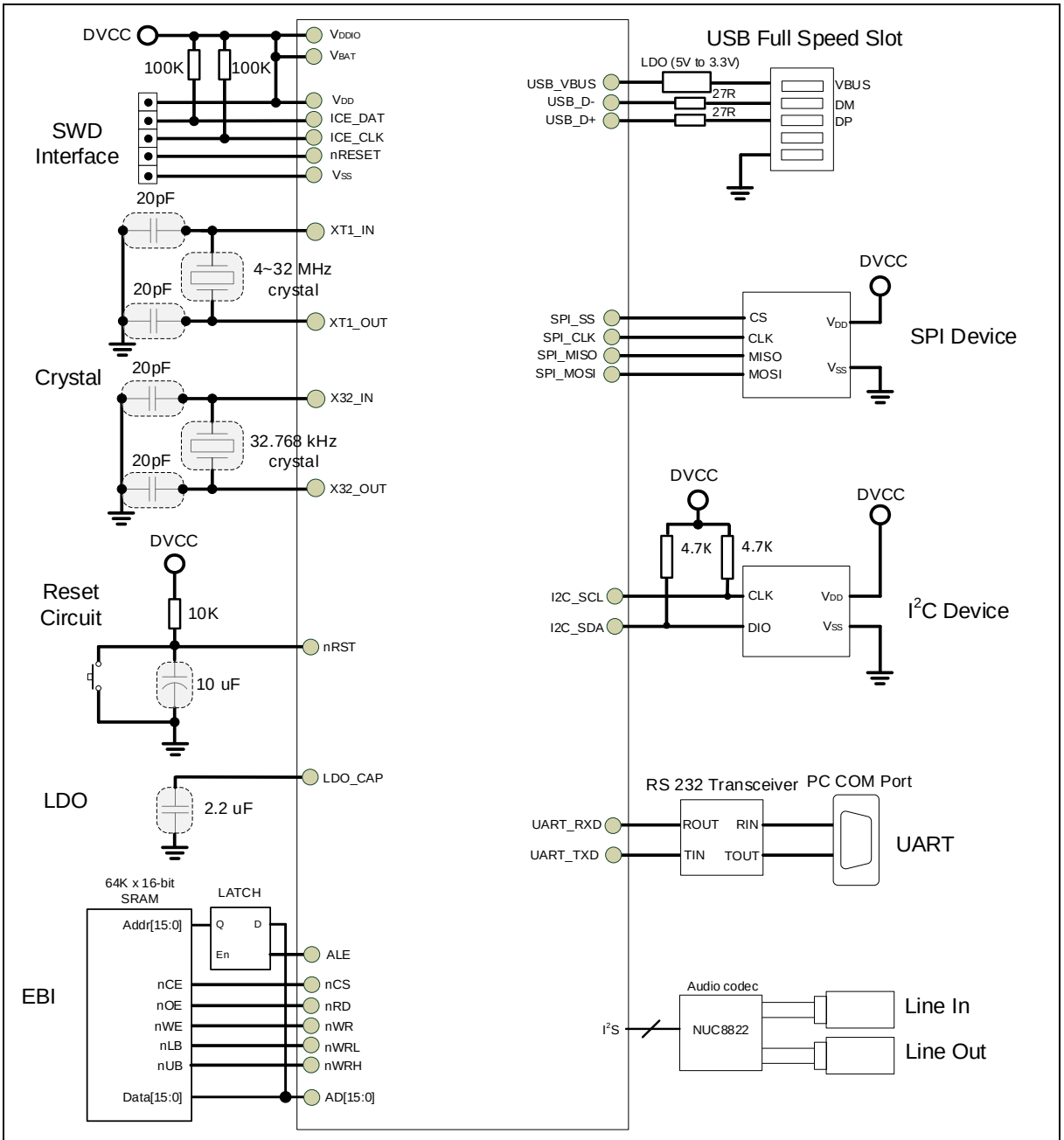
# 7 APPLICATION CIRCUIT

## 7.1 Power Supply Scheme




**Note:** $C_{LDO}$ must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

## 7.2 Peripheral Application Scheme




**Note 1:** It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

**Note 2:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

**Note 3:** $C_{LDO}$ must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

# 8 ELECTRICAL CHARACTERISTICS

## 8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

### 8.1.1 Voltage Characteristics

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $V_{DD}$-$V_{SS}$[1] | DC power supply | -0.3 | 4.0 | V |
| $V_{DDIO}$-$V_{SS}$[1] | $V_{DDIO}$ Power Supply | -0.3 | 4.0 | V |
| $V_{BAT}$-$V_{SS}$[1] | $V_{BAT}$ Power Supply | -0.3 | 4.0 | V |
| $\Delta V_{DD}$ | Variations between different $V_{DD}$ power pins | - | 50 | mV |
| $\lvert V_{DD} - AV_{DD} \rvert$ | Allowed voltage difference for $V_{DD}$ and $AV_{DD}$ | - | 50 | mV |
| $\Delta V_{SS}$ | Variations between different ground pins | - | 50 | mV |
| $\lvert V_{SS} - AV_{SS} \rvert$ | Allowed voltage difference for $V_{SS}$ and $AV_{SS}$ | - | 50 | mV |
| $V_{IN}$[3] | Input voltage on 5V-tolerance GPIO pin when $V_{DD} \geq 1.9$ V | $V_{SS}$-0.3 | 5.5 | V |
| | Input voltage on 5V-tolerance GPIO pin when 1.9 V > $V_{DD} \geq 1.71$ V | $V_{SS}$-0.3 | $V_{DD}$+3.6 | V |
| | Input voltage on 5V-tolerance GPIO pin when $V_{DD} < 1.71$ V | $V_{SS}$-0.3 | 3.6 | V |
| | Input voltage on any other pin[2] | $V_{SS}$-0.3 | 4.0 | V |

**Notes:**

1. All main power ($V_{DD}$, $V_{BAT}$, $AV_{DD}$, $V_{REF}$) and ground ($V_{SS}$, $AV_{SS}$) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current
3. All analog input pins on PF.2 ~ PF.5, PA.8 ~ PA.15, PC.0 ~ PC.3, PC.13, PD.10 ~ PD.12 and PB0 ~ PB15 don't support 5-tolerance.

Table 8.1-1 Voltage characteristics

### 8.1.2 Current Characteristics

| Symbol | Description | Min | Max | Unit |
|---|---|---|---|---|
| $\Sigma I_{DD}$[1] | Maximum current into $V_{DD}$ | - | 200 | mA |
| $I_{DDIO}$ | Maximum Current into $V_{DDIO}$ | - | 100 | |
| $I_{BAT}$ | Maximum Current into $V_{BAT}$ | - | 100 | |
| $\Sigma I_{SS}$ | Maximum current out of $V_{SS}$ | - | 100 | |
| $I_{IO}$ | Maximum current sunk by a I/O Pin | - | 20 | |
| | Maximum current sourced by a I/O Pin | - | 20 | |
| | Maximum current sunk by total I/O Pins[2] | - | 100 | |
| | Maximum current sourced by total I/O Pins[2] | - | 100 | |
| $I_{INJ(PIN)}$ [3] | Maximum injected current by a I/O Pin | - | ±5 | |
| $\Sigma I_{INJ(PIN)}$ [3] | Maximum injected current by total I/O Pins | - | ±25 | |

**Note:**

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current characteristics

### 8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- $T_A$ = ambient temperature (℃)
- $\theta_{JA}$ = thermal resistance junction-ambient (℃/Watt)
- $\theta_{JC}$ = thermal resistance junction-case (℃/Watt)
- $P_D$ = sum of internal and I/O power dissipation

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | -40 | - | 105 | ℃ |
| $T_J$ | Operating junction temperature | -40 | - | 125 | |
| $T_{ST}$ | Storage temperature | -65 | - | 150 | |
| $\theta_{JA}$[1] | Thermal resistance junction-ambient 33-pin QFN(5x5 mm) | - | 39.6 | - | ℃/Watt |
| | Thermal resistance junction-ambient 48-pin QFN(5x5 mm) | - | 37.8 | - | ℃/Watt |
| | Thermal resistance junction-ambient 48-pin LQFP(7x7 mm) | - | 60 | - | ℃/Watt |
| | Thermal resistance junction-ambient 64-pin LQFP(7x7 mm) | - | 58 | - | ℃/Watt |
| | Thermal resistance junction-ambient 128-pin LQFP(14x14 mm) | - | 38.5 | - | ℃/Watt |

**Note:**

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal characteristics

### 8.1.4 EMC Characteristics

#### *8.1.4.1 Electrostatic discharge (ESD)*

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

#### *8.1.4.2 Static latchup*

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

#### *8.1.4.3 Electrical fast transients (EFT)*

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

#### *8.1.4.4 Conducted Immunity (CI)*

The conducted immunity testing relates to electromagnetic disturbances coming from intended radio-frequency (RF) transmitters in the frequency range 150 kHz up to 80 MHz. The CI test is one important characteristic of touch key MCU to address the effects of unwanted noise disturbances.

The conducted immunity requirements for electronic products are defined in IEC 61000-4-6 by International Electrotechnical Commission (IEC).

| Symbol | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $V_{HBM}$[1] | Electrostatic discharge,human body mode | -4000 | - | +4000 | V |
| $V_{CDM}$[2] | Electrostatic discharge,charge device model | -250 | - | +250 | |
| LU[3] | Pin current for latch-up[3] | -200 @ class II | - | +200 @ class II | mA |
| $V_{EFT}$[4] | Fast transient voltage burst | -4.4 | - | -4.4 | kV |
| $V_{CI}$[5] | Conducted immunity for touch key @150kHz ~ 80MHz | -10 | - | 10 | V |

**Notes:**

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.
5. Determinded according to IEC 61000-4-6 standard and the performance class is class A.

Table 8.1-4 EMC characteristics

### 8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

| Pacakge | MSL |
|---|---|
| 33-pin QFN(5x5 mm) [1] | MSL 3 |
| 48-pin QFN(5x5 mm) [1] | MSL 3 |
| 48-pin LQFP(7x7 mm) [1] | MSL 3 |
| 64-pin LQFP(7x7 mm) [1] | MSL 3 |
| 128-pin LQFP(14x14 mm) [1] | MSL 3 |
| **Note:**<br>1. Determined according to IPC/JEDEC J-STD-020 | |

Table 8.1-5 Package Moisture Sensitivity(MSL)

### 8.1.6 Soldering Profile

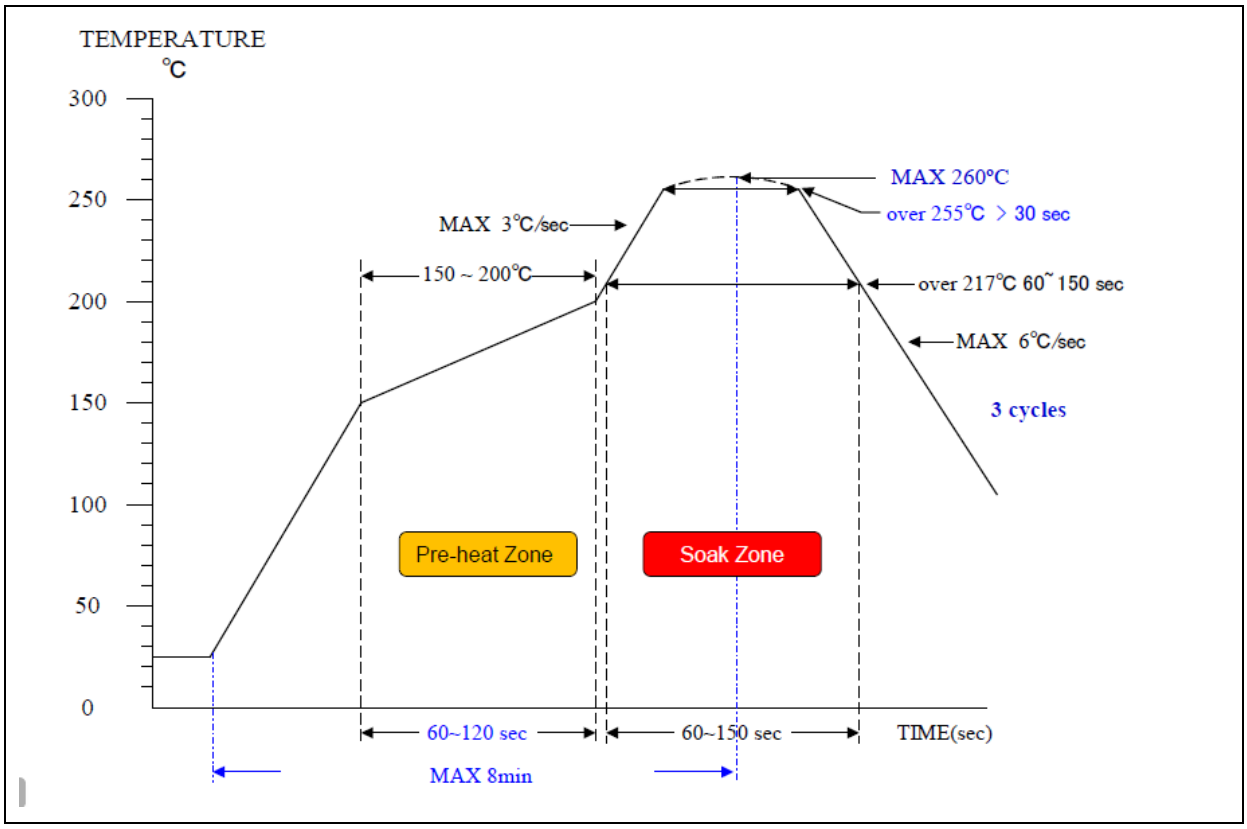



Figure 8.1-1 Soldering Profile from J-STD-020C

| Porfile Feature | Pb Free Package |
|---|---|
| Average ramp-up rate (217℃ to peak) | 3℃/sec. max |
| Preheat temperature 150℃ ~200℃ | 60 sec. to 120 sec. |
| Temperature maintained above 217℃ | 60 sec. to 150 sec. |
| Time with 5℃ of actual peak temperature | > 30 sec. |
| Peak temperature range | 260℃ |
| Ramp-down rate | 6℃/sec ax. |
| Time 25℃ to peak temperature | 8 min. max |
| **Note:**<br>1.Determined according to J-STD-020C | |

Table 8.1-6 Soldering Profile

## 8.2 General Operating Conditions

($V_{DD}$-$V_{SS}$ = 1.71 ~ 3.6 V, $T_A$ = 25°C, HCLK = 72 MHz unless otherwise specified.)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $f_{HCLK}$ | Internal AHB clock frequency | - | - | 72 | MHz | |
| $V_{DD}$ | Operation voltage | 1.71 | - | 3.6 | V | |
| $V_{DDIO}$ | $V_{DDIO}$ Operation voltage | 1.62 | - | 3.6 | | |
| $V_{BAT}$ | $V_{BAT}$ Operation voltage | 1.71 | - | 3.6 | | |
| $AV_{DD}$[1] [4] | Analog operation voltage | $V_{DD}$ | | | | |
| $V_{REF}$[4] | Analog reference voltage | 1.6 | - | $AV_{DD}$ | | |
| $V_{LDO}$ | LDO output voltage | - | 1.1 | - | | |
| $V_{BG}$ | Band-gap voltage | 1.164 | 1.2 | 1.236 | V | |
| $T_{VBG_ADC}$[3] | ADC sampling time when reading the band-gap voltage | 10 | - | - | µS | |
| $C_{LDO}$[2] | LDO output capacitor | 2.2 | | | µF | |
| $R_{ESR}$[3] | ESR of $C_{LDO}$ output capacitor | - | - | 0.5 | Ω | |
| $I_{RUSH}$[3] | InRush current on voltage regulator power-on (POR or wakeup from Standby) | - | 150 | 200 | mA | |
| $E_{RUSH}$[3] | InRush energy on voltage regulator power-on (POR or wakeup from Standby) | - | 3.76 | - | µC | $V_{DD}$ = 1.71 V, $T_A$ = 105 °C |

**Note:**

1. It is recommended to power $V_{DD}$ and $AV_{DD}$ from the same source. A maximum difference of 0.3 V between $V_{DD}$ and $AV_{DD}$ can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, $C_{LDO}$ must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General operating conditions

## 8.3 DC Electrical Characteristics

### 8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high except PC.0/PC.1/PC.2/PC.3 output low.
- The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 1.71 ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO} = V_{BAT}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in RRAM.

| Symbol | Conditions | $F_{HCLK}$ | Typ [1] | Max[1][2] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD_RUN}$ | Normal run mode with PL1 (PLSEL = 001), executed from RRAM, all peripherals disable<br>PLL, HIRC48, HXT, HIRC, MIRC, LXT or LIRC clock. | 72 MHz | 4.27 | 5 | 7.5 | 10 | mA |
| | | 60 MHz | 3.71 | 4.5 | 6 | 9.5 | |
| | | 50 MHz | 3.25 | 4 | 6.5 | 9 | |
| | | 48 MHz | 3.16 | 4 | 6.5 | 9 | |
| | | 12 MHz | 1.08 | 1.5 | 4 | 6.5 | |
| | | 6 MHz | 0.85 | 1.2 | 3.7 | 8.7 | |
| | | 4 MHz | 0.77 | 1.1 | 3.6 | 8.6 | |
| | | 2 MHz | 0.69 | 1 | 3.5 | 8.5 | |
| | | 1 MHz | 0.66 | 0.9 | 3.4 | 8.4 | |
| | | 32.768 kHz | 0.44 | 0.7 | 3.2 | 8.2 | |
| | | 32 kHz | 0.44 | 0.7 | 3.2 | 8.2 | |
| | Normal run mode with PL1 (PLSEL = 001), executed from RRAM, all peripherals enable<br>PLL, HIRC48, HXT, HIRC, MIRC, LXT or LIRC clock. | 72 MHz | 14.47 | 17 | 19.5 | 22 | |
| | | 60 MHz | 12.51 | 15 | 17.5 | 20 | |
| | | 50 MHz | 10.87 | 13 | 15.5 | 18 | |
| | | 48 MHz | 10.55 | 12.5 | 15 | 17.5 | |
| | | 12 MHz | 3.52 | 4.5 | 7 | 9.5 | |
| | | 6 MHz | 2.58 | 3.5 | 6 | 8.5 | |
| | | 4 MHz | 2.26 | 3 | 5.5 | 8 | |
| | | 2 MHz | 1.94 | 2.4 | 4.9 | 7.4 | |
| | | 1 MHz | 1.78 | 2.2 | 4.7 | 7.2 | |
| | | 32.768 kHz | 1.46 | 1.8 | 4.3 | 6.8 | |
| | | 32 kHz | 1.69 | 2.1 | 4.6 | 7.1 | |

**Notes:**

1. When analog peripheral blocks such as USB, DAC, OPA, PGA, ADC, ACMP, UTCPD, Touch Key, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current consumption in Normal Run mode

| Symbol | Conditions | $F_{HCLK}$ | Typ [1] | Max[1][2] | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| $I_{DD_IDLE}$ | Idle mode with PL1 (PLSEL = 001), all peripherals disable<br>PLL, HIRC48, HXT, HIRC, MIRC, LXT or LIRC clock. | 72 MHz | 2.38 | 3 | 5.5 | 8 | mA |
| | | 60 MHz | 2.14 | 2.7 | 5.2 | 7.7 | |
| | | 50 MHz | 1.93 | 2.4 | 4.9 | 7.4 | |
| | | 48 MHz | 1.89 | 2.4 | 4.9 | 7.4 | |
| | | 12 MHz | 0.75 | 1.1 | 3.6 | 8.6 | |
| | | 6 MHz | 0.69 | 1 | 3.5 | 8.5 | |
| | | 4 MHz | 0.66 | 0.9 | 3.4 | 8.4 | |
| | | 2 MHz | 0.64 | 0.9 | 3.4 | 8.4 | |
| | | 1 MHz | 0.63 | 0.9 | 3.4 | 8.4 | |
| | | 32.768 kHz | 0.44 | 0.7 | 3.2 | 8.2 | |
| | | 32 kHz | 0.44 | 0.7 | 3.2 | 8.2 | |
| | Idle mode with PL1 (PLSEL = 001), all peripherals enable<br>PLL, HIRC48, HXT, HIRC, MIRC, LXT or LIRC clock. | 72 MHz | 11.84 | 14.5 | 17 | 19.5 | |
| | | 60 MHz | 10.22 | 12.5 | 15 | 17.5 | |
| | | 50 MHz | 8.87 | 11 | 13.5 | 16 | |
| | | 48 MHz | 8.60 | 11 | 13.5 | 16 | |
| | | 12 MHz | 2.61 | 3.5 | 6 | 8.5 | |
| | | 6 MHz | 1.84 | 2.3 | 4.8 | 7.3 | |
| | | 4 MHz | 1.57 | 1.9 | 4.4 | 6.9 | |
| | | 2 MHz | 1.31 | 1.7 | 4.2 | 6.7 | |
| | | 1 MHz | 1.18 | 1.6 | 4.1 | 6.6 | |
| | | 32.768 kHz | 0.87 | 1.2 | 3.7 | 8.7 | |
| | | 32 kHz | 1.11 | 1.5 | 4 | 6.5 | |

**Notes:**

1. When analog peripheral blocks such as USB, DAC, OPA, PGA, ADC, ACMP, UTCPD, Touch Key, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle mode

| Symbol | Test Conditions | Power Level | LXT[1] 32.768 kHz | LIRC 32 kHz | Typ[2] | | | | Max[3][4] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | $T_A$= 25 °C | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | | | 1.8 V | 2.4 V | 3.0 V | 3.6 V | | | | |
| $I_{DD_DPD1}$ | DPD1, all peripherals disable | - | - | - | 0.05 | 0.10 | 0.26 | 1.29 | 3.0 | 16 | 20 | µA |
| | DPD1, all peripherals disable (DPDHOLDEN = 1) | - | - | - | 0.07 | 0.18 | 0.48 | 1.83 | 6.0 | 20 | 25 | |
| | DPD1, RTC enable and run | - | V | - | 0.32 | 0.40 | 0.59 | 1.63 | 4.0 | 17.5 | 22 | |
| $I_{DD_DPD0}$ | DPD0, all peripherals disable | - | - | - | 0.39 | 0.44 | 0.60 | 1.62 | 3.5 | 17 | 22 | uA |
| | DPD0, all peripherals disable (DPDHOLDEN = 1) | - | - | - | 0.41 | 0.52 | 0.82 | 2.17 | 6.5 | 21 | 27 | |
| | DPD0, RTC enable and run | - | V | - | 0.67 | 0.74 | 0.93 | 1.98 | 4.5 | 18.5 | 24 | |
| $I_{DD_SPD2}$ | SPD2, all peripherals disable without SRAM retention | PL4 | - | - | 2.02 | 2.14 | 2.46 | 3.81 | 5.2 | 15.5 | 30 | µA |
| | SPD2, all peripherals disable with 8KB SRAM retention | PL4 | - | - | 2.07 | 2.18 | 2.49 | 3.87 | 5.35 | 17.5 | 33.5 | |
| | SPD2, all peripherals disable with 24KB SRAM retention | PL4 | - | - | 2.15 | 2.27 | 2.58 | 3.95 | 5.65 | 21.5 | 40.5 | |
| | SPD2, all peripherals disable with 40KB SRAM retention | PL4 | - | - | 2.22 | 2.34 | 2.65 | 4.01 | 5.95 | 25.5 | 47.5 | |
| | SPD2, all peripherals disable with 168KB SRAM and 8KB LPSRAM retention | PL4 | - | - | 2.77 | 2.89 | 3.20 | 4.57 | 8.50 | 59.5 | 107 | |
| | SPD2, all peripherals disable without SRAM retention, RTC enable and run | PL4 | V | - | 2.31 | 2.45 | 2.79 | 4.19 | 6.2 | 17.00 | 32.00 | |
| $I_{DD_SPD1}$ | SPD1, all peripherals disable without SRAM retention | PL3 | - | - | 2.10 | 2.22 | 2.53 | 3.90 | 5.5 | 16.5 | 32 | uA |
| | SPD1, all peripherals disable with 8KB SRAM retention | PL3 | - | - | 2.21 | 2.32 | 2.64 | 4.00 | 5.75 | 20 | 36.5 | |
| | SPD1, all peripherals disable with 24KB SRAM retention | PL3 | - | - | 2.41 | 2.52 | 2.84 | 4.20 | 6.25 | 27 | 45.5 | |
| | SPD1, all peripherals disable with 40KB SRAM retention | PL3 | - | - | 2.60 | 2.71 | 3.02 | 4.39 | 6.75 | 34 | 54.5 | |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | SPD1, all peripherals disable with 168KB SRAM and 8KB LPSRAM retention | PL3 | - | - | 3.97 | 4.10 | 4.40 | 5.77 | 11 | 93.5 | 131 | |
| | SPD1, all peripherals disable without SRAM retention, RTC enable and run | PL3 | V | - | 2.37 | 2.52 | 2.85 | 4.25 | 6.5 | 18 | 34 | |
| $I_{DD_SPD0}$ | SPD0, all peripherals disable without SRAM retention | PL1 | - | - | 2.24 | 2.35 | 2.68 | 4.04 | 5.8 | 18.5 | 36 | uA |
| | SPD0, all peripherals disable with 8KB SRAM retention | PL1 | - | - | 2.51 | 2.63 | 2.93 | 4.31 | 6.3 | 22.5 | 44 | |
| | SPD0, all peripherals disable with 24KB SRAM retention | PL1 | - | - | 2.99 | 3.10 | 3.42 | 4.78 | 7.3 | 30.5 | 60 | |
| | SPD0, all peripherals disable with 40KB SRAM retention | PL1 | - | - | 3.46 | 3.58 | 3.90 | 5.26 | 8.3 | 38.5 | 76 | |
| | SPD0, all peripherals disable with 168KB SRAM and 8KB LPSRAM retention | PL1 | - | - | 6.90 | 7.02 | 7.35 | 8.69 | 16.8 | 106.5 | 212 | |
| | SPD0, all peripherals disable without SRAM retention, RTC enable and run | PL1 | V | - | 2.53 | 2.67 | 3.00 | 4.40 | 6.8 | 20 | 38 | |
| $I_{DD_NPD5}$ | NPD5, all peripherals disable without SRAM retention | PL4 | - | - | 8.33 | 8.45 | 8.79 | 10.19 | 33 | 180 | 360 | uA |
| | NPD5, all peripherals disable with 168KB SRAM retention | PL4 | - | - | 9.06 | 9.18 | 9.53 | 10.93 | 36.5 | 225 | 440 | |
| | NPD5, all peripherals disable with 168KB SRAM retention, RTC enable and run | PL4 | V | - | 9.35 | 9.51 | 9.88 | 11.31 | 37.5 | 226.5 | 442 | |
| $I_{DD_NPD4}$ | NPD4, all peripherals disable without SRAM retention | PL3 | - | - | 11.31 | 11.44 | 11.77 | 13.17 | 45 | 240 | 480 | uA |
| | NPD4, all peripherals disable with 168KB SRAM retention | PL3 | - | - | 13.13 | 13.28 | 13.62 | 15.03 | 65 | 330 | 660 | |
| | NPD4, all peripherals disable with 168KB SRAM retention, RTC enable and run | PL3 | V | - | 13.57 | 13.71 | 14.07 | 15.51 | 66 | 331.5 | 662 | |
| $I_{DD_NPD3}$ | NPD3, all peripherals disable without SRAM retention | PL1 | - | - | 17.32 | 17.44 | 17.78 | 19.17 | 60 | 330 | 660 | uA |
| | NPD3, all peripherals disable with 168KB SRAM retention | PL1 | - | - | 21.91 | 22.04 | 22.38 | 23.76 | 90 | 450 | 900 | |

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | NPD3, WDT/Timer use LIRC, UART/RTC use LXT with 168KB SRAM retention | PL1 | V | V | 22.60 | 22.77 | 23.17 | 24.64 | 92 | 453 | 904 | |
| $I_{DD_NPD2}$ | NPD2, all peripherals disable with 168KB SRAM retention | PL3 | - | - | 52.35 | 53.08 | 54.04 | 56.11 | 175 | 1400 | 2800 | uA |
| | NPD2, WDT/Timer use LIRC, UART/RTC use LXT with 168KB SRAM retention | PL3 | V | V | 53.48 | 54.27 | 55.31 | 57.41 | 177 | 1403 | 2804 | |
| $I_{DD_NPD1}$ | NPD1, all peripherals disable with 168KB SRAM retention | PL1 | - | - | 84.74 | 85.43 | 86.40 | 88.46 | 265 | 2000 | 4000 | uA |
| | NPD1, WDT/Timer use LIRC, UART/RTC use LXT with 168KB SRAM retention | PL1 | V | V | 86.05 | 86.80 | 87.82 | 89.98 | 267 | 2003 | 4004 | |
| $I_{DD_NPD0}$ | NPD0, all peripherals disable with 168KB SRAM retention | PL1 | - | - | 257.28 | 260.27 | 264.15 | 271.48 | 430 | 2500 | 5000 | uA |
| | NPD0, WDT/Timer use LIRC, UART/RTC use LXT with 168KB SRAM retention | PL1 | V | V | 258.68 | 261.72 | 265.55 | 273.15 | 432 | 2503 | 5004 | |

**Notes:**

1. Crystal used: AURUM XF66RU000032C0 for L3 gain level.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-3 Chip Current Consumption in Power-down mode

| Symbol | Test Conditions | LXT[*1] 32.768 kHz | Typ | | | | Max[*2] | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | $T_A$ = 25 °C | | | | $T_A$ = 25 °C | $T_A$ = 85 °C | $T_A$ = 105 °C | |
| | | | 1.80 V | 2.4 V | 3.0V | 3.6 V | | | | |
| $I_{BAT}$ | RTC off | - | 0.03 | 0.04 | 0.05 | 0.14 | 0.5 | 1 | 1.5 | µA |
| | RTC on | V | 0.31 | 0.34 | 0.38 | 0.50 | 1.5 | 2 | 2.5 | |

**Notes:**

1. Crystal used: AURUM XF66RU000032C0 for L3 gain level.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-4 $V_{BAT}$ Current Consumption in Power-down mode

| Symbol | Test Conditions | Typ[1] | | | Max[2] | | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | 25°C | 85°C | 105°C | 25°C | 85°C | 105°C | |
| $I_{DD_SRAM}$ | SRAM 8 KB static consumption | 0.26 | 1.27 | 2.56 | 0.5 | 4 | 8 | µA |
| | SRAM 24 KB static consumption | 0.75 | 3.57 | 7.23 | 1.5 | 12 | 24 | |
| | SRAM 40 KB static consumption | 1.22 | 5.58 | 11.29 | 2.5 | 20 | 40 | |
| | SRAM 72 KB static consumption | 2.04 | 9.01 | 18.25 | 4.5 | 36 | 72 | |
| | SRAM 104 KB static consumption | 2.85 | 12.48 | 25.34 | 6.5 | 52 | 104 | |
| | SRAM 168 KB static consumption | 4.45 | 19.56 | 39.69 | 10.5 | 84 | 168 | |

**Notes:**

1. Tested in power level 1 at SPD0.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-5 SRAM Static Current Consumption in Power-down mode

### 8.3.2 On-Chip Peripheral Current Consumption

- The typical values for $T_A$= 25 °C and $V_{DD}$ = $AV_{DD}$ = $V_{DDIO}$ = $V_{BAT}$ = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, $f_{HCLK}$ = 72 MHz, $f_{PCLK0, 1}$ = $f_{HCLK}$.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

| Peripheral | $I_{DD}$[1] | Unit |
|---|---|---|
| PDMA0 | 49 | uA |
| ISP | ~0 | |
| EBI | 13 | |
| ST | 66 | |
| CRC | 21 | |
| CRYPTO | 33 | |
| KeyStore | 12 | |
| RMC | 26 | |
| USB FS Host[4] | 531 | |
| SRAM0 | 8 | |
| SRAM1 | 7 | |
| GPA | 6 | |
| GPB | 7 | |
| GPC | 6 | |
| GPD | 6 | |
| GPE | 7 | |
| GPF | 6 | |
| GPG | 6 | |
| GPH | 7 | |
| RTC | 20 | |
| TMR0 | 119 | |
| TMR1 | 119 | |
| TMR2 | 122 | |
| TMR3 | 122 | |
| CLKO | 397 | |
| I2C0 | 17 | |

| | | |
|---|---|---|
| I2C1 | 20 | |
| I2C2 | 18 | |
| I2C3 | 20 | |
| QSPI0 | 397 | |
| SPI0 | 447 | |
| SPI1 | 444 | |
| SPI2 | 450 | |
| UART0 | 446 | |
| UART1 | 450 | |
| UART2 | 438 | |
| UART3 | 443 | |
| UART4 | 439 | |
| UART5 | 441 | |
| UART6 | 438 | |
| UART7 | 441 | |
| USB FS OTG[4] | 448 | |
| USB FS Device[4] | 509 | |
| EADC0[2] | 480 | |
| TRNG | 31 | |
| SPI3 | 445 | |
| USCI0 | 26 | |
| USCI1 | 28 | |
| WWDT | 82 | |
| DAC[5] | 19 | |
| EPWM0 | 50 | |
| EPWM1 | 52 | |
| EQEI0 | 17 | |
| EQEI1 | 20 | |
| Touch Key[7] | 61 | |
| ECAP0 | 20 | |
| ECAP1 | 22 | |
| ACMP2[3] | 63 | |
| PWM0 | 38 | |
| PWM1 | 43 | |

| | | |
|---|---|---|
| UTCPD0[8] | 268 | |
| CANRAM0 | 8 | |
| CANRAM1 | 9 | |
| CAN0 | 245 | |
| CAN1 | 246 | |
| HCLK1 | 5 | |
| LPDMA0 | 67 | |
| LPGPIO | 30 | |
| LPSRAM0 | 34 | |
| WDT | 44 | |
| LPSPI0 | 69 | |
| LPI2C0 | 47 | |
| LPUART0 | 76 | |
| LPTMR0 | 55 | |
| LPTMR1 | 54 | |
| LPTTMR0 | 57 | |
| LPTTMR1 | 56 | |
| LPADC0 | 78 | |
| OPA[6] | 54 | |

**Notes:**

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.
6. When the OPA is turned on, add an additional power consumption per OPA for the analog part.
7. When the Touch Key is turned on, add an additional power consumption per Touch Key for the analog part.
8. When the UTCPD is turned on, add an additional power consumption per UTCPD for the analog part.

Table 8.3-6 Peripheral Current Consumption

### 8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 12 MHz HIRC oscillator.

| Symbol | Parameter | Typ | Max | Unit |
|---|---|---|---|---|
| $t_{WU_IDLE}$[1] | Wakeup from IDLE mode | 10 | 11 | cycles |
| $t_{WU_DPD1}$[1][2] | Wakeup from deep Power-down mode 1 | 856 | 1189 | µS |
| $t_{WU_DPD0}$[1][2] | Wakeup from deep Power-down mode 0 | 252 | 312 | |
| $t_{WU_SPD2}$[1][2] | Wakeup from standby Power-down mode 2 | 288 | 301 | |
| $t_{WU_SPD1}$[1][2] | Wakeup from standby Power-down mode 1 | 194 | 207 | |
| $t_{WU_SPD0}$[1][2] | Wakeup from standby Power-down mode 0 | 110 | 123 | |
| $t_{WU_NPD5}$[1][2] | Wakeup from normal Power-down mode 5 running in RRAM | 232 | 245 | |
| | Wakeup from normal Power-down mode 5 running in RAM | 230 | 243 | |
| $t_{WU_NPD4}$[1][2] | Wakeup from normal Power-down mode 4 running in RRAM | 118 | 131 | |
| | Wakeup from normal Power-down mode 4 running in RAM | 116 | 129 | |
| $t_{WU_NPD3}$[1][2] | Wakeup from normal Power-down mode 3 running in RRAM | 55.20 | 68.2 | |
| | Wakeup from normal Power-down mode 3 running in RAM | 53.60 | 66.6 | |
| $t_{WU_NPD2}$[1][2] | Wakeup from normal Power-down mode 2 running in RRAM | 128.00 | 136 | |
| | Wakeup from normal Power-down mode 2 running in RAM | 126.00 | 134 | |
| $t_{WU_NPD1}$[1][2] | Wakeup from normal Power-down mode 1 running in RRAM | 36.80 | 37.8 | |
| | Wakeup from normal Power-down mode 1 running in RAM | 35.60 | 35.6 | |
| $t_{WU_NPD0}$[1][2] | Wakeup from normal Power-down mode 0 running in RRAM | 11.36 | 12.36 | |
| | Wakeup from normal Power-down mode 0 running in RAM | 10.00 | 11.00 | |

**Notes:**

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. The condition is HCLK=PCLK=HIRC

Table 8.3-7 Low-power mode wakeup timings

### 8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below $V_{SS}$ or above $V_{DD}$ should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to $V_{DD}$) to pins that include analog function which may potentially injection currents.

| Symbol | Parameter | Negative injection | Positive injection | Unit | Test Condition |
|---|---|---|---|---|---|
| $I_{INJ(PIN)}$ | Injected current by a I/O Pin | -0 | 0 | mA | Injected current on nReset pins |
| | | -0 | 0 | | Injected current on PF.2 ~ PF.5, PA.8 ~ PA.11, PC0~PC4, PC.13, PD.10 ~ PD.12 and PB0 ~ PB15 for all analog input function |
| | | -5 | - | | Injected current on any 5V tolerance I/O except analog input pin |

Table 8.3-8 I/O current injection characteristics

### 8.3.5 I/O DC Characteristics

#### *8.3.5.1 PIN Input Characteristics*

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input low voltage (Schmitt trigger) | 0 | - | $0.3*V_{DD}$ | V | |
| | Input low voltage (TTL trigger) | 0 | - | 0.7 | | $V_{DD}$ = 2.7 V |
| | | 0 | - | 0.5 | | $V_{DD}$ = 1.71 V |
| $V_{IH}$ | Input high voltage (Schmitt trigger) | $0.7*V_{DD}$ | - | $V_{DD}$ | V | |
| | Input high voltage (TTL trigger) | 1.48 | - | $V_{DD}$ | | $V_{DD}$ = 3.6 V |
| | | 0.9 | - | $V_{DD}$ | | $V_{DD}$ = 1.98V |
| $V_{HY}$[1] | Hysteresis voltage of schmitt input | - | $0.2*V_{DD}$ | - | V | |
| $I_{LK}$[2] | Input leakage current | -1 | - | 1 | µA | $V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode |
| | | -1 | - | 1 | | $V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode on any other 5v tolerance pins. $V_{DD}$ = 3.0 V |
| $R_{PU}$[1] | Pull up resistor | 40 | 51 | 61 | kΩ | $V_{DD}$ = 1.71 V ~ 3.6V |
| $R_{PD}$[1] | Pull down resistor | 40 | 51 | 61 | kΩ | $V_{DD}$ = 1.71 V ~ 3.6V |

**Notes:**
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-9 I/O input characteristics

### 8.3.5.2 I/O Output Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{SR}$[1] [2] [3][5] | Source current for quasi-bidirectional mode and high level | -6.7 | -8 | -9.9 | µA | $V_{DD}$ = 2.7 V<br>$V_{IN}$=($V_{DD}$-0.4) V |
| | | -6.7 | -8 | -9.9 | µA | $V_{DD}$ = 1.71 V<br>$V_{IN}$=($V_{DD}$-0.4) V |
| | Source current for push pull mode and high level | -12 | -15 | -21 | mA | $V_{DD}$ = 2.7 V<br>$V_{IN}$=($V_{DD}$-0.4) V |
| | | -6.5 | -9 | -11.5 | mA | $V_{DD}$ = 1.71 V<br>$V_{IN}$=($V_{DD}$-0.4) V |
| $I_{SK}$[1] [2] [4] | Sink current for push-pull mode and low level | 12 | 16.5 | 24.5 | mA | $V_{DD}$ = 2.7 V<br>$V_{IN}$= 0.4 V |
| | | 6 | 10 | 14 | mA | $V_{DD}$ = 1.71 V<br>$V_{IN}$= 0.4 V |
| $C_{IO}$[1] | I/O pin capacitance | - | 5 | - | pF | |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. The $I_{SR}$ and $I_{SK}$ must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed $\Sigma I_{DD}$ and $\Sigma I_{SS}$.
3. The range of output high level voltage ($V_{OH}$) is from $V_{DD}$-0.4 to $V_{DD}$ based on minimum value of source current ($I_{SR}$).
4. The range of output low level voltage ($V_{OL}$) is from 0 to 0.4 based on minimum value of sink current ($I_{SK}$).
5. The source current quasi-bidirectional mode specification does not include PC2,PC3.

Table 8.3-10 I/O output characteristics

### 8.3.5.3 nRESET Input Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{ILR}$ | Negative going threshold, nRESET | - | - | $0.3*V_{DD}$ | V | |
| $V_{IHR}$ | Positive going threshold, nRESET | $0.7*V_{DD}$ | - | - | V | |
| $R_{RST}$[1] | Internal nRESET pull up resistor | 40 | 51 | 61 | kΩ | |
| $t_{RP}$[1] | Minimum nRESET pulse width | 33 | - | - | µS | Normal run and Idle mode |
| | | 35 | - | - | | NPD0 mode |
| | | 39 | - | - | | NPD1 and NPD2 mode |
| | | 0.3 | - | - | | NPD3, NPD4, NPD5, SPD and DPD mode |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-11 nRESET Input Characteristics

## 8.4 AC Electrical Characteristics

### 8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC48M)

The 48 MHz RC oscillator is calibrated in production.

| Symbol. | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | 1.71 | - | 3.6 | V | |
| $f_{HIRC}$[1] | Oscillator frequnecy | 47.28 | 48 | 48.72 | MHz | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | Frequency drift over temperature and voltage | -1.5 | - | 1.5 | % | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | | -2.5 | - | +2.5 | % | $T_A$ = -20 ~ +85 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| | | -4 | - | +4 | % | $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| $I_{HIRC}$[1] | Operating current | - | 200 | - | µA | $V_{DD}$ = 3.3 V |
| $T_S$[2] | Stable time | - | 5 | 10 | µS | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) characteristics

### 8.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

The 12 MHz RC oscillator is calibrated in production.

| Symbol. | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | 1.71 | - | 3.6 | V | |
| $f_{HRC}$[1] | Oscillator frequnecy | 11.844 | 12 | 12.156 | MHz | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | Frequency drift over temperature and voltage | -1.3 | - | +1.3 | % | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | | -2 | - | +2 | % | $T_A$ = 0 ~ +85 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| | | -3 | - | +3 | % | $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| $I_{HRC}$[1] | Operating current | - | 135 | - | μA | $V_{DD}$ = 3.3 V |
| $T_S$[2] | Stable time | - | - | 20 | μS | $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

### 8.4.3 1~8 MHz Internal Median Speed RC Oscillator (MIRC)

The 1~8 MHz RC oscillator is calibrated in production.

| Symbol. | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | 1.71 | - | 3.6 | V | |
| $F_{MIRC}$[1] | Oscillator frequnecy | 0.975 | 1 | 1.025 | MHz | $T_A$ = 25 °C, $V_{DD}$ = 3.3 V |
| | | 1.95 | 2 | 2.05 | | |
| | | 3.9 | 4 | 4.1 | | |
| | | 7.8 | 8 | 8.2 | | |
| | Frequency drift over temperature and voltage | -2.5 | - | +2.5 | % | $T_A$ = 25 °C, $V_{DD}$ = 3.3 V |
| | | -3.5 | - | +3.5 | % | $T_A$ = -40 ~ +105 °C<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| $I_{MIRC}$[1] | Operating current | - | 10 | - | µA | 1 MHz, $V_{DD}$ = 3.3 V |
| | | - | 15 | - | | 2 MHz, $V_{DD}$ = 3.3 V |
| | | - | 20 | - | | 4 MHz, $V_{DD}$ = 3.3 V |
| | | - | 30 | - | | 8 MHz, $V_{DD}$ = 3.3 V |
| $T_S$[2] | Stable time | - | 10 | 19 | µS | 1 MHz, $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| | | - | 15 | 21 | | 2 MHz, $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$= 1.71 ~ 3.6 V |
| | | - | 20 | 26 | | 4 MHz, $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$= 1.71 ~ 3.6 V |
| | | - | 30 | 36 | | 8 MHz, $T_A$ = -40 ~ +105 °C,<br>$V_{DD}$ = 1.71 ~ 3.6 V |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design

Table 8.4-3 4 MHz Internal Median Speed RC Oscillator(MIRC) Characteristics

### 8.4.4 32 kHz Internal Low Speed RC Oscillator (LIRC)

| Symbol | Parameter | Min | Typ | Max] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | 1.71 | - | 3.6 | V | |
| $F_{LIRC}$[1] | Oscillator frequnecy | - | 32 | - | kHz | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | Frequency drift over temperature and voltage | - 1 | - | -1 | % | $T_A$ = 25 °C,<br>$V_{DD}$ = 3.3 V |
| | | -2 | - | +2 | % | $T_A$ = -40 ~ +105 °C<br>$V_{DD}$ = 1.71 ~ 3.6 V |
| $I_{LIRC}$[1] | Operating current | - | 0.2 | 0.3 | µA | $V_{DD}$ = 3.3 V |
| $T_S$ [2] | Stable time | - | - | 500 | µS | $T_A$ = -40 ~ +105 °C<br>$V_{DD}$ = 1.71 ~ 3.6 V |

**Notes:**

1. Guaranteed by characterization, not tested in production.
2. Guaranteed by design, not tested in production.

Table 8.4-4 32 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

### 8.4.5 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol | Parameter | Min[1] | Typ | Max[1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operating voltage | 1.71 | - | 3.6 | V | |
| $R_f$ | Internal feedback resister | - | 1 | - | MΩ | |
| $f_{HXT}$ | Oscillator frequency | 4 | - | 32 | MHz | |
| $I_{HXT}$ | Current consumption | - | 400 | - | μA | 4 MHz, Gain = L0, $C_L$ = 12.5 pF |
| | | - | 700 | - | | 12 MHz, Gain = L1, $C_L$ = 12.5 pF |
| | | - | 1000 | - | | 16 Mhz, Gain = L2, $C_L$ = 12.5 pF |
| | | - | 1500 | - | | 24 MHz, Gain = L3, $C_L$ = 12.5 pF |
| | | - | 2700 | - | | 32 MHz, Gain = L4, $C_L$ = 12.5 pF |
| $T_S$ | Stable time | - | 2600 | - | μS | 4 MHz, Gain = L0, $C_L$ = 12.5 pF |
| | | - | 2700 | - | | 12 MHz, Gain = L1, $C_L$ = 12.5 pF |
| | | - | 2500 | - | | 16 Mhz, Gain = L2, $C_L$ = 12.5 pF |
| | | - | 1700 | - | | 24 MHz, Gain = L3, $C_L$ = 12.5 pF |
| | | - | 1000 | - | | 32 MHz, Gain = L4, $C_L$ = 12.5 pF |
| $Du_{HXT}$ | Duty cycle | 40 | - | 60 | % | |
| Vpp | Peak-to-peak amplitude | 0.5 | 0.8 | 1.2 | V | |

**Notes:**

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~32 MHz High Speed Crystal (HXT) Oscillator

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rs | Equivalent series resisotr(ESR) | - | - | 150 | Ω | 4 MHz, Gain = L0, $C_L$ = 12.5 pF |
| | | - | - | 120 | | 12 MHz, Gain = L1, $C_L$ = 12.5 pF |
| | | - | - | 100 | | 16 Mhz, Gain = L2, $C_L$ = 12.5 pF |
| | | - | - | 80 | | 24 MHz, Gain = L3, $C_L$ = 12.5 pF |
| | | - | - | 50 | | 32 MHz, Gain = L4, $C_L$ = 12.5 pF |

**Notes:**

1. Guaranteed by characterization, not tested in production.
2. Safety factor ($S_f$) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

$R_{ADD}$: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor ($S_f$) of crystal in engineer stage, not for mass produciton.

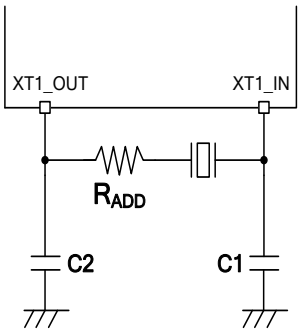



Table 8.4-6 External 4~32 MHz High Speed Crystal Characteristics

### *8.4.5.1 Typical Crystal Application Circuits*

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

| CRYSTAL | C1 | C2 | R1 |
|---|---|---|---|
| 4 MHz ~ 32 MHz | 10 ~ 20 pF | 10 ~ 20 pF | without |

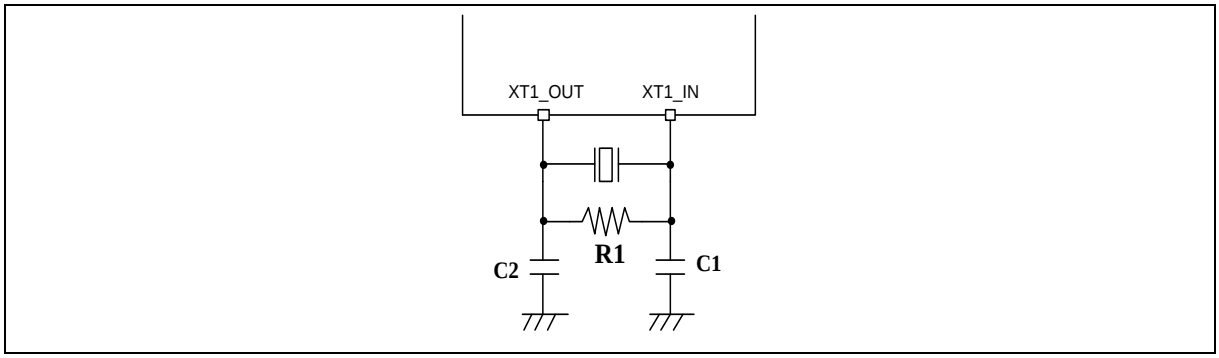
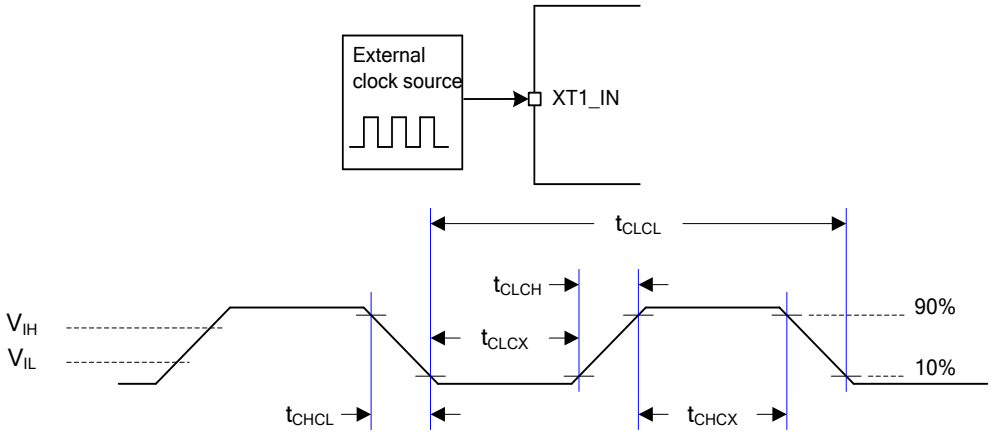



Figure 8.4-1 Typical Crystal Application Circuit

### 8.4.6 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $f_{HXT_ext}$ | External user clock source frequency | 1 | - | 32 | MHz | |
| $t_{CHCX}$ | Clock high time | 8 | - | - | nS | |
| $t_{CLCX}$ | Clock low time | 8 | - | - | nS | |
| $t_{CLCH}$ | Clock rise time | - | - | 10 | nS | Low (10%) to high level (90%) rise time |
| $t_{CHCL}$ | Clock fall time | - | - | 10 | nS | High (90%) to low level (10%) fall time |
| $Du_{E_HXT}$ | Duty cycle | 40 | - | 60 | % | |
| $V_{IH}$ | Input high voltage | $0.7*V_{DD}$ | - | $V_{DD}$ | V | The XT1_IN is set as schmitt trigger input mode. |
| $V_{IL}$ | Input low voltage | $V_{SS}$ | - | $0.3*V_{DD}$ | V | The XT1_IN is set as schmitt trigger input mode. |




Notes:

1.Guaranteed by characterization, not tested in production.

Table 8.4-7 External 4~32 MHz High Speed Clock Input Signal

### 8.4.7 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{BAT}$ | Operation voltage | 1.71 | - | 3.6 | V | |
| $T_{LXT}$ | Temperature range | -40 | - | 105 | °C | |
| $R_f$ | Internal feedback resistor | - | 8 | - | MΩ | |
| $F_{LXT}$ | Oscillator frequency | | 32.768 | | kHz | |
| $I_{LXT}$ | Current consumption | - | 240 | - | nA | ESR=35 kΩ, $C_L$ = 6 pF, Gain= L0 |
| | | - | 260 | - | | ESR=35 kΩ, $C_L$= 6 pF, Gain= L1 |
| | | - | 280 | - | | ESR=35 kΩ, $C_L$= 6 pF, Gain= L2 |
| | | - | 300 | - | | ESR=35 kΩ, $C_L$= 6 pF, Gain= L3 |
| | | - | 420 | - | | ESR=35 kΩ, $C_L$= 6 pF, Gain= L4 |
| | | - | 440 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L5 |
| | | - | 460 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L6 |
| | | - | 540 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L7 |
| | | - | 560 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L8 |
| | | - | 580 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L9 |
| | | - | 720 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L10 |
| | | - | 740 | - | | ESR=35 kΩ, $C_L$= 12.5 pF, Gain= L11 |
| | | - | 760 | - | | ESR=70 kΩ, $C_L$= 12.5 pF, Gain= L12 |
| | | - | 960 | - | | ESR=70 kΩ, $C_L$= 12.5 pF, Gain= L13 |
| | | - | 980 | - | | ESR=70 kΩ, $C_L$= 12.5 pF, Gain= L14 |
| | | - | 1000 | - | | ESR=70 kΩ, $C_L$= 12.5 pF, Gain= L15 |
| $Ts_{LXT}$ | Stable time | - | 1.5 | - | S | |
| $Du_{LXT}$ | Duty cycle | 30 | - | 70 | % | |
| $V_{pp}$ | Peak-to-peak amplitude | 0.2 | 0.5 | - | V | |

**Notes:**

1. Guaranteed by design, not tested in production.

Table 8.4-8 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| Rs | Equivalnet Series Resisotr(ESR) | - | 35 | 70 | kΩ | Crystal @32.768 kHz |

Table 8.4-9 External 32.768 kHz Low Speed Crystal Characteristics

### *8.4.7.1 Typical Crystal Application Circuits*

| CRYSTAL | C1 | C2 | R1 |
|---|---|---|---|
| 32.768 kHz, ESR < 70 KΩ | 7 ~ 20 pF | 7 ~ 20 pF | without |

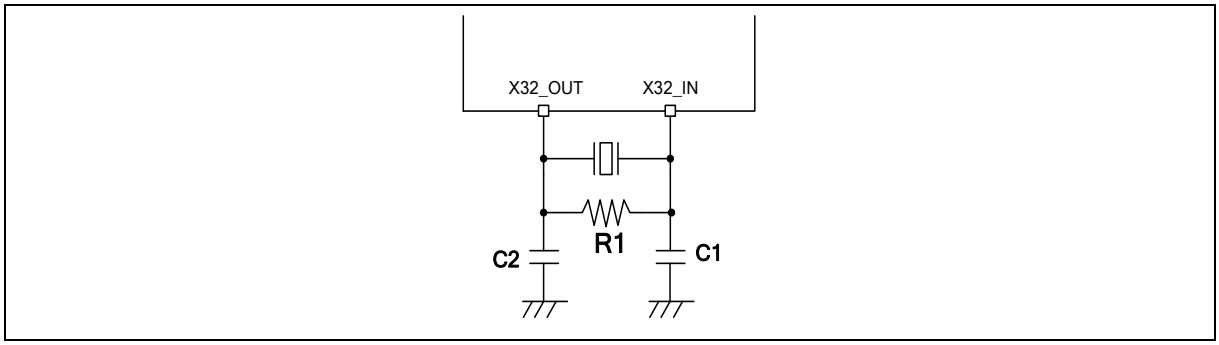
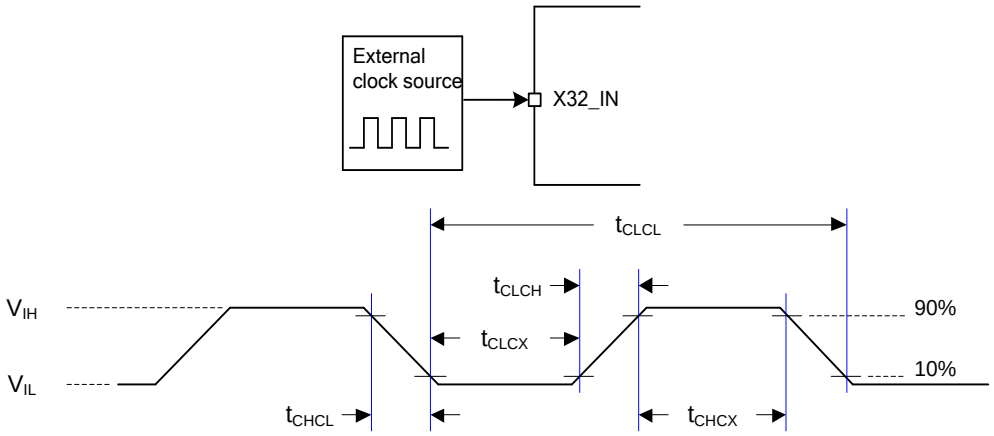



Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

### 8.4.8 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $f_{LXT_ext}$ | External clock source frequency | - | 32.768 | - | kHz | |
| $t_{CHCX}$ | Clock high time | 450 | - | - | nS | |
| $t_{CLCX}$ | Clock low time | 450 | - | - | nS | |
| $t_{CLCH}$ | Clock rise time | - | - | 50 | nS | Low (10%) to high level (90%) rise time |
| $t_{CHCL}$ | Clock fall time | - | - | 50 | nS | High (90%) to low level (10%) fall time |
| $Du_{E_LXT}$ | Duty cycle | 30 | - | 70 | % | |
| $V_{IH}$ | LXT input pin input high voltage | $0.7*V_{DD}$ | - | $V_{DD}$ | V | The X32_IN is set as schmitt trigger input mode. |
| $V_{IL}$ | LXT input pin input low voltage | $V_{SS}$ | - | $0.3*V_{DD}$ | V | The X32_IN is set as schmitt trigger input mode. |




**Notes:**

1.Guaranteed by design, not tested in production

Table 8.4-10 External 32.768 kHz Low Speed Clock Input Signal

### 8.4.9 PLL Characteristics

| Symbol | Parameter | Min[1] | Typ | Max[1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $f_{PLL_in}$ | PLL input clock | 1 | - | 24 | MHz | |
| $f_{PLL_OUT}$ | PLL multiplier output clock | 25 | - | 144 | MHz | |
| $f_{PLL_REF}$ | PLL reference clock | 1 | - | 8 | MHz | |
| $f_{PLL_VCO}$ | PLL voltage controlled oscillator | 144 | - | 500 | MHz | |
| $T_L$ | PLL locking time | - | - | 200 | µS | |
| Jitter[2] | Cycle-to-cycle Jitter | - | 250 | - | pS | |
| $I_{DD}$ | Power consumption | - | 3 | 4 | mA | $f_{PLL_VCO}$ = 500 MHz |

**Notes:**

1.Guaranteed by characterization, not tested in production

2.Guaranteed by design, not tested in production

Table 8.4-11 PLL Characteristics

### 8.4.10 I/O AC Characteristics

| Symbol | Parameter | Typ. | Max[1]. | Unit | Test Conditions[2] |
|---|---|---|---|---|---|
| $t_{f(IO)out}$ | Output high (90%) to low level (10%) fall time (Normal Slew Rate) | - | 9.78 | nS | CL = 30 pF, VDD >= 2.7 V |
| | | - | 6.68 | | CL = 10 pF, VDD >= 2.7 V |
| | | - | 15.03 | | CL = 30 pF, VDD >= 1.62 V |
| | | - | 10.41 | | CL = 10 pF, VDD >= 1.62 V |
| | Output high (90%) to low level (10%) fall time (High Slew Rate) | - | 5.81 | | $C_L$ = 30 pF, $V_{DD}$ >= 2.7 V |
| | | - | 3.69 | | $C_L$ = 10 pF, $V_{DD}$ >= 2.7 V |
| | | - | 9.44 | | $C_L$ = 30 pF, $V_{DD}$ >= 1.62 V |
| | | - | 5.74 | | $C_L$ = 10 pF, $V_{DD}$ >= 1.62 V |
| $t_{r(IO)out}$ | Output low (10%) to high level (90%) rise time (Normal Slew Rate) | - | 9.45 | nS | $C_L$ = 30 pF, $V_{DD}$ >= 2.7 V |
| | | - | 6.58 | | $C_L$ = 10 pF, $V_{DD}$ >= 2.7 V |
| | | - | 13.76 | | $C_L$ = 30 pF, $V_{DD}$ >= 1.62 V |
| | | - | 9.65 | | $C_L$ = 10 pF, $V_{DD}$ >= 1.62 V |
| | Output low (10%) to high level (90%) rise time (High Slew Rate) | - | 5.79 | nS | $C_L$ = 30 pF, $V_{DD}$ >= 2.7 V |
| | | - | 3.74 | | $C_L$ = 10 pF, $V_{DD}$ >= 2.7 V |
| | | - | 8.94 | | $C_L$ = 30 pF, $V_{DD}$ >= 1.62 V |
| | | - | 5.56 | | $C_L$ = 10 pF, $V_{DD}$ >= 1.62 V |
| $f_{max(IO)out}$[3] | I/O maximum frequency (Normal Slew Rate) | - | 34 | MHz | $C_L$ = 30 pF, $V_{DD}$ >= 2.7 V |
| | | - | 50 | | $C_L$ = 10 pF, $V_{DD}$ >= 2.7 V |
| | | - | 23 | | $C_L$ = 30 pF, $V_{DD}$ >= 1.62 V |
| | | - | 33 | | $C_L$ = 10 pF, $V_{DD}$ >= 1.62 V |
| | I/O maximum frequency (High Slew Rate) | - | 57 | MHz | $C_L$ = 30 pF, $V_{DD}$ >= 2.7 V |
| | | - | 89 | | $C_L$ = 10 pF, $V_{DD}$ >= 2.7 V |
| | | - | 36 | | $C_L$ = 30 pF, $V_{DD}$ >= 1.6 V |
| | | - | 59 | | $C_L$ = 10 pF, $V_{DD}$ >= 1.6 V |
| $I_{DIO}$[4] | I/O dynamic current consumption | - | 2.77 | mA | $C_L$ = 30 pF, $V_{DD}$ = 3.3 V, |
| | | - | 1.18 | | $C_L$ = 10 pF, $V_{DD}$ = 3.3 V, |
| | | - | 0.69 | | $C_L$ = 30 pF, $V_{DD}$ = 3.3 V, |
| | | - | 0.29 | | $C_L$ = 10 pF, $V_{DD}$ = 3.3 V, |

**Notes:**

1. Guaranteed by design result, not tested in production.
2. $C_L$ is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-12 I/O AC Characteristics

## 8.5 Analog Characteristics

### 8.5.1 LDO Characteristics

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $V_{DD}$ | Power supply | 1.71 | - | 3.6 | V | |
| $V_{LDO}$ | Output voltage | - | 1.1 | - | V | MCU @PL1 |

**Notes:**

1.It is recommended a 0.1μF bypass capacitor is connected between $V_{DD}$ and the closest $V_{SS}$ pin of the device.

2.For ensuring power stability, a $C_{LDO}$ capacitor must be connected between LDO_CAP pin and the closest $V_{SS}$ pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

3.$V_{LDO}$ is only used to supply internal power.

Table 8.5-1 LDO characteristics

### 8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $I_{POR}$[1] | POR operating current | - | 10 | 20 | μA | $V_{DD}$ = $AV_{DD}$ = 3.6V |
| $I_{LVR}$[1] | LVR operating current | - | 0.3 | 0.6 | | $V_{DD}$ = $AV_{DD}$ = 3.6V |
| $I_{BOD}$[1] | BOD operating current | - | 10 | 15 | | $V_{DD}$ = $AV_{DD}$ = 3.6V, Normal mode |
| | | - | 1 | 1.5 | | $V_{DD}$ = $AV_{DD}$ = 3.6V, Low Power mode |
| $V_{POR}$ | POR reset voltage (Rising edge) | 1.45 | 1.5 | 1.55 | V | |
| | POR reset voltage (Falling edge) | 1.4 | 1.45 | 1.5 | | |
| $V_{LVR}$ | LVR reset voltage (Rising edge) | 1.46 | 1.5 | 1.6 | | |
| | LVR reset voltage (Falling cedge) | 1.45 | 1.5 | 1.55 | | |
| $V_{BOD}$ | BOD brown-out detect voltage (Rising edge) | 1.56 | 1.68 | 1.80 | | BODVL = 0x8 |
| | | 1.76 | 1.88 | 2.00 | | BODVL = 0x9 |
| | | 1.96 | 2.08 | 2.20 | | BODVL = 0xA |
| | | 2.16 | 2.28 | 2.40 | | BODVL = 0xB |
| | | 2.36 | 2.48 | 2.60 | | BODVL = 0xC |
| | | 2.56 | 2.68 | 2.80 | | BODVL = 0xD |
| | | 2.76 | 2.88 | 3.00 | | BODVL = 0xE |
| | | 2.96 | 3.08 | 3.20 | | BODVL = 0xF |
| | BOD brown-out detect voltage (Falling edge) | 1.50 | 1.60 | 1.70 | | BODVL = 0x8 |
| | | 1.70 | 1.80 | 1.90 | | BODVL = 0x9 |
| | | 1.90 | 2.00 | 2.10 | | BODVL = 0xA |
| | | 2.10 | 2.20 | 2.30 | | BODVL = 0xB |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 2.30 | 2.40 | 2.50 | | BODVL = 0xC |
| | | 2.50 | 2.60 | 2.70 | | BODVL = 0xD |
| | | 2.70 | 2.80 | 2.90 | | BODVL = 0xE |
| | | 2.90 | 3.00 | 3.10 | | BODVL = 0xF |
| $T_{LVR_SU}$[2] | LVR startup time | - | - | 2000 | µS | |
| $T_{LVR_RE}$[1] | LVR respond time | - | 20 | 100 | | |
| $T_{BOD_SU}$[2] | BOD startup time | - | - | 2000 | | Normal mode |
| | | - | - | 20000 | | Low Power mode |
| $T_{BOD_RE}$[1] | BOD respond time | - | - | 130 | | Normal mode, DGSEL=0 |
| | | - | - | 5 | | Normal mode, DGSEL=3, HCLK = HIRC |
| | | - | 13000 | 20000 | | Low Power mode |
| $R_{VDDR}$[1] | VDD rise time rate | 10 | - | - | µS/V | POR Enabled |
| $R_{VDDF}$[1] | VDD fall time rate | 10 | - | - | | POR Enabled |
| | | 1000 | - | - | | LVR Enabled |
| | | 1300 | - | - | | BOD Enabled, Normal mode, DGSEL=0 |
| | | 50 | - | - | | BOD Enabled, Normal mode, DGSEL=3, HCLK = HIRC |

**Notes:**

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-2 Reset and Power Control Unit

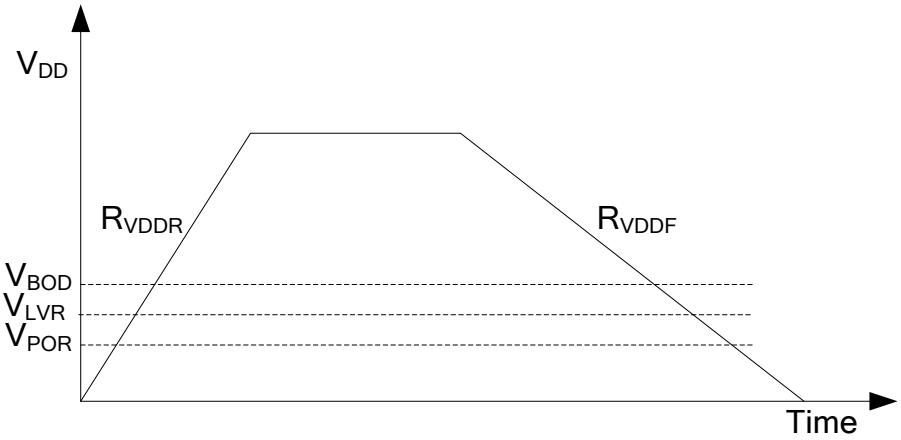



Figure 8.5-1 Power Ramp Up/Down Condition

### 8.5.3 12-bit SAR Analog To Digital Converter (ADC)

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $AV_{DD}$ | Analog operating voltage | 1.71 | - | 3.6 | V | $V_{DD} = AV_{DD}$ |
| $V_{REF}$ | Reference voltage | 1.6 | - | $AV_{DD}$ | V | |
| $V_{IN}$ | ADC channel input voltage | 0 | - | $V_{REF}$ | V | |
| $I_{ADC}$[1] | ADC Operating current ($AV_{DD}$ + $V_{REF}$ current) | - | 330 | - | μA | $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V<br>$F_{ADC}$ = 72 MHz<br>$T_{CONV} = 21 * T_{ADC}$ |
| $N_R$ | Resolution | 12 | | | Bit | |
| $F_{ADC}$[1]<br>$1/T_{ADC}$ | ADC Clock frequency | 12 | - | 72 | MHz | 1.7V ≦ $V_{REF}$ ≦ 3.6V |
| $T_{SMP}$ | Sampling Time | 1 | - | 256 | $1/F_{ADC}$ | $T_{SMP}$ = ( EXTSMPT(EADC_SCTLx[31:24]) + 1 ) * $T_{ADC}$ |
| $T_{CONV}$ | Conversion time | 21 | - | 276 | $1/F_{ADC}$ | $T_{CONV} = T_{SMP} + 20 * T_{ADC}$ |
| $F_{SPS}$[1] | Sampling Rate | 0.57 | - | 3.4 | MSPS | 1.7V ≦ $V_{REF}$ ≦ 3.6V<br>$F_{SPS} = F_{ADC} / T_{CONV}$<br>EXTSMPT(EADC_SCTLx[31:24]) = 0 |
| $T_{EN}$ | Enable to ready time | 5 | - | - | $1/F_{ADC}$ | |
| INL[1] | Integral Non-Linearity Error | -4 | - | +3 | LSB | $V_{REF} = AV_{DD}$ |
| DNL[1] | Differential Non-Linearity Error | -1 | - | +2 | LSB | $V_{REF} = AV_{DD}$ |
| $E_G$[1] | Gain error | -4 | - | +4 | LSB | $V_{REF} = AV_{DD}$ |
| $E_O$[1]$_T$ | Offset error | -4 | - | +4 | LSB | $V_{REF} = AV_{DD}$ |
| $E_A$[1] | Absolute Error | -4 | - | +4 | LSB | $V_{REF} = AV_{DD}$ |
| ENOB[1] | Effective number of bits | - | 10.0 | - | bits | $F_{ADC}$ = 72 MHz<br>$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V<br>Input Frequency = 20 kHz<br>$T_A$ = 25 °C |
| SINAD[1] | Signal-to-noise and distortion ratio | - | 60.2 | - | dB | |
| SNR[1] | Signal-to-noise ratio | - | 60.2 | - | | |
| THD[1] | Total harmonic distortion | - | -74 | - | | |
| $C_{IN}$[1] | Internal Capacitance | - | 3.1 | - | pF | |
| $R_{IN}$[1] | Internal Switch Resistance | - | - | 540 | Ω | |

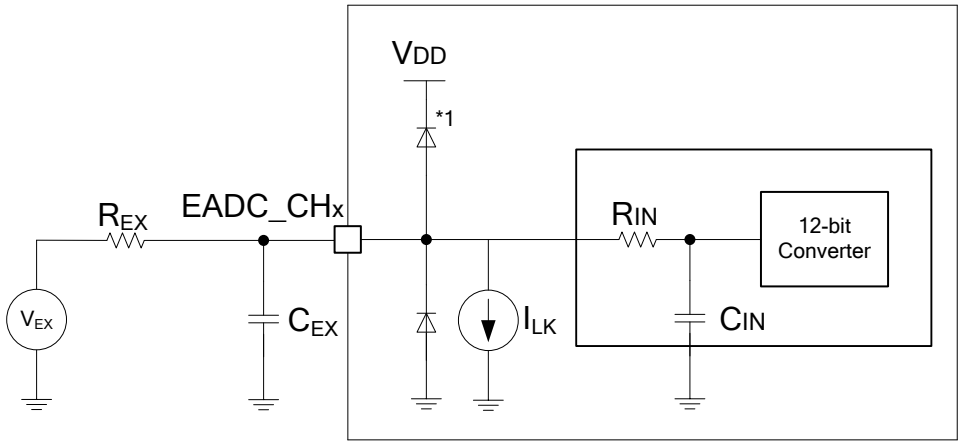
| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $R_{EX}$[1] | External input impedance | - | - | 23 | kΩ | $F_{ADC}$ = 72 MHz<br>$T_{SMP}$ = 256/$F_{ADC}$<br>$T_A$ = 25 °C |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. $R_{EX}$ max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks ($T_{SMP}$). $C_{EX}$ represents the capacitance of PCB and pad and is combined with $R_{EX}$ into a low-pass filter. Once the $R_{EX}$ and $C_{EX}$ values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

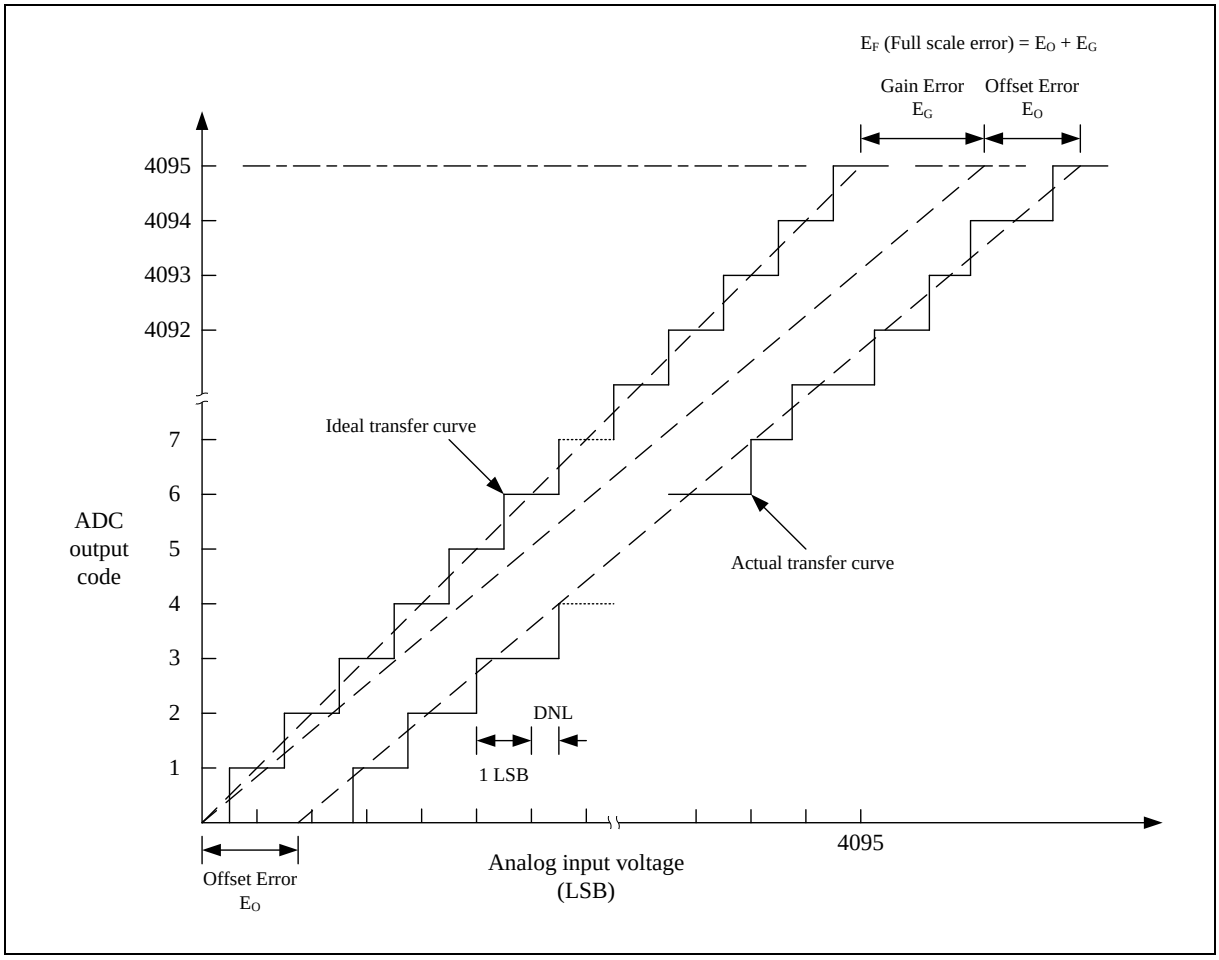
Table 8.5-3 ADC Characteristics




**Notes:**

1. The internal ESD diode doesn't be supported between IO and $V_{DD}$ at 5V tolerence IO pin.

**Note:** Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.




**Note:** The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

### 8.5.4 Digital to Analog Converter (DAC)

The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 1.8 | - | 3.6 | V | - |
| $N_R$ | Resolution | | 12 | | bit | - |
| $V_{REF}$ | Reference supply voltage | 1.5 | - | 3.6 | V | $V_{REF} \leq AV_{DD}$ |
| DNL[2] | Differential non-linearity error | -2 | - | 2 | LSB | 12-bit mode |
| INL[2] | Integral non-linearity error | -4 | - | 4 | LSB | 12-bit mode |
| OE[2] | Offset Error | -8 | - | 8 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | -4 | - | 4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| GE[2] | Gain Error | -10 | - | 10 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | -4 | - | 4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| AE[2] | Absolute Error | -10 | - | 10 | LSB | 12-bit mode<br>DACOUT buffer ON |
| | | -4 | - | 4 | LSB | 12-bit mode<br>DACOUT buffer OFF |
| $V_O$[1] | Output Voltage | 0.2 | - | AVDD-0.2 | V | DACOUT buffer ON |
| | | 1 LSB | - | VREF – 1 LSB | | DACOUT buffer OFF |
| $R_{LOAD}$[2] [3] | Resistive load | 7.5 | - | - | kΩ | DACOUT buffer ON |
| $R_O$[2] | Output impedance | - | 9.8 | - | kΩ | DACOUT buffer OFF |
| $C_{LOAD}$[2] [4] | Capacitive load | - | - | 20 | pF | DACOUT buffer OFF |
| $I_{DAC_AVDD}$[2] | DAC operating current on AVDD supply | - | 132 | - | μA | $AV_{DD}$ = 3.6V, no load, lowest code (0x000) |
| | | - | 410 | - | | $AV_{DD}$ = 3.6V, no load, middle code (0x800) |
| $I_{DAC_VREF}$[2] | DAC operating current on VREF supply | - | 170 | 240 | μA | $V_{REF}$ =3.6V, no load, middle code (0x800) |

| | | | | | | |
|---|---|---|---|---|---|---|
| $T_B$[2] | Settling Time | - | - | 2 | µs | Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB,<br>$C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$ |
| $F_S$ | Update Rate | - | - | 1 | $M_{SPS}$ | Max. frequency for a correct DAC_OUT change from core i to i+1LSB, $C_{LOAD} \leq 50pF$, $R_{LOAD} \geq 5k\Omega$ |
| $T_{WAKEUP}$ | Wake-up Time | - | 5 | 10 | µs | Wakeup time from OFF state. Input code between lowest and highest possible codes.<br>DAC clock source = 1MHz |
| PSRR[1] | Power Supply Rejection Ratio | - | -60 | -40 | dB | No $R_{LOAD}$, $C_{LOAD}$ = 50pF |

**Note:**

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and $AV_{SS}$.
4. Capacitive load at DACOUT pin.

Table 8.5-4 DAC Characteristics

### 8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 1.71 | - | 3.6 | V | $V_{DD} = AV_{DD}$ |
| $T_A$ | Temperature | -40 | - | 125 | ℃ | |
| $I_{ACMP}$[2] | ACMP operating current | - | 70 | - | μA | MODESEL = 11 |
| | | - | 35 | - | | MODESEL = 10 |
| | | - | 2 | - | | MODESEL = 01 |
| | | - | 1 | - | | MODESEL = 00 |
| $V_{CM}$[2] | Input common mode voltage range | 0 | - | $AV_{DD}$ | | |
| $V_{DI}$[2] | Differential input voltage sensitivity | 20 | - | - | mV | Hysteresis disable (HYSSEL = 00) |
| $V_{offset}$[2] | Input offset voltage | - | ±5 | ±10 | mV | MODESEL =11<br>Hysteresis disable (HYSSEL = 00) |
| | | - | ±10 | ±20 | mV | MODESEL =00~10<br>Hysteresis disable (HYSSEL = 00) |
| $V_{hys}$[2] | Hysteresis window | - | 0 | - | mV | HYSSEL = 000 |
| | | 10 | 20 | 40 | | HYSSEL = 010,<br>MODESEL =00~01 |
| | | | | | | HYSSEL = 011,<br>MODESEL =10~11 |
| | | 20 | 40 | 60 | | HYSSEL = 100<br>MODESEL =00~01 |
| | | | | | | HYSSEL = 101<br>MODESEL =10~11 |
| $A_v$[1] | DC voltage Gain | 51 | 70 | - | dB | |
| $T_d$[2] | Propagation delay | - | 30 | 60 | nS | MODESEL = 11 |
| | | - | 100 | 150 | | MODESEL = 10 |
| | | - | 0.8 | 2 | μS | MODESEL = 01 |
| | | - | 1.5 | 3.5 | | MODESEL = 00 |
| $T_{Setup}$[2] | Setup time | - | - | 1 | μS | MODESEL = 10~11 |
| | | - | - | 20 | | MODESEL = 00~01 |
| $A_{CRV}$[2] | CRV output voltage | -1 | - | 1 | LSB | AVDD x (CRV_SEL[5:0]/63) |
| $T_{SETUP_CRV}$[2] | Setup time | - | - | 0.6 | μS | CRV output voltage settle to ±5% |
| $I_{DD_CRV}$[2] | Operating current | - | 30 | 50 | μA | |

**Notes:**

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

### 8.5.6 Operation Amplifier (OPA)

The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$ = 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $AV_{DD}$ | Analog supply voltage | 1.8 | - | 3.6 | V | |
| $T_A$ | Temperature | -40 | - | 105 | ℃ | |
| $I_{OPA}$ | OPA operating current | - | 690 | 1450 | μA | PGA disabled, Normal mode |
| | | - | 230 | 500 | μA | PGA disabled, Low power mode |
| | | - | 950 | 1750 | μA | PGA enabled, Normal mode |
| | | - | 330 | 600 | μA | PGA enabled, low power mode |
| $V_{CM}$[2] | Common mode input range | 0.1 | - | $AV_{DD}$-0.1 | V | |
| $V_{OS}$[2] | Output Saturation Voltage | 0.1 | - | $AV_{DD}$-0.1 | V | $R_{LOAD}$ = 6 KΩ |
| $V_{OFFSET0}$[2] | Input offset voltage | - | ±1 | ±1.5 | mV | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2 |
| | | - | ±1 | ±3 | mV | $V_{CM}$=0.1 ~ $AV_{DD}$ – 0.1 |
| $\Delta V_{OFFSET0}$ | Input offset voltage drift | - | ±10 | - | μV/℃ | |
| CMRR[1] | Common Mode Rejection Ratio | - | 90 | - | dB | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2 |
| PSRR[1] | Power Supply Rejection Ratio | - | 100 | - | dB | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2 |
| GBW[2] | Bandwidth | - | 8.2 | - | MHz | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2, Normal mode |
| | | - | 1.5 | - | MHz | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2, Low power mode |
| SR[2] | Slew rate | - | 4.7 | - | V/μS | $R_{LOAD}$ = 6 KΩ, $C_{LOAD}$ = 50pF |
| | | - | 1 | - | V/μS | $R_{LOAD}$ = 6 KΩ, $C_{LOAD}$ = 50pF |
| AO[1] | Open loop gain | - | 91 | - | dB | |
| PM[1] | Phase Margin | - | 60 | - | degree | $AV_{DD}$=3.3V, $V_{CM}$=$AV_{DD}$/2 |
| GM[1] | Gain Margin | - | -6 | - | dB | |
| $T_{WAKEUP}$[2] | Wake up time from disable state | - | 2.8 | 7 | μS | Normal mode |
| | | - | 8 | 21 | μS | Low power mode |
| $R_{LOAD}$[2] | Resistive load | 6 | - | - | kΩ | |
| $C_{LOAD}$[2] | Capacitive load | - | - | 50 | pF | |
| eN | Input voltage noise density | - | TBD | - | $nV/\sqrt{Hz}$ | At 1kHz, $R_{LOAD}$ = 6 KΩ |
| | | - | TBD | - | $nV/\sqrt{Hz}$ | At 10kHz, $R_{LOAD}$ = 6 KΩ |
| $R_{PGA}$ | Rf/Ri internal resistance values in PGA mode | - | 12.6/12.6 | - | kΩ/kΩ | PGA Gain = 2 or -1 |
| | | - | 37.8/12.6 | - | kΩ/kΩ | PGA Gain = 4 or -3 |
| | | - | 88.2/12.6 | - | kΩ/kΩ | PGA Gain = 8 or -7 |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | - | 189/12.6 | - | kΩ/kΩ | PGA Gain = 16 or -15 |
| | | - | 390.6/12.6 | - | kΩ/kΩ | PGA Gain = 32 or -31 |
| $E_{GAIN_PGA}$[2] | Non inverting gain error | -1 | - | +1 | % | $AV_{DD}$ = 2.7 V ~ 3.6 V |
| | | -2 | - | +2 | % | $AV_{DD}$ = 1.8 V ~ 2.7 V |
| | inverting gain error | -2 | - | +2 | % | $AV_{DD}$ = 2.7 V ~ 3.6 V |
| | | -3 | - | +3 | % | $AV_{DD}$ = 1.8 V ~ 2.7 V |
| $GBW_{PGA}$ | PGA Bandwidth | GBW / $G_{PGA}$ | | | MHz | |

**Note:**

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.

Table 8.5-5 OPA Characteristics

### 8.5.7 Internal Voltage Reference

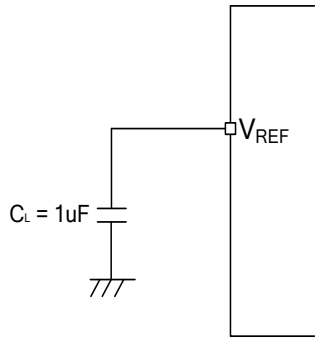
The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{REF_INT}$ | Internal reference voltage | 1.576 | 1.6 | 1.624 | V | $AV_{DD}$ >= 2.0 V |
| | | 2.017 | 2.048 | 2.079 | | $AV_{DD}$ >= 2.2 V |
| | | 2.463 | 2.5 | 2.538 | | $AV_{DD}$ >= 2.7 V |
| | | 3.026 | 3.072 | 3.118 | | $AV_{DD}$ >= 3.2 V |
| $T_S$[1] | Stable time | - | - | 2 | mS | $C_L$ =4.7 uF, $V_{REF}$ initial=0, Preload is enabled. |
| | | - | - | 480 | uS | $C_L$ =1 uF, $V_{REF}$ initial=0, Preload is enabled. |
| $I_{VREF_INT}$[1] | $V_{REF_INT}$ operating current | - | 70 | - | uA | |

**Note:**

1. Guaranteed by characterization, not tested in production

Table 8.5-6 Internal $V_{REF}$ Characteristics




**Note:** $V_{REF_INT}$ is only supported while package includes $V_{REF}$ pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

### 8.5.8 Temperature Sensor

The maximum values are obtained for $V_{DD}$ = 3.6 V and maximum ambient temperature ($T_A$), and the typical values for $T_A$= 25 °C and $V_{DD}$ = 3.3 V unless otherwise specified.

| Symbol | Parameter | Min | Typ | Max | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{TEMP_OS}$[1] | Temperature sensor offset voltage | 935 | 1010 | 1105 | mV | $T_A$ = 25°C |
| $T_C$[1] | Temperature Coefficient | -2.5 | -2.7 | -3.02 | mV/°C | |
| $T_S$[2] | Stable time | - | - | 5 | µS | |
| $T_{TEMP_ADC}$[1] | ADC sampling time when reading the temperature | 15 | - | - | µS | |
| $I_{TEMP}$[1] | Temperature sensor operating current | - | 5 | 10 | µA | |

**Note:**

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. $V_{TEMP}$ (mV) = $T_C$ (mV/°C) x Temperature (°C) + $V_{TEMP_OS}$ (mV)

Table 8.5-7 Temperture Sensor Characteristics

## 8.6 Communications Characteristics

### 8.6.1 SPI Dynamic Characteristics

| Symbol | Parameter | Specificaitons[1] | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Unit | |
| $F_{SPICLK}$<br>$1/ T_{SPICLK}$ | SPI clock frequency | - | - | 36 | MHz | 1.71 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| $t_{CLKH}$ | Clock output High time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{CLKL}$ | Clock output Low time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{DS}$ | Data input setup time | 0 | - | - | nS | |
| $t_{DH}$ | Data input hold time | 8.8 | - | - | nS | |
| $t_V$ | Data output valid time | - | - | 8.7 | nS | 1.71 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |

**Note:**

1. Guaranteed by design, not tested in production.

Table 8.6-1 SPI Master Mode Characteristics

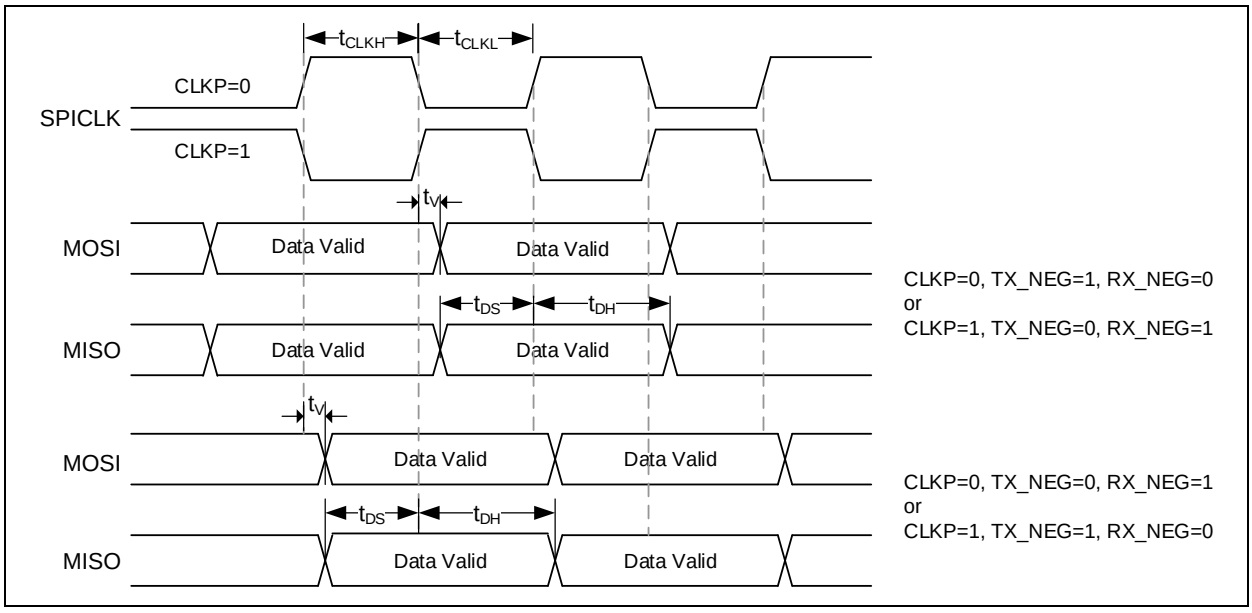



Figure 8.6-1 SPI Master Mode Timing Diagram

| Symbol | Parameter | Specificaitons[1] | | | | Test Conditions |
|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Unit | |
| $F_{SPICLK}$<br>$1/ T_{SPICLK}$ | SPI clock frequency | - | - | 16 | | 2.7 V ≤ VDD ≤ 3.6 V, CL = 30 pF |
| | | - | - | 14 | | 1.71 V ≤ VDD ≤ 3.6 V, CL = 30 pF |
| $t_{CLKH}$ | Clock output High time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{CLKL}$ | Clock output Low time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 2ns | - | - | | 2.7 V ≤ VDD ≤ 3.6 V, CL = 30 pF |
| | | 1 $T_{SPICLK}$ + 3ns | - | - | | 1.71 V ≤ VDD ≤ 3.6 V, CL = 30 pF |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | nS | |
| $t_{DS}$ | Data input setup time | 0 | - | - | nS | |
| $t_{DH}$ | Data input hold time | 7.4 | - | - | nS | |
| $t_V$ | Data output valid time | - | - | 32 | | 2.7 V ≤ VDD ≤ 3.6 V, CL = 30 pF |
| | | - | - | 36 | | 1.71 V ≤ VDD ≤ 3.6 V, CL = 30 pF |

**Note:**

1. Guaranteed by design, not tested in production.

Table 8.6-2 SPI Slave Mode Characteristics

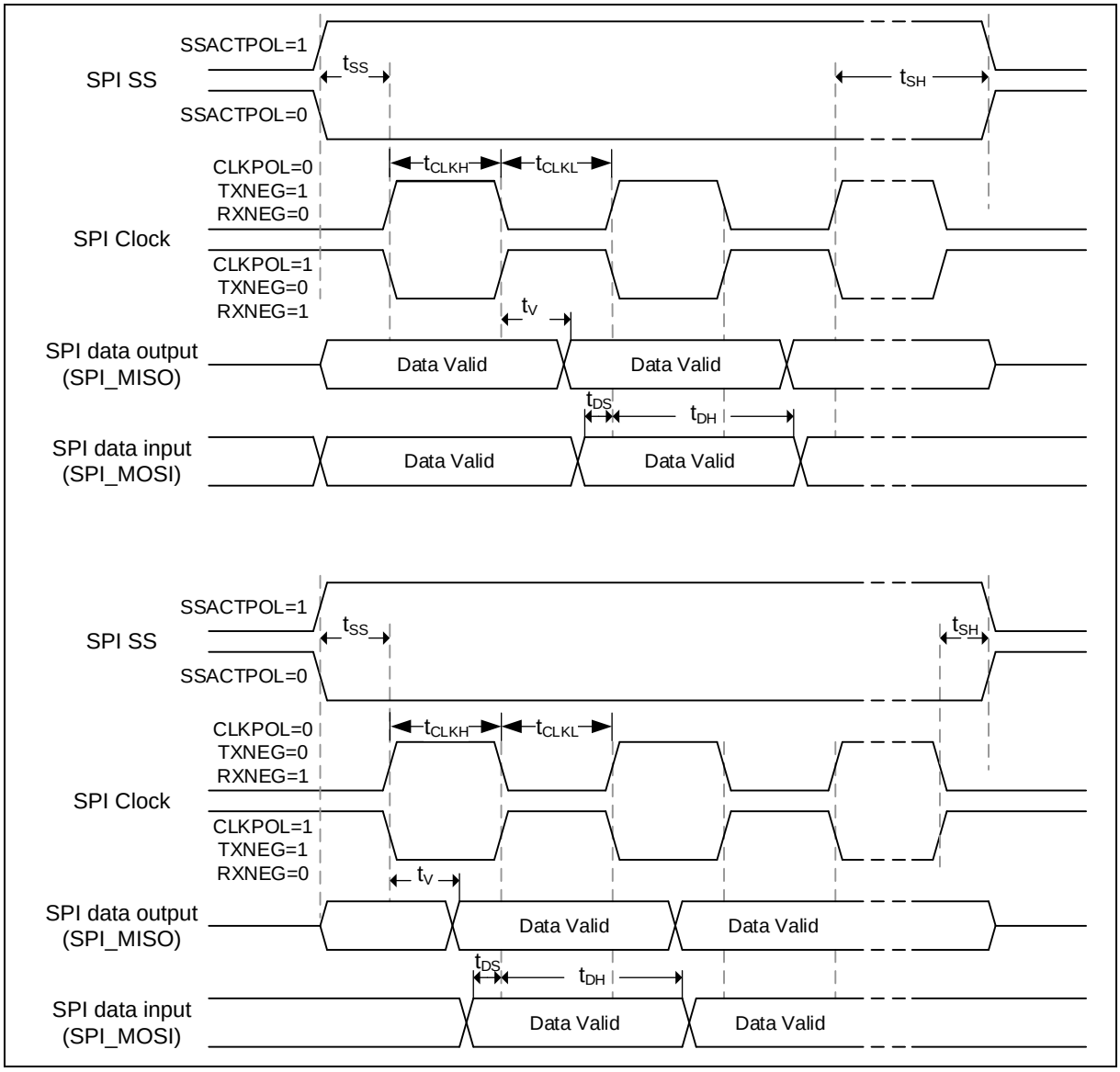



Figure 8.6-2 SPI Slave Mode Timing Diagram

### 8.6.2 I²C Dynamic Characteristics

| Symbol | Parameter | Standard Mode[1][2] | | Fast Mode[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{LOW}$ | SCL low period | 4.7 | - | 1.3 | - | μS |
| $t_{HIGH}$ | SCL high period | 4 | - | 0.6 | - | μS |
| $t_{SU;\ STA}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | μS |
| $t_{HD;\ STA}$ | START condition hold time | 4 | - | 0.6 | - | μS |
| $t_{SU;\ STO}$ | STOP condition setup time | 4 | - | 0.6 | - | μS |
| $t_{BUF}$ | Bus free time | 4.7[3] | - | 1.2[3] | - | μS |
| $t_{SU;DAT}$ | Data setup time | 250 | - | 100 | - | nS |
| $t_{HD;DAT}$ | Data hold time | 0[4] | 3.45[5] | 0[4] | 0.8[5] | μS |
| $t_r$ | SCL/SDA rise time | - | 1000 | 20+0.1$C_b$ | 300 | nS |
| $t_f$ | SCL/SDA fall time | - | 300 | - | 300 | nS |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

**Notes:**

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 I²C Characteristics

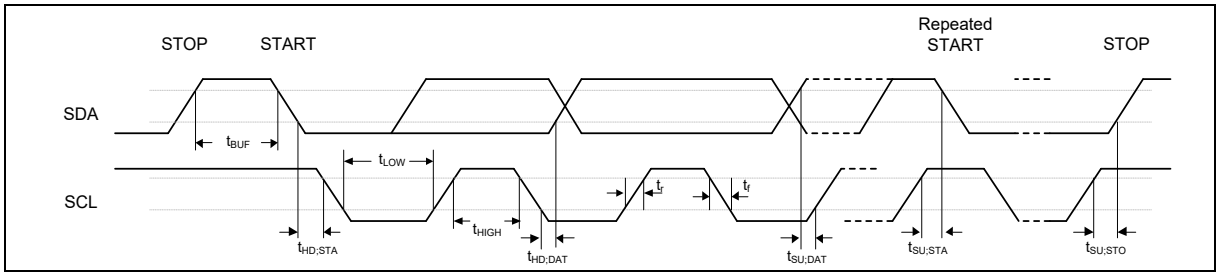



Figure 8.6-3 I²C Timing Diagram

### 8.6.3 USCI - SPI Dynamic Characteristics

| Symbol | Parameter | Min [1] | Typ | Max[1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $F_{SPICLK}$<br>$1/ T_{SPICLK}$ | SPI clock frequency | - | - | $f_{PCLK}$ / 2 | MHz | 1.71 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| $t_{CLKH}$ | Clock output High time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{CLKL}$ | Clock output Low time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{DS}$ | Data input setup time | 0 | - | - | nS | |
| $t_{DH}$ | Data input hold time | 2 | - | - | nS | |
| $t_V$ | Data output valid time | - | - | 1 | nS | 1.71 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |

**Note:**

1. Guaranteed by design, not tested in production.

Table 8.6-4 USCI-SPI Master Mode Characteristics

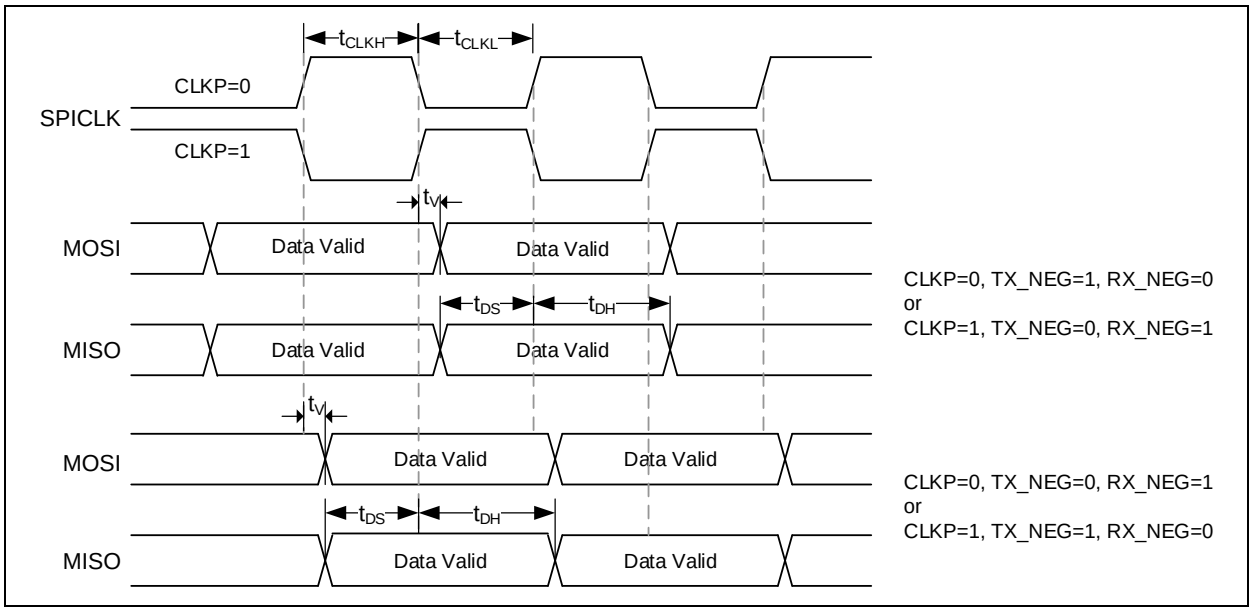



Figure 8.6-4 USCI-SPI Master Mode Timing Diagram

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $F_{SPICLK}$<br>$1/ T_{SPICLK}$ | SPI clock frequency | - | - | 13 | MHz | 2.7 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| | | - | - | 12 | | 1.71 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| $t_{CLKH}$ | Clock output High time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{CLKL}$ | Clock output Low time | $T_{SPICLK}$ / 2 | | | nS | |
| $t_{SS}$ | Slave select setup time | 1 $T_{SPICLK}$ + 2ns | - | - | | 2.7 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| | | 1 $T_{SPICLK}$ + 3ns | - | - | | 1.8 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| $t_{SH}$ | Slave select hold time | 1 $T_{SPICLK}$ | - | - | nS | |
| $t_{DS}$ | Data input setup time | 0 | - | - | nS | |
| $t_{DH}$ | Data input hold time | 2 | - | - | nS | |
| $t_V$ | Data output valid time | - | - | 38 | | 2.7 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |
| | | - | - | 40 | | 1.8 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF |

**Note:**

1. Guaranteed by design, not tested in production.

Table 8.6-5 USCI-SPI Slave Mode Characteristics

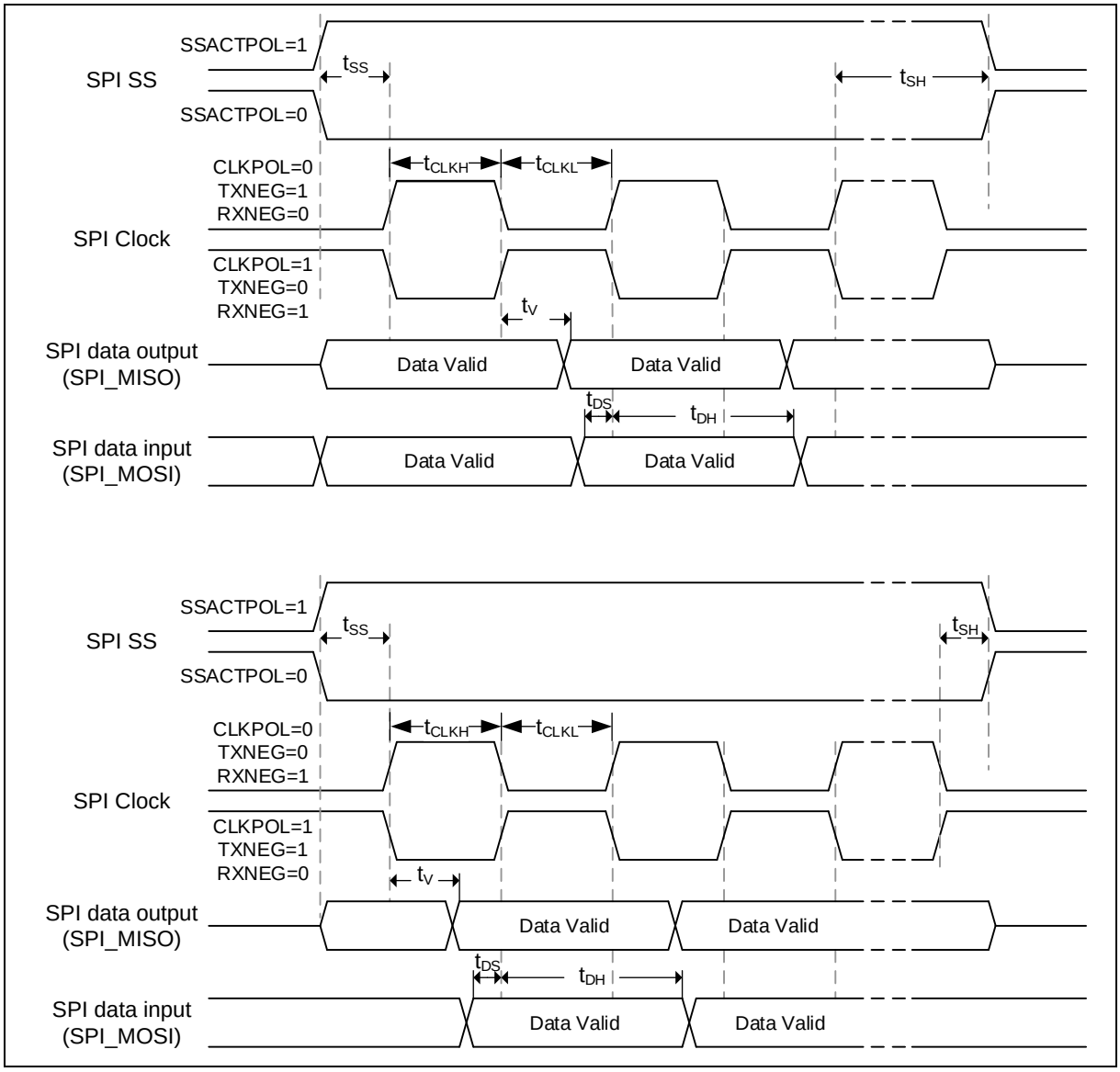



Figure 8.6-5 USCI-SPI Slave Mode Timing Diagram

### 8.6.4 USCI-I²C Dynamic Characteristics

| Symbol | Parameter | Standard Mode[1][2] | | Fast Mode[1][2] | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{LOW}$ | SCL low period | 4.7 | - | 1.3 | - | μS |
| $t_{HIGH}$ | SCL high period | 4 | - | 0.6 | - | μS |
| $t_{SU;\ STA}$ | Repeated START condition setup time | 4.7 | - | 0.6 | - | μS |
| $t_{HD;\ STA}$ | START condition hold time | 4 | - | 0.6 | - | μS |
| $t_{SU;\ STO}$ | STOP condition setup time | 4 | - | 0.6 | - | μS |
| $t_{BUF}$ | Bus free time | 4.7[3] | - | 1.2[3] | - | μS |
| $t_{SU;DAT}$ | Data setup time | 250 | - | 100 | - | nS |
| $t_{HD;DAT}$ | Data hold time | 0[4] | 3.45[5] | 0[4] | 0.8[5] | μS |
| $t_r$ | SCL/SDA rise time | - | 1000 | 20+0.1$C_b$ | 300 | nS |
| $t_f$ | SCL/SDA fall time | - | 300 | - | 300 | nS |
| $C_b$ | Capacitive load for each bus line | - | 400 | - | 400 | pF |

**Notes:**

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-6 USCI-I²C Characteristics

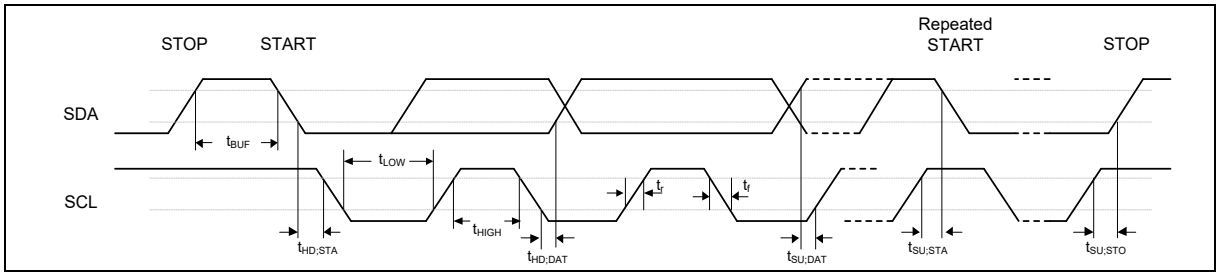



Figure 8.6-6 USCI-I²C Timing Diagram

### 8.6.5 CAN Characteristics

| Symbol | Parameter | Min | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|
| $t_{CAN_TXD}$ | TXD output delay | - | 22.5 | nS | 2.7 V ≤ VDD ≤ 3.6 V, $C_L$ = 30 pF<br>Normal slew rate |
| $t_{CAN_RXD}$ | RXD input delay | - | 12 | nS | 2.7 V ≤ VDD ≤ 3.6 V |

**Note:**

1. Guaranteed by design, not tested in production.

Table 8.6-7 CAN Characteristics

### 8.6.6 USB Characteristics

#### *8.6.6.1 USB Full-Speed Characteristics*

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Operation voltage | 3.0 | 3.3 | 3.6 | V | |
| $V_{BUS}$ | USB $V_{BUS}$ voltage detection voltage | 0 | - | $V_{DD}$ | V | |
| $V_{IH}$ | Input high | 2 | - | - | V | - |
| $V_{IL}$ | Input low | - | - | 0.8 | V | - |
| $V_{DI}$ | Differential input sensitivity | - | 0.2 | - | V | \|(USB_D+) - (USB_D-)\| |
| $V_{CM}$ | Differential common-mode range | 0.8 | - | 2.5 | V | Includes $V_{DI}$ range |
| $V_{SE}$ | Single-ended receiver threshold | 0.8 | - | 2 | V | - |
| | Receiver hysteresis | - | 200 | - | mV | - |
| $V_{OL}$ | Output low (driven) | 0 | - | 0.3 | V | - |
| $V_{OH}$ | Output high (driven) | 2.8 | - | 3.6 | V | - |
| $V_{CRS}$ | Output signal cross voltage | 1.3 | - | 2 | V | - |
| $R_{PU}$ | Pull-up resistor at D+ | 0.9 | 1.2 | 1.575 | kΩ | - |
| $R_{PD}$ | Pull-down resistor at D+ and D- | 14.25 | 19.5 | 24.8 | kΩ | - |
| $V_{TRM}$ | Termination voltage for upstream port pull-up (RPU) | 3 | - | 3.6 | V | - |
| $Z_{DRV}$ [2] | Driver output resistance | 10.9 | - | 25.1 | Ω | Steady state drive |
| $C_{IN}$ | Transceiver capacitance | - | - | 26 | pF | Pin to GND |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 43 Ω).

Table 8.6-8 USB Full-Speed Characteristics

### 8.6.6.2 USB Full-Speed PHY characteristics

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $T_{FR}$ | rise time | 4 | - | 20 | nS | $C_L$=50 pF |
| $T_{FF}$ | fall time | 4 | - | 20 | nS | $C_L$=50 pF |
| $T_{FRFF}$ | rise and fall time matching | 90 | - | 111.11 | % | $T_{FRFF} = T_{FR}/T_{FF}$ |

**Note:**

1.Guaranteed by characterization result, not tested in production.

Table 8.6-9 USB Full-Speed PHY Characteristics

### 8.6.7 UTCPD Characteristics

| Symbol | Parameter | Min [1] | Typ | Max [1] | Unit | Test Conditions |
|---|---|---|---|---|---|---|
| $V_{DD}$ | UTCPD Operation voltage | 3.0 | 3.3 | 3.6 | V | |
| $V_{BUS}$[2] | USB $V_{BUS}$ voltage detection voltage | 0.4 | - | $V_{DD}$ | V | VBSCALE = 0x0 |
| | | 0.2 | - | $V_{DD}$ | V | VBSCALE = 0x1 |
| $V_{OH_CC}$ | CC output high voltage | 1.05 | 1.125 | 1.2 | V | |
| $V_{OL_CC}$ | CC output low voltage | -0.075 | - | 0.075 | V | |
| $t_{f(CC)}$ / $t_{r(CC)}$ | CC rising time and falling time. 10% and 90% amplitude points, minimum is under unloaded condition. | 300 | - | - | nS | |
| $I_{CC_DEF}$ | Source current for default USB power when acting as DFP | 64 | 80 | 96 | µA | |
| $I_{CC_1.5A}$ | Source current for 1.5A power when acting as DFP | 165.6 | 180 | 194.4 | µA | |
| $I_{CC_3A}$ | Source current for 3A USB power when acting as DFP | 303.6 | 330 | 356.4 | µA | |
| Rd | Pull down CC termination resistance when acting as UFP | 4.59 | 5.1 | 5.61 | kΩ | |
| Rd_db[3] | Pull down CC termination resistance when acting as UFP with dead battery | - | 4.5 | - | kΩ | All supplies forced to 0V and 1V applied at CC and DB_CC pin. |
| Rd_ccdb[3] | Pull down CCDB resistance to keep CCDB1 and CCDB2 as low level. | 0.75 | - | 1.25 | MΩ | |

**Notes:**

1. Guaranteed by characterization result, not tested in production.
2. When PA.12 ($V_{BUS}$) OFFDIG is set to 1, the UTCPD will see $V_{BUS}$ voltage. In this condition, $V_{BUS}$ should be divided and make sure no larger than $V_{DD}$ all the time.
3. The GPIO characteristics of CC and CCDB pin are affected by Rd_db and Rd_ccdb respectively.

Table 8.6-10 UTCPD Characteristics

## 8.7 RRAM DC Electrical Characteristics

The devices are shipped to customers with the RRAM memory erased.

| Symbol | Parameter | Min[1] | Typ | Max[1] | Unit | Test Condition |
|---|---|---|---|---|---|---|
| $T_{PROG}$[2] | Program time (one word) | - | 300 | 500 | μS | $T_J$ = 25℃ |
| | Word line program time (64 words) 256-byte address aligmement | - | 2500 | 6400 | μS | |
| $I_{DD1}$ | Read current | - | 5.2 | - | mA | |
| $I_{DD2}$ | Program current | - | 11.0 | - | mA | |
| $N_{ENDUR}$ | Cycling Endurance | 10,000 | - | - | cycles[3] | $T_J$ = -40℃~125℃ |
| $T_{RET}$ | Data retention | 10 | - | - | year | 10 kcycle[3] , $T_J$ = 125℃ |

**Notes:**

1. Guaranteed by design, not tested in production.
2. The program command is only supported at power level 1 (PL1).
3. Number of RRAM program cycles.

Table 8.7-1 RRAM DC Electrical Characteristics

# 9 ABBREVIATIONS

## 9.1 Abbreviations

| Acronym | Description |
|---|---|
| ACMP | Analog Comparator Controller |
| ADC | Analog-to-Digital Converter |
| AES | Advanced Encryption Standard |
| APB | Advanced Peripheral Bus |
| AHB | Advanced High-Performance Bus |
| BOD | Brown-out Detection |
| CAN | Controller Area Network |
| CCAP | Camera Capture Interface |
| DAP | Debug Access Port |
| DES | Data Encryption Standard |
| EADC | Enhanced Analog-to-Digital Converter |
| EBI | External Bus Interface |
| EMAC | Ethernet MAC Controller |
| EPWM | Enhanced Pulse Width Modulation |
| FIFO | First In, First Out |
| RMC | RRAM Memory Controller |
| FPU | Floating-point Unit |
| GPIO | General-Purpose Input/Output |
| HCLK | The Clock of Advanced High-Performance Bus |
| HIRC | 12 MHz Internal High Speed RC Oscillator |
| HXT | 4~24 MHz External High Speed Crystal Oscillator |
| IAP | In Application Programming |
| ICP | In Circuit Programming |
| ISP | In System Programming |
| LDO | Low Dropout Regulator |
| LIN | Local Interconnect Network |
| LIRC | 10 kHz internal low speed RC oscillator (LIRC) |
| MPU | Memory Protection Unit |
| NVIC | Nested Vectored Interrupt Controller |
| PCLK | The Clock of Advanced Peripheral Bus |
| PDMA | Peripheral Direct Memory Access |
| PLL | Phase-Locked Loop |

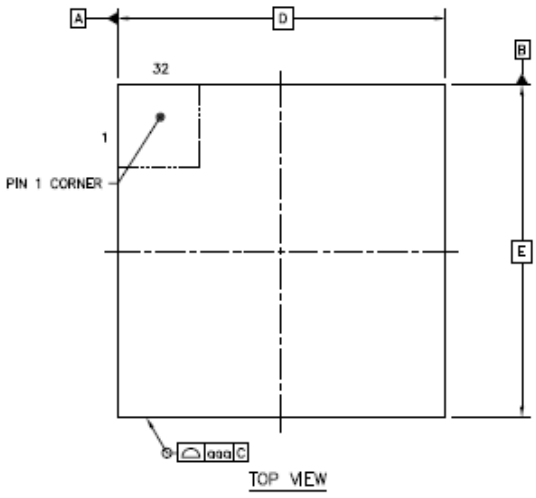
| | |
|---|---|
| PWM | Pulse Width Modulation |
| EQEI | Enhanced Quadrature Encoder Interface |
| SD | Secure Digital |
| SPI | Serial Peripheral Interface |
| SPS | Samples per Second |
| TDES | Triple Data Encryption Standard |
| TK | Touch Key |
| TMR | Timer Controller |
| UART | Universal Asynchronous Receiver/Transmitter |
| UCID | Unique Customer ID |
| USB | Universal Serial Bus |
| WDT | Watchdog Timer |
| WWDT | Window Watchdog Timer |

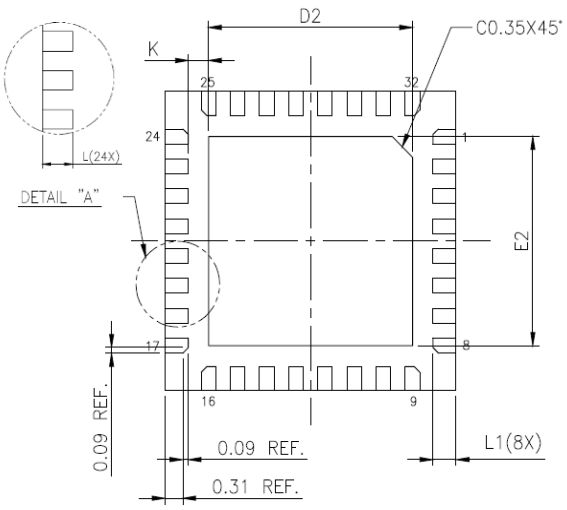
Table 9.1-1 List of Abbreviations

# 10 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compilant.

## 10.1 QFN 33L (5x5x0.8 mm, Pitch 0.5 mm, Lead Length 0.4 mm)



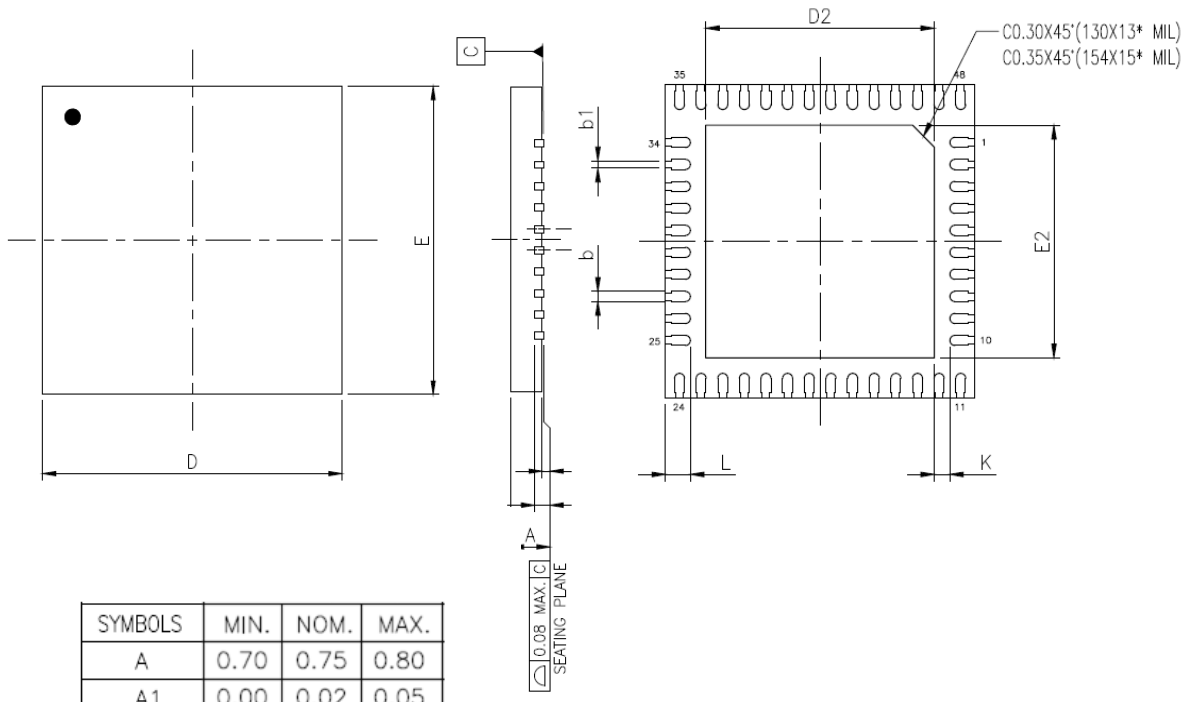




mm

| SYMBOLS | Min | Nom | Max |
|---|---|---|---|
| A | 0.7 | 0.75 | 0.8 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | | 0.2 REF | |
| b | 0.18 | 0.25 | 0.3 |
| D | | 5.0 BSC | |
| E | | 5.0 BSC | |
| e | | 0.5 BSC | |
| D2 | 3.45 | 3.5 | 3.55 |
| E2 | 3.45 | 3.5 | 3.55 |
| L | 0.35 | 0.4 | 0.45 |
| L1 | 0.33 | 0.4 | 0.43 |
| K | 0.2 | - | - |

QFN32_5x5_0.80_0.50_0.40_3.50x3.50

## 10.2 QFN 48L (5x5x0.8 mm, Pitch 0.35 mm, Lead Length 0.4 mm)

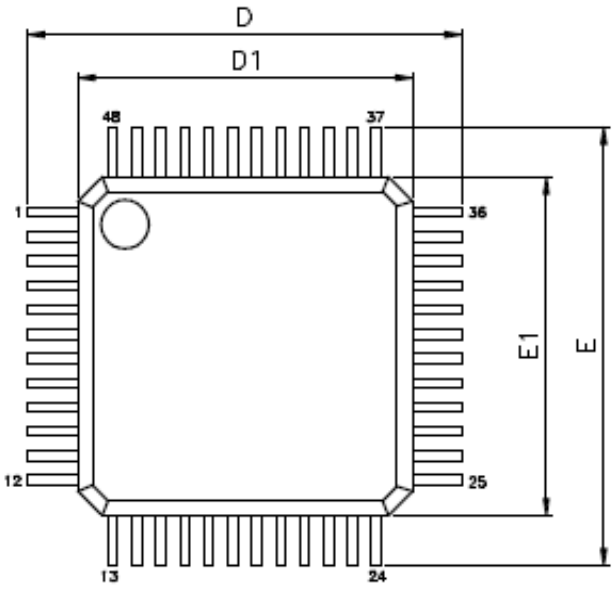



| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.13 | 0.18 | 0.23 |
| b1 | 0.07 | 0.12 | 0.17 |
| D | | 5.00 BSC | |
| E | | 5.00 BSC | |
| e | | 0.35 BSC | |
| K | 0.20 | — | — |

| PAD SIZE | D2 | | | E2 | | | L | | |
|---|---|---|---|---|---|---|---|---|---|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| 130X13* MIL | 3.65 | 3.70 | 3.75 | 3.65 | 3.70 | 3.75 | 0.35 | 0.40 | 0.45 |
| 154X15* MIL | 3.65 | 3.70 | 3.75 | 3.65 | 3.70 | 3.75 | 0.35 | 0.40 | 0.45 |

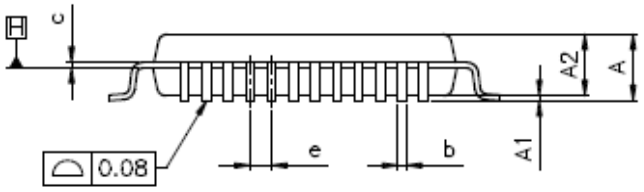
QFN48_5x5_0.80_0.35_0.40_3.70x3.70

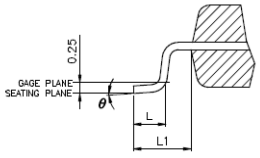
### 10.3 LQFP 48L (7x7x1.4 mm Footprint 2.0 mm)




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

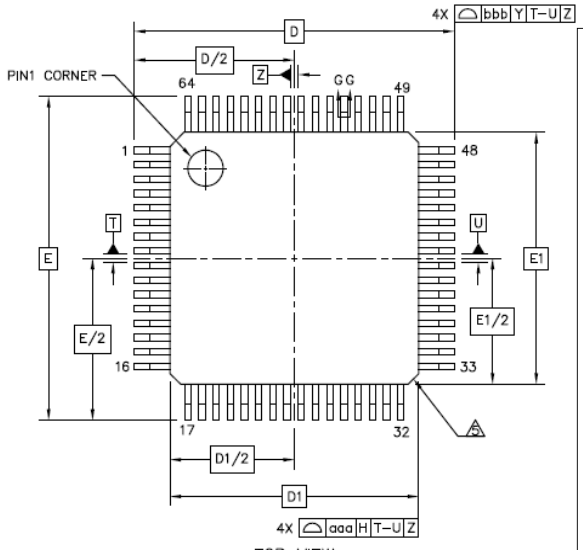
| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | -- | -- | 1.60 |
| A1 | 0.05 | -- | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | -- | 0.20 |
| D | 8.80 | 9.00 | 9.20 |
| D1 | 6.90 | 7.00 | 7.10 |
| E | 8.80 | 9.00 | 9.20 |
| E1 | 6.90 | 7.00 | 7.10 |
| e | 0.50 BSC | | |
| L | 0.45 | 0.60 | 0.75 |
| L1 | 1.00 REF | | |
| S | 0.20 | -- | -- |
| $\theta$ | 0° | 3.5° | 7° |
| $\theta$1 | 0° | -- | -- |
| $\theta$2 | 11° | 12° | 13° |
| $\theta$3 | 11° | 12° | 13° |

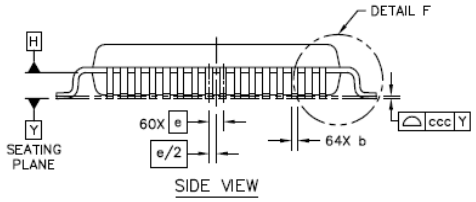


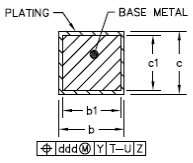



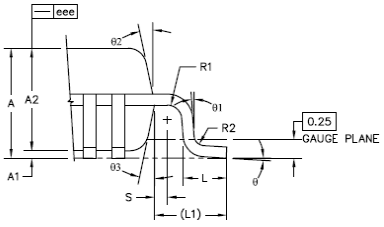

LQFP48_7X7_1.40_0.50_1.00

## 10.4 LQFP 64L (7x7x1.4 mm Footprint 2.0 mm)



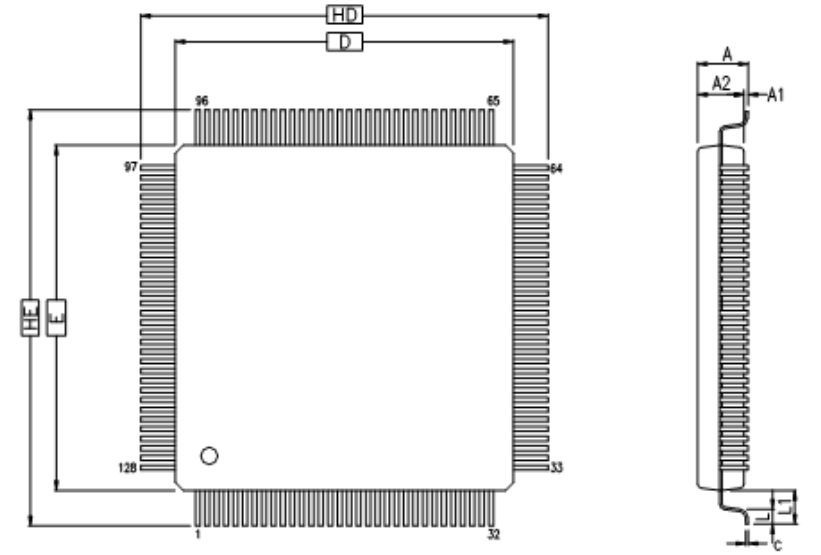




| | | SYMBOL | MIN | NOM | MAX |
|---|---|---|---|---|---|
| TOTAL THICKNESS | | A | --- | --- | 1.6 |
| STAND OFF | | A1 | 0.05 | --- | 0.15 |
| MOLD THICKNESS | | A2 | 1.35 | 1.4 | 1.45 |
| LEAD WIDTH(PLATING) | | b | 0.13 | 0.18 | 0.23 |
| LEAD WIDTH | | b1 | 0.13 | 0.16 | 0.19 |
| L/F THICKNESS(PLATING) | | c | 0.09 | --- | 0.2 |
| L/F THICKNESS | | c1 | 0.09 | --- | 0.16 |
| BODY SIZE | X | D | 8.8 | 9 | 9.2 |
| | Y | E | 8.8 | 9 | 9.2 |
| | X | D1 | 6.8 | 7 | 7.2 |
| | Y | E1 | 6.8 | 7 | 7.2 |
| LEAD PITCH | | e | 0.4 BSC | | |
| | | L | 0.45 | 0.6 | 0.75 |
| FOOTPRINT | | L1 | 1 REF | | |
| | | θ | 0° | 3.5° | 7° |
| | | θ1 | 0° | --- | --- |
| | | θ2 | 11° | 12° | 13° |
| | | θ3 | 11° | 12° | 13° |
| | | R1 | 0.08 | --- | --- |
| | | R2 | 0.08 | --- | 0.2 |
| | | S | 0.2 | --- | --- |
| COPLANARITY | | ccc | 0.08 | | |
| LEAD OFFSET | | ddd | 0.07 | | |
| MOLD FLATNESS | | eee | 0.05 | | |

LQFP64_7X7_1.40_0.40_1.00

### 10.5 LQFP 128L (14x14x1.4 mm Footprint 2.0 mm)




SIDE VIEW

| SYMBOL | MIN | NOM. | MAX. |
|---|---|---|---|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| HD | 15.85 | 16.00 | 16.15 |
| D | 13.85 | 14.00 | 14.15 |
| HE | 15.85 | 16.00 | 16.15 |
| E | 13.85 | 14.00 | 14.15 |
| b | 0.13 | 0.16 | 0.23 |
| e | - | 0.40 | - |
| θ° | 0 | 3.5 | 7 |
| c | 0.09 | - | 0.20 |
| L | 0.45 | 0.60 | 0.75 |
| L1 | - | 1.00 | - |
| Y | - | - | 0.10 |

LQFP128_14X14_1.40_0.40_1.00

# 11 REVISION HISTORY

| Date | Revision | Description |
|---|---|---|
| 2024.06.12 | 1.00 | • Initial version. |
| 2025.01.07 | 1.01 | • Revised QFN33 multi-function diagram and table in section 4.3.1<br>• Removed UTCPD0_CCDB1 and UTCPD0_CCDB2 of QFN33 in section 4.3.1錯誤! 找不到參照來源。.<br>• Revised temperature sensor spec in Table 8.5-7.<br>• Updated RRAM data retention spec in Table 8.7-1.<br>• Revised internal reference voltage in Table 8.5-6.<br>• Removed BOD15 spec in Table 8.5-2.<br>• Revised clock status description of NPD5, SPD and DPD mode in Table 6.2-2.<br>• Revised the max. PWM clock source from 144 Mhz to 72 Mhz in section 2.1 and chapter 1.<br>• Updated OPA low power mode spec in Table 8.5-5.<br>• Revised HIRC48M, HIRC and MIRC spec in Table 8.4-1, Table 8.4-2 and Table 8.4-3. |
| 2025.03.27 | 1.02 | • Revised HIRC and MIRC spec in Table 8.4-2 and Table 8.4-3 based on HTOL reliability test result.<br>• Added a note marking in HIRC48M and LIRC spec in Table 8.4-1 and Table 8.4-4. |
| 2025.08.18 | 1.03 | • Revised $V_{IH}$ and $V_{IL}$ spec in Table 8.3-9.<br>• Revised QFN33 pin diagram in section 4.2.1. |

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**Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.**

**All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.**

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