NuMicro® Family

Arm® Cortex®-M23-based Microcontroller

M2A23 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro M2A23 series is an automotive grade microcontroller with -40°C to +125°C operating temperature, 2.5V to 5.5V operating voltage and up to three sets of CAN FD functions to support automotive applications in body control, lighting control, and CAN Bridge/CAN Module.

The M2A23 series is based on Arm Cortex-M23 core running up to 72 MHz. It provides up to 256 Kbytes of embedded Flash Memory, 24 Kbytes of embedded SRAM, and 4 Kbytes of Flash loader memory (LDROM) for In-System Programming (ISP) that supports CAN FD/SPI/UART/I^2C boot loader function.

The M2A23 series supports plenty of peripherals, including up to four 32-bit timers, 12-ch 16-bit PWM generators, LIN function, two sets of UART with One-Wire mode, IrDA and RS485 functions, one set of I^2C, 1 set SPI, two sets of USCI (UART/I^2C/SPI) and two sets of LLSI.

The M2A23 series provides rich analog functions including 16-ch 12-bit ADC, temperature sensor, two sets of ACMP, low voltage reset (LVR) and brown-out detector (BOD) to ensure the system safety and reduce external components.

The package types of the M2A23 series include QFN 48-pin, LQFP 48-pin and LQFP 64-pin.

For the automotive and industrial market, the M2A23 series is targeted at applications such as:

- Body Control
- Ultrasonic Radar
- Advanced Exterior Lighting
- Interior Lighting
- CAN Bridge/CAN Module
- Mini LED

2 FEATURES

Core and System	
Arm Cortex-M23 without TrustZone	• Arm Cortex-M23 core, running up to 72 MHz • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • DSP extension 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option
Low Voltage Reset (LVR)	• LVR with 2.25V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash Memory	• 256 Kbytes on-chip Application ROM (APROM) • Embedded with 2 Kbytes cache, with performance at zero wait cycle in continuous address read access • 4 Kbytes on-chip Flash Memory for user program loader (LDROM) • All on-chip Flash Memory supporting 2 Kbytes page erase • Fast Flash programming verification with CRC-32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function • APROM Function Safety Protect feature
SRAM	• 24 Kbytes on-chip SRAM • Supports byte-, half-word- and word-access

	• Supports parity error check function (SRAM bank0) • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value • Supports order reverse setting and one's complement setting for input data and CRC checksum • Supports 8/16/32-bit of data width • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Up to 6 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Supports Fixed-priority and Round-robin priority modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for low-power system operation • Supports clock failure detection for external crystal oscillators and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to 0.25% accuracy that can optionally be used as a system clock • 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 144 MHz on-chip PLL, sourced from HIRC or HXT, allowing CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal
Timers	
32-bit Timer	• Four 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from

	external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated
Basic PWM (BPWM)	• Four 16-bit counters with 12-bit clock prescale for twenty-four 144 MHz PWM output channel • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger ADC to start conversion
PWM	• Supports maximum clock frequency up to 144 MHz • Up to one PWM module; each module provides 6 output channels. • Supports independent mode for PWM output/Capture input channel • Supports complementary mode for 3 complementary paired PWM output channels: • Dead-time insertion with 12-bit resolution • Two compared values during one period • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution PWM counter: • Up, down or up/down counter operation type • Supports mask function and tri-state enable for each PWM pin • Supports brake function: • Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup) • Noise filter for brake source from pin • Edge detect brake source to control brake state until brake interrupt cleared • Level detect brake source to auto recover function after brake condition removed • Supports interrupt on the following events: • PWM counter match 0, period value or compared value • Brake condition happened • Supports trigger ADC on the following events: • PWM counter match 0, period value or compared value

	• Capture Function Features: • Up to 6 capture input channels with 16-bit resolution • Supports rising or falling capture condition • Supports input rising/falling capture interrupt • Supports rising/falling capture with counter reload option • Supports PDMA transfer function for all PWM channels
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• One set of 12-bit, 16-ch 1.8 Msps SAR ADC with up to 16 single-ended input channels or 1 differential input pairs; 10-bit accuracy is guaranteed • Three internal channels for band-gap VBG, temperature sensor, and AVDD/4 • Supports external V_{REF} pin • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse, PWM or BPWM • Configurable ADC sampling time • Supports PDMA operation
Analog Comparator (ACMP)	• Up to two rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV and 30mV

Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 7.2 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 8-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports PDMA operation • Supports LIN function mode (Only UART0 with LIN function)
I^2C	• Up to one set of I^2C device with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • Supports PDMA operation • Supports setup/hold time programmable
SPI	• Up to one SPI controller with Master/Slave mode • Provides separate 4-level of 32-bit (or 8-level of 16-bit) depth transmit and receive FIFO buffers • Master mode up to 36 MHz (V_{DD} = 2.5 ~5.5V) • Slave mode up to 18 MHz (V_{DD} = 2.5 ~5.5V) • Configurable bit length of a transfer word from 8 to 32-bit • MSB first or LSB first transfer sequence

	• Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode • Supports PDMA operation
Universal Serial Control Interface (USCI)	• Up to two sets of USCI: USCI0 and USCI1 • Supports UART, SPI and I^2C function • Single byte TX and RX buffer mode **USCI_UART** • One transmit buffer and two receive buffer for data payload • Hardware auto flow control function and programmable flow control trigger level • Programmable baud-rate generator • Supports 9-bit data transfer • Baud rate detection by built-in capture event of baud rate generator • Supports Wake-up function (Data and nCTS Wakeup Only) • Supports PDMA transfer **USCI_SPI** • Master or Slave mode operation • Configurable bit length of a transfer word from 4 to 16-bit • One transmit buffer and two receive buffer for data payload • MSB first or LSB first transfer sequence • Word suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Wake-up function: input slave select transition • Supports one data channel half-duplex transfer **USCI_I2C** • Full master and slave device capability • 7-bit/10-bit addressing mode • Communication in Standard mode (100 kbps), Fast mode (up to 400 kbps) and Fast mode plus (1 Mbps) • Multi-master bus • One transmit buffer and two receive buffer for data payload • 10-bit bus time out capability • Supports Bus monitor mode • Wake-up by data toggle or address match in Power-down mode

	• Multiple address recognition • Setup/hold time programmable
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode
Controller Area Network with Feasibility Data Rate (CAN FD)	• Up to three CAN FD controllers • Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015 • Compliant with CAN FD version 1.0 with up to 64 data bytes supported • Supports CAN Error logging, AUTOSAR and SAE J1938 • Built-in 1K word (32-bit) Message SRAM for each CAN FD controller

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)
M2A23YG5AC	M2A23LG5AC	M2A23SG5AC
M2A23YE5AC	M2A23LE5AC	M2A23SE5AC
M2A23YD5AC	M2A23LD5AC	M2A23SD5AC

3.2 M2A23 Series Naming Rule

M2	A23	L	G	6	A	C
Core	**Line**	**Package**	**Flash Memory Size**	**SRAM Size**	**Revision**	**Temperature**
Cortex®-M23	A23: with CAN	Y: QFN48 (5x5 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm)	G: 256 KB E: 128 KB D: 64 KB	5: 24 KB	A	C:-40˚C to +125˚C

3.3 M2A23 Series Selection Guide

PART NUMBER		M2A23YG5AC	M2A23LG5AC	M2A23SG5AC	M2A23YE5AC	M2A23LE5AC	M2A23SE5AC	M2A23YD5AC	M2A23LD5AC	M2A23SD5AC
Flash Memory (KB)		256			128			64		
SRAM (KB)		24								
LDROM (KB)		4								
SPROM (KB)		2								
PLL (MHz)		144								
HXT		√								
LXT		√								
I/O		42	42	55	42	42	55	42	42	55
32-bit Timer		4								
BPWM		6								
PWM		6								
WDT/WWDT		√								
Connectivity	UART	2								
	SPI	1								
	I²C	1								
	USCI*	2								
	LLSI	2								
	CAN FD	3								
12-bit ADC		12	12	16	12	12	16	12	12	16
ACMP		2								
PDMA		6								
Package		QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)	QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)	QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)

USCI*: supports UART, SPI or I²C

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in the Multi-function Pin Diagram section or by using NuTool - PinConfig. The NuTool - PinConfig contains all Nuvoton NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.2 M2A23 Series Pin Configuration

4.2.1 QFN 48-Pin Diagram

Corresponding Part Number: M2A23YG5AC, M2A23YE5AC, M2A23YD5AC

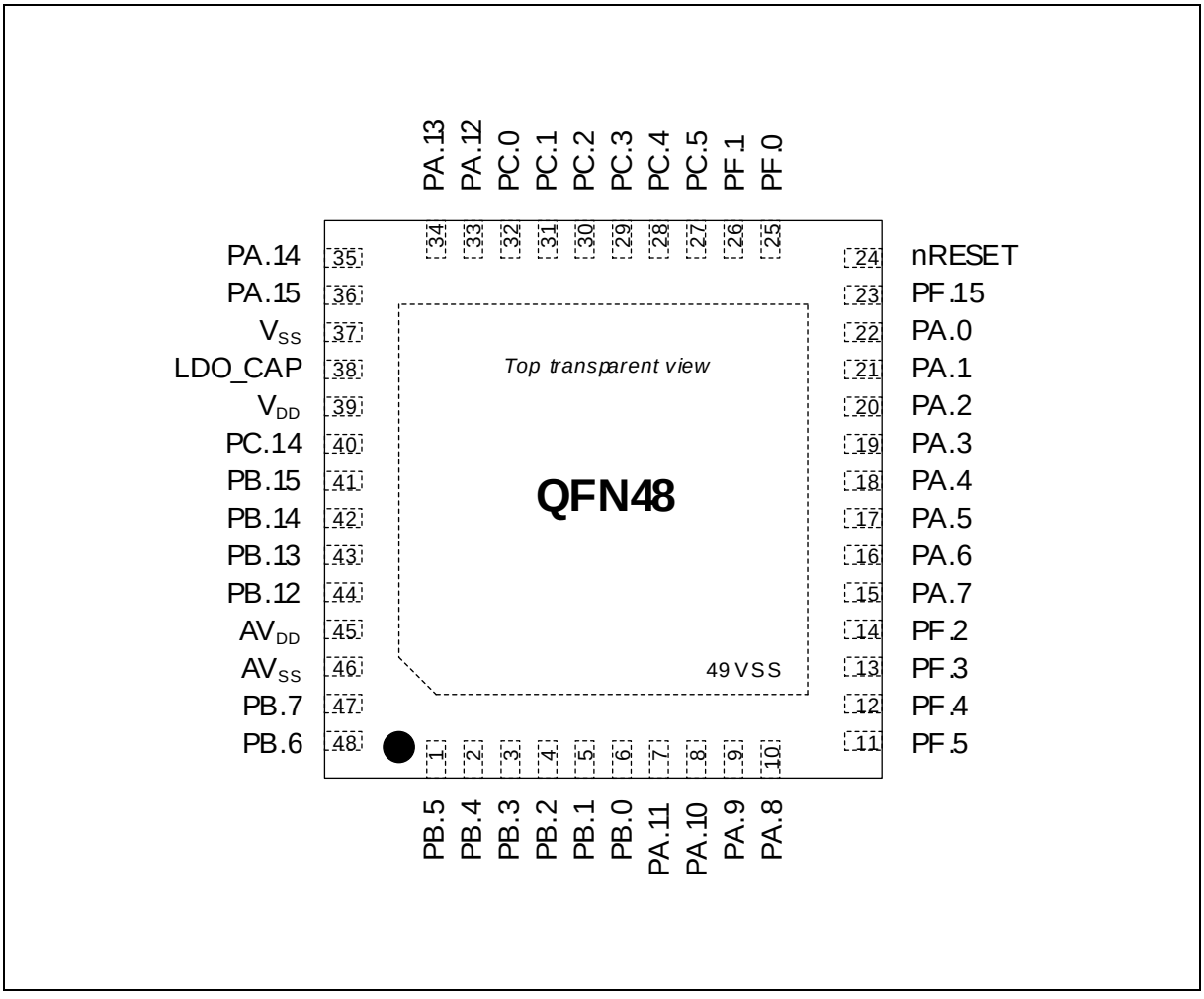


Figure 4.2-1 QFN 48-pin 5x5 Diagram

4.2.2 LQFP 48-Pin Diagram

Corresponding Part Number: M2A23LG5AC, M2A23LE5AC, M2A23LD5AC

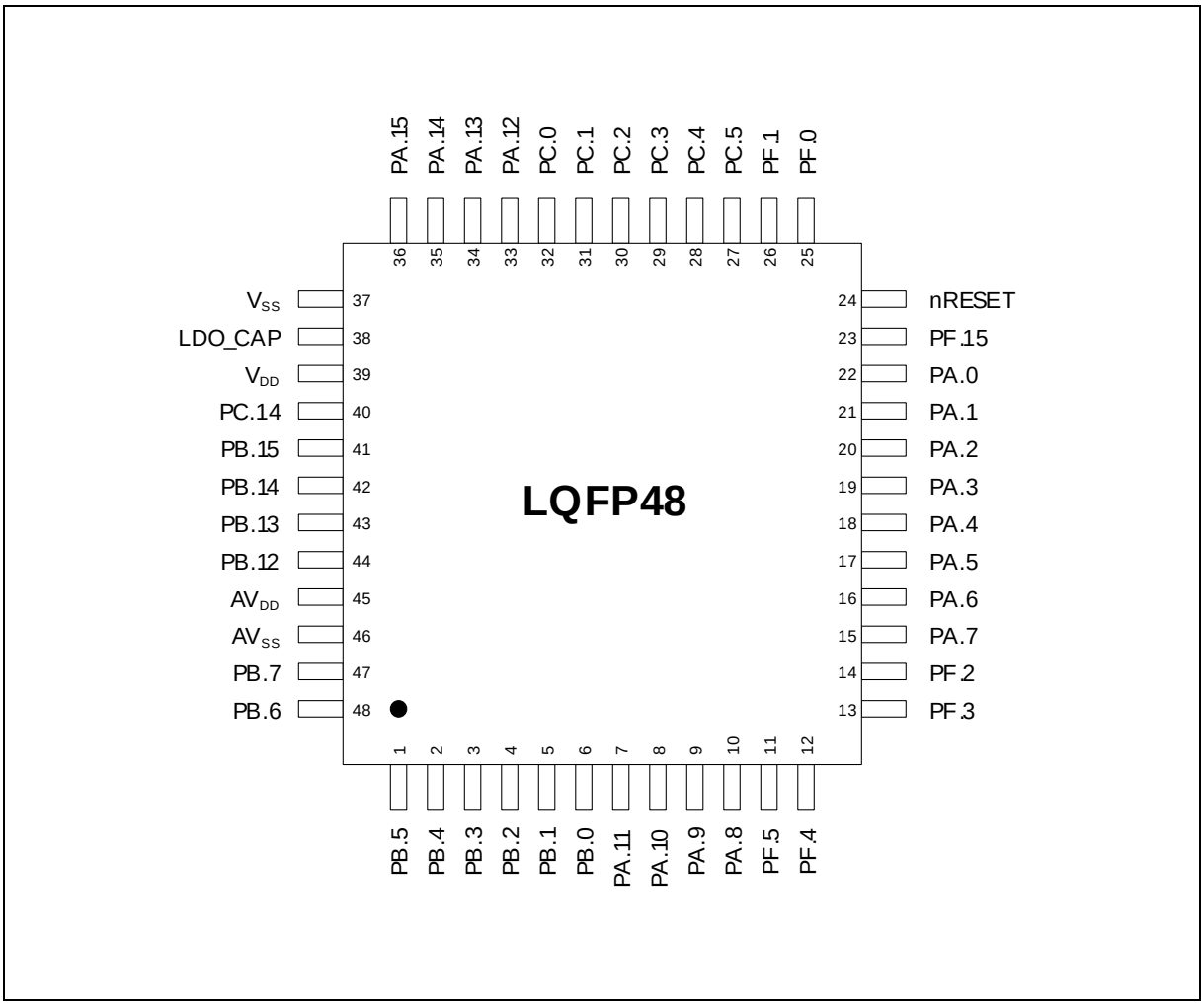


Figure 4.2-2 LQFP 48-pin Diagram

4.2.3 LQFP 64-Pin Diagram

Corresponding Part Number: M2A23SG5AC, M2A23SE5AC, M2A23SD5AC

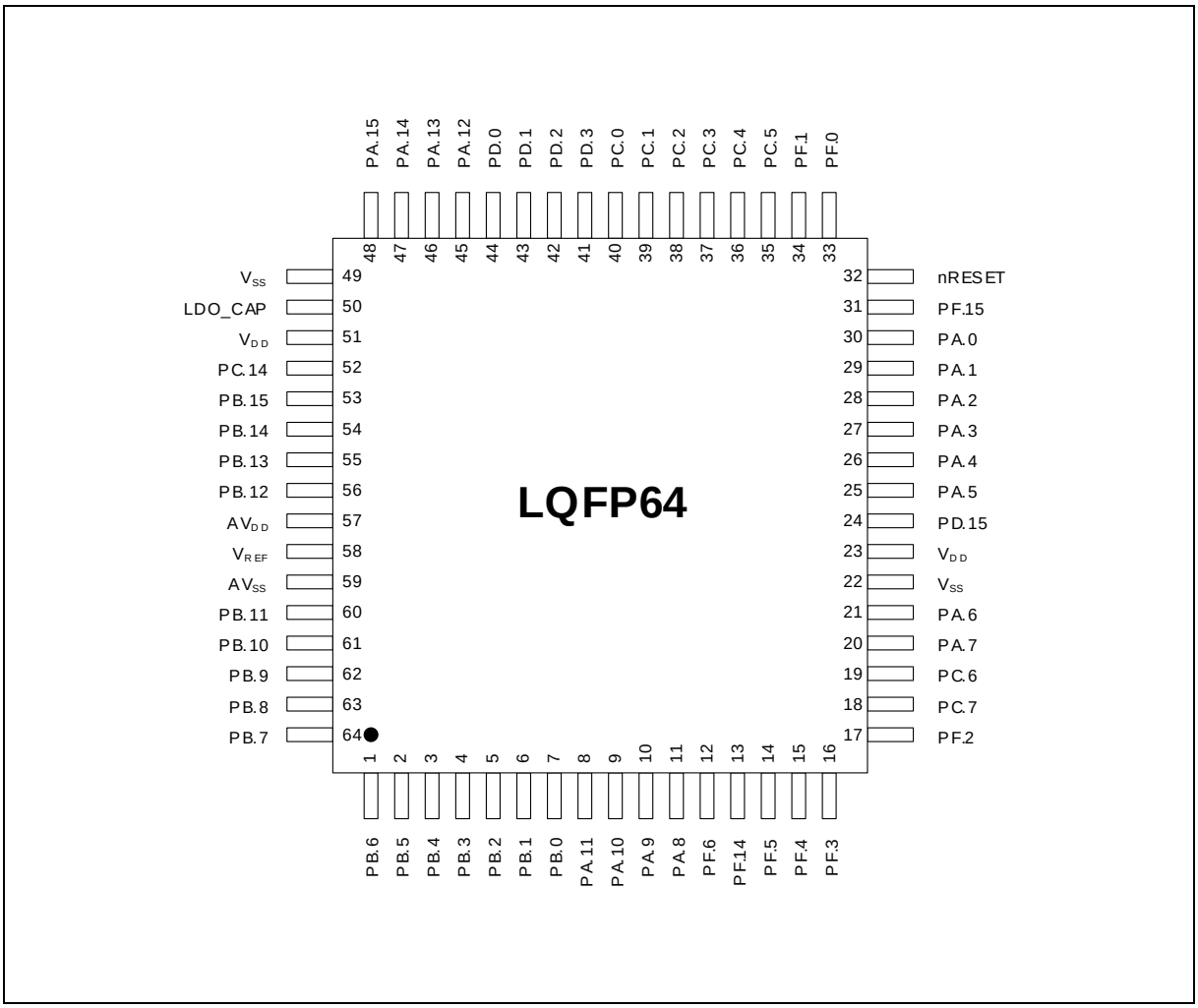


Figure 4.2-3 LQFP 64-pin Diagram

4.3 M2A23 Series Multi-function Pin Diagram

4.3.1 QFN 48-Pin Multi-function Pin Diagram

Corresponding Part Number: M2A23YG5AC, M2A23YE5AC, M2A23YD5AC

4.3.1.1 M2A23YG5AC

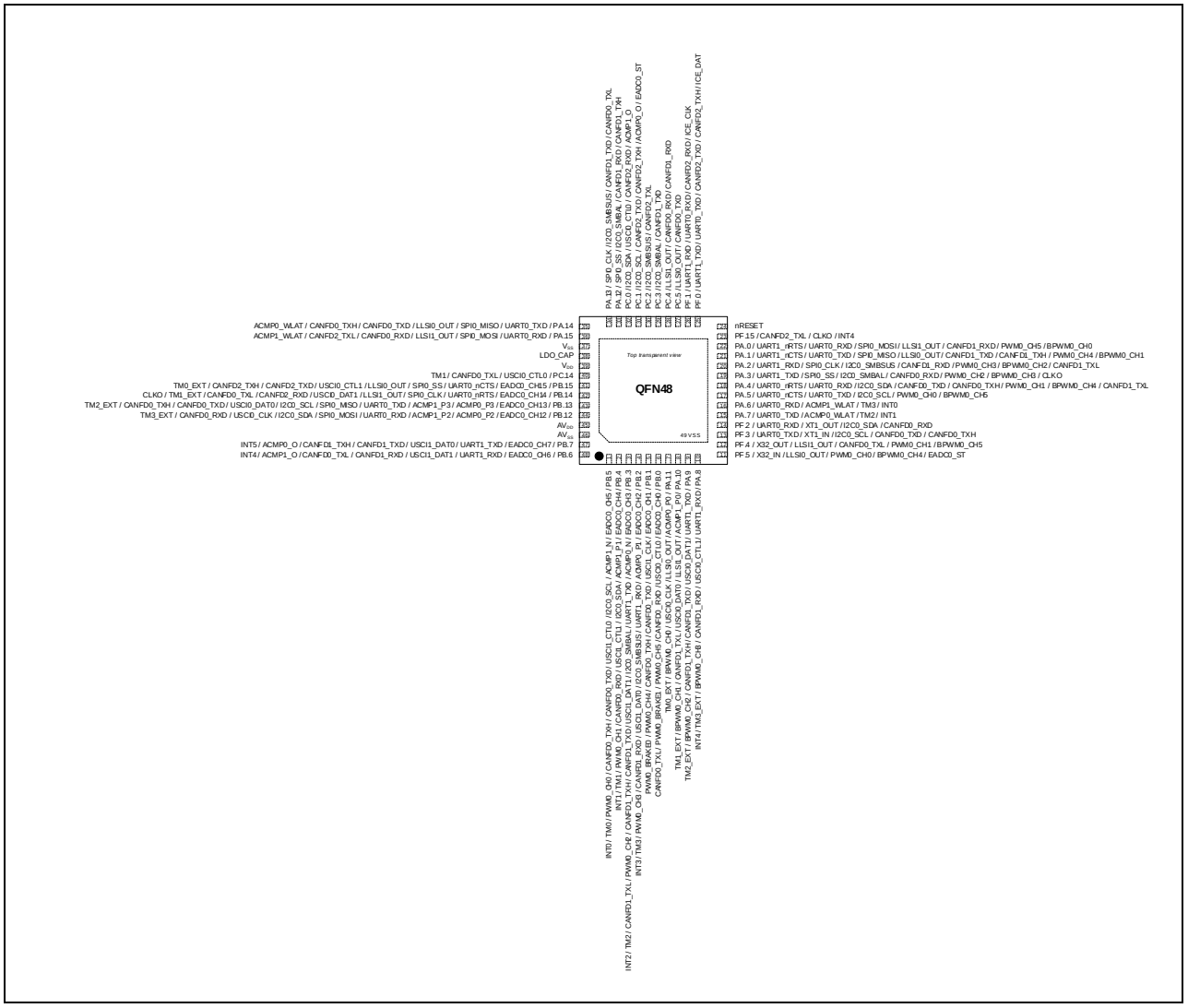


Figure 4.3-1 M2A23YG5AC Multi-function Pin Diagram

Pin	Type	M2A23YG5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD /

Pin	Type	M2A23YG5AC Pin Function
		PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT

Pin	Type	M2A23YG5AC Pin Function
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
49	P	EPAD

4.3.1.2 M2A23YE5AC

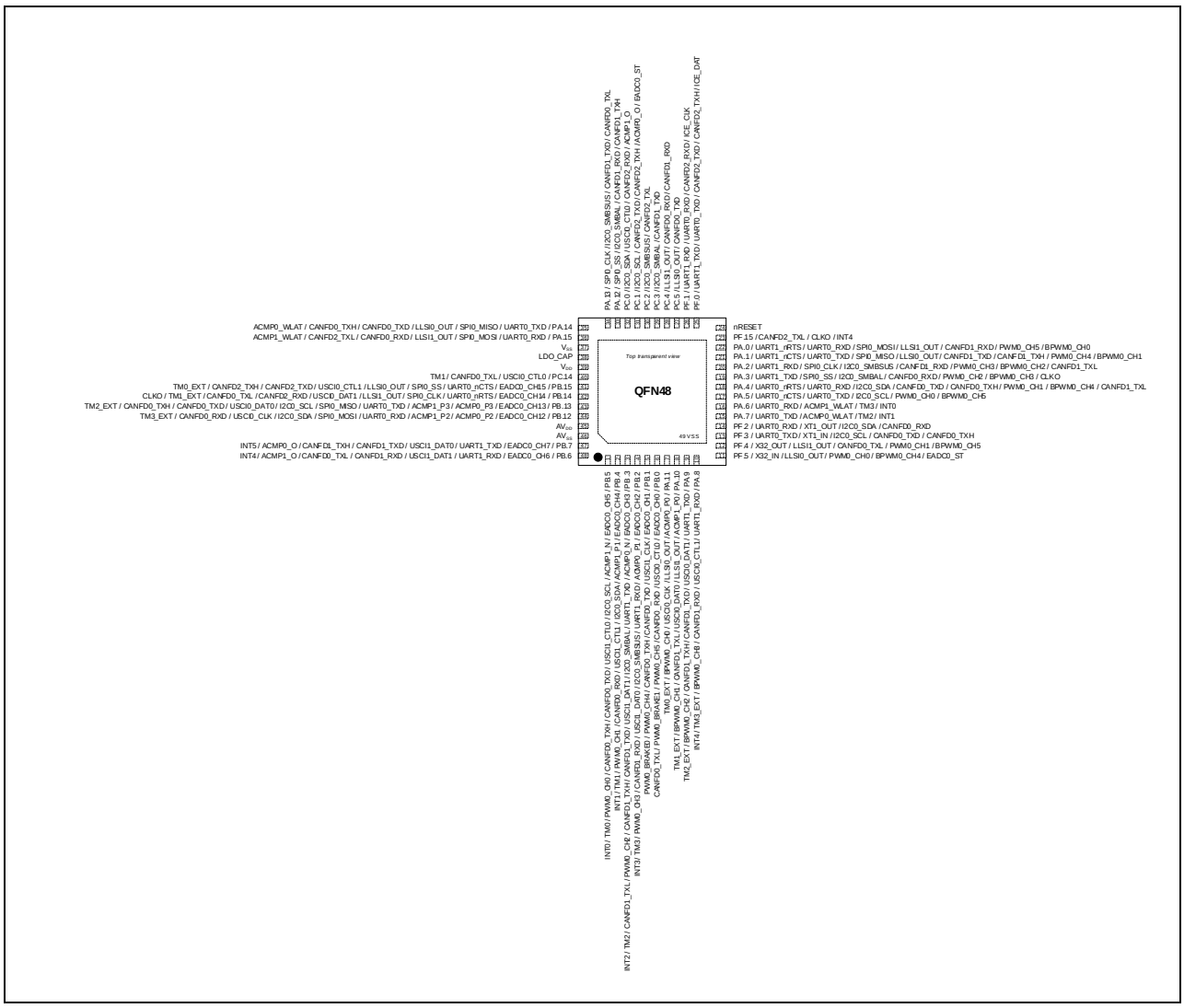


Figure 4.3-2 M2A23YE5AC Multi-function Pin Diagram

Pin	Type	M2A23YE5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT

Pin	Type	M2A23YE5AC Pin Function
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}

Pin	Type	M2A23YE5AC Pin Function
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
49	P	EPAD

4.3.1.3 M2A23YD5AC

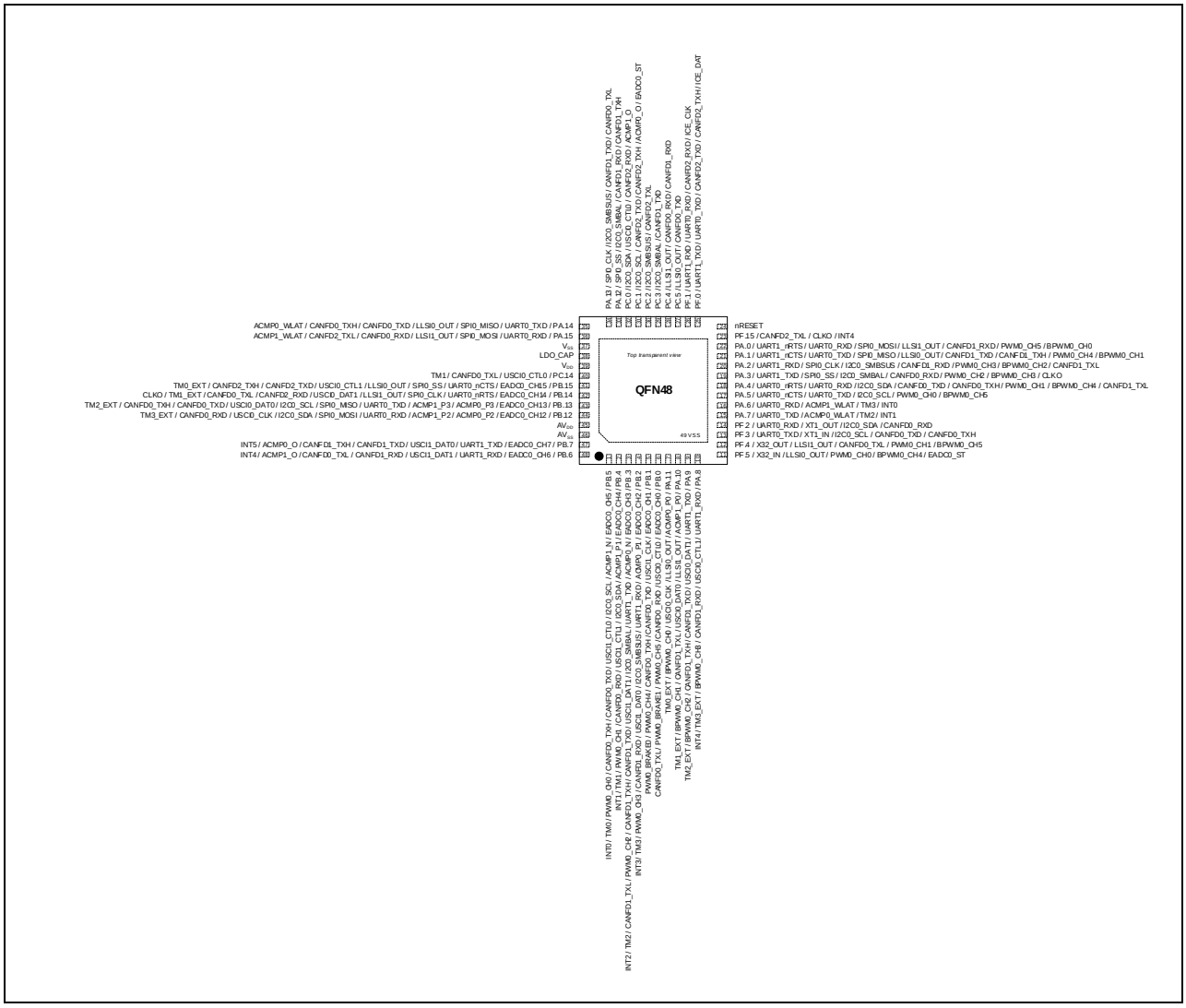


Figure 4.3-3 M2A23YD5AC Multi-function Pin Diagram

Pin	Type	M2A23YD5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT

Pin	Type	M2A23YD5AC Pin Function
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}

Pin	Type	M2A23YD5AC Pin Function
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
49	P	EPAD

4.3.2 LQFP 48-Pin Multi-function Pin Diagram

Corresponding Part Number: M2A23LG5AC, M2A23LE5AC, M2A23LD5AC

4.3.2.1 M2A23LG5AC

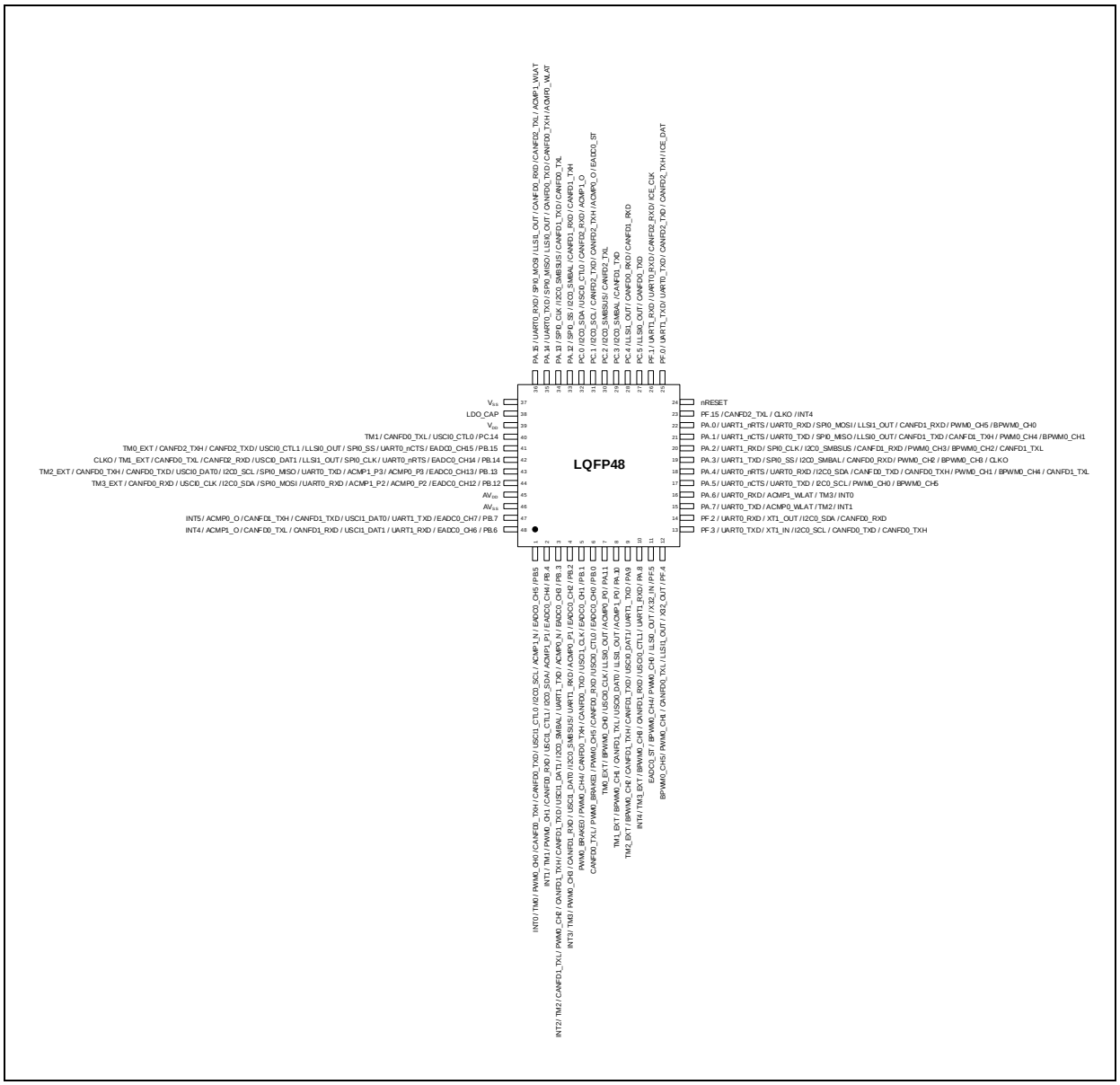


Figure 4.3-4 M2A23LG5AC Multi-function Pin Diagram

Pin	Type	M2A23LG5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2

Pin	Type	M2A23LG5AC Pin Function
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL

Pin	Type	M2A23LG5AC Pin Function
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4

4.3.2.2 M2A23LE5AC

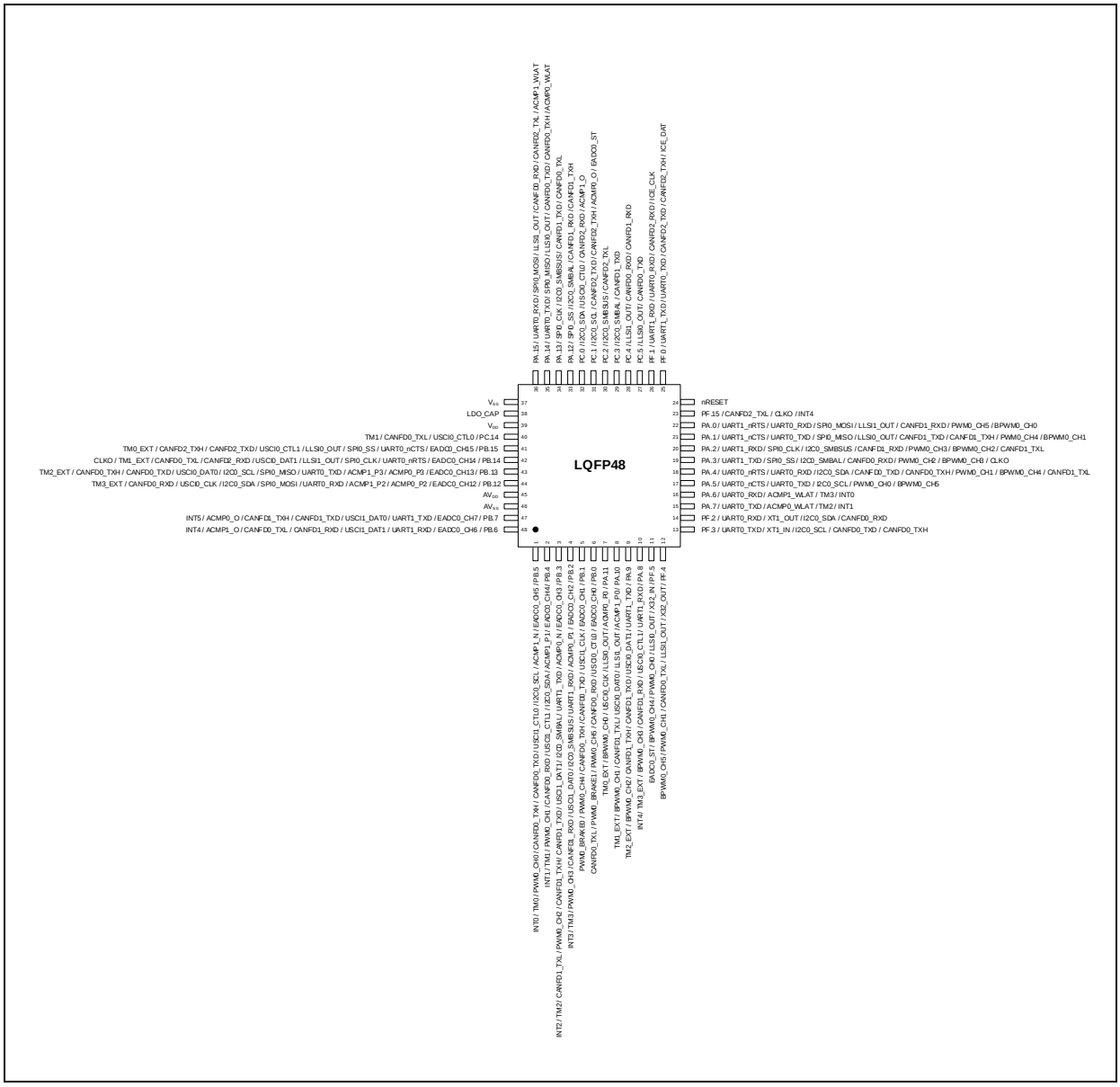


Figure 4.3-5 M2A23LE5AC Multi-function Pin Diagram

Pin	Type	M2A23LE5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0

Pin	Type	M2A23LE5AC Pin Function
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}

Pin	Type	M2A23LE5AC Pin Function
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4

4.3.2.3 M2A23LD5AC

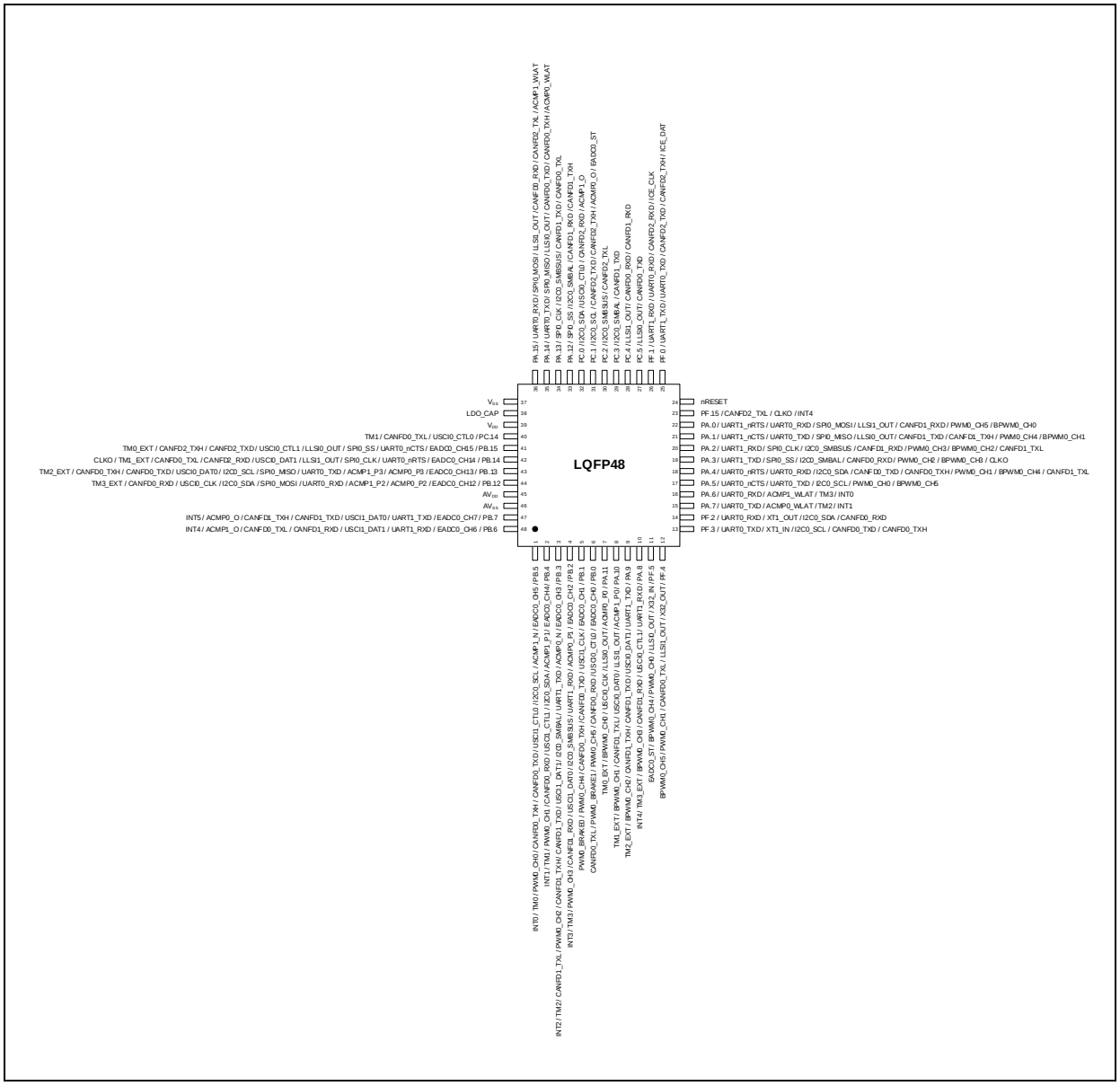


Figure 4.3-6 M2A23LD5AC Multi-function Pin Diagram

Pin	Type	M2A23LD5AC Pin Function
1	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
2	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
3	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
4	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
5	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0

Pin	Type	M2A23LD5AC Pin Function
6	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
7	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
9	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
10	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
12	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
13	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
14	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
15	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
16	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
17	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
18	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
19	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
20	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
21	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
22	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
23	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
26	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
27	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
28	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
29	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
30	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
31	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
32	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
33	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
34	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
35	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
36	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
37	P	V_{SS}

Pin	Type	M2A23LD5AC Pin Function
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
41	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
42	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
43	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
44	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5
48	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4

4.3.3 LQFP 64-Pin Multi-function Pin Diagram

Corresponding Part Number: M2A23SG5AC, M2A23SE5AC, M2A23SD5AC

4.3.3.1 M2A23SG5AC

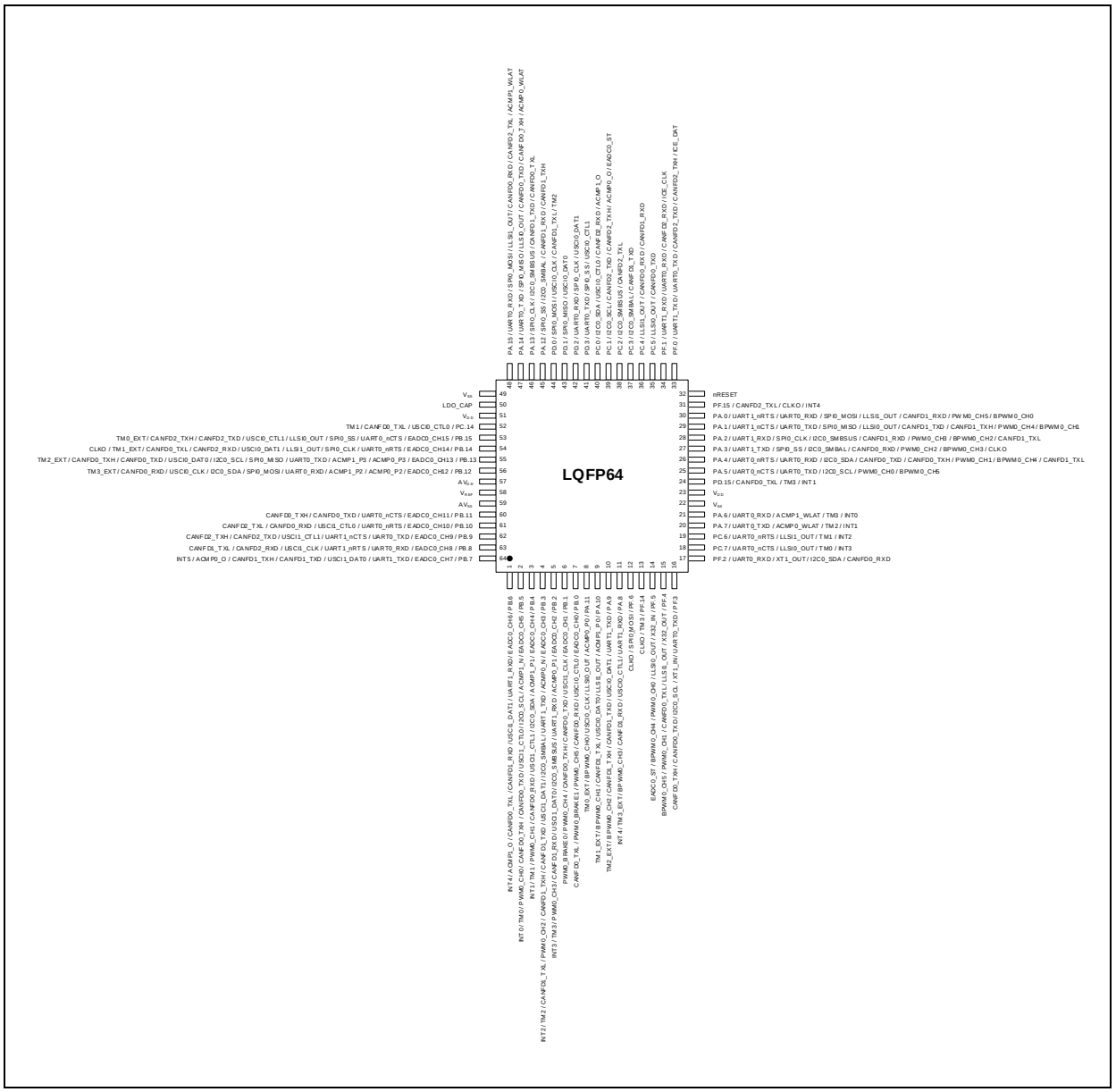


Figure 4.3-7 M2A23SG5AC Multi-function Pin Diagram

Pin	Type	M2A23SG5AC Pin Function
1	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
2	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
3	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1

Pin	Type	M2A23SG5AC Pin Function
4	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
5	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD / PWM0_CH3 / TM3 / INT3
6	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
7	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
8	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	I/O	PF.6 / SPI0_MOSI / CLKO
13	I/O	PF.14 / TM3 / CLKO
14	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
15	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
16	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
17	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
18	I/O	PC.7 / UART0_nCTS / LLSI0_OUT / TM0 / INT3
19	I/O	PC.6 / UART0_nRTS / LLSI1_OUT / TM1 / INT2
20	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / CANFD0_TXL / TM3 / INT1
25	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
26	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
27	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
28	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
29	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
30	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
31	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK

Pin	Type	M2A23SG5AC Pin Function
35	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
36	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD
37	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
38	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
39	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
40	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
41	I/O	PD.3 / UART0_TXD / SPI0_SS / USCI0_CTL1
42	I/O	PD.2 / UART0_RXD / SPI0_CLK / USCI0_DAT1
43	I/O	PD.1 / SPI0_MISO / USCI0_DAT0
44	I/O	PD.0 / SPI0_MOSI / USCI0_CLK / CANFD1_TXL / TM2
45	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
46	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
47	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
48	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
53	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
54	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
55	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
56	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / ADC0_CH11 / UART0_nCTS / CANFD0_TXD / CANFD0_TXH
61	I/O	PB.10 / ADC0_CH10 / UART0_nRTS / USCI1_CTL0 / CANFD0_RXD / CANFD2_TXL
62	I/O	PB.9 / ADC0_CH9 / UART0_TXD / UART1_nCTS / USCI1_CTL1 / CANFD2_TXD / CANFD2_TXH
63	I/O	PB.8 / ADC0_CH8 / UART0_RXD / UART1_nRTS / USCI1_CLK / CANFD2_RXD / CANFD1_TXL
64	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5

4.3.3.2 M2A23SE5AC

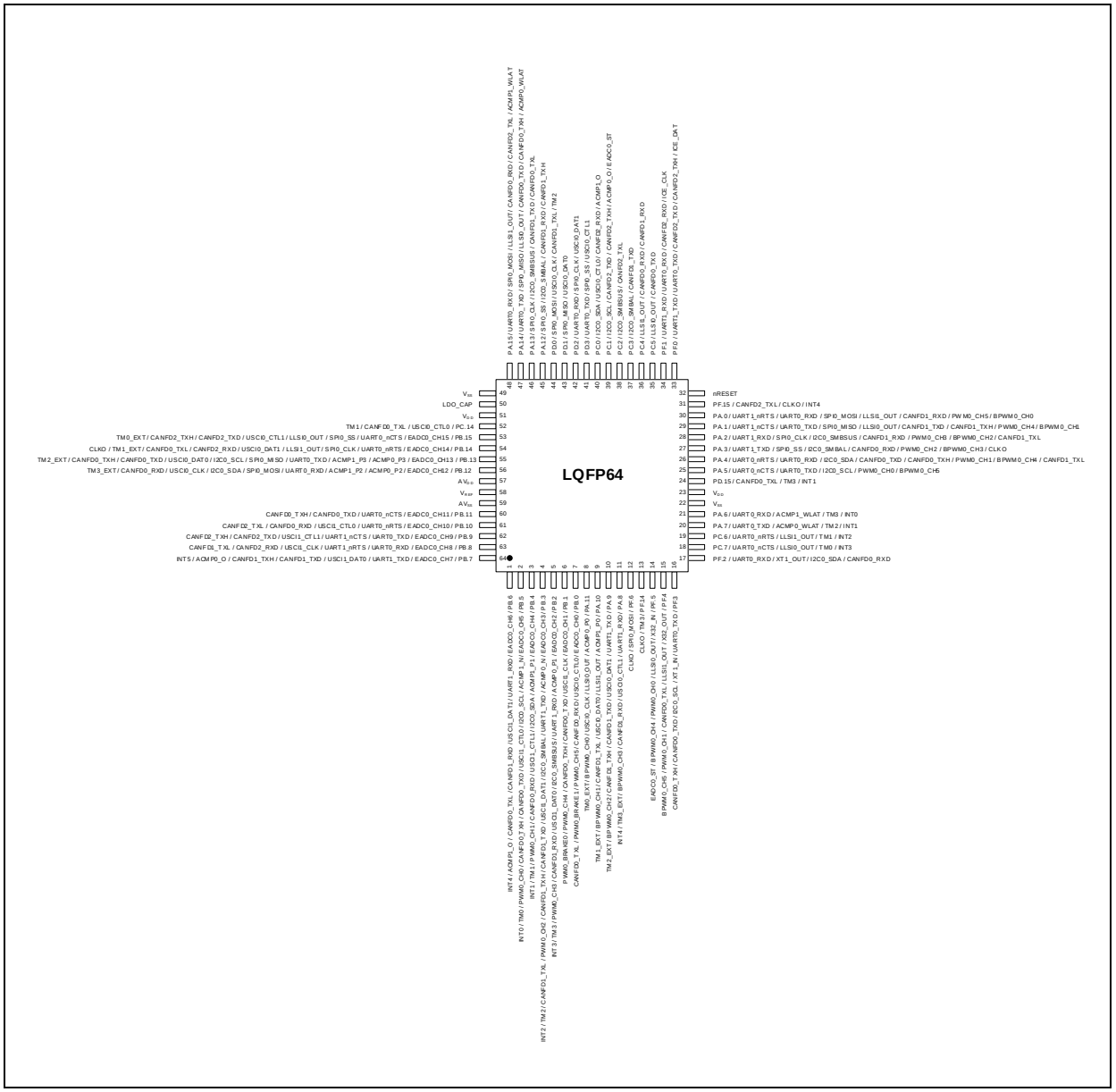


Figure 4.3-8 M2A23SE5AC Multi-function Pin Diagram

Pin	Type	M2A23SE5AC Pin Function
1	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
2	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
3	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
4	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
5	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD /

Pin	Type	M2A23SE5AC Pin Function
		PWM0_CH3 / TM3 / INT3
6	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
7	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
8	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	I/O	PF.6 / SPI0_MOSI / CLKO
13	I/O	PF.14 / TM3 / CLKO
14	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
15	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
16	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
17	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
18	I/O	PC.7 / UART0_nCTS / LLSI0_OUT / TM0 / INT3
19	I/O	PC.6 / UART0_nRTS / LLSI1_OUT / TM1 / INT2
20	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / CANFD0_TXL / TM3 / INT1
25	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
26	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
27	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
28	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
29	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
30	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
31	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
35	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
36	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD

Pin	Type	M2A23SE5AC Pin Function
37	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
38	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
39	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
40	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
41	I/O	PD.3 / UART0_TXD / SPI0_SS / USCI0_CTL1
42	I/O	PD.2 / UART0_RXD / SPI0_CLK / USCI0_DAT1
43	I/O	PD.1 / SPI0_MISO / USCI0_DAT0
44	I/O	PD.0 / SPI0_MOSI / USCI0_CLK / CANFD1_TXL / TM2
45	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
46	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
47	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
48	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
53	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
54	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
55	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
56	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / ADC0_CH11 / UART0_nCTS / CANFD0_TXD / CANFD0_TXH
61	I/O	PB.10 / ADC0_CH10 / UART0_nRTS / USCI1_CTL0 / CANFD0_RXD / CANFD2_TXL
62	I/O	PB.9 / ADC0_CH9 / UART0_TXD / UART1_nCTS / USCI1_CTL1 / CANFD2_TXD / CANFD2_TXH
63	I/O	PB.8 / ADC0_CH8 / UART0_RXD / UART1_nRTS / USCI1_CLK / CANFD2_RXD / CANFD1_TXL
64	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5

4.3.3.3 M2A23SD5AC

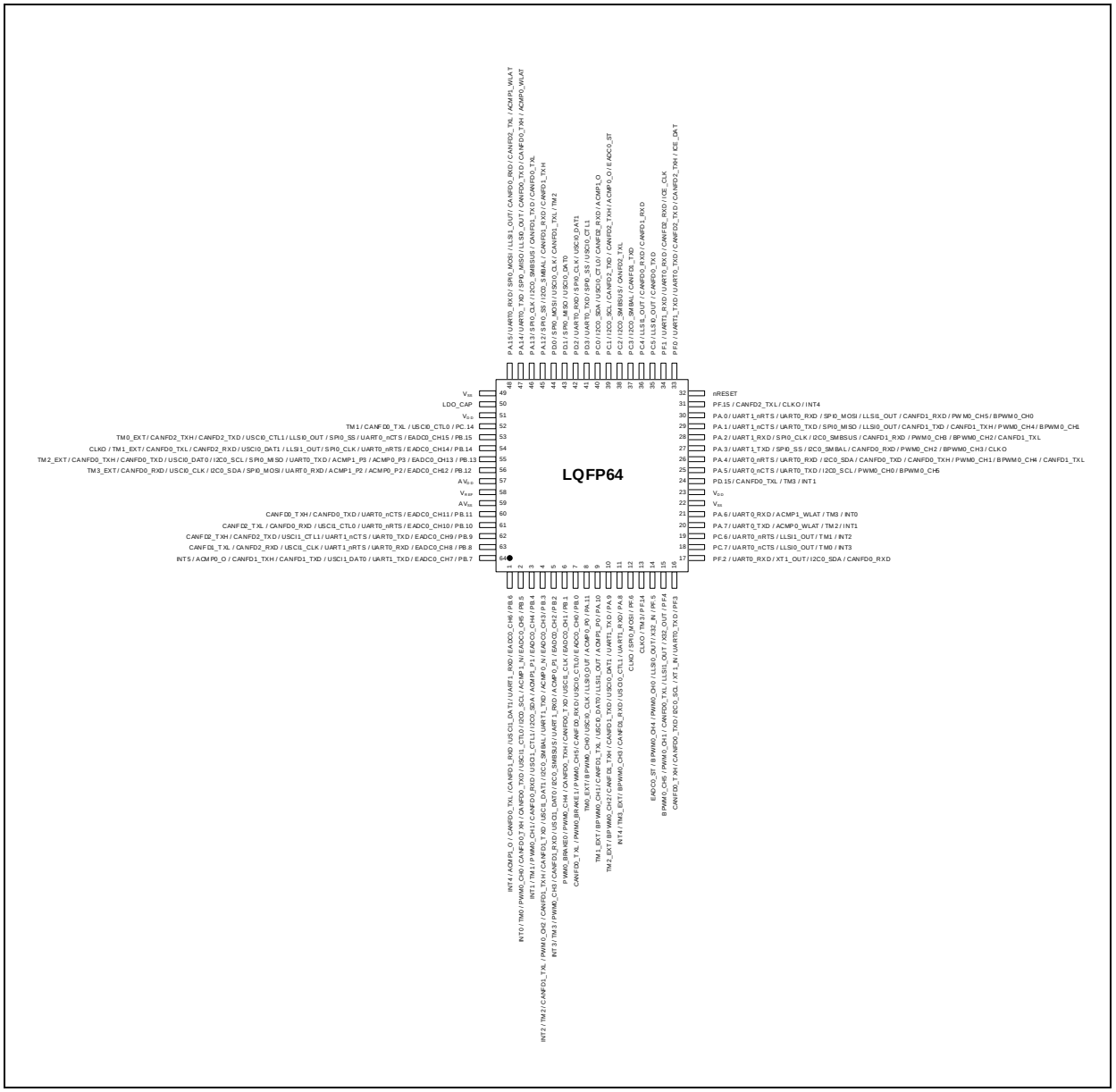


Figure 4.3-9 M2A23SD5AC Multi-function Pin Diagram

Pin	Type	M2A23SD5AC Pin Function
1	I/O	PB.6 / ADC0_CH6 / UART1_RXD / USCI1_DAT1 / CANFD1_RXD / CANFD0_TXL / ACMP1_O / INT4
2	I/O	PB.5 / ADC0_CH5 / ACMP1_N / I2C0_SCL / USCI1_CTL0 / CANFD0_TXD / CANFD0_TXH / PWM0_CH0 / TM0 / INT0
3	I/O	PB.4 / ADC0_CH4 / ACMP1_P1 / I2C0_SDA / USCI1_CTL1 / CANFD0_RXD / PWM0_CH1 / TM1 / INT1
4	I/O	PB.3 / ADC0_CH3 / ACMP0_N / UART1_TXD / I2C0_SMBAL / USCI1_DAT1 / CANFD1_TXD / CANFD1_TXH / PWM0_CH2 / CANFD1_TXL / TM2 / INT2
5	I/O	PB.2 / ADC0_CH2 / ACMP0_P1 / UART1_RXD / I2C0_SMBSUS / USCI1_DAT0 / CANFD1_RXD /

Pin	Type	M2A23SD5AC Pin Function
		PWM0_CH3 / TM3 / INT3
6	I/O	PB.1 / ADC0_CH1 / USCI1_CLK / CANFD0_TXD / CANFD0_TXH / PWM0_CH4 / PWM0_BRAKE0
7	I/O	PB.0 / ADC0_CH0 / USCI0_CTL0 / CANFD0_RXD / PWM0_CH5 / PWM0_BRAKE1 / CANFD0_TXL
8	I/O	PA.11 / ACMP0_P0 / LLSI0_OUT / USCI0_CLK / BPWM0_CH0 / TM0_EXT
9	I/O	PA.10 / ACMP1_P0 / LLSI1_OUT / USCI0_DAT0 / CANFD1_TXL / BPWM0_CH1 / TM1_EXT
10	I/O	PA.9 / UART1_TXD / USCI0_DAT1 / CANFD1_TXD / CANFD1_TXH / BPWM0_CH2 / TM2_EXT
11	I/O	PA.8 / UART1_RXD / USCI0_CTL1 / CANFD1_RXD / BPWM0_CH3 / TM3_EXT / INT4
12	I/O	PF.6 / SPI0_MOSI / CLKO
13	I/O	PF.14 / TM3 / CLKO
14	I/O	PF.5 / X32_IN / LLSI0_OUT / PWM0_CH0 / BPWM0_CH4 / ADC0_ST
15	I/O	PF.4 / X32_OUT / LLSI1_OUT / CANFD0_TXL / PWM0_CH1 / BPWM0_CH5
16	I/O	PF.3 / UART0_TXD / XT1_IN / I2C0_SCL / CANFD0_TXD / CANFD0_TXH
17	I/O	PF.2 / UART0_RXD / XT1_OUT / I2C0_SDA / CANFD0_RXD
18	I/O	PC.7 / UART0_nCTS / LLSI0_OUT / TM0 / INT3
19	I/O	PC.6 / UART0_nRTS / LLSI1_OUT / TM1 / INT2
20	I/O	PA.7 / UART0_TXD / ACMP0_WLAT / TM2 / INT1
21	I/O	PA.6 / UART0_RXD / ACMP1_WLAT / TM3 / INT0
22	P	V_{SS}
23	P	V_{DD}
24	I/O	PD.15 / CANFD0_TXL / TM3 / INT1
25	I/O	PA.5 / UART0_nCTS / UART0_TXD / I2C0_SCL / PWM0_CH0 / BPWM0_CH5
26	I/O	PA.4 / UART0_nRTS / UART0_RXD / I2C0_SDA / CANFD0_TXD / CANFD0_TXH / PWM0_CH1 / BPWM0_CH4 / CANFD1_TXL
27	I/O	PA.3 / UART1_TXD / SPI0_SS / I2C0_SMBAL / CANFD0_RXD / PWM0_CH2 / BPWM0_CH3 / CLKO
28	I/O	PA.2 / UART1_RXD / SPI0_CLK / I2C0_SMBSUS / CANFD1_RXD / PWM0_CH3 / BPWM0_CH2 / CANFD1_TXL
29	I/O	PA.1 / UART1_nCTS / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD1_TXD / CANFD1_TXH / PWM0_CH4 / BPWM0_CH1
30	I/O	PA.0 / UART1_nRTS / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD1_RXD / PWM0_CH5 / BPWM0_CH0
31	I/O	PF.15 / CANFD2_TXL / CLKO / INT4
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / UART0_TXD / CANFD2_TXD / CANFD2_TXH / ICE_DAT
34	I/O	PF.1 / UART1_RXD / UART0_RXD / CANFD2_RXD / ICE_CLK
35	I/O	PC.5 / LLSI0_OUT / CANFD0_TXD
36	I/O	PC.4 / LLSI1_OUT / CANFD0_RXD / CANFD1_RXD

Pin	Type	M2A23SD5AC Pin Function
37	I/O	PC.3 / I2C0_SMBAL / CANFD1_TXD
38	I/O	PC.2 / I2C0_SMBSUS / CANFD2_TXL
39	I/O	PC.1 / I2C0_SCL / CANFD2_TXD / CANFD2_TXH / ACMP0_O / ADC0_ST
40	I/O	PC.0 / I2C0_SDA / USCI0_CTL0 / CANFD2_RXD / ACMP1_O
41	I/O	PD.3 / UART0_TXD / SPI0_SS / USCI0_CTL1
42	I/O	PD.2 / UART0_RXD / SPI0_CLK / USCI0_DAT1
43	I/O	PD.1 / SPI0_MISO / USCI0_DAT0
44	I/O	PD.0 / SPI0_MOSI / USCI0_CLK / CANFD1_TXL / TM2
45	I/O	PA.12 / SPI0_SS / I2C0_SMBAL / CANFD1_RXD / CANFD1_TXH
46	I/O	PA.13 / SPI0_CLK / I2C0_SMBSUS / CANFD1_TXD / CANFD0_TXL
47	I/O	PA.14 / UART0_TXD / SPI0_MISO / LLSI0_OUT / CANFD0_TXD / CANFD0_TXH / ACMP0_WLAT
48	I/O	PA.15 / UART0_RXD / SPI0_MOSI / LLSI1_OUT / CANFD0_RXD / CANFD2_TXL / ACMP1_WLAT
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / USCI0_CTL0 / CANFD0_TXL / TM1
53	I/O	PB.15 / ADC0_CH15 / UART0_nCTS / SPI0_SS / LLSI0_OUT / USCI0_CTL1 / CANFD2_TXD / CANFD2_TXH / TM0_EXT
54	I/O	PB.14 / ADC0_CH14 / UART0_nRTS / SPI0_CLK / LLSI1_OUT / USCI0_DAT1 / CANFD2_RXD / CANFD0_TXL / TM1_EXT / CLKO
55	I/O	PB.13 / ADC0_CH13 / ACMP0_P3 / ACMP1_P3 / UART0_TXD / SPI0_MISO / I2C0_SCL / USCI0_DAT0 / CANFD0_TXD / CANFD0_TXH / TM2_EXT
56	I/O	PB.12 / ADC0_CH12 / ACMP0_P2 / ACMP1_P2 / UART0_RXD / SPI0_MOSI / I2C0_SDA / USCI0_CLK / CANFD0_RXD / TM3_EXT
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / ADC0_CH11 / UART0_nCTS / CANFD0_TXD / CANFD0_TXH
61	I/O	PB.10 / ADC0_CH10 / UART0_nRTS / USCI1_CTL0 / CANFD0_RXD / CANFD2_TXL
62	I/O	PB.9 / ADC0_CH9 / UART0_TXD / UART1_nCTS / USCI1_CTL1 / CANFD2_TXD / CANFD2_TXH
63	I/O	PB.8 / ADC0_CH8 / UART0_RXD / UART1_nRTS / USCI1_CLK / CANFD2_RXD / CANFD1_TXL
64	I/O	PB.7 / ADC0_CH7 / UART1_TXD / USCI1_DAT0 / CANFD1_TXD / CANFD1_TXH / ACMP0_O / INT5

4.4 Pin Mapping

Different part number with same package might has different function. Please refer to the selection guide in section 3.1, Pin Configuration in section 4.2 or NuTool - PinConfig.

Corresponding Part Number: M2A23YG5AC, M2A23YE5AC, M2A23YD5AC, M2A23LG5AC, M2A23LE5AC, M2A23LD5AC, M2A23SG5AC, M2A23SE5AC, M2A23SD5AC

	M2A23 Series		
Pin Name	M2A23Yx5AC	M2A23Lx5AC	M2A23Sx5AC
PB.5	1	1	2
PB.4	2	2	3
PB.3	3	3	4
PB.2	4	4	5
PB.1	5	5	6
PB.0	6	6	7
PA.11	7	7	8
PA.10	8	8	9
PA.9	9	9	10
PA.8	10	10	11
PF.6			12
PF.14			13
PF.5	11	11	14
PF.4	12	12	15
PF.3	13	13	16
PF.2	14	14	17
PC.7			18
PC.6			19
PA.7	15	15	20
PA.6	16	16	21
V_{SS}			22
V_{DD}			23
PD.15			24
PA.5	17	17	25
PA.4	18	18	26
PA.3	19	19	27
PA.2	20	20	28
PA.1	21	21	29

PA.0	22	22	30
PF.15	23	23	31
nRESET	24	24	32
PF.0	25	25	33
PF.1	26	26	34
PC.5	27	27	35
PC.4	28	28	36
PC.3	29	29	37
PC.2	30	30	38
PC.1	31	31	39
PC.0	32	32	40
PD.3			41
PD.2			42
PD.1			43
PD.0			44
PA.12	33	33	45
PA.13	34	34	46
PA.14	35	35	47
PA.15	36	36	48
V_{SS}	37	37	49
LDO_CAP	38	38	50
V_{DD}	39	39	51
PC.14	40	40	52
PB.15	41	41	53
PB.14	42	42	54
PB.13	43	43	55
PB.12	44	44	56
AV_{DD}	45	45	57
V_{REF}			58
AV_{SS}	46	46	59
PB.11			60
PB.10			61
PB.9			62
PB.8			63

PB.7	47	47	64
PB.6	48	48	1
V_{SS}	49		

4.5 Pin Functional Description

4.5.1 Multi-function Summary Table

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH6	A	ADC0 channel 6 analog input.
	ADC0_CH7	A	ADC0 channel 7 analog input.
	ADC0_CH8	A	ADC0 channel 8 analog input.
	ADC0_CH9	A	ADC0 channel 9 analog input.
	ADC0_CH10	A	ADC0 channel 10 analog input.
	ADC0_CH11	A	ADC0 channel 11 analog input.
	ADC0_CH12	A	ADC0 channel 12 analog input.
	ADC0_CH13	A	ADC0 channel 13 analog input.
	ADC0_CH14	A	ADC0 channel 14 analog input.
	ADC0_CH15	A	ADC0 channel 15 analog input.
	ADC0_ST	I	ADC0 external trigger input pin.

Group	Pin Name	Type	Description
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
CANFD0	CANFD0_RXD	I	CANF bus receiver input.
	CANFD0_TXD	O	CANF bus transmitter output.
	CANFD0_TXH	O	CAN0 bus transmitter high level line digital output.
	CANFD0_TXL	O	CAN0 bus transmitter low level line digital output.
CANFD1	CANFD1_RXD	I	CANF bus receiver input.
	CANFD1_TXD	O	CANF bus transmitter output.
	CANFD1_TXH	O	CAN1 bus transmitter high level line digital output.
	CANFD1_TXL	O	CAN1 bus transmitter low level line digital output.
CANFD2	CANFD2_RXD	I	CANF bus receiver input.
	CANFD2_TXD	O	CANF bus transmitter output.
	CANFD2_TXH	O	CAN2 bus transmitter high level line digital output.
	CANFD2_TXL	O	CAN2 bus transmitter low level line digital output.
CLKO	CLKO	O	Clock Out
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.

Group	Pin Name	Type	Description
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_ST	I	EADC0 external trigger input.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
LLSI0	LLSI0_OUT	O	LED Lighting Strip Interface 0 output pin.
LLSI1	LLSI1_OUT	O	LED Lighting Strip Interface 1 output pin.
PWM0	PWM0_BRAKE0	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE1	I	PWM0 Brake 1 input pin.
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	I/O	USCI1 clock pin.
	USCI1_CTL0	I/O	USCI1 control 0 pin.
	USCI1_CTL1	I/O	USCI1 control 1 pin.
	USCI1_DAT0	I/O	USCI1 data 0 pin.
	USCI1_DAT1	I/O	USCI1 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	LDO_CAP	A	LDO output pin. Note: This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital

Group	Pin Name	Type	Description
			circuit.
	V_{REF}	A	ADC reference voltage input. Note: This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. Note: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
	EPAD	P	Exposed pad served as ground pin (V_{SS}).

4.5.2 Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_nRTS	O	MFP2	UART1 request to Send output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH5	I/O	MFP11	PWM0 channel 5 output/capture input.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_nCTS	I	MFP2	UART1 clear to Send input pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	CANFD1_TXD	O	MFP9	CANF bus transmitter output.
	CANFD1_TXH	O	MFP10	CAN1 bus transmitter high level line digital output.
	PWM0_CH4	I/O	MFP11	PWM0 channel 4 output/capture input.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	I2C0_SMBSUS	O	MFP6	I^2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH3	I/O	MFP11	PWM0 channel 3 output/capture input.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	CANFD1_TXL	O	MFP13	CAN1 bus transmitter low level line digital output.
PA.3	PA.3	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	I2C0_SMBAL	O	MFP6	I^2C0 SMBus SMBALTER pin.

	Pin Name	Type	MFP	Description
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH2	I/O	MFP11	PWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	CLKO	O	MFP15	Clock Out.
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
	PWM0_CH1	I/O	MFP11	PWM0 channel 1 output/capture input.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	CANFD1_TXL	O	MFP13	CAN1 bus transmitter low level line digital output.
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	UART0_nCTS	I	MFP2	UART0 clear to Send input pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
	PWM0_CH0	I/O	MFP11	PWM0 channel 0 output/capture input.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
PA.6	PA.6	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PA.7	PA.7	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PA.8	PA.8	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.

	Pin Name	Type	MFP	Description
	USCI0_CTL1	I/O	MFP8	USCI0 control 1 pin.
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	BPWM0_CH3	I/O	MFP12	BPWM0 channel 3 output/capture input.
	TM3_EXT	I/O	MFP14	Timer3 external capture input/toggle output pin.
	INT4	I	MFP15	External interrupt 4 input pin.
PA.9	PA.9	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
	CANFD1_TXD	O	MFP9	CANF bus transmitter output.
	CANFD1_TXH	O	MFP10	CAN1 bus transmitter high level line digital output.
	BPWM0_CH2	I/O	MFP12	BPWM0 channel 2 output/capture input.
	TM2_EXT	I/O	MFP14	Timer2 external capture input/toggle output pin.
PA.10	PA.10	I/O	MFP0	General purpose digital I/O pin.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
	CANFD1_TXL	O	MFP10	CAN1 bus transmitter low level line digital output.
	BPWM0_CH1	I/O	MFP12	BPWM0 channel 1 output/capture input.
	TM1_EXT	I/O	MFP14	Timer1 external capture input/toggle output pin.
PA.11	PA.11	I/O	MFP0	General purpose digital I/O pin.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	USCI0_CLK	I/O	MFP8	USCI0 clock pin.
	BPWM0_CH0	I/O	MFP12	BPWM0 channel 0 output/capture input.
	TM0_EXT	I/O	MFP14	Timer0 external capture input/toggle output pin.
PA.12	PA.12	I/O	MFP0	General purpose digital I/O pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	I2C0_SMBAL	O	MFP6	I^2C0 SMBus SMBALTER pin.
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	CANFD1_TXH	O	MFP10	CAN1 bus transmitter high level line digital output.

	Pin Name	Type	MFP	Description
PA.13	PA.13	I/O	MFP0	General purpose digital I/O pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	I2C0_SMBSUS	O	MFP6	I²C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	CANFD1_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXL	O	MFP11	CAN0 bus transmitter low level line digital output.
PA.14	PA.14	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
	ACMP0_WLAT	I	MFP13	Analog comparator 0 window latch input pin
PA.15	PA.15	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	CANFD2_TXL	O	MFP11	CAN2 bus transmitter low level line digital output.
	ACMP1_WLAT	I	MFP13	Analog comparator 1 window latch input pin
PB.0	PB.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	USCI0_CTL0	I/O	MFP8	USCI0 control 0 pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH5	I/O	MFP11	PWM0 channel 5 output/capture input.
	PWM0_BRAKE1	I	MFP12	PWM0 Brake 1 input pin.
	CANFD0_TXL	O	MFP13	CAN0 bus transmitter low level line digital output.
PB.1	PB.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	USCI1_CLK	I/O	MFP8	USCI1 clock pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.

	Pin Name	Type	MFP	Description
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
	PWM0_CH4	I/O	MFP11	PWM0 channel 4 output/capture input.
	PWM0_BRAKE0	I	MFP12	PWM0 Brake 0 input pin.
PB.2	PB.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	ACMP0_P1	A	MFP1	Analog comparator 0 positive input 1 pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	I2C0_SMBSUS	O	MFP6	I^2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	USCI1_DAT0	I/O	MFP8	USCI1 data 0 pin.
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH3	I/O	MFP11	PWM0 channel 3 output/capture input.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PB.3	PB.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	ACMP0_N	A	MFP1	Analog comparator 0 negative input pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	I2C0_SMBAL	O	MFP6	I^2C0 SMBus SMBALTER pin.
	USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
	CANFD1_TXD	O	MFP9	CANF bus transmitter output.
	CANFD1_TXH	O	MFP10	CAN1 bus transmitter high level line digital output.
	PWM0_CH2	I/O	MFP11	PWM0 channel 2 output/capture input.
	CANFD1_TXL	O	MFP13	CAN1 bus transmitter low level line digital output.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	ACMP1_P1	A	MFP1	Analog comparator 1 positive input 1 pin.
	I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.

	Pin Name	Type	MFP	Description
	USCI1_CTL1	I/O	MFP8	USCI1 control 1 pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	PWM0_CH1	I/O	MFP11	PWM0 channel 1 output/capture input.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
	ACMP1_N	A	MFP1	Analog comparator 1 negative input pin.
	I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
	USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
	PWM0_CH0	I/O	MFP11	PWM0 channel 0 output/capture input.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT0	I	MFP15	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
	UART1_RXD	I	MFP3	UART1 data receiver input pin.
	USCI1_DAT1	I/O	MFP8	USCI1 data 1 pin.
	CANFD1_RXD	I	MFP9	CANF bus receiver input.
	CANFD0_TXL	O	MFP11	CAN0 bus transmitter low level line digital output.
	ACMP1_O	O	MFP13	Analog comparator 1 output pin.
	INT4	I	MFP14	External interrupt 4 input pin.
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	UART1_TXD	O	MFP3	UART1 data transmitter output pin.
	USCI1_DAT0	I/O	MFP8	USCI1 data 0 pin.
	CANFD1_TXD	O	MFP9	CANF bus transmitter output.
	CANFD1_TXH	O	MFP10	CAN1 bus transmitter high level line digital output.
	ACMP0_O	O	MFP13	Analog comparator 0 output pin.

	Pin Name	Type	MFP	Description
	INT5	I	MFP14	External interrupt 5 input pin.
PB.8	PB.8	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	UART1_nRTS	O	MFP3	UART1 request to Send output pin.
	USCI1_CLK	I/O	MFP8	USCI1 clock pin.
	CANFD2_RXD	I	MFP9	CANF bus receiver input.
	CANFD1_TXL	O	MFP11	CAN1 bus transmitter low level line digital output.
PB.9	PB.9	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	UART1_nCTS	I	MFP3	UART1 clear to Send input pin.
	USCI1_CTL1	I/O	MFP8	USCI1 control 1 pin.
	CANFD2_TXD	O	MFP9	CANF bus transmitter output.
	CANFD2_TXH	O	MFP10	CAN2 bus transmitter high level line digital output.
PB.10	PB.10	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	USCI1_CTL0	I/O	MFP8	USCI1 control 0 pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	CANFD2_TXL	O	MFP11	CAN2 bus transmitter low level line digital output.
PB.11	PB.11	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	UART0_nCTS	I	MFP2	UART0 clear to Send input pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
PB.12	PB.12	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
	ACMP0_P2	A	MFP1	Analog comparator 0 positive input 2 pin.
	ACMP1_P2	A	MFP1	Analog comparator 1 positive input 2 pin.

	Pin Name	Type	MFP	Description
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	I2C0_SDA	I/O	MFP6	I²C0 data input/output pin.
	USCI0_CLK	I/O	MFP8	USCI0 clock pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	TM3_EXT	I/O	MFP14	Timer3 external capture input/toggle output pin.
PB.13	PB.13	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
	ACMP0_P3	A	MFP1	Analog comparator 0 positive input 3 pin.
	ACMP1_P3	A	MFP1	Analog comparator 1 positive input 3 pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	I2C0_SCL	I/O	MFP6	I²C0 clock pin.
	USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
	TM2_EXT	I/O	MFP14	Timer2 external capture input/toggle output pin.
PB.14	PB.14	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
	CANFD2_RXD	I	MFP9	CANF bus receiver input.
	CANFD0_TXL	O	MFP11	CAN0 bus transmitter low level line digital output.
	TM1_EXT	I/O	MFP14	Timer1 external capture input/toggle output pin.
	CLKO	O	MFP15	Clock Out.
PB.15	PB.15	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
	UART0_nCTS	I	MFP2	UART0 clear to Send input pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.

	Pin Name	Type	MFP	Description
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	USCI0_CTL1	I/O	MFP8	USCI0 control 1 pin.
	CANFD2_TXD	O	MFP9	CANF bus transmitter output.
	CANFD2_TXH	O	MFP10	CAN2 bus transmitter high level line digital output.
	TM0_EXT	I/O	MFP14	Timer0 external capture input/toggle output pin.
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.
	USCI0_CTL0	I/O	MFP8	USCI0 control 0 pin.
	CANFD2_RXD	I	MFP9	CANF bus receiver input.
	ACMP1_O	O	MFP13	Analog comparator 1 output pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
	CANFD2_TXD	O	MFP9	CANF bus transmitter output.
	CANFD2_TXH	O	MFP10	CAN2 bus transmitter high level line digital output.
	ACMP0_O	O	MFP13	Analog comparator 0 output pin.
	ADC0_ST	I	MFP15	ADC0 external trigger input pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SMBSUS	O	MFP6	I^2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
	CANFD2_TXL	O	MFP11	CAN2 bus transmitter low level line digital output.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	I2C0_SMBAL	O	MFP6	I^2C0 SMBus SMBALTER pin.
	CANFD1_TXD	O	MFP10	CANF bus transmitter output.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
	CANFD1_RXD	I	MFP10	CANF bus receiver input.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.

	Pin Name	Type	MFP	Description
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
	INT2	I	MFP15	External interrupt 2 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	UART0_nCTS	I	MFP2	UART0 clear to Send input pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	TM0	I/O	MFP14	Timer0 event counter input/toggle output pin.
	INT3	I	MFP15	External interrupt 3 input pin.
PC.14	PC.14	I/O	MFP0	General purpose digital I/O pin.
	USCI0_CTL0	I/O	MFP8	USCI0 control 0 pin.
	CANFD0_TXL	O	MFP11	CAN0 bus transmitter low level line digital output.
	TM1	I/O	MFP14	Timer1 event counter input/toggle output pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	USCI0_CLK	I/O	MFP8	USCI0 clock pin.
	CANFD1_TXL	O	MFP11	CAN1 bus transmitter low level line digital output.
	TM2	I/O	MFP14	Timer2 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MISO	I/O	MFP4	SPI0 MISO (Master In, Slave Out) pin.
	USCI0_DAT0	I/O	MFP8	USCI0 data 0 pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	SPI0_CLK	I/O	MFP4	SPI0 serial clock pin.
	USCI0_DAT1	I/O	MFP8	USCI0 data 1 pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	SPI0_SS	I/O	MFP4	SPI0 slave select pin.
	USCI0_CTL1	I/O	MFP8	USCI0 control 1 pin.
PD.15	PD.15	I/O	MFP0	General purpose digital I/O pin.

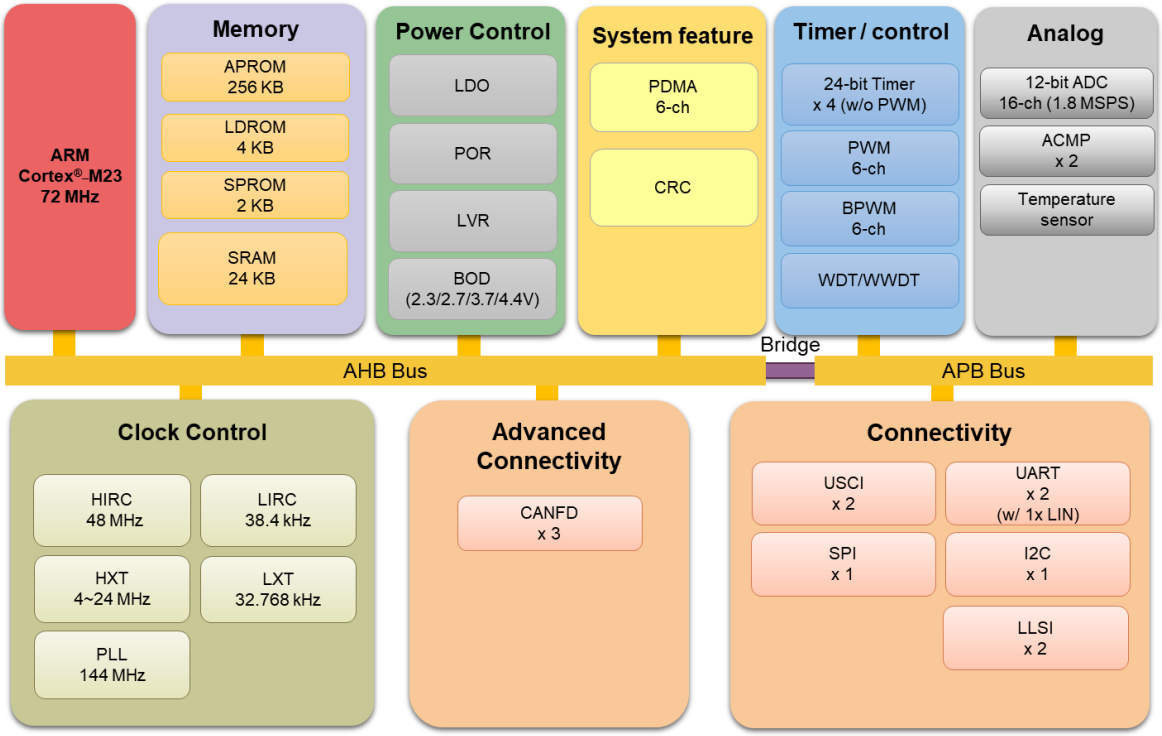
	Pin Name	Type	MFP	Description
	CANFD0_TXL	O	MFP11	CAN0 bus transmitter low level line digital output.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	INT1	I	MFP15	External interrupt 1 input pin.
PF.0	PF.0	I/O	MFP0	General purpose digital I/O pin.
	UART1_TXD	O	MFP2	UART1 data transmitter output pin.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	CANFD2_TXD	O	MFP9	CANF bus transmitter output.
	CANFD2_TXH	O	MFP10	CAN2 bus transmitter high level line digital output.
	ICE_DAT	I/O	MFP14	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
PF.1	PF.1	I/O	MFP0	General purpose digital I/O pin.
	UART1_RXD	I	MFP2	UART1 data receiver input pin.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	CANFD2_RXD	I	MFP9	CANF bus receiver input.
	ICE_CLK	I	MFP14	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
PF.2	PF.2	I/O	MFP0	General purpose digital I/O pin.
	UART0_RXD	I	MFP2	UART0 data receiver input pin.
	XT1_OUT	O	MFP3	External 4~24 MHz (high speed) crystal output pin.
	I2C0_SDA	I/O	MFP6	I^2C0 data input/output pin.
	CANFD0_RXD	I	MFP9	CANF bus receiver input.
PF.3	PF.3	I/O	MFP0	General purpose digital I/O pin.
	UART0_TXD	O	MFP2	UART0 data transmitter output pin.
	XT1_IN	I	MFP3	External 4~24 MHz (high speed) crystal input pin.
	I2C0_SCL	I/O	MFP6	I^2C0 clock pin.
	CANFD0_TXD	O	MFP9	CANF bus transmitter output.
	CANFD0_TXH	O	MFP10	CAN0 bus transmitter high level line digital output.
PF.4	PF.4	I/O	MFP0	General purpose digital I/O pin.
	X32_OUT	O	MFP3	External 32.768 kHz crystal output pin.

	Pin Name	Type	MFP	Description
	LLSI1_OUT	O	MFP7	LED Lighting Strip Interface 1 output pin.
	CANFD0_TXL	O	MFP10	CAN0 bus transmitter low level line digital output.
	PWM0_CH1	I/O	MFP11	PWM0 channel 1 output/capture input.
	BPWM0_CH5	I/O	MFP12	BPWM0 channel 5 output/capture input.
PF.5	PF.5	I/O	MFP0	General purpose digital I/O pin.
	X32_IN	I	MFP3	External 32.768 kHz crystal input pin.
	LLSI0_OUT	O	MFP7	LED Lighting Strip Interface 0 output pin.
	PWM0_CH0	I/O	MFP11	PWM0 channel 0 output/capture input.
	BPWM0_CH4	I/O	MFP12	BPWM0 channel 4 output/capture input.
	ADC0_ST	I	MFP15	ADC0 external trigger input pin.
PF.6	PF.6	I/O	MFP0	General purpose digital I/O pin.
	SPI0_MOSI	I/O	MFP4	SPI0 MOSI (Master Out, Slave In) pin.
	CLKO	O	MFP15	Clock Out.
PF.14	PF.14	I/O	MFP0	General purpose digital I/O pin.
	TM3	I/O	MFP14	Timer3 event counter input/toggle output pin.
	CLKO	O	MFP15	Clock Out.
PF.15	PF.15	I/O	MFP0	General purpose digital I/O pin.
	CANFD2_TXL	O	MFP11	CAN2 bus transmitter low level line digital output.
	CLKO	O	MFP14	Clock Out.
	INT4	I	MFP15	External interrupt 4 input pin.

Table 4.5-1 M2A23 GPIO Multi-function Table

5 BLOCK DIAGRAM

5.1 M2A23 Series Block Diagram



Please refer to the selection guide in section 3.3 for detailed information.

Figure 5.1-1 NuMicro M2A23 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm Cortex-M23 Core

The Cortex-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm TrustZone technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro M2A23 is embedded with Cortex-M23 processor. Figure 4.2-3 shows the functional controller of the processor.

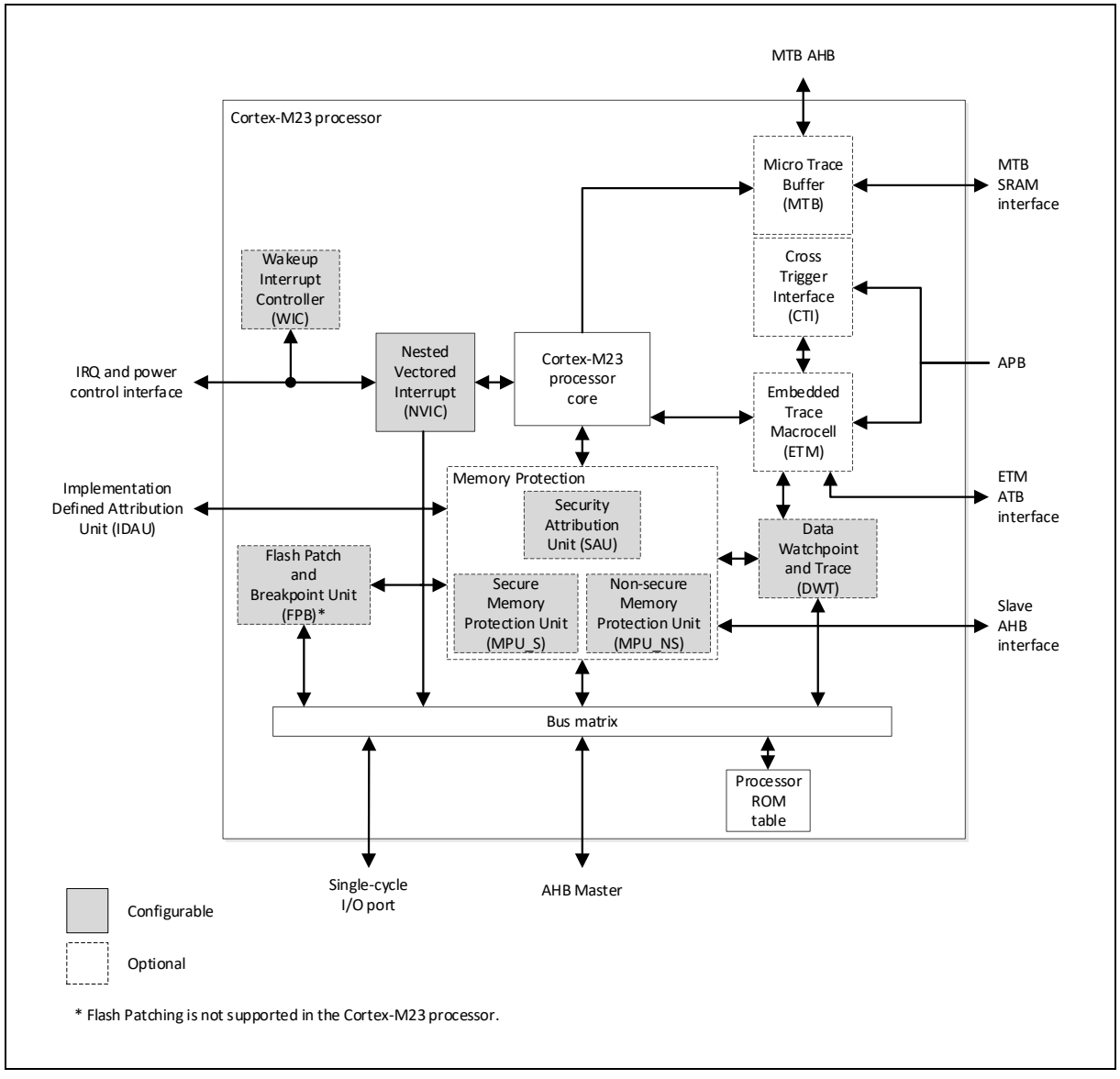


Figure 6.1-1 Cortex-M23 Block Diagram

Cortex-M23 processor features:

- Armv8-M Baseline architecture.
- Armv8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.

- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash Memory and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - System Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core and Flash Memory Controller (FMC) by writing 1 to CPURST (SYS_IPRST0[1])
  - nRESET glitch filter time 32us

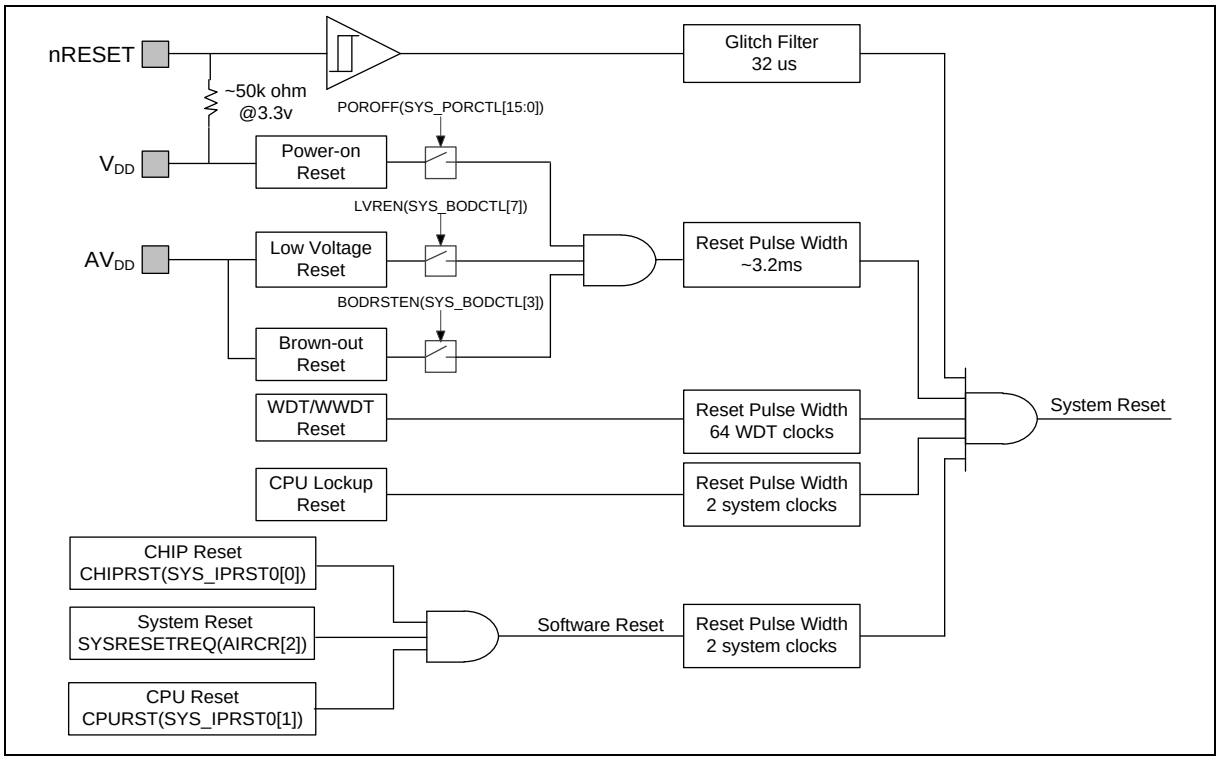


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M23 only; the other reset sources will reset Cortex-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	System	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[17:16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-

HCLKSEL (CLK_CLKSEL0[2:0])	0x7	0x7	0x7	0x7	0x7	0x7	0x7	0x7	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	0x0000	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
PGFF (FMC_ISPSTS[5])	0x0	-	-	-	-	-	-	-	-
VECMAP (FMC_ISPSTS[29:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
FBS (FMC_ISPSTS[30])	0x0	-	-	-	-	-	-	-	-
SCODE (FMC_ISPSTS[31])	Reload base on the last byte of	Reload base on the last byte of	Reload base on the last byte of	Reload base on the last byte of	Reload base on the last byte of	-	Reload base on the last byte of	-	-

	SPROM	SPROM	SPROM	SPROM	SPROM		SPROM		
FMC_APWPROT0	Reload base on CONFIG8	Reload base on CONFIG8	Reload base on CONFIG8	Reload base on CONFIG8	Reload base on CONFIG8	-	Reload base on CONFIG8	-	-
FMC_APWPKEEP (CONFIG10≠0xFFFF)	0x55AA	0x55AA	0x55AA	0x55AA	0x55AA	0x55AA	0x55AA	0x55AA	0x55AA
FMC_APWPKEEP (CONFIG10 = 0xFFFF)	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than V_{ILR} and the state keeps longer than t_{FR} (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above V_{IHR} and the state keeps longer than t_{FR} (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

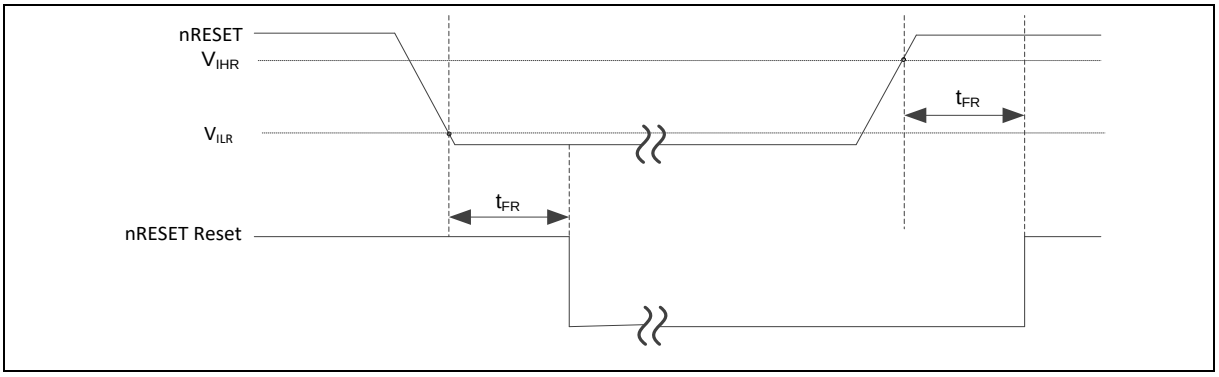


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

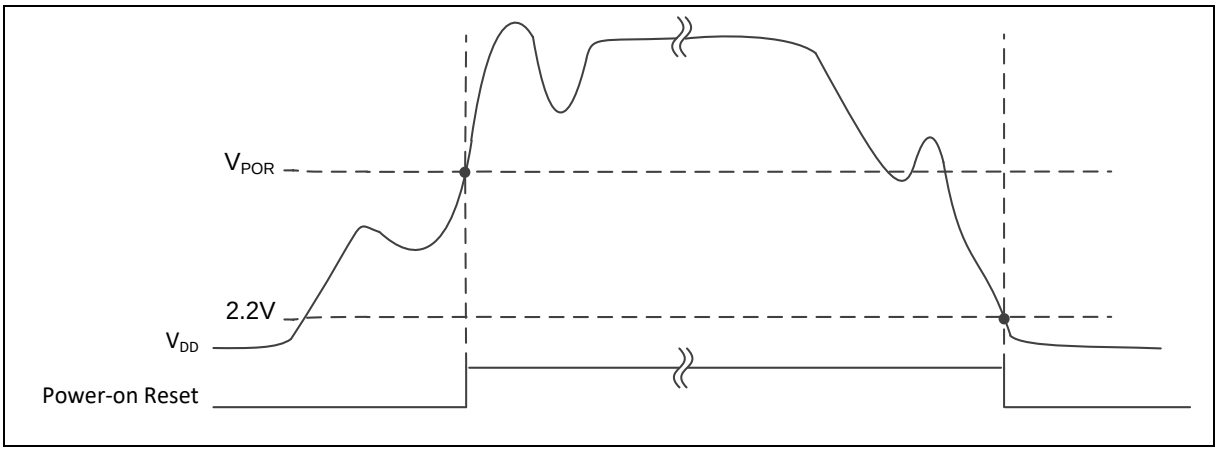


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

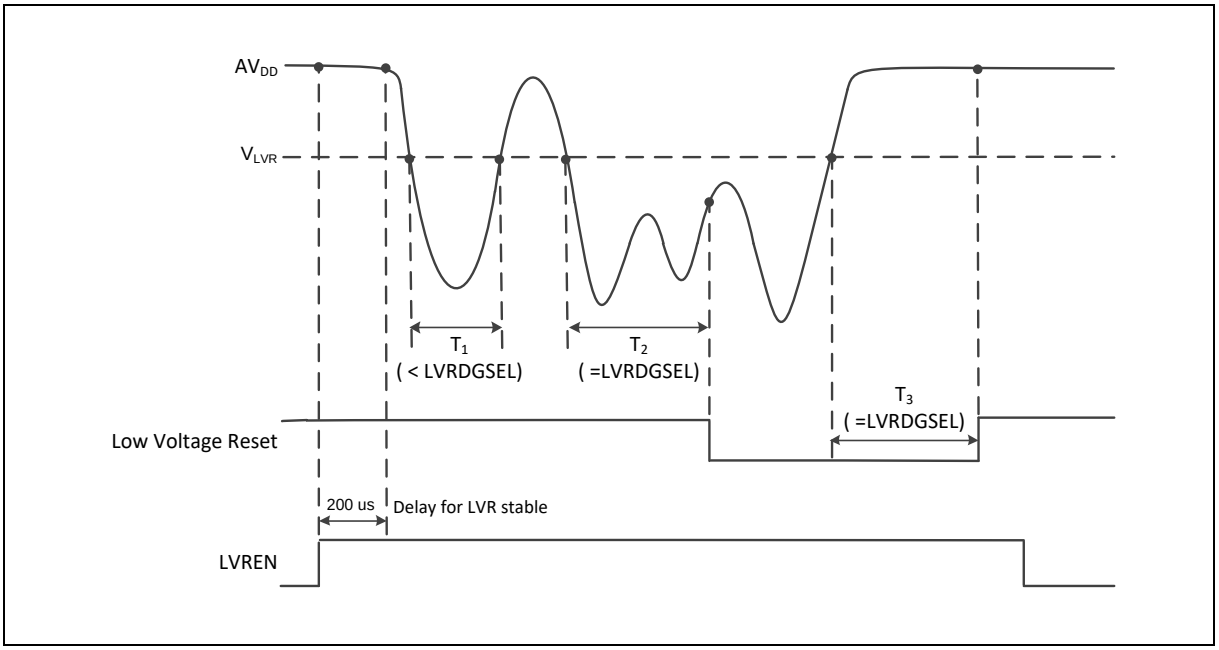


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[17:16]) and the state keeps longer than De-glitch time set by BODDGSEL

(SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [22:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

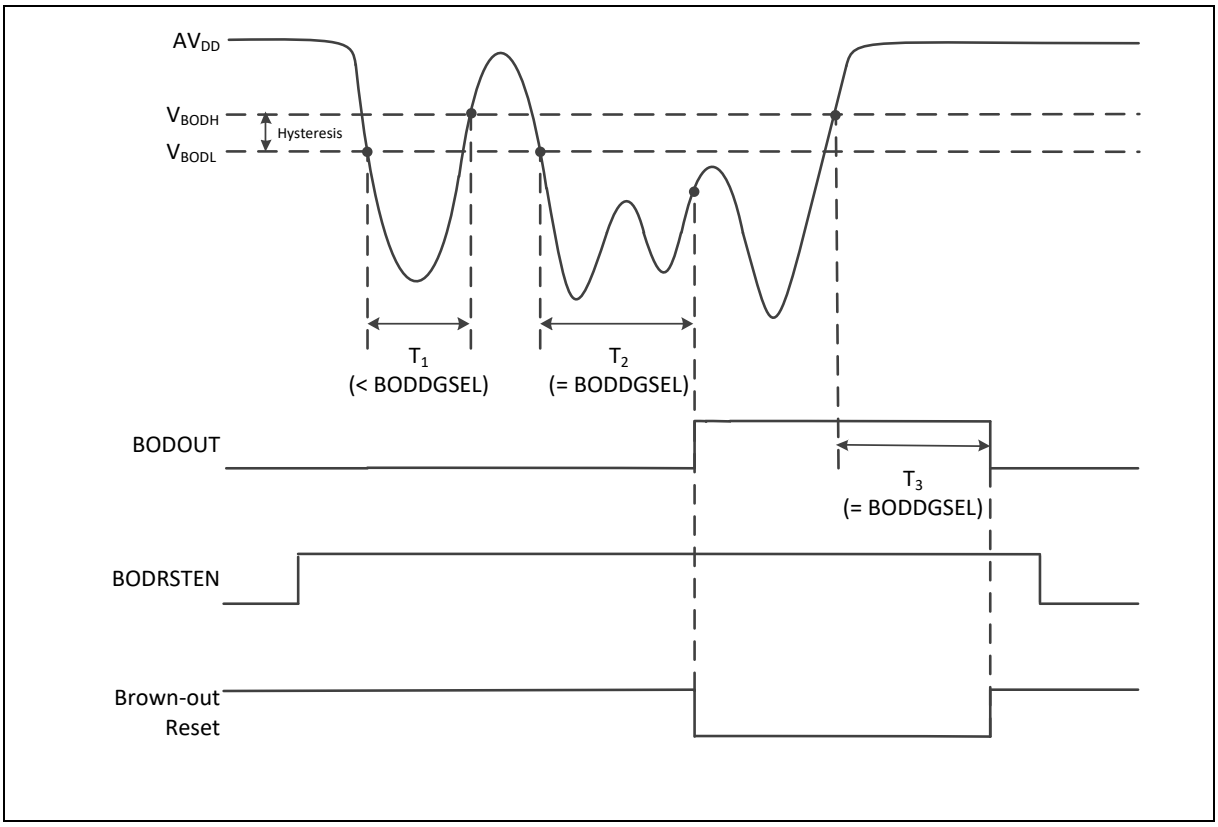


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and System Reset

The CPU Reset means Cortex-M23 core and Flash Memory Controller (FMC) are reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1

to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The System Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the System Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO_CAP and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Figure 6.2-6 shows the NuMicro M2A23 power distribution.

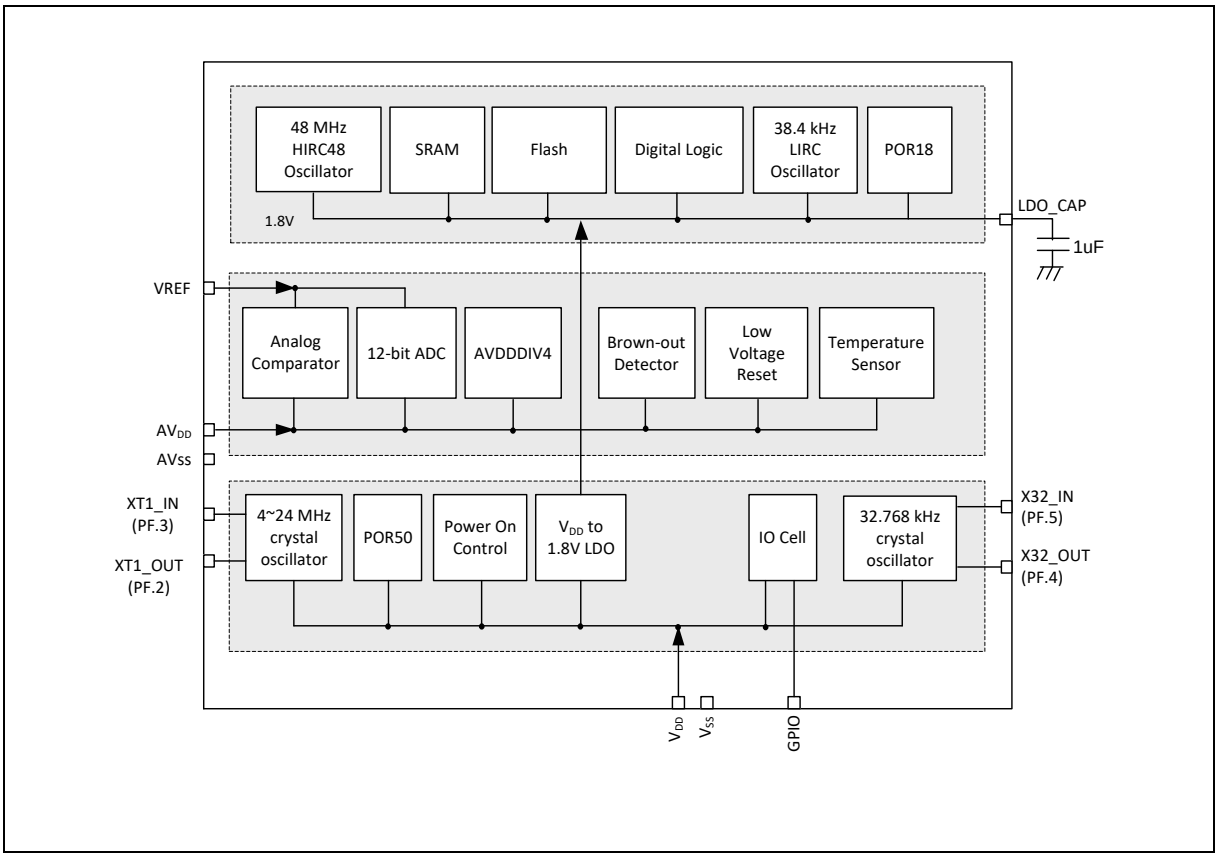


Figure 6.2-6 NuMicro M2A23 Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M2A23 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode in the M2A23 series.

Mode	CPU Operating Maximum	LDO_CAP(V)	Clock Disable

	Speed(MHz)		
Normal mode	72	1.8	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	1.8	Only CPU clock is disabled.
Power-down mode	CPU enters Power-down mode	1.8	Most clocks are disabled except LIRC/LXT, and only WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.2-2 Power Mode Table

There are different power mode entry settings and leaving condition for each power mode. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT [7]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	CPU Run WFI Instruction
Normal mode	0	0	NO
Idle mode (CPU enter Sleep mode)	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, Timer, UART, BOD, CLKFAIL, GPIO, EINT, USCI, I^2C and ACMP
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

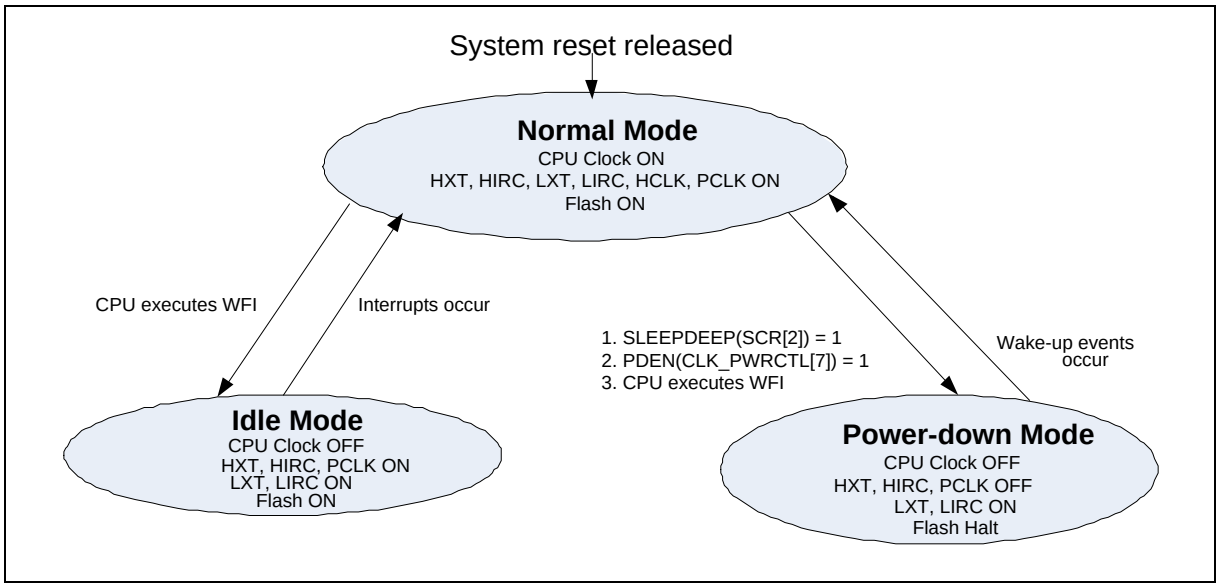


Figure 6.2-7 Power Mode State Machine

The detail clock status in each power mode is listed in Table 6.2-5.

Clocks	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~32 MHz XTL)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32.768 kHz XTL)	ON	ON	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]
PLL	ON	ON	Halt
MLDO	ON	ON	OFF
ULDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	Halt	Halt
UART	ON	ON	ON/OFF[5]
USCI	ON	ON	Halt

ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT (32.768 kHz XTL) ON or OFF depends on software setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on software setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
5. If UART clock source is selected as LXT and LXT is on.

Wake-up sources in Power-down mode:

BOD, CLKFAIL, EINT, GPIO, Timer, WDT, UART, USCI, I²C and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear (SYS_BODCTL[4]).
CLKFAIL	LXT Clock Fail Interrupt	After software writes 1 to clear (CLK_CLKDSTS[1]).
EINT	External Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]).
UART	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
	LIN Wake-up	After software writes 1 to clear LINWKF (UARTx_LINWKCTL[29]).
USCI UART	CTS Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I²C	Data toggle	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1

		to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.5 System Memory Map

The NuMicro M2A23 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M2A23 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0003_FFFF	FLASH_BA	Flash Memory Space (256 Kbytes)
0x2000_0000 – 0x2000_5FFF	SRAM0_BA	SRAM Memory Space (24 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA 0 Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4002_0000 – 0x4002_1FFF	CANFD0_BA	CANFD0 Control Registers
0x4002_4000 – 0x4002_5FFF	CANFD1_BA	CANFD1 Control Registers
0x4002_8000 – 0x4002_9FFF	CANFD2_BA	CANFD2 Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	ADC0_BA	Analog-Digital-Converter (ADC) 0 Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_C000 – 0x4005_CFFF	PWM0_BA	PWM0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers

0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4009_4000 – 0x4009_4FFF	LLSI0_BA	LLSI0 Control Registers
0x4009_5000 – 0x4009_5FFF	LLSI1_BA	LLSI1 Control Registers
0x4009_6000 – 0x4009_6FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	NVIC_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Organization

The M2A23 supports embedded SRAM with total 24 Kbytes size and the SRAM organization is separated to two banks: SRAM bank0 and SRAM bank1. The first bank has 4 Kbytes address space, the second bank has 20 Kbytes address space. The SRAM bank0 supports parity error check to make sure chip operating more stable.

- Supports total 24 Kbytes SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0
- Supports oversize response error

Table 6.2-9 shows the SRAM organization of M2A23. There are two SRAM banks in M2A23. The bank0 is addressed to 4 Kbytes and the bank1 is addressed to 20 Kbytes. The bank0 addess space is from 0x2000_0000 to 0x2000_0FFF. The bank1 addess space is from 0x2000_1000 to 0x2000_5FFF. The address between 0x2000_6000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

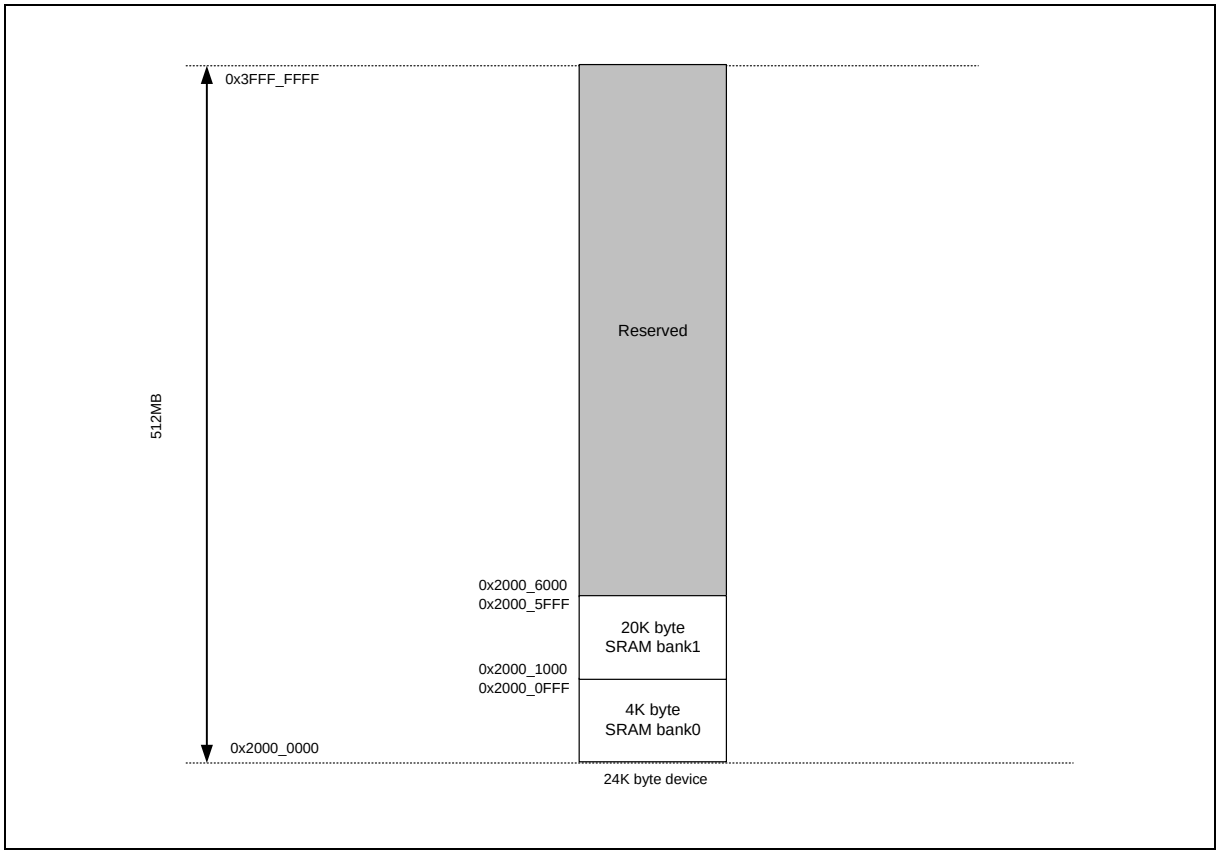


Figure 6.2-8 SRAM Memory Organization

6.2.7 Chip Bus Matrix

The M2A23 series supports Bus Matrix to manage the access arbitration between masters. The access arbitration use round-robin algorithm as the bus priority.

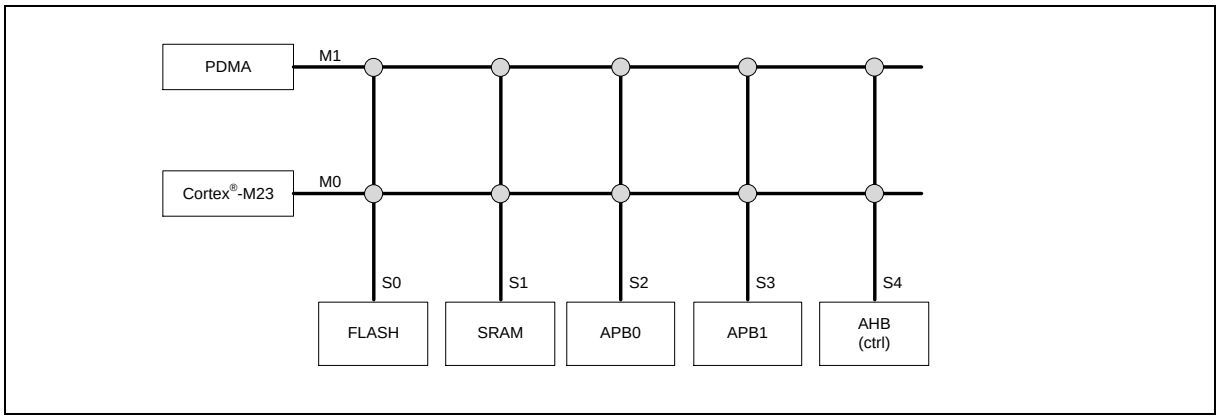


Figure 6.2-9 NuMicro M2A23 Bus Matrix Diagram

6.2.8 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if 32.768 kHz crystal is soldered and enabled, user has to set REFCKSEL (SYS_HIRCTRIMCTL [10] reference clock selection) to “0”, set FREQSEL (SYS_HIRCTRIMCTL [1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.9 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence. All proteced control registers are noted “(Write Protect)” and add an note “**Note:** This bit is write protected. Refer to the SYS_REGLCTL register “ in register description field.

6.2.10 System Timer (SysTick)

The Cortex-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm Cortex-M23 Technical Reference Manual” and “Arm v8-M Architecture Reference Manual”.

6.2.11 Nested Vectored Interrupt Controller (NVIC)

The Cortex-M23 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0 to R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "Arm Cortex-M23 Technical Reference Manual" and "Arm v8-M Architecture Reference Manual".

6.2.11.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by the M2A23 series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable

SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ57)	16 ~ 73	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	FMC_INT	Flash Memory Controller interrupt
22	6	Reserved	Reserved
23	7	Reserved	Reserved
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from INT0 pins
27	11	EINT1	External interrupt from INT1 pins
28	12	EINT2	External interrupt from INT2 pin
29	13	EINT3	External interrupt from INT3 pin
30	14	EINT4	External interrupt from INT4 pin
31	15	EINT5	External interrupt from INT5 pin
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[15:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	GPD_INT	External interrupt from PD[15:0] pin
36	20	Reserved	Reserved
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	Reserved	Reserved
39	23	SPI0_INT	SPI0 interrupt
40	24	BRAKE0_INT	PWM0 brake interrupt
41	25	PWM0_P0_INT	PWM0 pair 0 interrupt

42	26	PWM0_P1_INT	PWM0 pair 1 interrupt
43	27	PWM0_P2_INT	PWM0 pair 2 interrupt
44	28	Reserved	Reserved
45	29	Reserved	Reserved
46	30	Reserved	Reserved
47	31	Reserved	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	Reserved	Reserved
56	40	PDMA0_INT	PDMA0 interrupt
57	41	Reserved	Reserved
58	42	ADC0_INT	ADC0 interrupt source
59	43	Reserved	Reserved
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	BPWM0_INT	BPWM0 interrupt
62	46	LLSI0_INT	LLSI0 interrupt
63	47	LLSI1_INT	LLSI1 interrupt
64	48	CANFD00_INT	CANFD00 interrupt
65	49	CANFD01_INT	CANFD01 interrupt
66	50	CANFD10_INT	CANFD10 interrupt
67	51	CANFD11_INT	CANFD11 interrupt
68	52	CANFD20_INT	CANFD20 interrupt
69	53	CANFD21_INT	CANFD21 interrupt
70	54	Reserved	Reserved
71	55	Reserved	Reserved
72	56	USCI0_INT	USCI0 interrupt
73	57	USCI1_INT	USCI1 interrupt

Table 6.2-9 Interrupt Number Table

6.2.11.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Arm v8-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 7.2-10 Vector Figure Format

6.2.11.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.12 System Control Register

The Cortex-M23 status and operation mode control are managed by System Control Registers. Including Cortex-M23 interrupt priority and Cortex-M23 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm Cortex-M23 Technical Reference Manual*" and "*Arm v8-M Architecture Reference Manual*".

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4 to 24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

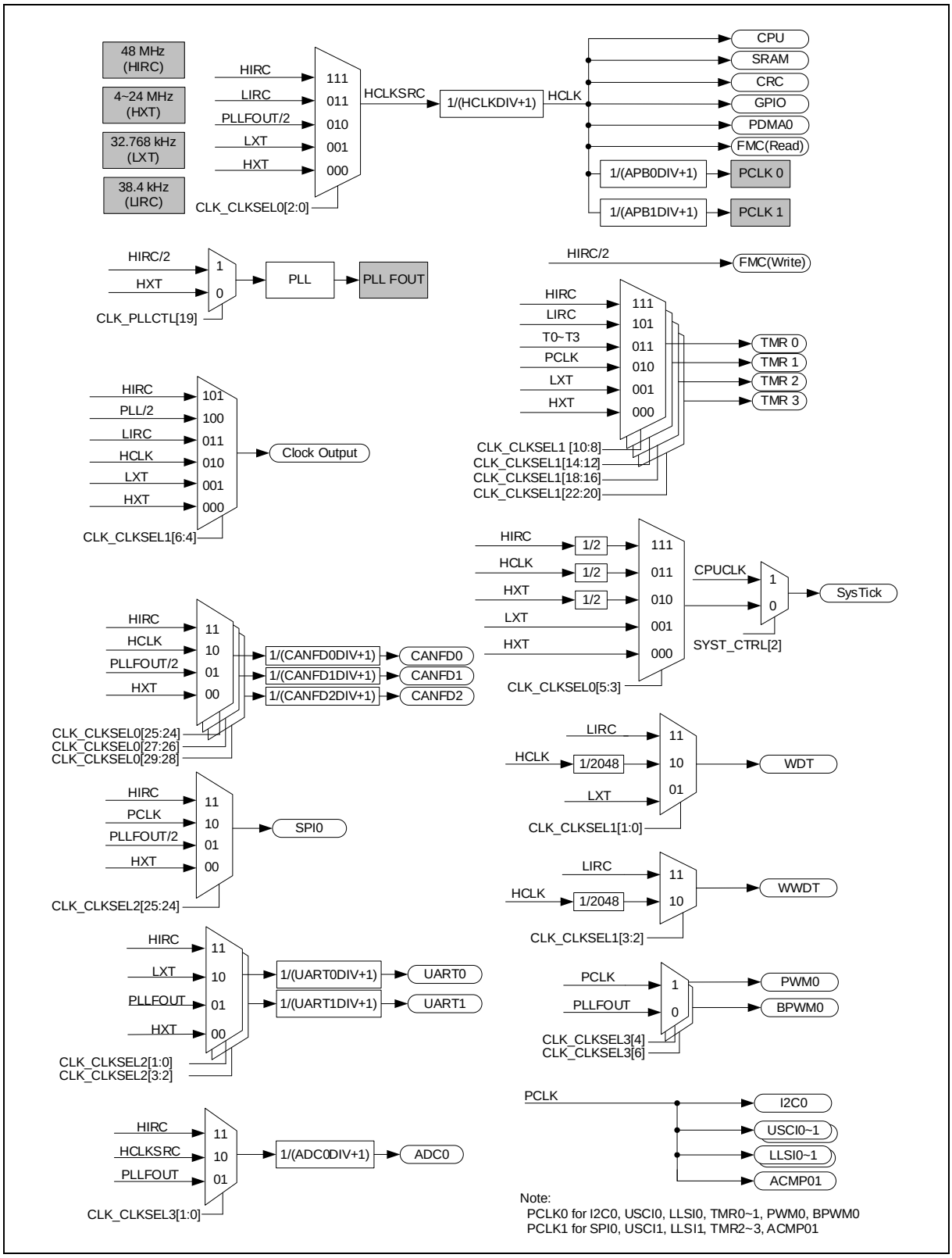


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low-speed crystal oscillator (LXT)
- 4 to 24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 48 MHz internal high speed oscillator divided by 2 (HIRC/2)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

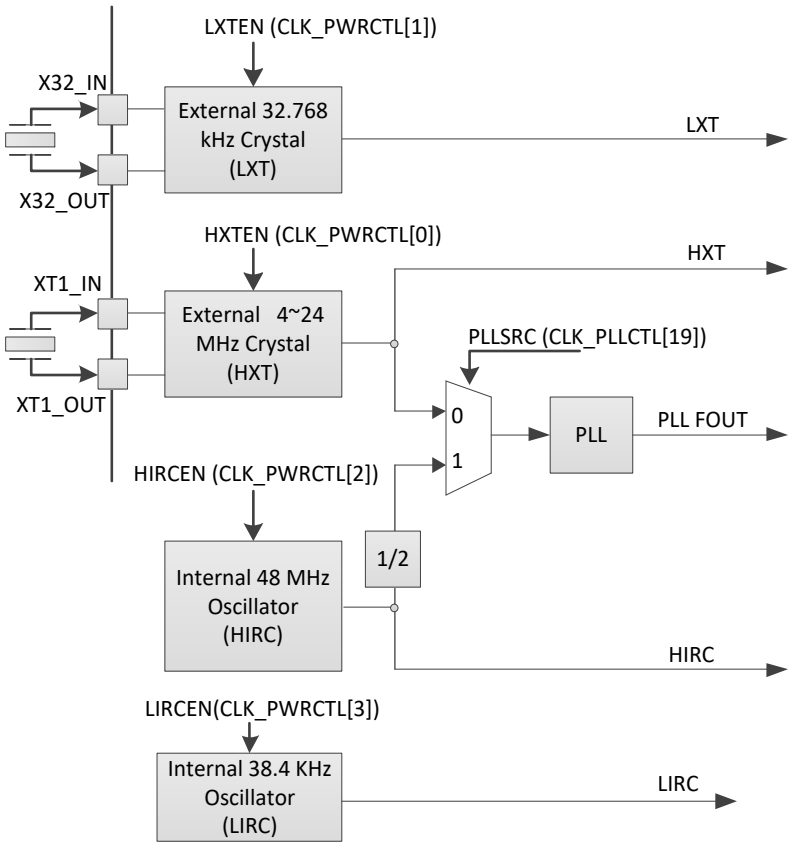
Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter starts counting and correlated clock stable index is set to 1 after stable counter value reaches a define value as shown in Table 6.3-1. System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-2 will automatically cleared when user disables the clock source. Besides, the clock stable index of HXT, HIRC and PLL will be automatically cleared when chip enters power-down and clock stable counter will re-count after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clock	341.33 us for 12 MHz
LXT	16384 LXT clock	500 ms for 32.768 kHz
PLL	It's based on the value of STBSEL (CLK_PLLCTL[23]) STBSEL = 0, stable count is 6144 clocks of PLL clock source. STBSEL = 1, stable count is 12288 clocks of PLL clock source. (Default)	STBSEL = 0, 512 us for 12 MHz STBSEL = 1, 1024 us for 12 MHz
LIRC	5 LIRC clock	130.2 us for 38.4 kHz
HIRC	It's based on the value of HIRCSTBS (CLK_PWRCTL[17:16]) HIRCSTBS = 00, stable count is 1024 HIRC clocks. HIRCSTBS = 01, stable count is 512 HIRC clocks.	HIRCSTBS = 0, 21.33 us for 48 MHz HIRCSTBS = 1, 10.66 us for 48 MHz

Table 6.3-1 Clock Stable Count Value Table

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
HXT	HXTEN(CLK_PWRCTL[0])	HXTSTB(CLK_STATUS[0])
LXT	LXTEN(CLK_PWRCTL[1])	LXTSTB(CLK_STATUS[1])
PLL	PD(CLK_PLLCTL[16])	PLLSTB(CLK_STATUS[2])
LIRC	LIRCEN(CLK_PWRCTL[3])	LIRCSTB(CLK_STATUS[3])
HIRC	HIRCEN(CLK_PWRCTL[2])	HIRCSTB(CLK_STATUS[4])

Table 6.3-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table

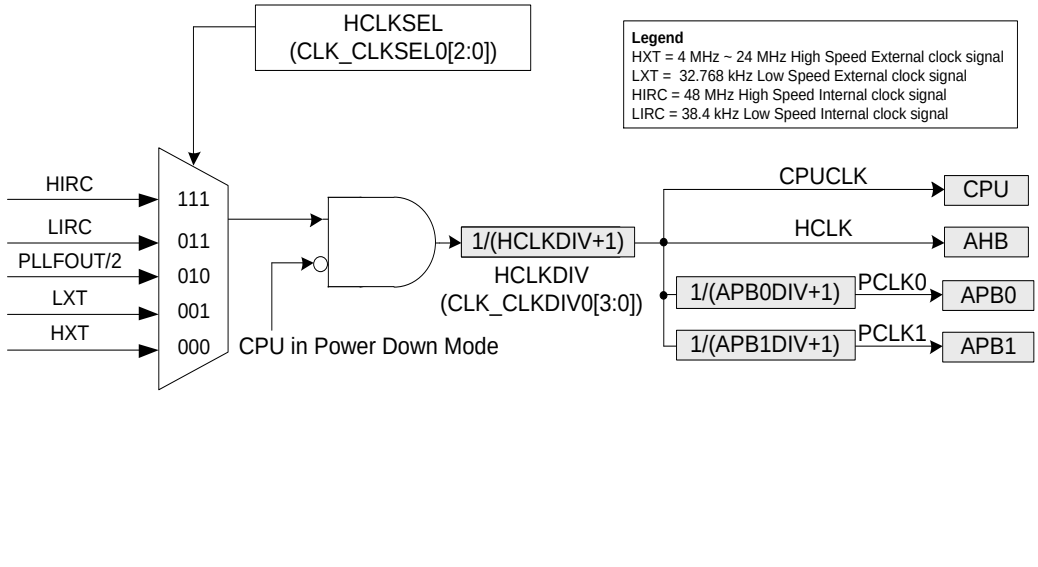


Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which are generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0 [2:0]). The block diagram is shown in Figure 6.3-3.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled by setting HXTFDEN (CLK_CLKDCTL[4]), the HIRC clock is enabled automatically. When LXT detector is enabled by setting LXTFDEN (CLK_CLKDCTL[12]), the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will automatically switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. HXT clock source stable flag, HXTSTB (CLK_STATUS[0]), will be cleared if HXT stops when using HXT fail detector function. User can try to recover HXT by disabling HXT and enabling HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recovered to oscillate after re-enable action and user can switch system clock to HXT again.

When LXT clock detector is enabled, the system clock will automatically switch to LIRC if LXT clock stops being detected on the following condition: system clock source comes from LXT. If LXT clock stop condition is detected, the LXTFIF (CLK_CLKDSTS[1]) is set to 1 and chip will enter interrupt if LXTFIEN (CLK_CLKDCTL[13]) is set to 1. LXT clock source stable flag, LXTSTB (CLK_STATUS[1]), will be cleared if LXT stops when using LXT fail detector function. User can try to recover LXT by disabling LXT and enabling LXT again to check if the clock stable bit is set to 1 or not. If LXT clock stable bit is set to 1, it means LXT is recovered to oscillate after re-enable action and user can switch system clock to LXT.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

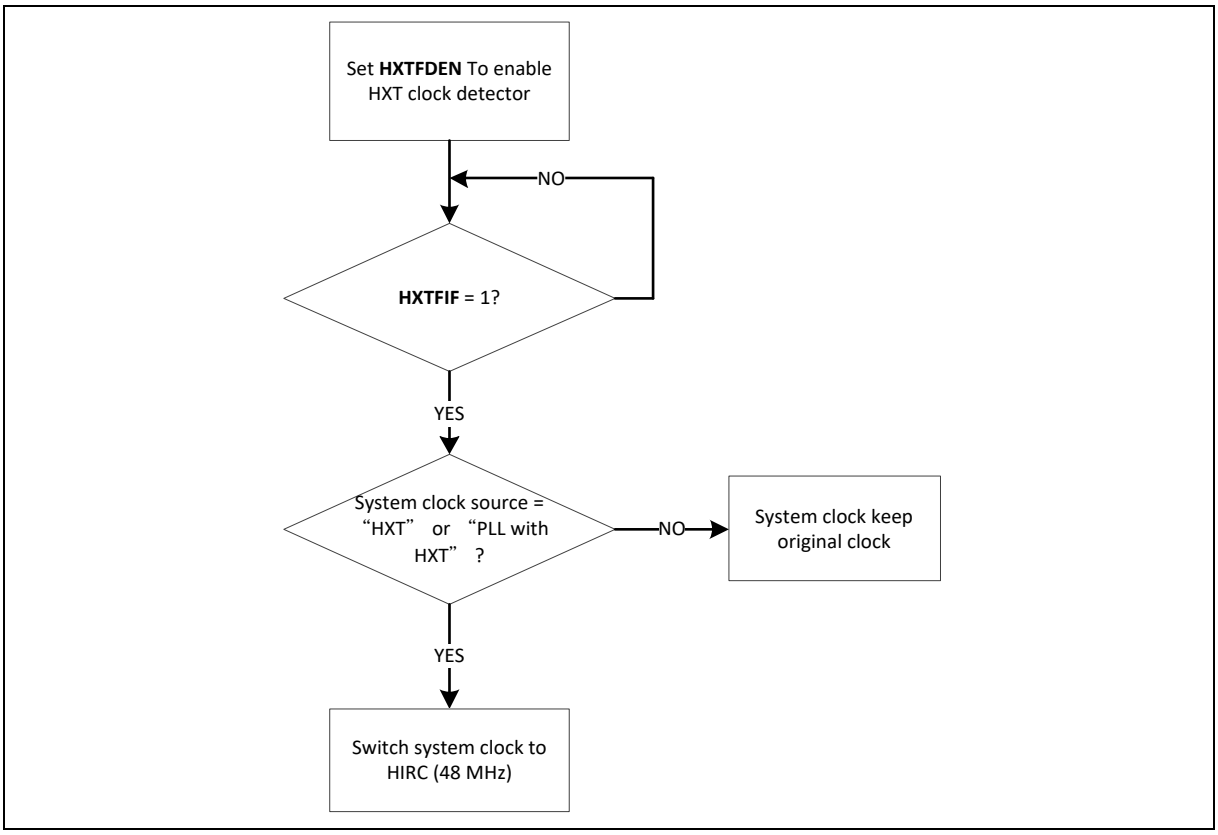


Figure 6.3-4 HXT Stop Protect Procedure

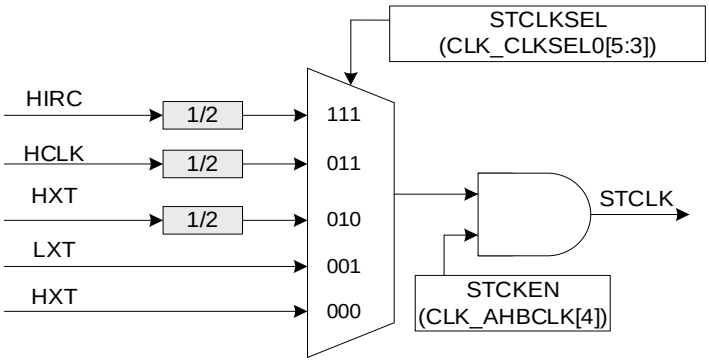
Besides, user can also set HXTFQDEN (CLK_CLKDCTL[16]) to monitor HXT CLK frequency range by HIRC clock. User can set UPERBD (CLK_CDUPB[10:0]) and LOWERBD (CLK_CDLOWB[10:0]) to decide monitoring frequency window. If target clock speed is greater than UPERBD or less than LOWERBD, the HXT Clock Frequency Range Detector Interrupt Flag HXTFQIF(CLK_CLKDSTS[8]) will be set to 1 and chip will enter interrupt if HXTFQIEN (CLK_CLKDCTL[17]) is set to 1.

The formula of UPERBD and LOWERBD is listed below.

HIRC_period* 1024 < HXT_period* UPERBD

HIRC_period* 1024 > HXT_period* LOWERBD

The clock source of SysTick in Cortex-M23 core can use CPU clock or external clock (SYST_CSR[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2 and CLK_CLKSEL3 description in Register Description section.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources, and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low-speed RC oscillator (LIRC) clock
  - 32.768 kHz external low-speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

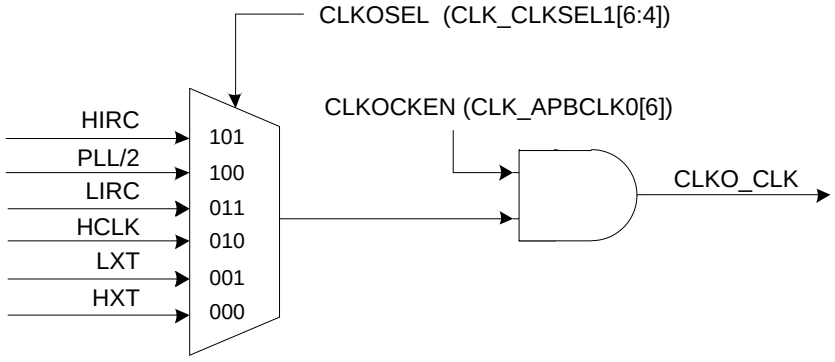
This device is equipped with a power-of-2 frequency divider composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIVI1EN(CLK_CLKOCTL[5]) is set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The clock output clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT or LIRC.



Note: Before clock switching, both the pre-selected and newly selected clock source must be turned on and stable.

Figure 6.3-6 Clock Source of Clock Output

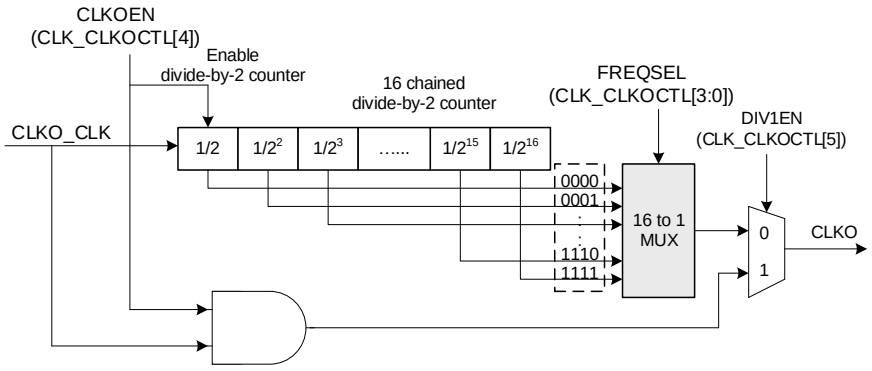


Figure 6.3-7 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 64/128/256 Kbytes on-chip embedded Flash, which consists of two 32/64/128 Kbytes Bank0 and Bank1 for application and configurable Data Flash to store some application dependent data. An User Configuration block is provided for system initialization. A loader ROM (LDROM) is used for In-System-Programming (ISP) function. A security protection ROM (SPROM) can conceal user program. A 1 Kbyte cache with zero wait cycle is implemented to improve the performance of code/data fetching. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without the chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade.
- Supports OTA (Over-The-Air) function.
- Supports 64/128/256 Kbytes application ROM (APROM).
- Supports 4 Kbytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 2 Kbytes security protection ROM (SPROM) to conceal user program.
- Supports User Configuration block to control system initialization.
- Supports 2 Kbytes page erase for all embedded Flash.
- Supports 32-bit/64-bit and multi-word Flash programming function.
- Supports CRC-32 checksum calculation function.
- Supports Flash all one verification function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.
- Supports cache memory to improve Flash access performance and reduce power consumption.
- Supports APROM Function Safety Protect feature.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 55 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 55 pins are arranged in 5 ports named as PA, PB, PC, PD, PF. PA and PB has 16 pins on port. PC and PF has 9 pins on port. PD has 5 pins on port. Each of the 55 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOIN = 0, all GPIO pins in mode Quasi-bidirectional after chip reset
  - CIOIN = 1, all GPIO pins in input tri-state mode after chip reset
- Supports independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports EINT0~5 edge detect and trigger function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. PDMA can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. PDMA has a total of 6 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 6 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, USCI, SPI, ACMP, PWM, EINT, I^2C, Timer, ADC and LLSI request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger BPWM, PWM, ADC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP0 output and ACMP1 output
- Supports internal capture triggered source from ACMP0 output, ACMP1 output, HXT, HIRC, LIRC and LXT

6.8 Basic PWM Generator and Capture Timer (BPWM)

6.8.1 Overview

The chip provides one BPWM generator — BPWM0. The BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for ADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.8.2 Features

6.8.2.1 BPWM Function Features

- Supports maximum clock frequency up to 144 MHz frequency
- Supports up to one BPWM module; the module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger ADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.8.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.9 PWM Generator and Capture Timer (PWM)

6.9.1 Overview

The chip provides one PWM generators — PWM0. Each PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also supports PDMA to transfer captured data to memory.

6.9.2 Features

6.9.2.1 PWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to one PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin, analog comparator, ADC result monitor and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter matches 0, period value or compared value
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports PWM output accumulator stop counter mode

- Support External Pin Trigger Function

6.9.2.2 *Capture Function Features*

- Supports 3-bit capture input noise filter
- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.10 Watchdog Timer (WDT)

6.10.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.10.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 0.488 ms ~ 32 s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT

6.11 Window Watchdog Timer (WWDT)

6.11.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.11.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.12 UART Interface Controller (UART)

6.12.1 Overview

The chip provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports eleven types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.12.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 8/8 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
  - LIN slave header time-out detection function
  - LIN response time-out detection function
  - LIN wake-up function
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission

direction

- Supports PDMA transfer function
- Supports Single-wire function mode
- Supports bus idle time-out mode
- Supports fractional Baud Rate divider

UART Feature	UART0	UART1	USCI-UART
FIFO	8 Bytes	8 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	√	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-
Received Data FIFO reached threshold Time-out Wake-up	√	√	-
Baud Rate Compensation	√	√	-
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.12-1 M2A23 Series UART Features

6.13 I²C Serial Interface Controller (I²C)

6.13.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There is one set of I²C controller which supports Power-down Wake-up function.

6.13.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports one I²C port
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports two-level buffer function
- Supports setup/hold time programmable
- Add pin swap function
- Supports Bus Management (SM/PM compatible) function Compatible with the SMBUS Specification Rev 2.0 (http://smbus.org/specs/) and PMBUS Specification Rev 1.2 (http://pmbus.org/)

6.14 Serial Peripheral Interface (SPI)

6.14.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one set of SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer.

6.14.2 Features

- One set of SPI controller
- Supports Master or Slave mode operation
- Master mode up to 36 MHz (when chip works at V_{DD} = 2.5~5.5V)
- Slave mode up to 18 MHz (when chip works at V_{DD} = 2.5~5.5V)
- Configurable bit length of a transaction word from 4 to 32-bit
- Provides separate 4-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports receive-only mode

6.15 USCI - Universal Serial Control Interface Controller (USCI)

6.15.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.15.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.16 USCI – UART Mode

6.16.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.16.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Supports 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

6.17 USCI - SPI Mode

6.17.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

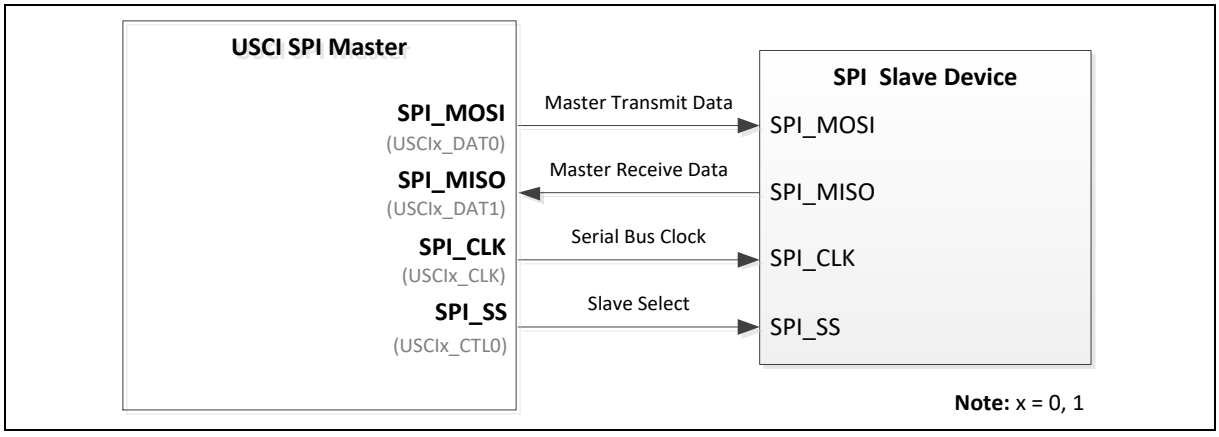


Figure 6.17-1 SPI Master Mode Application Block Diagram

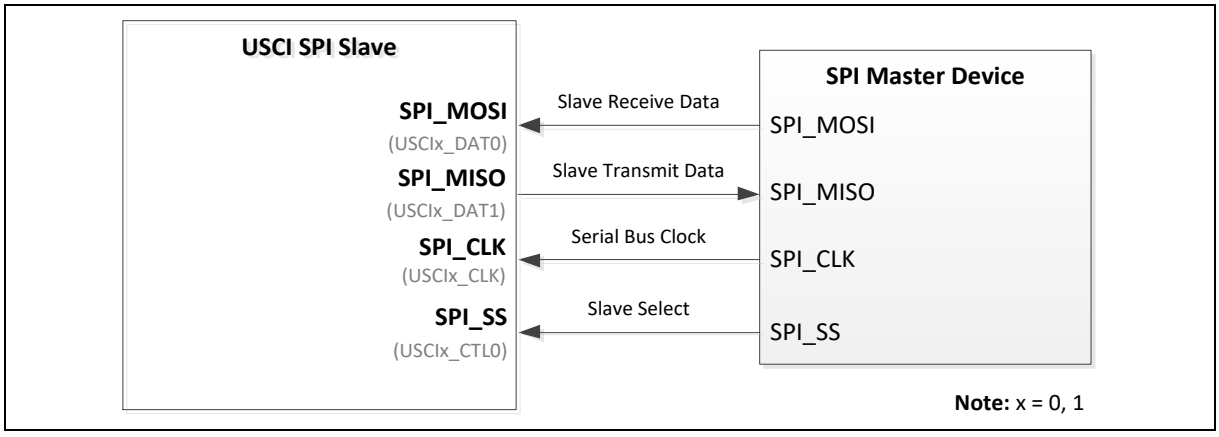


Figure 6.17-2 SPI Slave Mode Application Block Diagram

6.17.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master < f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function

- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.18 USCI - I²C Mode

6.18.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.18-1 for more detailed I²C BUS Timing.

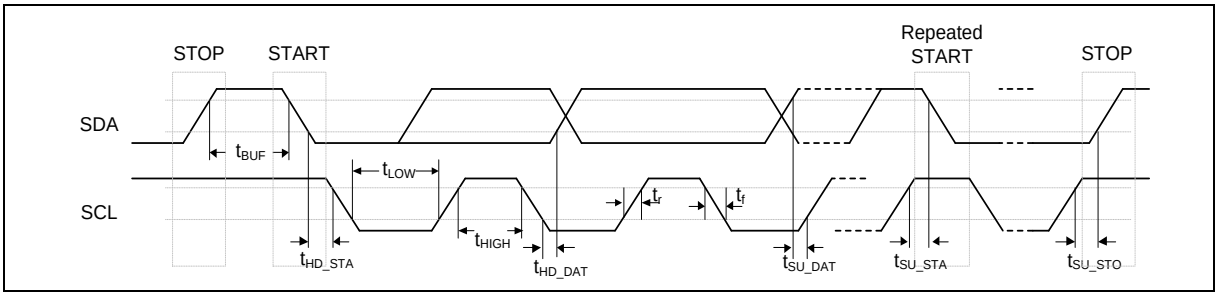


Figure 6.18-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.18.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.19 Controller Area Network with Flexible DataRate (CAN FD)

6.19.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and needs to be connected to additional transceiver hardware for the CAN bus physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.19.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.20 CRC Controller (CRC) - Configurable

6.20.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with 8-bits, 16-bits and 32-bits configurable polynomials.

6.20.2 Features

- Supports 8-bits, 16-bits and 32-bits configurable polynomials
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.21 LED Light Strip Interface (LLSI)

6.21.1 Overview

The LLSI is a RGB LED strip controller that can convert the RGB data for hundreds of LEDs per strip into T0 and T1 code output. There are two sets of LLSI that can be used.

6.21.2 Features

- Two sets of LLSI channels with IDLE polarity control
- Each LLSI has 4x32-bit TX FIFO
- Configurable transfer period and frame reset length
- Configurable T0H and T1H duty cycle
- Supports RGB and GRB output format
- Supports Software mode and PDMA base mode transfer

6.22 Analog-to-Digital Converter (ADC)

6.22.1 Overview

This chip contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with sixteen input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin STADC (PC.1/PF.5), timer0~3 overflow pulse trigger and BPWM trigger.

6.22.2 Features

- Analog input voltage range: 0 ~ AV_{DD}.
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog input channels
- Up to 1 fully differential analog input channel
- Maximum ADC peripheral clock frequency is 36 MHz
- Minimum ADC peripheral clock frequency is 4 MHz
- Up to 1.8 Msps sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - BPWM trigger with optional start delay period
  - PWM trigger with optional start delay period
  - ACMP0 and ACMP1 interrupt pulse triggers
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Three internal channels, band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}) and $AV_{DD}/4$.
- Supports PDMA transfer mode.
- Supports calibration function and calibration interrupt.

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}) and $AV_{DD}/4$ is active, the maximum sampling rate will be 300 ksps.

6.23 Analog Comparator Controller (ACMP)

6.23.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.23.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Support programmable hysteresis window: 0mV and 30mV
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2 and ACMP0_P3
  - 3 negative sources:
    - ACMP0_N0
    - Internal band-gap voltage (VBG)
    - Comparator Reference Voltage (CRV)
- ACMP1 supports
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2 and ACMP1_P3
  - 3 negative sources:
    - ACMP1_N0
    - Internal band-gap voltage (VBG)
    - Comparator Reference Voltage (CRV)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports window compare mode and window latch mode
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports triggers to ADC to convert
- Supports request to PDMA to transfer data

6.24 Peripherals Interconnection

6.24.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast response.

6.24.2 Peripherals Interconnect Matrix Table

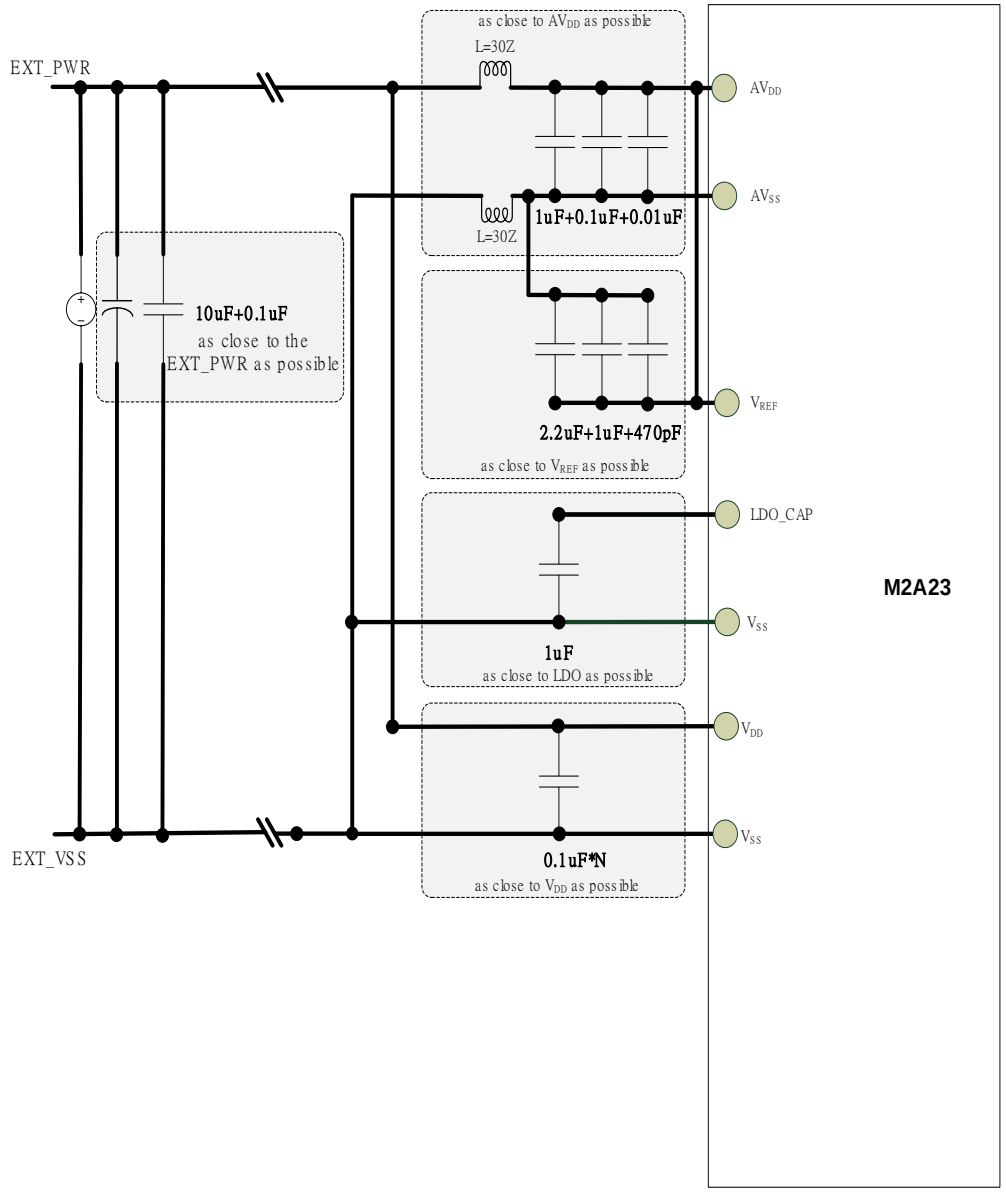
Source	Destination				
	ADC	HIRC TRIM	BPWM	PWM	Timer
LIRC	-	-	-	-	√
BPWM	√	-	-	-	-
PWM	√	-	-	-	-
LXT	-	√	-	-	-
Timer	√	-	√	√	√

Table 6.24-1 Peripherals Interconnect Matrix Table

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

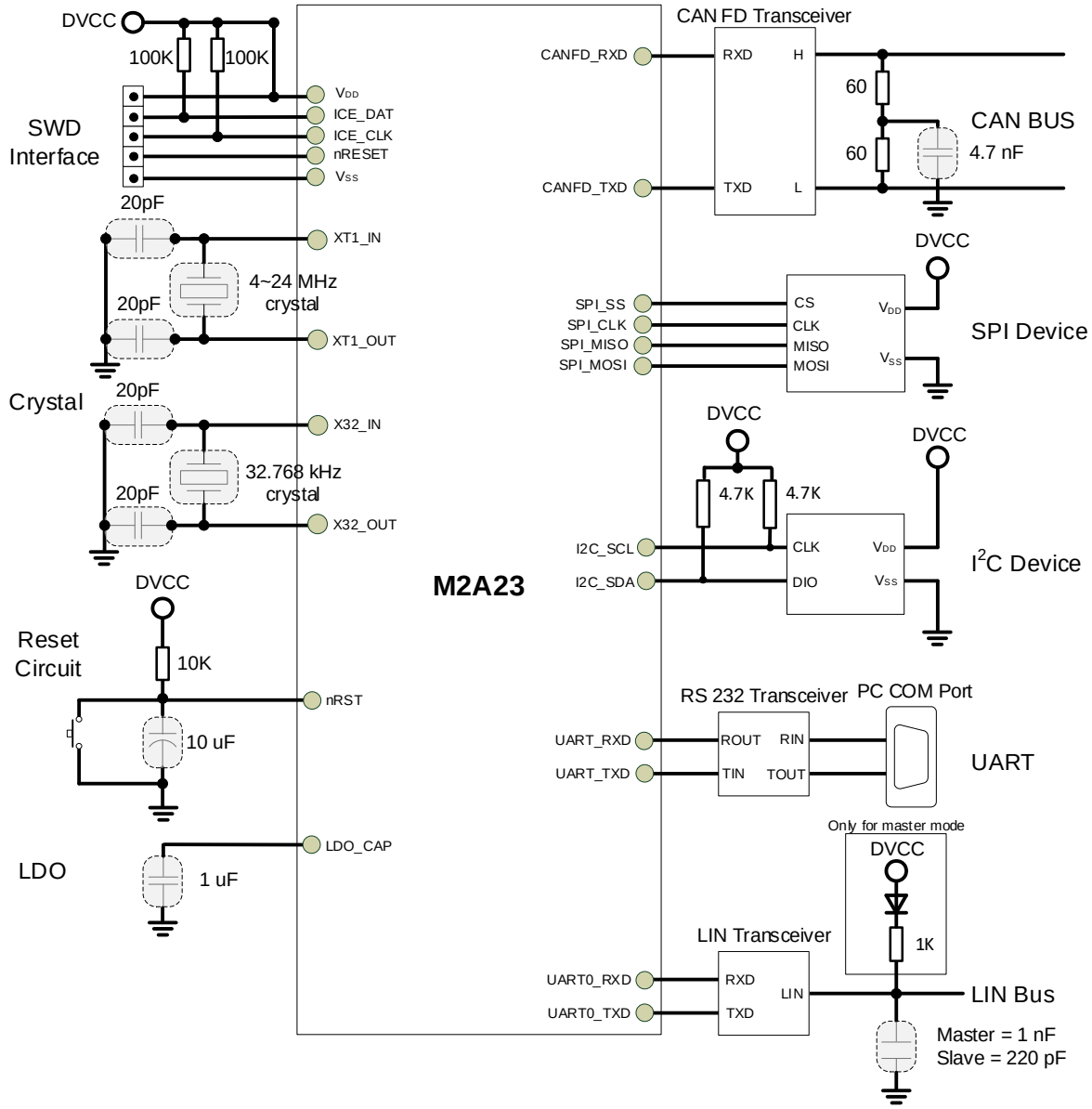
7.1.1 V_{REF} Connected to AV_{DD}



Note: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

Figure 7.1-1 Power supply scheme for V_{REF} connecting to AV_{DD}

7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Note 3: C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.

Figure 7.2-1 Peripheral Application Scheme

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Note:

1. All main power (V_{DD}, AV_{DD}, V_{REF}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characeristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>A_{VDD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- θ_{JC} = thermal resistance junction-case (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	125	℃
T_J	Operating junction temperature	-40	-	135	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1]	Thermal resistance junction-ambient 48-pin QFN(5x5 mm)	-	37.8	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	58	-	℃/Watt
θ_{JC}[1]	Thermal resistance junction-case 48-pin QFN(5x5 mm)	-	TBD	-	℃/Watt
	Thermal resistance junction-case 48-pin LQFP(7x7 mm)	-	TBD	-	℃/Watt
	Thermal resistance junction-case 64-pin LQFP(7x7 mm)	-	TBD	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	-8000	-	8000	V
V_{CDM}[2]	Electrostatic discharge,charge device model	-1000	-	1000	
LU[3]	Pin current for latch-up[3] Class I for room temperature Class II for max. Ta temperature	-300 @ Class I -100 @ Class II	-	300 @ Class I 100 @ Class II	mA
V_{EFT}[4]	Fast transient voltage burst	-4.4	-	4.4	kV
V_{SYSESD}	System electrostatic discharge (contact mode)	-2	-	2	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level.
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
48-pin QFN(5x5 mm) [1]	MSL 3
48-pin LQFP(7x7 mm) [1]	MSL 3
64-pin LQFP(7x7 mm) [1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

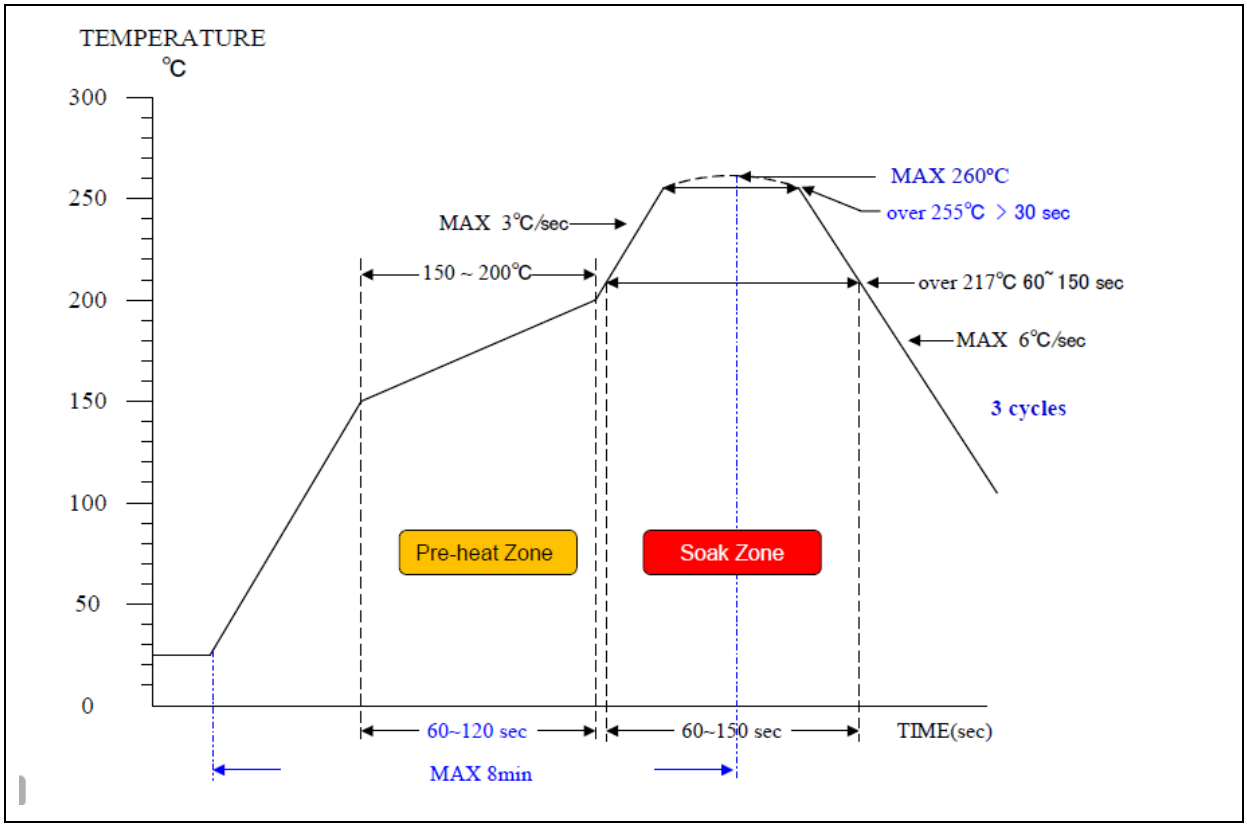


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C, HCLK = 72 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	2.5	-	5.5	V	
AV_{DD}[1][4]	Analog operation voltage	V_{DD}				
V_{REF}[4]	Analog reference voltage	2.5	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.174	1.210	1.246	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	12	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	200	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3	-	µC	V_{DD} = 2.5 V, T_A = 125 °C, I_{RUSH} = 150 mA for 15 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 5 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable, HIRC, PLL, HXT or LIRC clock, F_{HCLK} 24MHz from HXT, F_{HCLK} 4MHz and 3MHz from HIRC48M divide 12 and 16	72 MHz	16.50	16.79	17.28	19.22	mA
		48 MHz	9.28	9.41	9.94	11.84	
		24 MHz	5.04	5.16	5.91	7.97	
		12 MHz	3.37	3.46	3.98	5.83	
		4 MHz	2.05	2.12	2.64	4.48	
		3 MHz	1.88	1.96	2.48	4.32	
		32.768 kHz	0.10	0.12	0.64	2.47	
		38 kHz	0.09	0.12	0.64	2.47	
	Normal run mode, executed from Flash, all peripherals enable HIRC, PLL, HXT or LIRC clock, F_{HCLK} 24MHz from HXT, F_{HCLK} 4MHz and 3MHz from HIRC48M divide 12 and 16	72 MHz	39.38	39.92	40.57	42.74	
		48 MHz	23.54	23.81	24.47	26.59	
		24 MHz	11.97	12.19	13.14	15.37	
		12 MHz	8.16	8.31	8.89	10.83	
		4 MHz	4.76	4.87	5.42	7.31	
		3 MHz	4.33	4.44	4.99	6.88	
		32.768 kHz	0.11	0.13	0.66	2.50	
		38 kHz	0.10	0.13	0.66	2.50	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	
I_{DD_IDLE}	Idle mode, all peripherals disable, HIRC, PLL, HXT or LIRC clock, F_{HCLK} 24MHz from HXT, F_{HCLK} 4MHz and 3MHz from HIRC48M divide 12 and 16	72 MHz	5.79	5.97	6.50	8.36	mA
		48 MHz	2.10	2.18	2.71	4.55	
		24 MHz	1.42	1.52	2.21	4.21	
		12 MHz	1.56	1.64	2.16	4.00	
		4 MHz	1.44	1.51	2.03	3.87	
		3 MHz	1.42	1.50	2.02	3.85	
		32.768 kHz	0.08	0.12	0.64	2.47	
		38 kHz	0.08	0.12	0.64	2.47	
	Idle mode, all peripherals enable, HIRC, PLL, HXT or LIRC clock, F_{HCLK} 24MHz from HXT, F_{HCLK} 4MHz and 3MHz from HIRC48M divide 12 and 16	72 MHz	28.58	29.06	29.75	31.92	
		48 MHz	16.28	16.55	17.21	19.28	
		24 MHz	8.30	8.49	9.38	11.57	
		12 MHz	6.35	6.49	7.07	9.00	
		4 MHz	4.15	4.25	4.81	6.71	
		3 MHz	3.87	3.97	4.53	6.42	
		32.768 kHz	0.09	0.13	0.65	2.49	
		38 kHz	0.09	0.13	0.65	2.50	

Note:

1. When analog peripheral blocks such as ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[1] 32.768 kHz	LIRC 38 kHz	Typ[2]	Max[3][4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	14.90	38.90[5]	535.97	2302.51	µA
	Power-down mode, all peripherals disable	-	V	15.91	39.72	538.28	2307.01	
	Power-down mode, all peripherals disable	V	-	15.86	39.87	539.24	2309.08	
	Power-down mode, all peripherals disable	V	V	17.03	41.07	541.51	2313.84	
	Power-down mode, all peripherals disable Except WDT/Timer	-	V	16.72	40.45	541.52	2314.83	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	-	17.16	41.08	542.92	2319.80	
	Power-down mode, all peripherals disable Except WDT/Timer/UART	V	V	18.43	42.27	545.50	2321.65	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 12.5 pF for L2 gain level.
2. LVR enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 5 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 72 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[*1]	Unit
PDMA0	492	uA
ISP	~0	
ST	316	
CRC	118	
CANFD0	2439	
CANFD1	2454	
CANFD2	2457	
FMCIDLE	723	
CANRAM0	129	
CANRAM1	133	
CANRAM2	127	
GPA	179	
GPB	241	
GPC	227	
GPD	230	
GPF	230	
WDT	289	
WWDT	273	
TMR0	636	
TMR1	634	
TMR2	636	
TMR3	640	
CLKO	449	
I2C0	269	
SPI0	892	
UART0	1621	
UART1	1356	

ADC0[2]	1000	
ACMP01[3]	487	
PWM0	910	
BPWM0	543	
USCI0	338	
USCI1	338	
LLSI0	295	
LLSI1	286	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	65.77	-	µS
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	1.7	-	
t_{ET_IDLE}	Enter to IDLE mode	2	-	cycles
t_{ET_NPD}	Enter to normal Power-down mode	0.3	-	µS

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current, but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 2.5 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1	-	V_{DD}		V_{DD} = 2.5 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-2	-	2	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-2	-	2		V_{DD} < V_{IN} < 5 V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	60.9	-	135.4	kΩ	V_{DD} = 5.5V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-68.80	-	-138.70	µA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-51.10	-	-109.80	µA	V_{DD} = 3.0 V V_{IN} = (V_{DD} - 0.4) V
	Source current for push-pull mode and high level	-5.53	-	-11.20	mA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-4.11	-	-8.73	mA	V_{DD} = 3.3 V V_{IN} = (V_{DD} - 0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	8.99	-	25.00	mA	V_{DD} = 4.5 V V_{IN} = 0.4 V
		6.69	-	19.30	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	0	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	V_{DD}	V	
R_{RST}[*1]	Internal nRESET pull up resistor	74.2	-	193.2	kΩ	V_{DD} = 2.5V ~ 5.5V
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	µS	Normal run and Idle mode
		-	24	-		Fast wake up Power-down mode
		75	-	155		Power-down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +125 °C, V_{DD} = 2.5 ~ 5.5V
I_{HRC}[*1]	Operating current		471		µA	
T_S[*2]	Stable time		5		µS	T_A = -40°C ~ +125 °C, V_{DD} = 2.5 ~ 5.5V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.2 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~125°C V_{DD}=2.5V~5.5V Without software calibration
I_{LRC}	Operating current		1.1		μA	V_{DD} = 3.3V
T_S	Stable time		500		μS	T_A=-40~125°C V_{DD}=2.5V~5.5V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.3 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.5	-	5.5	V	
R_f	Internal feedback resister	-	1	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	250	600	μA	4 MHz, Gain = L0, C_L = 12.5 pF, DIP
		-	380	980		12 MHz, Gain = L1, C_L = 12.5 pF, DIP
		-	400	1050		16 MHz, Gain = L2, C_L = 12.5 pF, DIP
		-	750	2050		24 MHz, Gain = L3, C_L = 12.5 pF, DIP 12 MHz, Gain = L3, C_L = 12.5 pF, SMD
T_S	Stable time	-	2400	2700	μS	4 MHz, Gain = L0, C_L = 12.5 pF, DIP
		-	600	700		12 MHz, Gain = L1, C_L = 12.5 pF, DIP
		-	400	550		16 MHz, Gain = L2, C_L = 12.5 pF, DIP
		-	380	600		24 MHz, Gain = L3, C_L = 12.5 pF, DIP
		-	2000	2200		12 Mhz, Gain = L3, C_L = 12.5 pF, SMD
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	0.7	1	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz,C_L = 12.5 pF, Gain = L0, DIP
		-	-	50		Crystal @12 MHz, C_L = 12.5 pF, Gain = L1, DIP
		-	-	30		Crystal @16 MHz, C_L = 12.5 pF, Gain = L2, DIP

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L3, DIP
		-	-	120		Crystal @12 MHz, C_L = 12.5 pF, Gain = L3, SMD

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

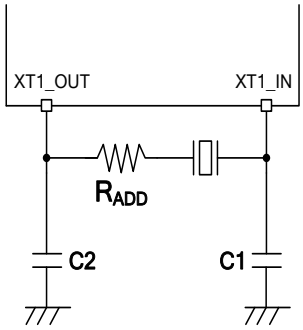


Table 8.4-4 External 4~32 MHz High Speed Crystal Characteristics

8.4.3.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

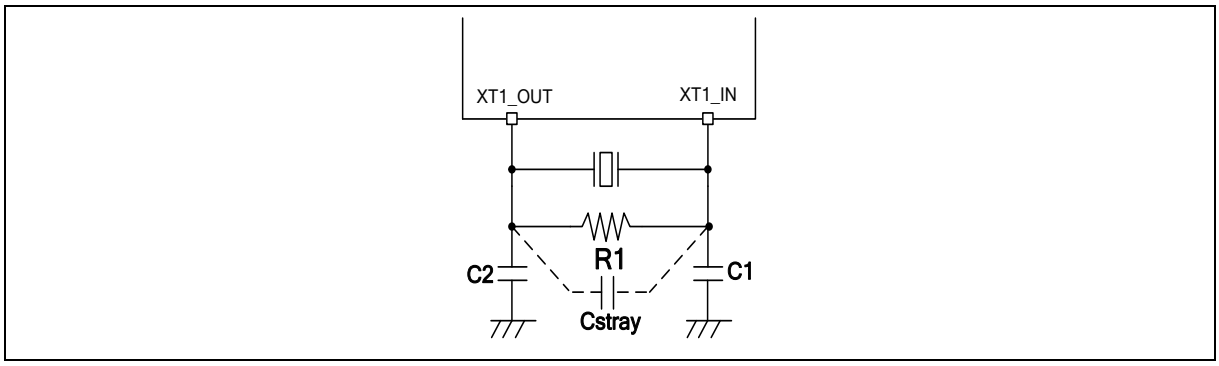
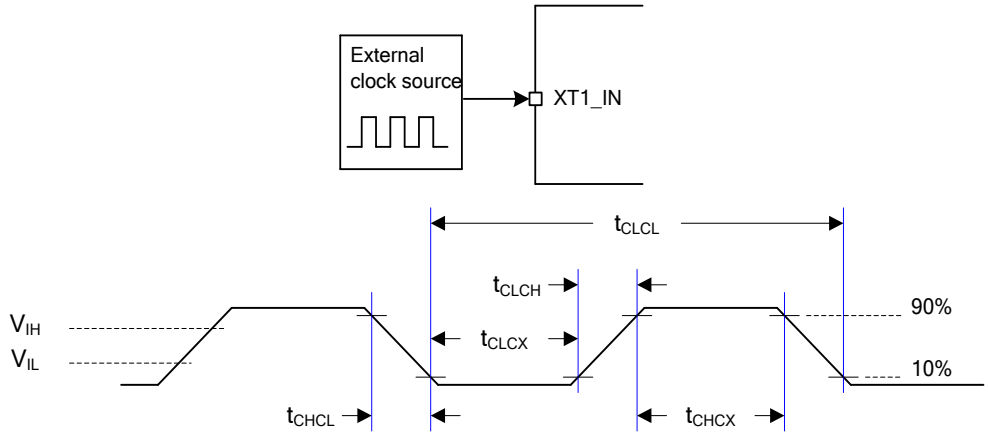


Figure 8.4-1 Typical Crystal Application Circuit

8.4.4 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	The XT1_IN is set as schmitt trigger input mode.
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	The XT1_IN is set as schmitt trigger input mode.



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~24 MHz High Speed Clock Input Signal

8.4.5 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.5	-	5.5	V	
T_{LXT}	Temperature range	-40	-	125	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	0.55	4.5	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L0
		-	0.65	4.8		ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	0.72	5.0		ESR=35 kΩ, C_L = 12.5 pF, Gain = L2
		-	0.9	5.7		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
		-	1	5.9		ESR=70 kΩ, C_L = 12.5 pF, Gain = L4
		-	1.1	6.2		ESR=70 kΩ, C_L = 12.5 pF, Gain = L5
		-	1.3	6.8		ESR=90 kΩ, C_L = 12.5 pF, Gain = L6
		-	1.6	7.7		ESR=90 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	1	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	0.5	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	90	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.5.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 5 pF ~ 20 pF range, designed for RTC applications, and selected to match the requirements of the crystal. The crystal manufacturer typically specifies a load capacitance (C_L) which is the series combination of C1, C2 and

Cstray. The Cstray, that is PCB and MCU pin capacitance, must be included (2 pF ~ 8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

The following equation gives the expression of C_L:

$$C_L = \frac{C1 \times C2}{C1 + C2} + C_{stray}$$

Since C1 = C2, then the capacitors are selected by:

$$C1 = C2 = (C_L - C_{stray}) \times 2$$

For example, C_L = 12.5 pF and Cstray = 2.5 pF, hence C1 = C2 = 20 pF

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

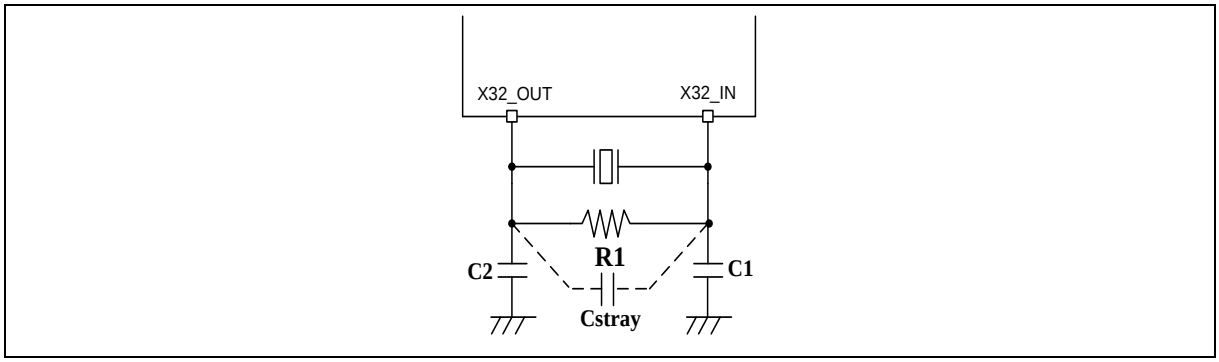
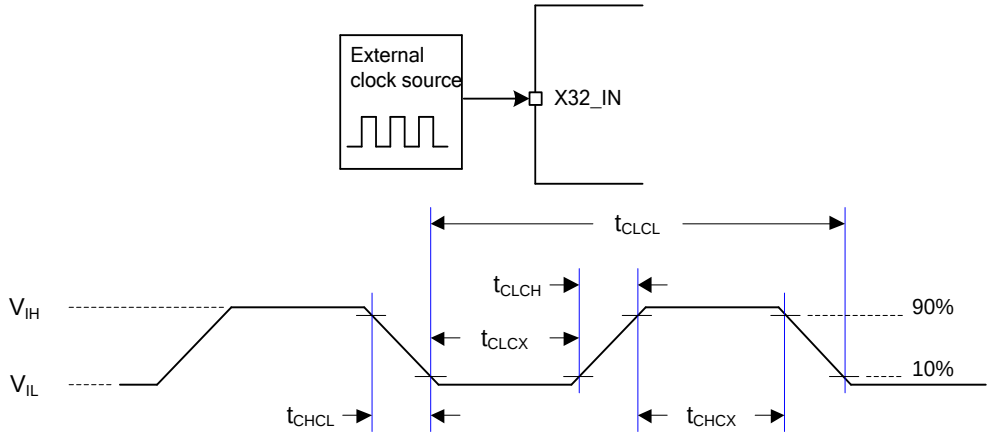


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.6 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.7 PLL Characteristics

Symbol	Parameter	Min[1]	Typ	Max[1]	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	144	MHz	
f_{PLL_REF}	PLL reference clock	0.8	-	8	MHz	
f_{PLL_VCO}	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	500	µS	
Jitter[2]	Cycle-to-cycle Jitter	-	-	350	pS	
I_{DD}	Power consumption	-	5	9	mA	f_{PLL_VCO} = 500 MHz

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-9 PLL Characteristics

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	7.62	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	5.32		C_L = 10 pF, V_{DD} >= 4.5 V
		-	12.69		C_L = 30 pF, V_{DD} >= 2.7 V
		-	9.33		C_L = 10 pF, V_{DD} >= 2.7 V
		-	13.87		C_L = 30 pF, V_{DD} >= 2.5V
		-	10.10		C_L = 10 pF, V_{DD} >= 2.5 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	6.89		C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.25		C_L = 10 pF, V_{DD} >= 4.5 V
		-	11.90		C_L = 30 pF, V_{DD} >= 2.7 V
		-	7.47		C_L = 10 pF, V_{DD} >= 2.7 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	45.95	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	69.66		C_L = 10 pF, V_{DD} >= 4.5 V
		-	27.11		C_L = 30 pF, V_{DD} >= 2.7 V
		-	39.68		C_L = 10 pF, V_{DD} >= 2.7 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	-	125	℃	
V_{DD}	Power supply	2.5	-	5.5	V	
V_{LDO}	Output voltage	1.62	1.8	1.98	V	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a C_{LDO} capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.
3. V_{LDO} is only used to supply internal power.

Table 8.5-1 LDO Characteristics

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	10	20	μA	AV_{DD} = 3.3V
I_{LVR}[*1]	LVR operating current	-	0.7	1		AV_{DD} = 3.3V
I_{BOD}[*1]	BOD operating current	-	10	20		AV_{DD} = 3.3V, Normal mode
		-	0.5	1		AV_{DD} = 3.3V, Low Power mode
V_{POR}	POR reset voltage (Falling edge)	2.1	2.2	2.3	V	
	POR reset voltage (Rising edge)	2.15	2.25	2.35		
V_{LVR}	LVR reset voltage (Falling edge)	2.15	2.25	2.35		
	LVR reset voltage (Rising edge)	2.20	2.30	2.40		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	2.27	2.30	2.40		BODVL = 0
		2.60	2.70	2.80		BODVL = 1
		3.60	3.70	3.80		BODVL = 2
		4.20	4.40	4.60		BODVL = 3
	BOD brown-out detect voltage (Rising edge)	2.28	2.38	2.48		BODVL = 0
		2.68	2.78	2.88		BODVL = 1
		3.68	3.78	3.88		BODVL = 2
		4.28	4.48	4.68		BODVL = 3
T_{LVR_SU}[*1]	LVR startup time	-	-	100	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	30	100		-

T_{BOD_SU}[*3]	BOD startup time	-	230	260		(RC38K * 9~10)
T_{BOD_RE}[*1]	BOD respond time	-	5	30		Normal mode (RC38K * 0~1)
		-	-	6000		Low Power mode (RC38K * ?)
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	µS/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		100	-	-		LVR Enabled
		20	-	-		BOD 2.3V Enabled, Normal mode
		30	-	-		BOD 2.7V Enabled, Normal mode
		50	-	-		BOD 3.7V Enabled, Normal mode
		70	-	-		BOD 4.4V Enabled, Normal mode
		1500	-	-		BOD 2.3V Enabled, Low Power mode
		3300	-	-		BOD 2.7V Enabled, Low Power mode
		9300	-	-		BOD 3.7V Enabled, Low Power mode
		13500	-	-		BOD 4.4V Enabled, Low Power mode

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.
3. Guaranteed by design, not tested in production

Table 8.5-2 Reset and Power Control Unit

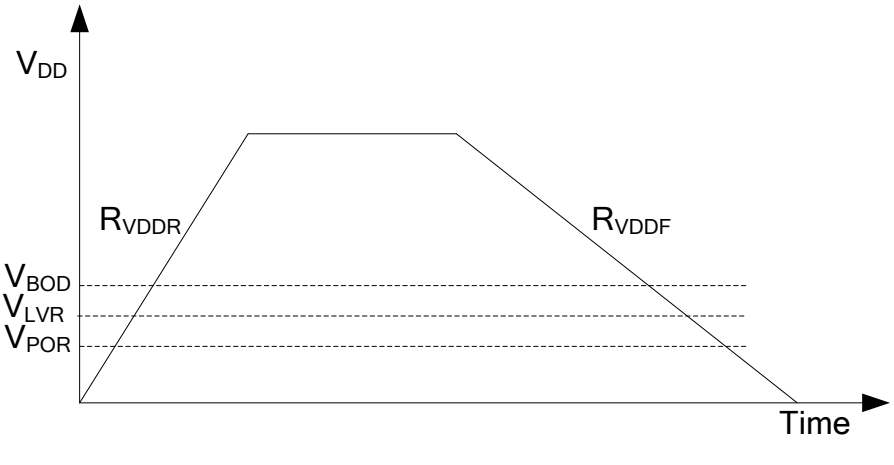


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog to Digital Converter (ADC)

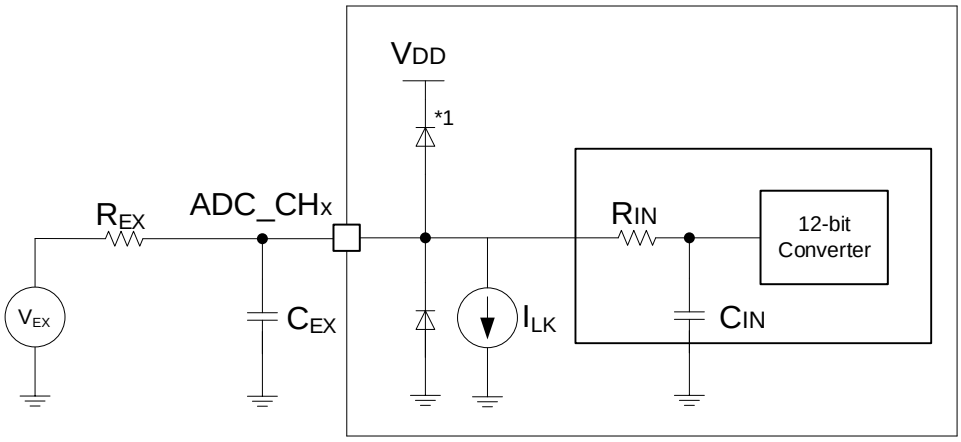
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.7	-	5.5	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	2.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	-	135	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 36 MHz $T_{CONV} = 18 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	36	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	19	-	274	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 18 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	210	-	1895	ksps	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(EADC_SCTLx[31:24])) = 0
T_{EN}	Enable to ready time	1	-	-	$1/F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-3.7	-	+3.3	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	+3.8	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits		10	-	bits	F_{ADC} = 36 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio		64	-	dB	
SNR[*1]	Signal-to-noise ratio		64	-		
C_{IN}[*1]	Internal Capacitance	-	3.6	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	400	850	Ω	

Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and *k* is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{F_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$

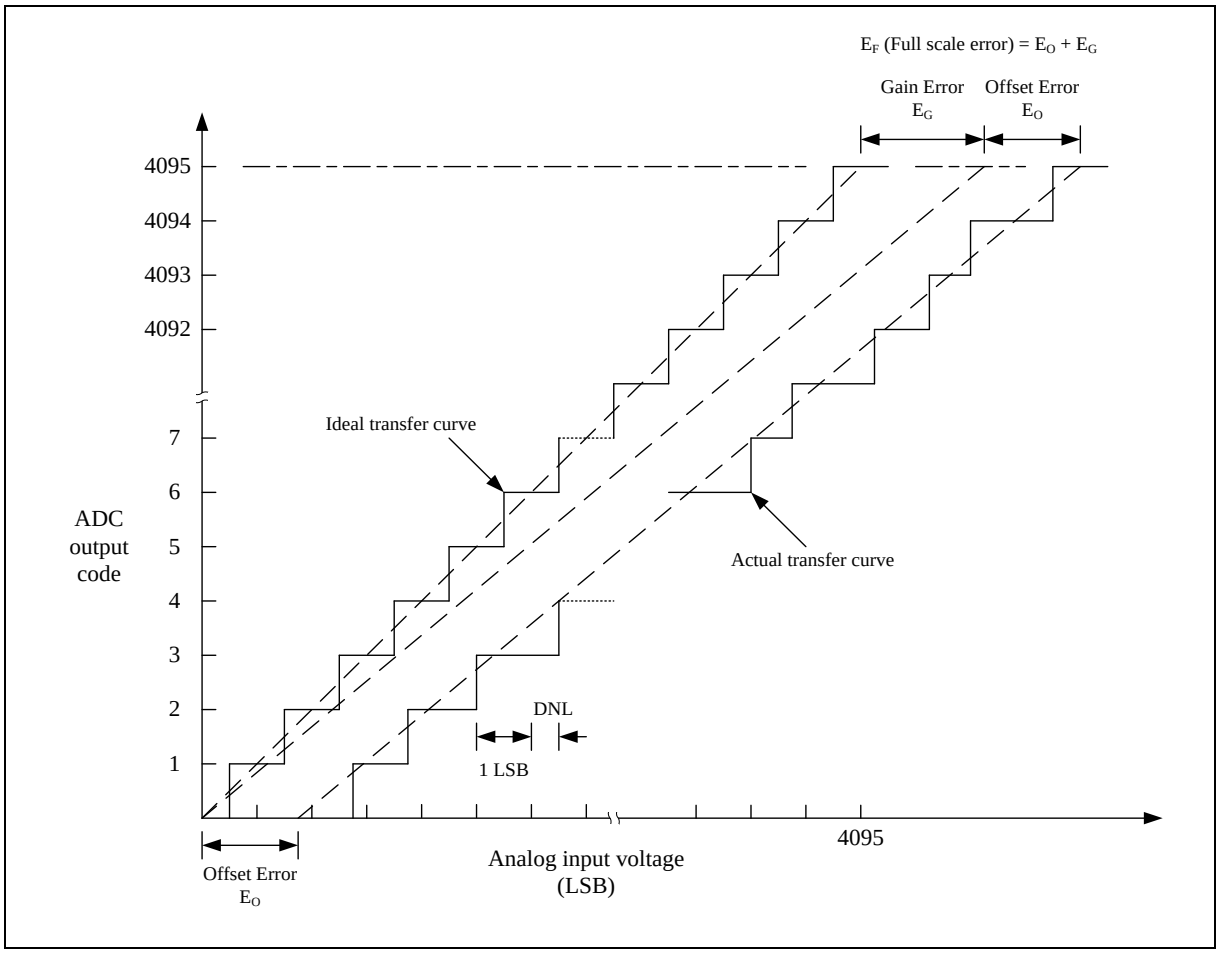
Table 8.5-3 ADC Characteristics



Note:

The internal ESD diode isn't supported between IO and V_{DD} at 5V tolerence IO pin.

Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Analog Comparator (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Analog supply voltage	2.5	-	5.5	V	
T_A	Temperature	-40	-	125	℃	
I_{ACMP}[*2]	ACMP operating current	-	75	200	μA	MODESEL = 01
V_{CM}[*2]	Input common mode voltage range	0	-	V_{DD}		
V_{DI}[*2]	Differential input voltage sensitivity	50	-	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	-	±30	mV	Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	20	-	mV	HYSSEL = 01
		-	30	60		HYSSEL = 10
		-	40	-		HYSSEL = 11
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	100	200	nS	MODESEL = 01
T_{Setup}[*2]	Setup time	-	-	5	μS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	V_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	5.8	-	kΩ	
T_{SETUP_CRV}[*1]	Setup time	-	-	0.5	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	60	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-4 ACMP Characteristics

8.5.5 Temperature Sensor

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	655	663	677	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	1.917	1.992	2.043	mV/°C	
T_S[*2]	Stable time	-	-	1	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	-	15	20	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	30	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Analog supply voltage	2.5	-	3.6	V	
T_A	Temperature	-40	-	125	°C	
I_{TEMP}	Temperature Sensor operating current	-	200	-	µA	
T_{ACC}	Temperature Accuracy	-	±1	±2	°C	
T_R	Temperature Resolution	-	0.0625	-	°C	
T_{CONV}	Conversion Time	-	84	100	mS	

Note:

1. Guaranteed by characterization, not tested in production

Table 8.5-5 Temperture Sensor Characteristics

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	58	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	34		2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	2	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	2	nS	2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-1 SPI Master Mode Characteristics

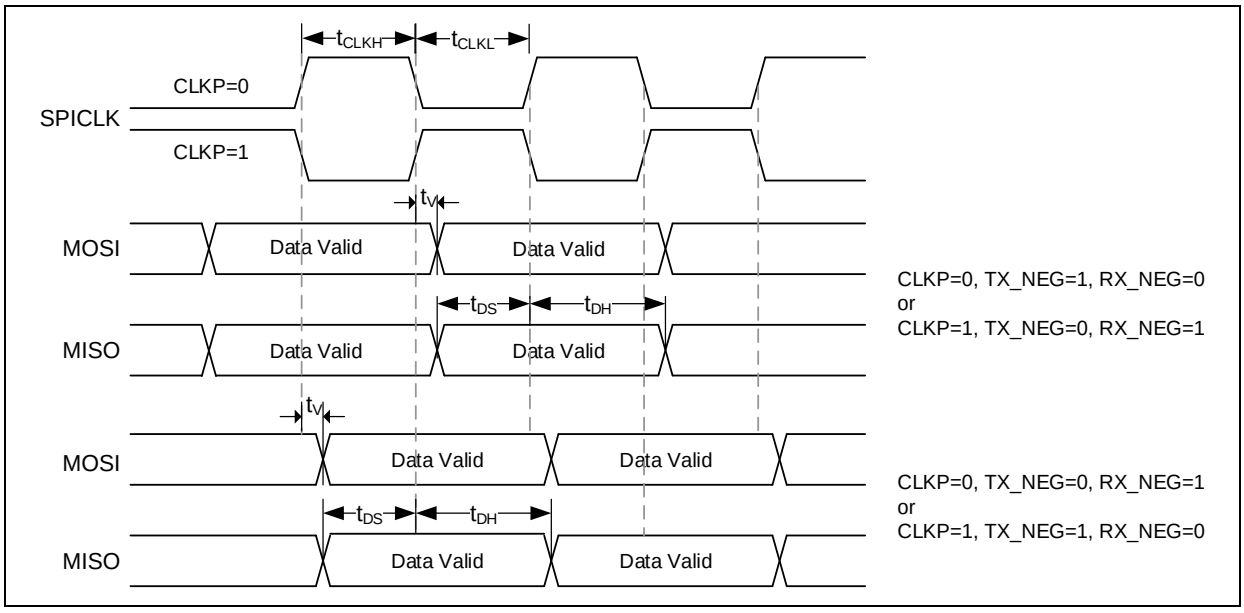


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	18.5	MHz	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	12.8		2.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 2ns	-	-		2.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	27	nS	4.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF
		-	-	39		2.5 V ≤ VDD ≤ 5.5 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-2 SPI Slave Mode Characteristics

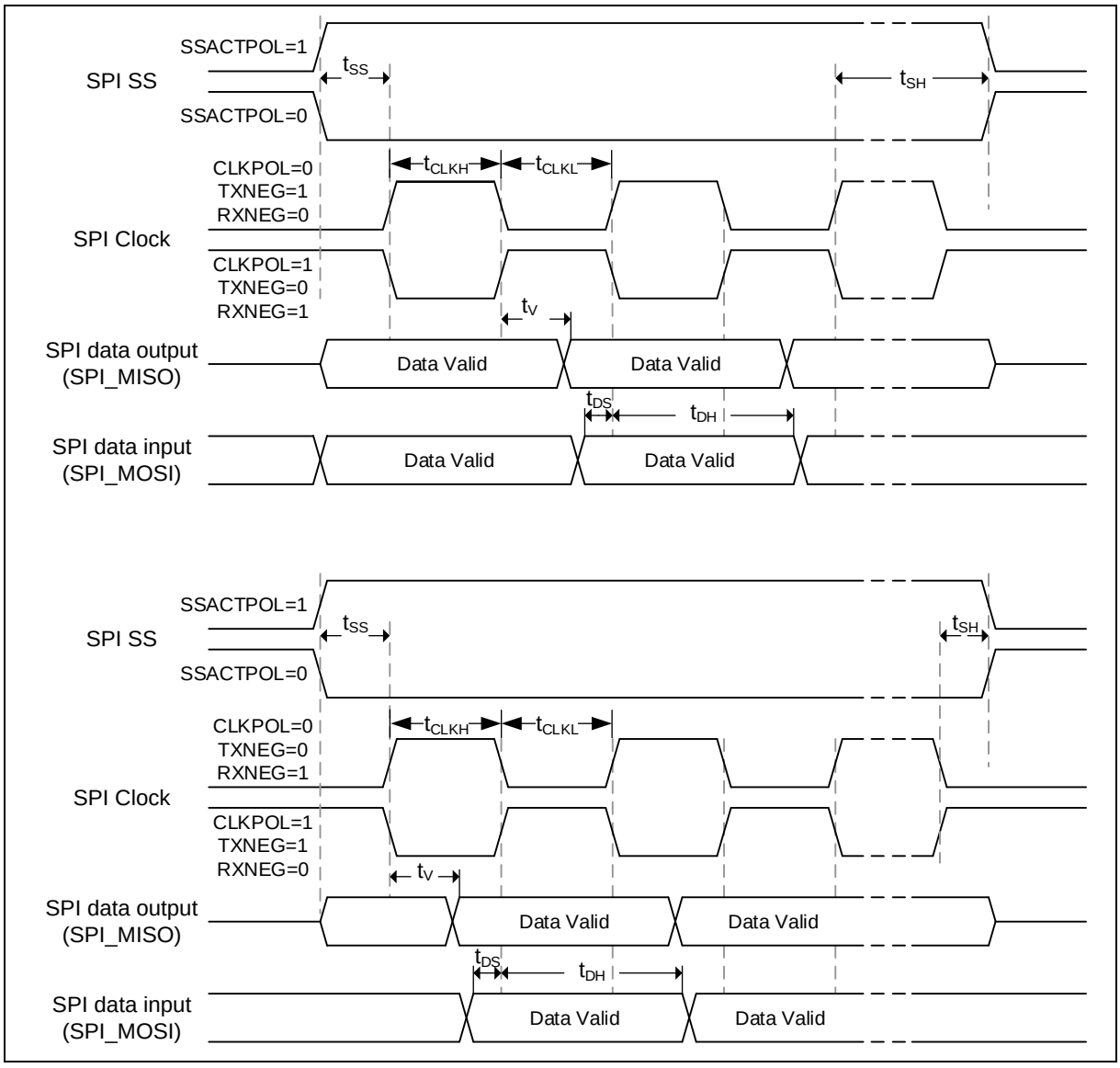


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 I²C Characteristics

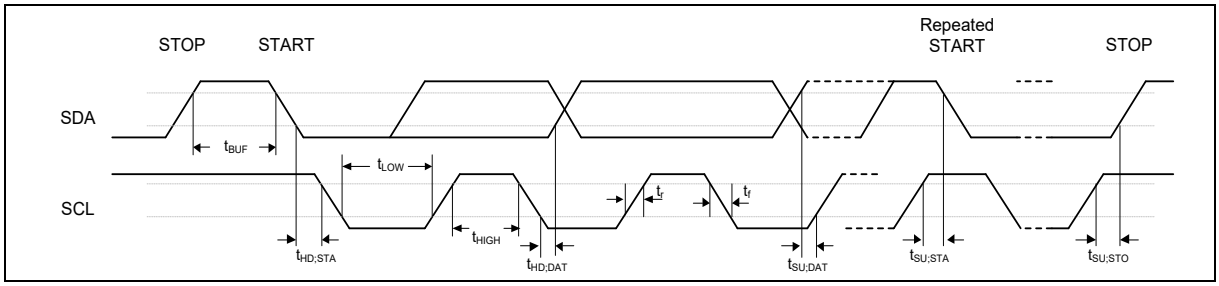


Figure 8.6-3 I²C Timing Diagram

8.6.3 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [1]	Typ	Max[1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	36	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	34		2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	1.5	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	1.5	nS	2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-4 USCI-SPI Master Mode Characteristics

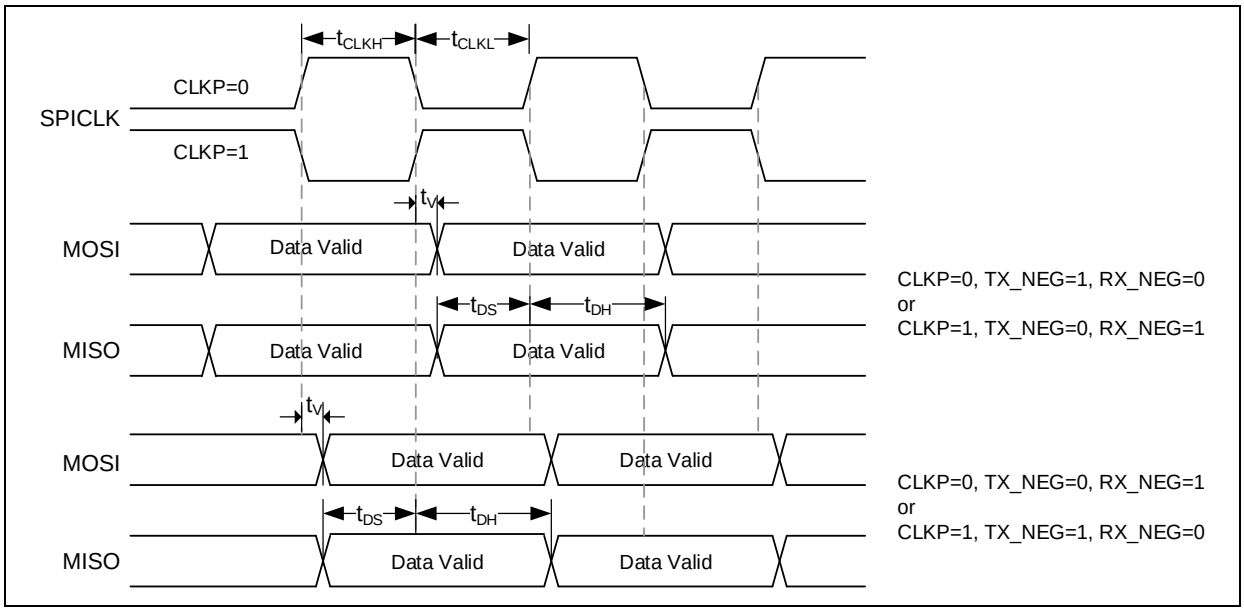


Figure 8.6-4 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	14.4	MHz	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	14.4		2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	TBD	-	-	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		TBD	-	-		2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	TBD	-	-	nS	
t_{DS}	Data input setup time	TBD	-	-	nS	
t_{DH}	Data input hold time	TBD	-	-	nS	
t_V	Data output valid time	-	-	54	nS	4.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
		-	-	54		2.5 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-5 USCI-SPI Slave Mode Characteristics

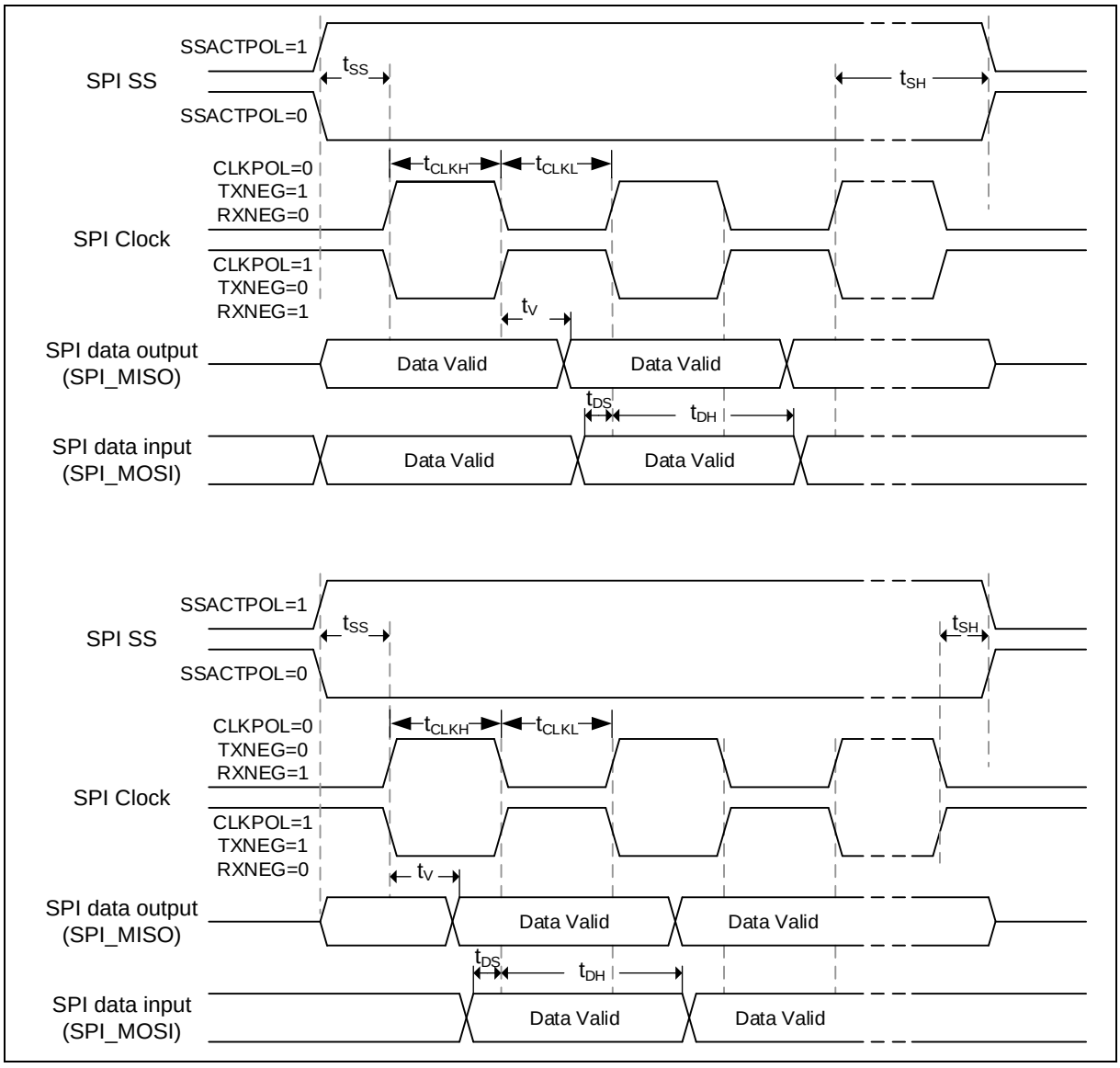


Figure 8.6-5 USCI-SPI Slave Mode Timing Diagram

8.6.4 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-6 USCI-I²C Characteristics

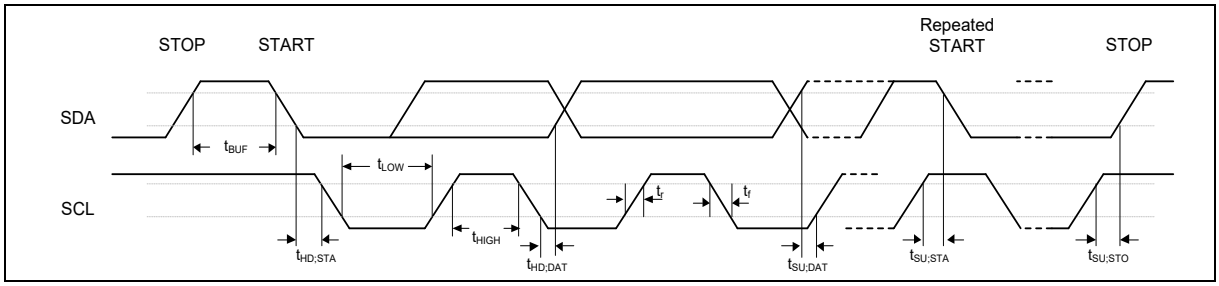


Figure 8.6-6 USCI-I²C Timing Diagram

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.62	1.8	1.98	V	T_A = 25°C
T_{ERASE}	Page erase time	-	20	-	ms	
T_{PROG}	Program time	-	60	-	µs	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Endurance	20,000	-		cycles[2]	T_J = -40°C~125°C
T_{RET}	Data retention	10	-	-	year	20 kcycle[3] T_J = 85°C
		2	-	-	year	20 kcycle[3] T_J = 105°C

Note:

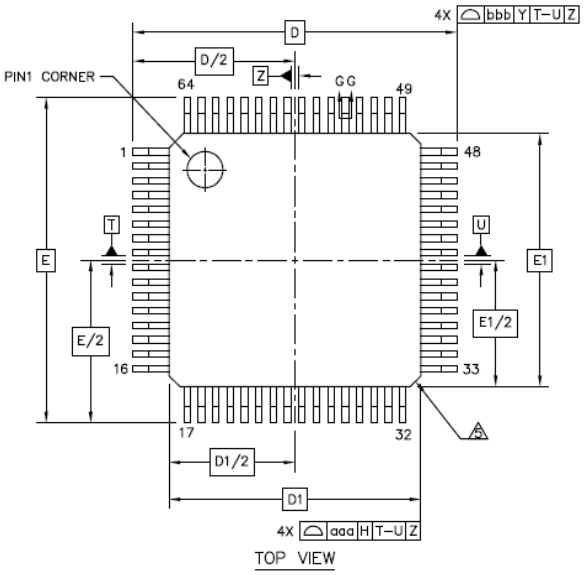
1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.

Table 8.7-1 Flash DC Electrical Characteristics

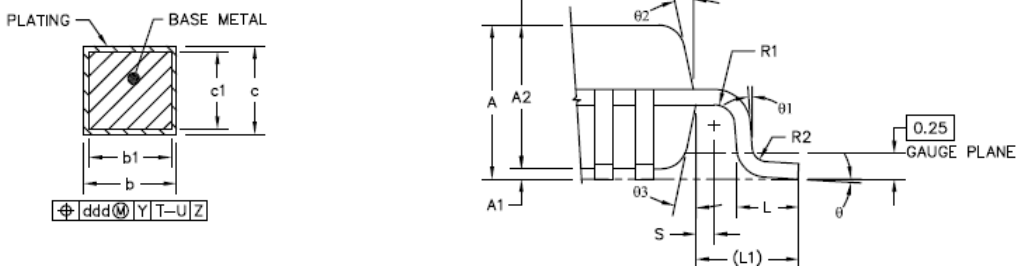
9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

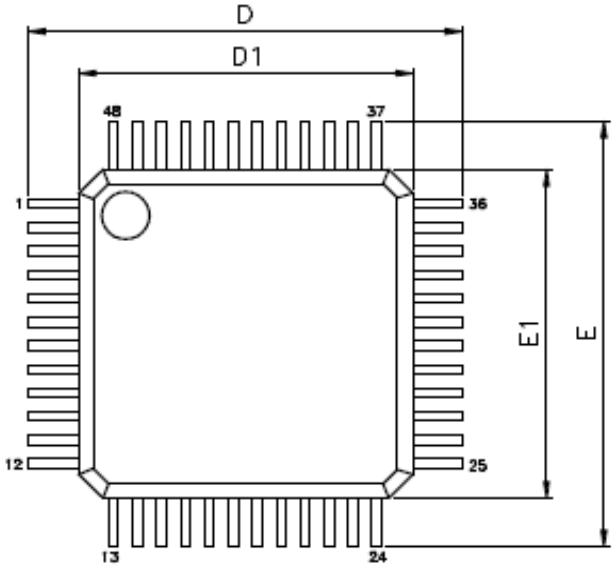
9.1 LQFP 64L (7x7x1.4 mm footprint 2.0 mm)

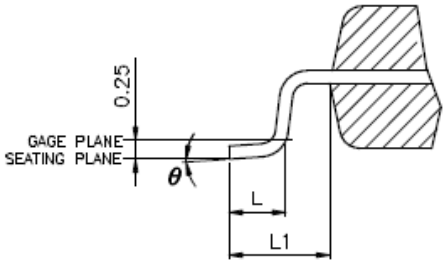


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		



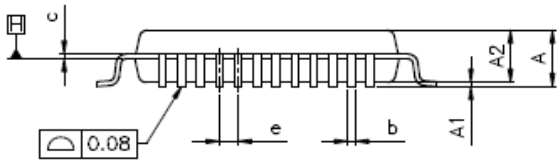
9.2 LQFP 48L (7x7x1.4 mm footprint 2.0 mm)



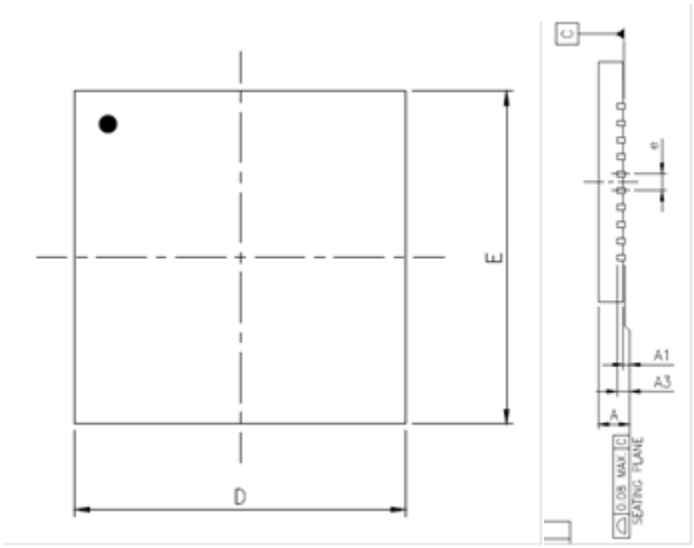


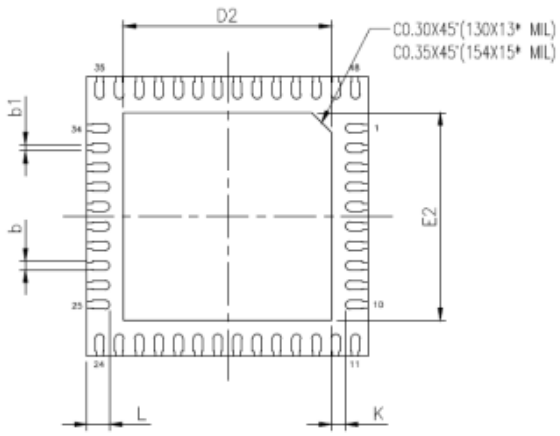
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°



9.3 QFN 48L (5x5x0.8mm, EP Size: 3.7x3.7mm)





SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
130X13* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45
154X15* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
DAP	Debug Access Port
DES	Data Encryption Standard
EBI	External Bus Interface
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	22.1184 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SD	Secure Digital

SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2025.03.05	1.00	Initial version.

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