NuMicro® Family

Arm® Cortex®-M23-based Microcontroller

M253xx3BE Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® M253xx3BE series 32-bit microcontroller is based on Arm® Cortex®-M23 core using Armv8-M architecture. It runs up to 48 MHz and features up to 128 Kbytes Flash, 16 Kbytes SRAM, 1.75V ~ 5.5V wide operating voltage, and -40°C to +105°C operating temperature.

Crystal-less USB 2.0 full speed device interface

The M253xx3BE series includes a crystal-less USB 2.0 full speed device supports maximum 1 Kbytes buffer size, provides up to 17 configurable endpoints, up to 5 VCOMs for configurable Isochronous, Bulk, Interrupt and Control transfer types.

UART interface

The M253xx3BE series supports up to 5 sets of UART with RS-485 and IrDA mode. The data payloads of 4 UARTs is equipped with 16/16 bytes entry FIFO for both receive and transmit side. The UART interfaced support flow control and PDMA mode.

CAN FD interface

One set of CAN FD interface, eligible for automotive related and industrial automation applications, is supported.

Rich Pheripherals for comprehensive product application scenarios

The M253xx3BE series provides plenty of peripherals such as Timers, Watchdog Timers, PDMA, up to 5 sets of UART, 2 sets of I^2C, 1 set of SPI/I^2S, Universal Serial Control Interface (USCI), and 6 channels of 16-bit PWM. It also includes high performance analog front-end circuit blocks, such as 12 channels of 12-bit 840 kSPS ADC, and a temperature sensor to enhance product performance, to reduce external components and form factor simultaneously.

Supported packages from QFN33 (5mm x 5mm) to LQFP48 (7mm x 7mm) with pin-compatible for different part numbers make the system design and parts change easily.

For the development, Nuvoton provides the NuMaker M253BE evaluation boards and Nu-Link debugger. The 3rd Party IDEs such as Keil® MDK, IAR EWARM and Eclippse IDE with GNU GCC compilers, are also supported.

USCI*: supports UART, SPI or I^2C

Product Line	UART	I^2C	SPI/I^2S	USCI*	USBD	CAN FD	Timer	PDMA	ADC	PWM
M253xx3BE	5	2	1	1	1	1	4	5	12	6

Table 3.1-1 NuMicro® M253xx3BE Series Key Features Support Table

The NuMicro® M253xx3BE series is suitable for a wide range of applications such as:

- USB Bridge
- Data Collector
- Battery Management System
- Automotive Related Module

2 FEATURES

Core and System	
Arm® Cortex®-M23 without TrustZone®	• Arm® Cortex®-M23 processor, running up to 48 MHz when V_{DD} = 1.75V ~ 5.5V • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access • Supports XOM feature with 1 region
Low power mode and current	• Low Power mode: – Idle mode • Power-down mode (PD) – Fast Wake-up Power-down mode (FWPD)
Wake-up source and wakeup time	• USCI, RTC, WDT, I^2C, Timer, UART, BOD, LVR, POR, GPIO, USBD, Debug interface, NMI and Reset pin from Power-down mode or Fast Wake-up Power-down mode
Power supply and low voltage detect	• Built-in LDO for wide operating voltage from 1.75V to 5.5V • Core power voltage: 1.5V • Brown-out detector – With 7 levels: 4.4V/3.7V/3.0V/2.7V/2.4V/2.0V/1.8V – Supports Brown-out Interrupt and Reset option • Low Voltage Reset – Threshold voltage levels: 1.55V
Cyclic Redundancy Calculation Unit	• Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 • Programmable order reverse setting for input data and CRC checksum • Programmable 1's complement setting for input data and CRC checksum. • Supports 8-/16-/32-bit of data width • Programmable seed value

	• 8-bit write mode: 1-AHB clock cycle operation • 16-bit write mode: 2-AHB clock cycle operation • 32-bit write mode: 4-AHB clock cycle operation • Supports using PDMA to write data to perform CRC operation
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• Up to 128 KB application ROM (APROM) • 4 KB Flash for user program loader (LDROM) • Up to 48 MHz with zero wait state for consecutive address read access • 12 bytes User Configuration Block to control system initiation. • 512B page erase for all embedded Flash • 32-bit and multi-word Flash programming function. • Supports In-System-Programming (ISP), In-Application-Programming (IAP) update embedded Flash memory • Supports CRC-32 checksum calculation function • Supports Flash all one verification function (hardware can check page erase verify) • Hardware external read protection of whole Flash memory by Security Lock Bit • Supports XOM feature with 1 region
SRAM	• 16 KB embedded SRAM • Supports byte-, half-word- and word-access • Supports PDMA mode
Peripheral DMA (PDMA)	• Up to 5 independent configurable channels for automatic data transfer between memories and peripherals • Channel 0, 1 support time-out function • Basic and Scatter-Gather Transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Two types of priorities modes: Fixed-priority and Round-robin modes • Transfer data width of 8, 16, and 32 bits • Single and burst transfer type • Source and destination address can be increment or fixed

	• PDMA transfer count up to 65536 • Request source form software, PSIO, SPI/I²S, UART, USCI, EADC, DAC, PWM capture event or TIMER
Clocks	
Clock Source	• Built-in 4.032 MHz internal high speed RC oscillator (MIRC) for system operation • Built-in 48 MHz internal high speed RC oscillator (HIRC) for system operation • Built-in 38.4 kHz internal low speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation. • Built-in 4~32 MHz external high speed crystal oscillator (HXT) for precise timing operation • Built-in 32.768 kHz external low speed crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock on-the-fly switch • Supports clock failure detection for high/low speed external crystal oscillator • HXT clock frequency accuracy detector • Supports exception (NMI) generated once a clock failure detected • Supports divided clock output
Timers	
32-bit Timer	**TIMER mode** • 4 sets of 32-bit timers with 24-bit up counters and 8-bit prescale counters • Independent clock source for each timer • One-shot, Periodic, Toggle and Continuous Counting operation modes • Event counting function to count the event from external pin • Input capture function to capture or reset counter value • External capture pin event for interval measurement. • External capture pin event to reset 24-bit up counter. • Chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag to trigger BPWM, EADC and PDMA. • Inter-Timer trigger capture mode
BPWM	• Supports maximum clock frequency up to 96 MHz • Each module provides 6 output channels

	• Supports independent mode for BPWM output/Capture input channel • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution BPWM counter, each module provides 1 BPWM counter – Up, down or up/down counter operation type • Supports mask function and tri-state enable for each BPWM pin • Supports interrupt on the following events: – BPWM counter match 0, period value or compared value • Supports trigger ADC on the following events: – BPWM counter match 0, period value or compared value • Capture Function Features – Up to 6 capture input channels with 16-bit resolution – Supports rising or falling capture condition – Supports input rising/falling capture interrupt – Supports rising/falling capture with counter reload option
Watchdog	• 20-bit free running up counter for WDT time-out interval • Clock sources from LIRC (default), HCLK/2048 or LXT • 9 selectable time-out period from 488us ~ 32 sec • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out • Selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Force WDT enabled after chip power on or reset. • WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
Window Watchdog	• Clock sources from HCLK/2048 (default) or LIRC • Window set by 6-bit down counter with 11-bit prescaler • WWDT counter suspends in Idle/Power-down mode • Supports Interrupt
RTC	• Software compensation by setting frequency compensate register (FCR),compensated clock accuracy reaches ±5ppm within 5 seconds • RTC counter (second, minute, hour) and calendar counter (day, month, year) • Alarm registers (second, minute, hour, day, month, year) • Selectable 12-hour or 24-hour mode

	• Automatic leap year recognition • Day of the Week counter • Daylight Saving Time software control • Periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 or 1 second • 1 Hz clock output for RTC calibration • Wake-up from idle mode and Power-down mode • 32 kHz oscillator gain control • RTC Time Tick and Alarm Match interrupt
Analog Interfaces	
EADC	• Conversion results held in 19 data registers with valid and overrun indicators. • Analog input voltage: 0~AV_{DD}. • Reference voltage from AV_{DD} • 12-bit resolution and 10-bit accuracy guaranteed • Up to 12 single-end analog external input channels • Supports 2 internal channels: – Band-gap VBG output – Temperature sensor input • Four ADC interrupts (ADINT0~3) with individual interrupt vector addresses. • ADC clock frequency up to 16 MHz. • Up to 730 KSPS conversion rate. • Configurable ADC internal sampling time • Up to 4 sample modules – Each of sample module 0~3 which is configurable for ADC converter channel – EADC_CH0~3 and trigger source. – Configurable PDMA – Configured resolution for 12-bit or 16-bit result – Supports Left-adjusted result – Averaging and oversampling (2^n times, n=0~8) to support up to 16-bit result – Configurable sampling time for each sample module. – Conversion results held in 19 data registers with valid and overrun indicators. • Supports digital comparator to monitor conversion result that can be under or over the compare register setting

	• Generate an interrupt when conversion result matches the compare register setting. • An A/D conversion can be started by: – Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18) – External pin STADC – Timer0~3 overflow pulse triggers – ADINT0/1 interrupt EOC (End of conversion) pulse triggers – BPWM triggers • Supports PDMA transfer • Auto turn on/off ADC power at power down or operation mode with wait state
Communication Interfaces	
UART	• Supports up to 5 UARTs: UART0, UART1, UART2, UART3, and UART4 • UART clock source can be from LIRC • UART baud rate clock from LXT(32.768 kHz) with 9600bps in Power-down mode • Baud rate up to 10 Mbps • Full-duplex asynchronous communications • Supports one-wire half-duplex communications • Separates receive and transmit 16/16 bytes FIFO • Programmable receiver buffer trigger level • Hardware auto-flow control (CTS and RTS) • IrDA (SIR) function – Supports 3/16 bit duration for normal mode • RS-485 9-bit mode and direction control • Programmable baud-rate generator up to 1/16 system clock • 8-bit receiver FIFO time-out detection function • Separates receive and transmit 16/16 bytes FIFO (Supported by UART0~UART3) • Programmable transmitting data delay time between the last stop and the next start bit • Auto-Baud Rate measurement and baud rate compensation function • Break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports RS-485 mode: – RS-485 9-bit mode

	– Hardware or software enables to program nRTS pin to control RS-485 transmission direction – nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in Power-down mode. – Hardware or software enables to program nRTS pin to control RS-485 transmission direction • Fully programmable serial-interface: – Programmable number of data bit, 5-, 6-, 7-, 8- bit character – Programmable parity bit, even, odd, no parity or stick parity bit generation and detection – Programmable stop bit, 1, 1.5, or 2 stop bit generation • Supports PDMA mode
SPI	• Supports Master or Slave mode operation • Master and slave mode up to 25 MHz (when chip works at V_{DD} = 3.0 ~ 5.5V) • Supports 2-bit Transfer mode • Supports Dual and Quad I/O Transfer mode • Configurable bit length of a transaction word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports Byte Reorder function • Supports Byte or Word Suspend mode • Supports PDMA transfer • Supports 3-Wire, no slave selection signal, bi-direction interface • Supports one data channel half-duplex transfer • Supports receive-only mode
I^2C	• Up to 2 sets of I^2C device • Master/Slave mode • Bidirectional data transfer between masters and slaves • Multi-master bus (no central master) • 7-bit and 10-bit addressing mode • Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps) • Arbitration between simultaneously transmitting masters without corruption of serial data on the bus • Serial clock synchronization allows devices with different bit rates to communicate via one serial bus • Serial clock synchronization can be used as a handshake

	mechanism to suspend and resume serial transfer • Supports 14-bit time-out counter requesting the I^2C interrupt if the I^2C bus hangs up and timer-out counter overflows • Programmable clocks allow versatile rate control • Multiple address recognition (four slave address with mask option) • Supports setup/hold time programmable • Multi-address Power-down wake-up function • Supports PDMA transfer
SPI/I2S	**SPI Mode** • Up to 1 set of SPI controller • Master or Slave mode operation • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers which depended on SPI setting of data width • MSB first or LSB first transfer sequence • Supports byte reorder function • Byte or Word Suspend mode • Master and slave mode up to 25 MHz (V_{DD} = 3.0V ~5.5V) • Supports one data channel half-duplex transfer • Supports receive-only mode • Supports PDMA transfer **I^2S Mode** • Up to 1 sets of I^2S by SPI controllers • Interface with external audio CODEC • Supports Master and Slave mode • Capable of handling 8-, 16-, 24- and 32-bit word sizes • Mono and stereo audio data • PCM mode A, PCM mode B, I^2S and MSB justified data format • Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving • Generates interrupt requests when buffer levels cross a programmable boundary • Each supports two PDMA requests, one for transmitting and the other for receiving
Universal Serial Control Interface (USCI)	• Up to 1 set of USCI • Supports UART, SPI and I^2C function

	• Single byte TX and RX buffer mode **USCI_UART** • One transmit buffer and two receive buffer for data payload • Hardware auto flow control function and programmable flow control trigger level • Programmable baud-rate generator • Supports 9-bit data transfer • Baud rate detection by built-in capture event of baud rate generator • Supports Wake-up function (Data and nCTS Wakeup Only) • Supports PDMA transfer **USCI_SPI** • Master or Slave mode operation • Configurable bit length of a transfer word from 4 to 16-bit • One transmit buffer and two receive buffer for data payload • MSB first or LSB first transfer sequence • Word suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Wake-up function: input slave select transition • Supports one data channel half-duplex transfer **USCI_I²C** • Full master and slave device capability • 7-bit/10-bit addressing mode • Communication in Standard mode (100 kbps), Fast mode (up to 400 kbps) and Fast mode plus (1 Mbps) • Multi-master bus • One transmit buffer and two receive buffer for data payload • 10-bit bus time out capability • Supports Bus monitor mode • Wake-up by data toggle or address match in Power-down mode • Multiple address recognition • Setup/hold time programmable
GPIO	• Four I/O modes: – Quasi bi-direction – Push-Pull output

	– Open-Drain output – Input only with high impendence • TTL/Schmitt trigger input selectable • I/O pin configured as interrupt source with edge/level trigger setting • Independent pull-up/pull-down control • High driver and high sink current I/O (up to 16 mA at 5V, 25°C) • Minimum I/O Speed – 25 MHz when V_{DD} = 2.7 ~ 5.5 V (-40°C ~ +105°C, CL=35p, high skew rate enabled) – 10 MHz when V_{DD} = 1.75 ~ 5.5 V (-40°C ~ +105°C, CL=35p, high skew rate enabled) • Software selectable slew rate control • Supports wake-up function • Supports I/O de-bounce with LIRC at power down • I/O configurations of multi-function pin are controlled by module or MFOS register settings.
Advanced Connectivity	
USB 2.0 Full Speed	• Compliant with USB 2.0 Full-Speed specification • Provides 1 interrupt vector with 4 different interrupt events (NEVWK, VBUSDET, USB and BUS) • Suspend function when no bus activity exists for 3 ms • Supports 17 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1024 bytes buffer size • Provides remote wake-up capability • Start of Frame (SOF) locked clock pulse generation • Supports USB 2.0 Link Power Management (LPM) • Supports Crystal-less function
CAN-FD	• Supports protocol version 2.0 part A, B and ISO 11898-1:2015 • Up to 64 data bytes supported • Supports CAN Error Logging • Supports AUTOSAR and J1939 • Two Receive FIFOs of three payloads each (up to 64 Bytes per payload) • Separate signaling on reception of High Priority Messages • Configurable Transmit FIFO / queue of three payload (up to 64

	Bytes per payload) • Support programmable loop-back test mode • Support maskable module interrupts • Support Power-down

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

Part No.	TSSOP20	TSSOP28	QFN33	LQFP48	LQFP64	LQFP80	LQFP128
M253xx3BE_64K				M253LD3BE			
M253xx3BE_128K			M253ZE3BE	M253LE3BE			

3.2 M253xx3BE Selection Guide

PART NUMBER		M253ZE3BE	M253LD3BE	M253LE3BE
Flash (KB)		128	64	128
SRAM (KB)		16	16	16
LDROM (KB)		4		
I/O		22	37	
32-bit Timer		4		
WDT/WWDT		√		
LXT		√		
RTC		√		
PWM		6		
Connectivity	USCI*	1		
	UART	5		
	SPI/I²S	1		
	I²C	2		
	CAN FD	1		
	USB 2.0 FS	1		
PDMA		5		
EBI		-		
CRC		√		
PLL(MHz)		-		
ISO-60730		√		
ACMP		2		
12-bit 840 kSPS SAR ADC		10	12	
Package		QFN33	LQFP48	

3.3 M253xx3BE Selection Code

M2	53	L	E	3	B	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex-M2	53: USB, CAN FD	Z: QFN33 (5x5 mm) L: LQFP48 (7x7 mm)	D: 64 KB E: 128 KB	3: 16 KB		E:-40˚C ~ 105˚C

4 PIN CONFIGURATION

Users can find pin configuration information in the M253xx3BE Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 Pin Configuration

4.1.1 M253xx3BE Pin Diagram

4.1.1.1 M253xx3BE QFN 33-Pin Diagram

Corresponding Part Number: M253ZE3BE

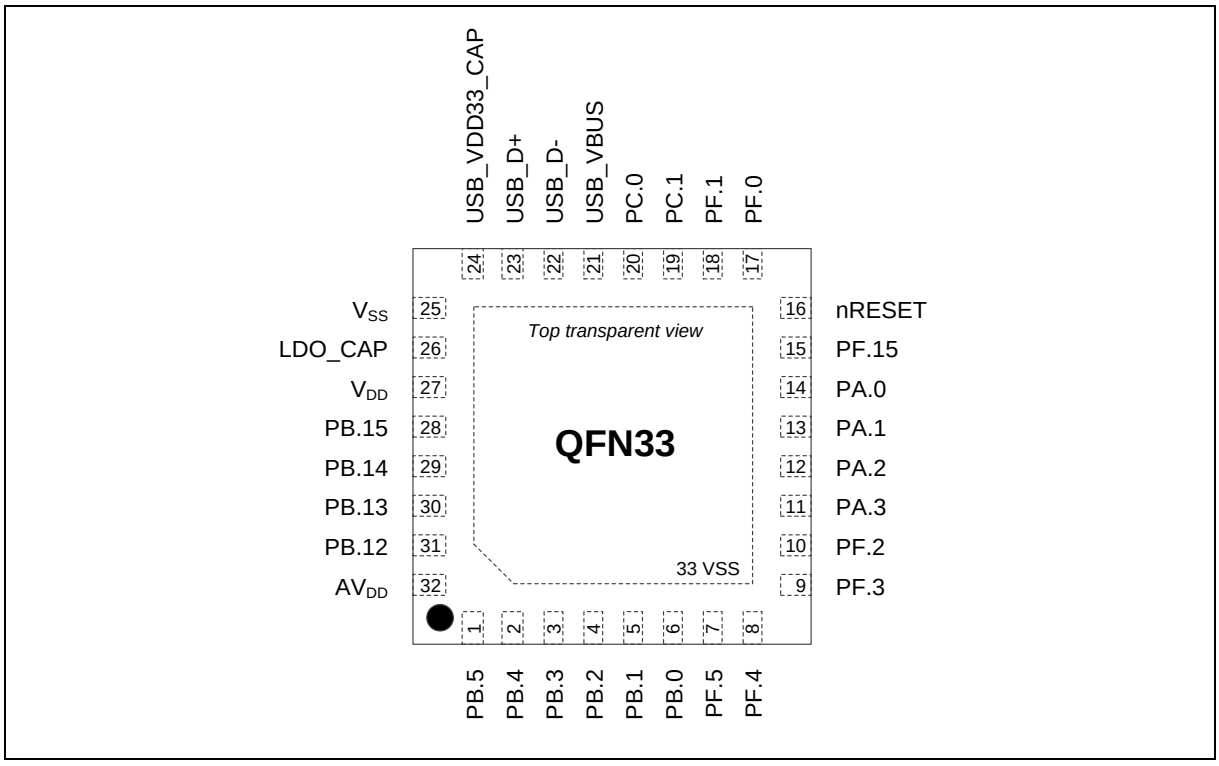


Figure 4.1-1 M253xx3BE QFN 33-pin Diagram

4.1.1.2 M253xx3BE LQFP 48-Pin Diagram

Corresponding Part Number: M253LD3BE, M253LE3BE

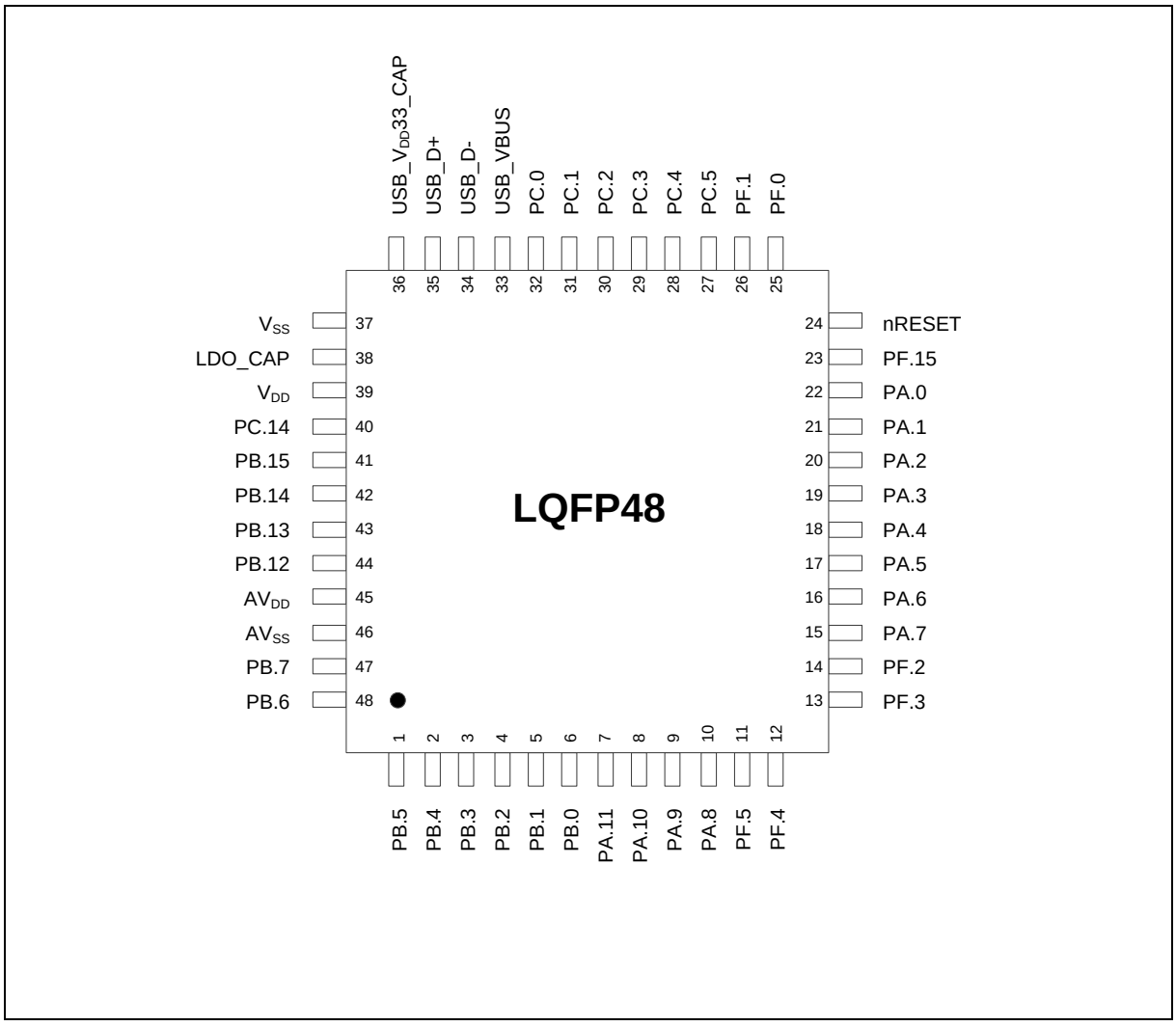


Figure 4.1-2 M253xx3BE LQFP 48-pin Diagram

4.1.2 M253xx3BE Multi-function Pin Diagram

4.1.2.1 M253xx3BE QFN 33-Pin Multi-function Pin Diagram

Corresponding Part Number: M253ZE3BE

M253ZE3BE

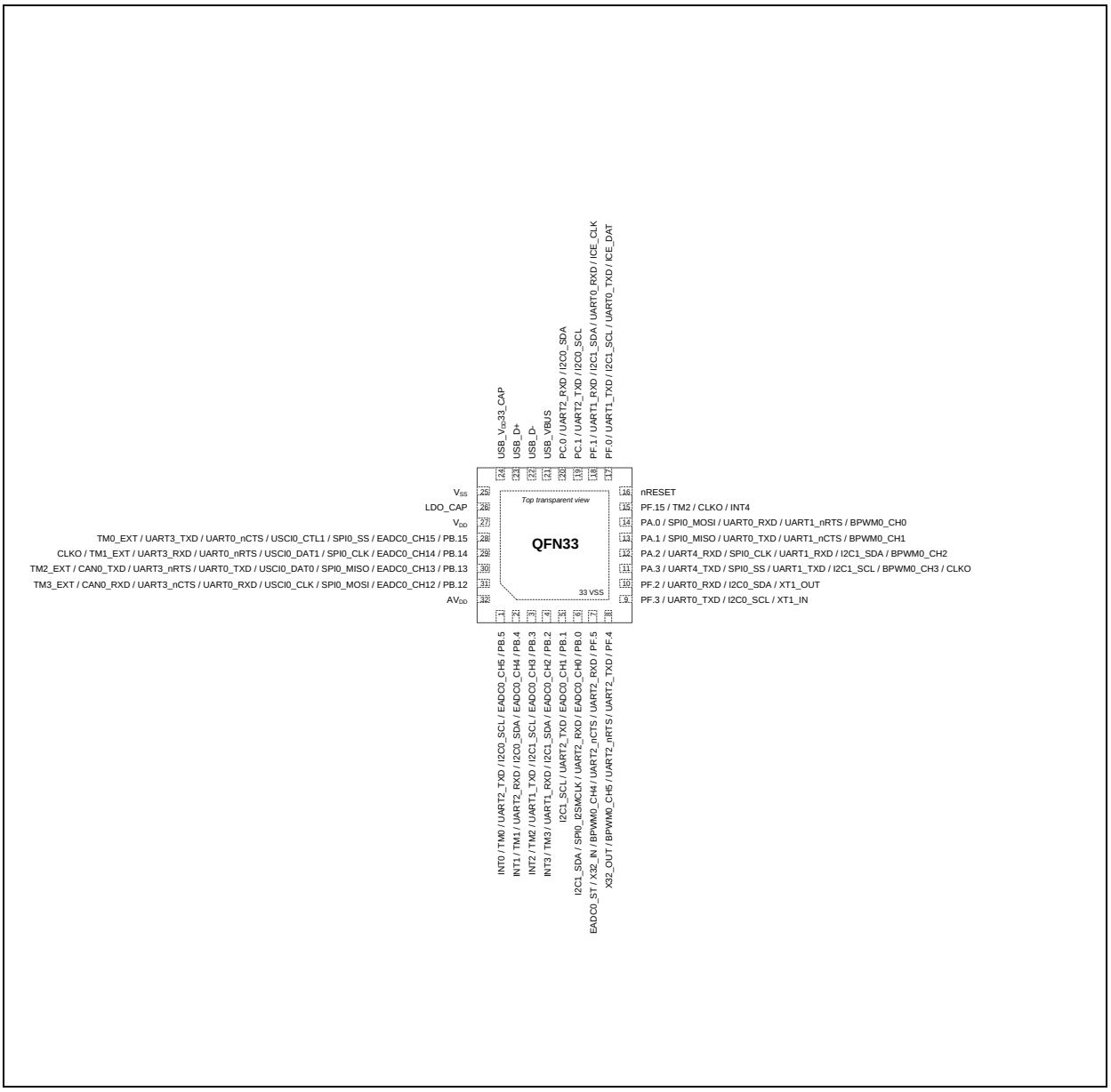


Figure 4.1-3 M253ZE3BE Multi-function Pin Diagram

Pin	M253ZE3BE Pin Function
1	PB.5 / EADC0_CH5 / I2C0_SCL / UART2_TXD / TM0 / INT0
2	PB.4 / EADC0_CH4 / I2C0_SDA / UART2_RXD / TM1 / INT1
3	PB.3 / EADC0_CH3 / I2C1_SCL / UART1_TXD / TM2 / INT2

Pin	M253ZE3BE Pin Function
4	PB.2 / EADC0_CH2 / I2C1_SDA / UART1_RXD / TM3 / INT3
5	PB.1 / EADC0_CH1 / UART2_TXD / I2C1_SCL
6	PB.0 / EADC0_CH0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
7	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
8	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
9	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
10	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
11	PA.3 / UART4_TXD / SPI0_SS / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
12	PA.2 / UART4_RXD / SPI0_CLK / UART1_RXD / I2C1_SDA / BPWM0_CH2
13	PA.1 / SPI0_MISO / UART0_TXD / UART1_nCTS / BPWM0_CH1
14	PA.0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0
15	PF.15 / TM2 / CLKO / INT4
16	nRESET
17	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
18	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
19	PC.1 / UART2_TXD / I2C0_SCL
20	PC.0 / UART2_RXD / I2C0_SDA
21	USB_VBUS
22	USB_D-
23	USB_D+
24	USB_VDD33_CAP
25	V_{SS}
26	LDO_CAP
27	V_{DD}
28	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / TM0_EXT
29	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / TM1_EXT / CLKO
30	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CAN0_TXD / TM2_EXT
31	PB.12 / EADC0_CH12 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CAN0_RXD / TM3_EXT
32	AV_{DD}

Table 4.1-1 M253ZE3BE Multi-function Pin Table

4.1.2.2 M253xx3BE LQFP 48-Pin Multi-function Pin Diagram

Corresponding Part Number: M253LD3BE, M253LE3BE

M253LD3BE/M253LE3BE

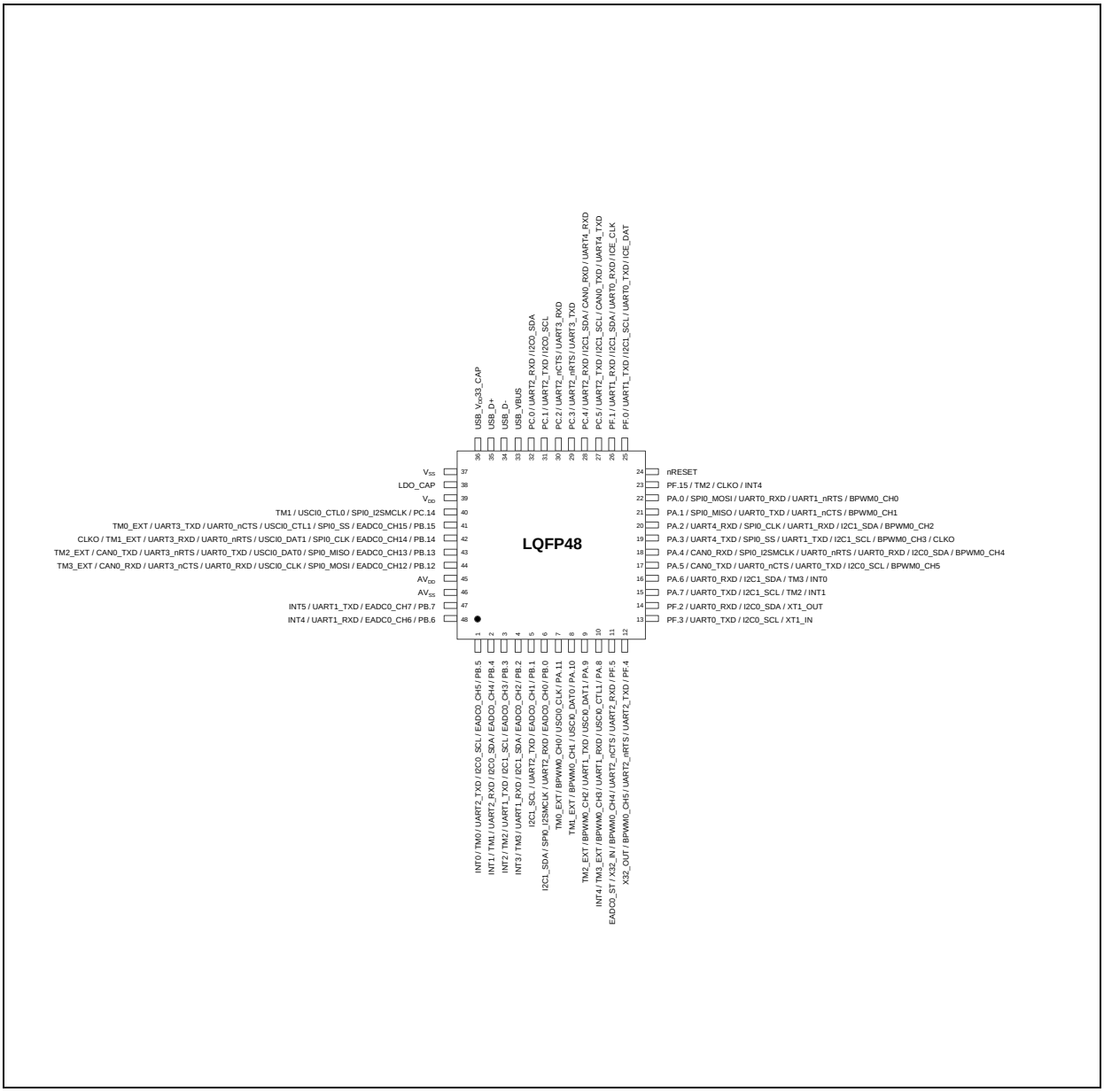


Figure 4.1-4 M253LD3BE/M253LE3BE Multi-function Pin Diagram

Pin	M253LD3BE / M253LE3BE Pin Function
1	PB.5 / EADC0_CH5 / I2C0_SCL / UART2_TXD / TM0 / INT0
2	PB.4 / EADC0_CH4 / I2C0_SDA / UART2_RXD / TM1 / INT1
3	PB.3 / EADC0_CH3 / I2C1_SCL / UART1_TXD / TM2 / INT2
4	PB.2 / EADC0_CH2 / I2C1_SDA / UART1_RXD / TM3 / INT3

Pin	M253LD3BE / M253LE3BE Pin Function
5	PB.1 / EADC0_CH1 / UART2_TXD / I2C1_SCL
6	PB.0 / EADC0_CH0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA
7	PA.11 / USCI0_CLK / BPWM0_CH0 / TM0_EXT
8	PA.10 / USCI0_DAT0 / BPWM0_CH1 / TM1_EXT
9	PA.9 / USCI0_DAT1 / UART1_TXD / BPWM0_CH2 / TM2_EXT
10	PA.8 / USCI0_CTL1 / UART1_RXD / BPWM0_CH3 / TM3_EXT / INT4
11	PF.5 / UART2_RXD / UART2_nCTS / BPWM0_CH4 / X32_IN / EADC0_ST
12	PF.4 / UART2_TXD / UART2_nRTS / BPWM0_CH5 / X32_OUT
13	PF.3 / UART0_TXD / I2C0_SCL / XT1_IN
14	PF.2 / UART0_RXD / I2C0_SDA / XT1_OUT
15	PA.7 / UART0_TXD / I2C1_SCL / TM2 / INT1
16	PA.6 / UART0_RXD / I2C1_SDA / TM3 / INT0
17	PA.5 / CAN0_TXD / UART0_nCTS / UART0_TXD / I2C0_SCL / BPWM0_CH5
18	PA.4 / CAN0_RXD / SPI0_I2SMCLK / UART0_nRTS / UART0_RXD / I2C0_SDA / BPWM0_CH4
19	PA.3 / UART4_TXD / SPI0_SS / UART1_TXD / I2C1_SCL / BPWM0_CH3 / CLKO
20	PA.2 / UART4_RXD / SPI0_CLK / UART1_RXD / I2C1_SDA / BPWM0_CH2
21	PA.1 / SPI0_MISO / UART0_TXD / UART1_nCTS / BPWM0_CH1
22	PA.0 / SPI0_MOSI / UART0_RXD / UART1_nRTS / BPWM0_CH0
23	PF.15 / TM2 / CLKO / INT4
24	nRESET
25	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / ICE_DAT
26	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / ICE_CLK
27	PC.5 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD
28	PC.4 / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD
29	PC.3 / UART2_nRTS / UART3_TXD
30	PC.2 / UART2_nCTS / UART3_RXD
31	PC.1 / UART2_TXD / I2C0_SCL
32	PC.0 / UART2_RXD / I2C0_SDA
33	USB_VBUS
34	USB_D-
35	USB_D+
36	USB_VDD33_CAP

Pin	M253LD3BE / M253LE3BE Pin Function
37	V_{SS}
38	LDO_CAP
39	V_{DD}
40	PC.14 / SPI0_I2SMCLK / USCI0_CTL0 / TM1
41	PB.15 / EADC0_CH15 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / TM0_EXT
42	PB.14 / EADC0_CH14 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / TM1_EXT / CLKO
43	PB.13 / EADC0_CH13 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / CAN0_TXD / TM2_EXT
44	PB.12 / EADC0_CH12 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / CAN0_RXD / TM3_EXT
45	AV_{DD}
46	AV_{SS}
47	PB.7 / EADC0_CH7 / UART1_TXD / INT5
48	PB.6 / EADC0_CH6 / UART1_RXD / INT4

Table 4.1-2 M253LD3BE/M253LE3BE Multi-function Pin Table

4.2 M253xx3BE Pin Mapping

Different part number with same package might has different function. Please refer to the M253xx3BE Selection Guide section, Pin Configuration section or NuTool - PinConfig.

Corresponding Part Number: M253xx3BE

	M253xx3BE	
Pin Name	33 Pin	48 Pin
PB.5	1	1
PB.4	2	2
PB.3	3	3
PB.2	4	4
PB.1	5	5
PB.0	6	6
PA.11		7
PA.10		8
PA.9		9
PA.8		10
PF.5	7	11
PF.4	8	12
PF.3	9	13
PF.2	10	14
PA.7		15
PA.6		16
PA.5		17
PA.4		18
PA.3	11	19
PA.2	12	20
PA.1	13	21
PA.0	14	22
PF.15	15	23
nRESET	16	24
PF.0	17	25
PF.1	18	26
PC.5		27
PC.4		28
PC.3		29

PC.2		30
PC.1	19	31
PC.0	20	32
USB_V_{BUS}	21	33
USB_D-	22	34
USB_D+	23	35
USB_VDD_{33_CAP}	24	36
V_{SS}	25	37
LDO_CAP	26	38
V_{DD}	27	39
PC.14		40
PB.15	28	41
PB.14	29	42
PB.13	30	43
PB.12	31	44
AV_{DD}	32	45
AV_{SS}		46
PB.7		47
PB.6		48

4.3 M253xx3BE Pin Functional Description

Group	Pin Name	GPIO	MFP	Type	Description
BPWM0	BPWM0_CH0	PA.11	MFP9	I/O	BPWM0 channel 0 output/capture input.
		PA.0	MFP12	I/O	
	BPWM0_CH1	PA.10	MFP9	I/O	BPWM0 channel 1 output/capture input.
		PA.1	MFP12	I/O	
	BPWM0_CH2	PA.9	MFP9	I/O	BPWM0 channel 2 output/capture input.
		PA.2	MFP12	I/O	
	BPWM0_CH3	PA.8	MFP9	I/O	BPWM0 channel 3 output/capture input.
		PA.3	MFP12	I/O	
	BPWM0_CH4	PF.5	MFP8	I/O	BPWM0 channel 4 output/capture input.
		PA.4	MFP12	I/O	
	BPWM0_CH5	PF.4	MFP8	I/O	BPWM0 channel 5 output/capture input.
		PA.5	MFP12	I/O	
CAN0	CAN0_RXD	PA.4	MFP2	I	CAN0 bus receiver input.
		PC.4	MFP10	I	
		PB.12	MFP9	I	
	CAN0_TXD	PA.5	MFP2	O	CAN0 bus transmitter output.
		PC.5	MFP10	O	
		PB.13	MFP9	O	
CLKO	CLKO	PA.3	MFP14	O	Clock Out
		PF.15	MFP14	O	
		PB.14	MFP14	O	
EADC0	EADC0_CH0	PB.0	MFP1	A	EADC0 channel 0 analog input.
	EADC0_CH1	PB.1	MFP1	A	EADC0 channel 1 analog input.
	EADC0_CH2	PB.2	MFP1	A	EADC0 channel 2 analog input.
	EADC0_CH3	PB.3	MFP1	A	EADC0 channel 3 analog input.
	EADC0_CH4	PB.4	MFP1	A	EADC0 channel 4 analog input.
	EADC0_CH5	PB.5	MFP1	A	EADC0 channel 5 analog input.
	EADC0_CH6	PB.6	MFP1	A	EADC0 channel 6 analog input.
	EADC0_CH7	PB.7	MFP1	A	EADC0 channel 7 analog input.
	EADC0_CH12	PB.12	MFP1	A	EADC0 channel 12 analog input.
	EADC0_CH13	PB.13	MFP1	A	EADC0 channel 13 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	EADC0_CH14	PB.14	MFP1	A	EADC0 channel 14 analog input.
	EADC0_CH15	PB.15	MFP1	A	EADC0 channel 15 analog input.
	EADC0_ST	PF.5	MFP11	I	EADC0 external trigger input.
I2C0	I2C0_SCL	PB.5	MFP6	I/O	I2C0 clock pin.
		PF.3	MFP4	I/O	
		PA.5	MFP9	I/O	
		PC.1	MFP9	I/O	
	I2C0_SDA	PB.4	MFP6	I/O	I2C0 data input/output pin.
		PF.2	MFP4	I/O	
		PA.4	MFP9	I/O	
		PC.0	MFP9	I/O	
I2C1	I2C1_SCL	PB.3	MFP4	I/O	I2C1 clock pin.
		PB.1	MFP9	I/O	
		PA.7	MFP8	I/O	
		PA.3	MFP9	I/O	
		PF.0	MFP3	I/O	
		PC.5	MFP9	I/O	
	I2C1_SDA	PB.2	MFP4	I/O	I2C1 data input/output pin.
		PB.0	MFP9	I/O	
		PA.6	MFP8	I/O	
		PA.2	MFP9	I/O	
		PF.1	MFP3	I/O	
		PC.4	MFP9	I/O	
ICE	ICE_CLK	PF.1	MFP14	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	PF.0	MFP14	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	PB.5	MFP15	I	External interrupt 0 input pin.
		PA.6	MFP15	I	
INT1	INT1	PB.4	MFP15	I	External interrupt 1 input pin.
		PA.7	MFP15	I	

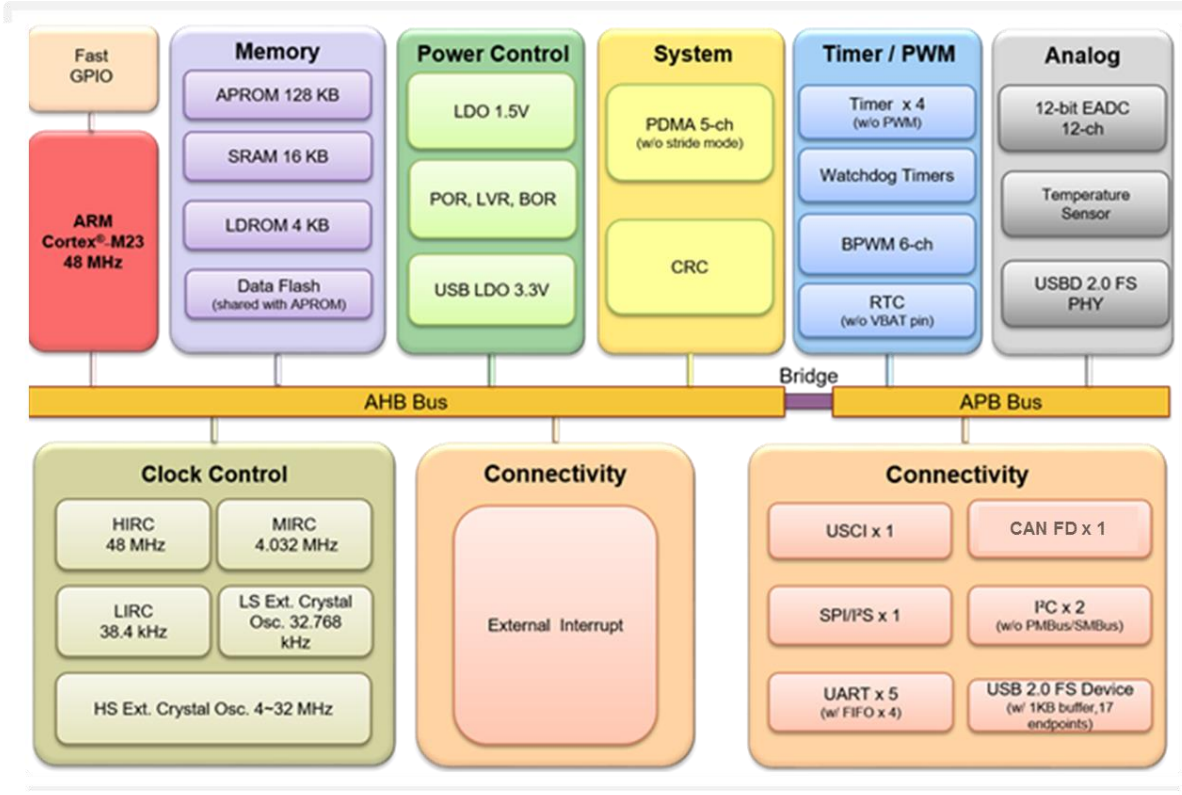
Group	Pin Name	GPIO	MFP	Type	Description
INT2	INT2	PB.3	MFP15	I	External interrupt 2 input pin.
INT3	INT3	PB.2	MFP15	I	External interrupt 3 input pin.
INT4	INT4	PA.8	MFP15	I	External interrupt 4 input pin.
		PF.15	MFP15	I	
		PB.6	MFP13	I	
INT5	INT5	PB.7	MFP13	I	External interrupt 5 input pin.
SPI0	SPI0_CLK	PA.2	MFP4	I/O	SPI0 serial clock pin.
		PB.14	MFP4	I/O	
	SPI0_I2SMCLK	PB.0	MFP8	I/O	SPI0 I^2S master clock output pin
		PA.4	MFP4	I/O	
		PC.14	MFP4	I/O	
	SPI0_MISO	PA.1	MFP4	I/O	SPI0 MISO (Master In, Slave Out) pin.
		PB.13	MFP4	I/O	
	SPI0_MOSI	PA.0	MFP4	I/O	SPI0 MOSI (Master Out, Slave In) pin.
		PB.12	MFP4	I/O	
	SPI0_SS	PA.3	MFP4	I/O	SPI0 slave select pin.
		PB.15	MFP4	I/O	
TM0	TM0	PB.5	MFP14	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	PA.11	MFP13	I/O	Timer0 external capture input/toggle output pin.
		PB.15	MFP13	I/O	
TM1	TM1	PB.4	MFP14	I/O	Timer1 event counter input/toggle output pin.
		PC.14	MFP13	I/O	
	TM1_EXT	PA.10	MFP13	I/O	Timer1 external capture input/toggle output pin.
		PB.14	MFP13	I/O	
TM2	TM2	PB.3	MFP14	I/O	Timer2 event counter input/toggle output pin.
		PA.7	MFP14	I/O	
		PF.15	MFP13	I/O	
	TM2_EXT	PA.9	MFP13	I/O	Timer2 external capture input/toggle output pin.
		PB.13	MFP13	I/O	
TM3	TM3	PB.2	MFP14	I/O	Timer3 event counter input/toggle output pin.
		PA.6	MFP14	I/O	

Group	Pin Name	GPIO	MFP	Type	Description
	TM3_EXT	PA.8	MFP13	I/O	Timer3 external capture input/toggle output pin.
		PB.12	MFP13	I/O	
UART0	UART0_RXD	PF.2	MFP3	I	UART0 data receiver input pin.
		PA.6	MFP7	I	
		PA.4	MFP8	I	
		PA.0	MFP7	I	
		PF.1	MFP4	I	
		PB.12	MFP6	I	
	UART0_TXD	PF.3	MFP3	O	UART0 data transmitter output pin.
		PA.7	MFP7	O	
		PA.5	MFP8	O	
		PA.1	MFP7	O	
		PF.0	MFP4	O	
		PB.13	MFP6	O	
	UART0_nCTS	PA.5	MFP7	I	UART0 clear to send input pin.
		PB.15	MFP6	I	
	UART0_nRTS	PA.4	MFP7	O	UART0 request to Send output pin.
		PB.14	MFP6	O	
UART1	UART1_RXD	PB.2	MFP6	I	UART1 data receiver input pin.
		PA.8	MFP7	I	
		PA.2	MFP8	I	
		PF.1	MFP2	I	
		PB.6	MFP6	I	
	UART1_TXD	PB.3	MFP6	O	UART1 data transmitter output pin.
		PA.9	MFP7	O	
		PA.3	MFP8	O	
		PF.0	MFP2	O	
		PB.7	MFP6	O	
	UART1_nCTS	PA.1	MFP8	I	UART1 clear to send input pin.
	UART1_nRTS	PA.0	MFP8	O	UART1 request to Send output pin.
UART2	UART2_RXD	PB.4	MFP13	I	UART2 data receiver input pin.
		PB.0	MFP7	I	

Group	Pin Name	GPIO	MFP	Type	Description
		PF.5	MFP2	I	
		PC.4	MFP8	I	
		PC.0	MFP8	I	
	UART2_TXD	PB.5	MFP13	O	UART2 data transmitter output pin.
		PB.1	MFP7	O	
		PF.4	MFP2	O	
		PC.5	MFP8	O	
		PC.1	MFP8	O	
	UART2_nCTS	PF.5	MFP4	I	UART2 clear to Send input pin.
		PC.2	MFP8	I	
	UART2_nRTS	PF.4	MFP4	O	UART2 request to Send output pin.
		PC.3	MFP8	O	
UART3	UART3_RXD	PC.2	MFP11	I	UART3 data receiver input pin.
		PB.14	MFP7	I	
	UART3_TXD	PC.3	MFP11	O	UART3 data transmitter output pin.
		PB.15	MFP7	O	
	UART3_nCTS	PB.12	MFP7	I	UART3 clear to Send input pin.
	UART3_nRTS	PB.13	MFP7	O	UART3 request to Send output pin.
UART4	UART4_RXD	PA.2	MFP2	I	UART4 data receiver input pin.
		PC.4	MFP11	I	
	UART4_TXD	PA.3	MFP2	O	UART4 data transmitter output pin.
		PC.5	MFP11	O	
USCI0	USCI0_CLK	PA.11	MFP6	I/O	USCI0 clock pin.
		PB.12	MFP5	I/O	
	USCI0_CTL0	PC.14	MFP5	I/O	USCI0 control 0 pin.
	USCI0_CTL1	PA.8	MFP6	I/O	USCI0 control 1 pin.
		PB.15	MFP5	I/O	
	USCI0_DAT0	PA.10	MFP6	I/O	USCI0 data 0 pin.
		PB.13	MFP5	I/O	
	USCI0_DAT1	PA.9	MFP6	I/O	USCI0 data 1 pin.
		PB.14	MFP5	I/O	
X32	X32_IN	PF.5	MFP10	I	External 32.768 kHz crystal input pin.

Group	Pin Name	GPIO	MFP	Type	Description
	X32_OUT	PF.4	MFP10	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PF.3	MFP10	I	External 4~32 MHz (high speed) crystal input pin.
	XT1_OUT	PF.2	MFP10	O	External 4~32 MHz (high speed) crystal output pin.

5 BLOCK DIAGRAM



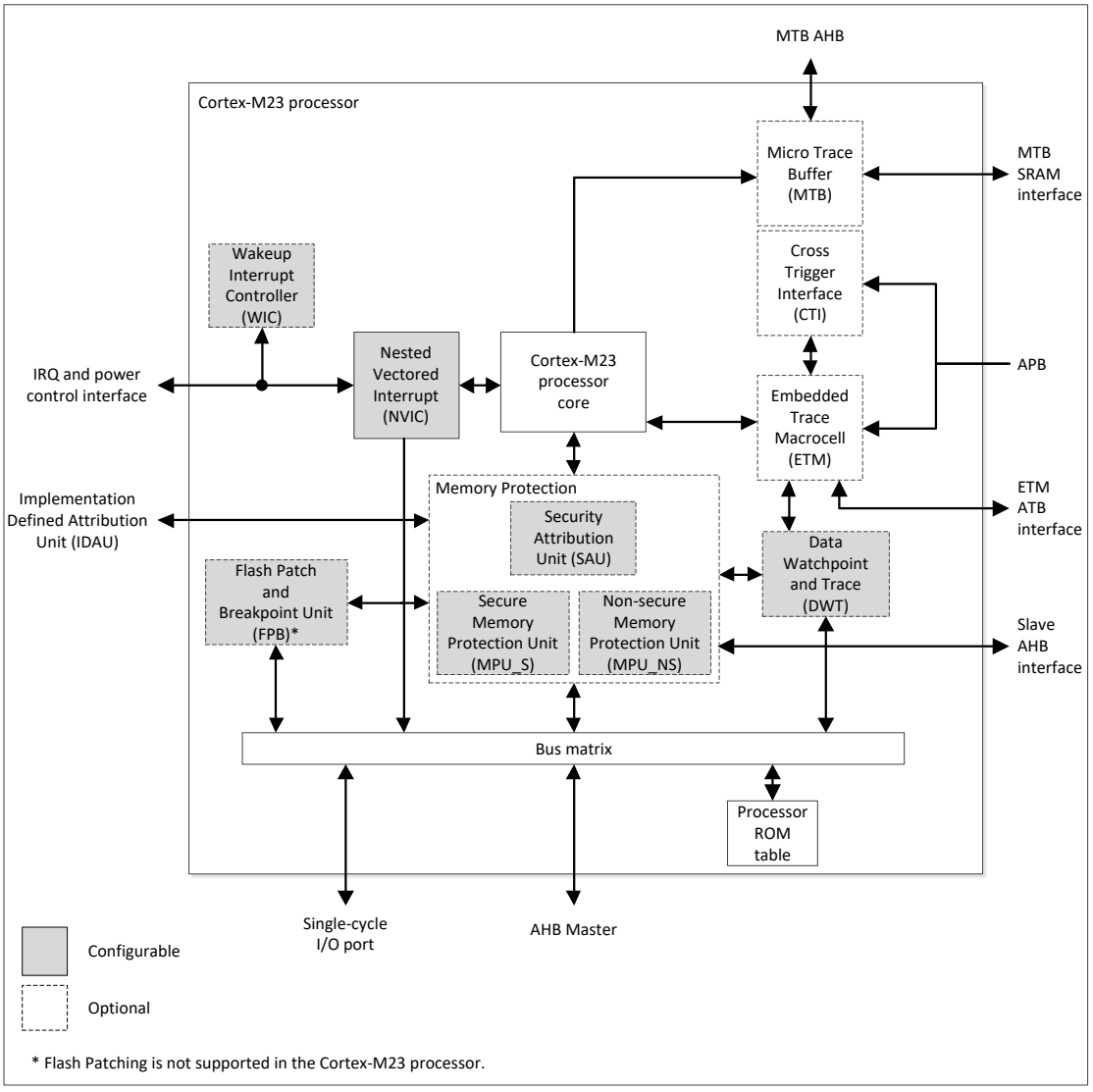
Please refer to the M253xx3BE Selection Guide section for detailed information.

Figure 4.3-1 M253xx3BE Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, which has an AMBA AHB5 interface supporting Arm® TrustZone® technology, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. The NuMicro® M253xx3BE is embedded with Cortex®-M23 processor.Figure 6.1-1 shows the functional controller of the processor.



Note: The M253xx3BE does not support security attribution unit, ETM, CTI and MTB function.

Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin with glitch filter time 24us
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core Only by writing 1 to CPURST (SYS_IPRST0[1])

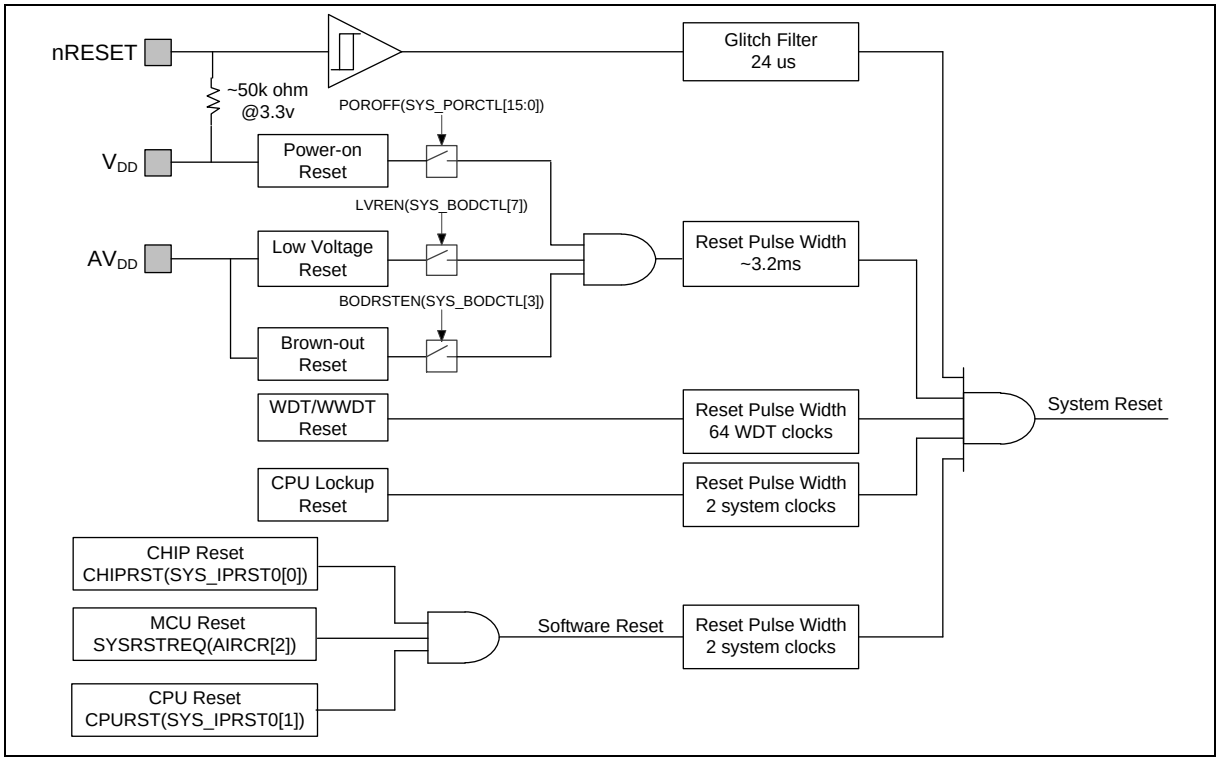


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	Reload from	-

(CLK_CLKSEL0[2:0])	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	CONFIG0	
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1]) BL (FMC_ISPCTL[16])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1))	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 24 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 24 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Table 6.2-2 shows the nRESET reset waveform.

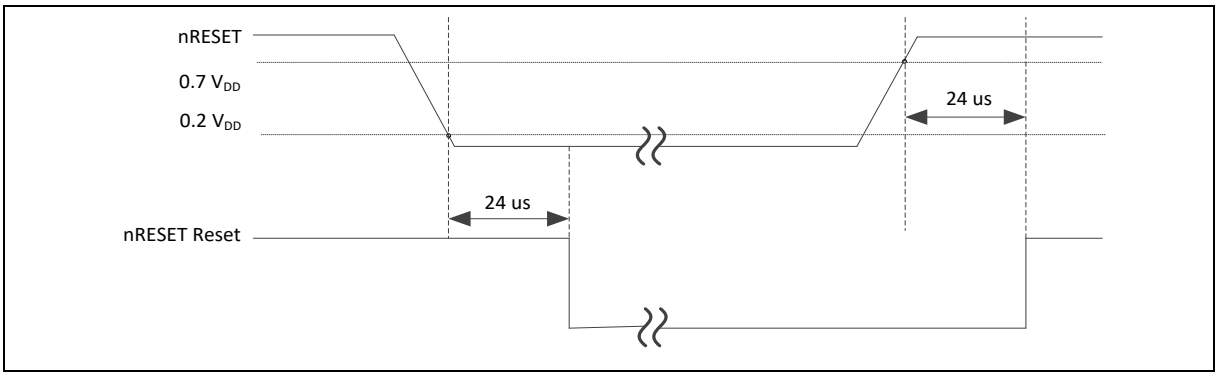


Figure 6.2-2 nRESET Reset Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-3 shows the power-on reset waveform.

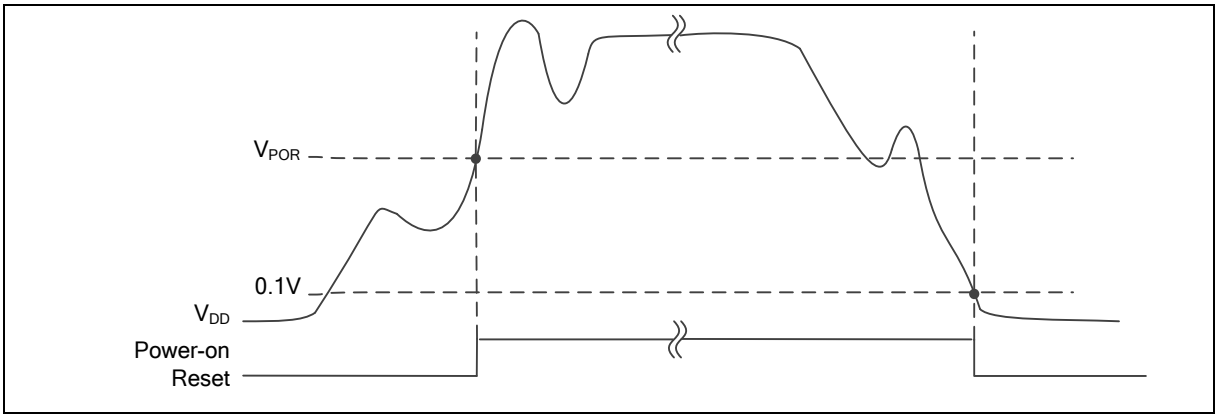


Figure 6.2-3 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-4 shows the Low Voltage Reset waveform.

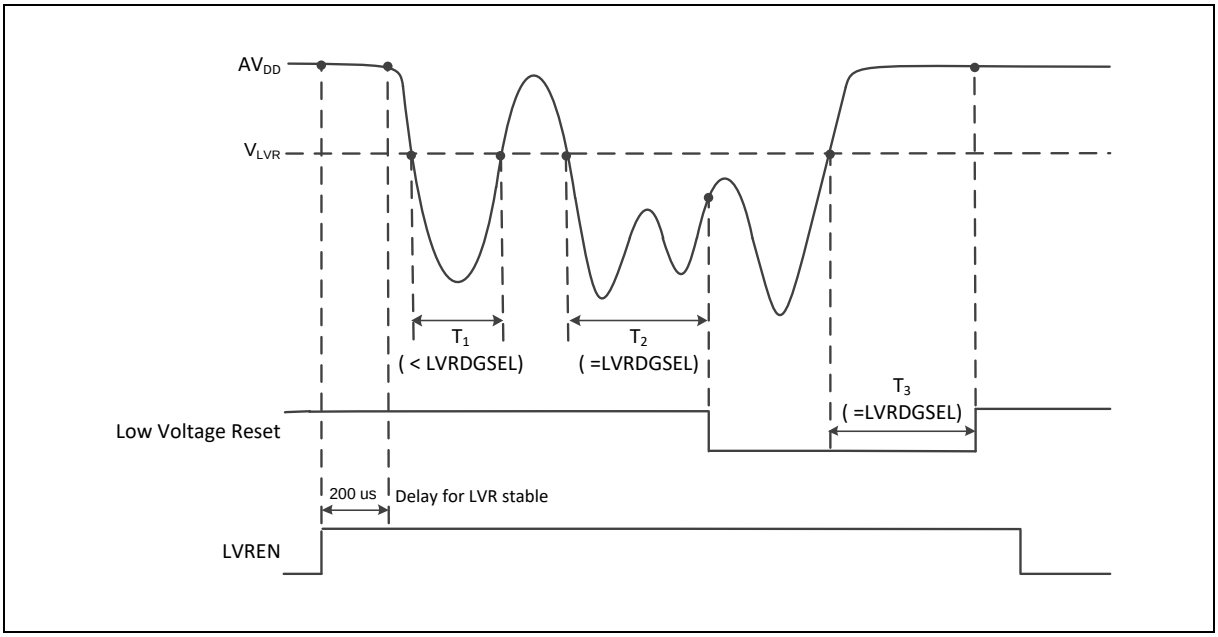


Figure 6.2-4 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-5 shows the Brown-out Detector waveform.

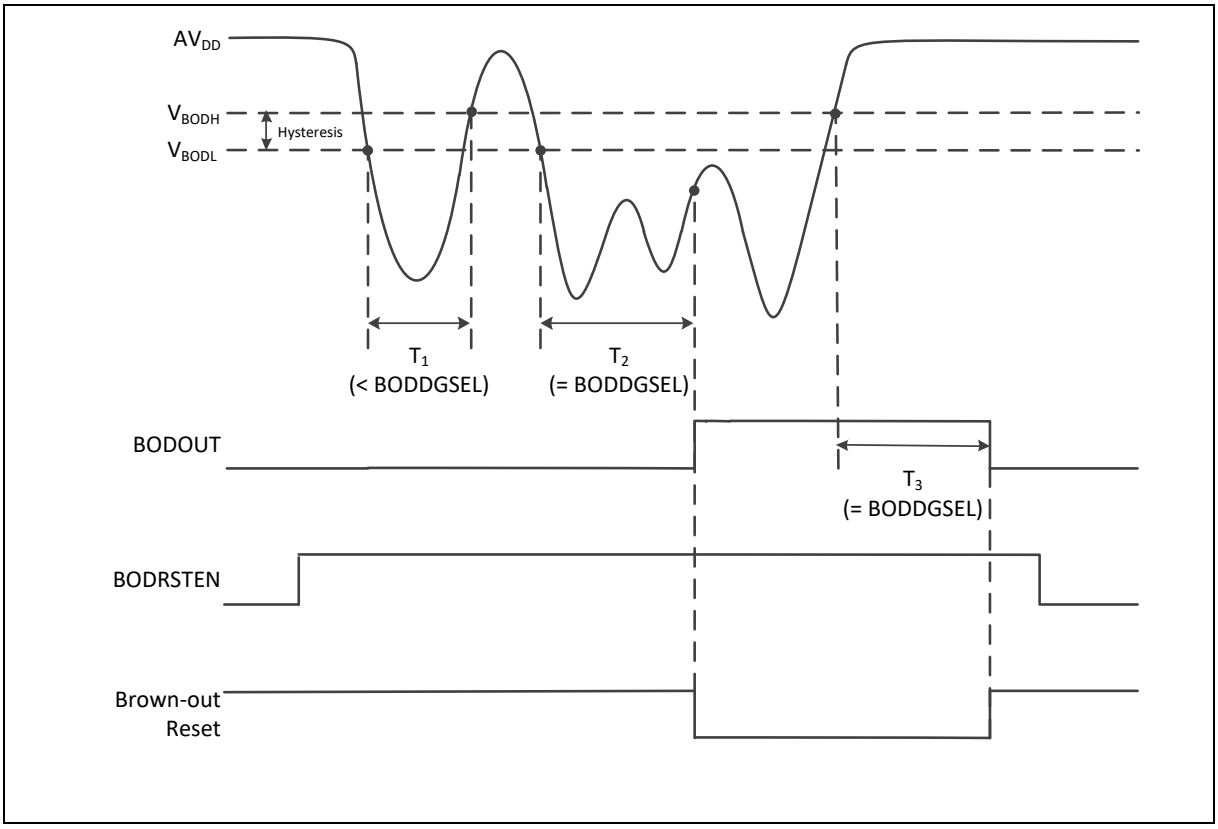


Figure 6.2-5 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer (WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into four segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.5V power for digital operation and I/O pins.
- USB transceiver power from VBUS offers the power for operating the USB transceiver.
- RTC power from regulator uninterrupted power domain provides, the power for RTC and 20 bytes backup registers.

Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-6 shows the power distribution of the M253xx3BE series.

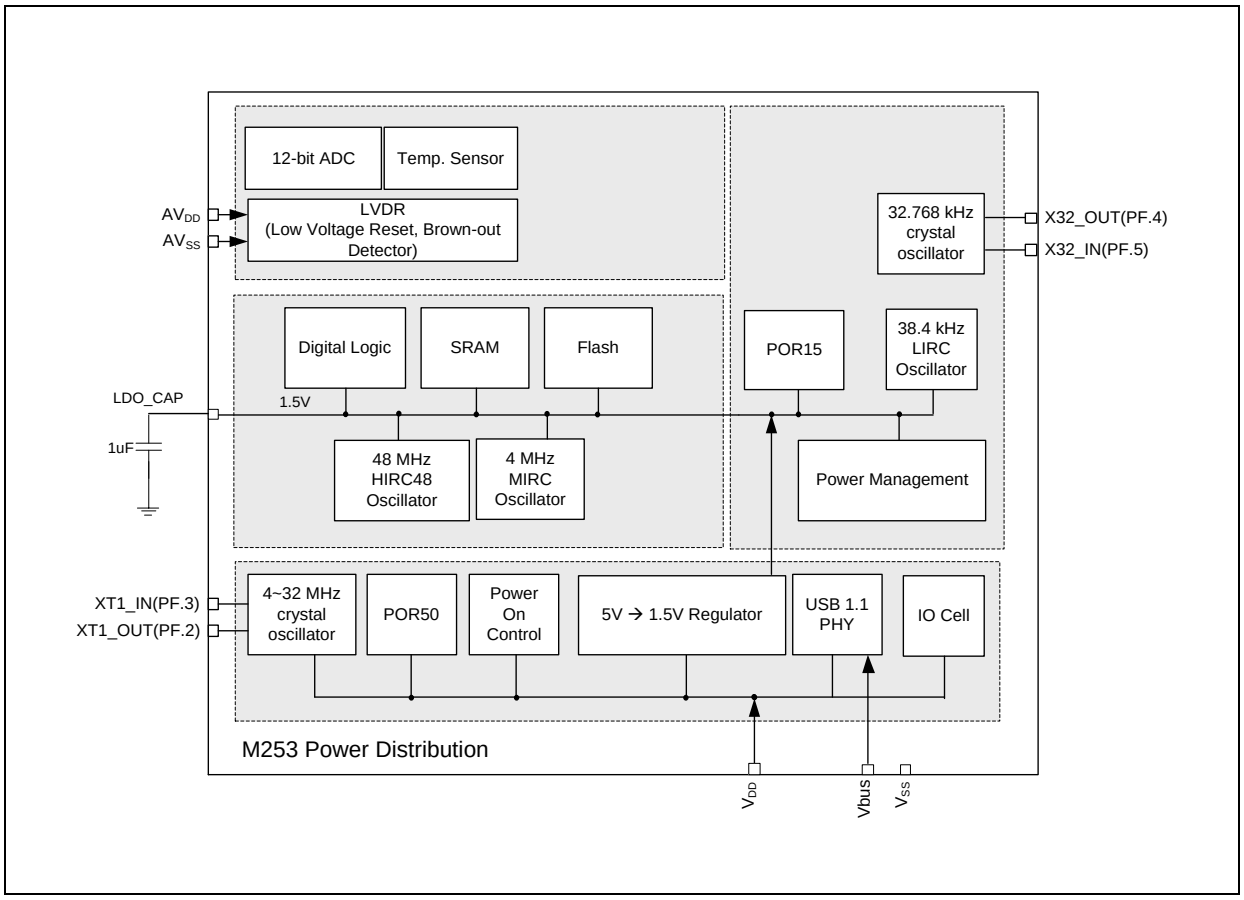


Figure 6.2-6 NuMicro® M253xx3BE Series Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M253xx3BE series has a power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power modes in the M253xx3BE series.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP(V)	Clock Disable
Normal mode	48	1.5	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	1.5	Only CPU clock is disabled.
Power-down mode	CPU enters Deep Sleep mode	1.5	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Fast wake up Power-down mode (FWPD)	CPU enters Sleep mode	1.5	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.2-2 Power Mode Table

There are different power mode entry settings. Each power mode has different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running ar normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL:[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode (CPU enters Sleep mode)	0	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	0	YES
Fast wake up Power-down mode (FWPD)	1	1	2	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, EINT, USCI and USBD
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

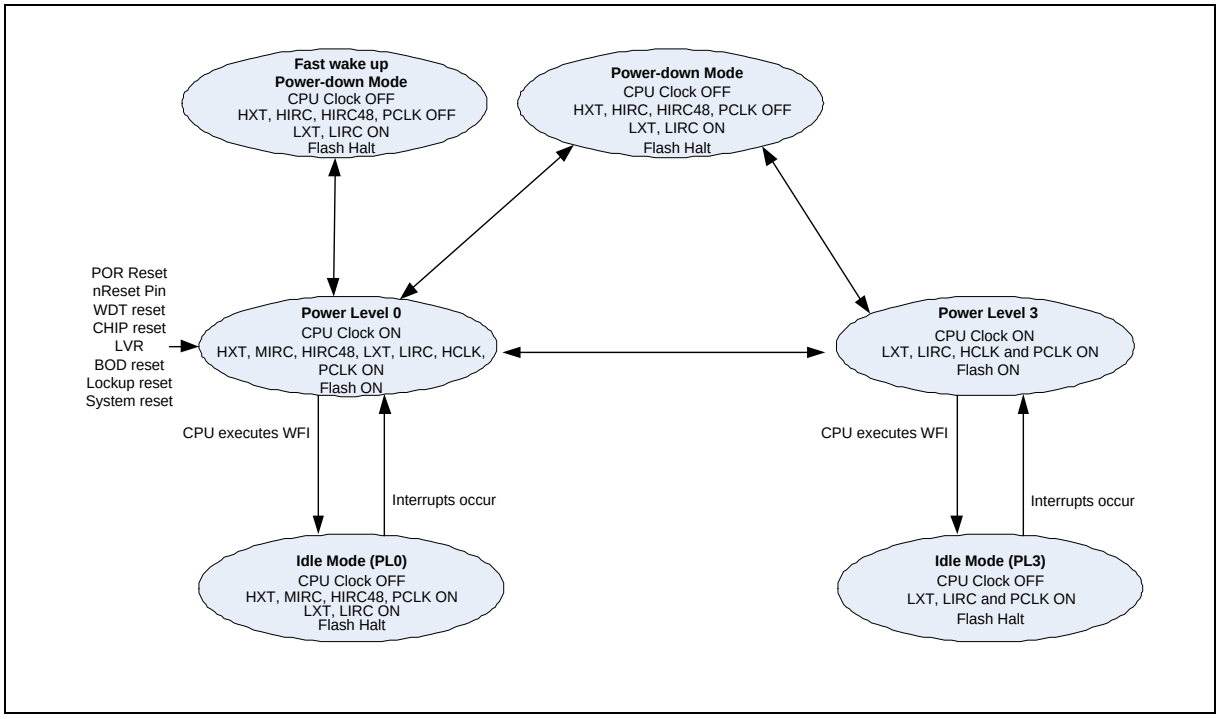


Figure 6.2-7 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on SOFTWARE setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If RTC clock source is selected as LXT and LXT is on.
6. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode PD
HXT (4~32 MHz XTL)	ON	ON	Halt
MIRC (4 MHz OSC)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]
LDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
WDT	ON	ON	ON/OFF[4]
WWDT	ON	ON	Halt
RTC	ON	ON	ON/OFF[5]
UART	ON	ON	ON/OFF[6]
USCI	ON	ON	Halt
I^2C	ON	ON	Halt
SPI	ON	ON	Halt
USBD	ON	ON	Halt
ADC	ON	ON	Halt

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

RTC, WDT, I²C, Timer, UART, USCI, BOD, GPIO, and USBD.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	Power-Down Mode	System Can Enter Power-Down Mode Again Condition*
		PD FWKPD	
BOD	Brown-Out Detector Interrupt	Y	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
LVR	LVR Reset	Y	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		N	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when DPD mode is entered.
INT	External Interrupt	Y	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	Y	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	Y	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	Y	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	Y	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	Y	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
UART	nCTS wake-up	Y	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	Incoming Data wake-up	Y	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	Y	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	Y	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	Y	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	Y	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	Y	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	Y	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	Y	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], and then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	Y	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	Y	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
USBD	Remote Wake-up	Y	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.5 Chip Bus Matrix

The M253xx3BE series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M253xx3BE series only supports little-endian data format.

6.2.6 System Memory Map

The M253xx3BE series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M253xx3BE series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0001_FFFF	FLASH_BA	FLASH Memory Space (128 Kbytes)
0x2000_0000 – 0x2000_3FFF	SRAM0_BA	SRAM Memory Space (16 Kbytes)
0x6000_0000 – 0x6FFF_FFFF	EXTMEM_BA	External Memory Space (256 Mbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC_BA	Enhanced Analog-Digital-Converter (EADC) Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x400A_0000 – 0x400A_0FFF	CANFD0_BA	CANFD0 Control Register
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers

System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 SRAM Memory Organization

The M253xx3BE series supports embedded SRAM with up to 16 Kbytes size.

- Supports up to 16 Kbytes SRAM
- Supports byte /half word /word write
- Supports oversize response error

Table 6.2-9 shows the M253xx3BE series SRAM organization. The address between 0x2000_4000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

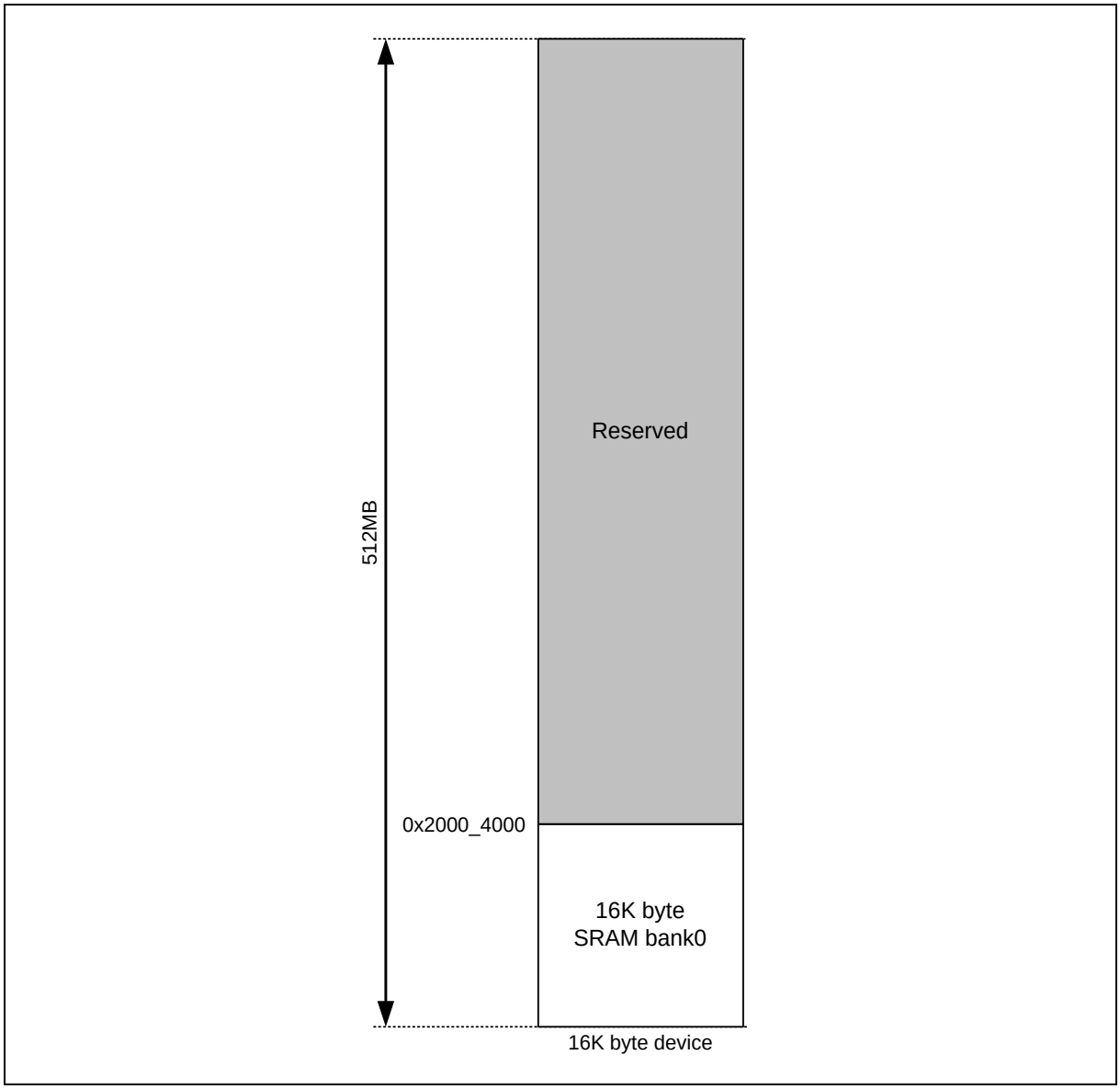


Figure 6.2-8 SRAM Memory Organization

6.2.8 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator) and MIRC trim (4.032 RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 4.032 MHz clock. In such case, if neither uses PLL as the system clock source nor solders 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_MIRCTRIMCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_MIRCTRIMCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_MIRCTRIMSTS[0] MIRC frequency lock status) “1” indicates the MIRC output frequency is accurate within 0.25% deviation.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if neither uses PLL as the system clock source nor solders 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTRIMCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTRIMCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

HIRC trim and MIRC trim can only work properly when the clock sources are stable. When the RC clock or the reference clock is not stable or the system goes into power down, HIRC trim and MIRC trim need to wait until the clock is stable or system wakes up, and then it can be enabled or will get a clock error flag.

6.2.9 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M23 Technical Reference Manual” and “Arm® v8-M Architecture Reference Manual”.

6.2.10 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-64 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and sub-priority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.10.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by the M253xx3BE series. Software can set 4 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xC0” (The 6-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80.

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Reserved	4~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12~13		Reserved
PendSV	14	0x00000038	Configurable

SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ63)	16 ~ 63	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	Reserved	Reserved
20	4	CLKFAIL	Clock fail detected interrupt
21	5	Reserved	Reserved
22	6	RTC_INT	Real time clock interrupt
23	7	Reserved	Reserved
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from PA.0, PD.2 or PE.4 pins
27	11	EINT1	External interrupt from PB.0, PD.3 or PE.5 pins
28	12	EINT2	External interrupt from PC.0 pin
29	13	EINT3	External interrupt from PD.0 pin
30	14	EINT4	External interrupt from PE.0 pin
31	15	EINT5	External interrupt from PF.0 pin
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[15:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	Reserved	Reserved
36	20	Reserved	Reserved
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	Reserved	Reserved
39	23	SPI0_INT	SPI0 interrupt
40	24	CANFD0_INT0	CANFD0 interrupt 0
41	25	CANFD0_INT1	CANFD0 interrupt 1
42	26	Reserved	Reserved

43	27	Reserved	Reserved
44	28	Reserved	Reserved
45	29	Reserved	Reserved
46	30	Reserved	Reserved
47	31	Reserved	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA_INT	PDMA interrupt
57	41	Reserved	Reserved
58	42	EADC_INT	EADC interrupt source 0
59	43	EADC1_INT	EADC interrupt source 1
60	44	Reserved	Reserved
61	45	BPWM0	BPWM0 interrupt
62	46	EADC_INT2	EADC interrupt source 2
63	47	EADC_INT3	EADC interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	UART3_INT	UART3 interrupt
66	50	USCI0	USCI0 interrupt
67	51	UART4_INT	UART4 interrupt
68	52	Reserved	Reserved
69	53	USBD_INT	USB device interrupt
70	54	Reserved	Reserved
71	55	Reserved	Reserved
72	56	Reserved	Reserved
73	57	Reserved	Reserved
74	58	Reserved	Reserved
75	59	Reserved	Reserved
76	60	Reserved	Reserved
77	61	Reserved	Reserved

78	62	Reserved	Reserved
79	63	Reserved	Reserved

Table 6.2-9 Interrupt Number Table

6.2.10.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M23 core executes the WFI instruction. After that, chip enters Power-down mode and waits for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~32 MHz external high speed crystal (HXT), 48 MHz internal high speed RC oscillator (HIRC) and 4 MHz internal median speed RC oscillator (MIRC) to reduce the overall system power consumption Figure 6.3-1 shows the clock generator and the overview of the clock source control.

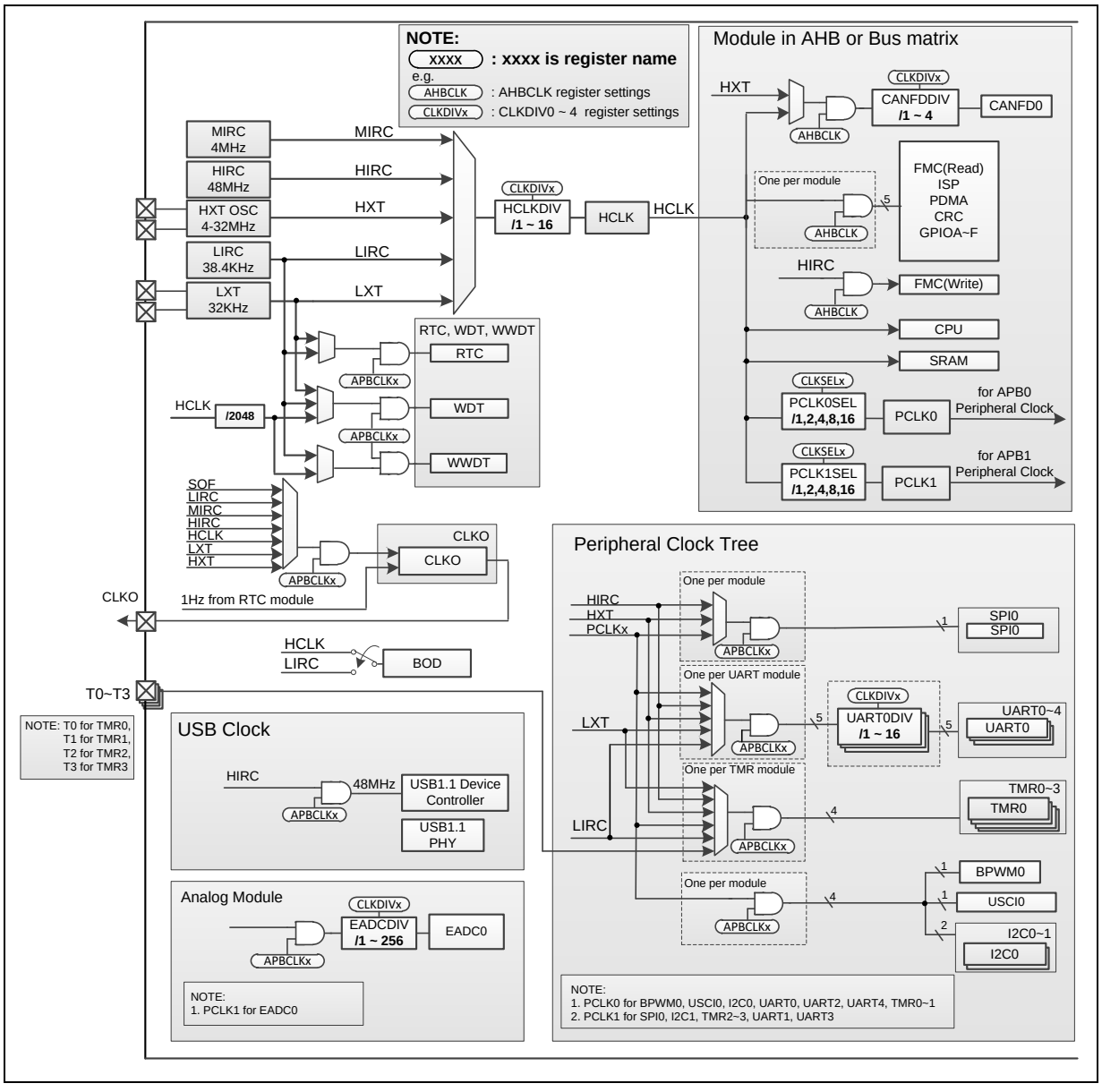


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 5 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~32 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)
- 4 MHz internal medium speed oscillator (MIRC)

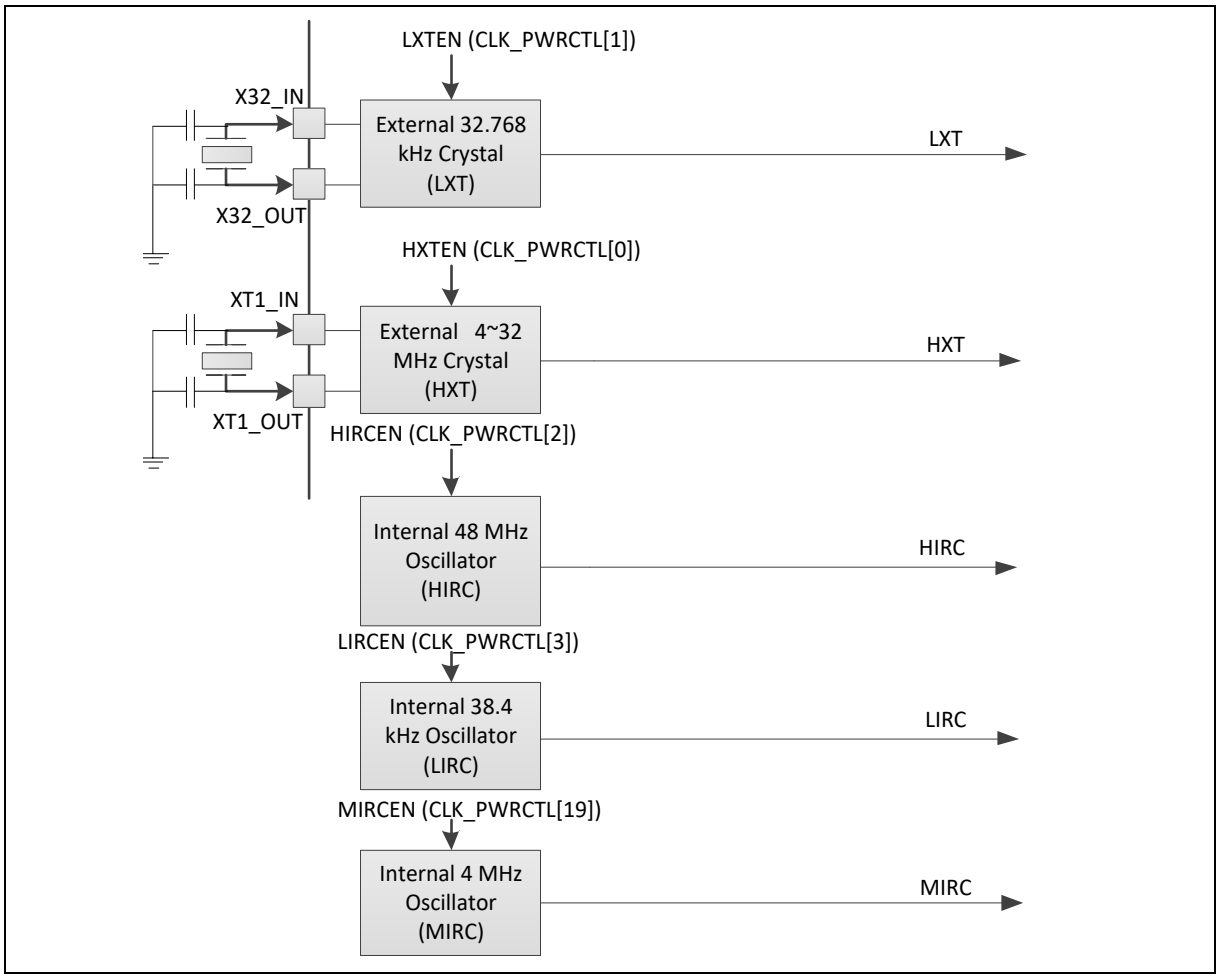


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which are generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3

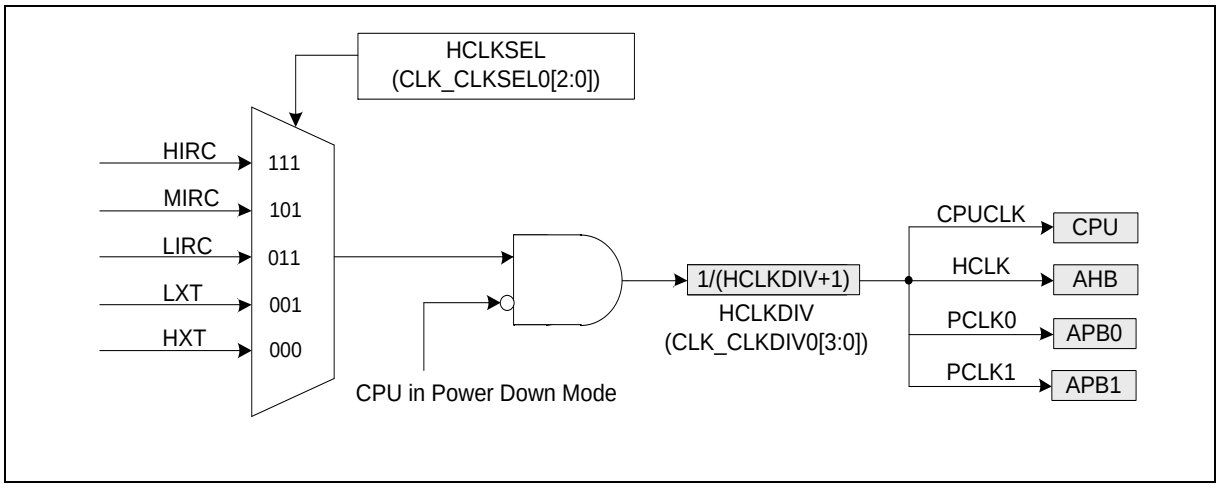


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the MIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to MIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to MIRC procedure is shown in Figure 6.3-4.

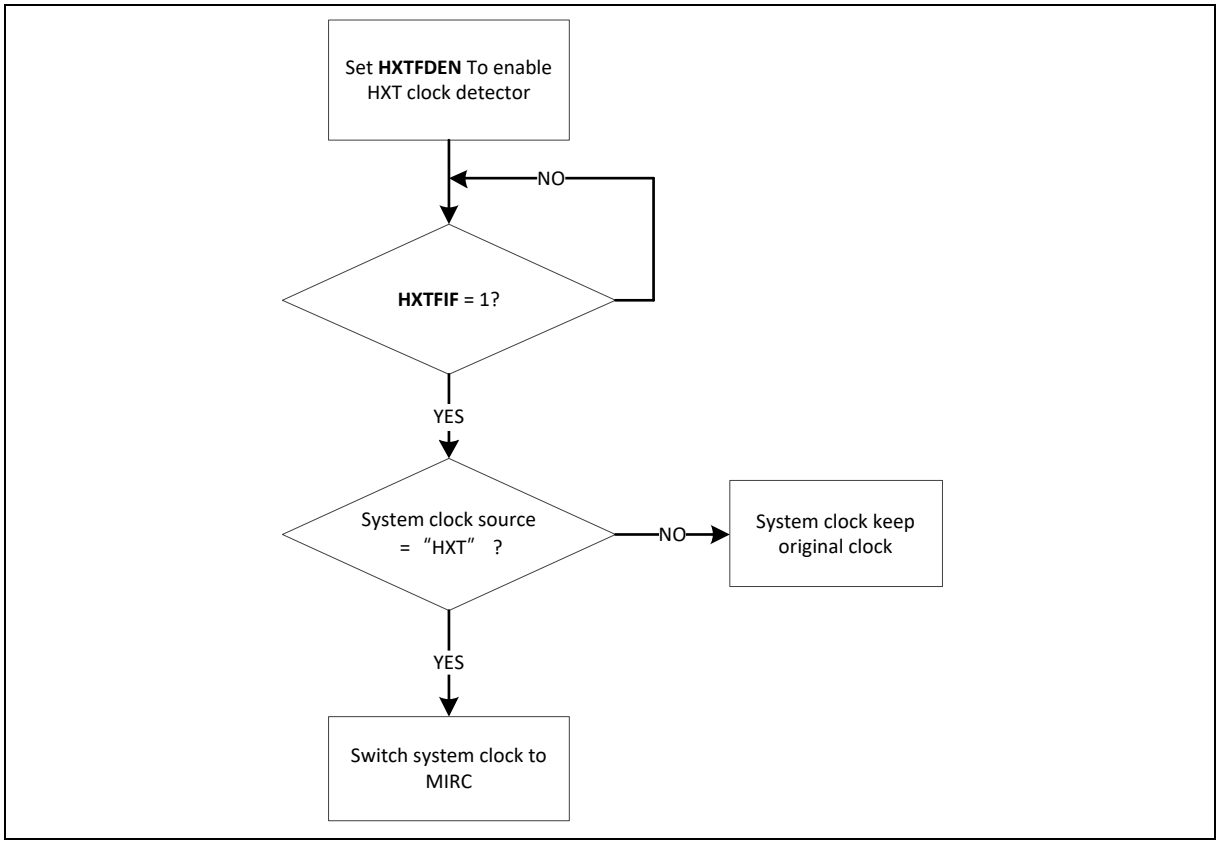


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M23 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

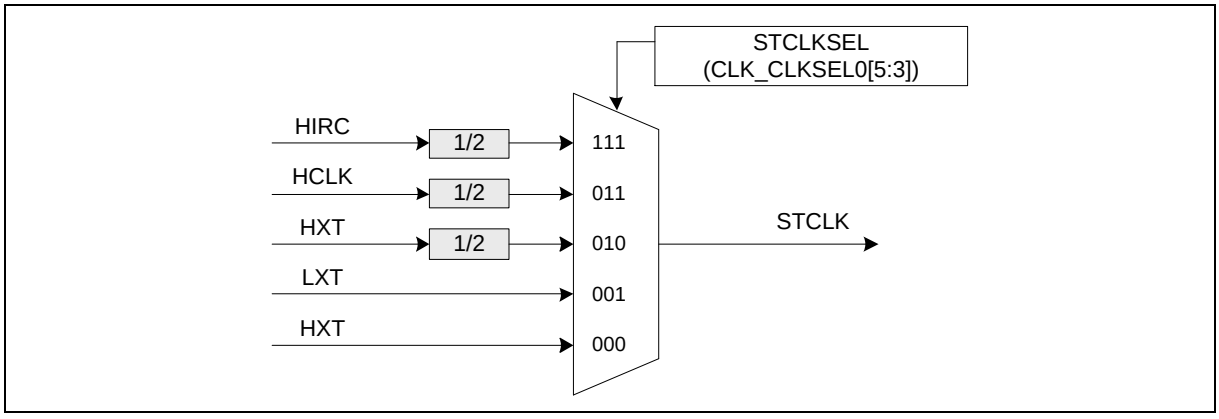


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral. Please refer to the CLK_CLKSEL1 and CLK_CLKSEL2 register description.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
  - 4 MHz internal medium speed oscillator (MIRC) clock if LCD and TK enabled.
- Peripherals Clock, except for HCLK, PCLK0 and PCLK1(When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to DIV1EN (CLK_CLKOCTL[5]), the chained counter starts to count. When writing 0 to DIV1EN (CLK_CLKOCTL[5]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

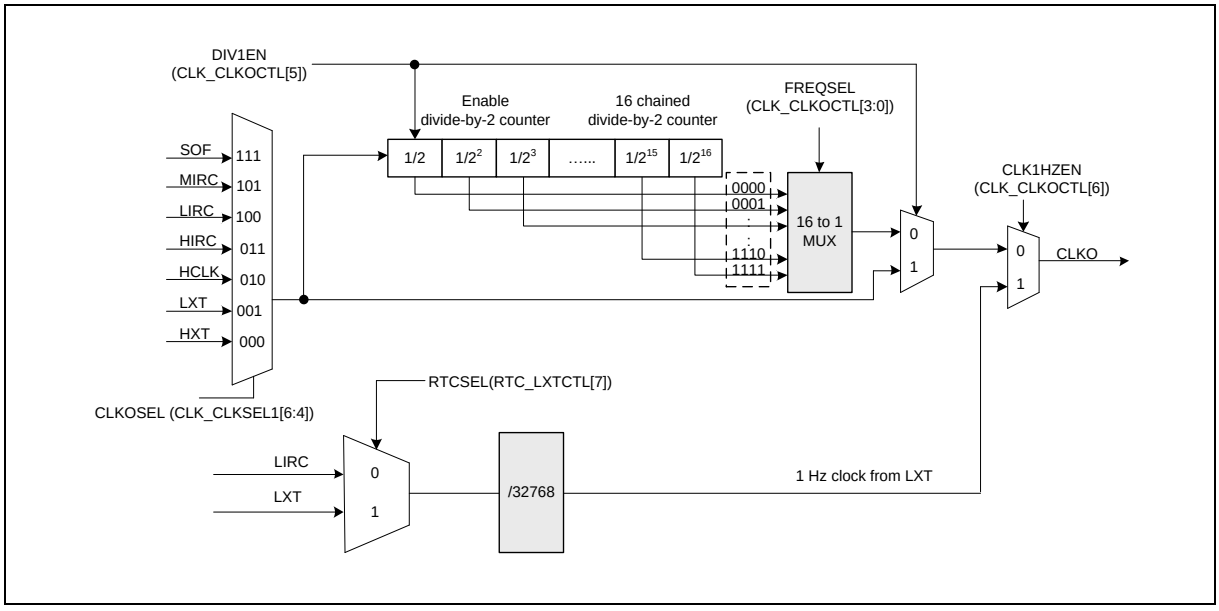


Figure 6.3-6 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock source of USB 1.0 is generated from 48 MHz HIRC. The generated clocks are shown in Figure 6.3-7.

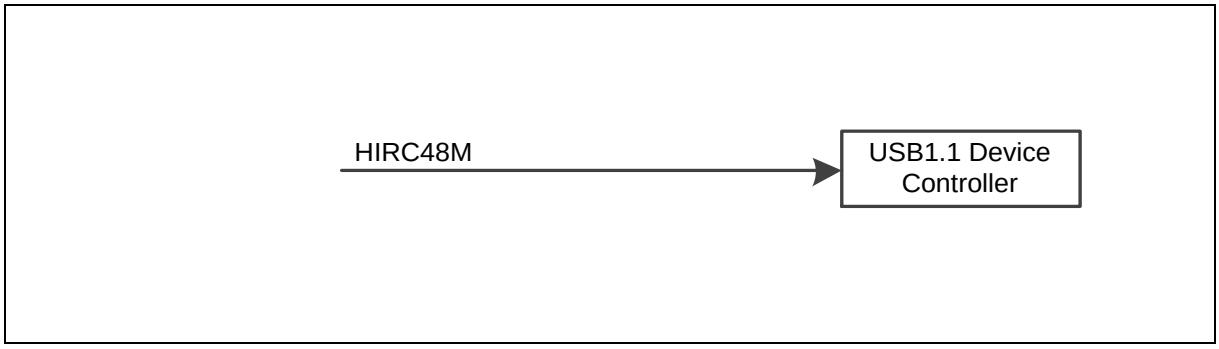


Figure 6.3-7 USB Clock Source

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The FMC is equipped with 128 Kbytes on-chip embedded Flash for application. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. XOM (Execution Only Memory) setting block to conceal user program in XOM region. A 512 bytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 128 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 1 XOM (Execution Only Memory) region to conceal user program in APROM
- Supports 12 bytes User Configuration block to control system initiation.
- Supports 512 bytes page erase for all embedded Flash
- Supports 32-bit and multi-word Flash programming function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports embedded SRAM remap to system vector memory
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 38 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 38 pins are arranged in 4 ports named as PA, PB, PC, and PF. PA and PB has 12 pins on port. PC has 7 pins on port. PF has 7 pins on port. Each of the 38 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 50 kΩ. Please refer to the M253xx3BE Datasheet for detailed pin operation voltage information about V_{DD} electrical characteristics.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Support independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Improve access efficiency by using single cycle I/O bus

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 5 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Request source can be from software,PSIO , SPI/I^2S, UART, USCI, EADC,DAC,PWM capture event and TIMER
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger BPWM, EADC, DAC and PDMA function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 417us ~ 27. 3 s if WDT_CLK = 38.4 kHz (LIRC).
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 38.4 kHz LIRC or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 Real Time Clock (RTC)

6.10.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.10.2 Features

- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
-
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.

6.11 Basic PWM Generator and Capture Timer (BPWM)

6.11.1 Overview

The chip provides one BPWM generators. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.11.2 Features

6.11.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to one BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC in the following events:
  - BPWM counter matches 0, period value or compared value

6.11.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.12 UART Interface Controller (UART)

6.12.1 Overview

The chip provides five channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, RS-485, and Single-wire function modes and auto-baud rate measuring function.

6.12.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes or 1/1 byte entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Support 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Support Single-wire function mode.

UART Feature	UART0 ~ UART3	UART4	USCI-UART
FIFO	16 Bytes	1 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	-	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	-	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	-	-
RS-485 Address Match (AAD mode) Wake-up	√	-	-
Received Data FIFO reached threshold Time-out Wake-up	√	-	
Baud Rate Compensation	√	-	
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.12-1 NuMicro® M253xx3BE Series UART Features

6.13 Serial Peripheral Interface (SPI)

6.13.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains one SPI controller performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. The SPI controller also supports I^2S mode to connect external audio CODEC. Please refer to the M253xx3BE Datasheet for detailed information about maximum SPI clock frequency of SPI master mode and SPI slave mode and range of SPI operation voltage.

6.13.2 Features

- SPI Mode
  - Supports one SPI controller
  - Supports Master or Slave mode operation
  - Configurable bit length of a transaction word from 8 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.14 I²C Serial Interface Controller (I²C)

6.14.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are two sets of I²C controllers that support Power-down wake-up function.

6.14.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to two I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability
- Supports setup/hold time programmable

6.15 USCI - Universal Serial Control Interface Controller (USCI)

6.15.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.15.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.16 USCI – UART Mode

6.16.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake up the system.

6.16.2 Features

- Supports one transmit buffer and two receive buffers for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Supports 9-bit Data Transfer (9-bit RS-485)
- Baud rate detection by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wake-up Only)

6.17 USCI - SPI Mode

6.17.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1.

This SPI protocol can operate as master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in master and Slave mode are shown below.

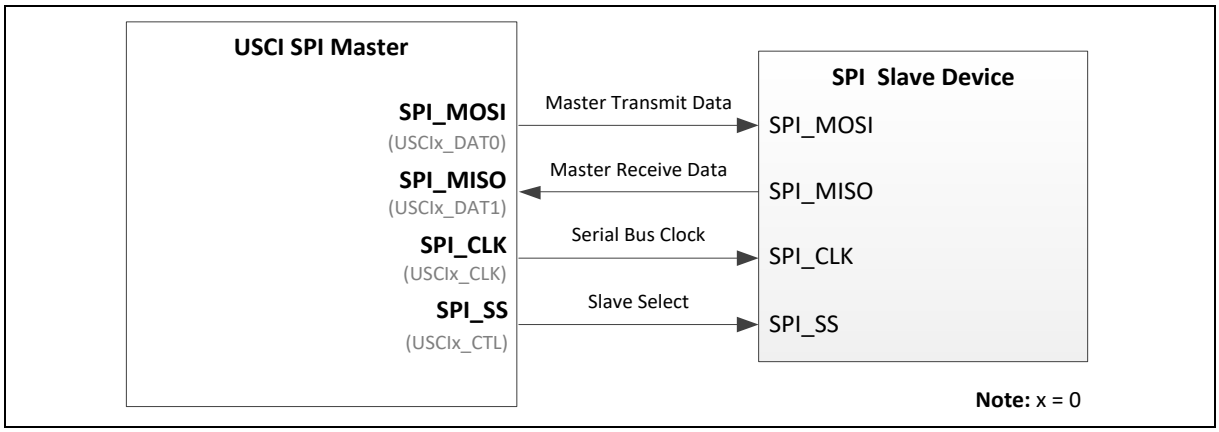


Figure 6.17-1 SPI Master Mode Application Block Diagram

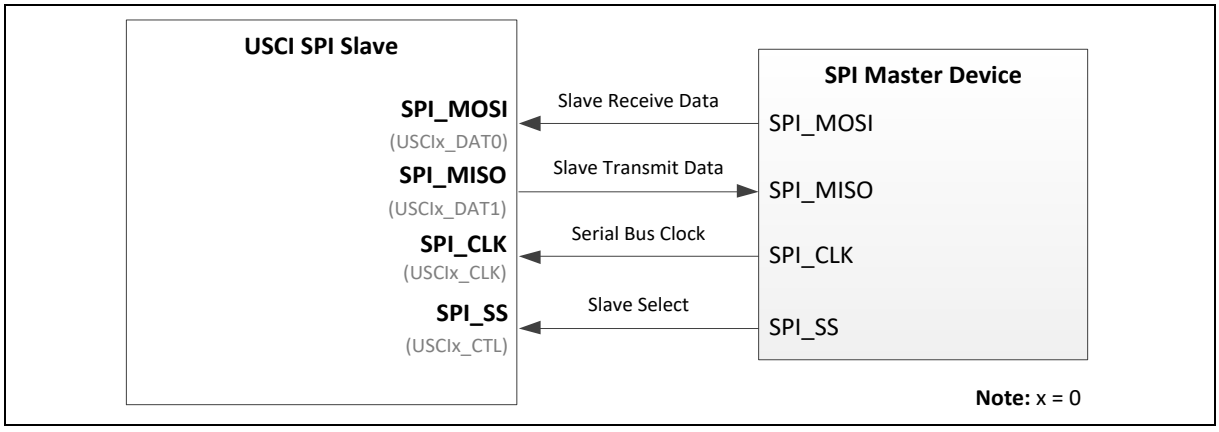


Figure 6.17-2 SPI Slave Mode Application Block Diagram

6.17.2 Features

- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports PDMA transfer

- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.18 USCI - I²C Mode

6.18.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.18-1 for more detailed I²C BUS Timing.

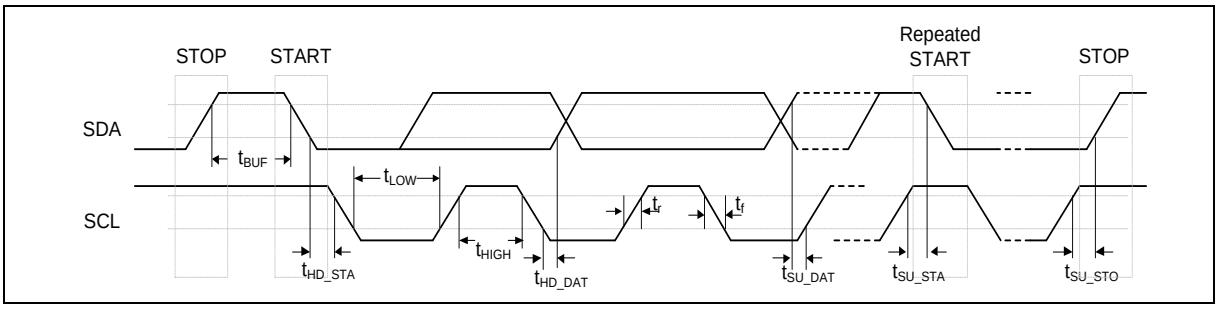


Figure 6.18-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enabling this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.18.2 Features

- Full master and slave device capability
- Supports 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffers for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.19 USB 2.0 Full-Speed Device Controller (USBD)

6.19.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports control/bulk/interrupt/isochronous transfer types.

In this device controller, there are two main interfaces: APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1 Kbytes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEG0~16).

There are 17 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, etc., and BUS events, such as suspend and resume, etc. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurred, and then check the related USB Endpoint Status Register (USBD_EPSTS0 and USBD_EPSTS1) to acknowledge what kind of event occurred in this endpoint.

A software-disconnect function is supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, the host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.19.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (SOF, NEVWK, VBUSDET, USB and BUS)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 17 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1 Kbytes buffer size
- Provides remote wake-up capability

6.20 Controller Area Network with Feasibility Data Rate (CAN FD)

6.20.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and needs to be connected to additional transceiver hardware for the CAN bus physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.20.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.21 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.21.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR ADC converter) with 12 external input channels and 2 internal channels. The ADC converter can be started by software trigger, PWM0/1 triggers, BPWM0/1 triggers, Timer0~3 overflow pulse triggers, ADINT0, ADINT1 interrupt EOC (End of conversion) pulse trigger and external pin (EADC0_ST) input signal.

6.21.2 Features

- Analog input voltage range: 0~AV_{DD}
- Reference voltage from AV_{DD} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 12 single-end analog external input channels
- 2 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP})
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses
- Maximum EADC clock frequency is 16 MHz
- Up to 730 KSPS conversion rate.
- Up to 4 sample modules:
  - Each of sample is configurable for EADC converter channel EADC_CH0~7,12~15 and trigger source
  - Sample module 16, 17 is fixed for EADC channel 16, 17 input sources as band-gap voltage, temperature sensor.
  - Configurable sampling time for each sample module
  - Supports left-adjusted result
  - 12-bit resolution for conversion result and 16-bit resolution for accumulated conversion result
  - Conversion results are held in 19 data registers with valid and overrun indicators
  - Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- An ADC conversion can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~3)
  - Write 1 to INTSWTRGn (EADC_SWTRG[n], n = 16,17) for internal channel
  - External pin EADC0_ST
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - BPWM0 triggers
- Supports configurable PDMA transfer
- Auto turn on/off EADC power at power off or operation mode with wait state(10us stable time)
- Supports digital comparator to monitor conversion result and user can select whether to generate an interrupt when conversion result matches the compare register setting

6.22 CRC Controller (CRC)

6.22.1 Overview

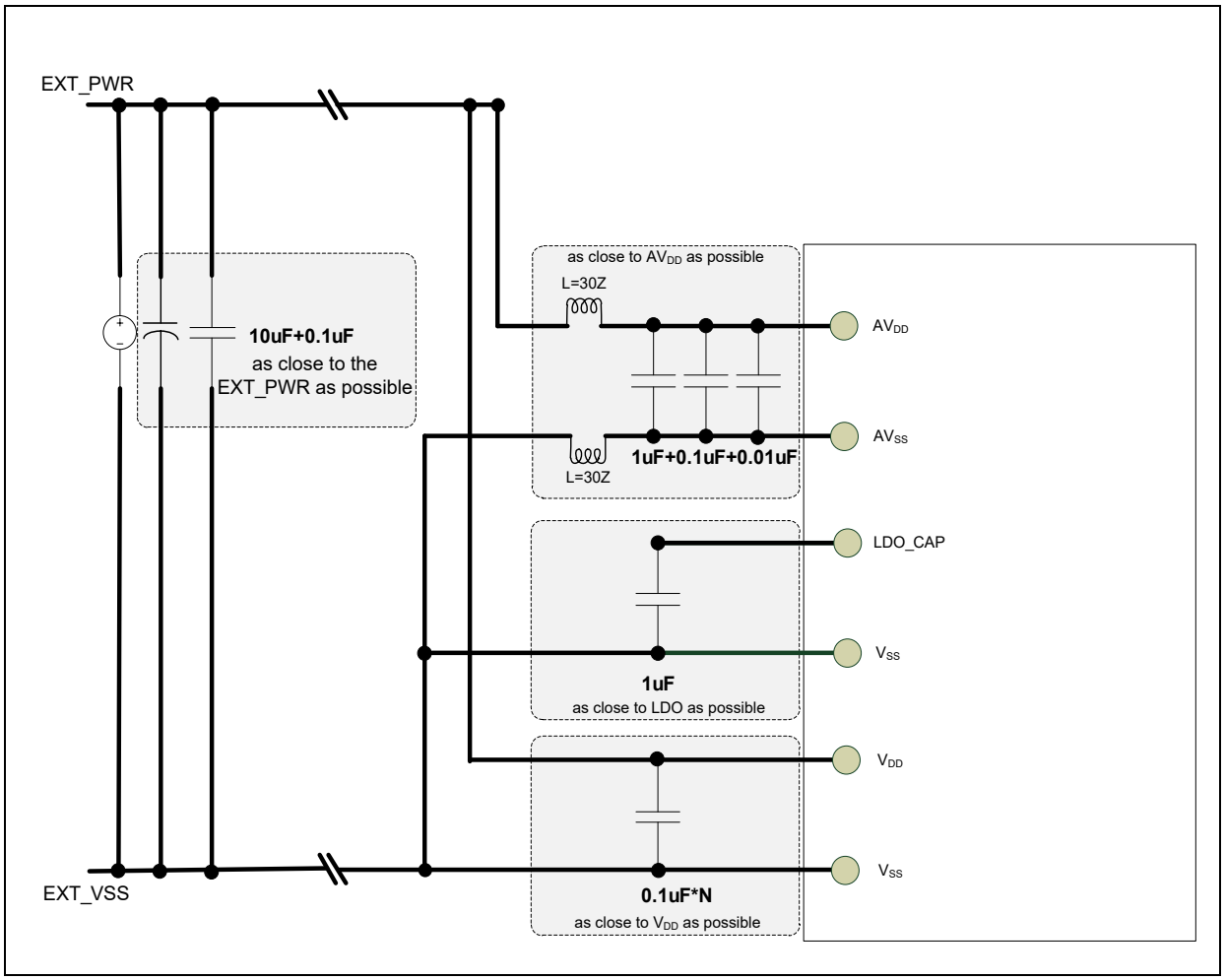
The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.22.2 Features

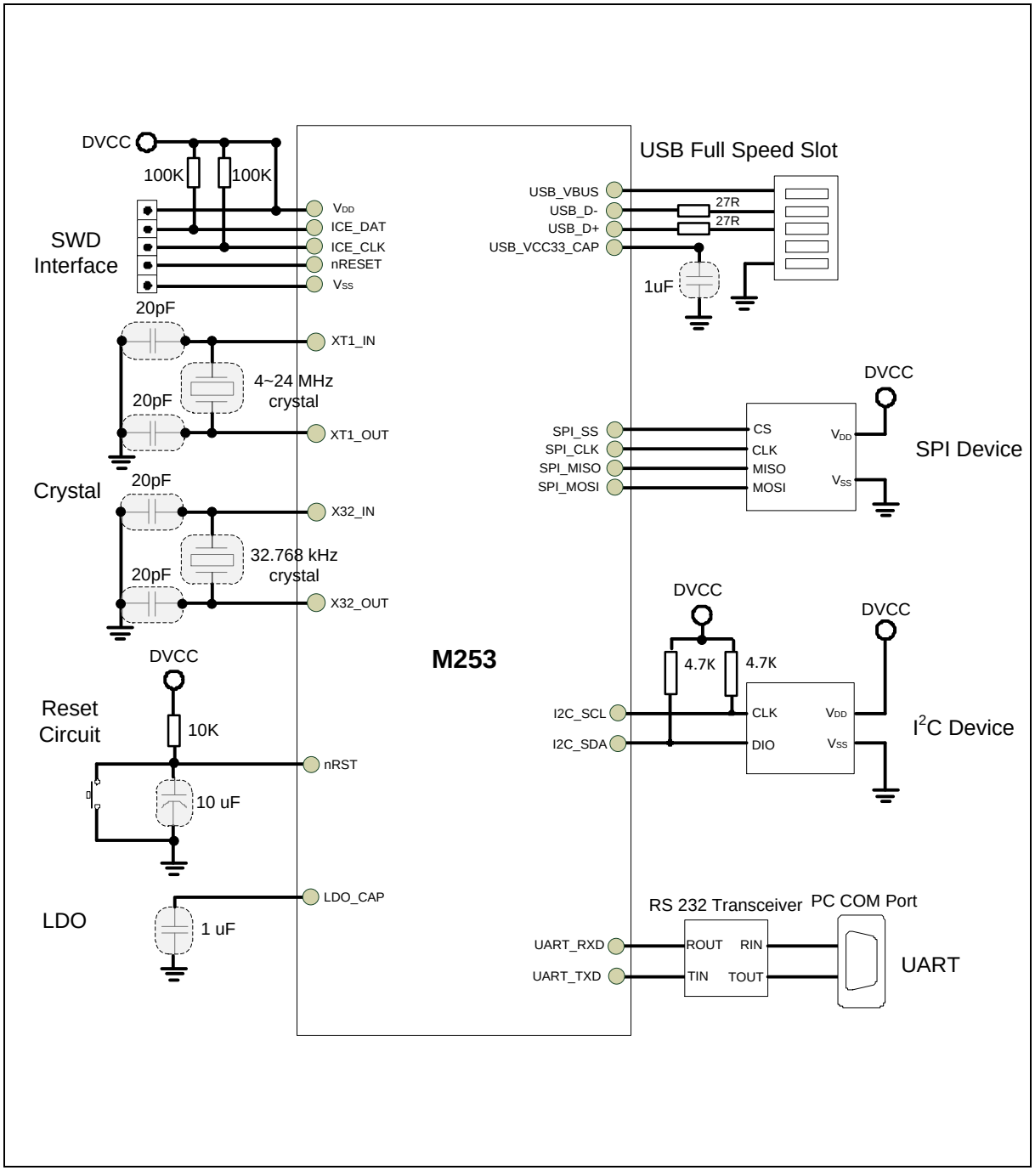
- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current.

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

1. T_A = ambient temperature (°C)
2. θ_{JA} = thermal resistance junction-ambient (°C/Watt)
3. P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 33-pin QFN(5x5 mm)	-	39.6	-	°C/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	°C/Watt

Note:
1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

1. A supply overvoltage is applied to each power supply pin
2. A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

1. Inductive loads:
   - Relays, switch contactors
   - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-750	-	+750	
LU[*3]	Pin current for latch-up[*3]	-100 @ Class I	-	+100 @ Class I	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity (MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
33-pin QFN(5x5 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

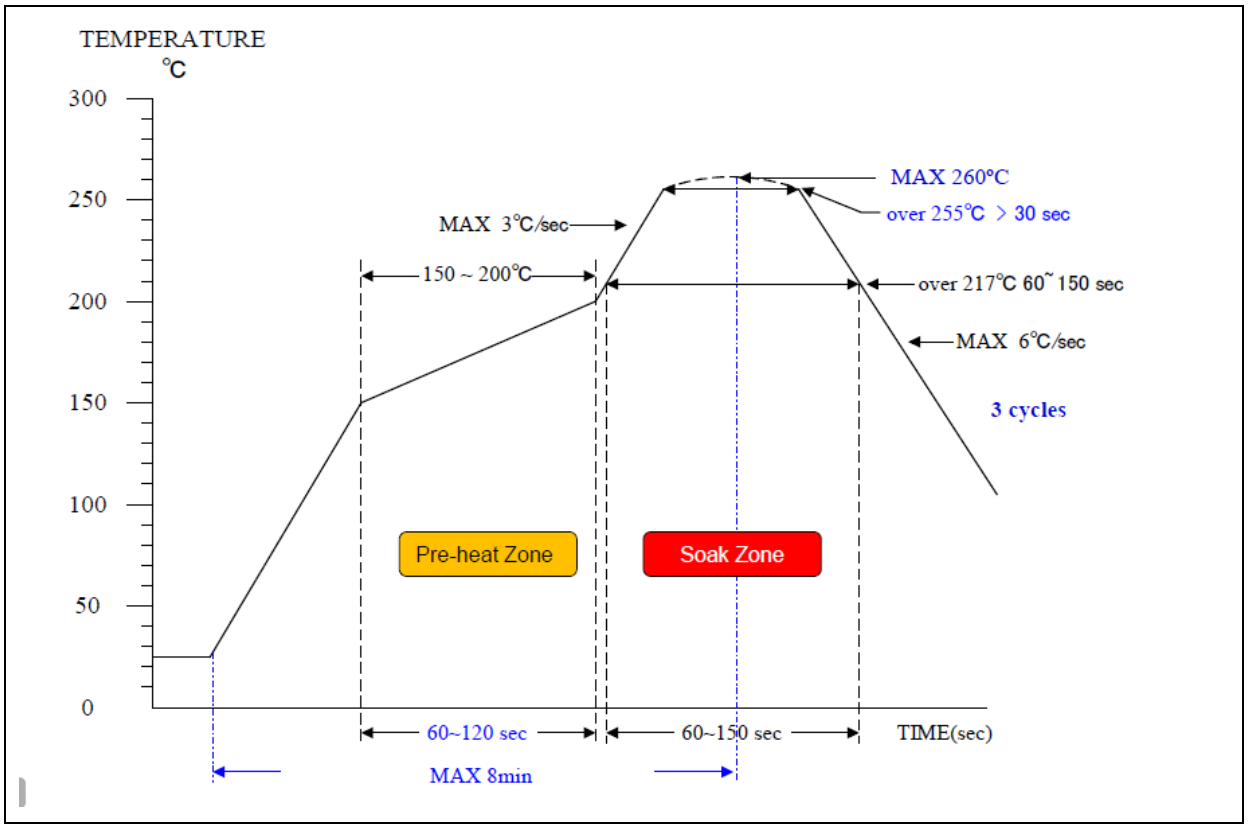


Figure 8.1-1 Soldering profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C /sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6°C /sec ax.
Time 25°C to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.75 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	1.75	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{LDO}	LDO output voltage	-	1.5	-		
V_{BG}	Band-gap voltage	795	815	840	mV	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	60	150	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	1.8	-	µC	V_{DD} = 1.8 V, T_A = 105 °C, I_{RUSH} = 60 mA for 30 µs

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

1. All GPIO pins are in push pull mode and output high.
2. The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.75 ~ 5.5 V unless otherwise specified.
3. $V_{DD} = AV_{DD} = V_{DDIO}$
4. When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
5. Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable. HCLK is set as HIRC, PLL or HXT clock.	48 MHz	5.15	6.8	6.85	6.9	mA
		32 MHz	3.88	5.3	5.35	5.4	
		24 MHz	3.00	4.0	4.05	4.1	
		12 MHz	1.90	2.5	2.55	2.6	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable. HCLK is set as MIRC clock.	4 MHz	0.62	0.87	0.92	0.97	
		2 MHz	0.43	0.62	0.67	0.72	
		1 MHz	0.34	0.48	0.53	0.58	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable. HCLK is set as HIRC, PLL or HXT clock.	48 MHz	12.58	16.5	16.55	16.6	
		32 MHz	8.46	13	13.05	13.1	
		24 MHz	7.03	9.2	9.25	9.3	
		12 MHz	4.21	5.6	5.65	5.7	
	Normal run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable. HCLK is set as MIRC clock.	4 MHz	1.18	1.7	1.75	1.8	
		2 MHz	0.72	1.0	1.05	1.1	
		1 MHz	0.48	0.70	0.75	0.80	

Note:

1. When analog peripheral blocks such as USB, ADC, ACMP, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	

I_{DD_IDLE}	Idle mode with PL0 (PLSEL = 00), all peripherals disable. HCLK is set as HIRC, PLL or HXT clock.	48 MHz	1.23	1.7	1.75	1.8	mA
		32 MHz	1.26	1.55	1.6	1.65	
		24 MHz	1.03	1.3	1.35	1.4	
		12 MHz	0.91	1.15	1.2	1.25	
	Idle mode with PL0 (PLSEL = 00), all peripherals disable. HCLK is set as MIRC clock.	4 MHz	0.28	0.4	0.45	0.5	
		2 MHz	0.27	0.38	0.43	0.48	
		1 MHz	0.26	0.37	0.42	0.47	
	Idle mode with PL0 (PLSEL = 00), all peripherals enable. HCLK is set as HIRC, PLL or HXT clock.	48 MHz	8.27	10.8	10.85	10.9	
		32 MHz	5.65	7.7	7.75	7.8	
		24 MHz	4.82	6.4	6.45	6.5	
		12 MHz	3.05	3.9	3.95	4.0	
	Idle mode with PL0 (PLSEL = 00), all peripherals enable. HCLK is set as MIRC clock.	4 MHz	0.83	1.15	1.2	1.25	
		2 MHz	0.54	0.75	0.8	0.85	
		1 MHz	0.40	0.55	0.6	0.65	

Note:

1. When analog peripheral blocks such as USB, ADC, PLL, HIRC, MIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 38.4 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	1.5	4.0	30	60	µA
	Power-down mode, RTC enable and run	V	-	3.0	5.5	32	62	
	Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	4.2	6.7	33	63	
	Power-down mode, WDT/Timer/UART enable and run	-	V	4.3	6.9	33	63	
	Power-down mode, WDT/Timer/UART/RTC enable and run, WDT use LIRC, UART/Timer/RTC use LXT	V	V	5.6	9.0	35	65	
I_{DD_FWPD}	Fast wake up Power-down mode, all peripherals disable	-	-	100	140	166	196	µA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run, WDT use LIRC, UART/Timer/RTC use LXT	V	V	105	145	171	201	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L3 gain level
2. V_{DD} = AV_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, ADC are ON, an additional power consumption should be considered.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

1. The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
2. All GPIO pins are set as output high of push pull mode without multi-function.
3. HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1}$ = f_{HCLK}.
4. The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on.
5. The peripheral clock selection keeps reset default setting.

Peripheral	I_{DD}[*1]	Unit
PDMA	186	µA
ISP	~0	
EXST	175	
CRC	34	
FMCIDLE	163	
MCAN	1180	
GPA	52	
GPB	59	
GPC	54	
GPF	56	
WDT	213	
RTC	167	
TMR0	356	
TMR1	355	
TMR2	421	
TMR3	427	
CLKO	204	
I2C0	137	
I2C1	144	
SPI0	644	
UART0	639	
UART1	637	
UART2	593	
UART3	653	
UART4	478	
USBD[*4]	1353	
EADC[*2]	367	

USCI0	205	
BPWM0	176	

Note:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the USB is turned on, add an additional power consumption per USB for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_DPD}[*1][*2]	Wakeup from deep Power-down mode	190	250	µs
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	19	30	
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	12	15	

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first

Table 8.3-5 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.8 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		0.8	-	V_{DD}		V_{DD} = 1.8 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 5 V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	45	52	59	kΩ	
R_{PD}[*1]	Pull down resistor	45	52	59	kΩ	

Note:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-7.0	-7.75	-9	µA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-7.0	-7.7	-9	µA	V_{DD} = 2.7 V V_{IN} = (V_{DD} - 0.4) V
		-7.0	-7.6	-9	µA	V_{DD} = 1.8 V V_{IN} = (V_{DD} - 0.4) V
	Source current for push-pull mode and high level	-5	-8	-11	mA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-3.7	-5.2	-6.7	mA	V_{DD} = 2.7 V V_{IN} = (V_{DD} - 0.4) V
		-2.2	-3.2	-4.2	mA	V_{DD} = 1.8 V V_{IN} = (V_{DD} - 0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	13	20	25	mA	V_{DD} = 4.5 V V_{IN} = 0.4 V
		8.5	13	16.5	mA	V_{DD} = 2.7 V V_{IN} = 0.4 V
		5	8	10	mA	V_{DD} = 1.8 V V_{IN} = 0.4 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	45	52	59	kΩ	
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	µs	Normal run and Idle mode
		-	24	-		Fast wake up Power-down mode
		-	TBD	-		Power-down mode
		-	0.1	-		Deep Power-down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to use 10 kΩ pull-up resistor and 10 µF capacitor on nRESET pin

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3 V
		-2[*1]	-	2[*1]	%	T_A = -20 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V
		-2.5[*1]	-	2.5[*1]	%	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V
I_{HRC}[*1]	Operating current	-	500	800	µA	
T_S[*2]	Stable time	-	14	16	µs	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.4.2 4 MHz Internal Median Speed RC Oscillator (MIRC)

The 4 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
F_{MRC}	Oscillator frequnecy	3.951	4.032	4.112	MHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3 V
		-10[*1]	-	10[*1]	%	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V
I_{MRC}[*1]	Operating current	-	-	30	µA	
T_S[*2]	Stable time	-	-	24	µs	T_A = -40 °C ~ +105 °C, V_{DD} = 1.75 V ~ 5.5 V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-2 4 MHz Internal Median Speed RC Oscillator (MIRC) Characteristics

8.4.3 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3 V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3 V
		-15	-	15	%	T_A = -40 °C ~ 105 °C V_{DD} = 1.75 V ~ 5.5 V Without software calibration
I_{LRC}	Operating current	-	0.85	1	µA	V_{DD} = 3.3 V
T_S	Stable time	-	-	70	µs	T_A = -40 °C ~ 105 °C V_{DD} = 1.75 V ~ 5.5 V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-3 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.4 External 4~32 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 32 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.75	-	5.5	V	
R_f	Internal feedback resister	-	1000	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	32	MHz	
I_{HXT}	Current consumption	-	45	150	µA	4 MHz, Gain = L0, C_L = 12.5 pF, ESR = 120 Ω
		-	80	250		8 MHz, Gain = L1, C_L = 12.5 pF, ESR = 60 Ω
		-	150	430		12 MHz, Gain = L2, C_L = 12.5 pF, ESR = 25 Ω
		-	230	600		16 Mhz, Gain = L3, C_L = 12.5 pF, ESR = 25 Ω
		-	280	760		24 MHz, Gain = L4, C_L = 12.5 pF, ESR = 25 Ω
		-	630	1550		32 MHz, Gain = L7, C_L = 12.5 pF, ESR = 25 Ω
T_S	Stable time	-	2550	2950	µs	4 MHz, Gain = L0, C_L = 12.5 pF, ESR = 120 Ω
		-	900	1250		8 MHz, Gain = L1, C_L = 12.5 pF, ESR = 60 Ω
		-	550	850		12 MHz, Gain = L2, C_L = 12.5 pF, ESR = 25 Ω
		-	400	700		16 Mhz, Gain = L3, C_L = 12.5 pF, ESR = 25 Ω
		-	300	650		24 MHz, Gain = L4, C_L = 12.5 pF, ESR = 25 Ω
		-	250	610		32 MHz, Gain = L7, C_L = 12.5 pF, ESR = 25 Ω
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	-	1.6	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-4 External 4~32 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	60		Crystal @8 MHz, C_L = 12.5 pF, Gain = L1
		-	-	25		Crystal @12 MHz, C_L = 12.5 pF, Gain = L2
		-	-	25		Crystal @16 MHz, C_L = 12.5 pF, Gain = L3
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L4
		-	-	25		Crystal @32 MHz, C_L = 12.5 pF, Gain = L7

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

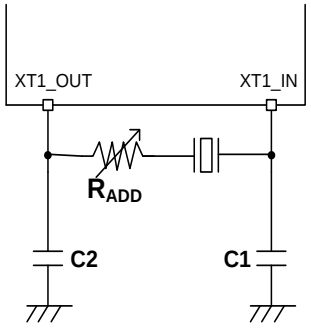


Table 8.4-5 External 4~32 MHz High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 32 MHz	10 ~ 20 pF	10 ~ 20 pF	without

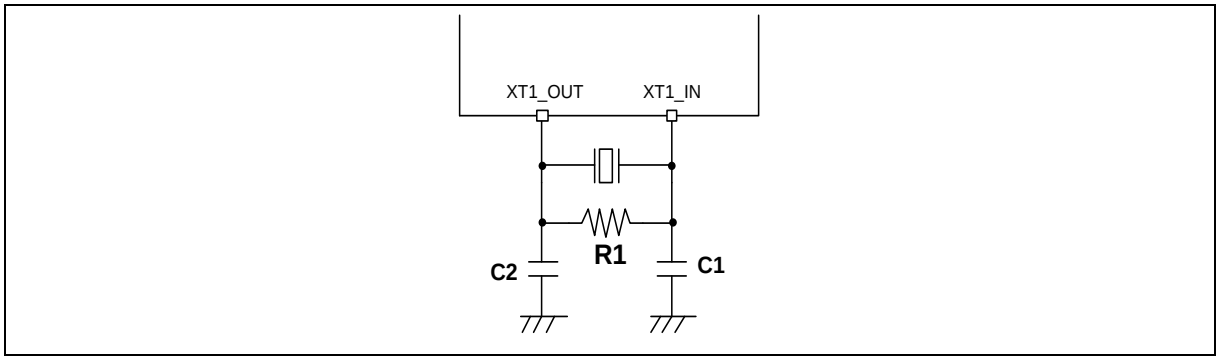
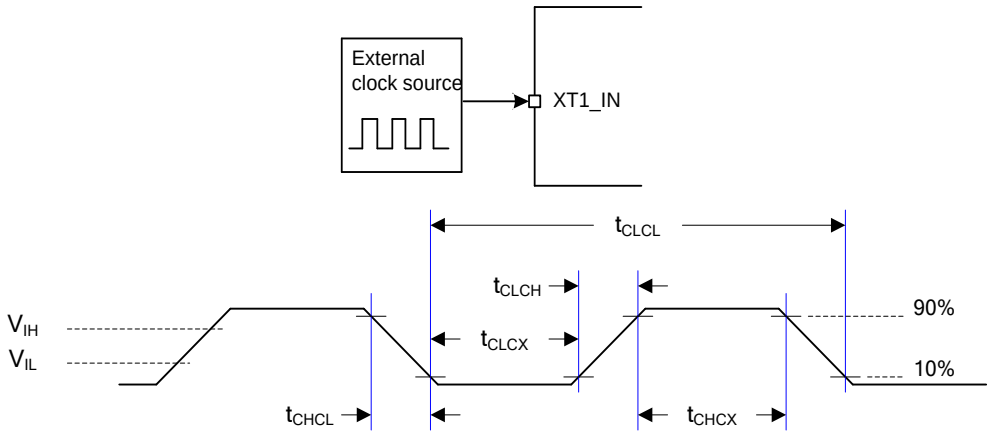


Figure 8.4-1 Typical Crystal Application Circuit

8.4.5 External 4~32 MHz High Speed Clock Input Signal Characteristics

For clock input mode, the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal needs to follow Table 8.4-6. The characteristics result from tests performed uses a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	32	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 4~32 MHz High Speed Clock Input Signal

8.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	1.75	-	5.5	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption from V_{DD}	-	0.6	2.0	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	0.74	2.5		ESR=70 kΩ, C_L = 12.5 pF, Gain = L2
		-	1	3.0		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
Ts_{LXT}	Stable time	-	2	-	s	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp} [*1]	Peak-to-peak amplitude	-	0.4	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-8 External 32.768 kHz Low Speed Crystal Characteristics

8.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

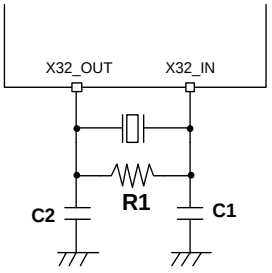
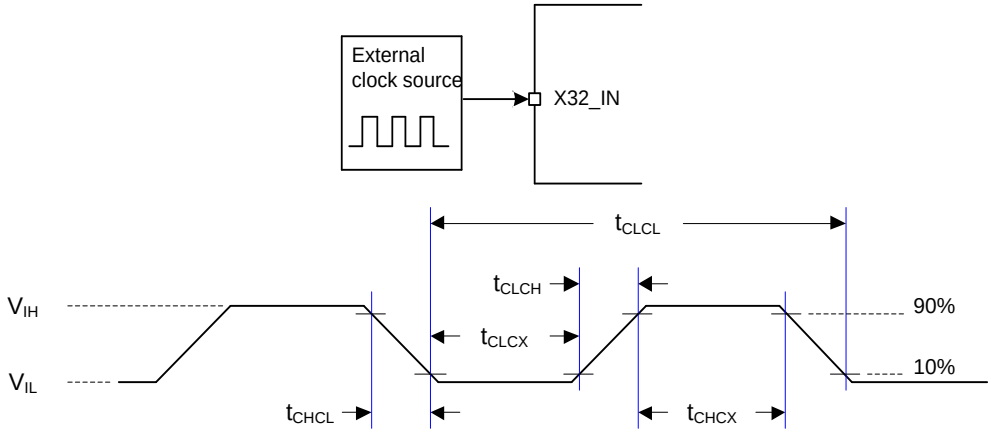


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillinator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal needs to follow Table 8.4-9. The characteristics result from tests performed uses a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	ns	
t_{CLCX}	Clock low time	450	-	-	ns	
t_{CLCH}	Clock rise time	-	-	50	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	ns	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production.

Table 8.4-9 External 32.768 kHz Low Speed Clock Input Signal

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	6.5	ns	C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	10		C_L = 30 pF, V_{DD} >= 2.7 V
		-	7		C_L = 10 pF, V_{DD} >= 2.7 V
		-	16.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	11.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	5		C_L = 30 pF, V_{DD} >= 4.5 V
		-	3.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	8		C_L = 30 pF, V_{DD} >= 2.7 V
		-	5		C_L = 10 pF, V_{DD} >= 2.7 V
		-	12.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	8		C_L = 10 pF, V_{DD} >= 1.8 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	-	7.5	ns	C_L = 30 pF, V_{DD} >= 4.5 V
		-	5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	12		C_L = 30 pF, V_{DD} >= 2.7 V
		-	8		C_L = 10 pF, V_{DD} >= 2.7 V
		-	20.5		C_L = 30 pF, V_{DD} >= 1.8 V
		-	13.5		C_L = 10 pF, V_{DD} >= 1.8 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	-	6.5	ns	C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.5		C_L = 10 pF, V_{DD} >= 4.5 V
		-	10		C_L = 30 pF, V_{DD} >= 2.7 V
		-	6.5		C_L = 10 pF, V_{DD} >= 2.7 V
		-	18		C_L = 30 pF, V_{DD} >= 1.8 V
		-	10.5		C_L = 10 pF, V_{DD} >= 1.8 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	47	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	70		C_L = 10 pF, V_{DD} >= 4.5 V
		-	30		C_L = 30 pF, V_{DD} >= 2.7 V
		-	44		C_L = 10 pF, V_{DD} >= 2.7 V
		-	18		C_L = 30 pF, V_{DD} >= 1.8 V

		-	26		C_L = 10 pF, V_{DD} >= 1.8 V
	I/O maximum frequency (High Slew Rate)	-	55	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	80		C_L = 10 pF, V_{DD} >= 4.5 V
		-	36		C_L = 30 pF, V_{DD} >= 2.7 V
		-	56		C_L = 10 pF, V_{DD} >= 2.7 V
		-	21		C_L = 30 pF, V_{DD} >= 1.8 V
		-	35		C_L = 10 pF, V_{DD} >= 1.8 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-10 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.75	-	5.5	V	
V_{LDO}	Output voltage	-	1.5	-	V	
T_A	Temperature	-40	-	105	°C	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in Table 8.5-1 are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	70	100	μA	AV_{DD} = 5.5V
I_{LVR}[*1]	LVR operating current	-	0.3	3		AV_{DD} = 5.5V
I_{BOD}[*1]	BOD operating current	-	40	60		AV_{DD} = 5.5V, Normal mode
		-	3	6		AV_{DD} = 5.5V, Low Power mode
V_{POR}	POR reset voltage	1.40	1.5	1.65	V	-
V_{LVR}	LVR reset voltage	1.55	1.6	1.7		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	1.70	1.80	1.90		BODVL = 1
		1.90	2.00	2.10		BODVL = 2
		2.30	2.40	2.50		BODVL = 3
		2.60	2.70	2.80		BODVL = 4
		2.90	3.00	3.10		BODVL = 5
		3.60	3.70	3.80		BODVL = 6
		4.25	4.40	4.50		BODVL = 7
	BOD brown-out detect voltage (Rising edge)	1.76	1.88	2.00		BODVL = 1
		1.96	2.08	2.20		BODVL = 2
		2.36	2.48	2.60		BODVL = 3
		2.66	2.78	2.90		BODVL = 4
		2.96	3.08	3.20		BODVL = 5
		3.66	3.78	3.90		BODVL = 6
		4.31	4.48	4.60		BODVL = 7

T_{LVR_SU}[*1]	LVR startup time	-	200	2000	µs	-
T_{LVR_RE}[*1]	LVR respond time	-	20	50		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	2000		-
T_{BOD_RE}[*1]	BOD respond time	-	1	2		Normal mode, BODDGSEL = 3, HCLK = 48 MHz,
		-	-	30000		Low Power mode
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	20000	µs/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled
		250	-	-		LVR Enabled
		10	-	-		BOD Enabled at Normal mode, BODDGSEL = 3, HCLK = 48 MHz,

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and power control unit

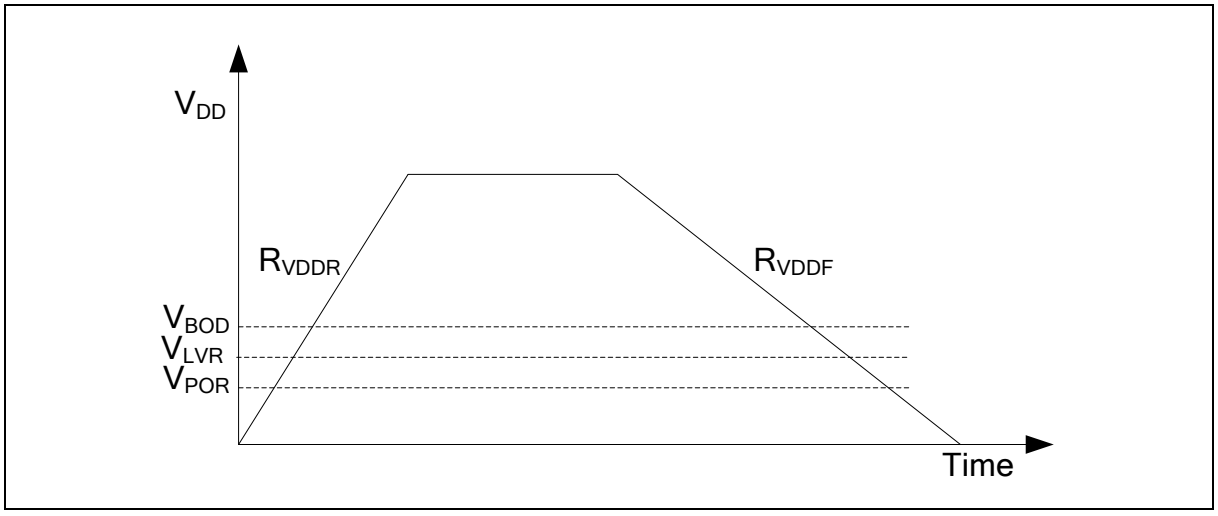


Figure 8.5-1 Power Ramp Up/Down Condition

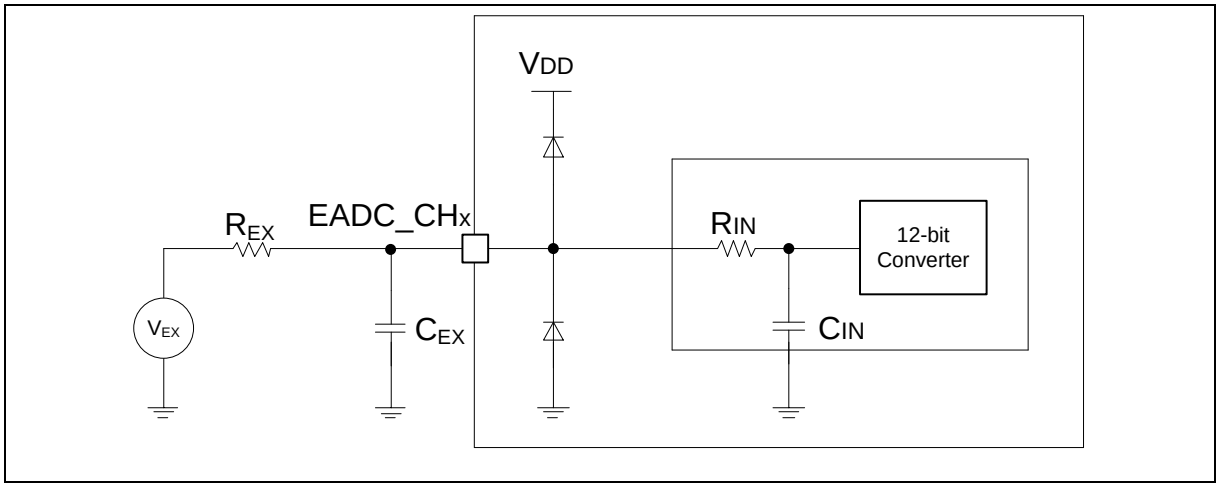
8.5.3 12-bit SAR Analog to Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	°C	
AV_{DD}	Analog operating voltage	1.75	-	5.5	V	$V_{DD} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	AV_{DD}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} current)	-	1000	TBD	µA	$AV_{DD} = V_{DD}$ = 3.3 V F_{ADC} = 16 MHz $T_{CONV} = 22 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	4	-	16	MHz	
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	22	-	277	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 21 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	30	-	730	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}	Enable to ready time	32	-	-	$1/F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-3	-	+3	LSB	
DNL[*1]	Differential Non-Linearity Error	-1	-	+3	LSB	
E_G[*1]	Gain error	-6	-	+6	LSB	
E_O[*1]$_T$	Offset error	-3	-	+3	LSB	
E_A[*1]	Absolute Error	-1.5	-	+6.5	LSB	
ENOB[*1]	Effective number of bits	10	-	-	bits	F_{ADC} = 16 MHz $AV_{DD} = V_{DD}$ = 3.3 V R_{EX} = 50 Ω Input Frequency = 10 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	64	-	dB	
SNR[*1]	Signal-to-noise ratio	-	64	-		
THD[*1]	Total harmonic distortion	-	-65	-		
C_{IN}[*1]	Internal Capacitance	-	26	30	pF	
R_{IN}[*1]	Internal Switch Resistance	-	0.5	-	kΩ	
R_{EX}[*1]	External input impedance	-	-	33	kΩ	

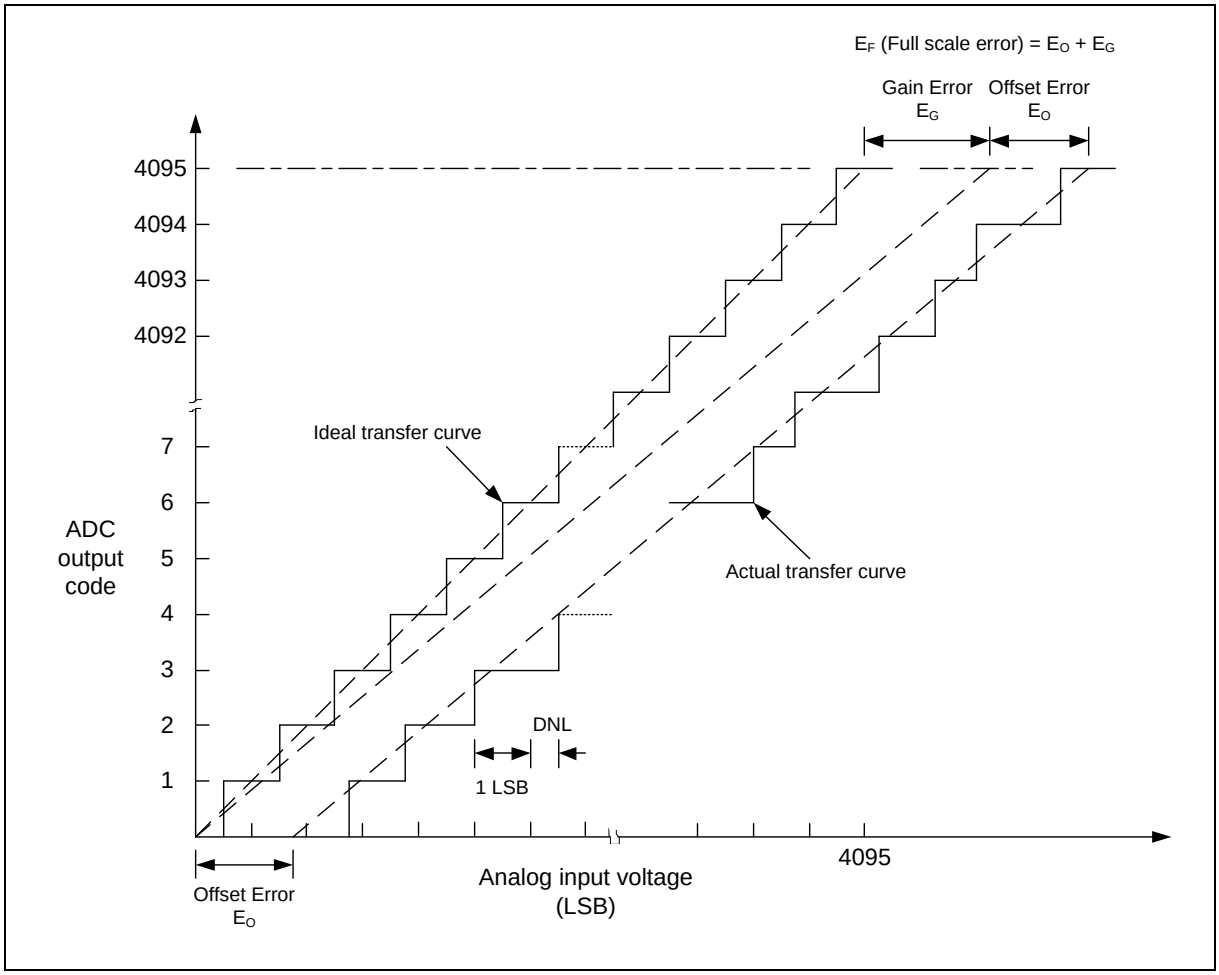
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Temperature Sensor

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	690	720	750	mV	T_A = 0 °C
T_C[*1]	Temperature Coefficient	-1.74	-1.83	-1.9	mV/°C	
I_{TEMP}[*1]	Operating current	-	16	30	μA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

8.6 Communications Characteristics

8.6.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	24		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	16		1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	4.5	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.5	ns	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4.5	ns	1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:
1. Guaranteed by design.

Table 8.6-1 SPI Master Mode Characteristics

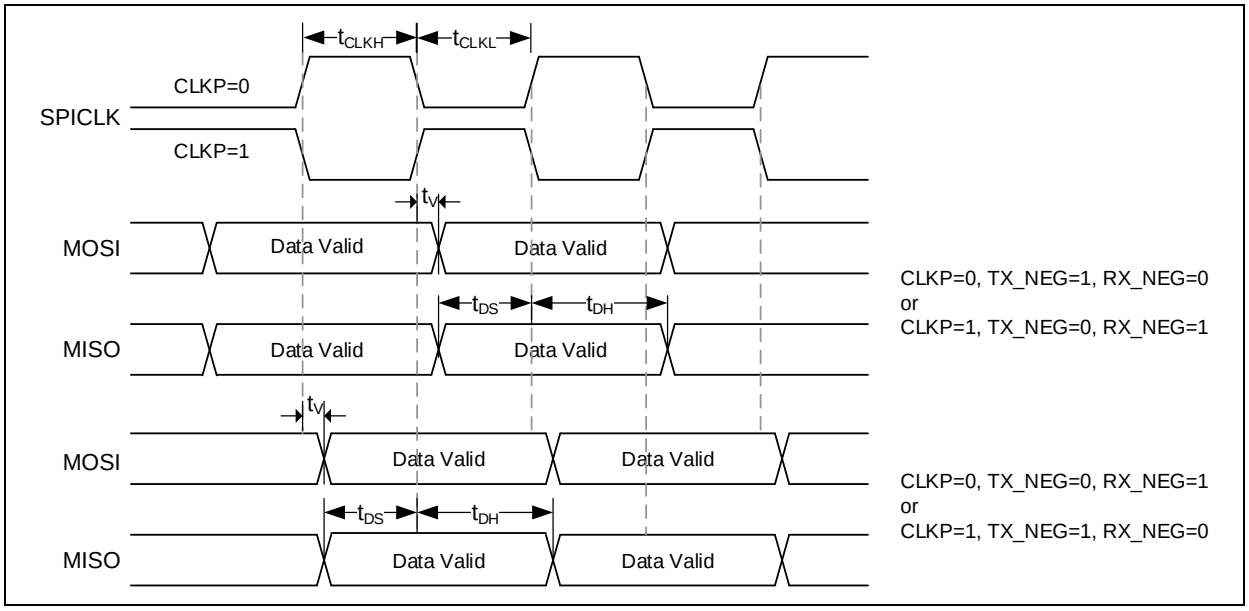


Figure 8.6-1 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	10	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	8		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	4		1.8 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 2ns	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	1.5	-	-	ns	
t_{DH}	Data input hold time	3.5	-	-	ns	
t_V	Data output valid time	-	-	35	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	42		2.7 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF
		-	-	74		1.8 V ≤ V_{DD} ≤ 5.5 V, CL = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 SPI Slave Mode Characteristics

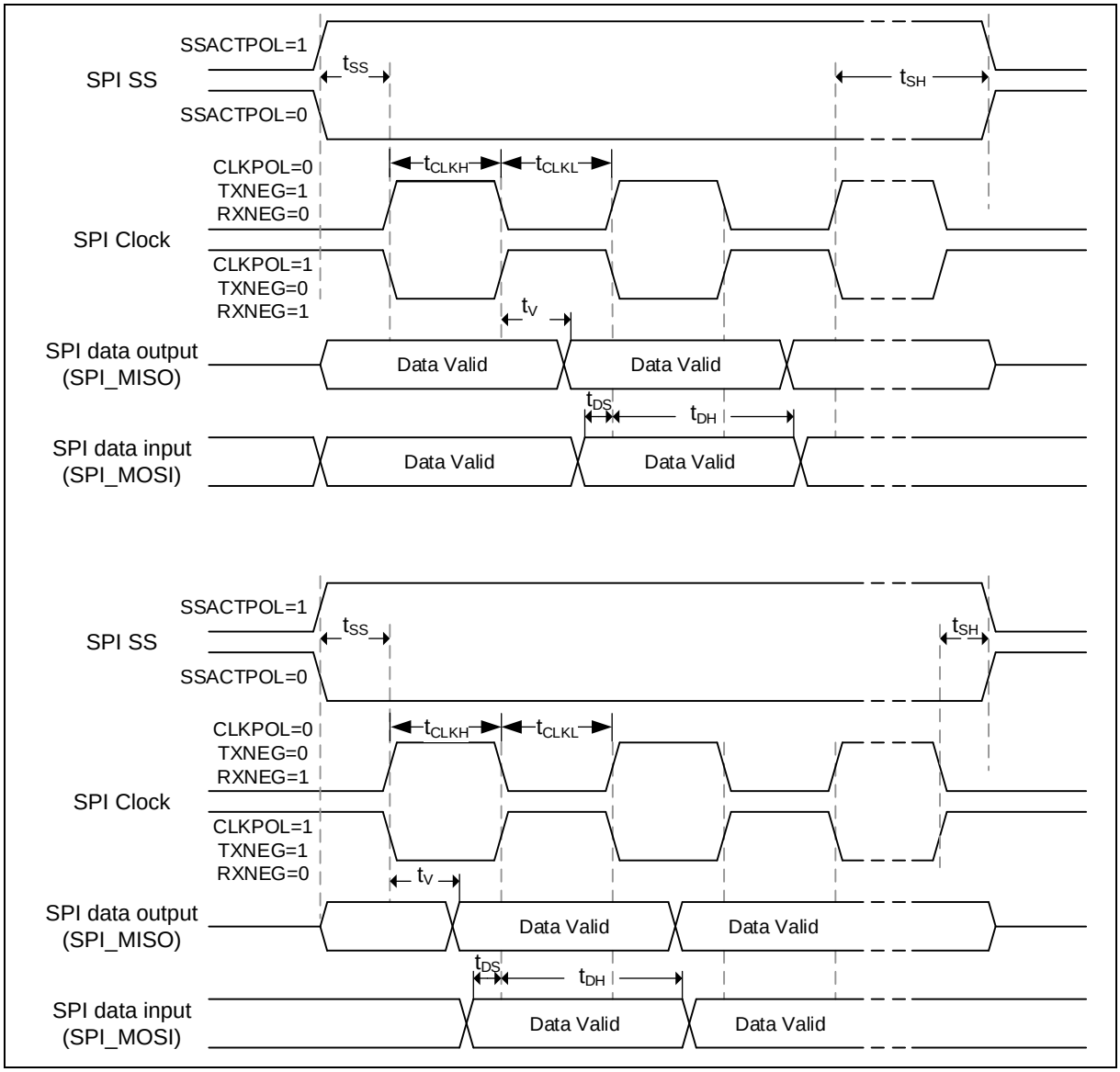


Figure 8.6-2 SPI Slave Mode Timing Diagram

8.6.2 SPI - I²S Dynamic Characteristics

Symbol	Parameter	Min [*1]	Max [*1]	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	80	-	ns	Master f_{PCLK} = 48 MHz, data: 24 bits, audio frequency = 128 kHz
$t_{w(CKL)}$	I²S clock low time	80	-		
$t_{v(WS)}$	WS valid time	2	6		Master mode
$t_{h(WS)}$	WS hold time	2	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD_SR)}$		7	-		Slave receiver
$t_{h(SD_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD_SR)}$		4	-		Slave receiver
$t_{v(SD_ST)}$	Data output valid time	-	25		Slave transmitter (after enable edge)
$t_{h(SD_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

Note:

1. Guaranteed by design.

Table 8.6-3 I²S Characteristics

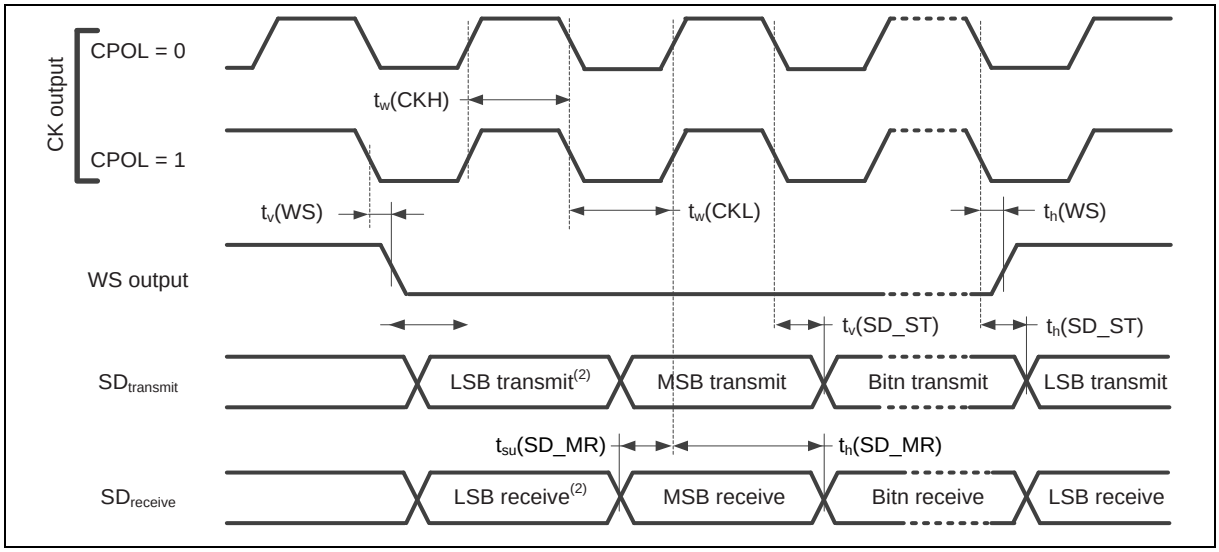


Figure 8.6-3 I²S Master Mode Timing Diagram

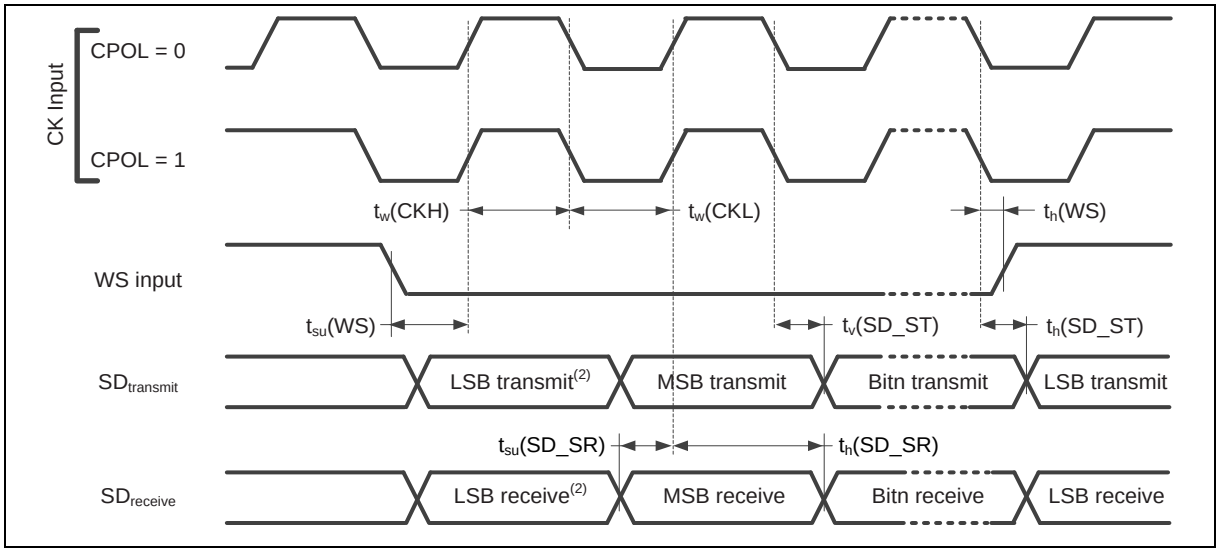


Figure 8.6-4 I²S Slave Mode Timing Diagram

8.6.3 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 I²C Characteristics

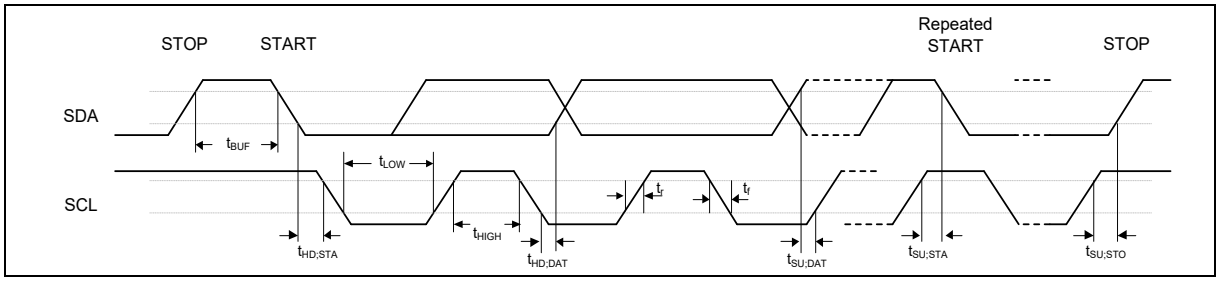


Figure 8.6-5 I²C Timing Diagram

8.6.4 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max[*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	24		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	16		1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	9	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	9	ns	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	8.5	ns	1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:
1. Guaranteed by design.

Table 8.6-5 USCI-SPI Master Mode Characteristics

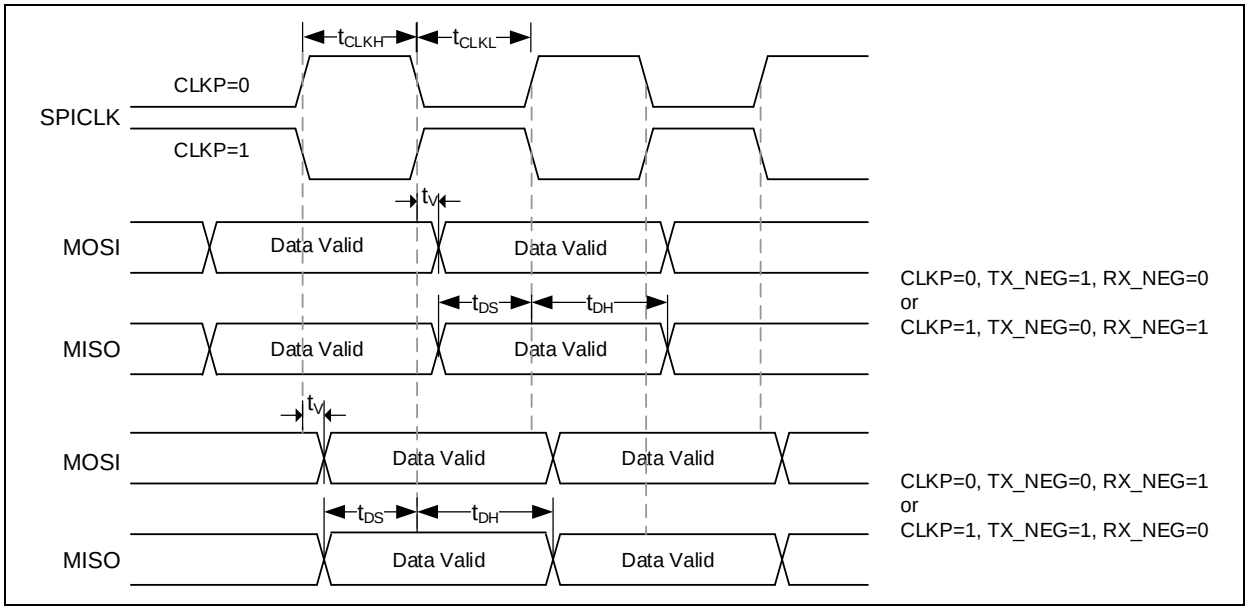


Figure 8.6-6 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	6	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	5		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	4		1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 2ns	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		1 T_{SPICLK} + 3ns	-	-		1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	4	-	-	ns	
t_V	Data output valid time	-	-	79	ns	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	88		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	117		1.8 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-6 USCI-SPI Slave Mode Characteristics

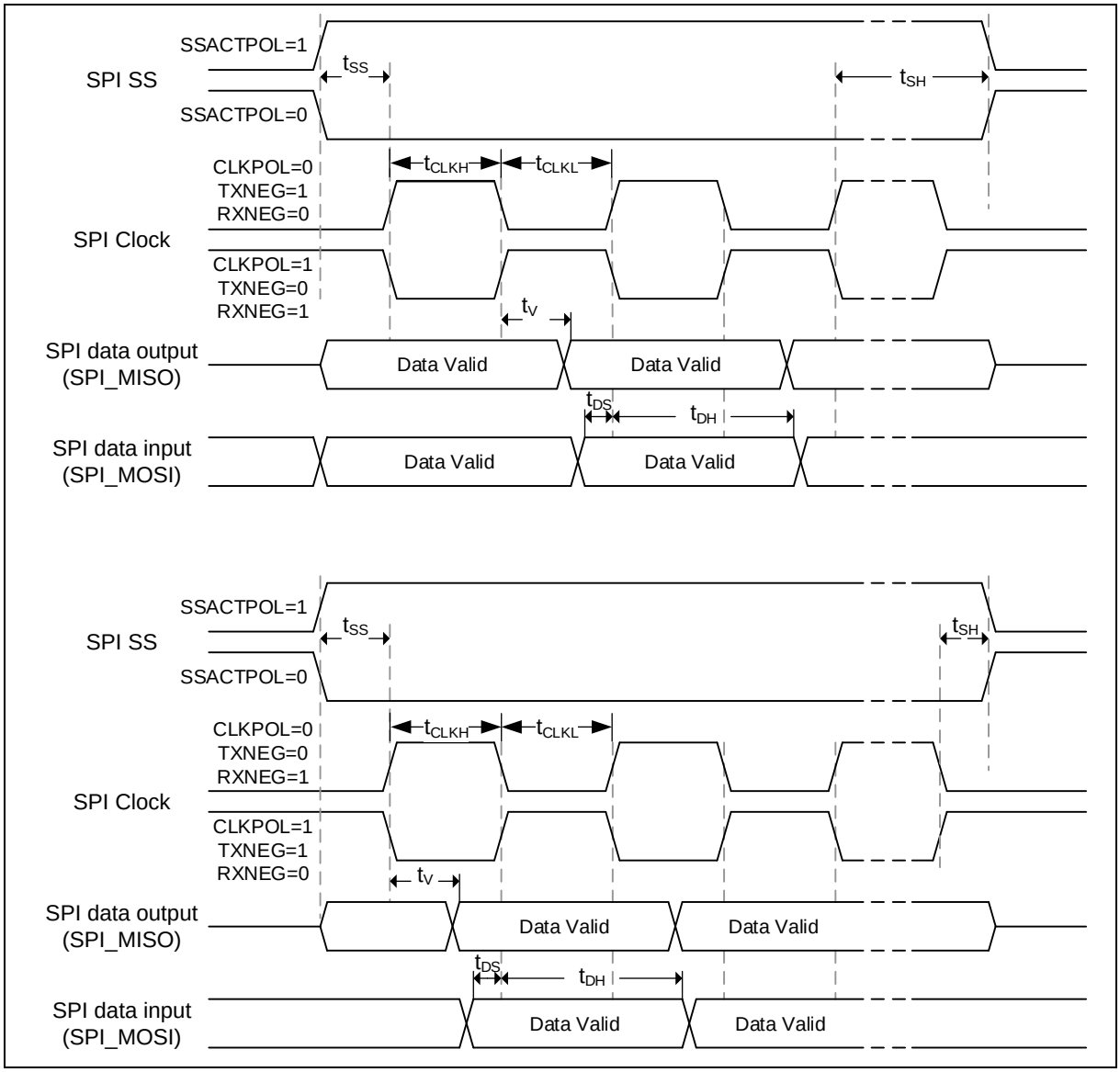


Figure 8.6-7 USCI-SPI Slave Mode Timing Diagram

8.6.5 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μs
t_{HIGH}	SCL high period	4	-	0.6	-	μs
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μs
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μs
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μs
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μs
$t_{SU;DAT}$	Data setup time	250	-	100	-	ns
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μs
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	ns
t_f	SCL/SDA fall time	-	300	-	300	ns
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-7 USCI-I²C Characteristics

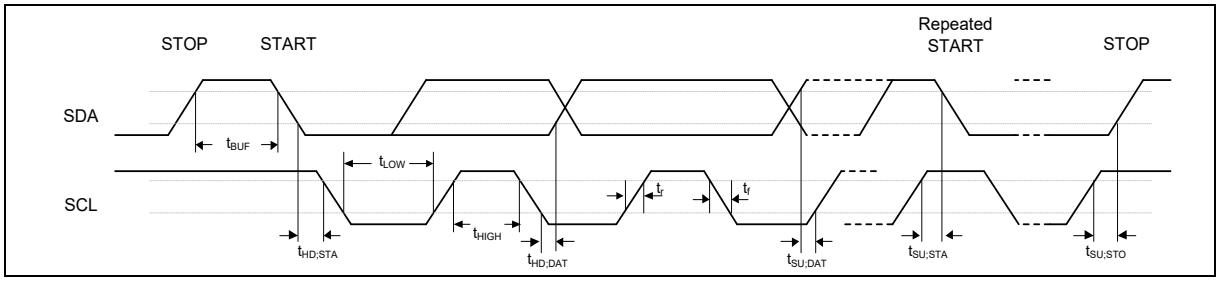


Figure 8.6-8 USCI-I²C Timing Diagram

8.6.6 USB Characteristics

8.6.6.1 USB Full-Speed Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BUS}	USB full speed transceiver operating voltage	4.4	-	5.25	V	-
V_{DD33}[*2]	USB Internal power regulator output	3.0	3.3	3.6	V	-
V_{IH}	Input high (driven)	2.0	-	-	V	-
V_{IL}	Input low	-	-	0.8	V	-
V_{DI}	Differential input sensitivity	0.2	-	-	V	|(USB_D+) - (USB_D-)|
V_{CM}	Differential common-mode range	0.8	-	2.5	V	Includes V_{DI} range
V_{SE}	Single-ended receiver threshold	0.8	-	2.0	V	-
	Receiver hysteresis	-	200	-	mV	-
V_{OL}	Output low (driven)	0	-	0.3	V	-
V_{OH}	Output high (driven)	2.8	-	3.6	V	-
V_{CRS}	Output signal cross voltage	1.3	-	2.0	V	-
R_{PU}	Pull-up resistor	1.19	-	1.9	kΩ	-
V_{TRM}	Termination voltage for upstream port pull-up (RPU)	3.0	-	3.6	V	-
Z_{DRV}[*3]	Driver output resistance	-	10	-	Ω	Steady state drive
C_{IN}	Transceiver capacitance	-	-	26	pF	Pin to GND

Note:

1. Guaranteed by characterization result, not tested in production.
2. To ensure stability, an external 1 µF output capacitor, 1 µF external capacitor must be connected between the USB_VDD33_CAP pin and the closest GND pin of the device.
3. USB_D+ and USB_D- must be connected with external series resistors to fit USB Full-speed spec request (28 ~ 44 Ω).

Table 8.6-8 USB Full-Speed Characteristics

8.6.6.2 USB Full-Speed PHY Characteristics

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
T_{FR}	rise time	4	-	20	ns	C_L = 50 pF
T_{FF}	fall time	4	-	20	ns	C_L = 50 pF
T_{FRFF}	rise and fall time matching	90	-	111.11	%	$T_{FRFF} = T_{FR}/T_{FF}$

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-9 USB Full-Speed PHY Characteristics

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.5	-	V	T_A = 25 °C
T_{ERASE}	Page erase time	-	4.2	-	ms	
T_{PROG}	Program time	-	42	-	µs	
I_{DD1}	Read current	-	3.15	-	mA	
I_{DD2}	Program current	-	3.5	-	mA	
I_{DD3}	Erase current	-	2	-	mA	
N_{ENDUR}	Endurance	20,000	-	-	cycles[2]	
T_{RET}	Data retention	10	-	-	year	20 kcycle[3] T_J = 125 °C
		20	-	-	year	20 kcycle[3] T_J = 105 °C

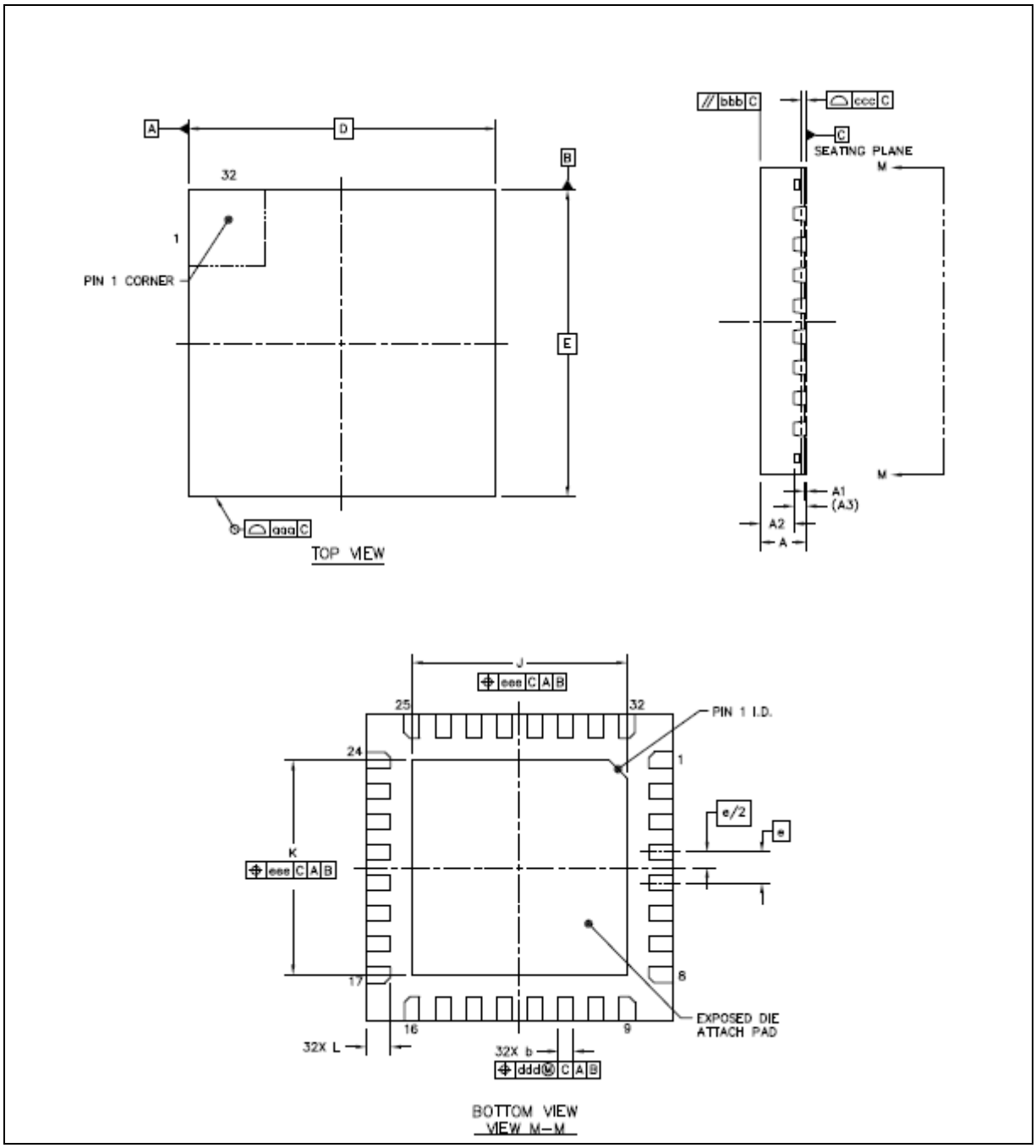
Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles.
3. Guaranteed by design.
4. The Erase/program command are only supported at power level 0.

9 PACKAGE DIMENSIONS

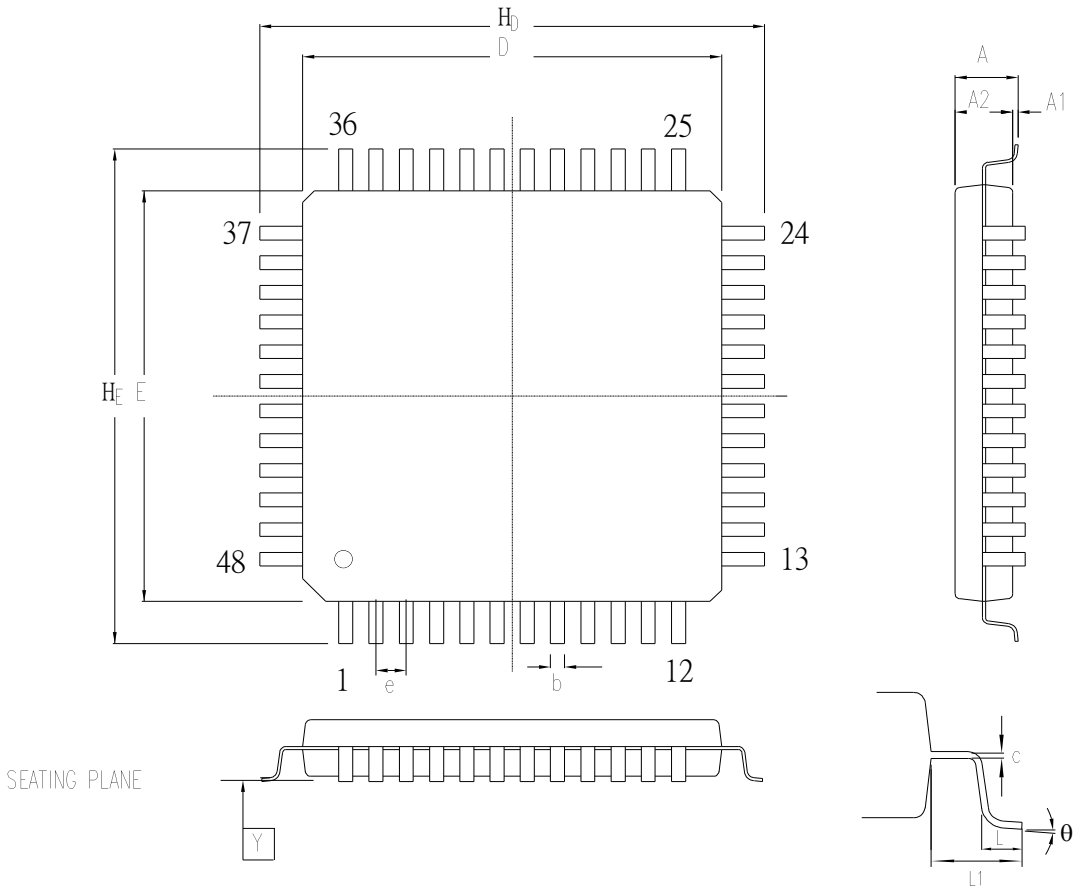
Package is Halogen-free, RoHS-compliant and TSCA-compliant.

9.1 QFN 33L (5x5x0.8 mm)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

9.2 LQFP 48L (7x7x1.4 mm Footprint 2.0 mm)



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	—	—	—	—
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~32 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2023.08.29	1.00	Initial version.
2025.02.06	1.01	Updated cover format.
2025.03.10	1.02	Updated the ”Kbytets” typo in chapter 1.

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