NuMicro® Family

Arm® Cortex®-M23-based Microcontroller

M2003 Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro M2003 series 32-bit microcontroller is based on Arm Cortex-M23 core with 32-bit hardware multiplier/divider. It runs up to 24 MHz and features 32 Kbytes Flash, 4 Kbytes SRAM, 2.4V to 5.5V operating voltage, and -40°C to 105°C operating temperature.

The M2003 series provides plenty of peripherals including 4 sets of 32-bit Timers, Watchdog Timers, 3-channel enhanced input capture, up to 2 sets of UART, 1 set of I^2C and 1 set of Universal Serial Control Interface (USCI) that can be set as UART/SPI/I^2C flexibly. Furthermore, all these communication interfaces have the individual FIFO to ensure the integrity of high-speed communication data. The M2003 series also provides rich analog peripherals including 8 single-end analog input channels of 500 kSPS 12-bit ADC and 6 channels of 16-bit PWM. The peripherals integrated into the M2003 series offer enhanced functionality compared to the NuMicro 1T 8051 series products.

Pin Compatible with N76E003 Series, N76S003 Series, MS51 Series and MG51 Series

The M2003 series with multiple function pins is fully compatible and seamlessly aligned with the Nuvoton N76E003 series, N76S003 series, MS51 series, and MG51 series. This includes compatibility with specific part numbers such as N76E003AT20, N76E003AQ20, N76E003BQ20, N76S003AT20, N76S003AQ20, MS51FB9AE, MS51XB9AE, MS51XB9BE, MG51FB9AE, MG51FC9AE, MG51XB9AE, and MG51XC9AE. Supported small form factor packages including TSSOP 20-pin and QFN 20-pin with pin-compatible for different part numbers make the system design and parts change easily.

For the development system, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, and NuEclipse IDE with GNU GCC compilers are also supported.

USCI*: supports UART, SPI or I^2C

+1*: The additional 1 set is generated by USCI.

Product Line	UART	I^2C	SPI	USCI*	Timer	PWM	ADC
M2003	2+1*	1+1*	+1*	1	4	6	8

Table 2.1-1 NuMicro M2003 Series Key Features Support Table

2 FEATURES

2.1 NuMicro® M2003 Features

Core And System	
Arm® Cortex®-M23 without TrustZone®	• Arm® Cortex®-M23 processor, running up to 24 MHz when V_{DD} = 2.4V ~ 5.5V • Built-in PMSAv8 Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • 32-bit Single-cycle hardware multiplier and 32-bit 17-cycle hardware divider • 24-bit system tick timer • Supports Programmble and maskable interrupt • Supports Low Power Sleep mode by WFI and WFE instructions • Supports single cycle I/O access
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option (4.4V/3.7V2.7V/2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Power Manager	• Supports Power-down mode
Security	• 128-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Flash	• 32 KB application ROM (APROM) • 4 KB on-chip Flash for user-defined loader (LDROM) • All on-chip Flash support 512 B page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • 2-wired ICP Flash updating through SWD interface • 32-bit Flash programming function
SRAM	• 4 KB on-chip SRAM • Supports byte-, half-word- and word-access
Clocks	
Internal Clock Source	• 24 MHz High-speed Internal RC oscillator (HIRC) for system operation • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation
Timers	
32-bit Timer	• Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source

	• One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports continue capture fucntion in TIMER0/TIMER2 • Supports chip wake-up function, if a timer interrupt signal is generated
ECAP	• 3 input channels • 24-bit Input Capture up-counting timer/counter • With noise filter in front end of input ports • Edge detector with three options: – Rising edge detection – Falling edge detection – Both edge detection • Captured events reset and/or reload capture counter • Supports compare-match function
PWM	• Supports maximum clock frequency up to 24 MHz • One PWM module providing 6 output channels • Supports independent mode for PWM output/Capture input channel • Supports complementary mode for 3 complementary paired PWM output channel – Dead-time insertion with 12-bit resolution – Two compared values during one period • Supports 12-bit prescaler from 1 to 4096 • Supports 16-bit resolution PWM counter – Up, down or up/down counter operation type • Supports mask function and tri-state enable for each PWM pin • Supports brake function – Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup) – Noise filter for brake source from pin – Edge detect brake source to control brake state until brake interrupt cleared – Level detect brake source to auto recover function after brake condition removed • Supports interrupt on the following events: – PWM counter match 0, period value or compared value

	– Brake condition happened • Supports trigger ADC on the following events: – PWM counter match 0, period value or compared value • Capture Function Features – Up to 6 capture input channels with 16-bit resolution – Supports rising or falling capture condition – Supports input rising/falling capture interrupt – Supports rising/falling capture with counter reload option
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), and HCLK/2048 with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• 12-bit, 8-ch 500 KSPS SAR ADC with up to 8 single-end analog input channels • One internal channel for band-gap VBG input • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse and PWM. • Configurable ADC sampling time.
Communication Interfaces	
UART	• Auto-Baud Rate measurement and baud rate compensation function • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports RS-485 9-bit mode and direction control • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function

	• Supports Single-wire function mode. • Supports TX and RX swap function mode
I²C	• One set of I²C device with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), and Fast mode plus (1 Mbps) • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports multi-address power-down wake-up function • Support pin swap function • Support setup/hold time programmable • Support two level buffer mode
Universal Serial Control Interface (USCI)	• Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and programmable flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator. • Supports wake-up function **SPI** • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function: input slave select transition • Supports one data channel half-duplex transfer **I²C** • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data
GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control

- Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1.1 M2003 Series

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

TSSOP20	QFN20
M2003FC1AE	M2003XC1AE

3.2 M2003 Series Naming Rule

M2	003	F	C	1	A	E
Core	**Line**	**Package**	**Flash**	**SRAM**	**Reserve**	**Temperature**
Cortex-M23		F: TSSOP20 (4.4x6.5x0.9 mm) X: QFN20 (3x3x0.8 mm)	C: 32 KB	1: 4 KB		E:-40° C ~ 105° C

3.3 NuMicro M2003 Series Selection Guide

Part Number		M2003	
		FC1AE	XC1AE
System Frequency (MHz)		24	24
Flash (KB)		32	32
SRAM (KB)		4	4
LDROM (KB)		4	4
SPROM (KB)		1	1
PMDA		-	-
I/O		18	18
RTC		-	-
32-bit Timer		4	4
16-bit PWM		6	6
16-bit BPWM		-	-
Connectivity	UART	2+1*	2+1*
	SPI	+1*	+1*
	I^2C	1+1*	1+1*
	USCI*	1	1
12-bit ADC		8 ch	8 ch
Temperature Sensor		-	-
Analog Comparator		-	-
Internal Vref		-	-
Package		TSSOP20	QFN20

Note: USCI*: supports UART, SPI or I^2C

+1*: The additional 1 set is generated by USCI.

4 PIN CONFIGURATION

Users can find pin configuration information in the M2003 Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1 M2003 Pin Configuration

4.1.1 M2003 Series Pin Diagram

4.1.1.1 M2003 Series TSSOP20-Pin Diagram

Corresponding Part Number: M2003FC1AE

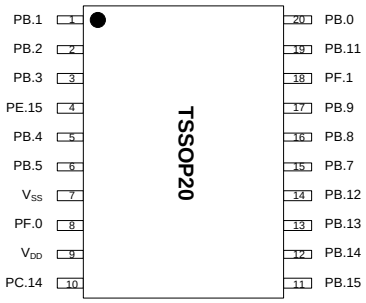


Figure 4.1-1 M2003 Series TSSOP20-pin Diagram

4.1.1.2 M2003 Series QFN20-Pin Diagram

Corresponding Part Number: M2003XC1AE

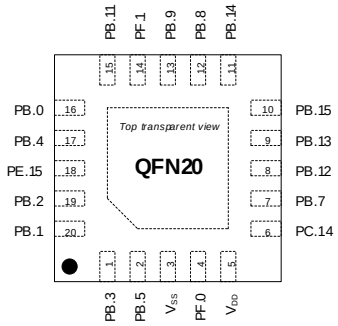


Figure 4.1-2 M2003 Series QFN20-pin Diagram

4.1.2 M2003 Series Multi-function Pin Diagram

4.1.2.1 M2003 Series TSSOP20-Pin Multi-function Pin Diagram

Corresponding Part Number: M2003FC1AE

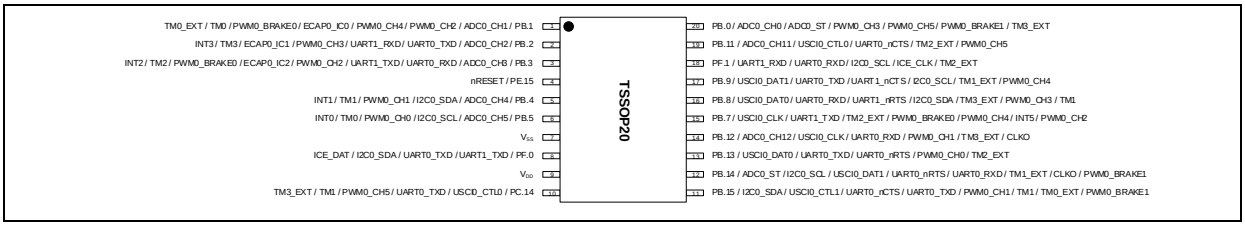


Figure 4.1-3 TSSOP20-Pin Diagram

Pin	Type	M2003FC1AE Pin Function
1	I/O	PB.1 / ADC0_CH1 / PWM0_CH2 / PWM0_CH4 / PWM0_BRAKE0 / TM0 / TM0_EXT/ECAP0_IC0
2	I/O	PB.2 / ADC0_CH2 / UART0_TXD / UART1_RXD / PWM0_CH3 / TM3 / INT3/ECAP0_IC1
3	I/O	PB.3 / ADC0_CH3 / UART0_RXD / UART1_TXD / PWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2/ECAP0_IC2
4	I	PE.15 / nRESET
5	I/O	PB.4 / ADC0_CH4 / I2C0_SDA / PWM0_CH1 / TM1 / INT1
6	I/O	PB.5 / ADC0_CH5 / I2C0_SCL / PWM0_CH0 / TM0 / INT0
7	P	V_{SS}
8	I/O	PF.0 / UART1_TXD / UART0_TXD / I2C0_SDA / ICE_DAT
9	P	V_{DD}
10	I/O	PC.14 / PWM0_CH5 / USCI0_CTL0 / TM1 / TM3_EXT
11	I/O	PB.15 / ADC0_CH15 / I2C0_SDA / USCI0_CTL1 / UART0_nCTS / PWM0_CH1 / TM0_EXT / PWM0_BRAKE1 / UART0_TXD
12	I/O	PB.14 / ADC0_ST / I2C0_SCL / USCI0_DAT1 / UART0_nRTS / TM1_EXT / CLKO / PWM0_BRAKE1/ UART0_RXD
13	I/O	PB.13 / USCI0_DAT0 / UART0_TXD / PWM0_CH0 / TM2_EXT/ UART0_nCTS
14	I/O	PB.12 / ADC0_CH12 / USCI0_CLK / UART0_RXD / PWM0_CH1 / TM3_EXT / CLKO
15	I/O	PB.7 / UART1_TXD / TM2_EXT / PWM0_BRAKE0 / PWM0_CH4 / INT5 / PWM0_CH2/USCI0_CLK
16	I/O	PB.8 / UART0_RXD / UART1_nRTS / TM3_EXT / PWM0_CH3 / TM1/USCI0_DAT0/I2C0_SDA
17	I/O	PB.9 / UART0_TXD / UART1_nCTS / TM1_EXT / PWM0_CH4/USCI0_DAT1/I2C0_SCL
18	I/O	PF.1 / UART1_RXD / UART0_RXD / I2C0_SCL / ICE_CLK
19	I/O	PB.11 / ADC0_CH11 / UART0_nCTS / TM2_EXT / PWM0_CH5/USCI0_CTL0
20	I/O	PB.0 / ADC0_CH0 / ADC0_ST / PWM0_CH3 / SPI1_I2SMCLK / PWM0_CH5 / PWM0_BRAKE1 / TM3_EXT

4.1.2.2 M2003 Series QFN20-Pin Multi-function Pin Diagram

Corresponding Part Number: M2003XC1AE

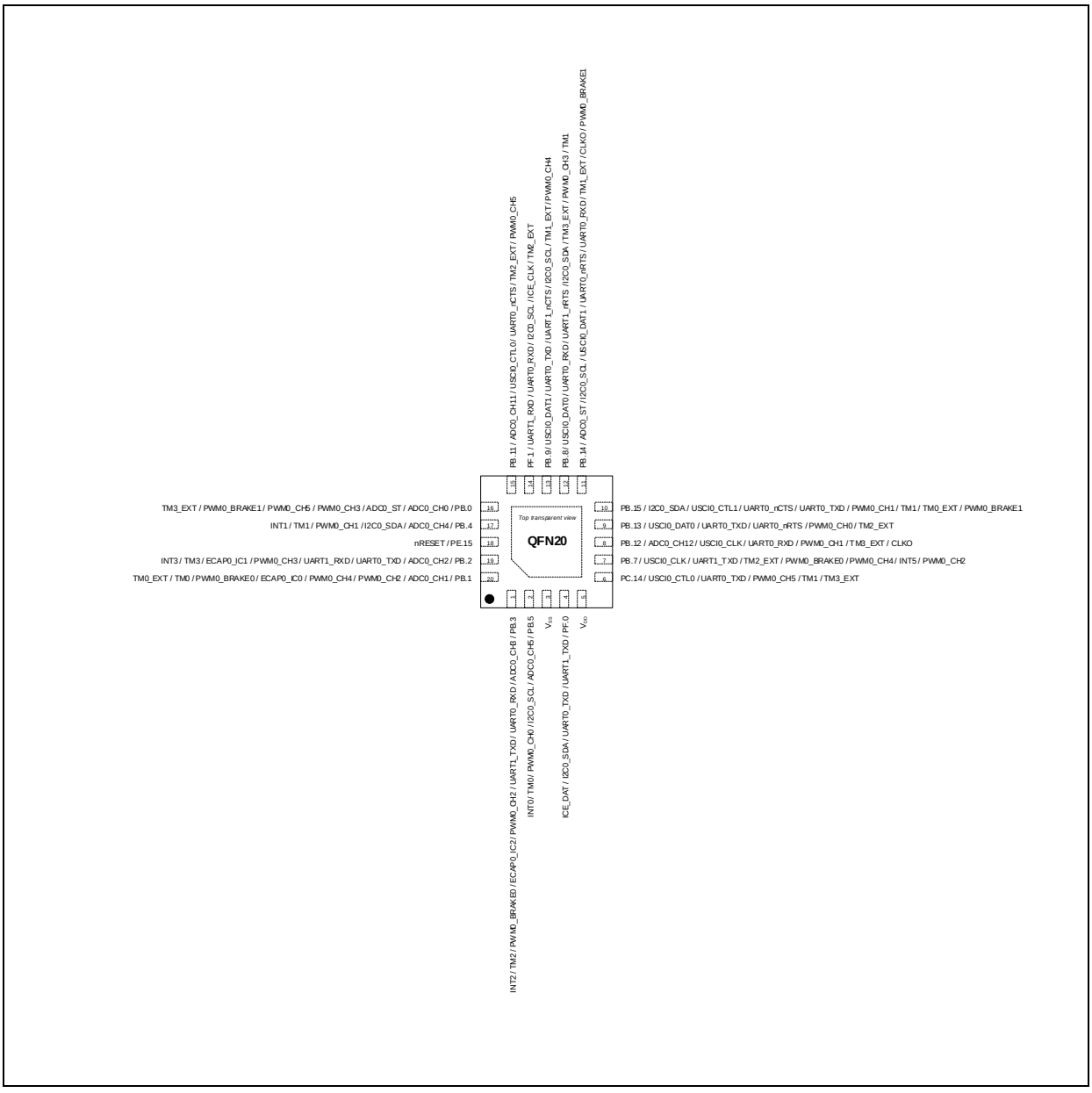


Figure 4.1-4 QFN20-Pin Multi-function Pin Diagram

Pin	Type	M2003FC1AE Pin Function
1	I/O	PB.3 / ADC0_CH3 / UART0_RXD / UART1_TXD / PWM0_CH2 / PWM0_BRAKE0 / TM2 / INT2/ECAP0_IC2
2	I/O	PB.5 / ADC0_CH5 / I2C0_SCL / PWM0_CH0 / TM0 / INT0
3	P	V_{SS}
4	I/O	PF.0 / UART1_TXD / UART0_TXD / I2C0_SDA / ICE_DAT
5	P	V_{DD}

Pin	Type	M2003FC1AE Pin Function
6	I/O	PC.14 / PWM0_CH5 / USCI0_CTL0 / TM1 / TM3_EXT
7	I/O	PB.7 / UART1_TXD / TM2_EXT / PWM0_BRAKE0 / PWM0_CH4 / INT5 / PWM0_CH2/USCI0_CLK
8	I/O	PB.12 / ADC0_CH12 / USCI0_CLK / UART0_RXD / PWM0_CH1 / TM3_EXT / CLKO
9	I/O	PB.13 / USCI0_DAT0 / UART0_TXD / PWM0_CH0 / TM2_EXT/ UART0_nCTS
10	I/O	PB.15 / ADC0_CH15 / I2C0_SDA / USCI0_CTL1 / UART0_nCTS / PWM0_CH1 / TM0_EXT / PWM0_BRAKE1 / UART0_TXD
11	I/O	PB.14 / ADC0_ST / I2C0_SCL / USCI0_DAT1 / UART0_nRTS / TM1_EXT / CLKO / PWM0_BRAKE1/ UART0_RXD
12	I/O	PB.8 / UART0_RXD / UART1_nRTS / TM3_EXT / PWM0_CH3 / TM1/USCI0_DAT0/I2C0_SDA
13	I/O	PB.9 / UART0_TXD / UART1_nCTS / TM1_EXT / PWM0_CH4/USCI0_DAT1/I2C0_SCL
14	I/O	PF.1 / UART1_RXD / UART0_RXD / I2C0_SCL / ICE_CLK
15	I/O	PB.11 / ADC0_CH11 / UART0_nCTS / TM2_EXT / PWM0_CH5/USCI0_CTL0
16	I/O	PB.0 / ADC0_CH0 / ADC0_ST / PWM0_CH3 / SPI1_I2SMCLK / PWM0_CH5 / PWM0_BRAKE1 / TM3_EXT
17	I/O	PB.4 / ADC0_CH4 / I2C0_SDA / PWM0_CH1 / TM1 / INT1
18	I	PE.15 / nRESET
19	I/O	PB.2 / ADC0_CH2 / UART0_TXD / UART1_RXD / PWM0_CH3 / TM3 / INT3/ECAP0_IC1
20	I/O	PB.1 / ADC0_CH1 / PWM0_CH2 / PWM0_CH4 / PWM0_BRAKE0 / TM0 / TM0_EXT/ECAP0_IC0

Table 4.1-1 M2003XC1AE Pin Multi-function Pin Table

4.2 M2003 Series Pin Mapping

Different part number with same package might has different function. Please refer to the M2003 Series Selection Guide, Pin Configuration section or NuTool - PinConfig.

Corresponding Part Number: M2003FC1AE, M2003XC1AE.

	M2003 Series	
Pin Name	**TSSOP 20**	**QFN 20**
PB.1	1	20
PB.2	2	19
PB.3	3	1
PE.15	4	18
PB.4	5	17
PB.5	6	2
VSS	7	3
PF.0	8	4
VDD	9	5
PC.14	10	6
PB.15	11	10
PB.14	12	11
PB.13	13	9
PB.12	14	8
PB.7	15	7
PB.8	16	12
PB.9	17	13
PF.1	18	14
PB.11	19	15
PB.0	20	16

4.3 Pin Functional Description

Group	Pin Name	Type	Description
ADC0	ADC0_CH0	A	ADC0 channel 0 analog input.
	ADC0_CH1	A	ADC0 channel 1 analog input.
	ADC0_CH2	A	ADC0 channel 2 analog input.
	ADC0_CH3	A	ADC0 channel 3 analog input.
	ADC0_CH4	A	ADC0 channel 4 analog input.
	ADC0_CH5	A	ADC0 channel 5 analog input.
	ADC0_CH11	A	ADC0 channel 11 analog input.
	ADC0_CH12	A	ADC0 channel 12 analog input.
	ADC0_ST	I	ADC0 external trigger input pin.
CLKO	CLKO	O	Clock Out
ECAP0	ECAP0_IC0	I	ECAP0 capture input 0 pin
	ECAP0_IC1	I	ECAP0 capture input 1 pin
	ECAP0_IC2	I	ECAP0 capture input 2 pin
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin. Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
PWM0	PWM0_BRAKE0	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE1	I	PWM0 Brake 1 input pin.
	PWM0_CH0	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	I/O	PWM0 channel 5 output/capture input.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.

Group	Pin Name	Type	Description
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
Power			
	V_{DD}	P	Power supply for I/O ports and LDO source for digital circuit.
	V_{SS}	P	Ground pin for digital circuit.

5 BLOCK DIAGRAM

5.1 M2003 Series Block Diagram

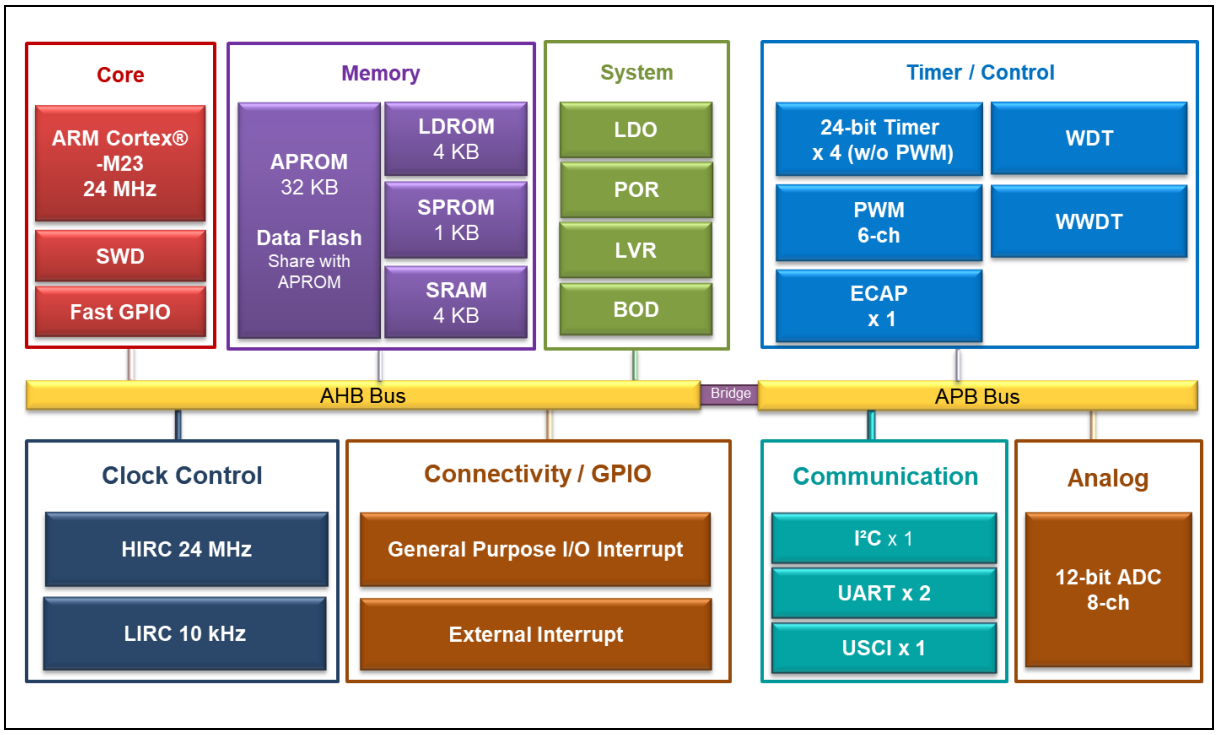


Figure 5.1-1 M2003 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M23 Core

The NuMicro® M2003 series is embedded with the Cortex®-M23 processor. The Cortex®-M23 processor is a low gate count, two-stage, and highly energy efficient 32-bit RISC processor, a debug access port supporting serial wire debug and single-cycle I/O ports. It has an NVIC component and MPU for memory-protection functionality. The processor also supports Security Extension. Figure 6.1-1 shows the functional controller of the processor.

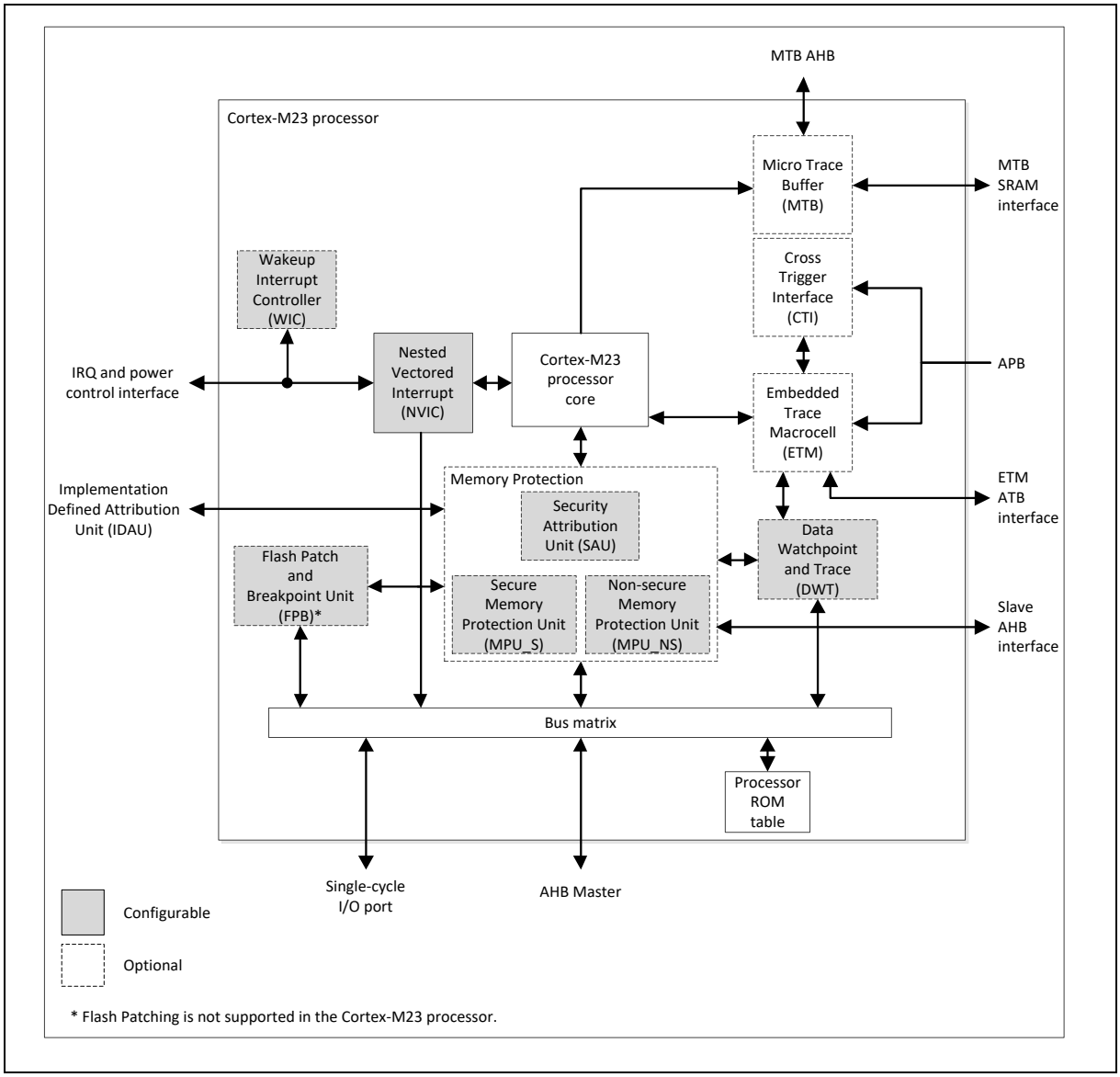


Figure 6.1-1 Cortex®-M23 Block Diagram

Cortex®-M23 processor features:

- Arm®v8-M Baseline architecture.
- Arm®v8-M Baseline Thumb®-2 instruction set that combines high code density with 32-bit performance.
- Support for single-cycle I/O access.
- Power control optimization of system components.
- Integrated sleep modes for low power consumption.
- Optimized code fetching for reduced Flash and ROM power consumption.
- A 32-bit Single cycle Hardware multiplier.
- A 32-bit Hardware divider.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Deterministic instruction cycle timing.
- Support for system level debug authentication.
- Support for Arm® Debug Interface Architecture ADIv5.1 Serial Wire Debug (SWD).
- ETM for instruction trace.
- Separated privileged and unprivileged modes.
- Security Extension supporting a Secure and a Non-secure state.
- Protected Memory System Architecture (PMSAv8) Memory Protection Units (MPUs) for both Secure and Non-secure states.
- Security Attribution Unit (SAU).
- SysTick timers for both Secure and Non-secure states.
- A Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor with up to 240 interrupts.

IRQ32 ~ IRQ63 Clear-enable Control Register (NVIC_ICER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER1	NVIC_BA+0x084	R/W	IRQ32 ~ IRQ63 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER1 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ00 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ00 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ63 Set-pending Control Register (NVIC_ISPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ32 ~ IRQ63 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ00 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ00 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ63 Clear-pending Control Register (NVIC_ICPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ32 ~ IRQ63 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ00 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ00 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ32 ~ IRQ63 Active Bit Register (NVIC_IABR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ32 ~ IRQ63 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ00 ~ IRQ31 Interrupt Target Non-secure Register (NVIC_ITNS0)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS0	NVIC_BA+0x280	R/W	IRQ00 ~ IRQ31 Interrupt Target Non-secure Register	0x0000_0000

31	30	29	28	27	26	25	24
ITNS							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITNS							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITNS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITNS							

Bits	Description	
[31:0]	**ITNS**	**Interrupt Target Non-secure Register** The NVIC_ITNS0-NVIC_INTS1 registers, determines whether each interrupt targets Non-secure or Secure state. 0 = Interrupt targets Secure state. 1 = Interrupt targets Non-secure state. This register is RAZ/WI when accessed as Non-secure.

IRQ32 ~ IRQ63 Interrupt Target Non-secure Register (NVIC_ITNS1)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS1	NVIC_BA+0x284	R/W	IRQ32 ~ IRQ63 Interrupt Target Non-secure Register	0x0000_0000

31	30	29	28	27	26	25	24
ITNS							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITNS							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITNS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITNS							

Bits	Description	
[31:0]	**ITNS**	**Interrupt Target Non-secure Register** The NVIC_ITNS0-NVIC_INTS1 registers, determines whether each interrupt targets Non-secure or Secure state. 0 = Interrupt targets Secure state. 1 = Interrupt targets Non-secure state. **Note:** This register is RAZ/WI when accessed as Non-secure.

IRQ0 ~ IRQ61 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..15**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ63 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		Reserved					
23	22	21	20	19	18	17	16
PRI_4n_2		Reserved					
15	14	13	12	11	10	9	8
PRI_4n_1		Reserved					
7	6	5	4	3	2	1	0
PRI_4n_0		Reserved					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** “0” denotes the highest priority and “3” denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** “0” denotes the highest priority and “3” denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** “0” denotes the highest priority and “3” denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** “0” denotes the highest priority and “3” denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

Priority Value PRI_4n_X[7:6] X=0,1,2,3	Secure Priority	Non-Secure Priority When PRIS=0	Non-Secure Priority When PRIS=1
0x0	0	0	128
0x1	64	64	160
0x2	128	128	192
0x3	192	192	224

Table 6.1-1 Priority Grouping

6.1.1.2 AHB Bus Matrix Priority Control Register

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
AHB Base Address: **AHB_BA = 0x4000_0400**				
AHBMCTL	0x40000400	R/W	AHB Bus Matrix Priority Control Register	0x0000_0001

AHB Bus Matrix Priority Control Register (AHBMCTL)

Register	Offset	R/W	Description	Reset Value
AHBMCTL	0x40000400	R/W	AHB Bus Matrix Priority Control Register	0x0000_0001

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							**INTACTEN**

Bits	Description	
[31:1]	**Reserved**	Reserved.
[0]	**INTACTEN**	**Highest AHB Bus Priority of Cortex®M23 Core Enable Bit (Write Protect)** Enable Cortex®-M23 core with highest AHB bus priority in AHB bus matrix. 0 = Round robin mode. 1 = Cortex®-M23 CPU with highest bus priority when interrupt occur. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset source are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset (POR)
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - System Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M23 core only by writing 1 to CPURST (SYS_IPRST0[1])

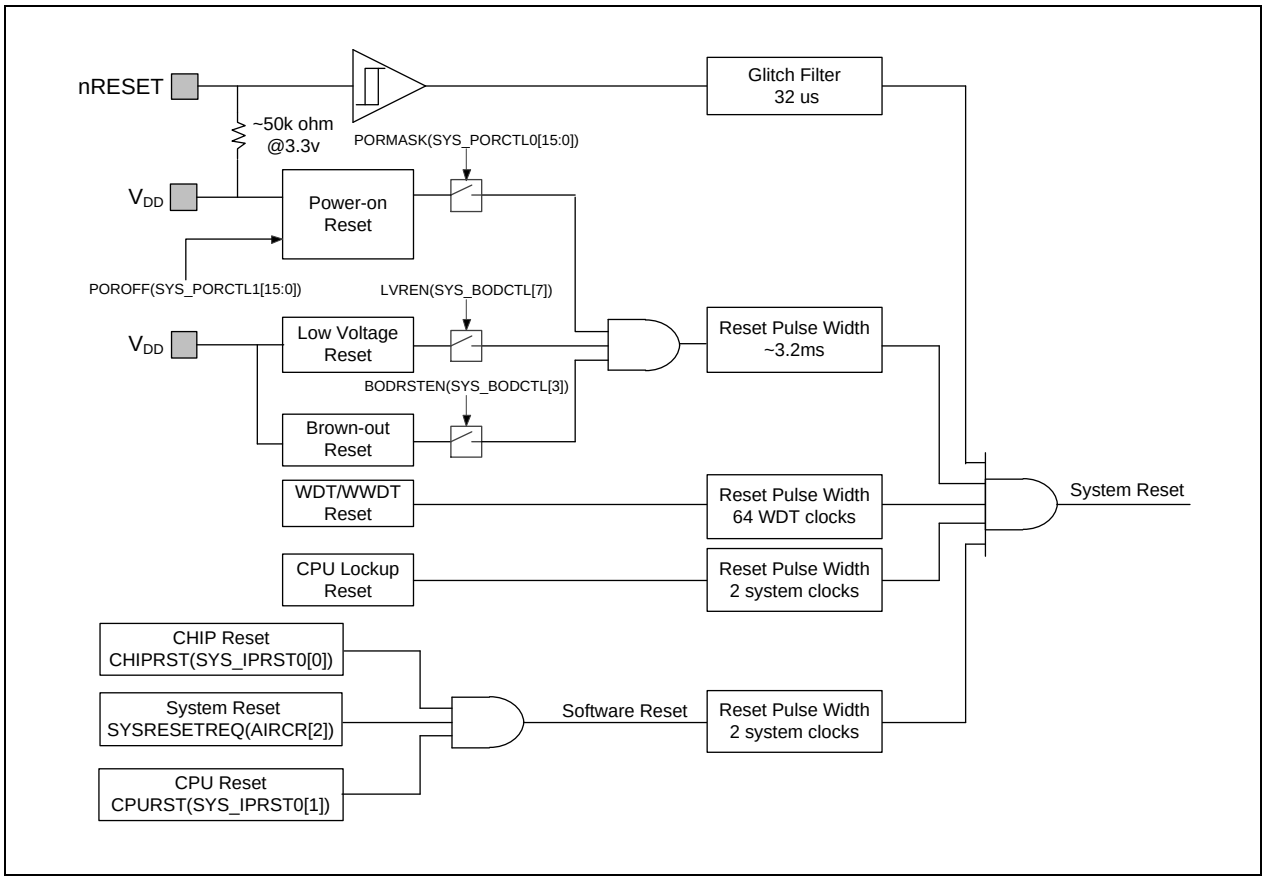


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M23 only; the other reset sources will reset Cortex®-M23 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x5 HIRC	0x5 HIRC	0x5 HIRC	0x5 HIRC	0x5 HIRC	0x5 HIRC	0x5 HIRC	0x5 HIRC	-
HCLKDIV (CLK_CLKDIV0[3:0])	0x0	0x0	0x0	0x0	0x0	0x3	0x0	0x3	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[18:16])									
BODRSTEN									

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	SYSTEM	CPU
(SYS_BODCTL[3])									
SYS_SRAMPC0	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PDMSEL (CLK_PMUCTL [2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1]) WDTEN (WDT_CTL[7])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
CBS (FMC_ISPSTS[2])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

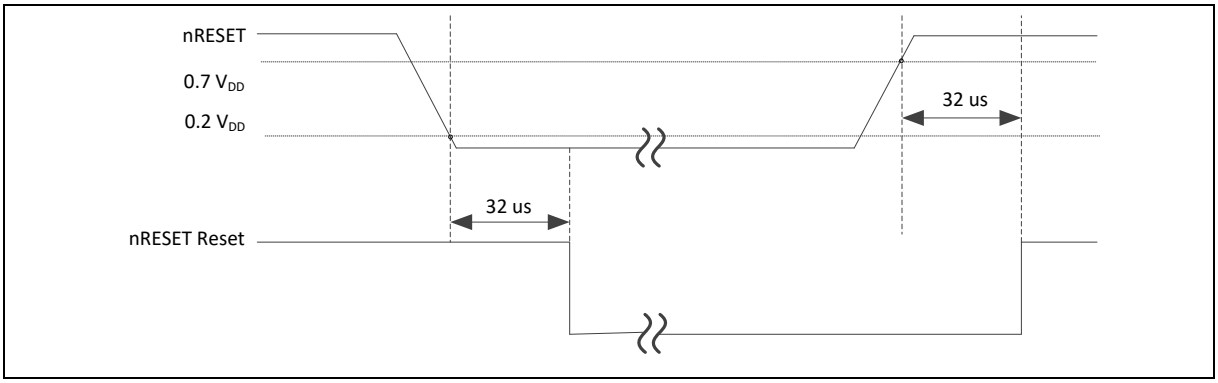


Figure 6.2-2 nRESET Reset Waveform

The special mode can enable nRESET pin function when system select other function for GPE.15, user can input special control signal for PE.15 make system force enable nRESET pin.

Figure 6.2-3 shows the method of entry special mode.

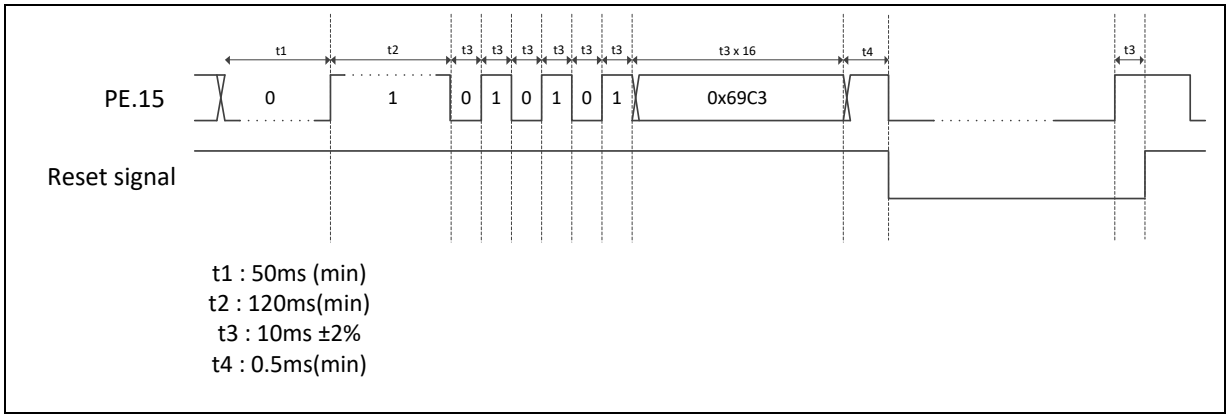


Figure 6.2-3 nRESET Reset Mode Enable Control Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage of LDO and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-4 shows the power-on reset waveform.

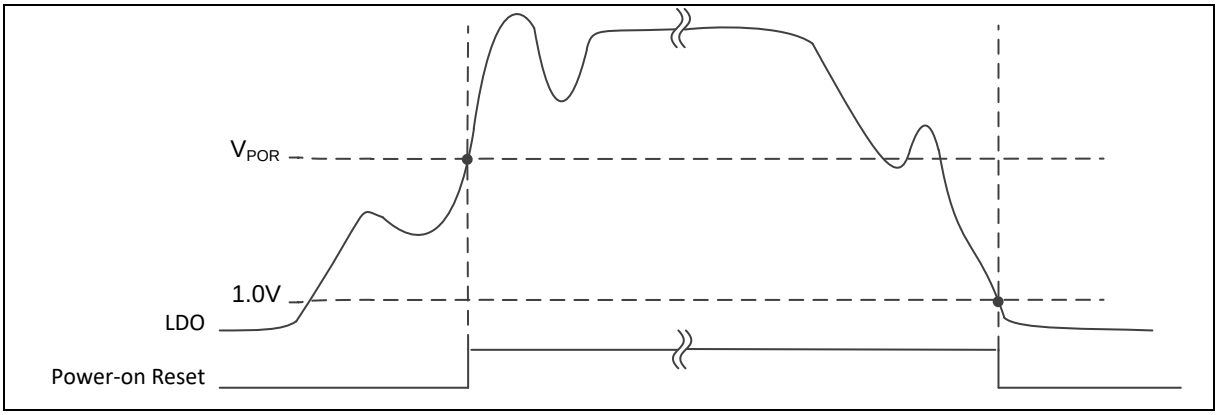


Figure 6.2-4 Power-on Reset (POR) Waveform

6.2.2.3 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the V_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-5 shows the Low Voltage Reset waveform.

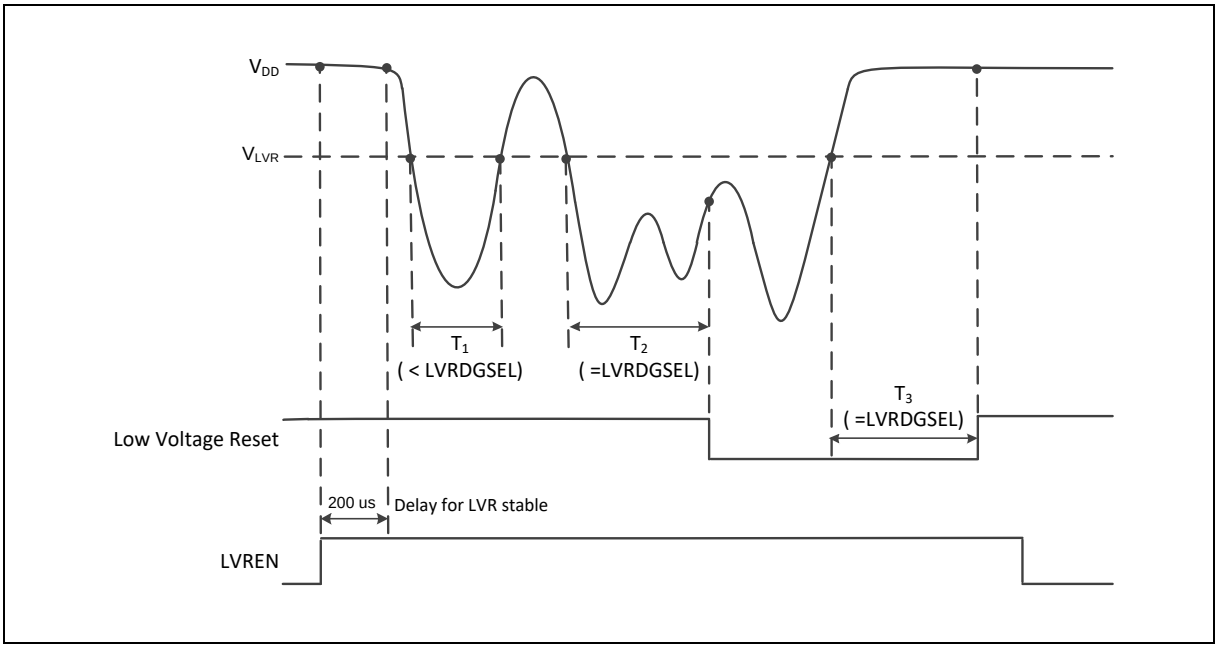


Figure 6.2-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 *Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), the BOD function will be active. Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} that is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the V_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user

configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-6 shows the Brown-out Detector waveform.

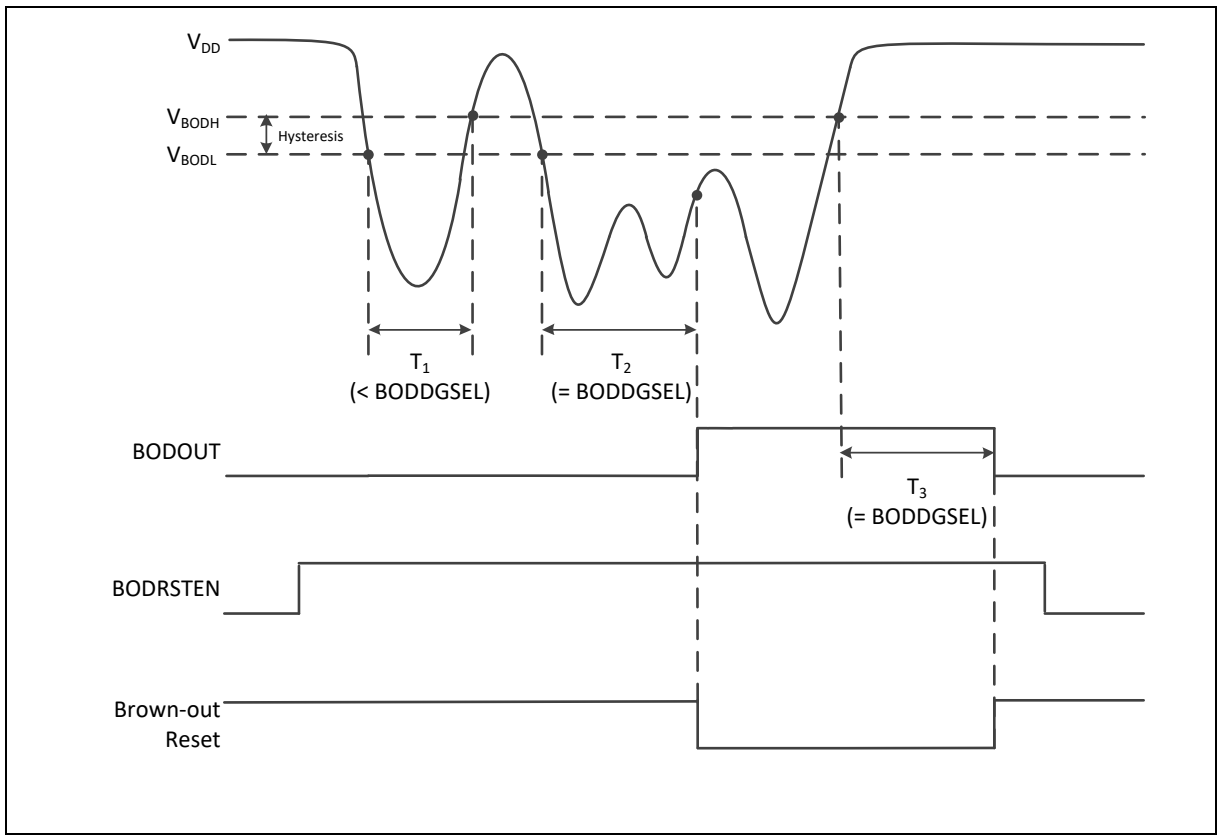


Figure 6.2-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hard fault at hard fault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and System Reset

The CPU Reset means only Cortex®-M23 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and

BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The System Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the System Reset.

6.2.3 Power Modes and Wake-up Sources

The power manager unit support several operating modes for saving power. Table 6.2-2 lists all power modes.

Mode	CPU Operating Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode	24 MHz	1.5	All clocks are disabled by control register. CLK_AHBCLK, CLK_APBCLK0 and CLK_APBCLK1.
Idle mode	CPU enter Sleep mode	keep	Only CPU clock is disabled.
Power-down mode (PD)	CPU enters Deep Sleep mode	keep	Most clocks are disabled except LIRC and only WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC.

Table 6.2-2 Power Mode Table

Each power mode has different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Power-down mode	1	1	0	YES

Table 6.2-3 Power Mode Entry Setting Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LIRC.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	EINT, GPIO, UART, BOD, WDT, Timer, I²C and USCI.
Available Clocks	All	All except CPU clock	LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

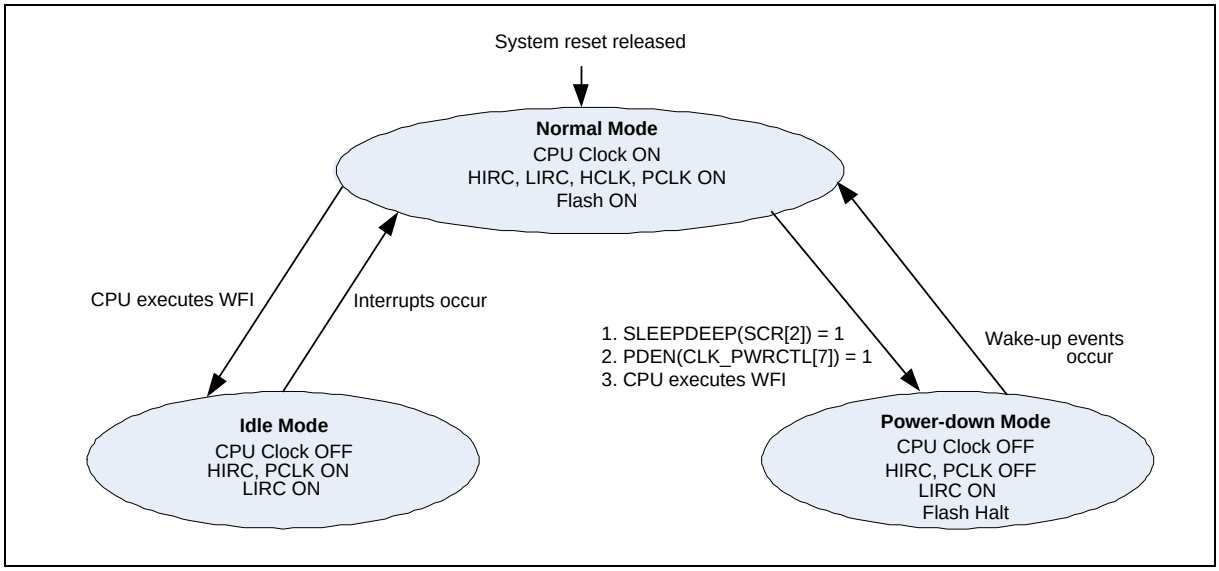


Figure 6.2-7 Power Mode State Machine

	Normal Mode	Idle Mode	Power-Down Mode (PD)
HIRC	ON	ON	Halt
LIRC	ON	ON	ON/OFF[1]
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
FLASH	ON	ON	Halt
TIMER	ON	ON	ON/OFF[2]
WDT	ON	ON	ON/OFF[3]
Others	ON	ON	Halt

Note:

1. LIRC ON or OFF depends on software setting in normal mode.
2. If TIMER clock source is selected as LIRC and LIRC is on.
3. If WDT clock source is selected as LIRC and LIRC is on.

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

EINT, GPIO, UART, BOD, WDT, Timer, I²C and USCI.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up	Wake-Up Condition	Power-down mode	System Can Enter Power-Down Mode Again Condition*

Source		PD	
BOD	Brown-out Detector Reset / Interrupt	V	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-out Detector Reset	-	After software writes 1 to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	After software writes 1 to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
EINT	External Interrupt	V	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	V	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	After software writes 1 to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
UART	nCTS wake-up	V	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to

			clear WKIF(I2C_WKSTS[0]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.4 System Memory Map

This chip provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. Only little-endian data format is supported.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_7FFF	FLASH_BA	FLASH Memory Space (32 KB)
0x2000_0000 – 0x2000_0FFF	SRAM0_BA	SRAM Memory Space (4 KB)
Secure Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
Secure APB Controllers Space (0x4004_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.5 SRAM Memory Organization

This chip supports embedded SRAM with a total of 4 Kbytes size.

- Supports total 4 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

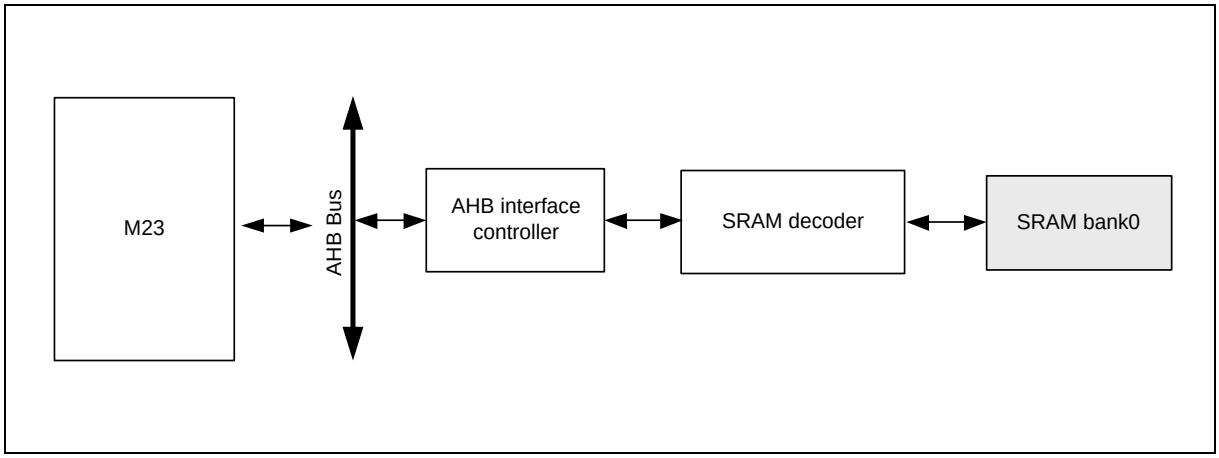


Figure 6.2-8 SRAM Block Diagram

Figure 6.2-9 shows the SRAM organization. The bank0 is addressed to 4 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2000_0FFF. The address between 0x2000_1000 to 0x2FFF_FFFF is illegal memory space and chip will enter hard fault if CPU accesses these illegal memory addresses.

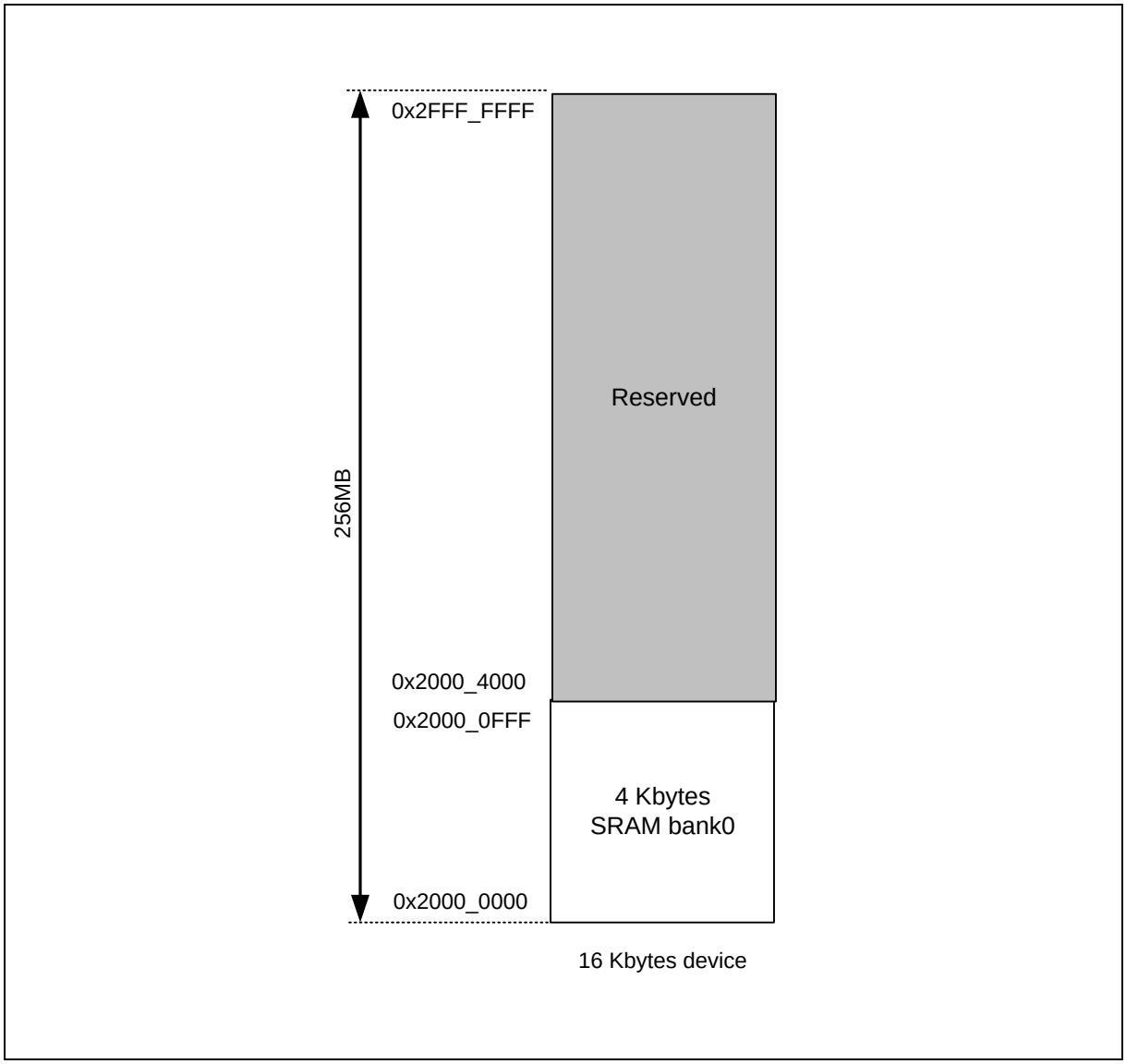


Figure 6.2-9 SRAM Memory Organization

6.2.6 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These write-protected system control registers, as listed in Table 6.2-8 , have write-protection after the power-on reset till user disables register protection.

Before writing to these protected registers, user has to unlock the write-protected mechanism by writing a register protection disable sequence to the REGLCTL register. The register protection disable sequence is writing the data “59h”, “16h” “88h” sequentially. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

Once a register protection disable sequence is writing to the REGLCTL register successfully, These write-protected registers will be unlocked and able to accept write access. It’s recommended to locked these registers by writing any value to REGLCTL register.

SYS_IPRST0	Address 0x4000_0008
SYS_BODCTL	address 0x4000_0018
SYS_PORCTL0	address 0x4000_0024
SYS_PORCTL1	address 0x4000_01EC
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_APBCLK1	address 0x4000_020C
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_CLKSEL2	address 0x4000_0218
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004
TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
PWM_CTL0	address 0x4005_8000
PWM_CTL1	address 0x4005_8000
PWM_DTCTL0_1	address 0x4005_8070
PWM_DTCTL2_3	address 0x4005_8074

PWM_DTCTL4_5	address 0x4005_8078
PWM_BRKCTL0_1	address 0x4005_80C8
PWM_BRKCTL2_3	address 0x4005_80CC
PWM_BRKCTL4_5	address 0x4005_80D0
PWM_SWBRK	address 0x4005_80DC
PWM_INTEN1	address 0x4005_80E4
PWM_INTSTS1	address 0x4005_80EC

Table 6.2-8 Protected Register List

6.2.7 System Timer (SysTick)

The Cortex®-M23 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit is cleared on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm®Cortex®-M23 Technical Reference Manual*" and "*Arm®v8-M Architecture Reference Manual*".

6.2.8 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-3 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and sub priority fields.
- Interrupt tail-chaining.
- An external Non maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.8.1 Exception Model and System Interrupt Map

Table 6.2-9 lists the exception model. Software can set 4 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x0” and the lowest priority is denoted as “0xC0” (The 6-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-4
NMI	2	0x00000008	-2
Non-secure Hard Fault (when AIRCR.BFHFNMINS is 0)	3	0x0000000C	-1
Reserved	4 ~ 10		Reserved
SVCall	11	0x0000002C	Configurable
Reserved	12 ~ 13		Reserved
PendSV	14	0x00000038	Configurable

SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ)	16 ~ 77	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-9 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-out low voltage detected interrupt
17	1		
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	Reserved	Reserved
20	4		
21	5	ISP_INT	FMC ISP interrupt
22	6		
23	7	Reserved	Reserved
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from PB.5 pins
27	11	EINT1	External interrupt from PB.4 pins
28	12	EINT2	External interrupt from PB.3 pins
29	13	EINT3	External interrupt from PB.2 pins
30	14		
31	15	EINT5	External interrupt from PB.7 pins
32	16		
33	17	GPB_INT	External interrupt from PB[15:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19		
36	20	GPE_INT	External interrupt from PE[15:0] pin
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	Reserved	Reserved
39	23		
40	24	Reserved	Reserved
41	25	PWM0_INT	PWM0 interrupt

42	26	Reserved	Reserved
43	27	Reserved	Reserved
44	28		
45	29	Reserved	Reserved
46	30	Reserved	Reserved
47	31	Reserved	Reserved
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39		
56	40		
57	41	Reserved	Reserved
58	42	ADC_INT	ADC interrupt source
59	43	Reserved	Reserved
60	44		
61	45	Reserved	Reserved
62	46	Reserved	Reserved
63	47	Reserved	Reserved
64	48	Reserved	Reserved
65	49	Reserved	Reserved
66	50	Reserved	Reserved
67	51		
68	52	USCI0_INT	USCI0 interrupt
69	53		
70	54	Reserved	Reserved
71	55	Reserved	Reserved
72	56		
73	57	Reserved	Reserved
74	58	Reserved	Reserved
75	59	Reserved	Reserved
76	60	ECAP0_INT	ECAP0 interrupt

77	61		
78	62	Reserved	Reserved
79	63	Reserved	Reserved

Table 6.2-10 Interrupt Number Table

6.2.8.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in the next section.

6.2.8.3 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ00 ~ IRQ31 Set-enable Control Register	0x0000_0000
NVIC_ISER1	NVIC_BA+0x004	R/W	IRQ32 ~ IRQ63 Set-enable Control Register	0x0000_0000
NVIC_ISER2	NVIC_BA+0x008	R/W	IRQ64 ~ IRQ95 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ00 ~ IRQ31 Clear-enable Control Register	0x0000_0000
NVIC_ICER1	NVIC_BA+0x084	R/W	IRQ32 ~ IRQ63 Clear-enable Control Register	0x0000_0000
NVIC_ICER2	NVIC_BA+0x088	R/W	IRQ64 ~ IRQ95 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ00 ~ IRQ31 Set-pending Control Register	0x0000_0000
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ32 ~ IRQ63 Set-pending Control Register	0x0000_0000
NVIC_ISPR2	NVIC_BA+0x108	R/W	IRQ64 ~ IRQ95 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ00 ~ IRQ31 Clear-pending Control Register	0x0000_0000
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ32 ~ IRQ63 Clear-pending Control Register	0x0000_0000
NVIC_ICPR2	NVIC_BA+0x188	R/W	IRQ64 ~ IRQ95 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ00 ~ IRQ31 Active Bit Register	0x0000_0000
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ32 ~ IRQ63 Active Bit Register	0x0000_0000
NVIC_IABR2	NVIC_BA+0x208	R/W	IRQ64 ~ IRQ95 Active Bit Register	0x0000_0000
NVIC_ITNS0	NVIC_BA+0x280	R/W	IRQ00 ~ IRQ31 Interrupt Target Non-secure Register	0x0000_0000
NVIC_ITNS1	NVIC_BA+0x284	R/W	IRQ32 ~ IRQ63 Interrupt Target Non-secure Register	0x0000_0000
NVIC_IPRn **n=0,1..15**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ63 Priority Control Register	0x0000_0000

IRQ00 ~ IRQ31 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ00 ~ IRQ31 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER1 registers enable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ32 ~ IRQ63 Set-enable Control Register (NVIC_ISER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER1	NVIC_BA+0x004	R/W	IRQ32 ~ IRQ63 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER1 registers enable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ00 ~ IRQ31 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ00 ~ IRQ31 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER1 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ32 ~ IRQ63 Clear-enable Control Register (NVIC_ICER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER1	NVIC_BA+0x084	R/W	IRQ32 ~ IRQ63 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER1 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ00 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ00 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ63 Set-pending Control Register (NVIC_ISPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ32 ~ IRQ63 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR1 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ00 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ00 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ32 ~ IRQ63 Clear-pending Control Register (NVIC_ICPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ32 ~ IRQ63 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR1 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ00 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ00 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ32 ~ IRQ63 Active Bit Register (NVIC_IABR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ32 ~ IRQ63 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR1 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ00 ~ IRQ31 Interrupt Target Non-secure Register (NVIC_ITNS0)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS0	NVIC_BA+0x280	R/W	IRQ00 ~ IRQ31 Interrupt Target Non-secure Register	0x0000_0000

31	30	29	28	27	26	25	24
ITNS							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITNS							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITNS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITNS							

Bits	Description	
[31:0]	**ITNS**	**Interrupt Target Non-secure Register** The NVIC_ITNS0-NVIC_INTS1 registers, determines whether each interrupt targets Non-secure or Secure state. 0 = Interrupt targets Secure state. 1 = Interrupt targets Non-secure state. This register is RAZ/WI when accessed as Non-secure.

IRQ32 ~ IRQ63 Interrupt Target Non-secure Register (NVIC_ITNS1)

Register	Offset	R/W	Description	Reset Value
NVIC_ITNS1	NVIC_BA+0x284	R/W	IRQ32 ~ IRQ63 Interrupt Target Non-secure Register	0x0000_0000

31	30	29	28	27	26	25	24
ITNS							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ITNS							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ITNS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ITNS							

Bits	Description	
[31:0]	**ITNS**	**Interrupt Target Non-secure Register** The NVIC_ITNS0-NVIC_INTS1 registers, determines whether each interrupt targets Non-secure or Secure state. 0 = Interrupt targets Secure state. 1 = Interrupt targets Non-secure state. **Note:** This register is RAZ/WI when accessed as Non-secure.

IRQ0 ~ IRQ61 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..15**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ63 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_4n_2		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_4n_1		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4n_0		**Reserved**					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** “0” denotes the highest priority and “3” denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** “0” denotes the highest priority and “3” denotes the lowest priority.
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** “0” denotes the highest priority and “3” denotes the lowest priority.
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** “0” denotes the highest priority and “3” denotes the lowest priority.
[5:0]	**Reserved**	Reserved.

Priority Value PRI_4n_X[7:6] X=0,1,2,3	Secure Priority	Non-Secure Priority When PRIS=0	Non-Secure Priority When PRIS=1
0x0	0	0	128
0x1	64	64	160
0x2	128	128	192
0x3	192	192	224

Table 6.2-11 Priority Grouping

6.2.8.4 AHB Bus Matrix Priority Control Register

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
AHB Base Address: **AHB_BA = 0x4000_0400**				
AHBMCTL	0x40000400	R/W	AHB Bus Matrix Priority Control Register	0x0000_0001

AHB Bus Matrix Priority Control Register (AHBMCTL)

Register	Offset	R/W	Description	Reset Value
AHBMCTL	0x40000400	R/W	AHB Bus Matrix Priority Control Register	0x0000_0001

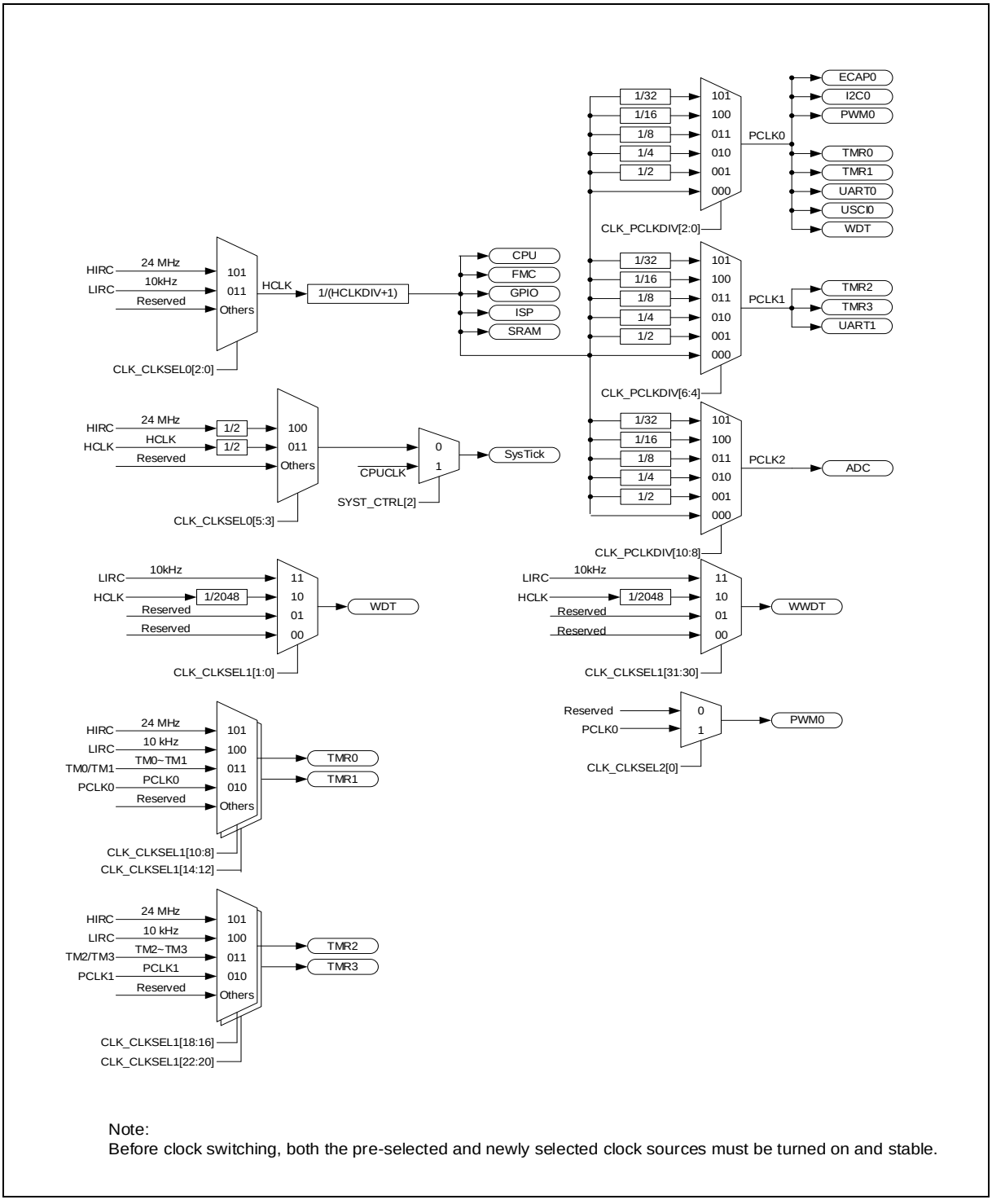
31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							**INTACTEN**

Bits	Description	
[31:1]	**Reserved**	Reserved.
[0]	**INTACTEN**	**Highest AHB Bus Priority of Cortex®M23 Core Enable Bit (Write Protect)** Enable Cortex®-M23 core with highest AHB bus priority in AHB bus matrix. 0 = Round robin mode. 1 = Cortex®-M23 CPU with highest bus priority when interrupt occur. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

6.3 Clock Controller

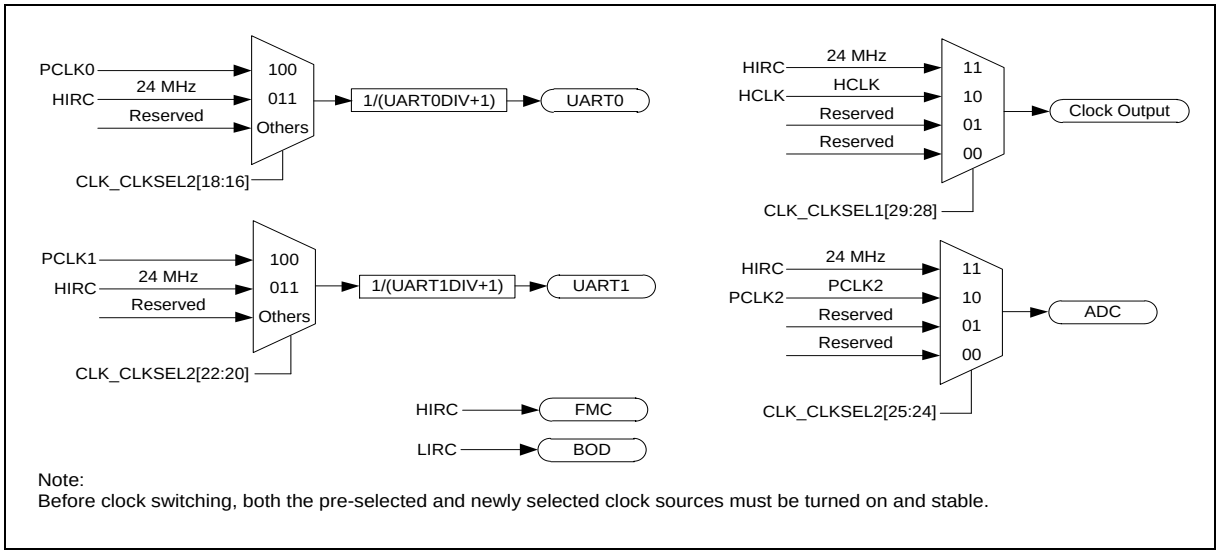
6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN (CLK_PWRCTL[7]) and core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 to Figure 6.3-2 show the clock generator and the overview of the clock source control.



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-1 Clock Generator Global View Diagram (1/3)



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-2 Clock Generator Global View Diagram (2/3)

6.3.2 Clock Generator

The clock generator consists of 2 clock sources, which are listed below:

- 24 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)

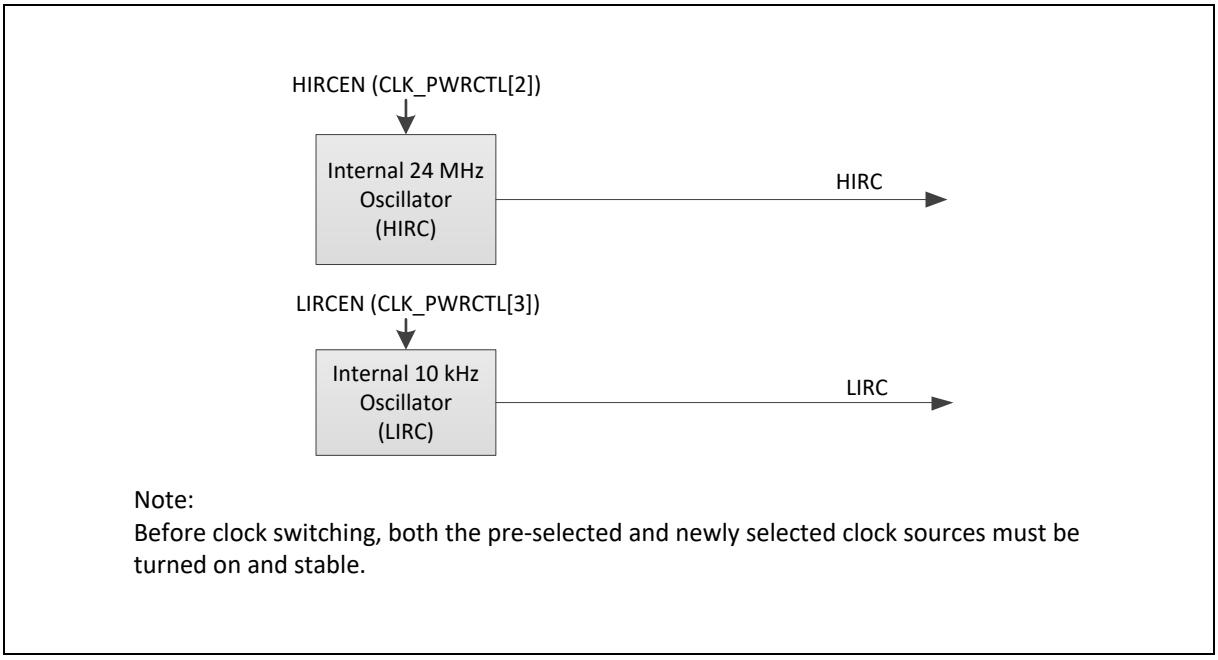


Figure 6.3-3 Clock Generator Block Diagram

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter starts counting and correlated clock stable index is set to 1 after stable counter value reaches a define value.

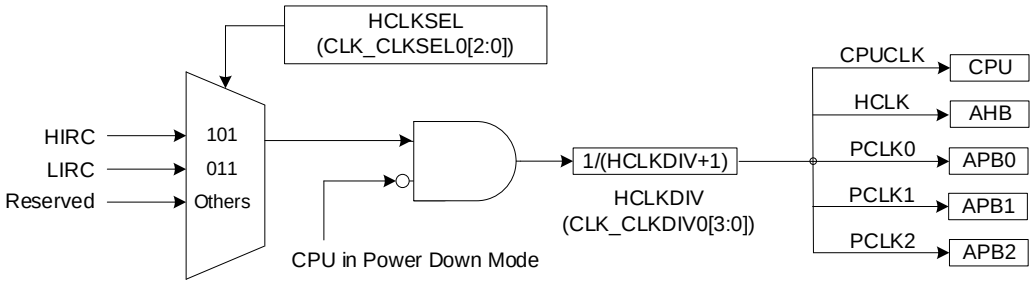
System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-1 will be auto cleared when user disables the clock source.

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
LIRC	LIRCEN (CLK_PWRCTL[3])	LIRCSTB (CLK_STATUS[3])
HIRC	HIRCEN (CLK_PWRCTL[2])	HIRCSTB (CLK_STATUS[4])

Table 6.3-1 Each Clock Source Enable Bit and Corresponding Stable Flag Table

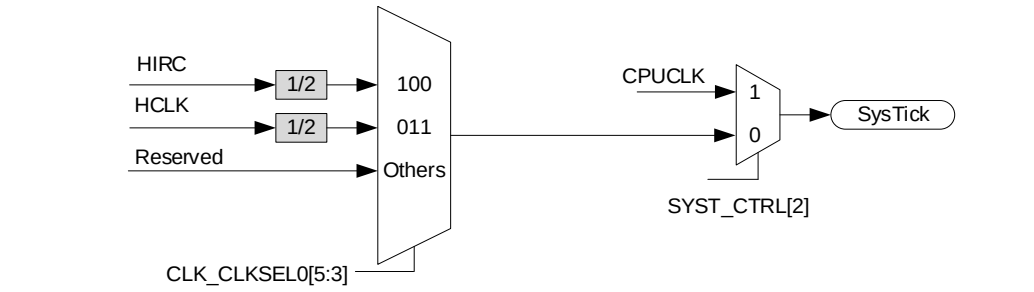
6.3.3 System Clock and SysTick Clock

The system clock has 2 clock sources, which are generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-4.



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-4 System Clock Block Diagram



Note:
Before clock switching, both the pre-selected and newly selected clock sources must be turned on and stable.

Figure 6.3-5 SysTick Clock Control Block Diagram

The clock source of SysTick in processor can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 2 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL1 and CLK_CLKSEL2 register.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
- Peripherals Clock

- when the modules adopt LIRC as clock source

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed by 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]). When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

If DIV1EN(CLK_CLKOCTL[5]) is set to 1, the clock output clock (CLKO_CLK) will bypass power-of-2 frequency divider. The output divider clock will be output to CLKO pin directly.

When entering Power-down mode, clock output does not output clock.

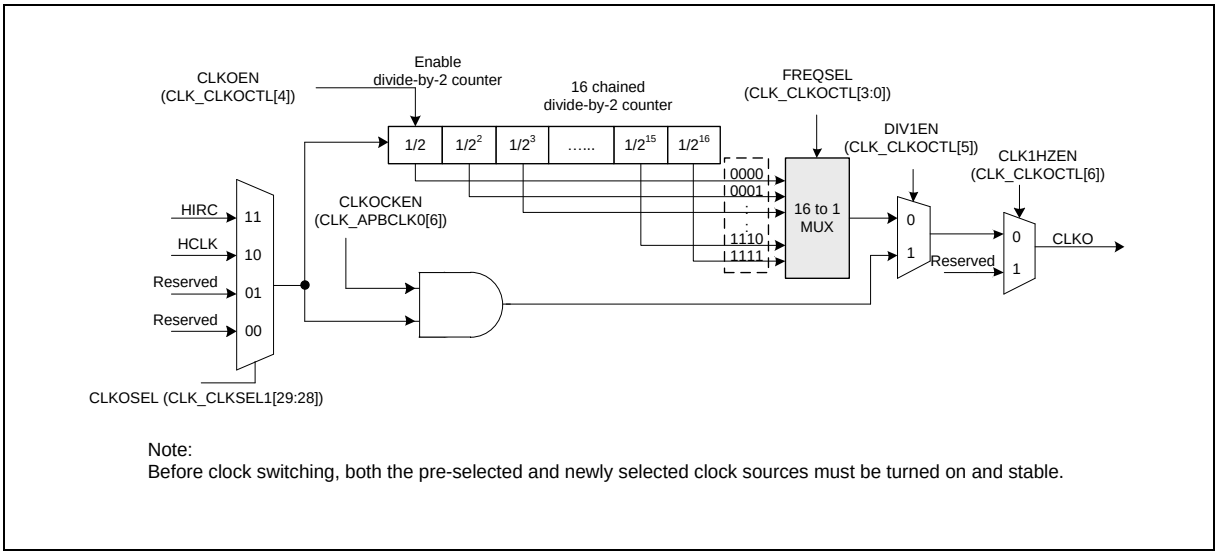


Figure 6.3-6 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

The FMC is equipped with on-chip embedded Flash for application. Thus, the total size of application ROM (APROM) is 32 Kbytes. A User Configuration block provides for system initiation. A 4 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A security protection ROM (SPROM) can conceal user program, and consists of native ISP functions. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 32 Kbytes application ROM (APROM)
- Supports 4 Kbytes loader ROM (LDROM)
- Supports 1 Kbytes security protection ROM (SPROM) to conceal user program
- Supports 16 bytes User Configuration block to control system initiation
- Supports 512 bytes page erase for all embedded Flash
- Supports 32-bit Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 18 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 18 pins are arranged in 4 ports named as PB, PC, PE, and PF. PB has 14 pins on port. PC has 1 pin on port. PF has 2 pins on port. PE has 1 pins on port. Each of the 18 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Please refer Datasheet for detailed pin operation voltage information about V_{DD} electrical characteristics.

6.5.2 Features

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level trigger setting
- I/O pin internal pull-up resistor enabled only in Quasi-bidirectional I/O mode
- Software selectable slew rate control
- Reset pin can be configured as GPIO

6.6 Timer Controller (TMR)

6.6.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.6.2 Features

6.6.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Support 3-bit capture input noise filter
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin (TMx_EXT) event for interval measurement
- Supports external capture pin (TMx_EXT) event to reset 24-bit up counter
- Supports internal clock (HIRC, LIRC) for capture event
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Supports Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM and ADC function
- Supports Inter-Timer trigger mode

6.7 PWM Generator and Capture Timer (PWM)

6.7.1 Overview

The chip provides one PWM generators. PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events use to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode, they have difference architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.7.2 Features

6.7.2.1 PWM Function Features

- Supports maximum clock frequency up to 24 MHz
- Supports up to two PWM modules, each module provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter matches 0, period value or compared value

6.7.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition

- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.8 Window Watchdog Timer (WWDT)

6.8.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.8.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.9 Enhanced Input Capture Timer (ECAP)

6.9.1 Overview

This device provides up to two units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.9.2 Features

- 3 input channels.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.
- Supports window mode capture function.

6.10 UART Interface Controller (UART)

6.10.1 Overview

The chip provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.10.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS and incoming data wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports Single-wire function mode

UART Feature	UART0/ UART1/
FIFO	16 Bytes
Auto Flow Control (CTS/RTS)	√
IrDA	√
RS-485 Function Mode	√
nCTS Wake-up	√

Incoming Data Wake-up	√
Baud Rate Compensation	√
Auto-Baud Rate Measurement	√
STOP Bit Length	1, 1.5, 2 bit
Word Length	5, 6, 7, 8 bits
Even / Odd Parity	√
Stick Bit	√
Note: √= Supported	

Table 6.10-1 UART Features

6.11 I²C Serial Interface Controller (I²C)

6.11.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There is one set of I²C controller which supports Power-down wake-up function.

6.11.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports one I²C port
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allow devices with different bit rates to communicate via one serial bus
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports two-level buffer function (only support in slave mode)
- Supports setup/hold time programmable

6.12 USCI - Universal Serial Control Interface Controller (USCI)

6.12.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.13 USCI – UART Mode

6.13.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.13.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.14 USCI - SPI Mode

6.14.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

6.14.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.15 USCI - I²C Mode

6.15.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP).

6.15.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by received ‘START’ symbol or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.16 Analog-to-Digital Converter (ADC)

6.16.1 Overview

The ADC contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with 8 input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin (ADC0_ST), timer0~3 overflow pulse trigger, PWM trigger trigger.

6.16.2 Features

- Operating voltage: 2.4V~5.5V.
- 12-bit resolution.
- Up to 8 single-end analog input channels.
- Maximum ADC peripheral clock frequency is 24 MHz.
- Up to 500 KSPS sampling rate.
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (ADC0_ST)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- Supports extend sample time function (0~16383 ADC clock).
- One internal channel from band-gap voltage (V_{BG}).

Note1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note2: If the internal channel for band-gap voltage is active, the maximum sampling rate will be 50k SPS.

6.17 Peripherals Interconnection

6.17.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast responds.

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme

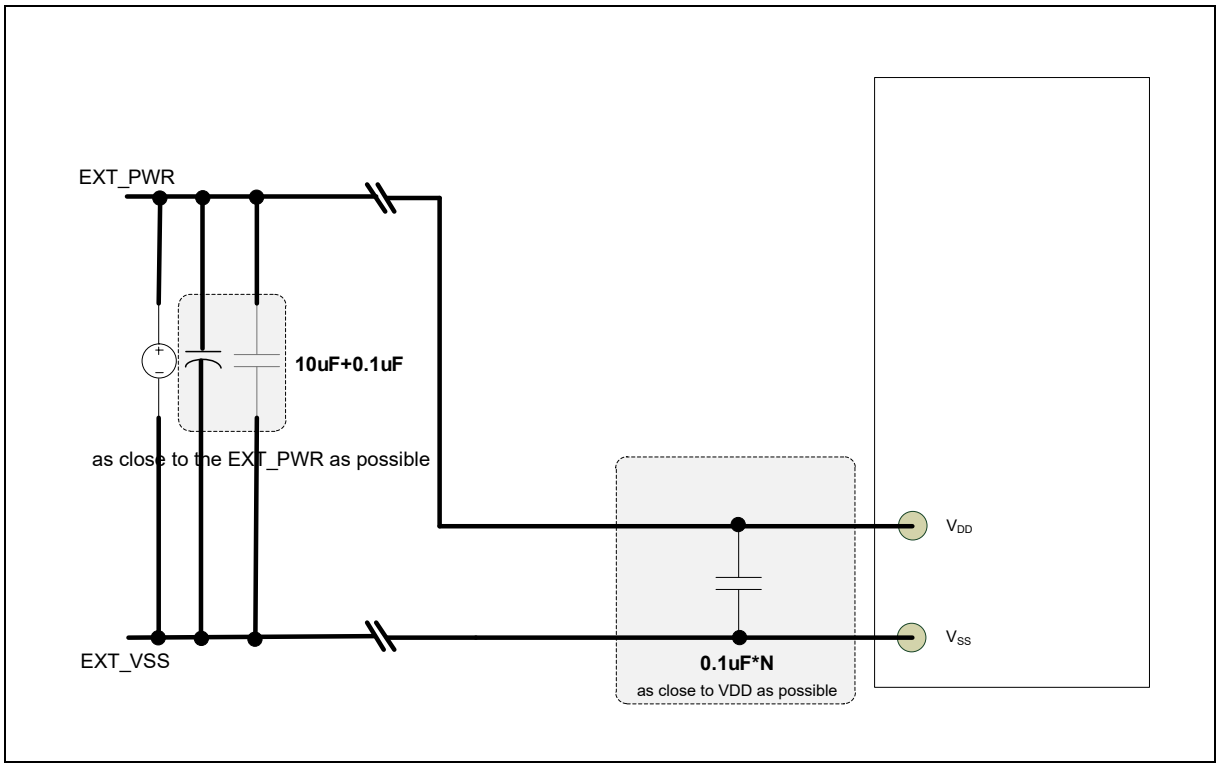
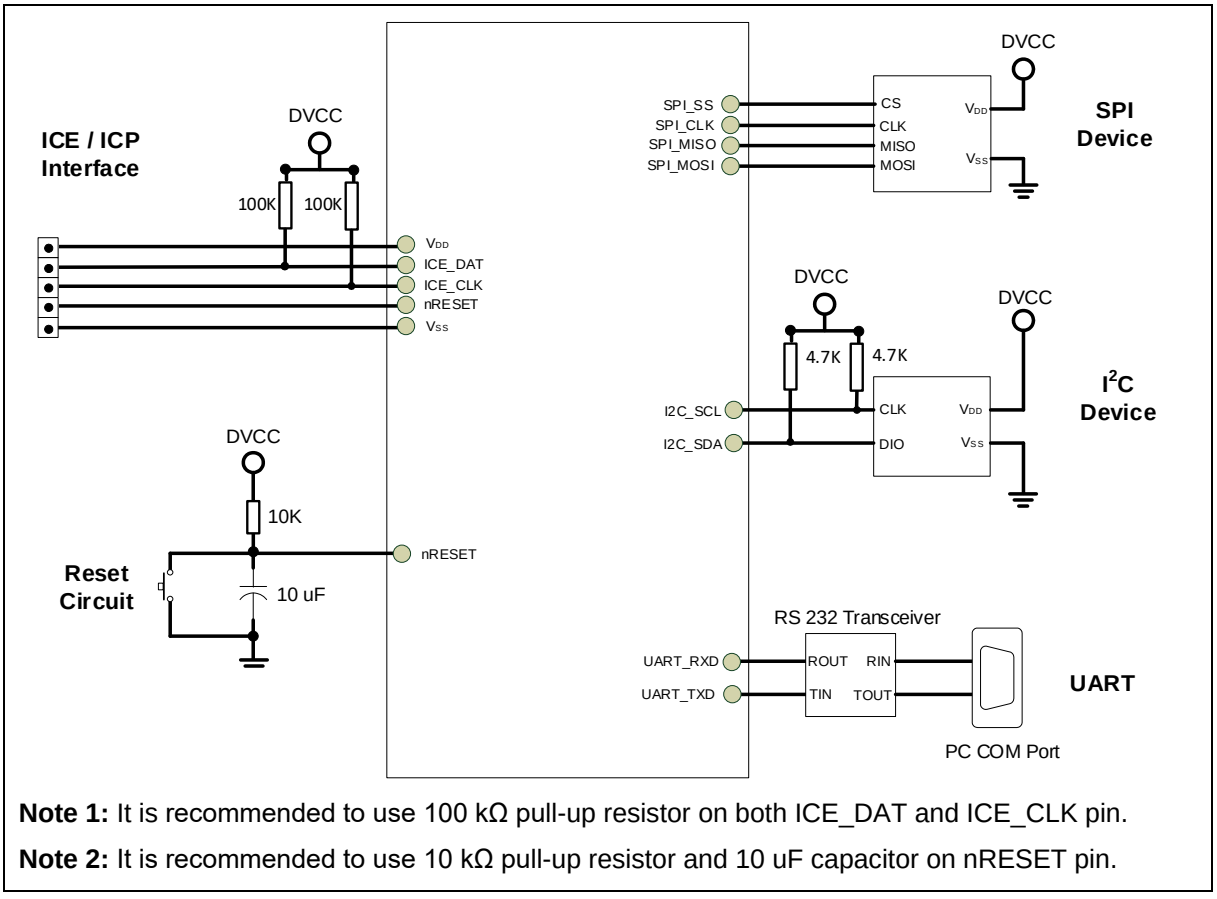


Figure 7.1-1 NuMicro® M2003 Power supply circuit

7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

Figure 7.2-1 NuMicro® M2003 Peripheral interface circuit

8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on any other pin[2]	V_{SS}-0.3	5.5	V

Notes:

1. All main power (V_{DD}) and ground (V_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current
3. 5V- tolerance pin specification does not include PC0~PC3 (Type-C PD pin)

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[1]	Maximum current into V_{DD}	-	150	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	150	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[2]	-	100	
	Maximum current sourced by total I/O Pins[2]	-	100	
$I_{INJ(PIN)}$ [3]	Maximum injected current by an I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA}) = T_C + (P_D \times \theta_{JC})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- θ_{JC} = thermal resistance junction-case (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[1]	Thermal resistance junction-ambient 20-pin TSSOP(4.4x6.5 mm)	-	38	-	℃/Watt
	Thermal resistance junction-ambient 20-pin QFN(3x3 mm)	-	68	-	℃/Watt
θ_{JC}[1]	Thermal resistance junction-case 20-pin TSSOP(4.4x6.5 mm)	-	10	-	℃/Watt
	Thermal resistance junction-case 20-pin QFN(3x3 mm)	-	7.5	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latch up performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system.

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International Electrotechnical Commission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[3]	Pin current for latch-up[3]	-200	-	+200	mA
V_{EFT}[4]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test and the performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
20-pin QFN(3x3 mm) [1]	MSL 3
20-pin TSSOP(4.4x6.5 mm) [1]	MSL 3

Note:

1. Determined according to IPC/JEDEC J-STD-020

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

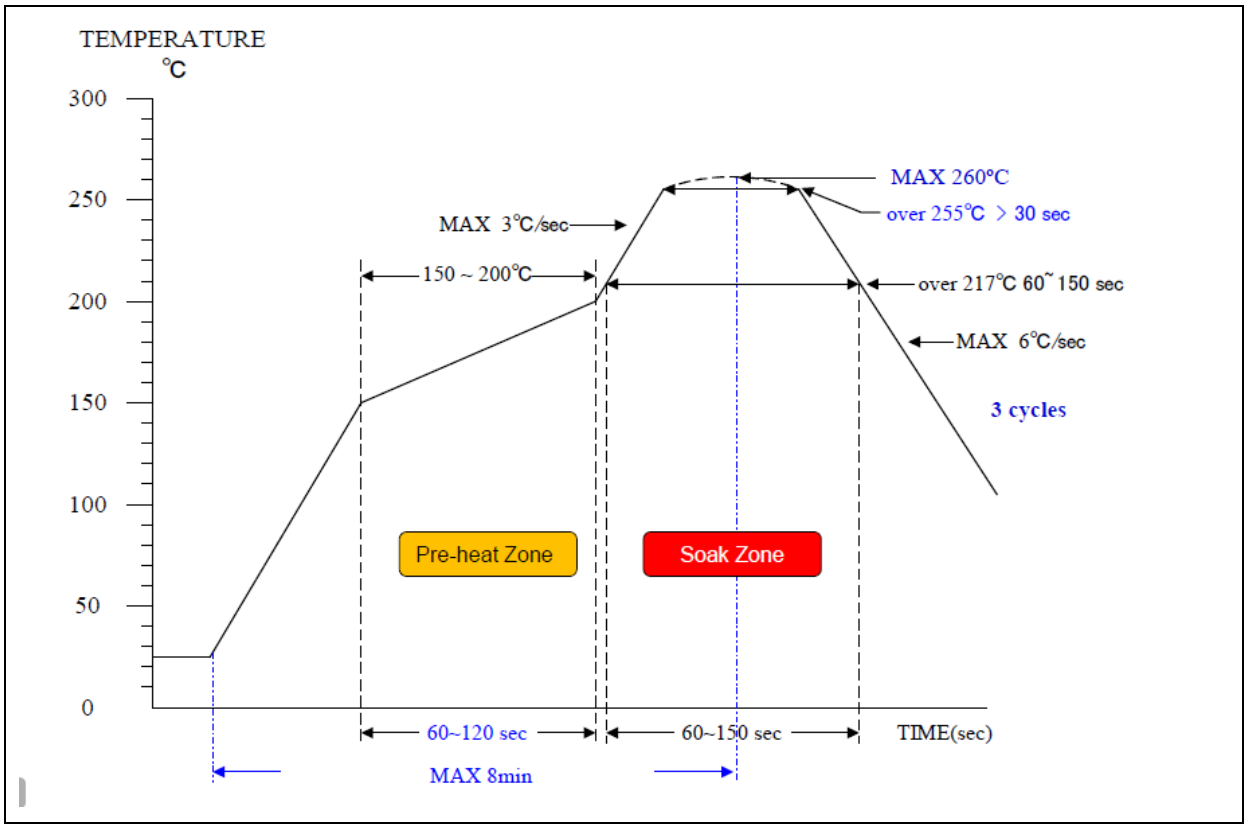


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5 V, T_A = 25°C, HCLK = 24 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	24	MHz	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	AV_{DD}				
V_{BG}	Band-gap voltage	1.15	1.2	1.30	mV	T_A = 25 °C
		1.14		1.33		T_A = -40°C ~105 °C
T_{VBG_ADC}[3]	ADC sampling time when reading the band-gap voltage	20	-	-	µS	

Note:

1. It is recommended to power VDD and AVDD from the same source. A maximum difference of 0.3 V between VDD and AVDD can be tolerated during power-on and power-off operation .
2. To ensure stability, an external output capacitor, CLDO must be connected between the LDO_CAP pin and the closest GND pin of the device. If there are two LDO_CAP pins or more, the capacitor value on each LDO pin needs to be divided equally.Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.
4. The specific operation voltage range of analog peripheral is listed in section 8.5.

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.4 ~ 5.5 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals are enabled, HCLK is the system clock and $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
		V_{DD}	5.5 V	5.5 V	5.5 V	5.5 V	
I_{DD_RUN}	Normal run mode executed from Flash, all peripherals disable, HIRC or LIRC clock	24 MHz	2.6	2.7	2.7	2.9	mA
		12 MHz	2.2	2.2	2.3	2.5	
		6 MHz	1.7	1.7	1.8	2.0	
		4 MHz	1.5	1.5	1.6	1.8	
		2 MHz	1.3	1.3	1.4	1.6	
		1.5 MHz	1.2	1.1	1.3	1.5	
		10 kHz	0.35	0.33	0.45	0.6	
	Normal run mode executed from Flash, all peripherals enable, HIRC or LIRC clock.	24 MHz	4.1	4.2	4.2	4.3	
		12 MHz	3.1	3.1	3.2	3.5	
		6 MHz	2.4	2.4	2.5	2.7	
		4 MHz	1.9	1.9	2.0	2.2	
		2 MHz	1.7	1.7	1.8	1.9	
		1.5 MHz	1.6	1.6	1.7	1.8	
		10 kHz	0.4	0.35	0.5	0.7	

Notes:

1. When analog peripheral blocks such as ADC, Timer, UART, PWM, I2C, USCI, HIRC, and LIRC are ON or GPIO toggle out, an additional power consumption should be considered.
2. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.

Table 8.3-1 Current Consumption In Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [1]	Max[1][2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
		V_{DD}	5.5 V	5.5 V	5.5 V	5.5 V	
I_{DD_IDLE}	Idle mode executed from Flash, all peripherals disable PLL, HIRC or LIRC clock	24 MHz	1.4	1.4	1.5	1.7	mA
		12 MHz	1.2	1.1	1.3	1.5	
		6 MHz	1.1	1.0	1.2	1.4	
		4 MHz	1.1	1.0	1.2	1.4	
		2 MHz	1.05	1.0	1.15	1.3	
		1.5 MHz	1.0	1.0	1.1	1.3	
		10 kHz	0.32	0.3	0.4	0.55	
	Idle mode executed from Flash, all peripherals enable PLL, HIRC or LIRC clock	24 MHz	2.6	2.7	2.7	2.9	
		12 MHz	2.1	2.1	2.2	2.4	
		6 MHz	1.6	1.6	1.7	1.9	
		4 MHz	1.4	1.4	1.5	1.7	
		2 MHz	1.2	1.2	1.3	1.5	
		1.5 MHz	1.15	1.1	1.2	1.4	
		10 kHz	0.32	0.3	0.4	0.55	

Notes:

1. When analog peripheral blocks such as ADC, HIRC and LIRC are ON, an additional power consumption should be considered.
2. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.

Table 8.3-2 Current consumption in Idle mode

Symbol	Test Conditions	Typ[2]				Max[3][4]			Unit
		T_A = 25 °C				T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
		2.4 V	3.3 V	4.5 V	5.5 V	5.5 V			
I_{DD_PD}	Power-down mode, all peripherals disable	5.5	5.8	6	6.5	6	9.2	30	µA
	Power-down mode, LVR enable and run, any other peripherals disable	5.9	6.2	6.5	7	6.2	10[2]	32	
	Power-down mode, LVR & BOD enable and run, any other peripherals disable	150	155	170	200	180	210	260	

Notes:

1. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.
2. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption In Power-down Mode

8.3.2 Wakeup Time From Low-Power Modes

The wakeup times given in Table 8.2-1 is measured on a wakeup phase with a 24 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode	17	-	cycles
t_{WU_NPD0}[1][2]	Wakeup from normal Power-down mode 0 running in flash	11.36	16	µS
t_{ET_IDLE}[1]	Enter to IDLE mode	17	-	cycles
t_{ET_NPD0}[1]	Enter to normal Power-down mode 0	1.64	-	µS

Notes:

1. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-4 Low-Power Mode Wakeup Timings

8.3.3 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} =
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on based on default clock source selection.

Peripheral	I_{DD}[1]	Unit
ADC	150	uA
FMC	53	
SRAM0	20	
GPB	29	
GPC	27	
GPE	28	
GPF	28	
TMR0	149	
TMR1	148	
TMR2	145	
TMR3	151	
CLKO	84	
I2C0	64	
UART0	215	
UART1	208	
USCI0	83	
WDT	102	
ECAP0	1	
PWM0	265	

Notes:

1. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.

Table 8.3-5 Peripheral Current Consumption

8.3.4 I/O DC Characteristics

8.3.4.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (I/O with TTL input)	V_{SS}-0.3	-	0.2V_{DD}-0.1	V	
V_{IL1}	Input low voltage (I/O with Schmitt trigger input and Xin)	0	-	0.3*V_{DD}	V	
V_{IH}	Input high voltage (I/O with TTL input)	0.2V_{DD}+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	0.7*V_{DD}	-	V_{DD}	V	
V_{HY}[1]	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[2]	Input leakage current	-1		1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1		1		V_{DD} < V_{IN} < 5.5 V, Open-drain or input only mode
R_{PU}	Pull up resistor	40	51	70	kΩ	

Notes:

1. All data listed is derived from thorough characterization, not tested in production unless explicitly stated otherwise Leakage could be higher than the maximum value, if abnormal injection happens.
2. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.3-6 I/O Input Characteristics

8.3.4.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-6.6	-	-9.3	µA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6.6	-	-9.3	µA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-6.6	-	-9.3	µA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-57.2	-	-58.3	µA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-9	-	-9.6	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-6	-	-6.6	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-4.2	-	-4.9	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V

		-18	-	-39	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	13	-	17	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		8	-	12	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		6	-	8	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-7 I/O Output Characteristics

8.3.4.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}[1]	Internal nRESET pull up resistor	45	-	60	KΩ	V_{DD} = 5.5 V
		45	-	65		V_{DD} = 2.4 V
t_{FR}[1]	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		10	-	25		Power down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-8 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 24 MHz Internal High Speed RC Oscillator (HIRC)

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +85 °C, V_{DD} = 2.4 ~ 5.5V
		-3[4]		3[4]	%	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	µA	
T_S[3]	Stable time	-	3	5	µs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Notes:

1. Default setting value for the product
2. Based on reload value.
3. Based on characterization, tested in production.
4. Guaranteed by characterization result, not tested in production.

Table 8.4-1 24 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.4.2 Internal 10 kHz Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[1]	-	10[1]	%	T_A = 25 °C, V_{DD} = 5V
		-35[2]	-	35[2]	%	T_A=-40~105°C Without software calibration
I_{LRC}[3]	Operating current	-	0.85	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Notes:

1. Guaranteed by characterization, tested in production.
2. Guaranteed by characterization, not tested in production.
3. Guaranteed by design.

Table 8.4-2 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.3 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[1].	Unit	Test Conditions[2]
$t_{f(IO)out}$	Normal mode [4] output high (90%) to low level (10%) falling time	4.6	5.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.9	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		6.6	8		C_L = 30 pF, V_{DD} >= 3.3 V
		4.3	5		C_L = 10 pF, V_{DD} >= 3.3 V
		8.5	12.5		C_L = 30 pF, V_{DD} >= 2.4 V
		8.0	10.7		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{f(IO)out}$	High slew rate mode [5] output high (90%) to low level (10%) falling time	4.0	4.3	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		4.9	5.8		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	13.8		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [4] output low (10%) to high level (90%) rising time	5.6	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.4	3.7		C_L = 10 pF, V_{DD} >= 5.5 V
		8.1	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		5.1	5.8		C_L = 10 pF, V_{DD} >= 3.3 V
		15.1	20.3		C_L = 30 pF, V_{DD} >= 2.4 V
		9.6	12.4		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	High slew rate mode [5] output low (10%) to high level (90%) rising time	4.8	5.2	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.1	2.5		C_L = 10 pF, V_{DD} >= 5.5 V
		6.4	7.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.0	3.7		C_L = 10 pF, V_{DD} >= 3.3 V
		12.7	16.9		C_L = 30 pF, V_{DD} >= 2.4 V
		5.4	7.4		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$[3]	I/O maximum frequency	24	24	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. PxSR.n bit value = 0, Normal output slew rate
5. PxSR.n bit value = 1, high speed output slew rate

Table 8.4-3 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[1]	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}[1]	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}[1]	BOD operating current	-	200	230		AV_{DD} = 5.5V
V_{PORR}	POR reset voltage (Power on rising threshold level)	1	1.15	1.3	V	-
V_{PORF}	POR reset voltage (Power off falling threshold level)	0.9	1.05	1.15		-
V_{LVR}	LVR reset threshold voltage	1.7	2.0	2.4		-
V_{BODR}	BOD brown-out detect voltage (Power on rising threshold level)	4.2	4.5	4.8		BOV[1:0] = [0,0]
		3.6	3.8	4.0		BOV[1:0] = [0,1]
		2.6	2.8	3		BOV[1:0] = [1,0]
		2.1	2.3	2.5		BOV[1:0] = [1,1]
V_{BODF}	BOD brown-out detect voltage (Power off falling threshold level)	4.1	4.4	4.7		BOV[1:0] = [0,0]
		3.5	3.7	3.9		BOV[1:0] = [0,1]
		2.5	2.7	2.9		BOV[1:0] = [1,0]
		2.0	2.2	2.4		BOV[1:0] = [1,1]
T_{LVR_SU}[1]	LVR startup time	60	-	80	μs	-
T_{LVR_RE}[1]	LVR respond time	0.4	-	4		Fsys = HIRC
		180	-	350		Fsys = LIRC
T_{BOD_SU}[1]	BOD startup time	180	-	320		Fsys = HIRC
T_{BOD_RE}[1]	BOD respond time	2.5	-	5		Fsys = HIRC
R_{VDDR}[1]	V_{DD} rise time rate	160	-	-	μS/V	POR Enabled
R_{VDDF}[1]	V_{DD} fall time rate	160	-	-		POR Enabled
		250	-	-		LVR Enabled
		160	-	-		BOD Enabled with Normal mode

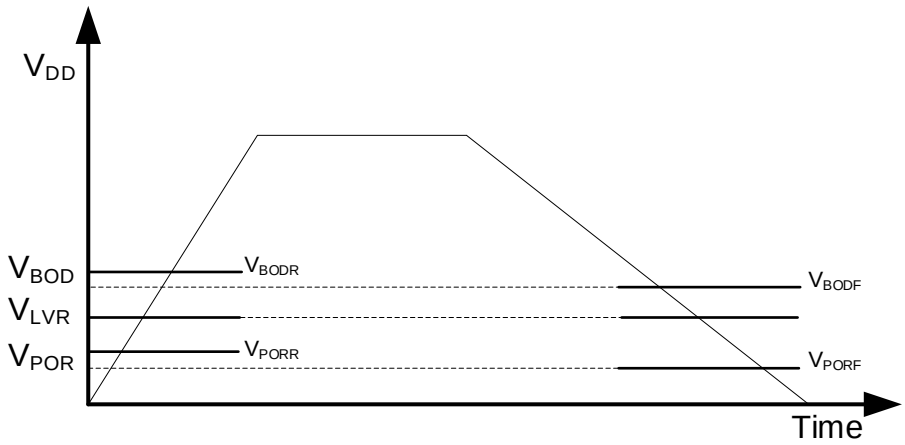
Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 8.5-2 Minimum Brown-Out Detect Pulse Width



Note: V_{POR} detect internal LDO voltage.

Figure 8.5-1 Power Ramp Up/Down Condition

8.5.2 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	2.4	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference voltage	2.4	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 500 kHz $T_{CONV} = 17 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADCEC}[1]	Encoding Rate	500			kHz	This value is fixed by ADC module
T_{ADCEC}	Encoding Time	2			μs	This value is fixed by ADC module
F_{ADCSMP}[1]	ADC Sampling Clock frequency	F_{SYS}/8		F_{SYS}	kHz	base on ADCDIV (ADCCON1[5:4]
T_{ADCSMP}	ADC Sampling Time [2]z	0.375	-	17	μs	F_{SYS} = 16MHz;
		0.417	-	11.3	μs	Fsys = 24MHz; ADCAQT = 1 by software[3]
F_{ADCCOV}	Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$	52.6		421	kHz	F_{SYS} = 16MHz;
		75.2		413	kHz	F_{SYS} = 24MHz;
T_{ADCCOV}[2]	Conversion Time $T_{ADCCOV} = T_{SMP} + T_{ADCEC}$	2.375		19	μs	F_{SYS} = 16MHz;
		2.417		13.3	μs	F_{SYS} = 24MHz;
T_{ADCEN}	ADC Enable to ready time	20	-	-	μs	
INL[1]	Integral Non-Linearity Error	-3	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[1]	Gain error	-0.4	-	+3.5	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_O[1]$_T$	Offset error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[1]	Absolute Error	-7		+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$
R_S	Input Channel Equivalent Resistance		0.5	2.5	kΩ	
C_{IN}	Input Equivalent Capacitance		2.5		pF	
R_{IN}[1]	Internal Switch Resistance	-	0.5	-	kΩ	
R_{EX}[1]	External input impedance	-	-	33	kΩ	

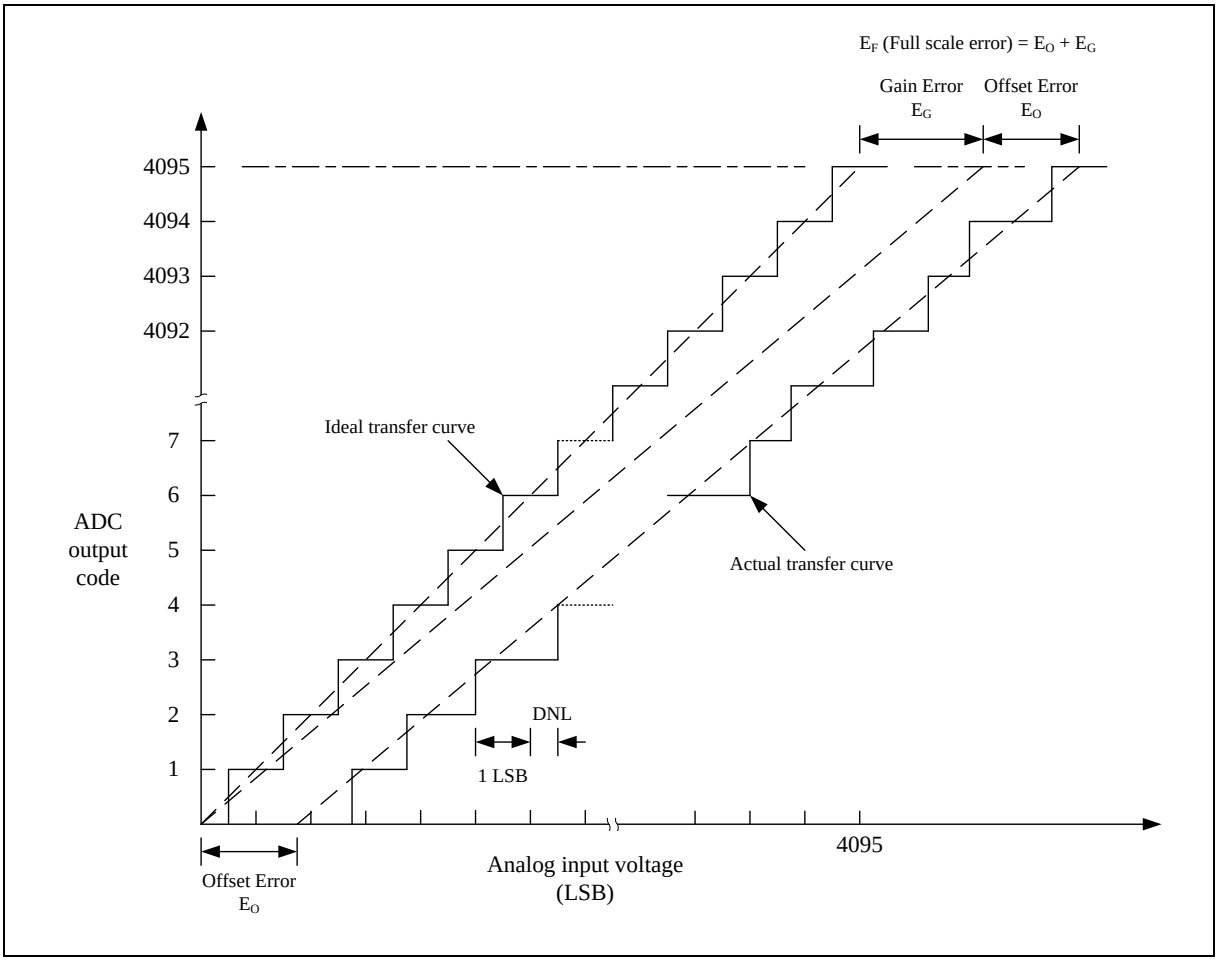
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

Note：

1. Guaranteed by characterization result, not tested in production.
2. ADC Convertion time T_{ADCCOV} = ADC Sampling Time (T_{SMP}) + ADC Encoding Time (T_{ADCEC}).
3. ADC Sampling Time T_{SMP} =. $\frac{4 * ADCAQT + 6}{F_{ADCSMP}}$ （F_{ADCSMP} base on ADCDIV (ADCCON1[5:4])

   F_{SYS} = 24MHz, ADC Sampling Time Minimum condition $\frac{4*1+6}{24MHz}$ (ADCAQT = 1, ADCDIV = 0), Since the minimum sampling time must over 370ns that means when FADCAQT = 24MHz, ADCAQT must be set as 1 by software at least.
4. R_{EX} maximum formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (TSMP). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.6 Communications Characteristics

8.6.1 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-1 I²C Characteristics

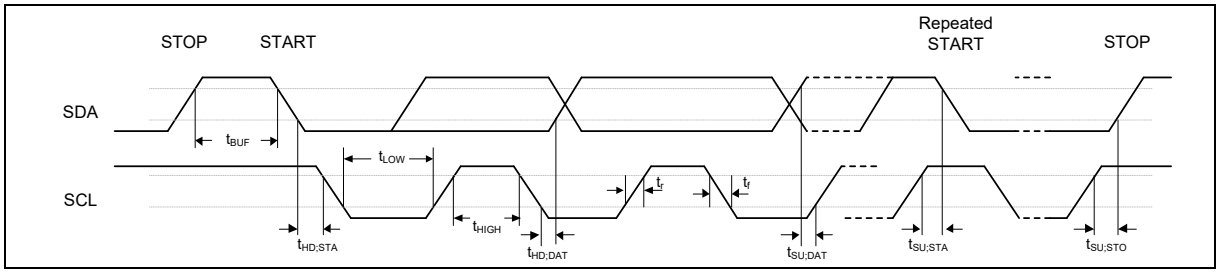


Figure 8.6-1 I²C Timing Diagram

8.6.2 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min [1]	Typ	Max[1]	Unit	Test Conditions
F_{SPICLK} $1/T_{SPICLK}$	SPI clock frequency			$F_{SYS}/2$	MHz	2.4 V ≤ VDD ≤ 5.5 V, CL = 30 pF
t_{CLKH}	Clock output High time	$T_{SPICLK}/2$			nS	
t_{CLKL}	Clock output Low time	$T_{SPICLK}/2$			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	1	nS	2.4 V ≤ VDD ≤ 5.5 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-2 USCI-SPI Master Mode Characteristics

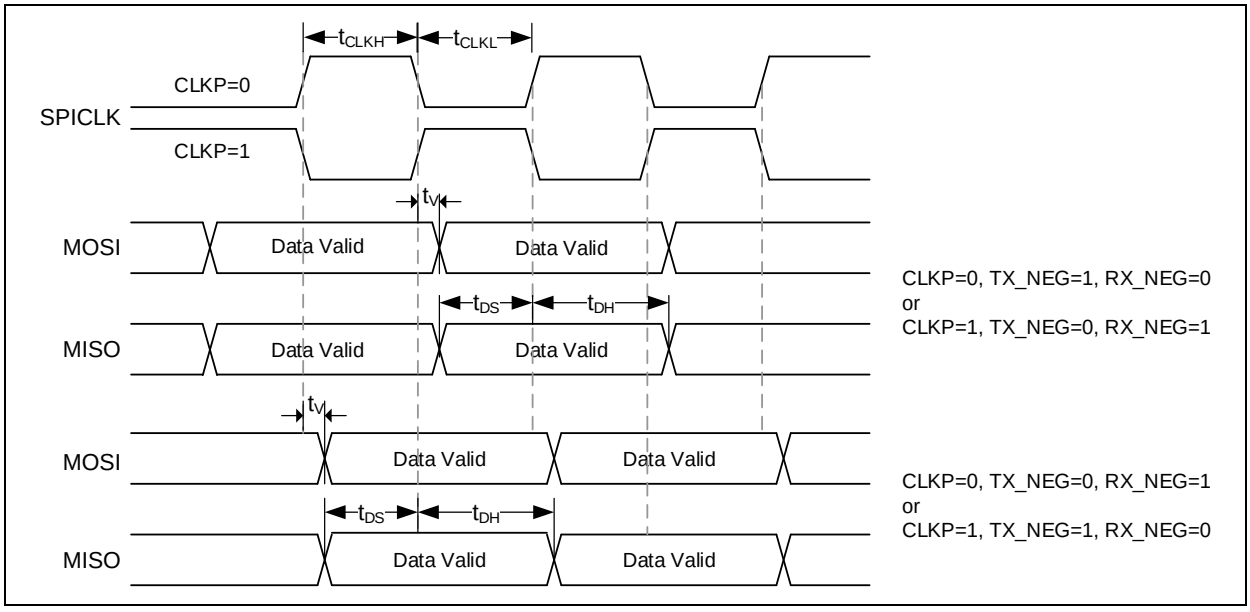


Figure 8.6-2 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [1]	Typ	Max [1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	$F_{SYS}/ 2$	MHz	2.4 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	$T_{SPICLK} / 2$			nS	
t_{CLKL}	Clock output Low time	$T_{SPICLK} / 2$			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	nS	2.4 V ≤ VDD ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	2	-	-	nS	
t_V	Data output valid time	-	-	39.5	nS	2.4 V ≤ VDD ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

Table 8.6-3 USCI-SPI Slave Mode Characteristics

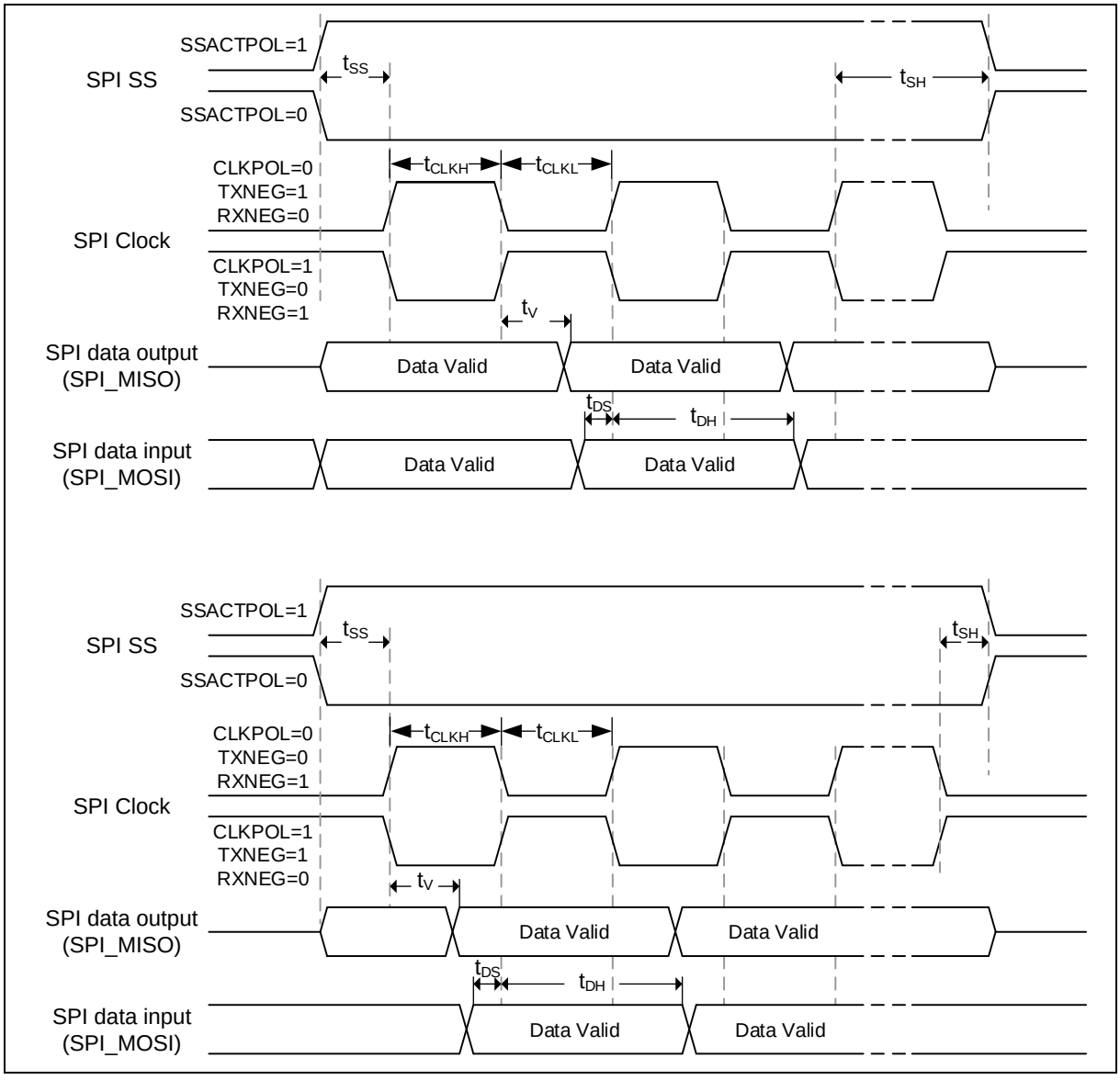


Figure 8.6-3 USCI-SPI Slave Mode Timing Diagram

8.6.3 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Notes:

1. Guaranteed by characteristic, not tested in production for I²C Master Mode
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-4 USCI-I²C Characteristics

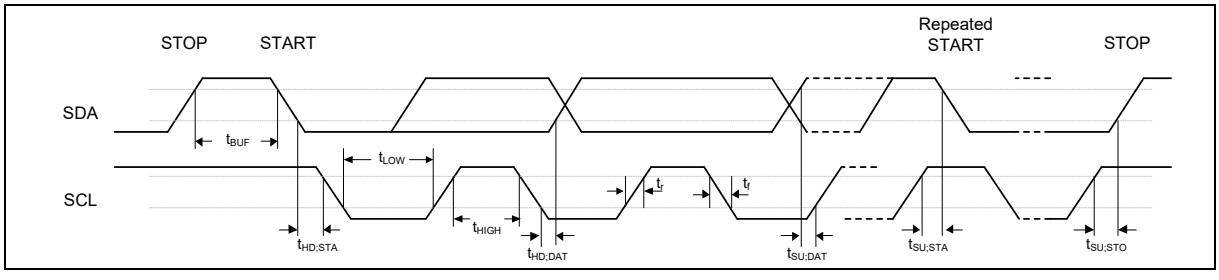
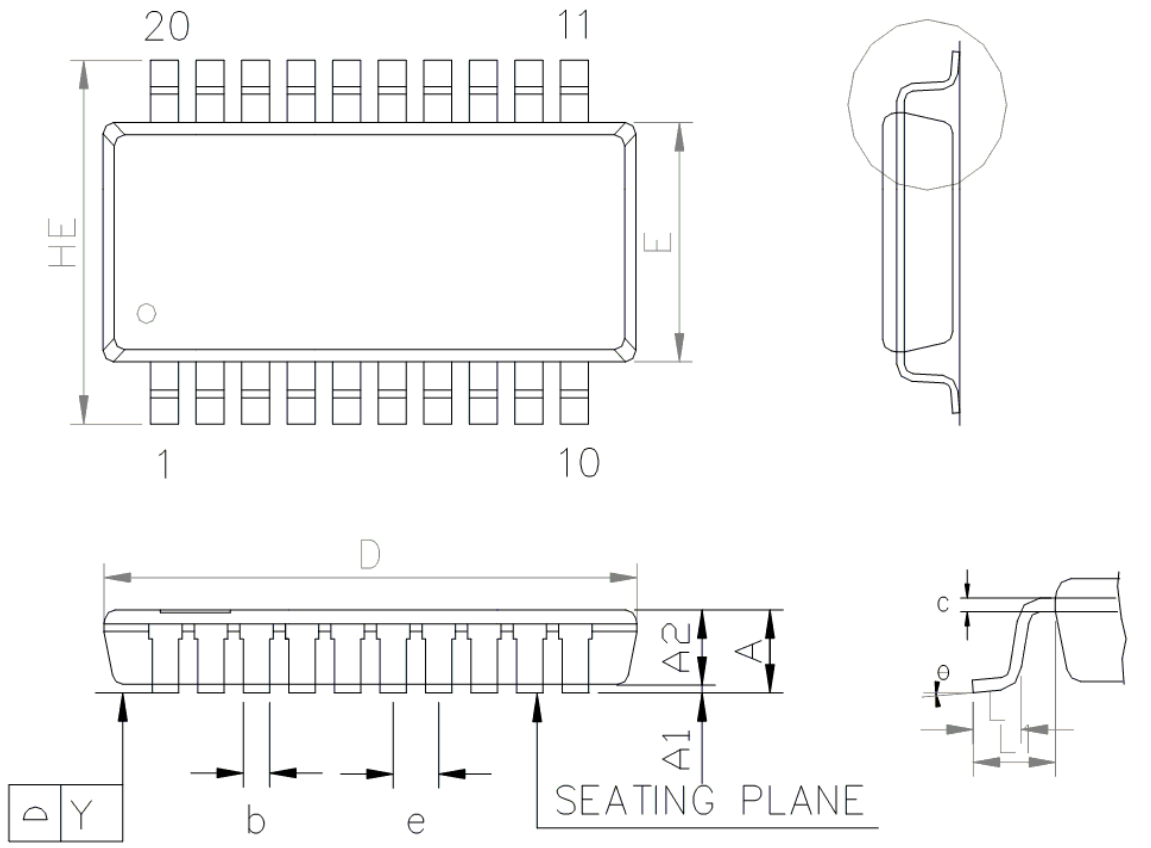


Figure 8.6-4 USCI-I²C Timing Diagram

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

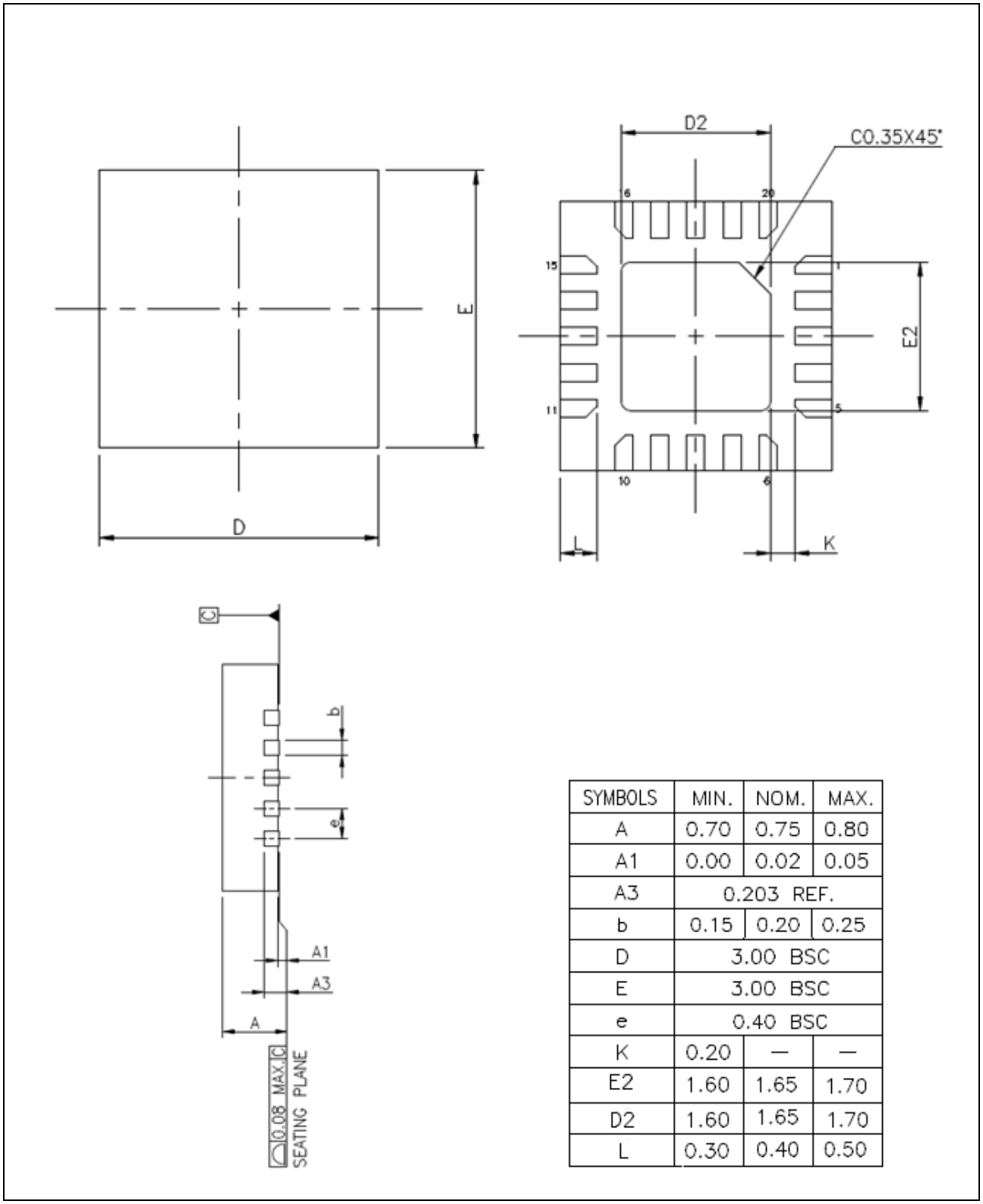
9.1 TSSOP 20-pin (4.4 x 6.5 x 0.9 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	0.90	1.05	0.031	0.035	0.041
E	4.30	4.40	4.50	0.169	0.173	0.177
HE	6.40 BSC			0.252 BSC		
D	6.40	6.50	6.60	0.252	0.256	0.260
L	0.50	0.60	0.75	0.020	0.024	0.030
L1	1.00 REF			0.039 REF		
b	0.19	-	0.30	0.007	-	0.012
e	0.65 BSC			0.026 BSC		
c	0.09	-	0.20	0.004	-	0.008
θ	0°	-	8°	0°	-	8°
Y	0.10 BASIC			0.004 BASIC		

Figure 9.1-1 TSSOP-20 Package Dimension

9.2 QFN 20-pin (3.0 x 3.0 x 0.8 mm)



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		3.00 BSC	
E		3.00 BSC	
e		0.40 BSC	
K	0.20	—	—
E2	1.60	1.65	1.70
D2	1.60	1.65	1.70
L	0.30	0.40	0.50

Figure 9.2-1 QFN-20 Package Dimension

9.3 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	2.5	-	ms	T_A = 25℃
T_{PROG}	Program time	-	20	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	4	-	mA	
I_{DD3}	Erase current	-	2	-	mA	
N_{ENDUR}	Endurance	100,000[2]	-		cycles	T_A = -40℃~105℃
T_{RET}	Data retention	50	-	-	year	100 k cycle[3] T_A = 55℃
		25	-	-	year	100 k cycle[3] T_A = 85℃
		10	-	-	year	100 k cycle[3] T_A = 105℃

Notes:

1. Number of program/erase cycles.
2. Guaranteed by design.
3. One Flash cycle is defined as the programming of a sector followed by an erase of the sector. The same address cannot be programmed again before next erase for program disturb concern.

Table 9.3-1 Flash Memory Characteristics

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
APB	Advanced Peripheral Bus
BOD	Brown-out Detection
FIFO	First In, First Out
FMC	Flash Memory Controller
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PWM	Pulse Width Modulation
QEI	Quadrature Encoder Interface
SPI	Serial Peripheral Interface
SPS	Samples per Second
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2024.04.10	1.00	Initial version.

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