NuMicro® Family

Arm® Cortex®-M0-based Microcontroller

M0A23U Series
Datasheet

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1 GENERAL DESCRIPTION

The NuMicro® M0A23U series 32-bit microcontroller based on Arm® Cortex®-M0 core is qualified by AEC-Q100 grade 1 with LIN and CAN support. It provides compact packages with highly flexible digital pin function assignment, rich analog peripherals, -40°C to 125°C operating temperature, 2.4V ~ 5.5V operating voltage, CAN 2.0B and LIN interface for robust communication. The M0A23U series targets robust and high operating temperature applications, such as 24 GHz mmWave radar, Battery Management System (BMS), car lighting, electric window lifter, and power seat.

The M0A23U series provides SSOP20 and TSSOP28 package with rich analog and digital functions, which are especially suitable for small form factor applications. The SSOP20 provides up to 18 I/O pins and the TSSOP28 provides up to 26 I/O pins. Each I/O pin of the M0A23U series can be arbitrarily assigned to digital peripherals, such as UART, SPI, and PWM. The M0A23U series provides rich analog functions including 17-ch 12-bit 800 kSPS ADC, 1 set of 5-bit DAC and 2 sets of ACMP in both SSOP20 and TSSOP28 package. Moreover, it provides low voltage reset (LVR) and brown-out detector (BOD) to ensure the system safety.

The M0A23U series runs up to 48 MHz and supports hardware divider. It provides 32 Kbytes Flash memory, 4 Kbytes SRAM and 2 Kbytes LDROM for ISP (In-System Programming) feature for easily firmware update. It is equipped with plenty of peripherals including up to four 32-bit timers, 6-ch 16-bit PWM generators, 1 set of CAN 2.0B controller, 2 sets of LIN functions, 5-ch PDMA, 2 sets of UART with One-Wire mode, IrDA and RS485 functions. Besides, the M0A23U series provides two sets of Universal Serial Control Interfaces (USCI) that can be configured as UART, SPI or I^2C.

The package types of the M0A23U series include SSOP20 (5.3x7.2x1.75 mm) and TSSOP28 (4.4x9.7x1.0 mm).

1.1 Key Features and Applications

Product Line	CAN	UART	LIN	USCI	Timer	PWM	PDMA	ADC	ACMP	Divider
M0A23U	1	2	2	2	4	6	5	17	2	1

Table 1.1-1 NuMicro® M0A23U Series Key Features Table

The M0A23U series is targeted at applications such as:

- 24GHz mmWave radar
- BMS (Battery Management System)
- Industrial control
- Car lighting
- Car windows
- Power seat

2 FEATURES

Core and System	
Arm® Cortex®-M0	• Arm® Cortex®-M0 core, running up to 48 MHz • Built-in Nested Vectored Interrupt Controller (NVIC) • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Four-level BOD with brown-out interrupt and reset option(4.4V/3.7V/2.7V/2.3V)
Low Voltage Reset (LVR)	• LVR with 2.22V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • One built-in temperature sensor
AEC-Q100	• AEC-Q100 grade 1 qualified
32-bit H/W Divider(HDIV)	• Signed (two's complement) integer calculation • 32-bit dividend with 16-bit divisor calculation capacity • 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit) • 6 HCLK clocks taken for one cycle calculation
Memories	
Boot Loader	• Nuvoton ISP (In-System-Programming) tool for firmware upgrade via UART • ISP/IAP libraries
Flash	• Up to 32 KB application ROM (APROM) • 2 KB on-chip Flash for user-defined loader (LDROM) • All on-chip Flash support 512 bytes page erase • Fast Flash programming verification with CRC • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities

	• Configurable boot up sources including boot loader, user-defined loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit and multi-word Flash programming function
SRAM	• Up to 4 KB embedded SRAM • Supports byte-, half-word- and word-access • Supports PDMA mode
Cyclic Redundancy Calculation (CRC)	• Supports CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials • Programmable initial value • Programmable order reverse setting and one's complement setting for input data and CRC checksum • 8-bit, 16-bit, and 32-bit data width • 8-bit write mode with 1-AHB clock cycle operation • 16-bit write mode with 2-AHB clock cycle operation • 32-bit write mode with 4-AHB clock cycle operation • Uses DMA to write data with performing CRC operation
Peripheral DMA (PDMA)	• Supports up to 5 independent configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Fixed-priority and Round-robin priorities modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Request source can be from software, UART, ADC, PWM and Timer
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.768 kHz Low-speed eXternal crystal oscillator (LXT) for low-power system operation • Supports clock failure detection for external crystal oscillators

	and exception generatation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC) trimmed to ±0.25% accuracy that can optionally be used as a system clock • 38.4 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation
Timers	
32-bit Timer	• Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for enhanced interval measurement and resetting 24-bit up counter • Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated • Timer interrupt flag or external capture interrupt flag to trigger PWM, ADC and PDMA
PWM	• Three 16-bit counters with 12-bit prescale for six 48 MHz PWM output channels • Supports independent mode for PWM output/Capture input channel • Supports complementary mode for 3 complementary paired PWM output channel • Dead-time insertion with 12-bit resolution • Two compared values during one period • Supports 16-bit resolution PWM counter • Up, down or up-down PWM counter type • Supports mask function and tri-state enable for each PWM pin • Supports brake function • Up to 6 independent input capture channels with 16-bit resolution counter • Counter synchronous start function • Able to trigger ADC to start conversion
Watchdog	• 20-bit free running up counter for WDT time-out interval • Selectable time-out interval (24 ~ 220) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC)

	• System kept in reset state for a period of (1 / WDT_CLK) * 63. • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out • Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register • Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT
Window Watchdog	• Clock sources from HCLK/2048 (default selection) or LIRC • Window set by 6-bit down counter with 11-bit prescale • WWDT counter suspends in Idle/Power-down mode • Supports Interrupt
Analog Interfaces	
Analog-to-Digital Converter (ADC)	• Analog input voltage range: 0 ~ AV_{DD} (voltage of V_{DD} pin). • 12-bit resolution and 10-bit accuracy is guaranteed • Up to 17 single-end analog input channels or 8 differential analog input channels • Maximum ADC peripheral clock frequency is 16 MHz • Up to 800 kSPS sampling rate • Four operation modes: - Single mode: A/D conversion is performed one time on a specified channel - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion • An A/D conversion can be started by: - Software Write 1 to ADST bit - External pin (STADC) - Timer 0~3 overflow pulse trigger - PWM trigger

	• Each conversion result is held in data register of each channel with valid and overrun indicators • Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting. • 4 internal channels band-gap voltage (VBG), temperature sensor (V_{TEMP}), internal reference voltage and DAC0 output • Supports PDMA transfer mode
Digital to Analog Converter (DAC)	• Supports one 5-bit 100 kSPS voltage type DAC • Analog output voltage range: 0~AV_{DD} (voltage of V_{DD} pin) • Reference voltage from internal reference voltage V_{REF} pin or AV_{DD} • DAC maximum conversion updating rate 100 kSPS • Rail to rail settle time 10us • Supports software and timer0~3 trigger to start DAC conversion • Supports PDMA mode
Analog Comparator (ACMP)	• Analog input voltage range: 0 ~ AV_{DD} (voltage of V_{DD} pin) • Up to two rail-to-rail analog comparators • Supports hysteresis function • Supports wake-up function • Selectable input sources of positive input and negative input **ACMP0 supports:** • 3 multiplexed I/O pins at positive sources: - ACMP0_P0, Comparator Reference Voltage (CRV), and DAC0 output • 5 negative sources: - ACMP0_N0, ACMP0_N1, ACMP0_N2, ACMP0_N3 - Comparator Reference Voltage (CRV) **ACMP1 supports:** • 3 multiplexed I/O pins at positive sources: - ACMP1_P0, Comparator Reference Voltage (CRV), and DAC0 output • 5 negative sources: - ACMP1_N0, ACMP1_N1, ACMP1_N2, ACMP1_N3 - Comparator Reference Voltage (CRV) • Shares one ACMP interrupt vector for all comparators • Interrupts generated when compare results change (Interrupt

	event condition is programmable) • Supports triggers for break events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0, UART1 • UART baud rate clock from LXT (32.768 kHz) with 9600bps can work normally in power down mode even system clock is stopped • Full-duplex asynchronous communications • Separates receive and transmit 16/16 bytes entry FIFO for data payloads • Supports hardware auto-flow control (RX, TX, CTS and RTS) and programmable receiver buffer trigger level • Supports programmable baud rate generator for each channel individually • Supports 8-bit receiver buffer time-out detection function • Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT [15:8]) • Supports Auto-Baud Rate measurement and baud rate compensation function • Supports break error, frame error, parity error and receive/transmit buffer overflow detection function • Fully programmable serial-interface characteristics • Programmable number of data bit, 5-, 6-, 7-, 8- bit character • Programmable parity bit, even, odd, no parity or stick parity bit generation and detection • Programmable stop bit, 1, 1.5, or 2 stop bit generation • Supports LIN function mode • Supports LIN master/slave mode • Supports programmable break generation function for transmitter • Supports break detection function for receiver • Supports LIN slave header time-out detection function • Supports LIN response time-out detection function • Supports LIN wake-up function • Supports IrDA SIR function mode • Supports for 3/16 bit duration for normal mode

	• Supports RS-485 mode • Supports RS-485 9-bit mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function • Supports PDMA mode • Supports Single-wire function mode.
CAN	• Supports CAN protocol version 2.0 part A and B • Bit rates up to 1 MBit/s • 32 Message Objects • Supports wake-up function
Universal Serial Control Interface (USCI)	• Supports one set of USCI • USCI supports UART, SPI and I^2C function • Single byte TX and RX buffer mode **UART** • One transmit buffer and two receive buffer for data payload • Hardware auto flow control function and programmable flow control trigger level • Programmable baud-rate generator • Supports 9-Bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports Wake-up function (Data and nCTS Wakeup Only) • Supports PDMA transfer **SPI** • Master or Slave mode operation (maximum frequency: master = fPCLK / 2, slave < fPCLK / 5) • Configurable bit length of a transfer word from 4 to 16-bit • One transmit buffer and two receive buffer for data payload • MSB first or LSB first transfer sequence • Word suspend function • Supports PDMA transfer • Supports 3-wire, no slave select signal, bi-direction interface • Wake-up function: input slave select transition

	• Supports one data channel half-duplex transfer
I²C	
	• Full master and slave device capability • 7-bit addressing mode (10-bit mode Not supported) • Communication in standard mode (100 kbps) or in fast mode (up to 400 kbps) • Multi-master bus • One transmit buffer and two receive buffer for data payload • Supports 10-bit bus time-out capability • Supports Bus monitor mode • Power down wake-up by data toggle or address match • Multiple address recognition • Device address flag • Setup/hold time programmable
GPIO	• Four I/O modes: - Quasi-bidirectional mode - Push-Pull Output mode - Open-Drain Output mode - Input only with high impendence mode • Schmitt trigger input • I/O pin configured as interrupt source with edge/level trigger setting • Supports high drive and high sink current I/O • Supports independent pull-up control • Maximum I/O Speed is 24 MHz when V_{DD} = 2.4 ~ 5.5V. • Supports up to 18/26 GPIOs for SSOP20 TSSOP28 respectively • Enabling the pin interrupt function will also enable the wake-up function

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

SSOP20	TSSOP28
M0A23OC1ACU	M0A23EC1ACU

3.2 NuMicro® M0A23U Series Selection Guide

3.2.1 NuMicro® M0A23U Series

Part Number	Flash (KB)	SRAM (KB)	ISP ROM (KB)	I/O	Timer	PWM	PDMA	Connectivity				DAC	LXT	ACMP	ADC(12-Bit)	AEC-Q100	Package
								USCI*	UART	LIN	CAN						
M0A23OC1ACU	32	4	2	18	4	6	5	2	2	2	1	1	1	2	17-ch	Grade 1	SSOP20
M0A23EC1ACU	32	4	2	26	4	6	5	2	2	2	1	1	1	2	17-ch	Grade 1	TSSOP28

USCI*: supports UART, SPI or I^2C

3.2.2 NuMicro® M0A23U Selection Code

Core	Series	Package	Flash Size	SRAM Size	Revision	Temperature	Automotive Grade
M0	A23	O	C	1	A	C	U
Cortex®-M0	A23: with CAN	O: SSOP20 (5.3x7.2 mm) E: SSOP28 (4.4x9.7 mm)	C: 32 KB	1: 4 KB		C:-40˚C ~ 125˚C	U:AEC-Q100 qualified

4 PIN CONFIGURATION

The pin configuaration information can be found in the M0A23U Series Multi-function Summary Table section or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps configure GPIO multi-function pins correctly and handily.

4.1 Pin Configuration

4.1.1 M0A23U Series Pin Diagram

4.1.1.1 SSOP20 Package

Corresponding Part Number: M0A23OC1ACU

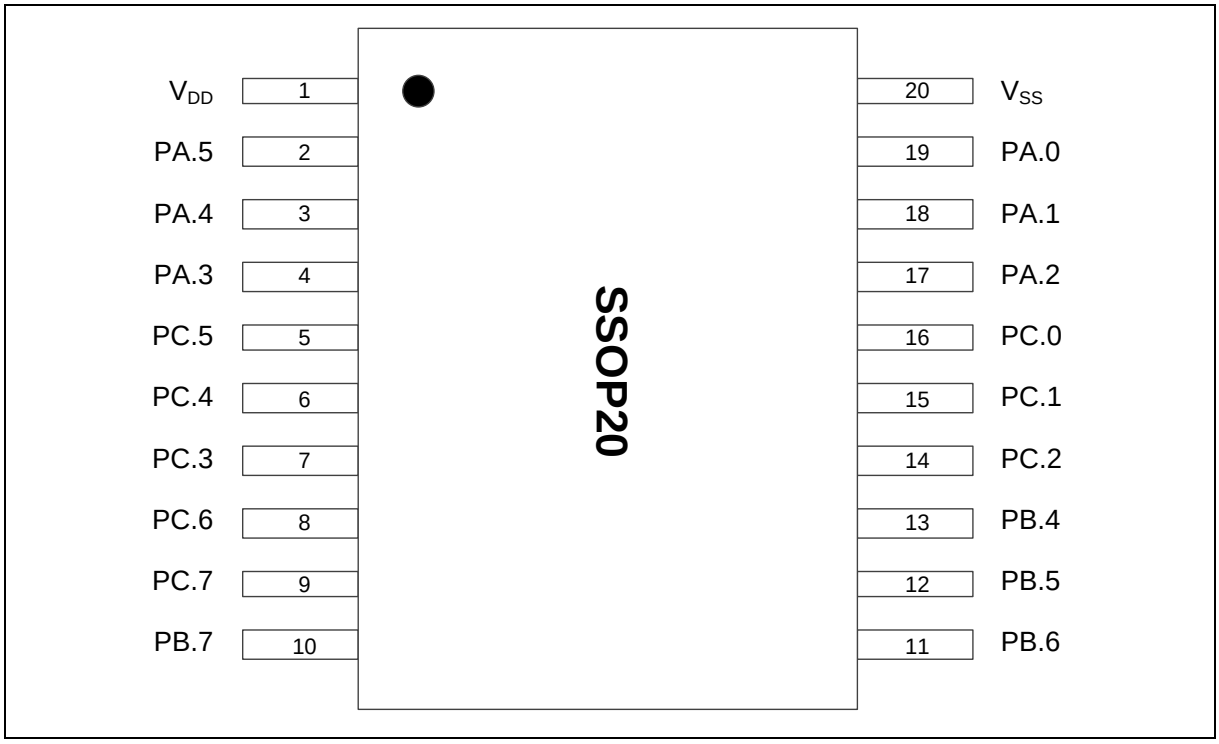


Figure 4.1-1 M0A23U Series SSOP 20-pin Diagram

4.1.1.2 TSSOP28 Package

Corresponding Part Number: M0A23EC1ACU.

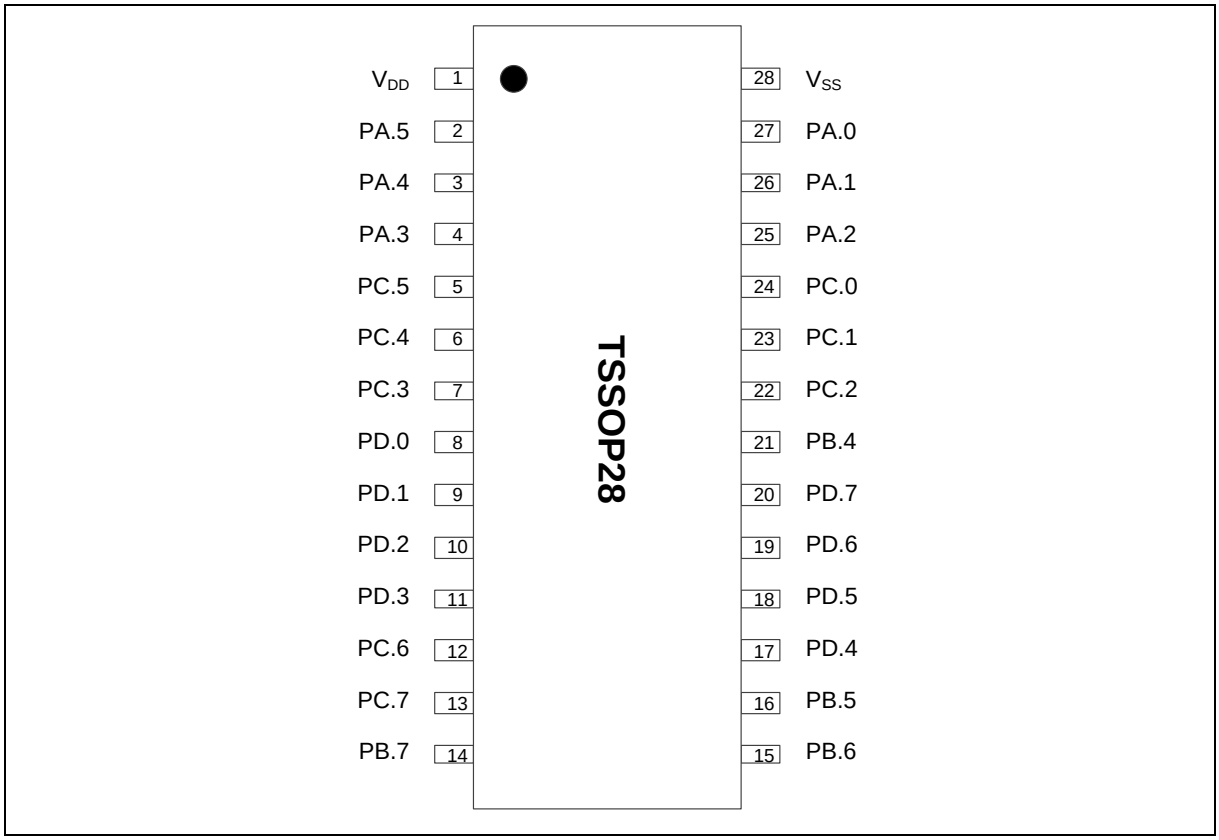


Figure 4.1-2 M0A23U Series TSSOP 28-pin Diagram

4.1.2 M0A23U Series Function Pin Table

4.1.2.1 SSOP20 Package

Corresponding Part Number: M0A23OC1ACU.

M0A23OC1ACU Multi-function Pin Table

Pin	M0A23OC1ACU Pin Function
1	V_{DD}
2	PA.5 / ADC0_CH16 / UART0_nRTS / XT1_IN / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / ACMP0_WLAT
3	PA.4 / ADC0_CH15 / UART0_nRTS / XT1_OUT / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / ACMP1_WLAT
4	PA.3 / nRESET / UART0_nCTS / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_RXD / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_RXD / INT0
5	PC.5 / ADC0_CH14 / X32_IN / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT1
6	PC.4 / ADC0_CH13 / X32_OUT / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT2
7	PC.3 / ADC0_CH12 / ACMP0_N3 / ACMP1_N3 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT3
8	PC.6 / ADC0_CH11 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT4
9	PC.7 / ADC0_CH10 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT5
10	PB.7 / ADC0_CH9 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / ACMP0_WLAT
11	PB.6 / ADC0_CH8 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / ACMP1_WLAT
12	PB.5 / ADC0_CH7 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O /

Pin	M0A23OC1ACU Pin Function
	ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT0
13	PB.4 / ADC0_CH6 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / UART1_nCTS
14	PC.2 / ADC0_CH5 / ACMP0_N2 / ACMP1_N2 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / UART1_nRTS
15	PC.1 / ADC0_CH4 / ACMP0_N1 / ACMP1_N1 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD
16	PC.0 / ADC0_CH3 / ACMP1_P0 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE0
17	PA.2 / ADC0_CH2 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE1
18	PA.1 / ADC0_CH1 / ACMP0_N0 / ACMP1_N0 / VREF+ / ICE_CLK / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE0
19	PA.0 / ADC0_CH0 / DAC0_OUT / ACMP0_P0 / ICE_DAT / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE1
20	V_{SS}

4.1.2.2 TSSOP28 Package

Corresponding Part Number: M0A23EC1ACU.

M0A23EC1ACU Multi-function Pin Table

Pin	M0A23EC1ACU Pin Function
1	V_{DD}
2	PA.5 / ADC0_CH16 / UART0_nRTS / XT1_IN / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / ACMP0_WLAT
3	PA.4 / ADC0_CH15 / UART0_nRTS / XT1_OUT / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 /

Pin	M0A23EC1ACU Pin Function
	USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / ACMP1_WLAT
4	PA.3 / nRESET / UART0_nCTS / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_RXD / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_RXD / INT0
5	PC.5 / ADC0_CH14 / X32_IN / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT1
6	PC.4 / ADC0_CH13 / X32_OUT / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT2
7	PC.3 / ADC0_CH12 / ACMP0_N3 / ACMP1_N3 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT3
8	PD.0 / PWM0_CH4 / UART0_TXD / USCI1_CLK / TM0
9	PD.1 / PWM0_CH5 / UART0_RXD / USCI1_DAT0 / TM1
10	PD.2 / PWM0_CH0 / USCI1_DAT1 / TM2 / UART1_nCTS
11	PD.3 / PWM0_CH1 / USCI1_CTL0 / TM3 / UART1_nRTS
12	PC.6 / ADC0_CH11 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT4
13	PC.7 / ADC0_CH10 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / INT5
14	PB.7 / ADC0_CH9 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / ACMP0_WLAT
15	PB.6 / ADC0_CH8 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / ACMP1_WLAT
16	PB.5 / ADC0_CH7 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / INT0
17	PD.4 / PWM0_CH0 / UART0_TXD / USCI0_CLK / TM0
18	PD.5 / PWM0_CH1 / UART0_RXD / USCI0_DAT0 / TM1
19	PD.6 / PWM0_CH2 / USCI0_DAT1 / TM2 / UART1_nCTS

Pin	M0A23EC1ACU Pin Function
20	PD.7 / PWM0_CH3 / USCI0_CTL0 / TM3 / UART1_nRTS
21	PB.4 / ADC0_CH6 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / UART1_nCTS
22	PC.2 / ADC0_CH5 / ACMP0_N2 / ACMP1_N2 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / UART1_nRTS
23	PC.1 / ADC0_CH4 / ACMP0_N1 / ACMP1_N1 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD
24	PC.0 / ADC0_CH3 / ACMP1_P0 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE0
25	PA.2 / ADC0_CH2 / UART0_nRTS / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE1
26	PA.1 / ADC0_CH1 / ACMP0_N0 / ACMP1_N0 / VREF+ / ICE_CLK / UART0_nCTS / CLKO / PWM0_CH0 / PWM0_CH2 / PWM0_CH4 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI1_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM0 / TM2 / TM0_EXT / TM2_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE0
27	PA.0 / ADC0_CH0 / DAC0_OUT / ACMP0_P0 / ICE_DAT / UART0_nCTS / CLKO / PWM0_CH1 / PWM0_CH3 / PWM0_CH5 / UART0_TXD / UART0_RXD / USCI0_CLK / USCI0_DAT0 / USCI0_DAT1 / USCI0_CTL0 / USCI0_CTL1 / USCI1_CLK / USCI1_DAT0 / USCI1_DAT1 / USCI1_CTL0 / CAN0_TXD / CAN0_RXD / ACMP0_O / ACMP1_O / ADC0_ST / TM1 / TM3 / TM1_EXT / TM3_EXT / UART1_TXD / UART1_RXD / PWM0_BRAKE1
28	V_{SS}

4.2 Pin Description

Different part number with same package might have different functions. Please refer to the selection guide in section 3.2.

4.2.1 M0A23U Series Pin Description

20 Pin	28 Pin	Pin Name	Type	MFP	Description
1	1	V_{DD}	P	MFP0	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
2	2	PA.5	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH16	A	MFP1	ADC0 channel 16 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		XT1_IN	I	MFP3	External 4~24 MHz (high speed) crystal input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		ACMP0_WLAT	I	MFP30	Analog comparator 0 window latch input pin
3	3	PA.4	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		XT1_OUT	O	MFP3	External 4~24 MHz (high speed) crystal output pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		ACMP1_WLAT	I	MFP30	Analog comparator 1 window latch input pin

20 Pin	28 Pin	Pin Name	Type	MFP	Description
4	4	PA.3	I	MFP0	General purpose digital input pin.
		nRESET	I	MFP2	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		PWM0_CH0	I	MFP5	PWM0 channel 0 capture input.
		PWM0_CH2	I	MFP6	PWM0 channel 2 capture input.
		PWM0_CH4	I	MFP7	PWM0 channel 4 capture input.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I	MFP10	USCI0 clock pin.
		USCI0_DAT0	I	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I	MFP15	USCI1 clock pin.
		USCI1_DAT0	I	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I	MFP18	USCI1 control 0 pin.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I	MFP24	Timer0 event counter input pin.
		TM2	I	MFP25	Timer2 event counter input pin.
		TM0_EXT	I	MFP26	Timer0 external capture input pin.
		TM2_EXT	I	MFP27	Timer2 external capture input pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT0	I	MFP30	External interrupt 0 input pin.
5	5	PC.5	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.
		X32_IN	I	MFP2	External 32.768 kHz crystal input pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT1	I	MFP30	External interrupt 1 input pin.
6	6	PC.4	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
		X32_OUT	O	MFP2	External 32.768 kHz crystal output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT2	I	MFP30	External interrupt 2 input pin.
7	7	PC.3	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
		ACMP0_N3	A	MFP1	Analog comparator 0 negative input 3 pin.
		ACMP1_N3	A	MFP1	Analog comparator 1 negative input 3 pin.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT3	I	MFP30	External interrupt 3 input pin.
	8	PD.0	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH4	I/O	MFP2	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP3	UART0 data transmitter output pin.
		USCI1_CLK	I/O	MFP4	USCI1 clock pin.
		TM0	I/O	MFP5	Timer0 event counter input/toggle output pin.
	9	PD.1	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH5	I/O	MFP2	PWM0 channel 5 output/capture input.
		UART0_RXD	I	MFP3	UART0 data receiver input pin.
		USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
		TM1	I/O	MFP5	Timer1 event counter input/toggle output pin.
	10	PD.2	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH0	I/O	MFP2	PWM0 channel 0 output/capture input.
		CAN0_TXD	O	MFP3	CAN0 bus transmitter output.
		USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
		TM2	I/O	MFP5	Timer2 event counter input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	11	PD.3	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH1	I/O	MFP2	PWM0 channel 1 output/capture input.
		CAN0_RXD	I	MFP3	CAN0 bus receiver input.
		USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
		TM3	I/O	MFP5	Timer3 event counter input/toggle output pin.
		UART1_nRTS	O	MFP6	UART1 request to Send output pin.
8	12	PC.6	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT4	I	MFP30	External interrupt 4 input pin.
9	13	PC.7	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		INT5	I	MFP30	External interrupt 5 input pin.
10	14	PB.7	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		ACMP0_WLAT	I	MFP30	Analog comparator 0 window latch input pin
11	15	PB.6	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		ACMP1_WLAT	I	MFP30	Analog comparator 1 window latch input pin
12	16	PB.5	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		INT0	I	MFP30	External interrupt 0 input pin.
	17	PD.4	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH0	I/O	MFP2	PWM0 channel 0 output/capture input.
		UART0_TXD	O	MFP3	UART0 data transmitter output pin.
		USCI0_CLK	I/O	MFP4	USCI0 clock pin.
		TM0	I/O	MFP5	Timer0 event counter input/toggle output pin.
	18	PD.5	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH1	I/O	MFP2	PWM0 channel 1 output/capture input.
		UART0_RXD	I	MFP3	UART0 data receiver input pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.
		TM1	I/O	MFP5	Timer1 event counter input/toggle output pin.
	19	PD.6	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH2	I/O	MFP2	PWM0 channel 2 output/capture input.
		CAN0_TXD	O	MFP3	CAN0 bus transmitter output.
		USCI0_DAT1	I/O	MFP4	USCI0 data 1 pin.
		TM2	I/O	MFP5	Timer2 event counter input/toggle output pin.
		UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
	20	PD.7	I/O	MFP0	General purpose digital I/O pin.
		PWM0_CH3	I/O	MFP2	PWM0 channel 3 output/capture input.
		CAN0_RXD	I	MFP3	CAN0 bus receiver input.
		USCI0_CTL0	I/O	MFP4	USCI0 control 0 pin.
		TM3	I/O	MFP5	Timer3 event counter input/toggle output pin.
		UART1_nRTS	O	MFP6	UART1 request to Send output pin.
13	21	PB.4	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		UART1_nCTS	I	MFP30	UART1 clear to Send input pin.
14	22	PC.2	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
		ACMP0_N2	A	MFP1	Analog comparator 0 negative input 2 pin.
		ACMP1_N2	A	MFP1	Analog comparator 1 negative input 2 pin.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		UART1_nRTS	O	MFP30	UART1 request to Send output pin.
15	23	PC.1	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
		ACMP0_N1	A	MFP1	Analog comparator 0 negative input 1 pin.
		ACMP1_N1	A	MFP1	Analog comparator 1 negative input 1 pin.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
16	24	PC.0	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
		ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		PWM0_BRAKE0	I	MFP30	PWM0 Brake 0 input pin.
17	25	PA.2	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
		UART0_nRTS	O	MFP2	UART0 request to Send output pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		PWM0_BRAKE1	I	MFP30	PWM0 Brake 1 input pin.
18	26	PA.1	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
		ACMP0_N0	A	MFP1	Analog comparator 0 negative input 0 pin.
		ACMP1_N0	A	MFP1	Analog comparator 1 negative input 0 pin.
		V_{REF}	A	MFP1	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
		ICE_CLK	I	MFP2	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
		PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
		PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
		TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
		TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		PWM0_BRAKE0	I	MFP30	PWM0 Brake 0 input pin.
19	27	PA.0	I/O	MFP0	General purpose digital I/O pin.
		ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
		DAC0_OUT	A	MFP1	DAC0 channel analog output.
		ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
		ICE_DAT	I/O	MFP2	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
		UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
		CLKO	O	MFP4	Clock Out
		PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
		PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
		PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
		UART0_TXD	O	MFP8	UART0 data transmitter output pin.
		UART0_RXD	I	MFP9	UART0 data receiver input pin.
		USCI0_CLK	I/O	MFP10	USCI0 clock pin.
		USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
		USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
		USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
		USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
		USCI1_CLK	I/O	MFP15	USCI1 clock pin.
		USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
		USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
		USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
		CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
		CAN0_RXD	I	MFP20	CAN0 bus receiver input.
		ACMP0_O	O	MFP21	Analog comparator 0 output pin.
		ACMP1_O	O	MFP22	Analog comparator 1 output pin.
		ADC0_ST	I	MFP23	ADC0 external trigger input pin.
		TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
		TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.

20 Pin	28 Pin	Pin Name	Type	MFP	Description
		TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
		TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
		UART1_TXD	O	MFP28	UART1 data transmitter output pin.
		UART1_RXD	I	MFP29	UART1 data receiver input pin.
		PWM0_BRAKE1	I	MFP30	PWM0 Brake 1 input pin.
20	28	V_{SS}	P	MFP0	Ground pin for digital circuit.

4.2.2 M0A23U Series Multi-function Summary Table

Group	Pin Name	GPIO	MFP	Type	Description
ACMP0	ACMP0_N0	PA.1	MFP1	A	Analog comparator 0 negative input 0 pin.
	ACMP0_N1	PC.1	MFP1	A	Analog comparator 0 negative input 1 pin.
	ACMP0_N2	PC.2	MFP1	A	Analog comparator 0 negative input 2 pin.
	ACMP0_N3	PC.3	MFP1	A	Analog comparator 0 negative input 3 pin.
	ACMP0_O	PA.5	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PA.4	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.5	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.4	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.3	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.6	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.7	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PB.7	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PB.6	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PB.5	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PB.4	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.2	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.1	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PC.0	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PA.2	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PA.1	MFP21	O	Analog comparator 0 output pin.
	ACMP0_O	PA.0	MFP21	O	Analog comparator 0 output pin.
	ACMP0_P0	PA.0	MFP1	A	Analog comparator 0 positive input 0 pin.
	ACMP0_WLAT	PA.5	MFP30	I	Analog comparator 0 window latch input pin
	ACMP0_WLAT	PB.7	MFP30	I	Analog comparator 0 window latch input pin

Group	Pin Name	GPIO	MFP	Type	Description
ACMP1	ACMP1_N0	PA.1	MFP1	A	Analog comparator 1 negative input 0 pin.
	ACMP1_N1	PC.1	MFP1	A	Analog comparator 1 negative input 1 pin.
	ACMP1_N2	PC.2	MFP1	A	Analog comparator 1 negative input 2 pin.
	ACMP1_N3	PC.3	MFP1	A	Analog comparator 1 negative input 3 pin.
	ACMP1_O	PA.5	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PA.4	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.5	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.4	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.3	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.6	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.7	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PB.7	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PB.6	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PB.5	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PB.4	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.2	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.1	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PC.0	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PA.2	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PA.1	MFP22	O	Analog comparator 1 output pin.
	ACMP1_O	PA.0	MFP22	O	Analog comparator 1 output pin.
	ACMP1_P0	PC.0	MFP1	A	Analog comparator 1 positive input 0 pin.
	ACMP1_WLAT	PA.4	MFP30	I	Analog comparator 1 window latch input pin
	ACMP1_WLAT	PB.6	MFP30	I	Analog comparator 1 window latch input pin
ADC0	ADC0_CH0	PA.0	MFP1	A	ADC0 channel 0 analog input.
	ADC0_CH1	PA.1	MFP1	A	ADC0 channel 1 analog input.
	ADC0_CH10	PC.7	MFP1	A	ADC0 channel 10 analog input.
	ADC0_CH11	PC.6	MFP1	A	ADC0 channel 11 analog input.
	ADC0_CH12	PC.3	MFP1	A	ADC0 channel 12 analog input.
	ADC0_CH13	PC.4	MFP1	A	ADC0 channel 13 analog input.
	ADC0_CH14	PC.5	MFP1	A	ADC0 channel 14 analog input.
	ADC0_CH15	PA.4	MFP1	A	ADC0 channel 15 analog input.
	ADC0_CH16	PA.5	MFP1	A	ADC0 channel 16 analog input.
	ADC0_CH2	PA.2	MFP1	A	ADC0 channel 2 analog input.

Group	Pin Name	GPIO	MFP	Type	Description
	ADC0_CH3	PC.0	MFP1	A	ADC0 channel 3 analog input.
	ADC0_CH4	PC.1	MFP1	A	ADC0 channel 4 analog input.
	ADC0_CH5	PC.2	MFP1	A	ADC0 channel 5 analog input.
	ADC0_CH6	PB.4	MFP1	A	ADC0 channel 6 analog input.
	ADC0_CH7	PB.5	MFP1	A	ADC0 channel 7 analog input.
	ADC0_CH8	PB.6	MFP1	A	ADC0 channel 8 analog input.
	ADC0_CH9	PB.7	MFP1	A	ADC0 channel 9 analog input.
	ADC0_ST	PA.5	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PA.4	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PA.3	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.5	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.4	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.3	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.6	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.7	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PB.7	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PB.6	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PB.5	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PB.4	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.2	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.1	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PC.0	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PA.2	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PA.1	MFP23	I	ADC0 external trigger input pin.
	ADC0_ST	PA.0	MFP23	I	ADC0 external trigger input pin.
CAN0	CAN0_RXD	PA.5	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PA.4	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PA.3	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.5	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.4	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.3	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PD.3	MFP3	I	CAN0 bus receiver input.
	CAN0_RXD	PC.6	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.7	MFP20	I	CAN0 bus receiver input.

Group	Pin Name	GPIO	MFP	Type	Description
	CAN0_RXD	PB.7	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PB.6	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PB.5	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PD.7	MFP3	I	CAN0 bus receiver input.
	CAN0_RXD	PB.4	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.2	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.1	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PC.0	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PA.2	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PA.1	MFP20	I	CAN0 bus receiver input.
	CAN0_RXD	PA.0	MFP20	I	CAN0 bus receiver input.
	CAN0_TXD	PA.5	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PA.4	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.5	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.4	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.3	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PD.2	MFP3	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.6	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.7	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PB.7	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PB.6	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PB.5	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PD.6	MFP3	O	CAN0 bus transmitter output.
	CAN0_TXD	PB.4	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.2	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.1	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PC.0	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PA.2	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PA.1	MFP19	O	CAN0 bus transmitter output.
	CAN0_TXD	PA.0	MFP19	O	CAN0 bus transmitter output.
CLKO	CLKO	PA.5	MFP4	O	Clock Out
	CLKO	PA.4	MFP4	O	Clock Out
	CLKO	PC.5	MFP4	O	Clock Out
	CLKO	PC.4	MFP4	O	Clock Out

Group	Pin Name	GPIO	MFP	Type	Description
	CLKO	PC.3	MFP4	O	Clock Out
	CLKO	PC.6	MFP4	O	Clock Out
	CLKO	PC.7	MFP4	O	Clock Out
	CLKO	PB.7	MFP4	O	Clock Out
	CLKO	PB.6	MFP4	O	Clock Out
	CLKO	PB.5	MFP4	O	Clock Out
	CLKO	PB.4	MFP4	O	Clock Out
	CLKO	PC.2	MFP4	O	Clock Out
	CLKO	PC.1	MFP4	O	Clock Out
	CLKO	PC.0	MFP4	O	Clock Out
	CLKO	PA.2	MFP4	O	Clock Out
	CLKO	PA.1	MFP4	O	Clock Out
	CLKO	PA.0	MFP4	O	Clock Out
DAC0	DAC0_OUT	PA.0	MFP1	A	DAC0 channel analog output.
ICE	ICE_CLK	PA.1	MFP2	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	PA.0	MFP2	I/O	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	PA.3	MFP30	I	External interrupt 0 input pin.
	INT0	PB.5	MFP30	I	External interrupt 0 input pin.
INT1	INT1	PC.5	MFP30	I	External interrupt 1 input pin.
INT2	INT2	PC.4	MFP30	I	External interrupt 2 input pin.
INT3	INT3	PC.3	MFP30	I	External interrupt 3 input pin.
INT4	INT4	PC.6	MFP30	I	External interrupt 4 input pin.
INT5	INT5	PC.7	MFP30	I	External interrupt 5 input pin.
PWM0	PWM0_BRAKE0	PC.0	MFP30	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE0	PA.1	MFP30	I	PWM0 Brake 0 input pin.
	PWM0_BRAKE1	PA.2	MFP30	I	PWM0 Brake 1 input pin.
	PWM0_BRAKE1	PA.0	MFP30	I	PWM0 Brake 1 input pin.
	PWM0_CH0	PA.5	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PA.3	MFP5	I	PWM0 channel 0 capture input.
	PWM0_CH0	PC.4	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PD.2	MFP2	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PC.6	MFP5	I/O	PWM0 channel 0 output/capture input.

Group	Pin Name	GPIO	MFP	Type	Description
	PWM0_CH0	PB.7	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PB.5	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PD.4	MFP2	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PC.2	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PC.0	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH0	PA.1	MFP5	I/O	PWM0 channel 0 output/capture input.
	PWM0_CH1	PA.4	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PC.5	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PC.3	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PD.3	MFP2	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PC.7	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PB.6	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PD.5	MFP2	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PB.4	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PC.1	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PA.2	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH1	PA.0	MFP5	I/O	PWM0 channel 1 output/capture input.
	PWM0_CH2	PA.5	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PA.3	MFP6	I	PWM0 channel 2 capture input.
	PWM0_CH2	PC.4	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PC.6	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PB.7	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PB.5	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PD.6	MFP2	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PC.2	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PC.0	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH2	PA.1	MFP6	I/O	PWM0 channel 2 output/capture input.
	PWM0_CH3	PA.4	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PC.5	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PC.3	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PC.7	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PB.6	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PD.7	MFP2	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PB.4	MFP6	I/O	PWM0 channel 3 output/capture input.

Group	Pin Name	GPIO	MFP	Type	Description
	PWM0_CH3	PC.1	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PA.2	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH3	PA.0	MFP6	I/O	PWM0 channel 3 output/capture input.
	PWM0_CH4	PA.5	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PA.3	MFP7	I	PWM0 channel 4 capture input.
	PWM0_CH4	PC.4	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PD.0	MFP2	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PC.6	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PB.7	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PB.5	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PC.2	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PC.0	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH4	PA.1	MFP7	I/O	PWM0 channel 4 output/capture input.
	PWM0_CH5	PA.4	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PC.5	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PC.3	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PD.1	MFP2	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PC.7	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PB.6	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PB.4	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PC.1	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PA.2	MFP7	I/O	PWM0 channel 5 output/capture input.
	PWM0_CH5	PA.0	MFP7	I/O	PWM0 channel 5 output/capture input.
TM0	TM0	PA.5	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PA.3	MFP24	I	Timer0 event counter input pin.
	TM0	PC.4	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PD.0	MFP5	I/O	Timer0 event counter input/toggle output pin.
	TM0	PC.6	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PB.7	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PB.5	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PD.4	MFP5	I/O	Timer0 event counter input/toggle output pin.
	TM0	PC.2	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PC.0	MFP24	I/O	Timer0 event counter input/toggle output pin.
	TM0	PA.1	MFP24	I/O	Timer0 event counter input/toggle output pin.

Group	Pin Name	GPIO	MFP	Type	Description
TM1	TM1	PA.4	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PC.5	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PC.3	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PD.1	MFP5	I/O	Timer1 event counter input/toggle output pin.
	TM1	PC.7	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PB.6	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PD.5	MFP5	I/O	Timer1 event counter input/toggle output pin.
	TM1	PB.4	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PC.1	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PA.2	MFP24	I/O	Timer1 event counter input/toggle output pin.
	TM1	PA.0	MFP24	I/O	Timer1 event counter input/toggle output pin.
TM2	TM2	PA.5	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PA.3	MFP25	I	Timer2 event counter input pin.
	TM2	PC.4	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PD.2	MFP5	I/O	Timer2 event counter input/toggle output pin.
	TM2	PC.6	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PB.7	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PB.5	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PD.6	MFP5	I/O	Timer2 event counter input/toggle output pin.
	TM2	PC.2	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PC.0	MFP25	I/O	Timer2 event counter input/toggle output pin.
	TM2	PA.1	MFP25	I/O	Timer2 event counter input/toggle output pin.
TM3	TM3	PA.4	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PC.5	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PC.3	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PD.3	MFP5	I/O	Timer3 event counter input/toggle output pin.
	TM3	PC.7	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PB.6	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PD.7	MFP5	I/O	Timer3 event counter input/toggle output pin.
	TM3	PB.4	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PC.1	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PA.2	MFP25	I/O	Timer3 event counter input/toggle output pin.
	TM3	PA.0	MFP25	I/O	Timer3 event counter input/toggle output pin.
TM0	TM0_EXT	PA.5	MFP26	I/O	Timer0 external capture input/toggle output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	TM0_EXT	PA.3	MFP26	I	Timer0 external capture input pin.
	TM0_EXT	PC.4	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PC.6	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PB.7	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PB.5	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PC.2	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PC.0	MFP26	I/O	Timer0 external capture input/toggle output pin.
	TM0_EXT	PA.1	MFP26	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1_EXT	PA.4	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PC.5	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PC.3	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PC.7	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PB.6	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PB.4	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PC.1	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PA.2	MFP26	I/O	Timer1 external capture input/toggle output pin.
	TM1_EXT	PA.0	MFP26	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2_EXT	PA.5	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PA.3	MFP27	I	Timer2 external capture input pin.
	TM2_EXT	PC.4	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PC.6	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PB.7	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PB.5	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PC.2	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PC.0	MFP27	I/O	Timer2 external capture input/toggle output pin.
	TM2_EXT	PA.1	MFP27	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3_EXT	PA.4	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PC.5	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PC.3	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PC.7	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PB.6	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PB.4	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PC.1	MFP27	I/O	Timer3 external capture input/toggle output pin.
	TM3_EXT	PA.2	MFP27	I/O	Timer3 external capture input/toggle output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	TM3_EXT	PA.0	MFP27	I/O	Timer3 external capture input/toggle output pin.
UART0	UART0_RXD	PA.5	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PA.4	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PA.3	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.5	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.4	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.3	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PD.1	MFP3	I	UART0 data receiver input pin.
	UART0_RXD	PC.6	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.7	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PB.7	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PB.6	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PB.5	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PD.5	MFP3	I	UART0 data receiver input pin.
	UART0_RXD	PB.4	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.2	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.1	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PC.0	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PA.2	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PA.1	MFP9	I	UART0 data receiver input pin.
	UART0_RXD	PA.0	MFP9	I	UART0 data receiver input pin.
	UART0_TXD	PA.5	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PA.4	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.5	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.4	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.3	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PD.0	MFP3	O	UART0 data transmitter output pin.
	UART0_TXD	PC.6	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.7	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PB.7	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PB.6	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PB.5	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PD.4	MFP3	O	UART0 data transmitter output pin.
	UART0_TXD	PB.4	MFP8	O	UART0 data transmitter output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	UART0_TXD	PC.2	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.1	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PC.0	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PA.2	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PA.1	MFP8	O	UART0 data transmitter output pin.
	UART0_TXD	PA.0	MFP8	O	UART0 data transmitter output pin.
	UART0_nCTS	PA.3	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.5	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.4	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.3	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.6	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.7	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PB.7	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PB.6	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PB.5	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PB.4	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.2	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.1	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PC.0	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PA.2	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PA.1	MFP3	I	UART0 clear to Send input pin.
	UART0_nCTS	PA.0	MFP3	I	UART0 clear to Send input pin.
	UART0_nRTS	PA.5	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PA.4	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.3	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.6	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.7	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PB.7	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PB.6	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PB.5	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PB.4	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.2	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.1	MFP2	O	UART0 request to Send output pin.
	UART0_nRTS	PC.0	MFP2	O	UART0 request to Send output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	UART0_nRTS	PA.2	MFP2	O	UART0 request to Send output pin.
UART1	UART1_RXD	PA.5	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PA.4	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PA.3	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.5	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.4	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.3	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.6	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.7	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PB.7	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PB.6	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PB.5	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PB.4	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.2	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.1	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PC.0	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PA.2	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PA.1	MFP29	I	UART1 data receiver input pin.
	UART1_RXD	PA.0	MFP29	I	UART1 data receiver input pin.
	UART1_TXD	PA.5	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PA.4	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.5	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.4	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.3	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.6	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.7	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PB.7	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PB.6	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PB.5	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PB.4	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.2	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.1	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PC.0	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PA.2	MFP28	O	UART1 data transmitter output pin.

Group	Pin Name	GPIO	MFP	Type	Description
	UART1_TXD	PA.1	MFP28	O	UART1 data transmitter output pin.
	UART1_TXD	PA.0	MFP28	O	UART1 data transmitter output pin.
	UART1_nCTS	PD.2	MFP6	I	UART1 clear to Send input pin.
	UART1_nCTS	PD.6	MFP6	I	UART1 clear to Send input pin.
	UART1_nCTS	PB.4	MFP30	I	UART1 clear to Send input pin.
	UART1_nRTS	PD.3	MFP6	O	UART1 request to Send output pin.
	UART1_nRTS	PD.7	MFP6	O	UART1 request to Send output pin.
	UART1_nRTS	PC.2	MFP30	O	UART1 request to Send output pin.
USCI0	USCI0_CLK	PA.5	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PA.4	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PA.3	MFP10	I	USCI0 clock pin.
	USCI0_CLK	PC.5	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.4	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.3	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.6	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.7	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PB.7	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PB.6	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PB.5	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PD.4	MFP4	I/O	USCI0 clock pin.
	USCI0_CLK	PB.4	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.2	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.1	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PC.0	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PA.2	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PA.1	MFP10	I/O	USCI0 clock pin.
	USCI0_CLK	PA.0	MFP10	I/O	USCI0 clock pin.
	USCI0_CTL0	PA.5	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PA.4	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PA.3	MFP13	I	USCI0 control 0 pin.
	USCI0_CTL0	PC.5	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.4	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.3	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.6	MFP13	I/O	USCI0 control 0 pin.

Group	Pin Name	GPIO	MFP	Type	Description
	USCI0_CTL0	PC.7	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PB.7	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PB.6	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PB.5	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PD.7	MFP4	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PB.4	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.2	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.1	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PC.0	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PA.2	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PA.1	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL0	PA.0	MFP13	I/O	USCI0 control 0 pin.
	USCI0_CTL1	PA.5	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PA.3	MFP14	I	USCI0 control 1 pin.
	USCI0_CTL1	PC.5	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PC.3	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PC.7	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PB.6	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PB.4	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PC.1	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PA.2	MFP14	I/O	USCI0 control 1 pin.
	USCI0_CTL1	PA.0	MFP14	I/O	USCI0 control 1 pin.
	USCI0_DAT0	PA.5	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PA.4	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PA.3	MFP11	I	USCI0 data 0 pin.
	USCI0_DAT0	PC.5	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.4	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.3	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.6	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.7	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PB.7	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PB.6	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PB.5	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PD.5	MFP4	I/O	USCI0 data 0 pin.

Group	Pin Name	GPIO	MFP	Type	Description
	USCI0_DAT0	PB.4	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.2	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.1	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PC.0	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PA.2	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PA.1	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT0	PA.0	MFP11	I/O	USCI0 data 0 pin.
	USCI0_DAT1	PA.5	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PA.4	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PA.3	MFP12	I	USCI0 data 1 pin.
	USCI0_DAT1	PC.5	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.4	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.3	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.6	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.7	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PB.7	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PB.6	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PB.5	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PD.6	MFP4	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PB.4	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.2	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.1	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PC.0	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PA.2	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PA.1	MFP12	I/O	USCI0 data 1 pin.
	USCI0_DAT1	PA.0	MFP12	I/O	USCI0 data 1 pin.
USCI1	USCI1_CLK	PA.5	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PA.4	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PA.3	MFP15	I	USCI1 clock pin.
	USCI1_CLK	PC.5	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PC.4	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PC.3	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PD.0	MFP4	I/O	USCI1 clock pin.
	USCI1_CLK	PC.6	MFP15	I/O	USCI1 clock pin.

Group	Pin Name	GPIO	MFP	Type	Description
	USCI1_CLK	PC.7	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PB.7	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PB.6	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PB.5	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PB.4	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PC.2	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PC.1	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PC.0	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PA.2	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PA.1	MFP15	I/O	USCI1 clock pin.
	USCI1_CLK	PA.0	MFP15	I/O	USCI1 clock pin.
	USCI1_CTL0	PA.5	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PA.4	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PA.3	MFP18	I	USCI1 control 0 pin.
	USCI1_CTL0	PC.5	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.4	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.3	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PD.3	MFP4	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.6	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.7	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PB.7	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PB.6	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PB.5	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PB.4	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.2	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.1	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PC.0	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PA.2	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PA.1	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL0	PA.0	MFP18	I/O	USCI1 control 0 pin.
	USCI1_CTL1	PA.4	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PC.4	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PC.6	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PB.7	MFP14	I/O	USCI1 control 1 pin.

Group	Pin Name	GPIO	MFP	Type	Description
	USCI1_CTL1	PB.5	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PC.2	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PC.0	MFP14	I/O	USCI1 control 1 pin.
	USCI1_CTL1	PA.1	MFP14	I/O	USCI1 control 1 pin.
	USCI1_DAT0	PA.5	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PA.4	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PA.3	MFP16	I	USCI1 data 0 pin.
	USCI1_DAT0	PC.5	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.4	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.3	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PD.1	MFP4	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.6	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.7	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PB.7	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PB.6	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PB.5	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PB.4	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.2	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.1	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PC.0	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PA.2	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PA.1	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT0	PA.0	MFP16	I/O	USCI1 data 0 pin.
	USCI1_DAT1	PA.5	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PA.4	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PA.3	MFP17	I	USCI1 data 1 pin.
	USCI1_DAT1	PC.5	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.4	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.3	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PD.2	MFP4	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.6	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.7	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PB.7	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PB.6	MFP17	I/O	USCI1 data 1 pin.

Group	Pin Name	GPIO	MFP	Type	Description
	USCI1_DAT1	PB.5	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PB.4	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.2	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.1	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PC.0	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PA.2	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PA.1	MFP17	I/O	USCI1 data 1 pin.
	USCI1_DAT1	PA.0	MFP17	I/O	USCI1 data 1 pin.
V_{REF}	V_{REF}	PA.1	MFP1	A	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
X32	X32_IN	PC.5	MFP2	I	External 32.768 kHz crystal input pin.
	X32_OUT	PC.4	MFP2	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	PA.5	MFP3	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	PA.4	MFP3	O	External 4~24 MHz (high speed) crystal output pin.
nRESET	nRESET	PA.3	MFP2	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

4.2.3 M0A23U Series Multi-function Summary Table Sorted by GPIO

	Pin Name	Type	MFP	Description
PA.0	PA.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH0	A	MFP1	ADC0 channel 0 analog input.
	DAC0_OUT	A	MFP1	DAC0 channel analog output.
	ACMP0_P0	A	MFP1	Analog comparator 0 positive input 0 pin.
	ICE_DAT	I/O	MFP2	Serial wired debugger data pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.

	Pin Name	Type	MFP	Description
	PWM0_BRAKE1	I	MFP30	PWM0 Brake 1 input pin.
PA.1	PA.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH1	A	MFP1	ADC0 channel 1 analog input.
	ACMP0_N0	A	MFP1	Analog comparator 0 negative input 0 pin.
	ACMP1_N0	A	MFP1	Analog comparator 1 negative input 0 pin.
	V_{REF}	A	MFP1	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
	ICE_CLK	I	MFP2	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.

	Pin Name	Type	MFP	Description
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	PWM0_BRAKE0	I	MFP30	PWM0 Brake 0 input pin.
PA.2	PA.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH2	A	MFP1	ADC0 channel 2 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	PWM0_BRAKE1	I	MFP30	PWM0 Brake 1 input pin.

	Pin Name	Type	MFP	Description
PA.3	PA.3	I	MFP0	General purpose digital input pin.
	nRESET	I	MFP2	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	PWM0_CH0	I	MFP5	PWM0 channel 0 capture input.
	PWM0_CH2	I	MFP6	PWM0 channel 2 capture input.
	PWM0_CH4	I	MFP7	PWM0 channel 4 capture input.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I	MFP10	USCI0 clock pin.
	USCI0_DAT0	I	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I	MFP15	USCI1 clock pin.
	USCI1_DAT0	I	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I	MFP18	USCI1 control 0 pin.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I	MFP24	Timer0 event counter input pin.
	TM2	I	MFP25	Timer2 event counter input pin.
	TM0_EXT	I	MFP26	Timer0 external capture input pin.
	TM2_EXT	I	MFP27	Timer2 external capture input pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT0	I	MFP30	External interrupt 0 input pin.
PA.4	PA.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH15	A	MFP1	ADC0 channel 15 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	XT1_OUT	O	MFP3	External 4~24 MHz (high speed) crystal output pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.

	Pin Name	Type	MFP	Description
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	ACMP1_WLAT	I	MFP30	Analog comparator 1 window latch input pin
PA.5	PA.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH16	A	MFP1	ADC0 channel 16 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	XT1_IN	I	MFP3	External 4~24 MHz (high speed) crystal input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.

	Pin Name	Type	MFP	Description
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	ACMP0_WLAT	I	MFP30	Analog comparator 0 window latch input pin
PB.4	PB.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH6	A	MFP1	ADC0 channel 6 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.

	Pin Name	Type	MFP	Description
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	UART1_nCTS	I	MFP30	UART1 clear to Send input pin.
PB.5	PB.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH7	A	MFP1	ADC0 channel 7 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.

	Pin Name	Type	MFP	Description
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT0	I	MFP30	External interrupt 0 input pin.
PB.6	PB.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH8	A	MFP1	ADC0 channel 8 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.

	Pin Name	Type	MFP	Description
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	ACMP1_WLAT	I	MFP30	Analog comparator 1 window latch input pin
PB.7	PB.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH9	A	MFP1	ADC0 channel 9 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.

	Pin Name	Type	MFP	Description
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	ACMP0_WLAT	I	MFP30	Analog comparator 0 window latch input pin
PC.0	PC.0	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH3	A	MFP1	ADC0 channel 3 analog input.
	ACMP1_P0	A	MFP1	Analog comparator 1 positive input 0 pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.

	Pin Name	Type	MFP	Description
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	PWM0_BRAKE0	I	MFP30	PWM0 Brake 0 input pin.
PC.1	PC.1	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH4	A	MFP1	ADC0 channel 4 analog input.
	ACMP0_N1	A	MFP1	Analog comparator 0 negative input 1 pin.
	ACMP1_N1	A	MFP1	Analog comparator 1 negative input 1 pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.

	Pin Name	Type	MFP	Description
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
PC.2	PC.2	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH5	A	MFP1	ADC0 channel 5 analog input.
	ACMP0_N2	A	MFP1	Analog comparator 0 negative input 2 pin.
	ACMP1_N2	A	MFP1	Analog comparator 1 negative input 2 pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.

	Pin Name	Type	MFP	Description
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	UART1_nRTS	O	MFP30	UART1 request to Send output pin.
PC.3	PC.3	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH12	A	MFP1	ADC0 channel 12 analog input.
	ACMP0_N3	A	MFP1	Analog comparator 0 negative input 3 pin.
	ACMP1_N3	A	MFP1	Analog comparator 1 negative input 3 pin.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.

	Pin Name	Type	MFP	Description
	INT3	I	MFP30	External interrupt 3 input pin.
PC.4	PC.4	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH13	A	MFP1	ADC0 channel 13 analog input.
	X32_OUT	O	MFP2	External 32.768 kHz crystal output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT2	I	MFP30	External interrupt 2 input pin.
PC.5	PC.5	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH14	A	MFP1	ADC0 channel 14 analog input.

	Pin Name	Type	MFP	Description
	X32_IN	I	MFP2	External 32.768 kHz crystal input pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT1	I	MFP30	External interrupt 1 input pin.
PC.6	PC.6	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH11	A	MFP1	ADC0 channel 11 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out

	Pin Name	Type	MFP	Description
	PWM0_CH0	I/O	MFP5	PWM0 channel 0 output/capture input.
	PWM0_CH2	I/O	MFP6	PWM0 channel 2 output/capture input.
	PWM0_CH4	I/O	MFP7	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI1_CTL1	I/O	MFP14	USCI1 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM0	I/O	MFP24	Timer0 event counter input/toggle output pin.
	TM2	I/O	MFP25	Timer2 event counter input/toggle output pin.
	TM0_EXT	I/O	MFP26	Timer0 external capture input/toggle output pin.
	TM2_EXT	I/O	MFP27	Timer2 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT4	I	MFP30	External interrupt 4 input pin.
PC.7	PC.7	I/O	MFP0	General purpose digital I/O pin.
	ADC0_CH10	A	MFP1	ADC0 channel 10 analog input.
	UART0_nRTS	O	MFP2	UART0 request to Send output pin.
	UART0_nCTS	I	MFP3	UART0 clear to Send input pin.
	CLKO	O	MFP4	Clock Out
	PWM0_CH1	I/O	MFP5	PWM0 channel 1 output/capture input.
	PWM0_CH3	I/O	MFP6	PWM0 channel 3 output/capture input.
	PWM0_CH5	I/O	MFP7	PWM0 channel 5 output/capture input.

	Pin Name	Type	MFP	Description
	UART0_TXD	O	MFP8	UART0 data transmitter output pin.
	UART0_RXD	I	MFP9	UART0 data receiver input pin.
	USCI0_CLK	I/O	MFP10	USCI0 clock pin.
	USCI0_DAT0	I/O	MFP11	USCI0 data 0 pin.
	USCI0_DAT1	I/O	MFP12	USCI0 data 1 pin.
	USCI0_CTL0	I/O	MFP13	USCI0 control 0 pin.
	USCI0_CTL1	I/O	MFP14	USCI0 control 1 pin.
	USCI1_CLK	I/O	MFP15	USCI1 clock pin.
	USCI1_DAT0	I/O	MFP16	USCI1 data 0 pin.
	USCI1_DAT1	I/O	MFP17	USCI1 data 1 pin.
	USCI1_CTL0	I/O	MFP18	USCI1 control 0 pin.
	CAN0_TXD	O	MFP19	CAN0 bus transmitter output.
	CAN0_RXD	I	MFP20	CAN0 bus receiver input.
	ACMP0_O	O	MFP21	Analog comparator 0 output pin.
	ACMP1_O	O	MFP22	Analog comparator 1 output pin.
	ADC0_ST	I	MFP23	ADC0 external trigger input pin.
	TM1	I/O	MFP24	Timer1 event counter input/toggle output pin.
	TM3	I/O	MFP25	Timer3 event counter input/toggle output pin.
	TM1_EXT	I/O	MFP26	Timer1 external capture input/toggle output pin.
	TM3_EXT	I/O	MFP27	Timer3 external capture input/toggle output pin.
	UART1_TXD	O	MFP28	UART1 data transmitter output pin.
	UART1_RXD	I	MFP29	UART1 data receiver input pin.
	INT5	I	MFP30	External interrupt 5 input pin.
PD.0	PD.0	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH4	I/O	MFP2	PWM0 channel 4 output/capture input.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	USCI1_CLK	I/O	MFP4	USCI1 clock pin.
	TM0	I/O	MFP5	Timer0 event counter input/toggle output pin.
PD.1	PD.1	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH5	I/O	MFP2	PWM0 channel 5 output/capture input.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	USCI1_DAT0	I/O	MFP4	USCI1 data 0 pin.
	TM1	I/O	MFP5	Timer1 event counter input/toggle output pin.
PD.2	PD.2	I/O	MFP0	General purpose digital I/O pin.

	Pin Name	Type	MFP	Description
	PWM0_CH0	I/O	MFP2	PWM0 channel 0 output/capture input.
	CAN0_TXD	O	MFP3	CAN0 bus transmitter output.
	USCI1_DAT1	I/O	MFP4	USCI1 data 1 pin.
	TM2	I/O	MFP5	Timer2 event counter input/toggle output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
PD.3	PD.3	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH1	I/O	MFP2	PWM0 channel 1 output/capture input.
	CAN0_RXD	I	MFP3	CAN0 bus receiver input.
	USCI1_CTL0	I/O	MFP4	USCI1 control 0 pin.
	TM3	I/O	MFP5	Timer3 event counter input/toggle output pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.
PD.4	PD.4	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH0	I/O	MFP2	PWM0 channel 0 output/capture input.
	UART0_TXD	O	MFP3	UART0 data transmitter output pin.
	USCI0_CLK	I/O	MFP4	USCI0 clock pin.
	TM0	I/O	MFP5	Timer0 event counter input/toggle output pin.
PD.5	PD.5	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH1	I/O	MFP2	PWM0 channel 1 output/capture input.
	UART0_RXD	I	MFP3	UART0 data receiver input pin.
	USCI0_DAT0	I/O	MFP4	USCI0 data 0 pin.
	TM1	I/O	MFP5	Timer1 event counter input/toggle output pin.
PD.6	PD.6	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH2	I/O	MFP2	PWM0 channel 2 output/capture input.
	CAN0_TXD	O	MFP3	CAN0 bus transmitter output.
	USCI0_DAT1	I/O	MFP4	USCI0 data 1 pin.
	TM2	I/O	MFP5	Timer2 event counter input/toggle output pin.
	UART1_nCTS	I	MFP6	UART1 clear to Send input pin.
PD.7	PD.7	I/O	MFP0	General purpose digital I/O pin.
	PWM0_CH3	I/O	MFP2	PWM0 channel 3 output/capture input.
	CAN0_RXD	I	MFP3	CAN0 bus receiver input.
	USCI0_CTL0	I/O	MFP4	USCI0 control 0 pin.
	TM3	I/O	MFP5	Timer3 event counter input/toggle output pin.
	UART1_nRTS	O	MFP6	UART1 request to Send output pin.

5 BLOCK DIAGRAM

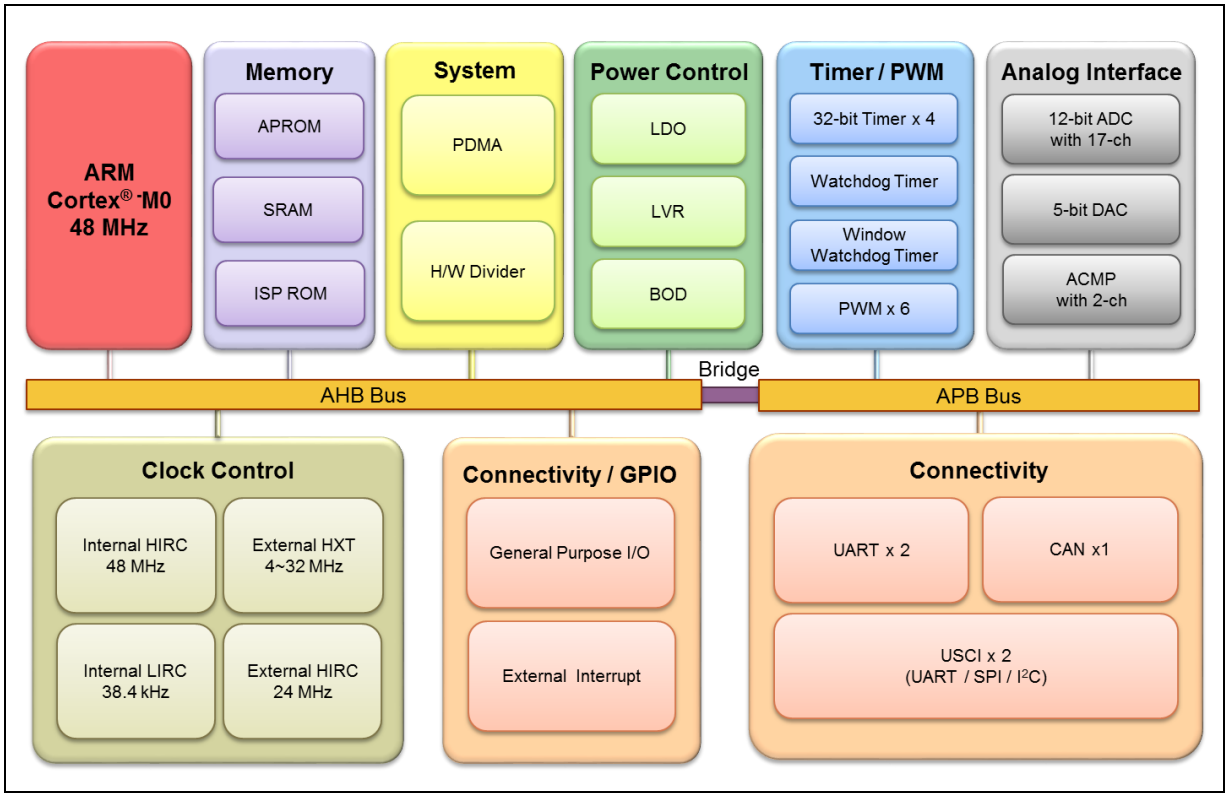


Figure 4.2-1 NuMicro® M0A23U Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Arm® Cortex®-M0 Core

The Cortex®-M0 core is a configurable, multistage, 32-bit RISC processor, which has an AMBA AHB-Lite interface and includes an NVIC component. It also has optional hardware debug functionality. The core can execute Thumb code and is compatible with other Cortex®-M profile processor. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. Figure 6.1-1 shows the functional block diagram of processor.

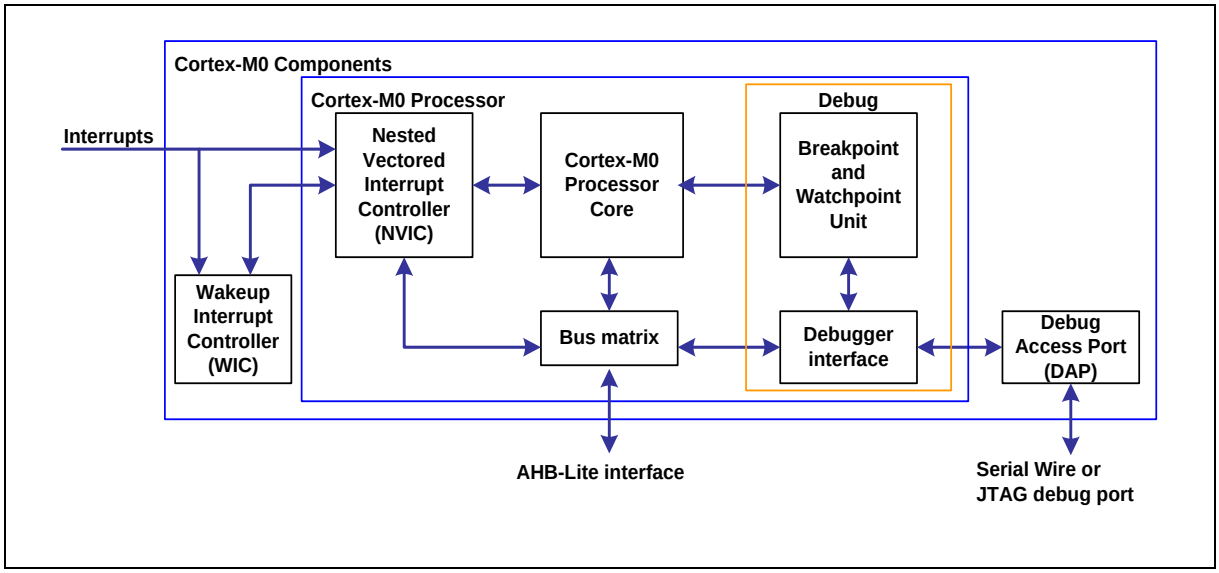


Figure 6.1-1 Functional Block Diagram

The implemented device provides:

- A low gate count processor:
  - Arm®6-M Thumb® instruction set
  - Thumb-2 technology
  - Arm®6-M compliant 24-bit SysTick timer
  - A 32-bit hardware multiplier
  - System interface supported with little-endian data accesses
  - Ability to have deterministic, fixed-latency, interrupt handling
  - Load/store-multiples and multicycle-multiplies that can be abandoned and restarted to facilitate rapid interrupt handling
  - C Application Binary Interface compliant exception model. This is the Armv6-M, C Application Binary Interface (C-ABI) compliant exception model that enables the use of pure C functions as interrupt handlers
  - Low Power Sleep mode entry using the Wait For Interrupt (WFI), Wait For Event (WFE) instructions, or return from interrupt sleep-on-exit feature
- NVIC:
  - 32 external interrupt inputs, each with four levels of priority

  - Dedicated Non-maskable Interrupt (NMI) input
  - Supports for both level-sensitive and pulse-sensitive interrupt lines
  - Supports Wake-up Interrupt Controller (WIC) and, providing Ultra-low Power Sleep mode
- Debug support:
  - Four hardware breakpoints
  - Two watchpoints
  - Program Counter Sampling Register (PCSR) for non-intrusive code profiling
  - Single step and vector catch capabilities
- Bus interfaces:
  - Single 32-bit AMBA-3 AHB-Lite system interface that provides simple integration to all system peripherals and memory
  - Single 32-bit slave port that supports the DAP (Debug Access Port)

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Orginization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex®-M0 core Only by writing 1 to CPURST (SYS_IPRST0[1])
  - nRESET glitch filter time 32us

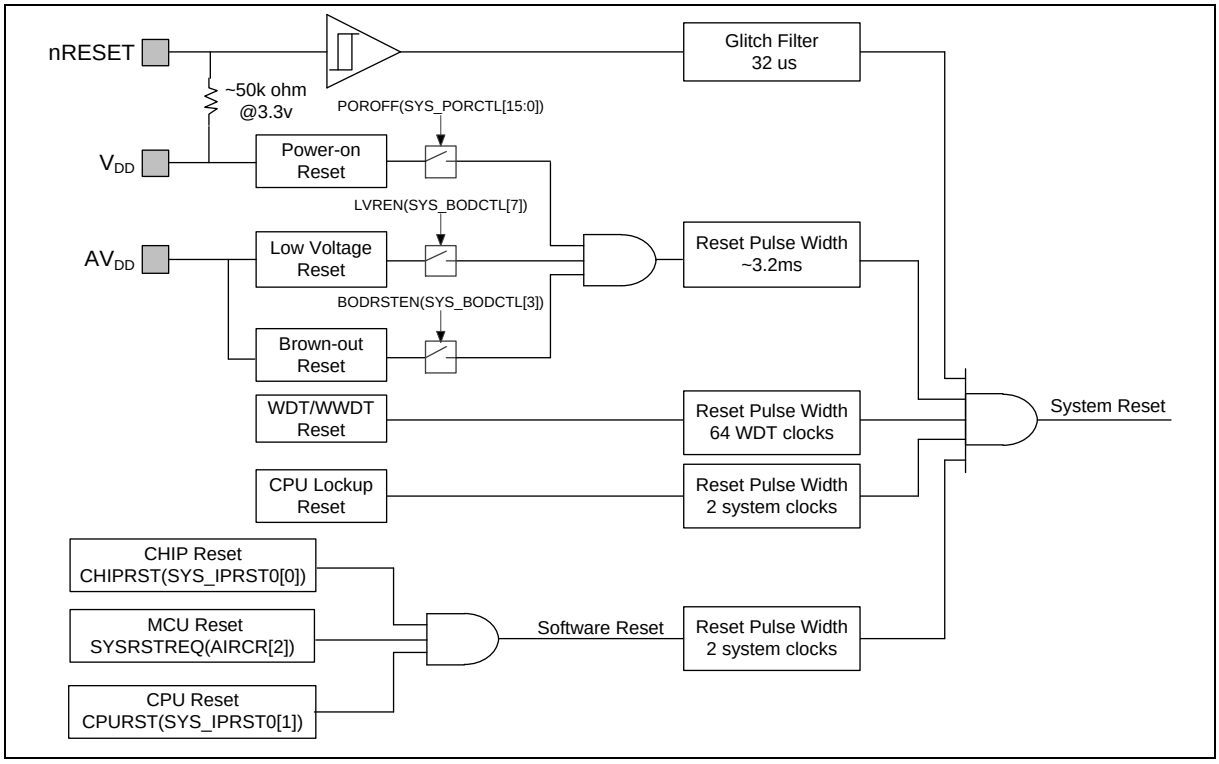


Figure 6.2-1 System Reset Sources

There are a total of 9 reset sources in the NuMicro® family. In general, CPU reset is used to reset Cortex®-M0 only; the other reset sources will reset Cortex®-M0 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	**POR**	**NRESET**	**WDT**	**LVR**	**BOD**	**Lockup**	**CHIP**	**MCU**	**CPU**
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[16])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-

HCLKSEL (CLK_CLKSEL0[2:0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	-	-	-	-	-	-	-	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
HIRCSTB (CLK_STATUS[4])	0x0	-	-	-	-	-	-	-	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0700	0x0700	0x0700	0x0700	0x0700	-	0x0700	-	-
WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
BS (FMC_ISPCTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
CBS (FMC_ISPSTS[2:1))	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-2 shows the nRESET reset waveform.

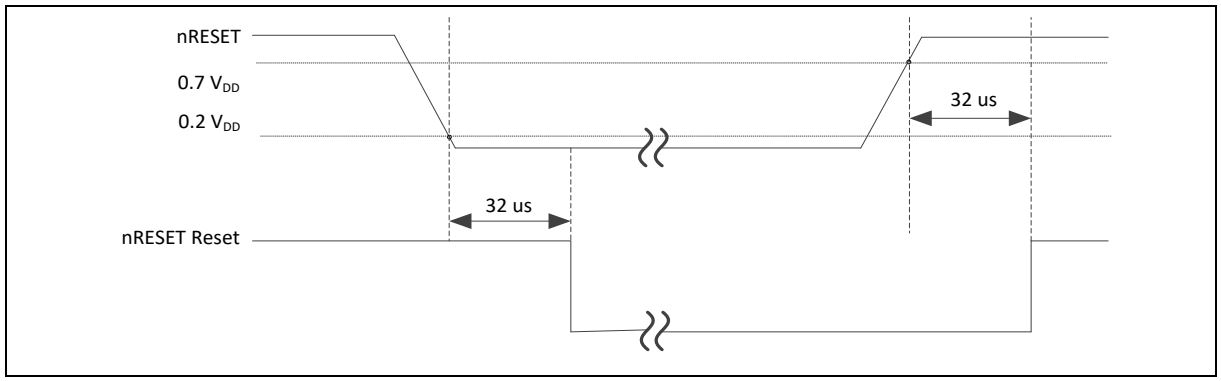


Figure 6.2-2 nRESET Reset Waveform

The special mode can enable nRESET pin function when system select other function for GPA.3, user can input special control signal for GPA.3 make system force enable nRESET pin.

Figure 6.2-3 shows the method of entry special mode.

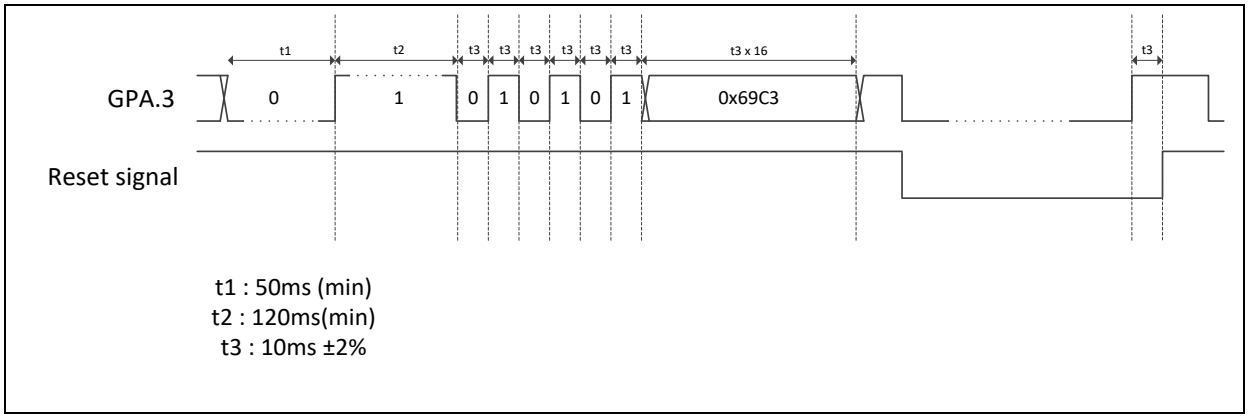


Figure 6.2-3 nRESET Reset Mode Enable Control Waveform

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-4 shows the power-on reset waveform.

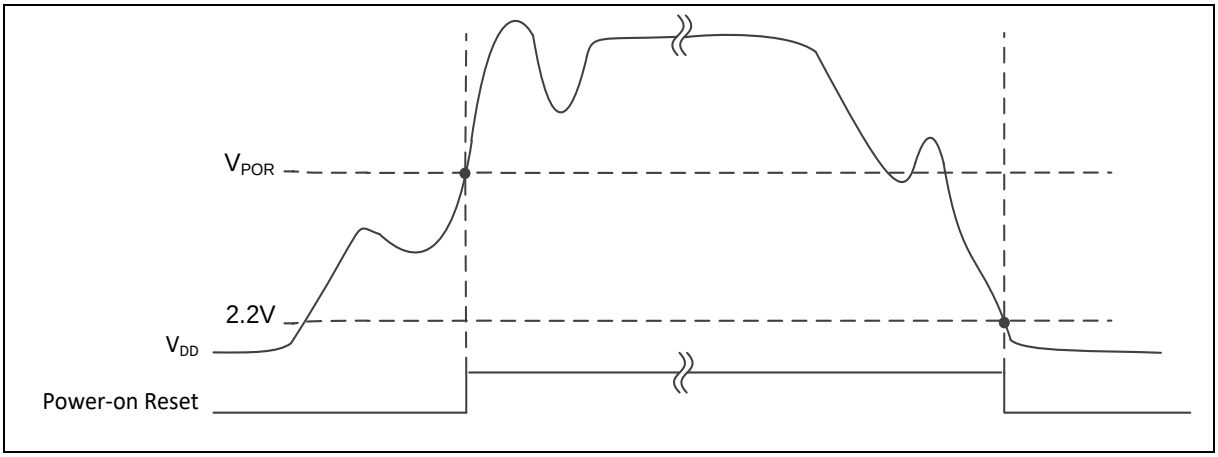


Figure 6.2-4 Power-on Reset (POR) Waveform

6.2.2.3 *Low Voltage Reset (LVR)*

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-5 shows the Low Voltage Reset waveform.

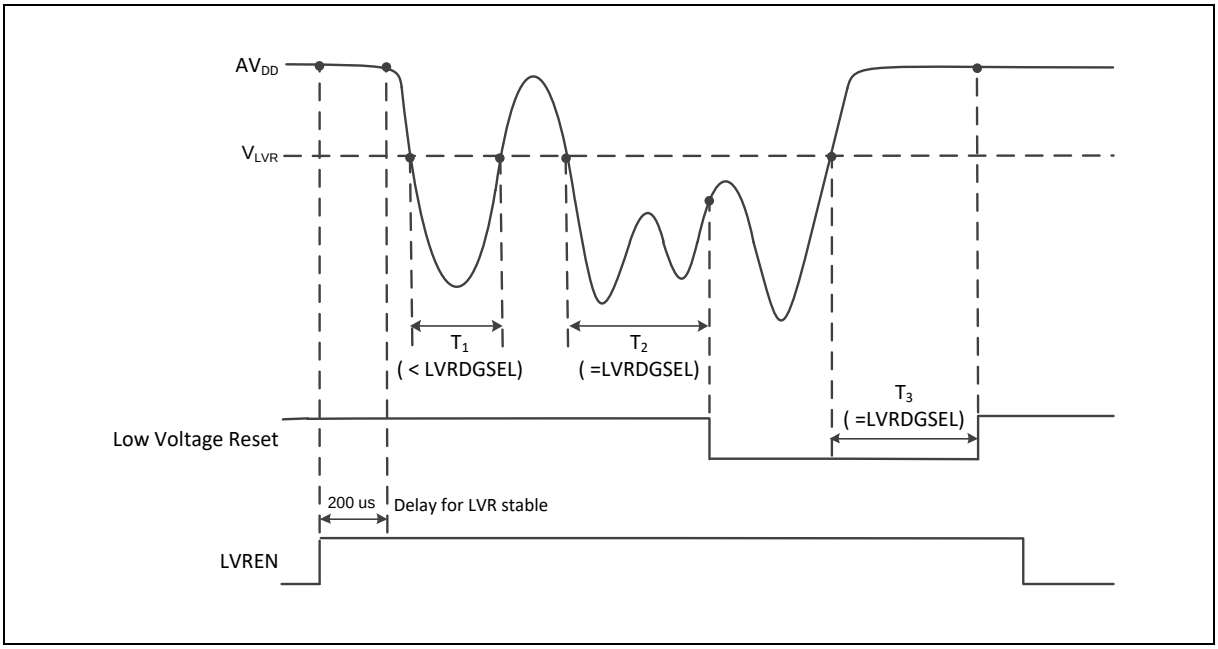


Figure 6.2-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 *Brown-out Detector Reset (BOD Reset)*

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[17:16]) and the state keeps longer than De-glitch time set by BODDGSEL

(SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-6 shows the Brown-out Detector waveform.

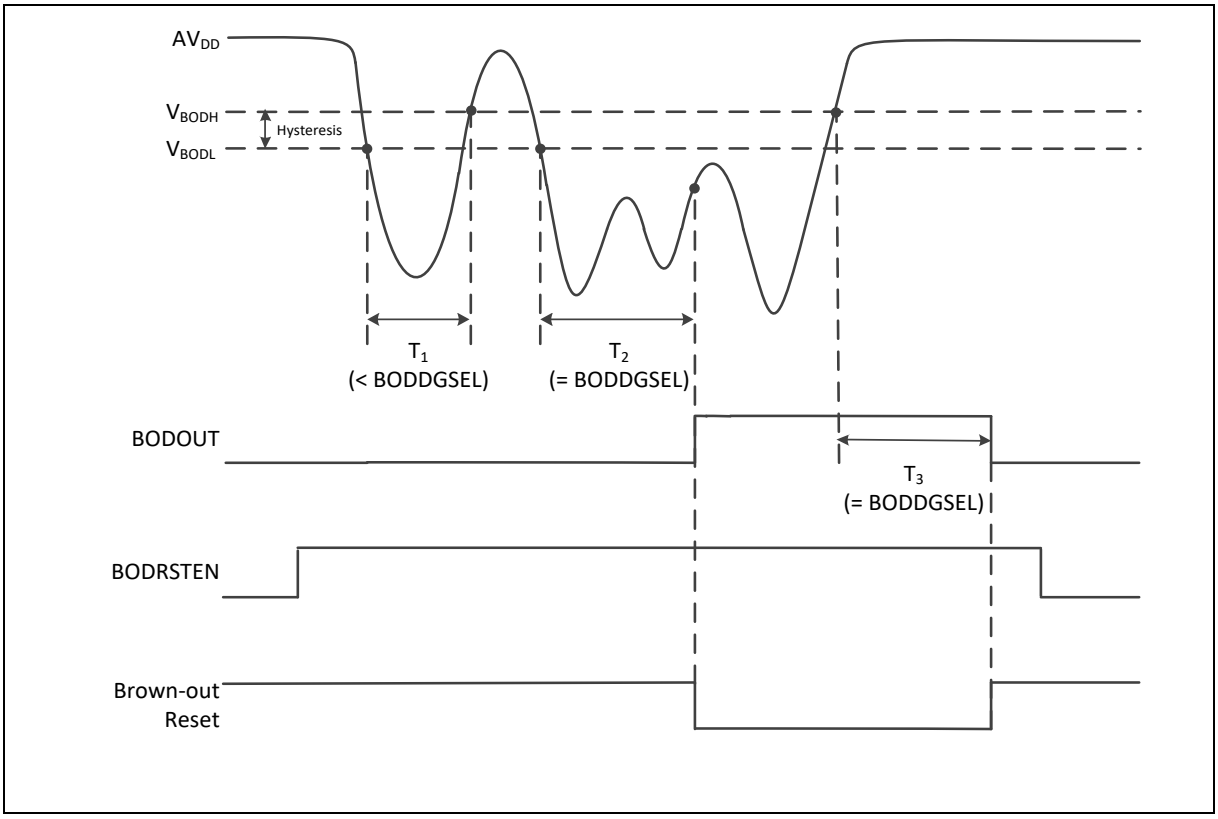


Figure 6.2-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex®-M0 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[0]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into three segments:

- Analog power from V_{DD} and V_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides a fixed 1.8V power for digital operation and I/O pins.

The outputs of internal voltage regulators, LDO and V_{DD}, require an external capacitor which should be located close to the corresponding pin. Figure 6.2-7 shows the NuMicro® M0A23U power distribution.

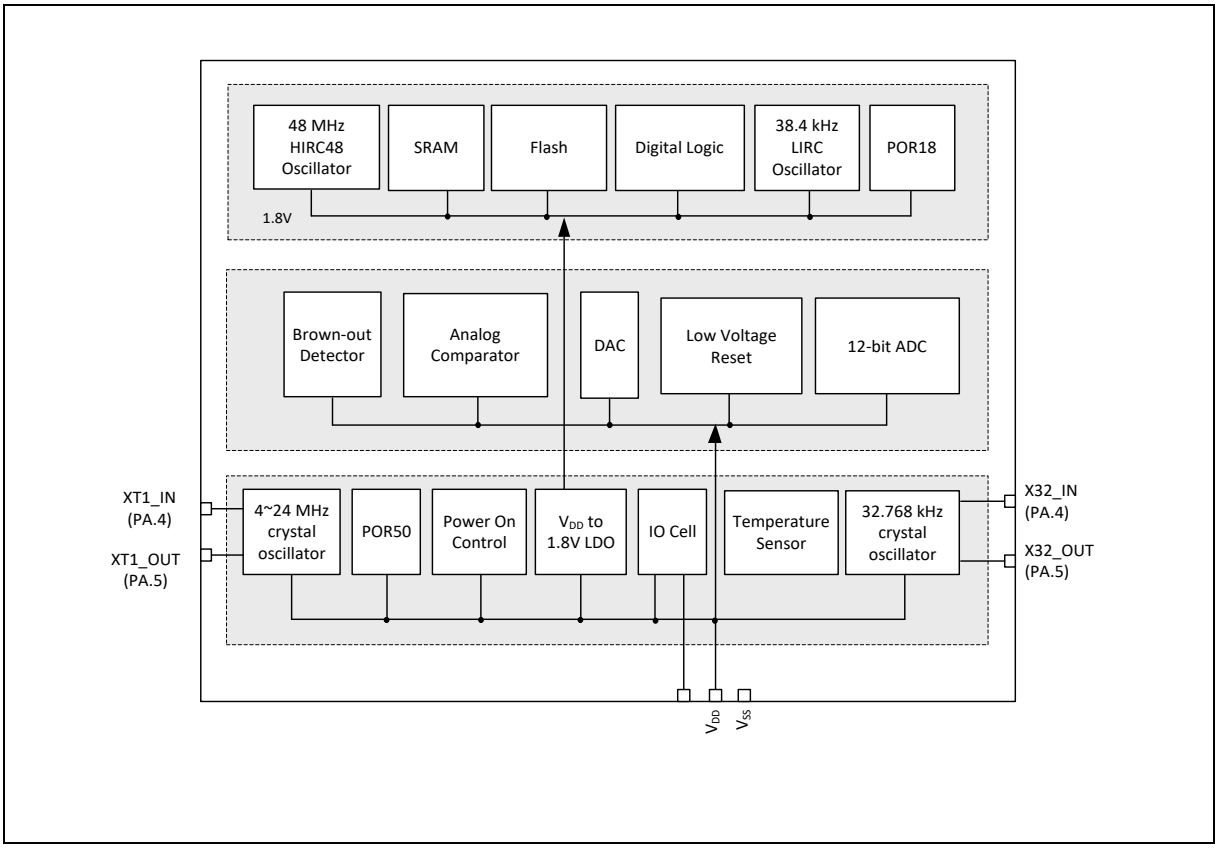


Figure 6.2-7 NuMicro® M0A23U Power Distribution Diagram

6.2.4 Power Modes and Wake-up Sources

The M0A23U series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode in the M0A23U series.

Mode	CPU Operating Maximum Speed(MHz)	Clock Disable
Normal mode	48	All clocks are disabled by control register.
Idle mode	CPU enter Sleep mode	Only CPU clock is disabled.

Power-down mode	CPU enters Power-down mode	Most clocks are disabled except LIRC/LXT, and only WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.

Table 6.2-2 Power Mode Table

There are different power mode entry settings and leaving condition for each power mode. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running in normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCT:[7]) and execute WFI instruction.

Register/Instruction Mode	**SLEEPDEEP (SCR[2])**	**PDEN (CLK_PWRCTL[7])**	**CPU Run WFI Instruction**
Normal mode	0	0	NO
Idle mode (CPU enter Sleep mode)	0	0	YES
Power-down mode (CPU enters Deep Sleep mode)	1	1	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode. Table 6.2-4 lists the available clocks for each power mode.

Power Mode	**Normal Mode**	**Idle Mode**	**Power-Down Mode**
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all clocks stop except LXT and LIRC. SRAM content retended.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	WDT, Timer, UART, BOD, GPIO, EINT, USCI, CAN and ACMP
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Difference Table

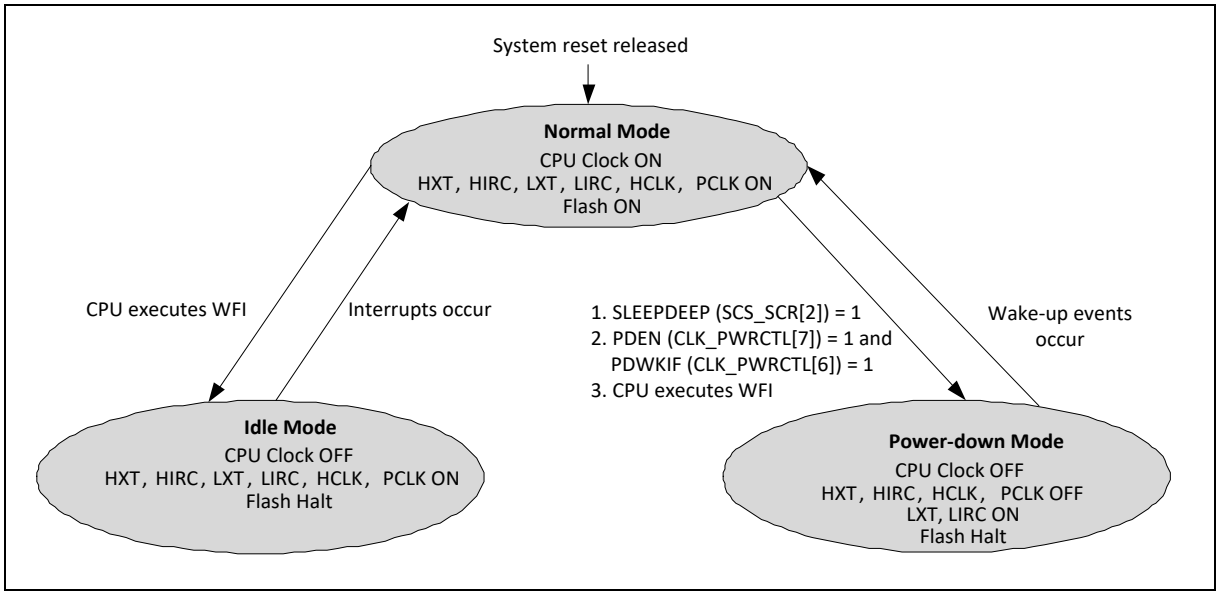


Figure 6.2-8 Power Mode State Machine

1. LXT (32768 Hz XTL) ON or OFF depends on SW setting in normal mode.
2. LIRC (38.4 kHz OSC) ON or OFF depends on S/W setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC and LIRC is on.
5. If UART clock source is selected as LXT and LXT is on.

	Normal Mode	Idle Mode	Power-Down Mode
HXT (4~24 MHz XTL)	ON	ON	Halt
HIRC48 (48 MHz OSC)	ON	ON	Halt
LXT (32768 Hz XTL)	ON	ON	ON/OFF[1]
LIRC (38.4 kHz OSC)	ON	ON	ON/OFF[2]
MLDO	ON	ON	OFF
ULDO	ON	ON	ON
CPU	ON	Halt	Halt
HCLK/PCLK	ON	ON	Halt
SRAM retention	ON	ON	ON
FLASH	ON	ON	Halt
GPIO	ON	ON	Halt
PDMA	ON	ON	Halt
TIMER	ON	ON	ON/OFF[3]
PWM	ON	ON	Halt
WDT	ON	ON	ON/OFF[4]
WWDT	ON	Halt	Halt
UART	ON	ON	ON/OFF[6]
USCI	ON	ON	Halt
ADC	ON	ON	Halt
ACMP	ON	ON	Halt

Table 6.2-5 Clocks in Power Modes

Wake-up sources in Power-down mode:

WDT, Timer, UART, USCI, BOD, GPIO, CAN, and ACMP.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-5 lists the condition about how to enter Power-down mode again for each peripheral.

*User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up Source	Wake-Up Condition	System Can Enter Power-Down Mode Again Condition*
BOD	Brown-Out Detector Interrupt	After software writes 1 to clear (SYS_BODCTL[4]).
INT	External Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	After software write 1 to clear the Px_INTSRC[n] bit.
TIMER	Timer Interrupt	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
WDT	WDT Interrupt	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).

UART0/1	nCTS wake-up	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
CAN	RX Data wake-up	After software writes 1 to clear WAKUP_STS (CAN_WU_STATUS[0]).
ACMP	Comparator Power-Down Wake-Up Interrupt	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]) and WKIF1 (ACMP_STATUS[9]).

Table 6.2-6 Condition of Entering Power-down Mode Again

6.2.5 System Memory Map

The NuMicro® M0A23U series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The M0A23U series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x0000_7FFF	FLASH_BA	FLASH Memory Space (32 Kbytes)
0x2000_0000 – 0x2000_0FFF	SRAM0_BA	SRAM Memory Space (4 Kbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA_BA	Peripheral DMA Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4001_4000 – 0x4001_7FFF	HDIV_BA	Hardware Divider Register
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_0FFF	WDT_BA	Watchdog Timer Control Registers
0x4004_3000 – 0x4004_3FFF	ADC_BA	Analog-Digital-Converter (ADC) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/ 1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC0_BA	DAC 0 Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	PWM0_BA	PWM0 Control Registers

0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers
0x400A_0000 – 0x400A_0FFF	CAN0_BA	CAN0 Control Registers
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
0x400D_1000 – 0x400D_1FFF	USCI1_BA	USCI1 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers
0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.6 SRAM Memory Orginization

The M0A23U supports embedded SRAM with total 4 Kbytes size

- Supports total 4 Kbytes SRAM
- Supports byte / half word / word write
- Supports oversize response error

Table 6.2-9 shows the SRAM organization of M0A23U. The address between 0x2000_1000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

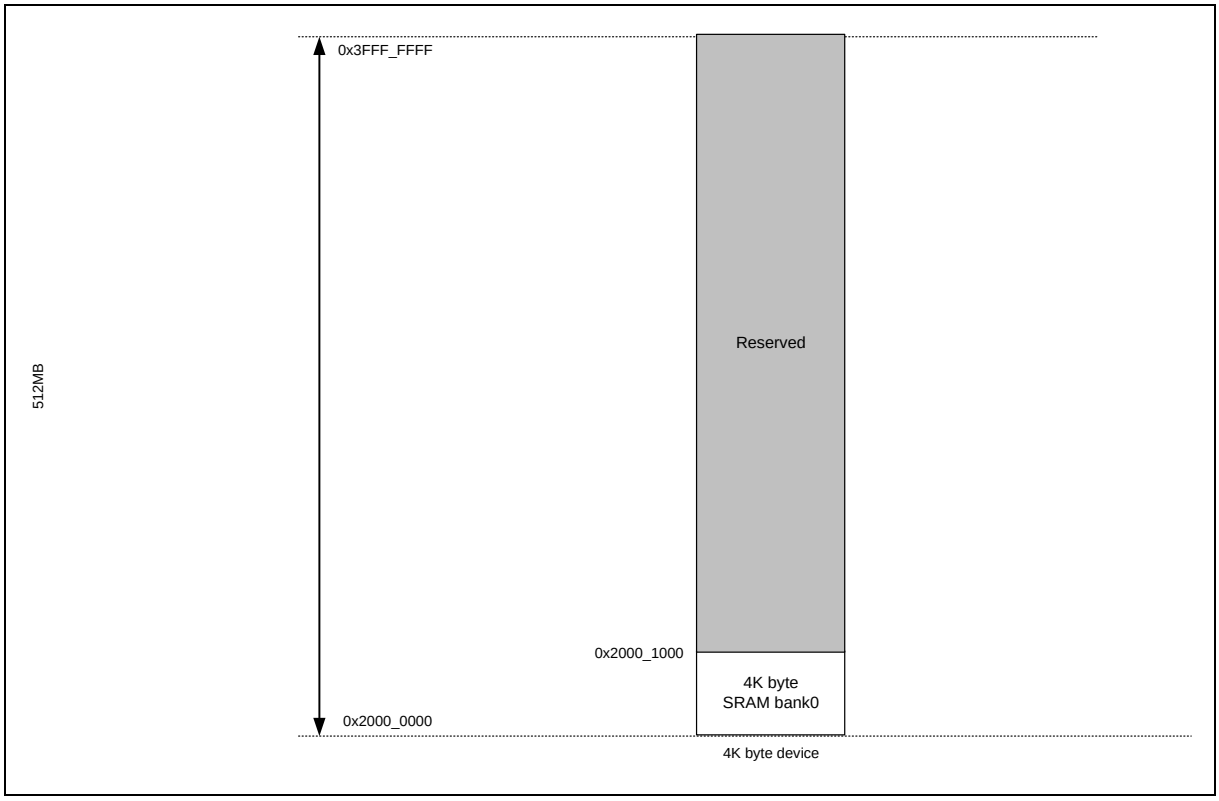


Figure 6.2-9 SRAM Memory Organization

6.2.7 Chip Bus Matrix

The M0A23U series supports Bus Matrix to manage the access arbitration between masters. The access arbitration use round-robin algorithm as the bus priority.

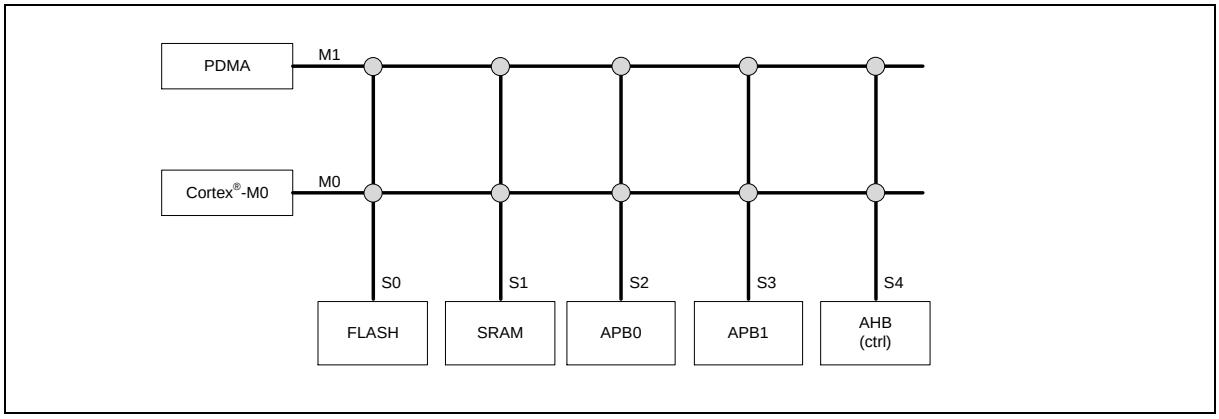


Figure 6.2-10 NuMicro® M0A23U Bus Matrix Diagram

6.2.8 IRC Auto Trim

This chip supports auto-trim function: the HIRC trim (48 MHz RC oscillator), according to the accurate external 32.768 kHz crystal oscillator, automatically gets accurate output frequency, 0.25 % deviation within all temperature ranges.

In HIRC case, the system needs an accurate 48 MHz clock. In such case, if not soldering 32.768 kHz crystal or 12 MHz crystal in system, user has to set REFCKSEL (SYS_HIRCTRIMCTL [10] reference clock selection) to “0”, set FREQSEL (SYS_HIRCTRIMCTL [1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTRIMSTS[0] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.9 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence. All proteced control registers are noted “(Write Protect)” and add an note “**Note:** This bit is write protected. Refer to the SYS_REGLCTL register in register description field.

6.2.10 UART0_TXD/USCI0_DAT0 Modulation with PWM

This chip supports UART0_TXD/USCI_DAT0 to modulate with PWM channel. User can set MODPWMSEL(SYS_MODCTL[7:4]) to choose which PWM0 channel to modulate with UART0_TXD/USCI0_DAT0 and set MODEN(SYS_MODCTL[0]) to enable modulation function. User can set TXDINV(UART_LINE[8]) to inverse UART0_TXD or DATOINV(UUART_LINECTL[5]) to inverse USCI0_DAT0 before modulating with PWM.

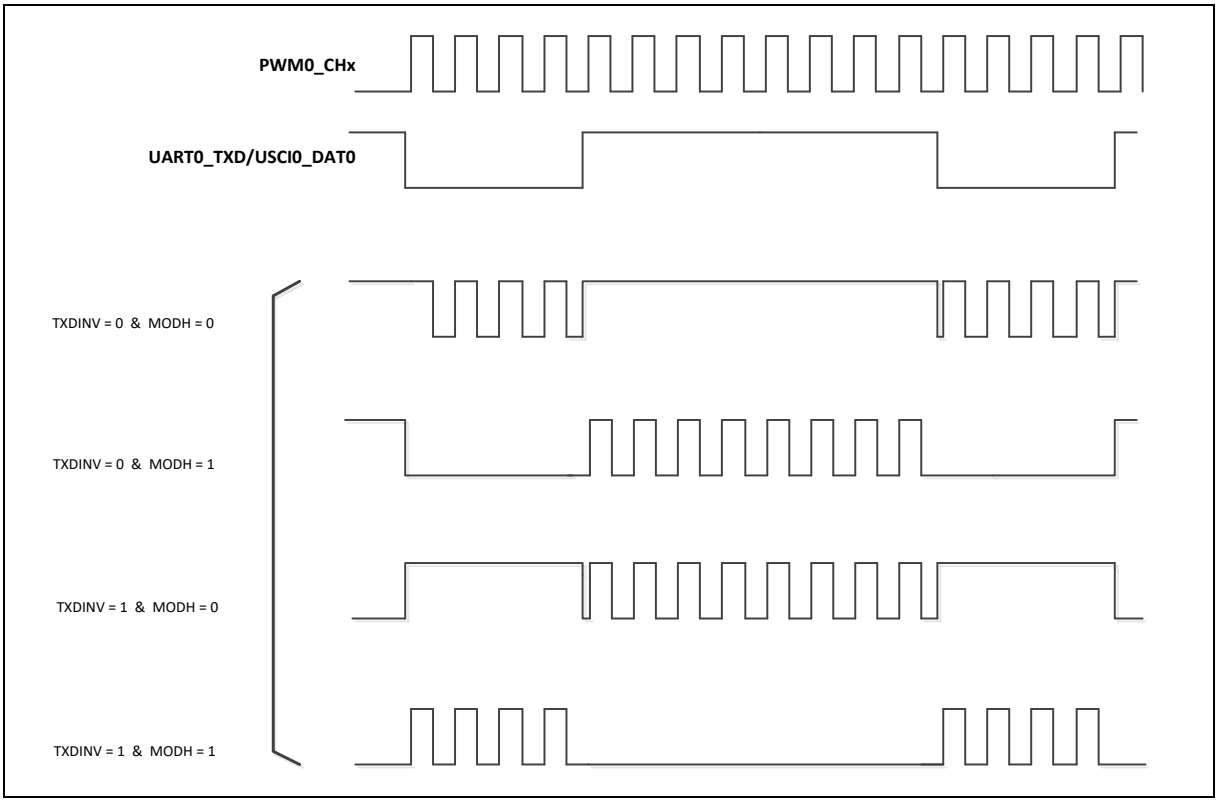


Figure 6.2-11 UART0_TXD/USCI0_DAT0 Modulated with PWM Channel

6.2.11 System Timer (SysTick)

The Cortex®-M0 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the “Arm® Cortex®-M0 Technical Reference Manual” and “Arm® v6-M Architecture Reference Manual”.

6.2.11.1 System Timer Control Register Map

R: read only, **W**: write only, **R/W**: both read and write

Register	Offset	R/W	Description	Reset Value
SYST Base Address: **SCS_BA = 0xE000_E000**				
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

6.2.11.2 System Timer Control Register Description

SysTick Control and Status Register (SYST_CTRL)

Register	Offset	R/W	Description	Reset Value
SYST_CTRL	SCS_BA+0x10	R/W	SysTick Control and Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							COUNTFLAG
15	14	13	12	11	10	9	8
Reserved							
7	6	5	4	3	2	1	0
Reserved					CLKSRC	TICKINT	ENABLE

Bits	Description	
[31:17]	**Reserved**	Reserved.
[16]	**COUNTFLAG**	**System Tick Counter Flag** Returns 1 if timer counted to 0 since last time this register was read. COUNTFLAG is set by a count transition from 1 to 0. COUNTFLAG is cleared on read or by a write to the Current Value register.
[15:3]	**Reserved**	Reserved.
[2]	**CLKSRC**	**System Tick Clock Source Selection** 0 = Clock source is the (optional) external reference clock. 1 = Core clock used for SysTick.
[1]	**TICKINT**	**System Tick Interrupt Enabled** 0 = Counting down to 0 does not cause the SysTick exception to be pended. Software can use COUNTFLAG to determine if a count to zero has occurred. 1 = Counting down to 0 will cause the SysTick exception to be pended. Clearing the SysTick current value register by a register write in software will not cause SysTick to be pended.
[0]	**ENABLE**	**System Tick Counter Enabled** 0 = Counter Disabled. 1 = Counter will operate in a multi-shot manner.

SysTick Reload Value Register (SYST_LOAD)

Register	Offset	R/W	Description	Reset Value
SYST_LOAD	SCS_BA+0x14	R/W	SysTick Reload Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
RELOAD							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
RELOAD							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RELOAD							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**RELOAD**	**System Tick Reload Value** The value to load into the Current Value register when the counter reaches 0.

SysTick Current Value Register (SYST_VAL)

Register	Offset	R/W	Description	Reset Value
SYST_VAL	SCS_BA+0x18	R/W	SysTick Current Value Register	0xXXXX_XXXX

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CURRENT							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CURRENT							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CURRENT							

Bits	Description	
[31:24]	**Reserved**	Reserved.
[23:0]	**CURRENT**	**System Tick Current Value** Current counter value. This is the value of the counter at the time it is sampled. The counter does not provide read-modify-write protection. The register is write-clear. A software write of any value will clear the register to 0.

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The Cortex®-M0 provides an interrupt controller as an integral part of the exception mode, named as "Nested Vectored Interrupt Controller (NVIC)", which is closely coupled to the processor core and provides following features:

- Nested and Vectored interrupt support
- Automatic processor state saving and restoration
- Reduced and deterministic interrupt latency

The NVIC prioritizes and handles all supported exceptions. All exceptions are handled in "Handler Mode". This NVIC architecture supports 32 (IRQ[31:0]) discrete interrupts with 4 levels of priority. All of the interrupts and most of the system exceptions can be configured to different priority levels. When an interrupt occurs, the NVIC will compare the priority of the new interrupt to the current running one's priority. If the priority of the new interrupt is higher than the current one, the new interrupt handler will override the current handler.

When an interrupt is accepted, the starting address of the interrupt service routine (ISR) is fetched from a vector table in memory. There is no need to determine which interrupt is accepted and branch to the starting address of the correlated ISR by software. While the starting address is fetched, NVIC will also automatically save processor state including the registers "PC, PSR, LR, R0~R3, R12" to the stack. At the end of the ISR, the NVIC will restore the mentioned registers from stack and resume the normal execution. Thus it will take less and deterministic time to process the interrupt request.

The NVIC supports "Tail Chaining" which handles back-to-back interrupts efficiently without the overhead of states saving and restoration and therefore reduces delay time in switching to pending ISR at the end of current ISR. The NVIC also supports "Late Arrival" which improves the efficiency of concurrent ISRs. When a higher priority interrupt request occurs before the current ISR starts to execute (at the stage of state saving and starting address fetching), the NVIC will give priority to the higher one without delay penalty. Thus it advances the real-time capability.

For more detailed information, please refer to the "Arm® Cortex®-M0 Technical Reference Manual" and "Arm® v6-M Architecture Reference Manual".

6.2.12.1 Exception Model and System Interrupt Map

Table 6.2-8 lists the exception model supported by the M0A23U series. Software can set four levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as "0" and the lowest priority is denoted as "3". The default priority of all the user-configurable interrupts is "0". Note that priority "0" is treated as the fourth priority on the system, after three system exceptions "Reset", "NMI" and "Hard Fault".

Exception Name	Vector Number	Priority
Reset	1	-3
NMI	2	-2
Hard Fault	3	-1
Reserved	4 ~ 10	Reserved
SVCall	11	Configurable
Reserved	12 ~ 13	Reserved
PendSV	14	Configurable

SysTick	15	Configurable
Interrupt (IRQ0 ~ IRQ31)	16 ~ 47	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-Out low voltage detected interrupt
17	1	WDT_INT	Watchdog Timer interrupt
18	2	EINT024	External interrupt from EINT0,2,4.
19	3	EINT135	External interrupt from EINT1.3.5
20	4	GPAB_INT	External interrupt from PA, PB pin
21	5	GPCD_INT	External interrupt from PC, PD pin
22	6	PWM0_INT	PWM0 interrupt
23	7	Reserved	Reserved
24	8	TMR0_INT	Timer 0 interrupt
25	9	TMR1_INT	Timer 1 interrupt
26	10	TMR2_INT	Timer 2 interrupt
27	11	TMR3_INT	Timer 3 interrupt
28	12	UART0_INT	UART0 interrupt
29	13	UART1_INT	UART1 interrupt
30	14	Reserved	Reserved
31	15	CAN0_INT	CAN0 interrupt
32	16	Reserved	Reserved
33	17	Reserved	Reserved
34	18	Reserved	Reserved
35	19	Reserved	Reserved
36	20	Reserved	Reserved
37	21	Reserved	Reserved
38	22	USCI0	USCI0 interrupt
39	23	Reserved	Reserved
40	24	DAC0_INT	DAC0 interrupt
41	25	ACMP01_INT	ACMP0 and ACMP1 interrupt
42	26	PDMA_INT	PDMA interrupt

43	27	USCI1	USCI1 interrupt
44	28	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
45	29	ADC_INT	ADC interrupt
46	30	CLKFAIL	Clock fail detected or IRC Auto Trim interrupt
47	31	Reserved	Reserved

Table 6.2-9 Interrupt Number Table

6.2.12.2 Vector Table

When an interrupt is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. For Armv6-M, the vector table base address is fixed at 0x00000000. The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Vector Table Word Offset	Description
0	SP_main – The Main stack pointer
Vector Number	Exception Entry Pointer using that Vector Number

Table 7.2-10 Vector Figure Format

6.2.12.3 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not be activated. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.12.4 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..7**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

IRQ0 ~ IRQ31 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x000	R/W	IRQ0 ~ IRQ31 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x080	R/W	IRQ0 ~ IRQ31 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ31 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ31 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0 registers force interrupts into the pending state, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ31 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0 registers remove the pending state from interrupts, and show which interrupts are pending Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ31 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ31 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0 registers indicate which interrupts are active. 0 = interrupt not active. 1 = interrupt active.

IRQ0 ~ IRQ31 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..7**	0xE000E400 +0x4*n	R/W	IRQ0 ~ IRQ31 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_4n_2		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
PRI_4n_1		**Reserved**					
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
PRI_4n_0		**Reserved**					

Bits	Description	
[31:30]	**PRI_4n_3**	**Priority of IRQ_4n+3** "0" denotes the highest priority and "3" denotes the lowest priority
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_4n_2**	**Priority of IRQ_4n+2** "0" denotes the highest priority and "3" denotes the lowest priority
[21:16]	**Reserved**	Reserved.
[15:14]	**PRI_4n_1**	**Priority of IRQ_4n+1** "0" denotes the highest priority and "3" denotes the lowest priority
[13:8]	**Reserved**	Reserved.
[7:6]	**PRI_4n_0**	**Priority of IRQ_4n+0** "0" denotes the highest priority and "3" denotes the lowest priority
[5:0]	**Reserved**	Reserved.

Software Trigger Interrupt Register (STIR)

Register	Offset	R/W	Description	Reset Value
STIR	0xE000EF00	R/W	Software Trigger Interrupt Registers	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**INTID**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTID							

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8:0]	**INTID**	**Interrupt ID** Write to the STIR To Generate An Interrupt from Software When the USERSETMPEND bit in the SCR is set to 1, unprivileged software can access the STIR Interrupt ID of the interrupt to trigger, in the range 0-31. For example, a value of 0x03 specifies interrupt IRQ3.

6.2.12.5 NMI Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NMI Base Address: **NMI_BA = 0x4000_0300**				
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

NMI Source Interrupt Enable Register (NMIEN)

Register	Offset	R/W	Description	Reset Value
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UART1_INT	**UART0_INT**	**EINT5**	**EINT4**	**EINT3**	**EINT2**	**EINT1**	**EINT0**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**CLKFAIL**	**Reserved**	**PWRWU_INT**	**IRC_INT**	**BODOUT**

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 NMI Source Enable (Write Protect)** 0 = UART1 NMI source Disabled. 1 = UART1 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[14]	**UART0_INT**	**UART0 NMI Source Enable (Write Protect)** 0 = UART0 NMI source Disabled. 1 = UART0 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[13]	**EINT5**	**External Interrupt From PC.7 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PC.7 pin NMI source Disabled. 1 = External interrupt from PC.7 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[12]	**EINT4**	**External Interrupt From PC.6 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PC.6 pin NMI source Disabled. 1 = External interrupt from PC.6 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[11]	**EINT3**	**External Interrupt From PC.3 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PC.3 pin NMI source Disabled. 1 = External interrupt from PC.3 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[10]	**EINT2**	**External Interrupt From PC.4 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PC.4 pin NMI source Disabled. 1 = External interrupt from PC.4 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[9]	**EINT1**	**External Interrupt From PC.5 Pin NMI Source Enable (Write Protect)**

		0 = External interrupt from PC.5 pin NMI source Disabled. 1 = External interrupt from PC.5 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[8]	**EINT0**	**External Interrupt From PA.3 or PB.5 Pin NMI Source Enable (Write Protect)** 0 = External interrupt from PA.3 or PB.5 pin NMI source Disabled. 1 = External interrupt from PA.3 or PB.5 pin NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[7:5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected and IRC Auto Trim Interrupt NMI Source Enable (Write Protect)** 0 = Clock fail detected and IRC Auto Trim interrupt NMI source Disabled. 1 = Clock fail detected and IRC Auto Trim interrupt NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**Reserved**	Reserved.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up NMI Source Enable (Write Protect)** 0 = Power-down mode wake-up NMI source Disabled. 1 = Power-down mode wake-up NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**IRC_INT**	**IRC TRIM NMI Source Enable (Write Protect)** 0 = IRC TRIM NMI source Disabled. 1 = IRC TRIM NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**BODOUT**	**BOD NMI Source Enable (Write Protect)** 0 = BOD NMI source Disabled. 1 = BOD NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

NMI Source Interrupt Status Register (NMISTS)

Register	Offset	R/W	Description	Reset Value
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UART1_INT	**UART0_INT**	**EINT5**	**EINT4**	**EINT3**	**EINT2**	**EINT1**	**EINT0**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**CLKFAIL**	**Reserved**	**PWRWU_INT**	**IRC_INT**	**BODOUT**

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[14]	**UART0_INT**	**UART0 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[13]	**EINT5**	**External Interrupt From PC.7 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PC.7 interrupt is deasserted. 1 = External Interrupt from PC.7 interrupt is asserted.
[12]	**EINT4**	**External Interrupt From PC.6 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PC.6 interrupt is deasserted. 1 = External Interrupt from PC.6 interrupt is asserted.
[11]	**EINT3**	**External Interrupt From PC.3 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PC.3 interrupt is deasserted. 1 = External Interrupt from PC.3 interrupt is asserted.
[10]	**EINT2**	**External Interrupt From PC.4 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PC.4 interrupt is deasserted. 1 = External Interrupt from PC.4 interrupt is asserted.
[9]	**EINT1**	**External Interrupt From PC.5 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PC.5 interrupt is deasserted. 1 = External Interrupt from PC.5 interrupt is asserted.
[8]	**EINT0**	**External Interrupt From PA.3 or PB.5 Pin Interrupt Flag (Read Only)** 0 = External Interrupt from PA.3 or PB.5 interrupt is deasserted. 1 = External Interrupt from PA.3 or PB.5 interrupt is asserted.
[7:5]	**Reserved**	Reserved.

[4]	**CLKFAIL**	**Clock Fail Detected or IRC Auto Trim Interrupt Flag (Read Only)** 0 = Clock fail detected or IRC Auto Trim interrupt is deasserted. 1 = Clock fail detected or IRC Auto Trim interrupt is asserted.
[3]	**Reserved**	Reserved.
[2]	**PWRWU_INT**	**Power-down Mode Wake-up Interrupt Flag (Read Only)** 0 = Power-down mode wake-up interrupt is deasserted. 1 = Power-down mode wake-up interrupt is asserted.
[1]	**IRC_INT**	**IRC TRIM Interrupt Flag (Read Only)** 0 = HIRC TRIM interrupt is deasserted. 1 = HIRC TRIM interrupt is asserted.
[0]	**BODOUT**	**BOD Interrupt Flag (Read Only)** 0 = BOD interrupt is deasserted. 1 = BOD interrupt is asserted.

6.2.13 System Control Register

The Cortex®-M0 status and operation mode control are managed by System Control Registers. Including CPUID, Cortex®-M0 interrupt priority and Cortex®-M0 power management can be controlled through these system control registers.

For more detailed information, please refer to the "*Arm® Cortex®-M0 Technical Reference Manual*" and "*Arm® v6-M Architecture Reference Manual*".

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
SCR Base Address: **SCS_BA = 0xE000_E000**				
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

Interrupt Control State Register (ICSR)

Register	Offset	R/W	Description	Reset Value
ICSR	SCS_BA+0xD04	R/W	Interrupt Control and State Register	0x0000_0000

31	30	29	28	27	26	25	24
NMIPENDSET	Reserved		PENDSVSET	PENDSVCLR	PENDSTSET	PENDSTCLR	Reserved
23	22	21	20	19	18	17	16
ISRPREEMPT	ISRPENDING	Reserved				VECTPENDING	
15	14	13	12	11	10	9	8
VECTPENDING				RETTOBASE	Reserved		
7	6	5	4	3	2	1	0
Reserved		VECTACTIVE					

Bits	Description	
[31]	**NMIPENDSET**	**NMI Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes NMI exception state to pending. Read Operation: 0 = NMI exception is not pending. 1 = NMI exception is pending. **Note:** Because NMI is the highest-priority exception, normally the processor enters the NMI exception handler as soon as it detects a write of 1 to this bit. Entering the handler then clears this bit to 0. This means a read of this bit by the NMI exception handler returns 1 only if the NMI signal is reasserted while the processor is executing that handler.
[30:29]	**Reserved**	Reserved.
[28]	**PENDSVSET**	**PendSV Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes PendSV exception state to pending. Read Operation: 0 = PendSV exception is not pending. 1 = PendSV exception is pending. **Note:** Writing 1 to this bit is the only way to set the PendSV exception state to pending.
[27]	**PENDSVCLR**	**PendSV Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the PendSV exception. **Note:** This is a write only bit. To clear the PENDSV bit, you must “write 0 to PENDSVSET and write 1 to PENDSVRTC_CAL” at the same time.

[26]	**PENDSTSET**	**SysTick Exception Set-pending Bit** Write Operation: 0 = No effect. 1 = Changes SysTick exception state to pending. Read Operation: 0 = SysTick exception is not pending. 1 = SysTick exception is pending.
[25]	**PENDSTCLR**	**SysTick Exception Clear-pending Bit** Write Operation: 0 = No effect. 1 = Removes the pending state from the SysTick exception. **Note:** This is a write only bit. To clear the PENDST bit, you must "write 0 to PENDSTSET and write 1 to PENDSTRTC_CAL" at the same time.
[24]	**Reserved**	Reserved.
[23]	**ISRPREEMPT**	**Interrupt Preempt Bit (Read Only)** If set, a pending exception will be serviced on exit from the debug halt state.
[22]	**ISRPENDING**	**Interrupt Pending Flag, Excluding NMI and Faults (Read Only)** 0 = Interrupt not pending. 1 = Interrupt pending.
[21:18]	**Reserved**	Reserved.
[17:12]	**VECTPENDING**	**Number of the Highest Pended Exception** Indicate the Exception Number of the Highest Priority Pending Enabled Exception 0 = no pending exceptions. Nonzero = the exception number of the highest priority pending enabled exception. The value indicated by this field includes the effect of the BASEPRI and FAULTMASK registers, but not any effect of the PRIMASK register.
[11]	**RETTOBASE**	**Preempted Active Exceptions Indicator** Indicate whether There are Preempted Active Exceptions 0 = there are preempted active exceptions to execute. 1 = there are no active exceptions, or the currently-executing exception is the only active exception.
[10:6]	**Reserved**	Reserved.
[5:0]	**VECTACTIVE**	**Number of the Current Active Exception** 0 = Thread mode. Non-zero = The exception number of the currently active exception.

Application Interrupt and Reset Control Register (AIRCR)

Register	Offset	R/W	Description	Reset Value
AIRCR	SCS_BA+0xD0C	R/W	Application Interrupt and Reset Control Register	0xFA05_0000

31	30	29	28	27	26	25	24
VECTORKEY							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
VECTORKEY							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ENDIANNESS	**Reserved**				**PRIGROUP**		
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved					**SYSRESETREQ**	**VECTCLRACTIVE**	**VECTRESET**

Bits	Description	
[31:16]	**VECTORKEY**	**Register Access Key** When writing this register, this field should be 0x05FA, otherwise the write action will be unpredictable. The VECTORKEY filed is used to prevent accidental write to this register from resetting the system or clearing of the exception status.
[15]	**ENDIANNESS**	**Data Endianness** 0 = Little-endian. 1 = Big-endian.
[14:11]	**Reserved**	Reserved.
[10:8]	**PRIGROUP**	**Interrupt Priority Grouping** This field determines the Split Of Group priority from subpriority,
[7:3]	**Reserved**	Reserved.
[2]	**SYSRESETREQ**	**System Reset Request** Writing This Bit to 1 Will Cause A Reset Signal To Be Asserted To The Chip And Indicate A Reset Is Requested This bit is write only and self-cleared as part of the reset sequence.
[1]	**VECTCLRACTIVE**	**Exception Active Status Clear Bit** Setting This Bit To 1 Will Clears All Active State Information For Fixed And Configurable Exceptions This bit is write only and can only be written when the core is halted. **Note:** It is the debugger's responsibility to re-initialize the stack.
[0]	**VECTRESET**	Reserved.

PRIGROUP	Binary Point	Group Priority Bits	Subpriority Bits	Number Of Group Priorities	Subpriorities
0b000	bxxxxxxx.y	[7:1]	[0]	128	2
0b001	bxxxxxx.yy	[7:2]	[1:0]	64	4
0b010	bxxxxx.yyy	[7:3]	[2:0]	32	8
0b011	bxxxx.yyyy	[7:4]	[3;0]	16	16
0b100	bxxx.yyyyy	[7:5]	[4:0]	8	32
0b101	bxx.yyyyyy	[7:6]	[5:0]	4	64
0b110	bx.yyyyyyy	[7]	[6:0]	2	128
0b111	b.yyyyyyyy	None	[7:0]	1	256

Table 6.2-10 Priority Grouping

System Control Register (SCR)

Register	Offset	R/W	Description	Reset Value
SCR	SCS_BA+0xD10	R/W	System Control Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved			**SEVONPEND**	**Reserved**	**SLEEPDEEP**	**SLEEPONEXIT**	**Reserved**

Bits	Description	
[31:5]	**Reserved**	Reserved.
[4]	**SEVONPEND**	**Send Event on Pending** 0 = Only enabled interrupts or events can wake up the processor, while disabled interrupts are excluded. 1 = Enabled events and all interrupts, including disabled interrupts, can wake up the processor. When an event or interrupt enters pending state, the event signal wakes up the processor from WFE. If the processor is not waiting for an event, the event is registered and affects the next WFE. The processor also wakes up on execution of an SEV instruction or an external event.
[3]	**Reserved**	Reserved.
[2]	**SLEEPDEEP**	**Processor Deep Sleep and Sleep Mode Selection** Control Whether the Processor Uses Sleep Or Deep Sleep as its Low Power Mode. 0 = Sleep. 1 = Deep sleep.
[1]	**SLEEPONEXIT**	**Sleep-on-exit Enable Control** This bit indicate Sleep-On-Exit when Returning from Handler Mode to Thread Mode. 0 = Do not sleep when returning to Thread mode. 1 = Enter sleep, or deep sleep, on return from an ISR to Thread mode. **Note:** Setting this bit to 1 enables an interrupt driven application to avoid returning to an empty main application.
[0]	**Reserved**	Reserved.

System Handler Priority Register 2 (SHPR2)

Register	Offset	R/W	Description	Reset Value
SHPR2	SCS_BA+0xD1C	R/W	System Handler Priority Register 2	0x0000_0000

31	30	29	28	27	26	25	24
PRI_11		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_11**	**Priority of System Handler 11 – SVCall** “0” denotes the highest priority and “3” denotes the lowest priority.
[29:0]	**Reserved**	Reserved.

System Handler Priority Register 3 (SHPR3)

Register	Offset	R/W	Description	Reset Value
SHPR3	SCS_BA+0xD20	R/W	System Handler Priority Register 3	0x0000_0000

31	30	29	28	27	26	25	24
PRI_15		**Reserved**					
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
PRI_14		**Reserved**					
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Reserved							

Bits	Description	
[31:30]	**PRI_15**	**Priority of System Handler 15 – SysTick** "0" denotes the highest priority and "3" denotes the lowest priority.
[29:24]	**Reserved**	Reserved.
[23:22]	**PRI_14**	**Priority of System Handler 14 – PendSV** "0" denotes the highest priority and "3" denotes the lowest priority.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex®-M0 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT) and 48 MHz internal high speed RC oscillator (HIRC) to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.

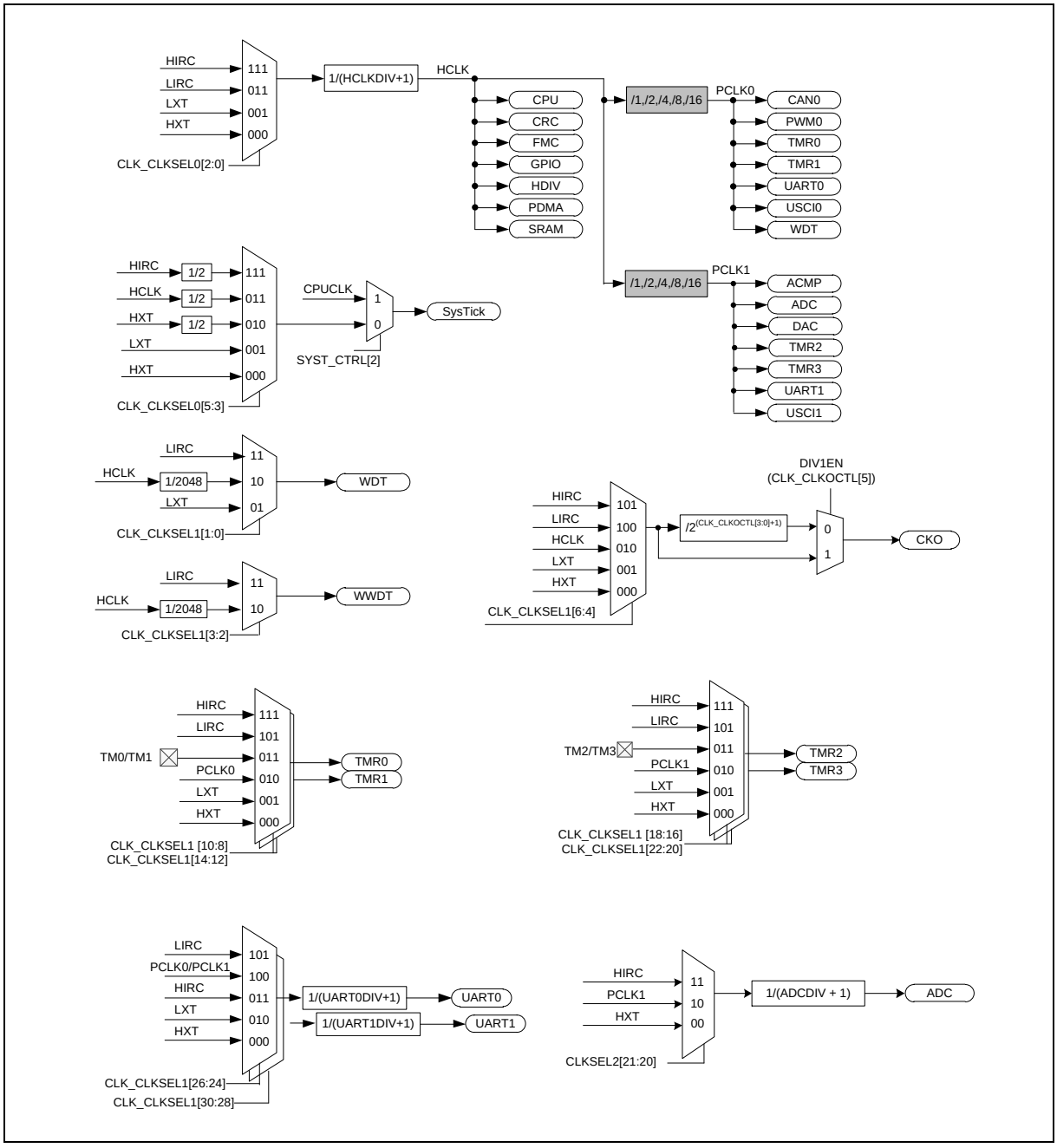


Figure 6.3-1 Clock Generator Global View Diagram

6.3.2 Clock Generator

The clock generator consists of 4 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- 48 MHz internal high speed RC oscillator (HIRC)
- 38.4 kHz internal low speed RC oscillator (LIRC)

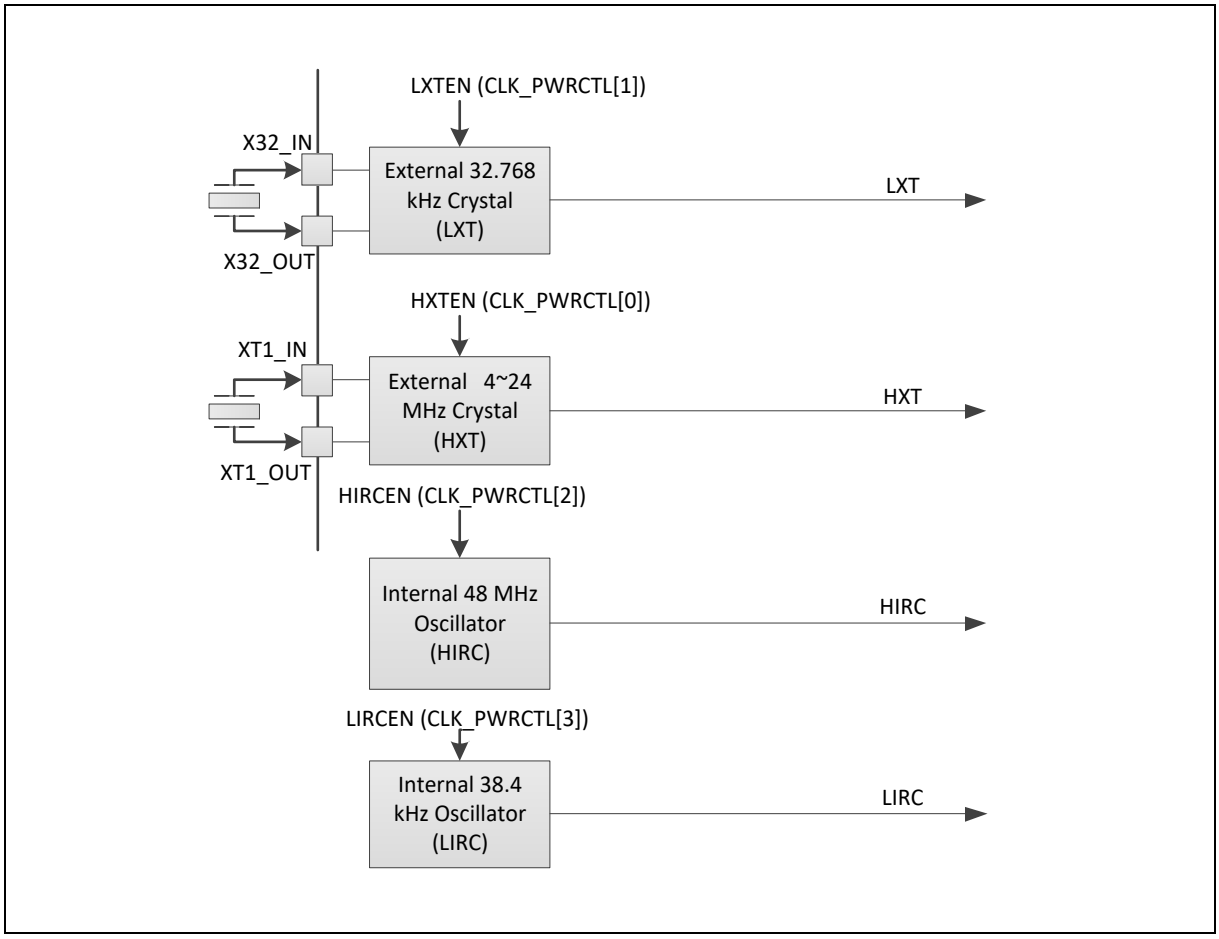


Figure 6.3-2 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 4 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-3

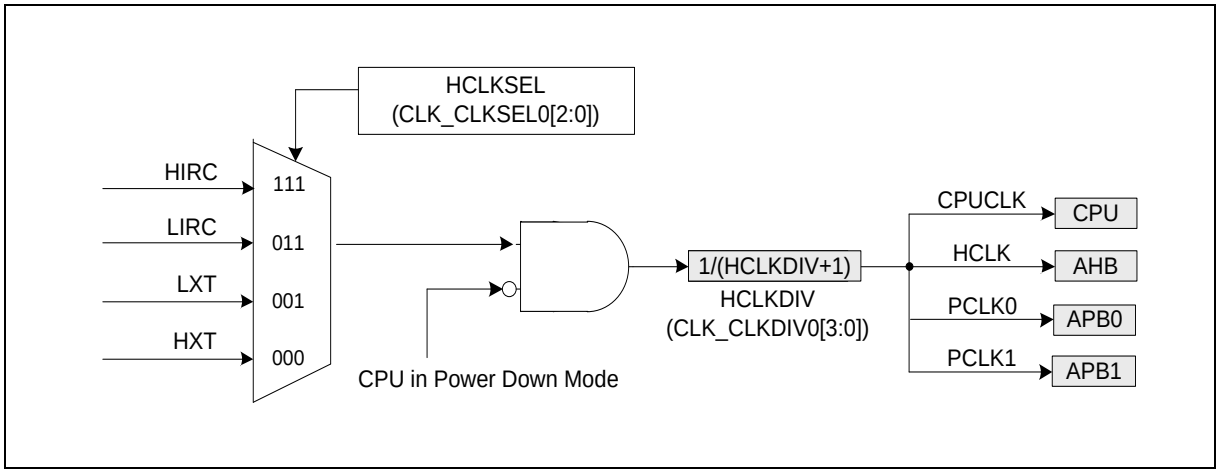


Figure 6.3-3 System Clock Block Diagram

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIEN (CLK_CLKDCTL[5]) is set to 1. User can trying to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

The HXT clock stop detect and system clock switch to HIRC procedure is shown in Figure 6.3-4.

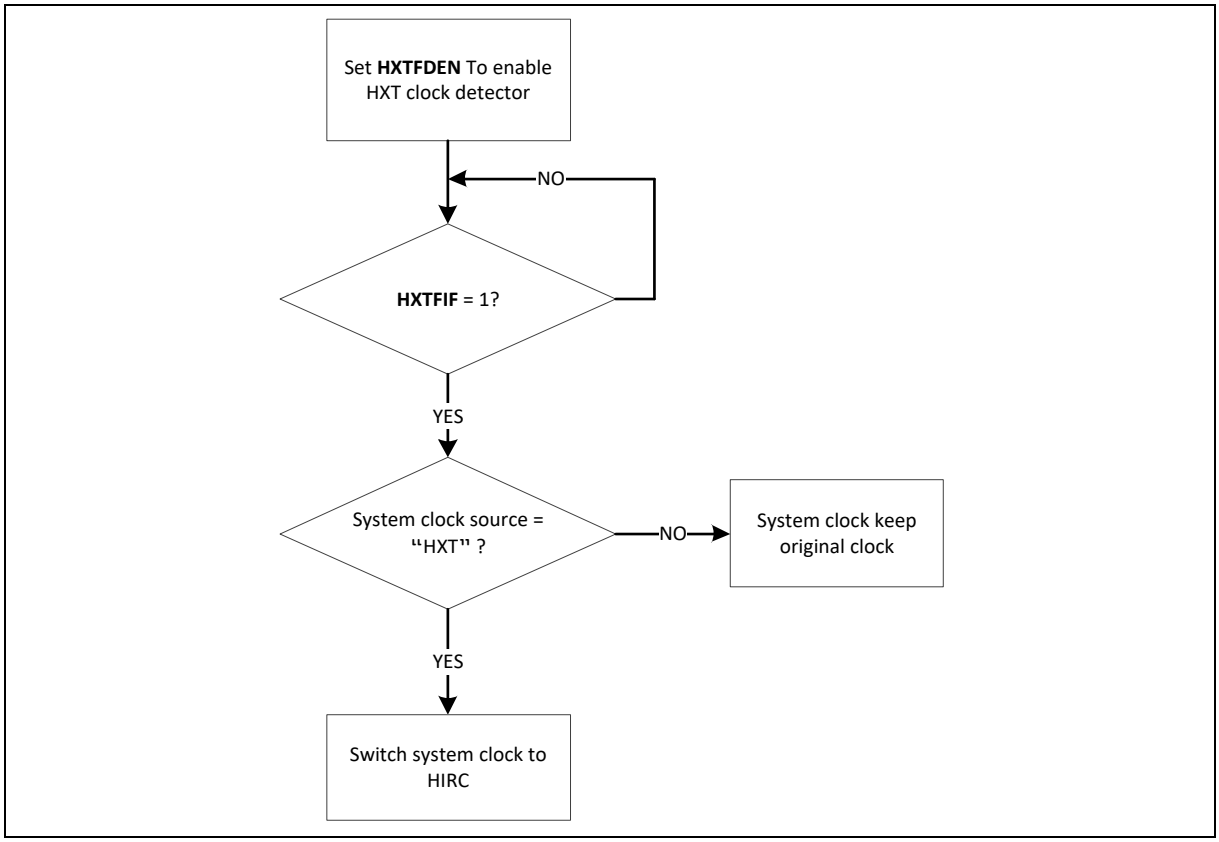


Figure 6.3-4 HXT Stop Protect Procedure

The clock source of SysTick in Cortex®-M0 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-5.

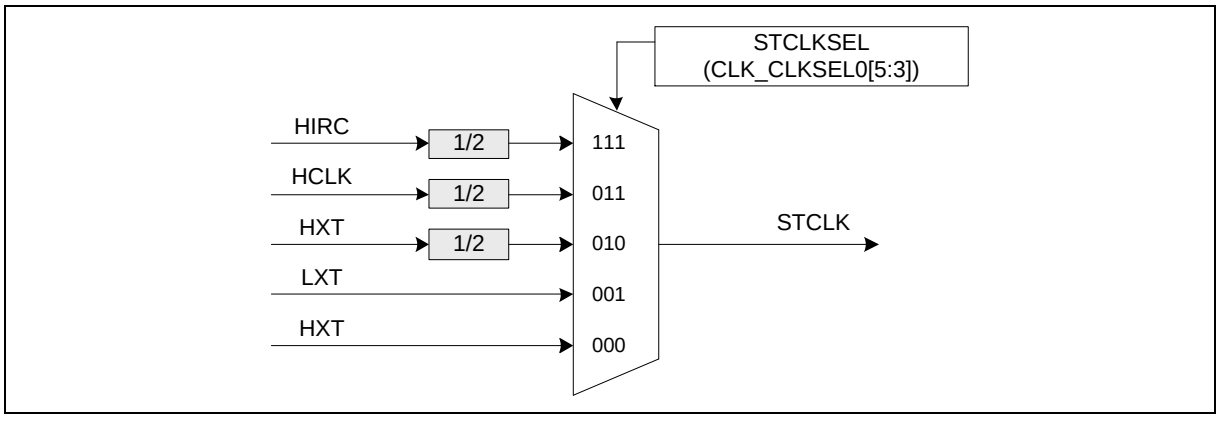


Figure 6.3-5 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

The peripherals clock has different clock source switch setting, which depends on the different peripheral.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

For theses clocks, which still keep active, are listed below:

- Clock Generator
  - 38.4 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider which is composed by16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

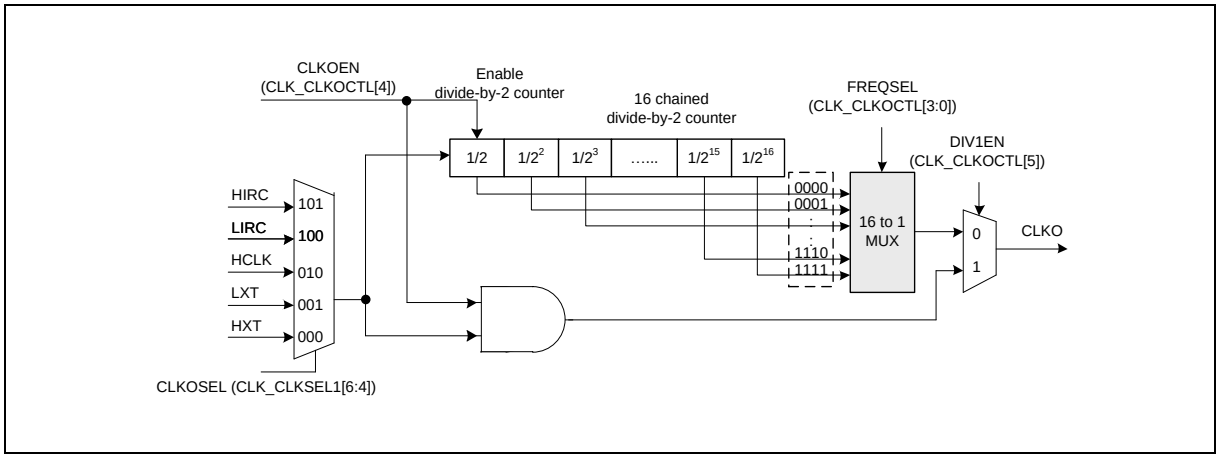


Figure 6.3-6 Clock Output Block Diagram

6.4 Flash Memory Controller (FMC)

6.4.1 Overview

This chip is equipped with 16/32 Kbytes on-chip embedded Flash. A User Configuration block is provided for system initialization. A loader ROM (LDROM) is used for In-System-Programming (ISP) function. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without the chip reset after the embedded Flash is updated.

6.4.2 Features

- Supports 16/32 Kbytes application ROM (APROM).
- Supports 512 bytes page size for 16/32 Kbytes Flash.
- Supports 2 Kbytes loader ROM (LDROM).
- Supports configurable Data Flash size to share with APROM.
- Supports 12 bytes User Configuration block to control system initialization.
- Supports 512 bytes page erase for all embedded Flash.
- Supports CRC-32 checksum calculation function.
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory.

6.5 General Purpose I/O (GPIO)

6.5.1 Overview

This chip has up to 26 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 26 pins are arranged in 4 ports named as PA, PB, PC, PD. PA has 6 pins on port, PB has 4 pins on port. PC and PD have 8 pins on port. Each 26 pins is independent and has the corresponding register bits to control the pin mode function and data, except GPA[3]. GPA[3] is a input pin.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Each I/O pin has a very weakly individual pull-up resistor which is about 50 kΩ. Please refer to the M0A23U Datasheet for detailed pin operation voltage information about V_{DD} electrical characteristics.

6.5.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up control
- Enabling the pin interrupt function will also enable the wake-up function

6.6 PDMA Controller (PDMA)

6.6.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. The PDMA controller has a total of 5 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.6.2 Features

- Supports 5 independently configurable channels
- Selectable 2 level of priority (fixed priority or round-robin priority)
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and UART, USCI, ADC, PWM, DAC and TIMER request
- Supports Scatter-Gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on channel 0 and channel1

6.7 Timer Controller (TMR)

6.7.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

6.7.2 Features

6.7.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports internal capture triggered while internal ACMP output signal and LIRC transition
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger PWM, ADC, PDMA function
- Supports Inter-Timer trigger mode

6.8 Watchdog Timer (WDT)

6.8.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.8.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 416us ~ 27.3 s if WDT_CLK = 38.4 kHz (LIRC).
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC or LXT.

6.9 Window Watchdog Timer (WWDT)

6.9.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

6.9.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.10 PWM Generator and Capture Timer (PWM)

6.10.1 Overview

The chip provides one PWM generator. PWM supports 6 channels of PWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit PWM counter with 16-bit comparator. The PWM counter supports up, down and up-down counter types. PWM uses comparator compared with counter to generate events. These events are used to generate PWM pulse, interrupt and trigger signal for ADC to start conversion.

The PWM generator supports two standard PWM output modes: Independent mode and Complementary mode. They have different architecture. In Complementary mode, there are two comparators to generate various PWM pulse with 12-bit dead-time generator. For PWM output control unit, it supports polarity output, independent pin mask and brake functions.

The PWM generator also supports input capture function to latch PWM counter value to the corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.10.2 Features

6.10.2.1 PWM Function Features

- Supports maximum clock frequency up to 48 MHz
- Supports up to one PWM module and provides 6 output channels
- Supports independent mode for PWM output/Capture input channel
- Supports complementary mode for 3 complementary paired PWM output channel
  - Dead-time insertion with 12-bit resolution
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution PWM counter
  - Up, down and up-down counter operation type
- Supports mask function and tri-state enable for each PWM pin
- Supports brake function
  - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
  - Noise filter for brake source from pin
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM counter matches 0, period value or compared value
  - Brake condition happened
- Supports trigger ADC on the following events:
  - PWM counter matches 0, period value or compared value

6.10.2.2 Capture Function Features

- Supports up to 6 capture input channels with 16-bit resolution
- Supports rising or falling capture condition

- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for PWM all channels

6.11 UART Interface Controller (UART)

6.11.1 Overview

The chip provides two channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports eleven types of interrupts. The UART controller supports flow control function. The UART controller also supports LIN, IrDA SIR, RS-485, and Single-wire function modes and auto-baud rate measuring function.

6.11.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY (UART_TOUT[15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - Supports 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
  - Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
  - Supports for 3/16 bit duration for normal mode
- Supports LIN function mode
  - Supports LIN master/slave mode
  - Supports programmable break generation function for transmitter
  - Supports break detection function for receiver
  - Supports LIN slave header time-out detection function
  - Supports LIN response time-out detection function
  - Supports LIN wake-up function
- Supports RS-485 function mode
  - Supports RS-485 9-bit mode
  - Supports hardware or software enables to program nRTS pin to control RS-485

transmission direction

- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0/ UART1	USCI-UART
FIFO	16 Bytes	TX: 1 Byte RX: 2 Bytes
Auto Flow Control (CTS/RTS)	√	√
IrDA	√	-
LIN	√	-
RS-485 Function Mode	√	√
nCTS Wake-up	√	√
Imcoming Data Wake-up	√	√
Received Data FIFO reached threshold Wake-up	√	-
RS-485 Address Match (AAD mode) Wake-up	√	-
Auto-Baud Rate Measurement	√	√
STOP Bit Length	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√
Stick Bit	√	-
Note: √= Supported		

Table 6.11-1 NuMicro® M0A23U Series UART Features

6.12 USCI - Universal Serial Control Interface Controller (USCI)

6.12.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.12.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.13 USCI – UART Mode

6.13.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter being independent, frames can start at different points in time for transmission and reception.

The UART controller also provides auto flow control. There are two conditions to wake-up the system.

6.13.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection by built-in capture event of baud rate generator
- Supports PDMA capability
- Supports Wake-up function (Data and nCTS Wakeup Only)

6.14 USCI - SPI Mode

6.14.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as Master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in Master and Slave mode are shown below.

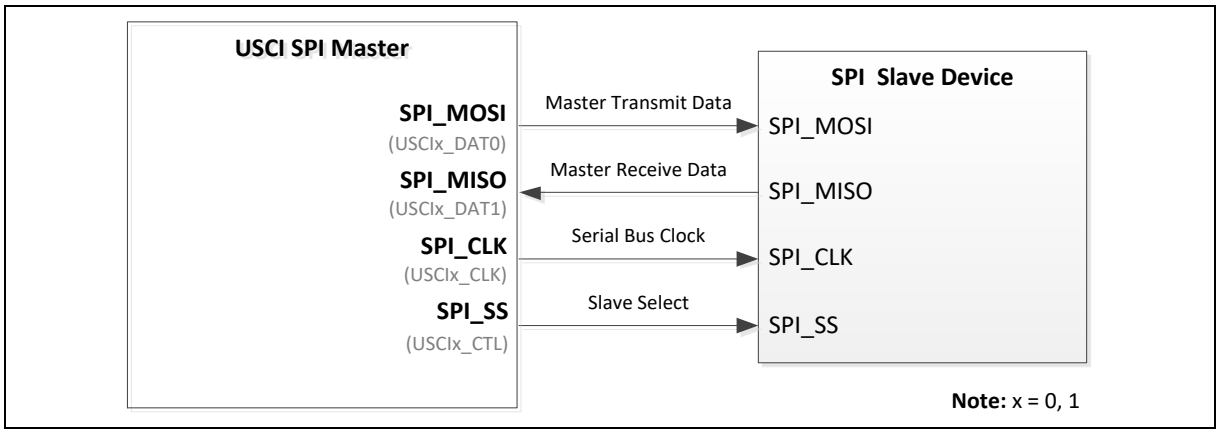


Figure 6.14-1 SPI Master Mode Application Block Diagram

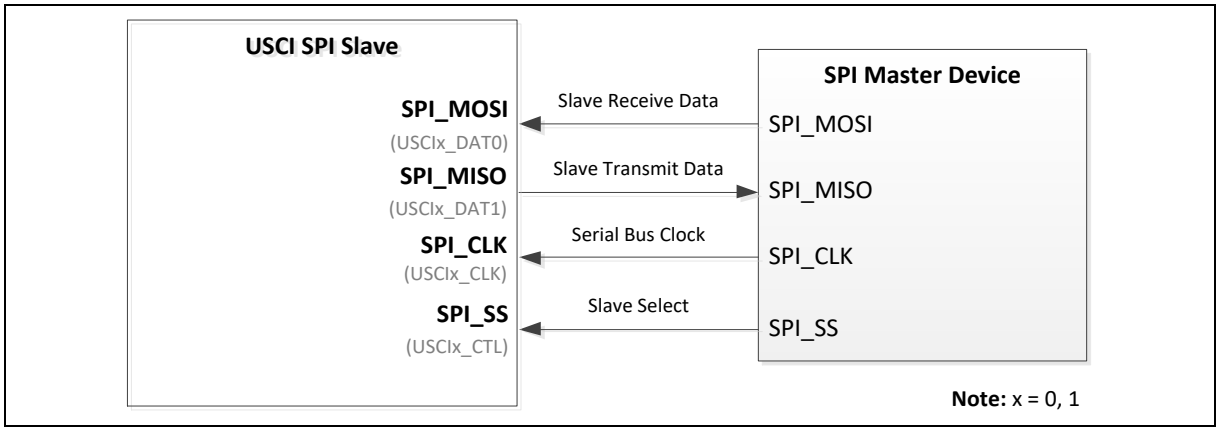


Figure 6.14-2 SPI Slave Mode Application Block Diagram

6.14.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence
- Supports Word Suspend function

- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.15 USCI - I²C Mode

6.15.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.15-1 for more detailed I²C BUS Timing.

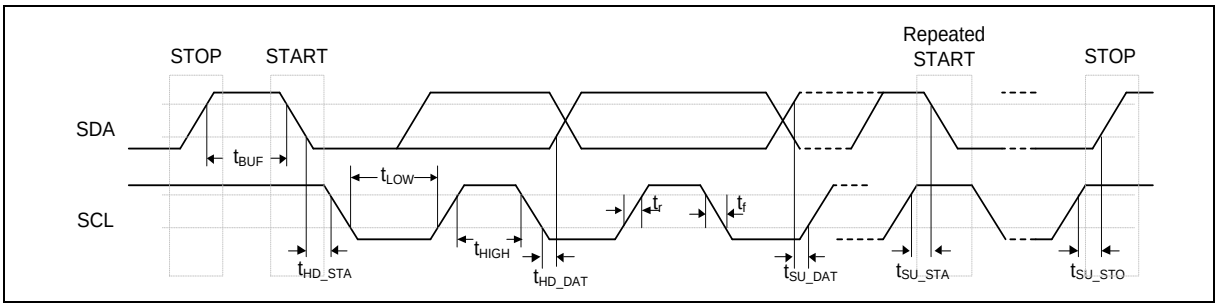


Figure 6.15-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enabling this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.15.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kBit/s) or in fast mode (up to 400 kBit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by data toggle or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.16 Controller Area Network (CAN)

6.16.1 Overview

The Bosch CAN (is named as C_CAN) consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1 MBit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

6.16.2 Features

- Supports CAN protocol version 2.0 part A and B
- Bit rates up to 1 MBit/s
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Objects)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Programmable loop-back mode for self-test operation
- 16-bit module interfaces to the AMBA APB bus
- Supports wake-up function

6.17 CRC Controller (CRC)

6.17.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32 settings.

6.17.2 Features

- Supports four common polynomials CRC-CCITT, CRC-8, CRC-16, and CRC-32
  - CRC-CCITT: $X^{16} + X^{12} + X^5 + 1$
  - CRC-8: $X^8 + X^2 + X + 1$
  - CRC-16: $X^{16} + X^{15} + X^2 + 1$
  - CRC-32: $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.18 Hardware Divider (HDIV)

6.18.1 Overview

The hardware divider (HDIV) is useful to the high performance application. The hardware divider is a signed, integer divider with both quotient and remainder outputs.

6.18.2 Features

- Signed (two's complement) integer calculation
- 32-bit dividend with 16-bit divisor calculation capacity
- 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
- Divided by zero warning flag
- Write divisor to trigger calculation

6.19 Analog-to-Digital Converter (ADC)

6.19.1 Overview

The chip contains one 12-bit successive approximation analog-to-digital converter (SAR A/D converter) with twenty one input channels. The A/D converter supports four operation modes: Single, Burst, Single-cycle Scan and Continuous Scan mode. The A/D converter can be started by software, external pin, timer0~3 overflow pulse trigger and PWM trigger.

6.19.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of V_{DD} pin).
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 17 single-end analog input channels or 8 differential analog input channels
- Maximum ADC peripheral clock frequency is 16 MHz
- Up to 800 kSPS sampling rate
- Configurable ADC internal sampling time
- Four operation modes:
  - Single mode: A/D conversion is performed one time on a specified channel.
  - Burst mode: A/D converter samples and converts the specified single channel and sequentially stores the result in FIFO.
  - Single-cycle Scan mode: A/D conversion is performed only one cycle on all specified channels with the sequence from the smallest numbered channel to the largest numbered channel.
  - Continuous Scan mode: A/D converter continuously performs Single-cycle Scan mode until software stops A/D conversion.
- An A/D conversion can be started by:
  - Software Write 1 to ADST bit
  - External pin (STADC)
  - Timer 0~3 overflow pulse trigger
  - PWM trigger with optional start delay period
- Each conversion result is held in data register of each channel with valid and overrun indicators.
- Conversion result can be compared with specified value and user can select whether to generate an interrupt when conversion result matches the compare register setting.
- 4 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}), internal reference voltage and DAC0 output
- Support PDMA transfer mode.

Note 1: ADC sampling rate = (ADC peripheral clock frequency) / (total ADC conversion cycle)

Note 2: If the internal channel for temperature sensor is active, the minimum time of sample stage should be T_{TEMP_ADC}. Please refer to section 8.5.7 in the relative Datasheet for detailed information.

Note 3: If the internal channel for band-gap voltage is active, the minimum time of sample stage should be T_{VBG_ADC}. Please refer to section 8.2 in the relative Datasheet for detailed information.

6.20 Digital to Analog Converter (DAC)

6.20.1 Overview

The DAC module is a 5-bit, voltage output digital-to-analog converter. It can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.20.2 Features

- Supports one 5-bit 100 kSPS voltage type DAC
- Analog output voltage range: 0~AV_{DD} (voltage of V_{DD} pin)
- Reference voltage from internal reference voltage V_{REF} pin or AV_{DD}.
- DAC maximum conversion updating rate 100 kSPS
- Rail to rail settle time 10us
- Supports software and timer0~3 trigger to start DAC conversion.
- Supports PDMA mode.

6.21 Analog Comparator Controller (ACMP)

6.21.1 Overview

The chip provides two comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

6.21.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of V_{DD} pin)
- Up to two rail-to-rail analog comparators
- Supports hysteresis function
  - Support programmable hysteresis window: 0mV and 30mV
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 3 multiplexed I/O pins at positive sources:
    - ACMP0_P0, Comparator Reference Voltage (CRV), and DAC0 output
  - 5 negative sources:
    - ACMP0_N0, ACMP0_N1, ACMP0_N2, ACMP0_N3
    - Comparator Reference Voltage (CRV)
- ACMP1 supports
  - 3 multiplexed I/O pins at positive sources:
    - ACMP1_P0, Comparator Reference Voltage (CRV), and DAC0 output
  - 5 negative sources:
    - ACMP1_N0, ACMP1_N1, ACMP1_N2, ACMP1_N3
    - Comparator Reference Voltage (CRV)
- Shares one ACMP interrupt vector for all comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for PWM
- Supports window compare mode and window latch mode

6.22 Peripherals Interconnection

6.22.1 Overview

Some peripherals have interconnections which allow autonomous communication or synchronous action between peripherals without needing to involve the CPU. Peripherals interact without CPU saves CPU resources, reduces power consumption, operates with no software latency and fast response.

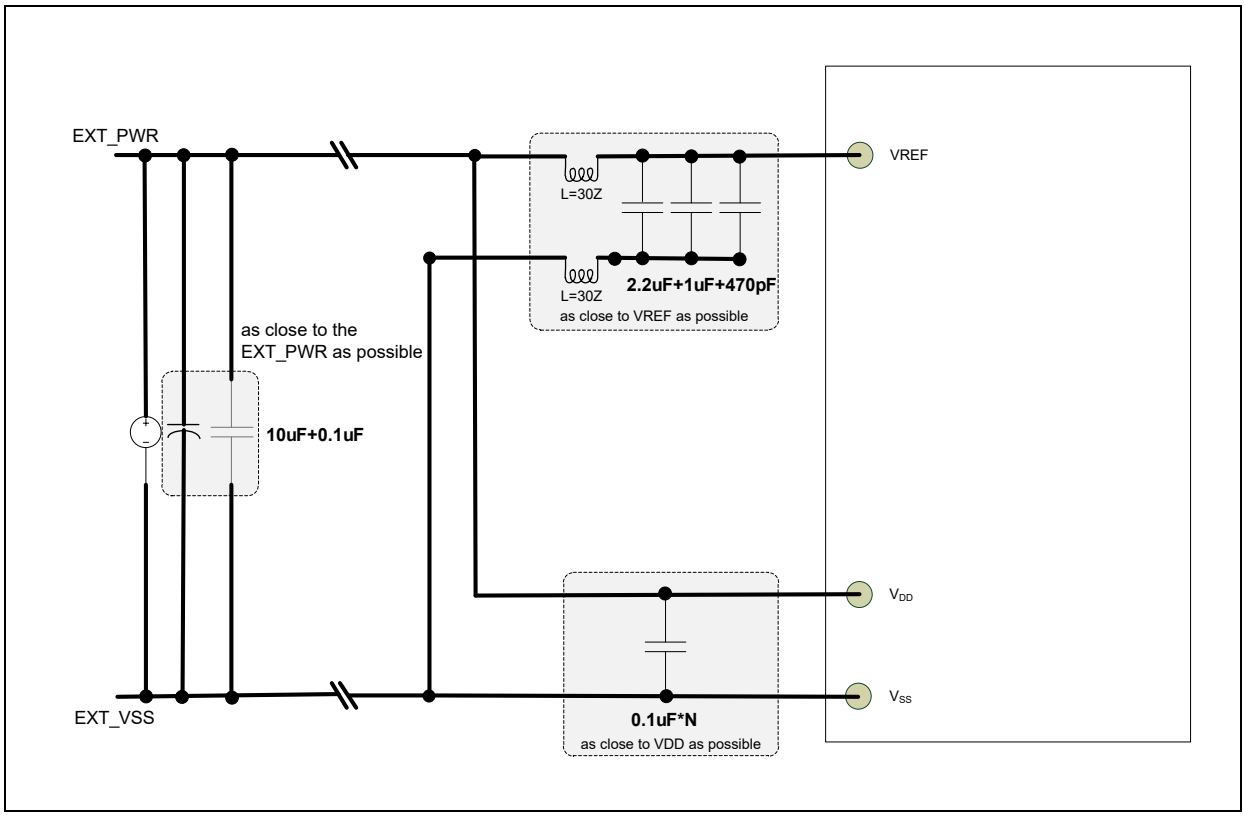
6.22.2 Peripherals Interconnect Matrix Table

Source	Destination			
	ADC	DAC	PWM	Timer
LIRC	-	-	-	4
PWM	1	-	-	-
Timer	1	2	3	5

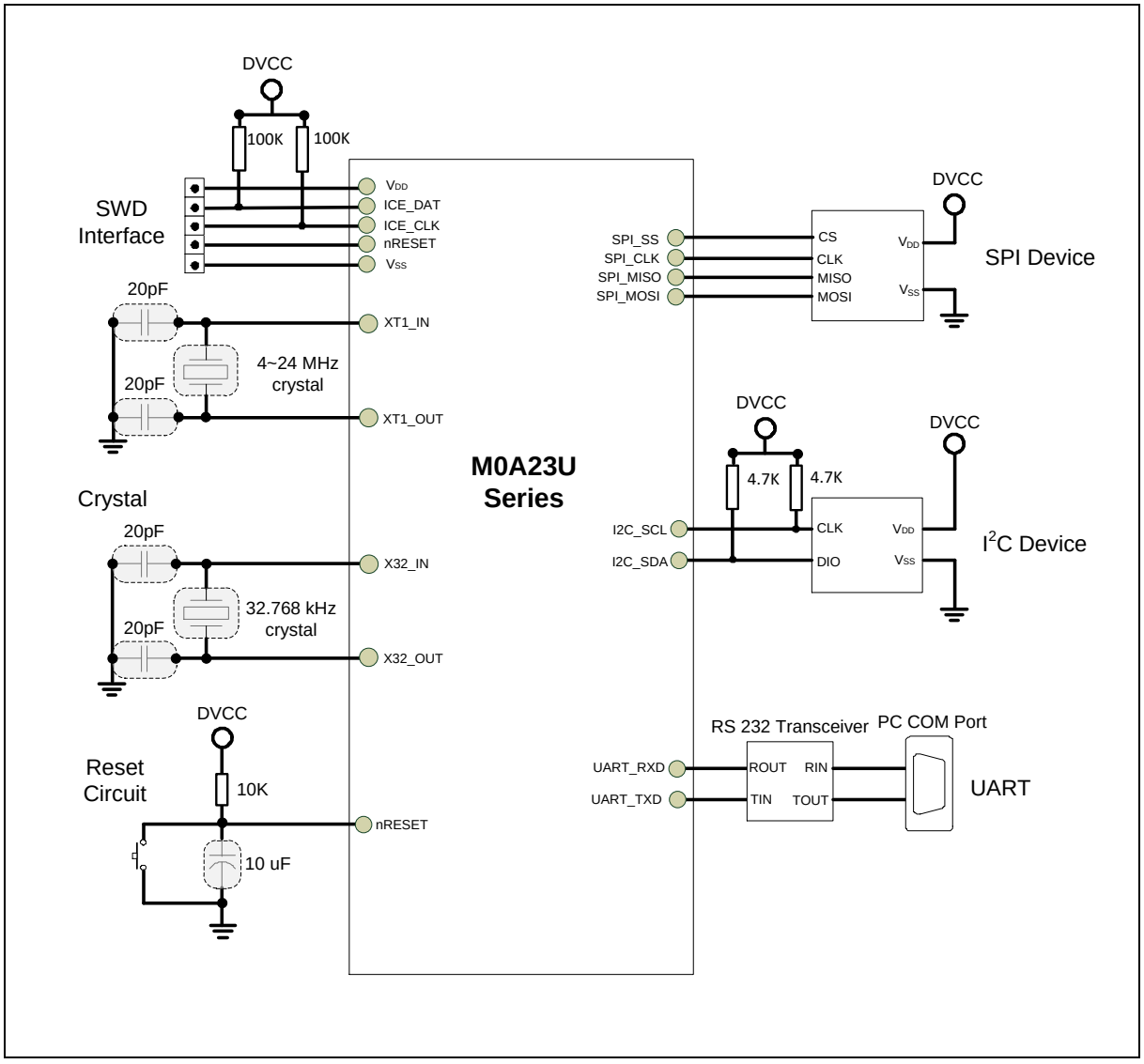
Table 6.22-1 Peripherals Interconnect Matrix Table

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



8 ELECTRICAL CHARACTERISTICS

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
V_{IN}	Input voltage on any other pin[*2]	V_{SS}-0.3	6.5	V

Note:

1. All main power (V_{DD}) and ground (V_{SS}) pins must be connected to the external power supply.
2. Refer to Table 8.1-2 for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>V_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	125	℃
T_J	Operating junction temperature	-40	-	135	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 20-pin SSOP(4.4x6.5 mm)	-	38	-	℃/Watt
	Thermal resistance junction-ambient 28-pin TSSOP(4.4x9.7 mm)	-	30	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic Discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static Latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical Fast Transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-6000	-	+6000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[*3]	-150	-	+150	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
20-pin SSOP(4.4x6.5 mm) [*1]	MSL 3
28-pin TSSOP(4.4x9.7 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity (MSL)

8.1.6 Soldering Profile

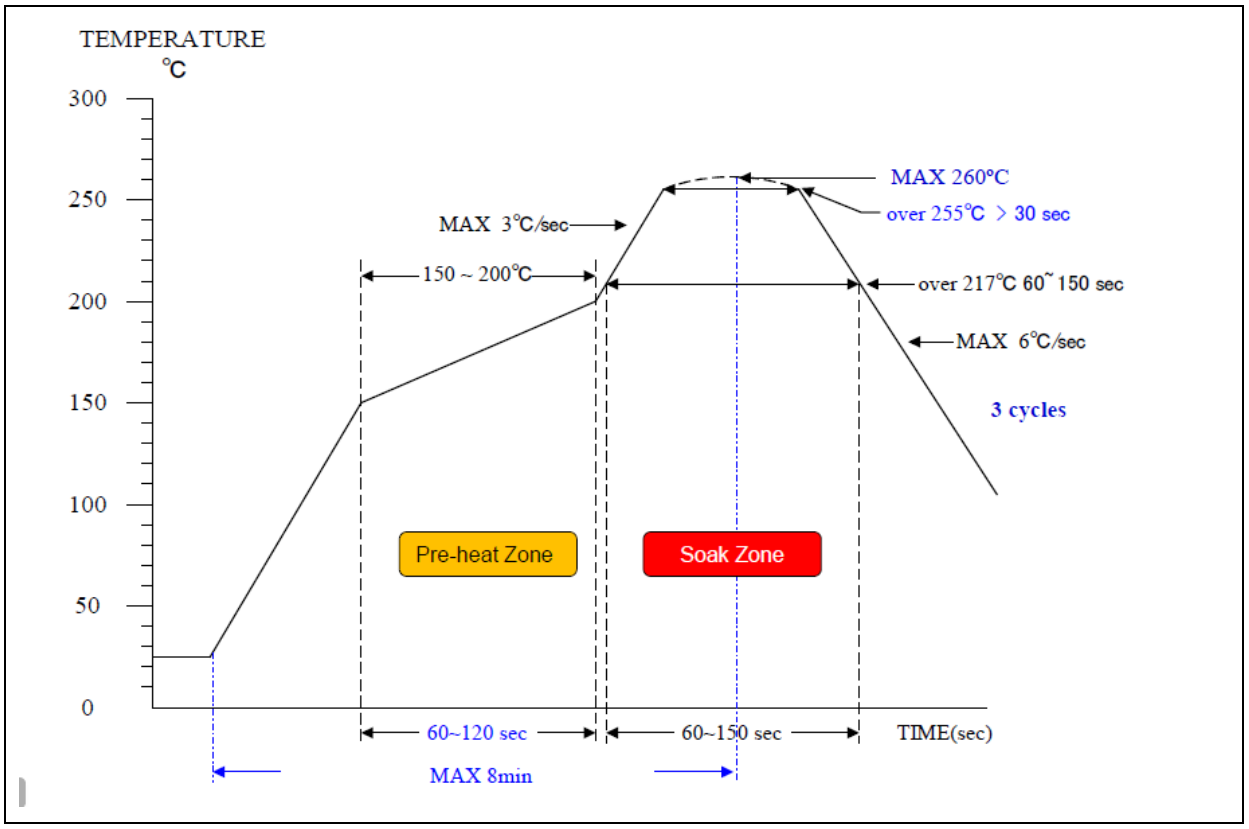


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 2.4 ~ 5.5V, T_A = 25°C, HCLK = 48 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	48	MHz	
V_{DD}	Operation voltage	2.4	-	5.5	V	
V_{REF}	Analog reference voltage	2.4	-	V_{DD}		
V_{LDO}	LDO output voltage	-	1.8	-		
V_{BG}	Band-gap voltage	1.174	1.210	1.246	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	12	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	1			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	150	200	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	3	-	µC	V_{DD} = 2.4 V, T_A = 125 °C, I_{RUSH} = 150 mA for 15 µs

Note:

1. It is recommended to power V_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 1 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 2.4 ~ 5.5 V unless otherwise specified.
- V_{DD}
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	
I_{DD_RUN}	Normal run mode, executed from Flash, all peripherals disable HIRC, HXT, LIRC or LXT clock	48 MHz(HIRC48M)	8.89	9.79	9.83	10.36	mA
		24 MHz(HIRC48M/2)	5.41	5.71	6.00	6.80	
		24 MHz(HXT24M)	5.39	5.90	6.41	7.40	
		12 MHz(HXT24M/2)	3.42	3.80	4.26	5.20	
		4 MHz(HXT24M/6)	2.06	2.37	2.78	3.67	
		38.4 KHz	0.12	0.14	0.33	1.03	
		32.768 KHz	0.12	0.14	0.33	1.03	
	Normal run mode, executed from Flash, all peripherals enable HIRC, HXT, LIRC or LXT clock	48 MHz(HIRC48M)	16.62	18.04	18.22	18.97	
		24 MHz(HIRC48M/2)	9.44	9.99	10.39	11.28	
		24 MHz(HXT24M)	8.86	9.58	10.25	11.37	
		12 MHz(HXT24M/2)	5.15	5.65	6.20	7.19	
		4 MHz(HXT24M/6)	2.63	2.98	3.43	4.34	
		38.4 KHz	0.13	0.15	0.35	1.05	
		32.768 KHz	0.13	0.15	0.35	1.05	

Note:

1. When analog peripheral blocks such as, DAC, ADC, ACMP, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	

I_{DD_IDLE}	Idle mode, all peripherals disable HIRC, HXT, LIRC or LXT clock	48 MHz(HIRC48M)	2.77	2.90	3.15	3..89	mA
		24 MHz(HIRC48M/2)	2.10	2.20	2.45	3.17	
		24 MHz(HXT24M)	2.10	2.41	2.83	3.71	
		12 MHz(HXT24M/2)	1.76	2.07	2.47	3.34	
		4 MHz(HXT24M/6)	1.50	1.80	2.19	3.06	
		38.4 KHz	0.12	0.14	0.33	1.02	
		32.768 KHz	0.12	0.14	0.33	1.02	
	Idle mode, all peripherals enable HIRC, HXT, LIRC or LXT clock	48 MHz(HIRC48M)	10.26	10.88	11.36	12.25	
		24 MHz(HIRC48M/2)	5.85	6.19	6.54	7.36	
		24 MHz(HXT24M)	5.59	6.13	6.69	7.71	
		12 MHz(HXT24M/2)	3.51	3.93	4.41	5.35	
		4 MHz(HXT24M/6)	2.09	2.41	2.83	3.73	
		38.4 KHz	0.13	0.15	0.34	1.04	
		32.768 KHz	0.13	0.15	0.34	1.04	

Note:

1. When analog peripheral blocks such as, DAC, ADC, ACMP, , HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1]	LIRC	Typ[*2]	Max[*3][*4]			Unit
		32.768 kHz	38.4 kHz	T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 125 °C	
I_{DD_PD}	Power-down mode, all peripherals disable	-	-	11	19	198	847	µA
	Power-down mode, WDT/Timer/UART enable and run	V	-	13	21	201	856	
	Power-down mode, WDT/Timer enable and run	-	V	13	21	202	860	
	Power-down mode, WDT/Timer/UART enable and run, WDT use LIRC, UART/Timer use LXT	V	V	14	23	204	865	

Note:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L1 gain level.
2. V_{DD} = 3.3V, LVR17 enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as DAC, ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 48 MHz, $f_{PCLK0, 1} = f_{HCLK}$.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA	292	uA
ISP	0	
HDIV	53	
CRC	56	
SRAM0	65	
WDT	121	
TMR0	298	
TMR1	251	
TMR2	292	
TMR3	258	
CLKO	61	
ACMP01	358	
UART0	879	
UART1	935	
ADC	483	
USCI0	487	
USCI1	510	
DAC	47	
PWM0	1235	

Note:
1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 48 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit

t_{WU_IDLE}	Wakeup from IDLE mode	5	6	cycles
t_{WU_NPD}[*1][*2]	Wakeup from normal Power-down mode	65.77	-	
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	1.7	-	
t_{ET_IDLE}	Enter to IDLE mode	2	-	cycles
t_{ET_NPD}	Enter to normal Power-down mode	0.3	-	

Note:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.

Table 8.3-5 Low-power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PA0~PA2, PA4, PA5, PB4~PB7 and PC0~PC7 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	$0.3*V_{DD}$	V	
	Input low voltage (TTL trigger)	0	-	0.8		V_{DD} = 4.5 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 2.4 V
V_{IH}	Input high voltage (Schmitt trigger)	$0.7*V_{DD}$	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 5.5 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		0.8	-	V_{DD}		V_{DD} = 2.4 V
V_{HY}[*1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[*2]	Input leakage current	-1	-	1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1	-	1		$V_{DD} < V_{IN} < 5$ V, Open-drain or input only mode on any other 5v tolerance pins
R_{PU}[*1]	Pull up resistor	84.12	-	87.26	kΩ	V_{DD} = 5.5V

Note:
1. Guaranteed by characterization result, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	-561.14	-	-606.28	μA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-97.30	-	-108.50	μA	V_{DD} = 3.0 V V_{IN} = (V_{DD} - 0.4) V
	Source current for push-pull mode and high level	-22.85	-	-28.14	mA	V_{DD} = 4.5 V V_{IN} = (V_{DD} - 0.4) V
		-5.95	-	-7.64	mA	V_{DD} = 3.0 V V_{IN} = (V_{DD} - 0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	12.73	-	15.26	mA	V_{DD} = 4.5 V V_{IN} = 0.45 V
		9.23	-	10.79	mA	V_{DD} = 3.0 V V_{IN} = 0.45 V
C_{IO}[*1]	I/O pin capacitance	-	5	-	pF	

Note:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	0	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	V_{DD}	V	
R_{RST}[*1]	Internal nRESET pull up resistor	42.2		45.7	kΩ	
t_{FR}[*1]	nRESET input filtered pulse time	-	24	-	μS	Normal run and Idle mode
		-	24	-		Fast wake up Power-down mode
		75	-	155		Power-down mode

Note:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[*1]	-	2[*1]	%	T_A = -40°C ~ +125 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[*1]	Operating current		471		µA	
T_S[*2]	Stable time		5		µS	T_A = -40°C ~ +125 °C, V_{DD} = 2.4 ~ 5.5V

Note:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator (HIRC) Characteristics

8.4.3 38.4 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC} [*2]	Oscillator frequnecy	-	38.4	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~125°C V_{DD}=2.4V~5.5V Without software calibration
I_{LRC}	Operating current		1.1		μA	V_{DD} = 3.3V
T_S	Stable time		500		μS	T_A=-40~125°C V_{DD}=2.4V~5.5V

Note:

1. Guaranteed by characterization, not tested in production.
2. The 38.4 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-2 38.4 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.4.4 External 4~24 MHz High Speed Crystal Resonator (HXT) characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
R_f	Internal feedback resister	-	1	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	-	250	600	μA	4 MHz, Gain = L0, C_L = 12.5 pF, DIP
		-	380	980		12 MHz, Gain = L1, C_L = 12.5 pF, DIP
		-	400	1050		16 MHz, Gain = L2, C_L = 12.5 pF, DIP
		-	750	2050		24 Mhz, Gain = L3, C_L = 12.5 pF, DIP 12 Mhz, Gain = L3, C_L = 12.5 pF, SMD
		-	1400	3500		16 MHz, Gain = L4, C_L = 12.5 pF, SMD
		-	2100	5100		24 MHz, Gain = L7, C_L = 12.5 pF, SMD
T_S	Stable time	-	2400	2700	μS	4 MHz, Gain = L0, C_L = 12.5 pF, DIP
		-	600	680		12 MHz, Gain = L1, C_L = 12.5 pF, DIP
		-	400	500		16 MHz, Gain = L2, C_L = 12.5 pF, DIP
		-	380	470		24 Mhz, Gain = L3, C_L = 12.5 pF, DIP
		-	2000	2200		12 Mhz, Gain = L3, C_L = 12.5 pF, SMD
		-	1900	2500		16 MHz, Gain = L4, C_L = 12.5 pF, SMD
		-	1400	1900		24 MHz, Gain = L7, C_L = 12.5 pF, SMD
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	0.7	1	-	V	

Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0, DIP
		-	-	50		Crystal @12 MHz, C_L = 12.5 pF, Gain = L1, DIP
		-	-	30		Crystal @16 MHz, C_L = 12.5 pF, Gain = L2, DIP
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L3, DIP
		-	-	120		Crystal @12 MHz, C_L = 12.5 pF, Gain = L3, SMD
		-	-	100		Crystal @16 MHz, C_L = 12.5 pF, Gain = L4, SMD
		-	-	50		Crystal @24 MHz, C_L = 12.5 pF, Gain = L7, SMD

Note:

1. Guaranteed by characterization, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

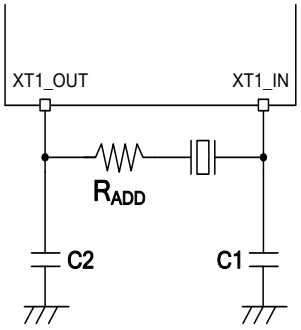


Table 8.4-4 External 4~24 MHz High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

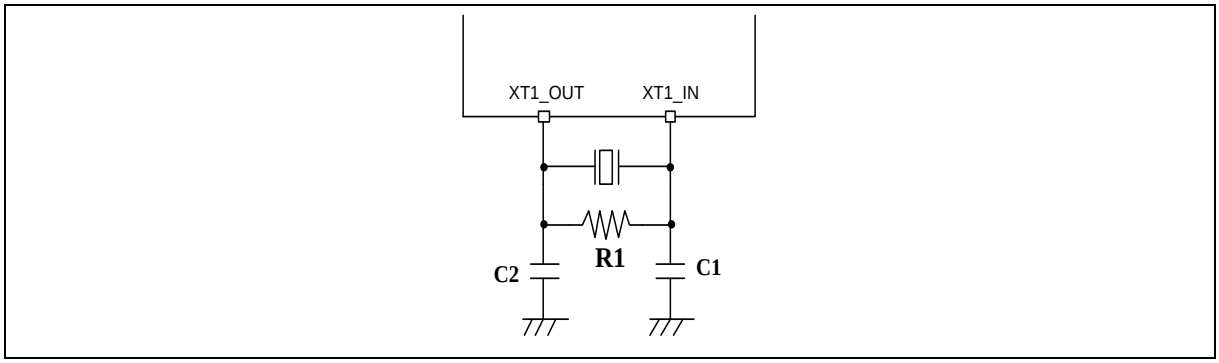
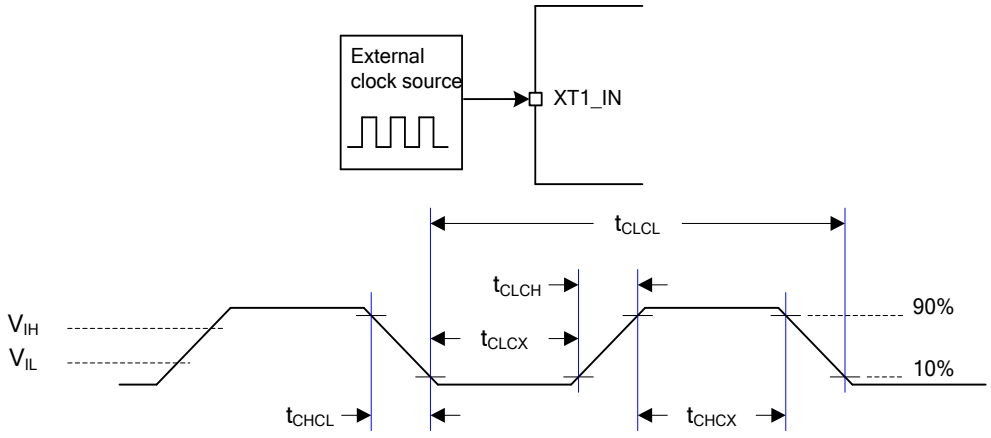


Figure 8.4-1 Typical Crystal Application Circuit

8.4.5 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by characterization, not tested in production.

Table 8.4-5 External 4~24 MHz High Speed Clock Input Signal

8.4.6 External 32.768 kHz Low Speed Crystal (LXT) characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operation voltage	2.4	-	5.5	V	
T_{LXT}	Temperature range	-40	-	125	°C	
R_f	Internal feedback resistor	-	15	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	-	0.55	4.4	µA	ESR=35 kΩ, C_L = 12.5 pF, Gain = L0
		-	0.65	4.6		ESR=35 kΩ, C_L = 12.5 pF, Gain = L1
		-	0.72	4.8		ESR=35 kΩ, C_L = 12.5 pF, Gain = L2
		-	0.9	5.2		ESR=70 kΩ, C_L = 12.5 pF, Gain = L3
		-	1	5.4		ESR=70 kΩ, C_L = 12.5 pF, Gain = L4
		-	1.1	5.6		ESR=70 kΩ, C_L = 12.5 pF, Gain = L5
		-	1.3	6.0		ESR=90 kΩ, C_L = 12.5 pF, Gain = L6
		-	1.6	6.6		ESR=90 kΩ, C_L = 12.5 pF, Gain = L7
Ts_{LXT}	Stable time	-	1	-	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	-	0.5	-	V	

Note:
1. Guaranteed by characterization, not tested in production.

Table 8.4-6 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	90	kΩ	Crystal @32.768 kHz

Table 8.4-7 External 32.768 kHz Low Speed Crystal Characteristics

8.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

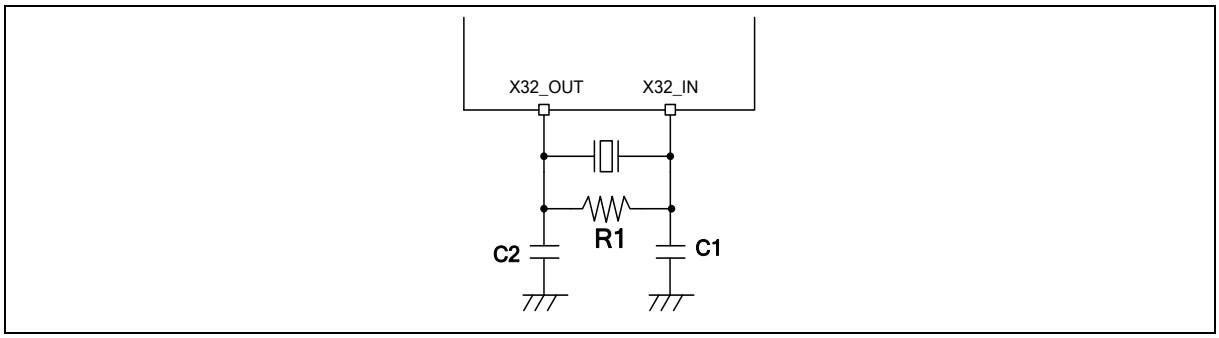
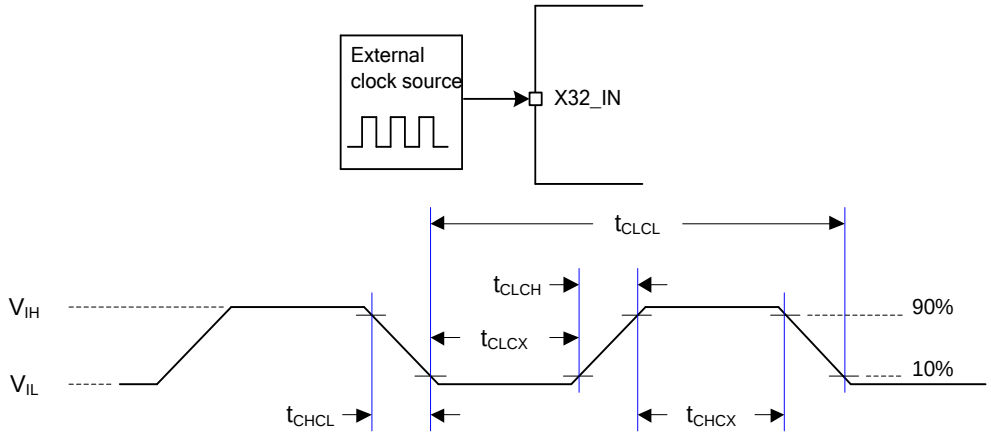


Figure 8.4-2 Typical 32.768 kHz Crystal Application Circuit

8.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1. Guaranteed by design, not tested in production

Table 8.4-8 External 32.768 kHz Low Speed Clock Input Signal

8.4.8 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	-	7.62	nS	C_L = 30 pF, V_{DD} >= 4.5 V
		-	5.32		C_L = 10 pF, V_{DD} >= 4.5 V
		-	12.69		C_L = 30 pF, V_{DD} >= 2.7 V
		-	9.33		C_L = 10 pF, V_{DD} >= 2.7 V
		-	13.87		C_L = 30 pF, V_{DD} >= 2.4V
		-	10.10		C_L = 10 pF, V_{DD} >= 2.4 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	-	6.89		C_L = 30 pF, V_{DD} >= 4.5 V
		-	4.25		C_L = 10 pF, V_{DD} >= 4.5 V
		-	11.90		C_L = 30 pF, V_{DD} >= 2.7 V
		-	7.47		C_L = 10 pF, V_{DD} >= 2.7 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	-	45.95	MHz	C_L = 30 pF, V_{DD} >= 4.5 V
		-	69.66		C_L = 10 pF, V_{DD} >= 4.5 V
		-	27.11		C_L = 30 pF, V_{DD} >= 2.7 V
		-	39.68		C_L = 10 pF, V_{DD} >= 2.7 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Note:

1. Guaranteed by characterization result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-9 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	2.4	-	5.5	V	
V_{LDO}	Output voltage	-	1.8	-	V	
T_A	Temperature	-40	-	125	℃	

Note:

1. It is recommended a 0.1μF bypass capacitor is connected between V_{DD} and the closest V_{SS} pin of the device.
2. For ensuring power stability, a 1μF capacitor must be connected between LDO_CAP pin and the closest V_{SS} pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	10	20	μA	V_{DD} = 3.3V
I_{LVR}[*1]	LVR operating current	-	0.7	1		V_{DD} = 3.3V
I_{BOD}[*1]	BOD operating current	-	10			V_{DD} = 3.3V, Normal mode
		-	1			V_{DD} = 3.3V, Enable Low Power mode
V_{POR}	POR reset voltage	2.10	2.20	2.30	V	
V_{LVR}	LVR reset voltage	2.12	2.22	2.32		
V_{BOD}	BOD brown-out detect voltage (Falling edge)	2.15	2.30	2.45		BODVL = 0
		2.55	2.70	2.85		BODVL = 1
		3.45	3.70	3.95		BODVL = 2
		4.15	4.40	4.65		BODVL = 3
	BOD brown-out detect voltage (Rising edge)	2.23	2.38	2.53		BODVL = 0
		2.63	2.78	2.93		BODVL = 1
		3.53	3.78	4.03		BODVL = 2
		4.23	4.48	4.73		BODVL = 3
T_{LVR_SU}[*1]	LVR startup time	-	200	TBD	μS	-
T_{LVR_RE}[*1]	LVR respond time	-	20	100		-
T_{BOD_SU}[*1]	BOD startup time	-	1000	TBD		-
T_{BOD_RE}[*1]	BOD respond time	-	100			Normal mode
		-	11200	TBD		Low Power mode
R_{VDDR}[*1]	V_{DD} rise time rate	10	-	-	μS/V	POR Enabled
R_{VDDF}[*1]	V_{DD} fall time rate	10	-	-		POR Enabled

		833.33	-	-		LVR Enabled
		500	-	-		BOD 2.3V Enabled, Normal mode
		166.67	-	-		BOD 2.7V Enabled, Normal mode
		62.5	-	-		BOD 3.7V Enabled, Normal mode
		43.49	-	-		BOD 4.4V Enabled, Normal mode
		55600	-	-		BOD 2.3V Enabled, Low Power mode
		18533	-	-		BOD 2.7V Enabled, Low Power mode
		6950	-	-		BOD 3.7V Enabled, Low Power mode
		4834.79	-	-		BOD 4.4V Enabled, Low Power mode

Note:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

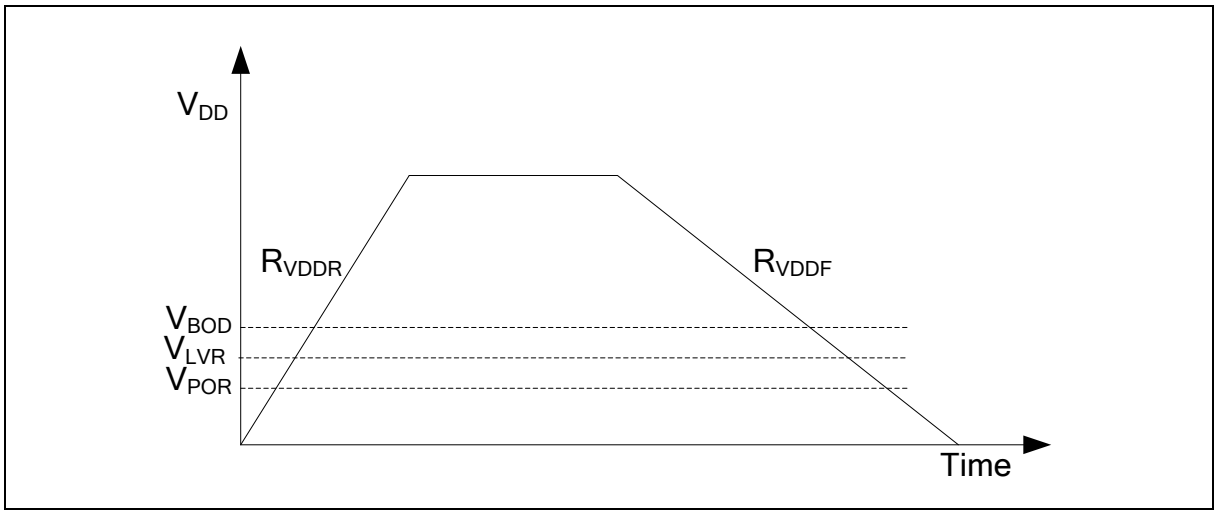


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

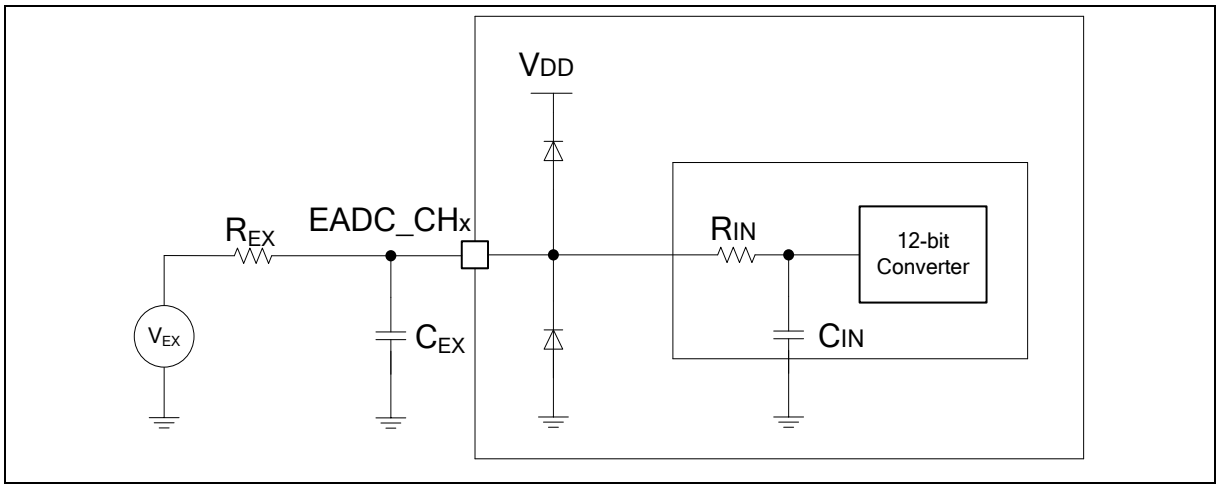
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	125	℃	
V_{DD}	Analog operating voltage	2.4	-	5.5	V	V_{DD}
V_{REF}	Reference voltage	2.4	-	V_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (V_{DD} + V_{REF} current)	-	-	4.5	mA	$V_{DD} = V_{REF}$ = 5.5 V F_{ADC} = 16 MHz $T_{CONV} = 18 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	-	-	16	MHz	
T_{SMP}	Sampling Time	4	-	259	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 4) * T_{ADC}
T_{CONV}	Conversion time	18	-	273	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 14 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	-	-	800	kSPS	$F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(ADC_ESMPCTL[7:0]) = 0
T_{EN}	Enable to ready time	1	-	-	μS	
INL[*1]	Integral Non-Linearity Error	-1.6	-	1.83	LSB	$V_{REF} = V_{DD}$, except SSOP20 and TSSOP28
		-1.68	-	1.35	LSB	$V_{REF} = V_{DD}$ SSOP20 and TSSOP28
DNL[*1]	Differential Non-Linearity Error	-1	-	2.44	LSB	$V_{REF} = V_{DD}$, except SSOP20 and TSSOP28
		-1	-	2.06	LSB	$V_{REF} = V_{DD}$ SSOP20 and TSSOP28
E_G[*1]	Gain error	-2.44	-	-0.75	LSB	$V_{REF} = V_{DD}$, except SSOP20 and TSSOP28
		-1.94	-	-0.5	LSB	$V_{REF} = V_{DD}$ SSOP20 and TSSOP28
E_O[*1]$_T$	Offset error	-0.25	-	1.81	LSB	$V_{REF} = V_{DD}$, except SSOP20 and TSSOP28
		0.56	-	1.5	LSB	$V_{REF} = V_{DD}$ SSOP20 and TSSOP28
E_A[*1]	Absolute Error	-3.56	-	2.69	LSB	$V_{REF} = V_{DD}$, except SSOP20 and TSSOP28
		-2.94	-	3	LSB	$V_{REF} = V_{DD}$ SSOP20 and TSSOP28
ENOB[*1]	Effective number of bits	-	10	-	bits	F_{ADC} = 16 MHz

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
SINAD[*1]	Signal-to-noise and distortion ratio	-	62	-	dB	V_{DD} = V_{REF} = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SNR[*1]	Signal-to-noise ratio	-	62	-		
THD[*1]	Total harmonic distortion	-	-80	-		
C_{IN}[*1]	Internal Capacitance	-	TBD	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	TBD	kΩ	
R_{EX}[*1]	External input impedance	-	-	TBD	kΩ	

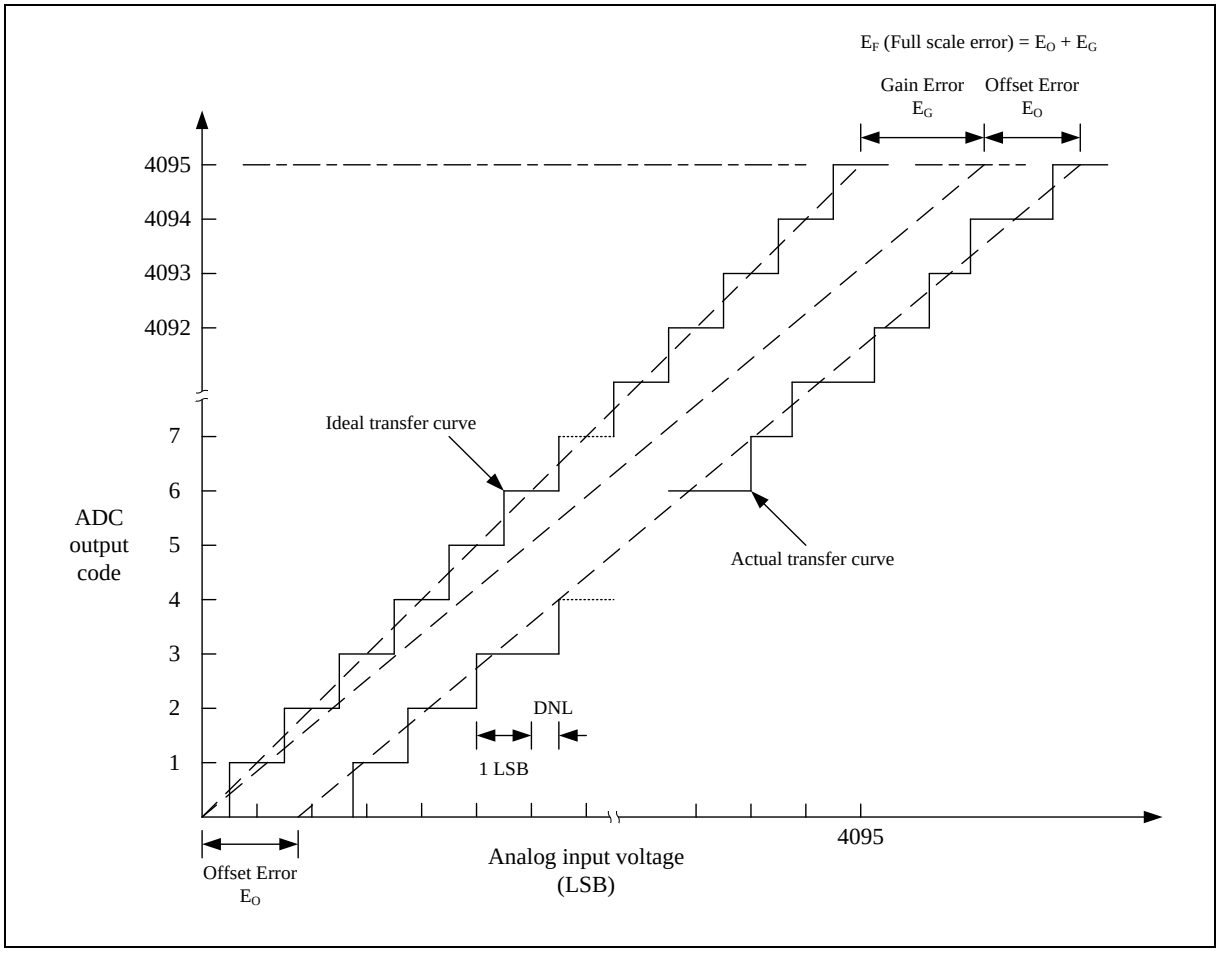
Note:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} = \frac{k}{f_{ADC} \times C_{IN} \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Analog supply voltage	2.4	-	5.5	V	
N_R	Resolution		5		bit	
V_{REF}	Reference supply voltage	2.4	-	V_{DD}	V	$V_{REF} \leq V_{DD}$
DNL[*2]	Differential non-linearity error	-	-	±0.05	LSB	
INL[*2]	Integral non-linearity error	-	-	±0.1	LSB	
OE[*2]	Offset Error	-	-	±0.1	LSB	
GE[*2]	Gain Error	-	-	±2	LSB	
AE[*2]	Absolute Error	-	-	±0.5	LSB	
-	Monotonic		5-bit guaranteed		-	-
V_O[*1]	Output Voltage	1*LSB	-	V_{REF} - 1*LSB	V	
R_O[*2]	Output impedance	4	5	6	kΩ	
C_{LOAD}[*2] [*4]	Capacitive load	-	-	50	pF	-
I_{DAC_VDD}[*2]	DAC operating current on V_{DD} supply	-	38	-	μA	
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	38	-	μA	
T_B[*2]	Settling Time	-	-	10	μS	Full scale: for a 5-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB, $C_{LOAD} \leq$ 50pF
PSRR[*1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and V_{SS}.
4. Capacitive load at DACOUT pin.

8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Analog supply voltage	2.4	-	5.5	V	
T_A	Temperature	-40	-	125	℃	
I_{ACMP}[*2]	ACMP operating current	-	75	200	μA	MODESEL = 01
V_{CM}[*2]	Input common mode voltage range	0	-	V_{DD}		
V_{DI}[*2]	Differential input voltage sensitivity	50	-	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	-	±30	mV	Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	20	-	mV	HYSSEL = 01
		-	30	60		HYSSEL = 10
		-	40	-		HYSSEL = 11
A_v[*1]	DC voltage Gain	43	70	-	dB	
T_d[*2]	Propagation delay	-	100	200	nS	MODESEL = 01
T_{Setup}[*2]	Setup time	-	-	5	μS	
A_{CRV}[*2]	CRV output voltage	-5	-	5	%	V_{DD} x (1/6+CRVCTL/24)
R_{CRV}[*2]	Unit resistor value	-	5.8	-	kΩ	
T_{SETUP_CRV}[*1]	Setup time	-	-	0.5	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	60	μA	

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

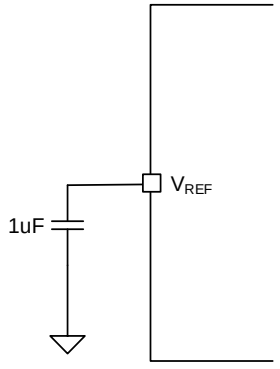
8.5.6 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	1.49	1.536	1.59	V	V_{DD} >= 2.0 V
		1.98	2.048	2.11		V_{DD} >= 2.4 V
		2.48	2.560	2.64		V_{DD} >= 2.9 V
		2.97	3.072	3.17		V_{DD} >= 3.4 V
		3.97	4.096	4.22		V_{DD} >= 4.5 V
T_S[*1]	Stable time	-	0.5	0.8	mS	C_L = 4.7 uF, V_{REF} initial = 0, Preload is enabled.
		-	9.3	13	mS	C_L = 4.7 uF, V_{REF} initial = 5.5, Preload is enabled.
		-	24	180	mS	C_L = 1 uF, V_{REF} initial = 0, Preload is enabled.
		-	2	2.6	mS	C_L = 1 uF, V_{REF} initial = 5.5, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	-	1	mA	
I_{VREF_LOAD}[*1]	V_{REF_INT} output loading current	-	-	1	mA	

Note:

1. Guaranteed by characterization, not tested in production.



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.7 Temperature Sensor

The maximum values are obtained for V_{DD} = 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	655	654	656	mV	T_A = 0°C
T_C[*1]	Temperature Coefficient	-1.99	-2.00	-2.01	mV/°C	
T_S[*2]	Stable time	-	-	1	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	-	15	20	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	30	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Analog supply voltage	2.5	-	3.6	V	
T_A	Temperature	-40	-	125	°C	
I_{TEMP}	Temperature Sensor operating current	-	200	-	µA	
T_{ACC}	Temperature Accuracy	-	±1	±2	°C	
T_R	Temperature Resolution	-	0.0625	-	°C	
T_{CONV}	Conversion Time	-	84	100	mS	

Note:

1. Guaranteed by characterization, not tested in production.

8.6 Communications Characteristics

8.6.1 USCI-SPI Dynamic Characteristics

Symbol	Parameter	Min [*1]	Typ	Max[*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	24	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	24		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	5	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	TBD	nS	2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-1 USCI-SPI Master Mode Characteristics

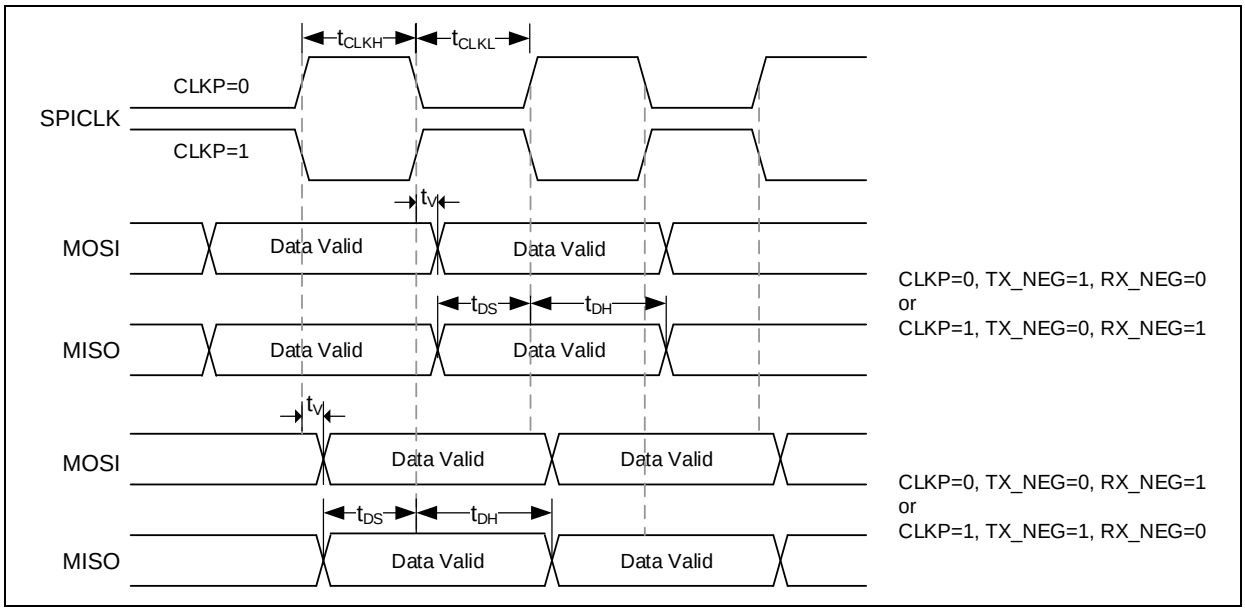


Figure 8.6-1 USCI-SPI Master Mode Timing Diagram

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	7	MHz	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	7		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		TBD	-	-		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	2	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	65	nS	4.5 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
		-	-	TBD		2.7 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. Guaranteed by design.

Table 8.6-2 USCI-SPI Slave Mode Characteristics

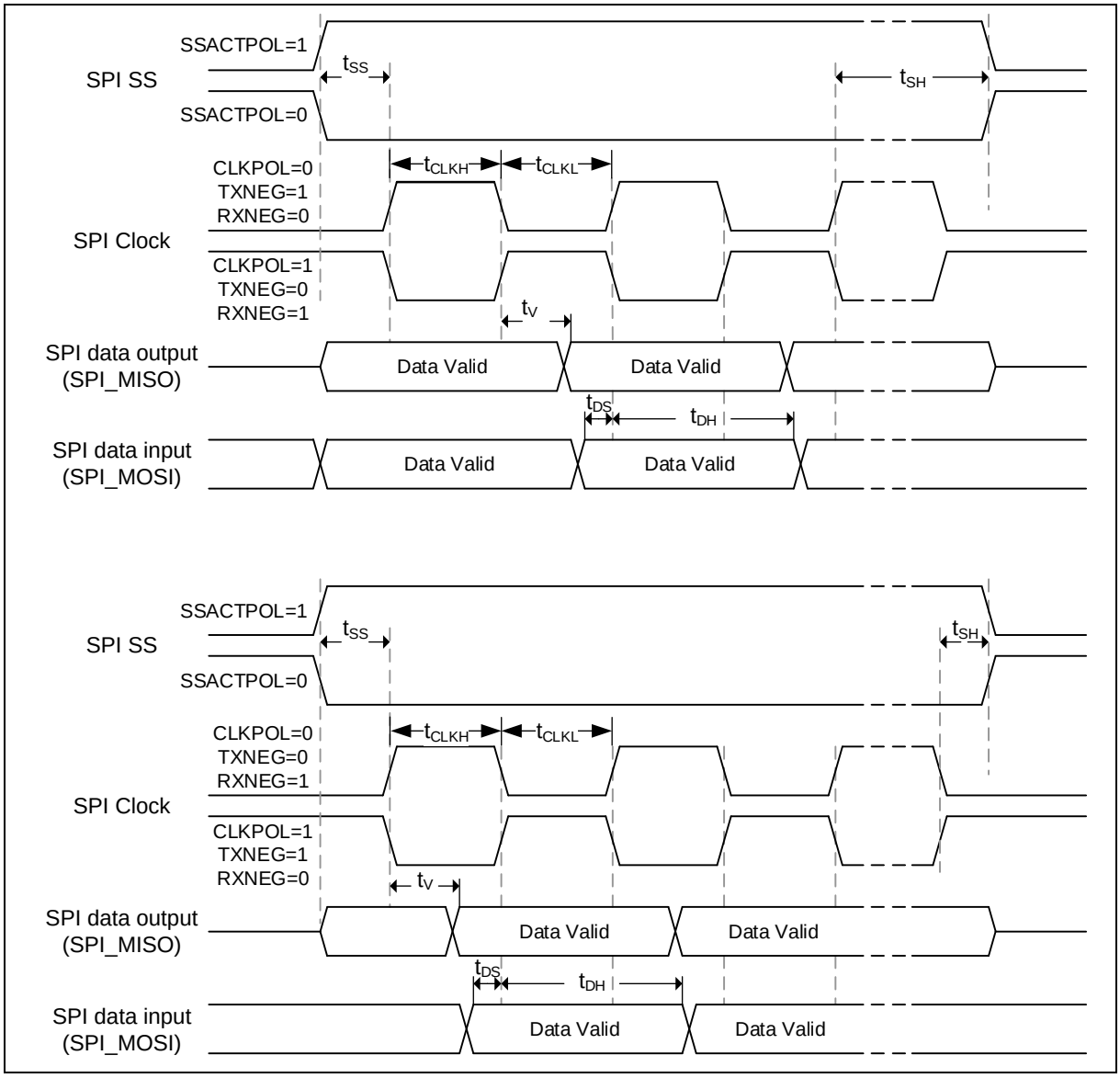


Figure 8.6-2 USCI-SPI Slave Mode Timing Diagram

8.6.2 USCI-I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I2C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I2C frequency.
3. I2C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.6-3 USCI-I²C Characteristics

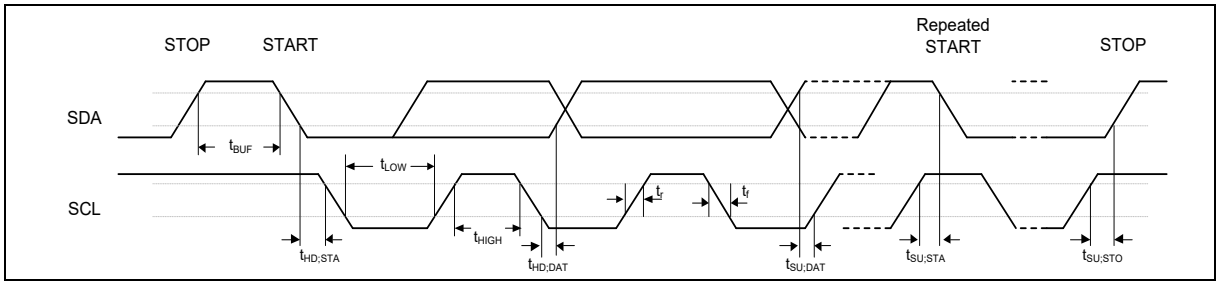


Figure 8.6-3 USCI-I²C Timing Diagram

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	-	1.5	-	V	T_A = 25℃
T_{ERASE}	Page erase time	-	20	-	mS	
T_{PROG}	Program time	-	60	-	μS	
I_{DD1}	Read current	-	7	-	mA	
I_{DD2}	Program current	-	8	-	mA	
I_{DD3}	Erase current	-	12	-	mA	
N_{ENDUR}	Cycling Endurance	20,000	-	-	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	10	-	-	year	20 kcycle[2], T_J = 85℃
		100	-	-	year	20 kcycle[2], T_J = 25℃

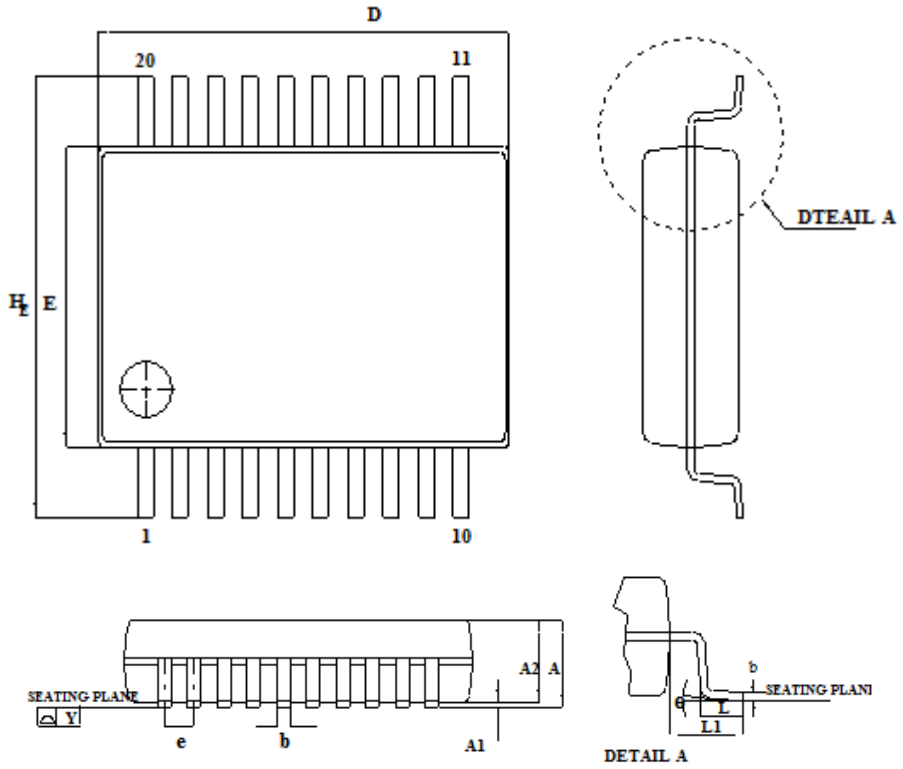
Note:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
3. Guaranteed by design.

9 PACKAGE DIMENSIONS

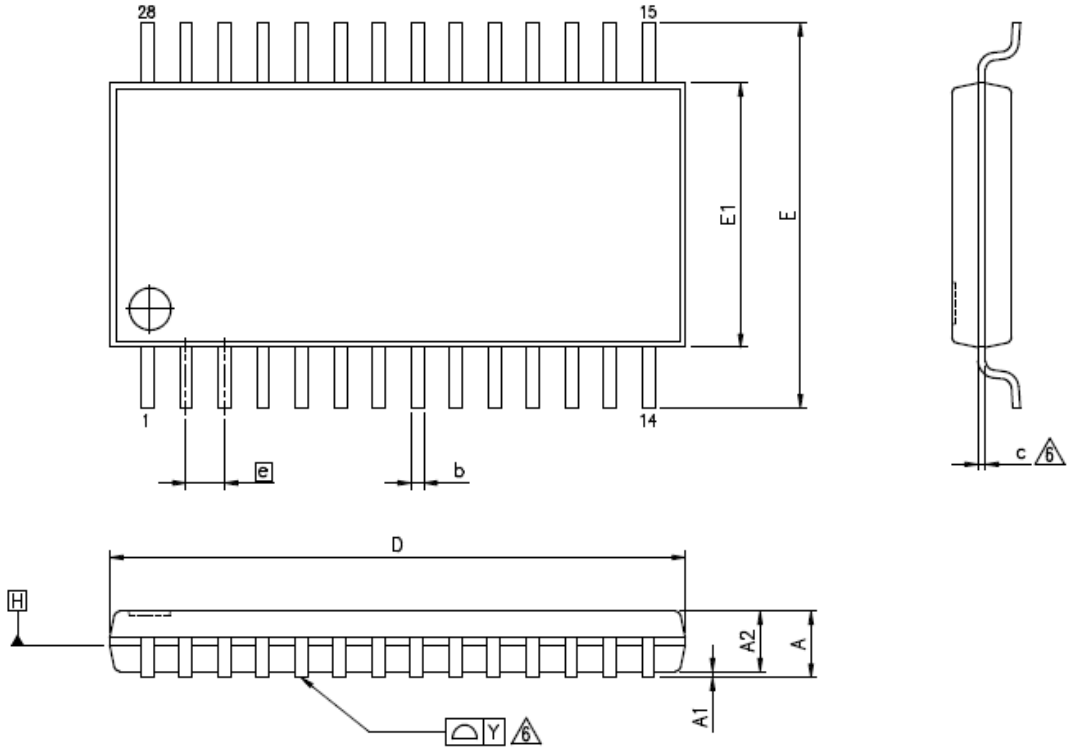
Package is Halogen-free, RoHS-compliant and TSCA-compliant.

9.1 SSOP 20 (5.3x7.2x1.75 mm)



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
H_E	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
θ	0	—	8	0	—	8

9.2 TSSOP 28 (4.4x9.7x1.0 mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

10 ABBREVIATIONS

10.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop
PWM	Pulse Width Modulation

QEI	Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Description
2023.07.18	1.00	• Initial version.
2024.01.23	1.01	• Fixed PA.3 type to input only in section 4.2.1, 4.2.2 and 4.2.3. • Removed non-supported register VTOR and SHPR1 in section 6.2.13.

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