NuMicro® Family

1T 8051-based Microcontroller

CM1003 Series

CM1003CJ3AE

CM1003DJ3AE

CM1003DL8AE

Datasheet

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1 GENERAL DESCRIPTION

The NuMicro CM1003 series is an embedded Flash Memory type 1T 8051-based microcontroller. The instruction set is fully compatible with the standard 80C51 and performance enhanced. It supports 16/24 MHz core speed and features up to 64 KB of Flash Memory, 256 bytes of RAM and 4 KB of auxiliary RAM (XRAM), 4 KB of Flash loader memory (LDROM), 2.4V to 5.5V operating voltage, and -40°C to +105°C operating temperature.

The CM1003 series also provides plenty of peripherals including two 16-bit Timers, one 16-bit Timer2 with three-channel input capture mode, one Watchdog Timer, one Self Wake-up Timer, one 16-bit auto-reload Timer3 for general purpose or baud rate generator, two UARTs with frame error detection and automatic address recognition, three ISO 7816-3 interfaces, one SPI, one I^2C, six basic PWM output channels, six enhanced PWM output channels, 8-channel shared pin interrupt for all I/Os, and 15-channel 12-bit 500 ksps ADC with continuous mode. The peripherals are equipped with 24 sources with 4-level-priority interrupts capability.

Supported packages include QFN 33-pin and LQFP 48-pin.

For the development, Nuvoton provides the NuMaker evaluation board and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil C51, IAR EW8051, and NuEclipse SDCC compilers are also supported.

1.1 Key Features and Applications

Product Line	UART	ISO 7816-3	I^2C	SPI	Timer	PWM	ADC
CM1003CJ3AE CM1003DJ3AE CM1003DL8AE	2	3	1	1	4	12	15

Table 1.1-1 NuMicro CM1003 Series Key Features Support Table

The CM1003 series is suitable for a wide range of applications such as:

- Home Appliances
- LED Lighting Control
- Motor Control
- Industrial Automation

2 FEATURES

Core and System	
8051	• Fully static design 8-bit high performance 1T 8051-based CMOS microcontroller • Instruction set fully compatible with MCS-51 • 4-priority-level interrupts capability • Dual Data Pointers (DPTRs)
Power on Reset (POR)	• POR with 1.15V threshold voltage level
Brown-out Detector (BOD)	• 4-level selection, with brown-out interrupt and reset option (4.4V / 3.7V / 2.7V / 2.2V)
Low Voltage Reset (LVR)	• LVR with 2.0V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID) • 128-bytes security protection memory SPROM
Memories	
Flash Memory	• Up to 64 Kbytes of APROM for User Code • 4/3/2/1 Kbytes of Flash for loader (LDROM) configure from APROM for In-System-Programmable (ISP) • Flash Memory accumulated with pages of 128 bytes from APROM by In-Application-Programmable (IAP) means whole APROM can be used as Data Flash • An additional 128 bytes security protection memory SPROM • Code lock for security by CONFIG
SRAM	• 256 bytes on-chip RAM • Additional 4 Kbytes on-chip auxiliary RAM (XRAM) accessed by MOVX instruction
Clocks	
External Clock Source	• 4~24 MHz High-speed external crystal oscillator (HXT) for precise timing operation
Internal Clock Source	• Default 16 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25°C, 3.3 V), ±2% in -20°C to +105°C, ±4% in -40°C to -20°C.

	• Selectable 24 MHz high-speed internal oscillator (HIRC) trimmed to ±1% (accuracy at 25°C, 3.3 V) switch by software. • 10 kHz low-speed internal oscillator (LIRC) calibrating to ±10% by software from high-speed internal oscillator
Timers	
16-bit Timer	• Two 16-bit Timers/Counters 0 and 1 compatible with standard 8051. • One 16-bit Timer2 with three-channel input capture module and 9 input pin can be selected. • One 16-bit auto-reload Timer3, which can be the baud rate clock source of UART0 and UART1.
Watchdog	• 6-bit free running up counter for WDT time-out interval. • Selectable time-out interval is 6.40 ms ~ 1.638s since WDT_CLK = 10 kHz (LIRC) • Able to wake up from Power-down or Idle mode • Interrupt or reset selectable on watchdog time-out
Wake-up Timer	• 16-bit free running up counter for time-out interval • Clock sources from LIRC • Able to self Wake-up wake up from Power-down or Idle mode, and auto reload count value • Supports Interrupt
PWM	• Up to 12 output pins can be selected • Supports maximum clock source frequency up to 24 MHz • Supports up to four PWM modules, PWM0 module provides 6 output channels. PWM1 ~ PWM3 module provides 2 output channels. • Supports independent mode for PWM output • Supports complementary mode for 3 complementary paired PWM output channels • Supports 16-bit resolution PWM counter • Supports mask function and tri-state enable for each PWM pin • PWM0 module supporting Dead-time insertion with 8-bit resolution • PWM0 module supporting brake function • PWM0 module supporting trigger ADC events
Analog Interfaces	
Analog-to-Digital	• Analog input voltage range: 0 ~ AV_{DD}

Converter (ADC)	• 12-bit resolution and 10-bit accuracy is guaranteed • Up to 15 single-end analog input channels • 1 internal channel, which is band-gap voltage (VBG) • Up to 500 ksps sampling rate • Software Write 1 to ADCS bit • External pin (STADC) trigger • PWM trigger • Supports continues convert function auto store the A/D conversion result in XRAM
Communication Interfaces	
UART	• Supports up to 2 UARTs: UART0, UART1 • Up to three sets of ISO 7816-3 device configuration as UART • UART baud rate clock from HIRC or HXT • Full-duplex asynchronous communications • Programmable 9th bit • TXD and RXD pins of UART0 exchangeable via software
I²C	• One sets of I²C device • Master/Slave mode • Bidirectional data transfer between masters and slaves • 7-bit addressing mode • Standard mode (100 kbps) and Fast mode (400 kbps) • Supports 8-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflows • Supports hold time programmable
SPI	• One set of SPI device • Supports Master or Slave mode operation • Supports MSB first or LSB first transfer sequence • Slave mode up to 12 MHz
ISO-7816	• Up to three sets ISO 7816-3 device • Supports ISO 7816-3 compliant T=0, T=1 • Supports full-duplex UART mode
GPIO	• Four I/O modes: – Quasi-bidirectional mode – Push-Pull Output mode

	– Open-Drain Output mode – Input only with high impendence mode • Schmitt trigger input / TTL mode selectable • Each I/O pin configured as interrupt source with edge/level trigger setting • Standard interrupt pins $\overline{INT0}$ and $\overline{INT1}$ • Supports high drive and high sink current I/O • I/O pin internal pull-up resistor enabled in input mode • Maximum I/O Speed is 24 MHz • Enabling the pin interrupt function will also enable the wake-up function
ESD & EFT	
ESD	• HBM pass ±7 kV
EFT	• > ±4.4 kV
Latch-up	• 200 mA pass

3 PARTS INFORMATION

3.1 CM1003 Series Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

	TSSOP20	QFN20	QFN33	LQFP48
Part No.	CM1003BF2AE CM1003CF2AE	CM1003BF3AE CM1003CF3AE	CM1003CJ3AE CM1003DJ3AE	CM1003DL8AE

3.2 CM1003 Series Naming Rule

C	M	1	003	C	J	3	A	E
NTNJ	Product Group	CPU Core	Device Family	Flash Size	Pin Count	Package Type	Version	Operation Temperature
C	M:MCU	1:8051	003	B: 16 KB C: 32 KB D: 64 KB	F: 20 J: 32/33 L: 48	2: TSSOP 3: QFN 8: LQFP		E: -40°C ~ +105°C

3.3 CM1003 Series Selection Gude

Part Number[3]	Flash Memory (KB)	SRAM (B)	LDROM (KB) [1]	I/O	Timer	PWM	Connectivity				ADC(12-Bit)	Package
							ISO 7816-3 [2]	UART	SPI	I²C		
CM1003BF2AE	16	256+1K	4	18	4	6	-	2	1	1	8-ch	TSSOP20
CM1003BF3AE	16	256+1K	4	18	4	6	-	2	1	1	8-ch	QFN20
CM1003CF2AE	32	256+1K	4	18	4	6	-	2	1	1	8-ch	TSSOP20
CM1003CF3AE	32	256+1K	4	18	4	6	-	2	1	1	8-ch	QFN20
CM1003CJ3AE	32	256+4K	4	30	4	12	3	2	1	1	15-ch	QFN33
CM1003DJ3AE	64	256+4K	4	30	4	12	3	2	1	1	15-ch	QFN33
CM1003DL8AE	64	256+4K	4	46	4	12	3	2	1	1	15-ch	LQFP48

Note:

1. ISP ROM programmable 1/2/3/4 KB Flash for user program loader (LDROM) shared from ARPOM.
2. ISO 7816-3 configurable as UART function, GPIO defined as UART2 ~ UART4.
3. This document is only for CM1003xJxAE/CM1003xLxAE 4 KB RAM series products. The specifications for the part numbers with a gray background in this form should refer to the CM1003xFxAE 1 KB RAM series product DS.

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuaration informations by using NuTool - PinConfigure. The NuTool - PinConfigure contains all Nuvoton NuMicro® Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 CM1003 Series Pin Diagram

4.1.1.1 LQFP48 Package

Corresponding Part Number: CM1003DL8AE

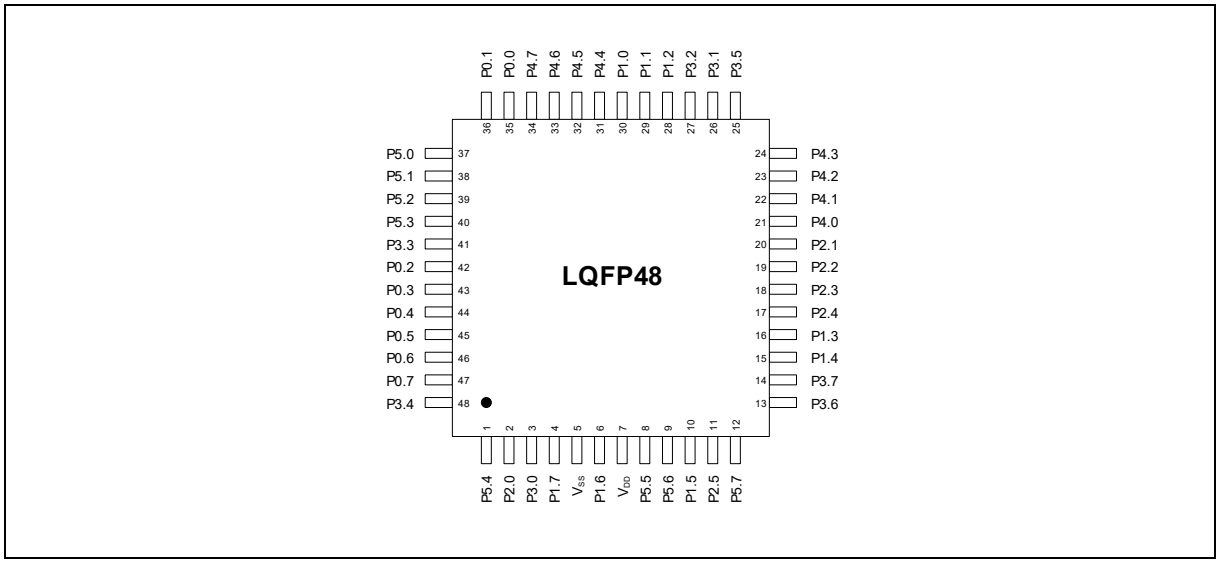


Figure 4.1-1 LQFP48 Pin Assignment

4.1.1.2 QFN33 Package

Corresponding Part Number: CM1003CJ3AE / CM1003DJ3AE

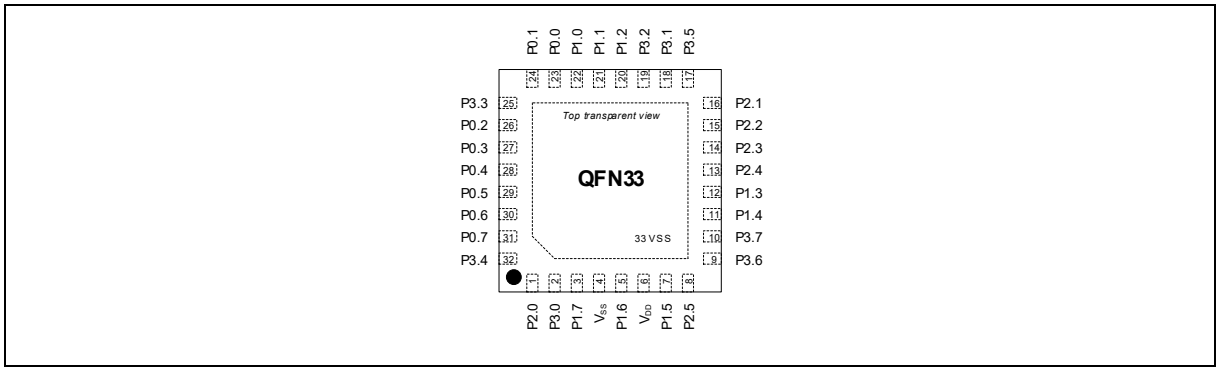


Figure 4.1-2 QFN33 Pin Assignment

4.1.2 CM1003 Series Multi Function Pin Diagram

4.1.2.1 LQFP48 Package

Corresponding Part Number: CM1003DL8AE

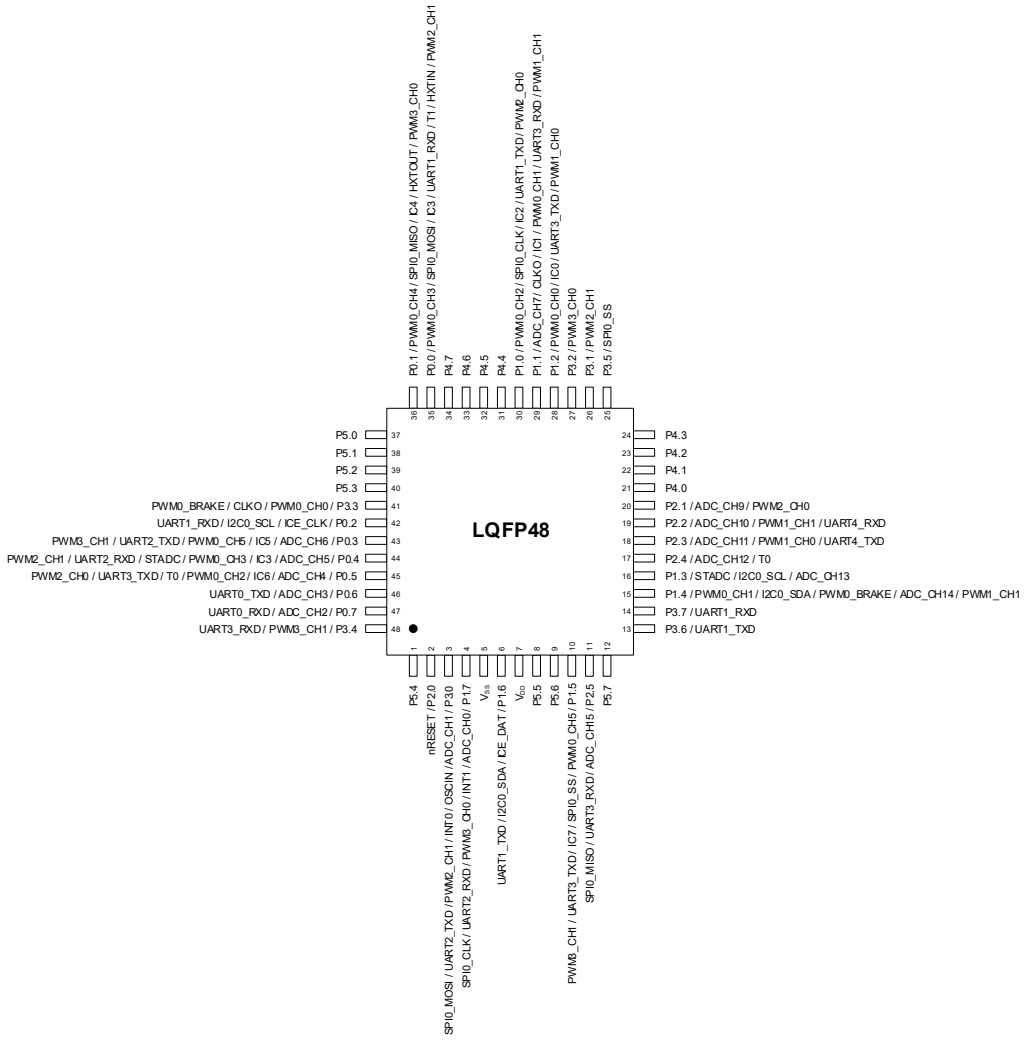


Figure 4.1-3 Pin Assignment of LQFP48 Package

Pin	Type	CM1003DL8AE Pin Function
1	I/O	P5.4
2	I/O	P2.0 / nRESET
3	I/O	P3.0 / ADC_CH1 / OSCIN / INT0 / PWM2_CH1 / UART2_TXD / SPI0_MOSI
4	I/O	P1.7 / ADC_CH0 / INT1 / PWM3_CH0 / UART2_RXD / SPI0_CLK

Pin	Type	CM1003DL8AE Pin Function
5	P	V_{SS}
6	I/O	P1.6 / ICE_DAT / I2C0_SDA / UART1_TXD
7	P	V_{DD}
8	I/O	P5.5
9	I/O	P5.6
10	I/O	P1.5 / PWM0_CH5 / SPI0_SS / IC7 / UART3_TXD / PWM3_CH1
11	I/O	P2.5 / ADC_CH15 / UART3_RXD / SPI0_MISO
12	I/O	P5.7
13	I/O	P3.6 / UART1_TXD
14	I/O	P3.7 / UART1_RXD
15	I/O	P1.4 / PWM0_CH1 / I2C0_SDA / PWM0_BRAKE / ADC_CH14 / PWM1_CH1
16	I/O	P1.3 / STADC / I2C0_SCL / ADC_CH13
17	I/O	P2.4 / ADC_CH12 / T0
18	I/O	P2.3 / ADC_CH11 / PWM1_CH0 / UART4_TXD
19	I/O	P2.2 / ADC_CH10 / PWM1_CH1 / UART4_RXD
20	I/O	P2.1 / ADC_CH9 / PWM2_CH0
21	I/O	P4.0
22	I/O	P4.1
23	I/O	P4.2
24	I/O	P4.3
25	I/O	P3.5 / SPI0_SS
26	I/O	P3.1 / PWM2_CH1
27	I/O	P3.2 / PWM3_CH0
28	I/O	P1.2 / PWM0_CH0 / IC0 / UART3_TXD / PWM1_CH0
29	I/O	P1.1 / ADC_CH7 / CLKO / IC1 / PWM0_CH1 / UART3_RXD / PWM1_CH1
30	I/O	P1.0 / PWM0_CH2 / SPI0_CLK / IC2 / UART1_TXD / PWM2_CH0
31	I/O	P4.4
32	I/O	P4.5
33	I/O	P4.6
34	I/O	P4.7
35	I/O	P0.0 / PWM0_CH3 / SPI0_MOSI / IC3 / UART1_RXD / T1 / HXTIN / PWM2_CH1
36	I/O	P0.1 / PWM0_CH4 / SPI0_MISO / IC4 / HXTOUT / PWM3_CH0
37	I/O	P5.0

Pin	Type	CM1003DL8AE Pin Function
38	I/O	P5.1
39	I/O	P5.2
40	I/O	P5.3
41	I/O	P3.3 / PWM0_CH0 / CLKO / PWM0_BRAKE
42	I/O	P0.2 / ICE_CLK / I2C0_SCL / UART1_RXD
43	I/O	P0.3 / ADC_CH6 / IC5 / PWM0_CH5 / UART2_TXD / PWM3_CH1
44	I/O	P0.4 / ADC_CH5 / IC3 / PWM0_CH3 / STADC / UART2_RXD / PWM2_CH1
45	I/O	P0.5 / ADC_CH4 / IC6 / PWM0_CH2 / T0 / UART3_TXD / PWM2_CH0
46	I/O	P0.6 / ADC_CH3 / UART0_TXD
47	I/O	P0.7 / ADC_CH2 / UART0_RXD
48	I/O	P3.4 / PWM3_CH1 / UART3_RXD

Table 4.1-1 LQFP48 Package Multi-function Pin Table

4.1.2.2 QFN33 Package

Corresponding Part Number: CM1003CJ3AE / CM1003DJ3AE

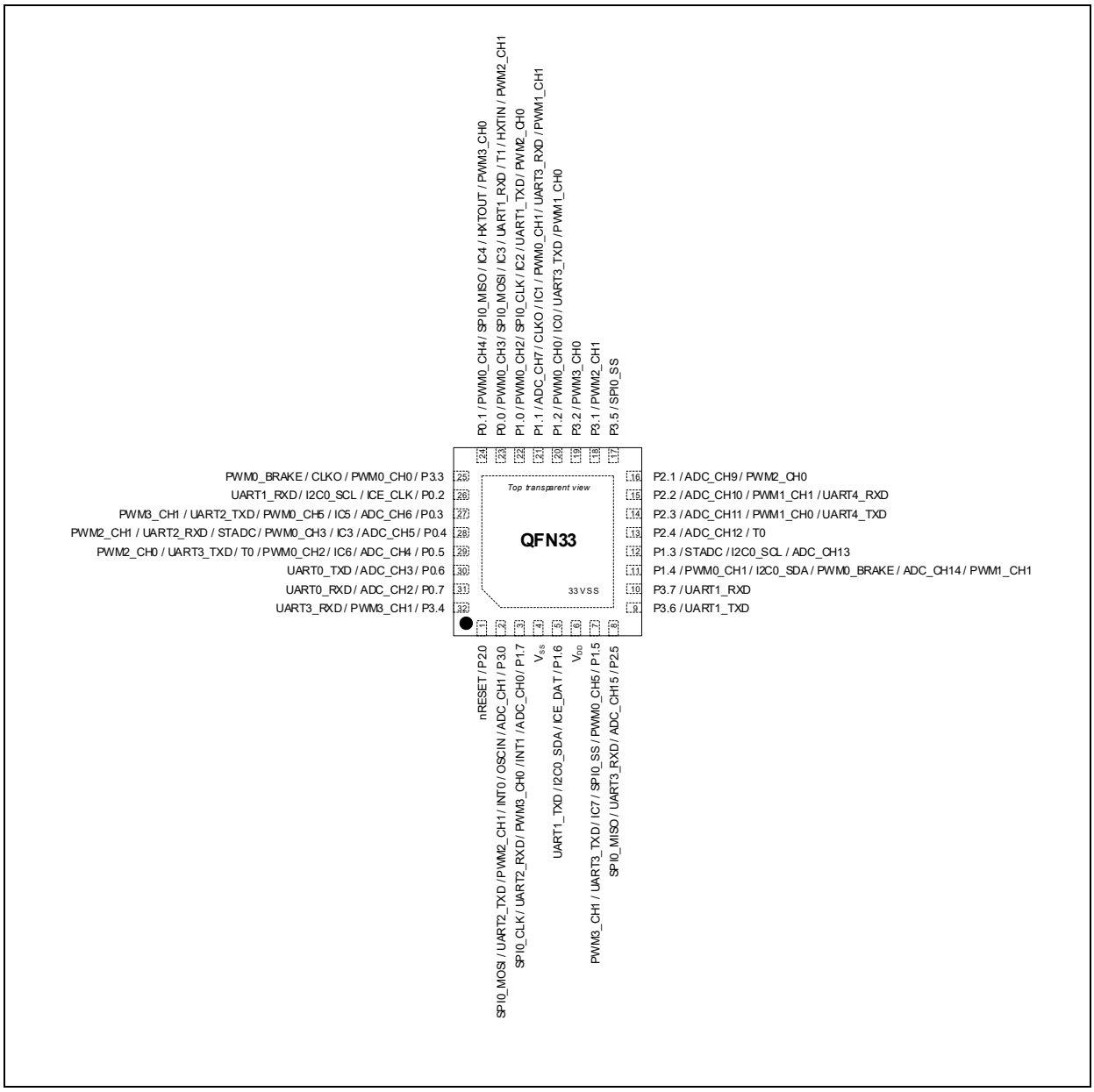


Figure 4.1-4 Pin Assignment of QFN33 Package

Pin	Type	CM1003CJ3AE / CM1003DJ3AE Pin Function
1	I/O	P2.0 / nRESET
2	I/O	P3.0 / ADC_CH1 / OSCIN / INT0 / PWM2_CH1 / UART2_TXD / SPI0_MOSI
3	I/O	P1.7 / ADC_CH0 / INT1 / PWM3_CH0 / UART2_RXD / SPI0_CLK
4	P	V_{SS}

Pin	Type	CM1003CJ3AE / CM1003DJ3AE Pin Function
5	I/O	P1.6 / ICE_DAT / I2C0_SDA / UART1_TXD
6	P	V_{DD}
7	I/O	P1.5 / PWM0_CH5 / SPI0_SS / IC7 / UART3_TXD / PWM3_CH1
8	I/O	P2.5 / ADC_CH15 / UART3_RXD / SPI0_MISO
9	I/O	P3.6 / UART1_TXD
10	I/O	P3.7 / UART1_RXD
11	I/O	P1.4 / PWM0_CH1 / I2C0_SDA / PWM0_BRAKE / ADC_CH14 / PWM1_CH1
12	I/O	P1.3 / STADC / I2C0_SCL / ADC_CH13
13	I/O	P2.4 / ADC_CH12 / T0
14	I/O	P2.3 / ADC_CH11 / PWM1_CH0 / UART4_TXD
15	I/O	P2.2 / ADC_CH10 / PWM1_CH1 / UART4_RXD
16	I/O	P2.1 / ADC_CH9 / PWM2_CH0
17	I/O	P3.5 / SPI0_SS
18	I/O	P3.1 / PWM2_CH1
19	I/O	P3.2 / PWM3_CH0
20	I/O	P1.2 / PWM0_CH0 / IC0 / UART3_TXD / PWM1_CH0
21	I/O	P1.1 / ADC_CH7 / CLKO / IC1 / PWM0_CH1 / UART3_RXD / PWM1_CH1
22	I/O	P1.0 / PWM0_CH2 / SPI0_CLK / IC2 / UART1_TXD / PWM2_CH0
23	I/O	P0.0 / PWM0_CH3 / SPI0_MOSI / IC3 / UART1_RXD / T1 / HXTIN / PWM2_CH1
24	I/O	P0.1 / PWM0_CH4 / SPI0_MISO / IC4 / HXTOUT / PWM3_CH0
25	I/O	P3.3 / PWM0_CH0 / CLKO / PWM0_BRAKE
26	I/O	P0.2 / ICE_CLK / I2C0_SCL / UART1_RXD
27	I/O	P0.3 / ADC_CH6 / IC5 / PWM0_CH5 / UART2_TXD / PWM3_CH1
28	I/O	P0.4 / ADC_CH5 / IC3 / PWM0_CH3 / STADC / UART2_RXD / PWM2_CH1
29	I/O	P0.5 / ADC_CH4 / IC6 / PWM0_CH2 / T0 / UART3_TXD / PWM2_CH0
30	I/O	P0.6 / ADC_CH3 / UART0_TXD
31	I/O	P0.7 / ADC_CH2 / UART0_RXD
32	I/O	P3.4 / PWM3_CH1 / UART3_RXD
33	EPAD	V_{SS}

Table 4.1-2 QFN33 Package Multi-function Pin Table

4.2 CM1003 Series Pin Description

4.2.1 CM1003 Series Pin Mapping

	CM1003	
Pin Name	**33 Pin**	**48 Pin**
P5.4		1
P2.0	1	2
P3.0	2	3
P1.7	3	4
V_{SS}	4	5
P1.6	5	6
V_{DD}	6	7
P5.5		8
P5.6		9
P1.5	7	10
P2.5	8	11
P5.7		12
P3.6	9	13
P3.7	10	14
P1.4	11	15
P1.3	12	16
P2.4	13	17
P2.3	14	18
P2.2	15	19
P2.1	16	20
P4.0		21
P4.1		22
P4.2		23
P4.3		24
P3.5	17	25
P3.1	18	26
P3.2	19	27
P1.2	20	28
P1.1	21	29
P1.0	22	30

P4.4		31
P4.5		32
P4.6		33
P4.7		34
P0.0	23	35
P0.1	24	36
P5.0		37
P5.1		38
P5.2		39
P5.3		40
P3.3	25	41
P0.2	26	42
P0.3	27	43
P0.4	28	44
P0.5	29	45
P0.6	30	46
P0.7	31	47
P3.4	32	48

4.2.2 CM1003 Series Pin Functional Description

Symbol		Multi-Function Description[1]	
LQFP48	QFN 33		
7	6	**VDD**	Supply voltage V_{DD} for operation.
5	4	**VSS**	Ground potential.
35	23	**P0.0**	Port 0 bit 0.
		PWM0_CH3	PWM0 output channel 3.
		PWM2_CH1	PWM2 output channel 1.
		IC3	Input capture channel 3.
		SPI0_MOSI	SPI master output/slave input.
		UART1_RXD	UART1 receive input.
		XT1_IN	External 4~24 MHz (high speed) crystal input pin.
		OSCIN	If the EXTEN[1:0] = 10b, OSCIN is the external clock input pin.
		T1	External count input to Timer/Counter 1 or its toggle output.
36	24	**P0.1**	Port 0 bit 1.
		PWM0_CH4	PWM0 output channel 4.
		PWM3_CH0	PWM3 output channel 0.
		IC4	Input capture channel 4.
		SPI0_MISO	SPI master input/slave output.
		XT1_OUT	External 4~24 MHz (high speed) crystal output pin.
42	26	**P0.2**	Port 0 bit 2.
		I2C0_SCL	I^2C clock.
		UART1_RXD	UART1 receive input.
		ICE_CLK	ICE / ICP clock input.

Symbol		Multi-Function Description[1]	
LQFP48	QFN 33		
43	27	**P0.3**	Port 0 bit 3.
		ADC_CH6	ADC input channel 6.
		PWM0_CH5	PWM0 output channel5
		PWM3_CH1	PWM3 output channel1
		IC5	Input capture channel 5.
		UART2_TXD	UART2 transmit data output.
		SC0_CLK	Smart Card 0 clock pin
44	28	**P0.4**	Port 0 bit 4.
		ADC_CH5	ADC input channel 5.
		PWM0_CH3	PWM0 output channel 3.
		PWM2_CH1	PWM2 output channel 1.
		IC3	Input capture channel 3.
		UART2_RXD	UART2 receive input.
		SC0_DAT	Smart Card 0 data pin
		STADC	External start ADC trigger
45	29	**P0.5**	Port 0 bit 5.
		ADC_CH4	ADC input channel 4.
		PWM0_CH2	PWM0 output channel 2.
		PWM2_CH0	PWM2 output channel 0.
		IC6	Input capture channel 6.
		UART3_TXD	UART3 transmit data output.
		SC1_CLK	Smart card clock pin.
		T0	External count input to Timer/Counter 0 or its toggle output.
46	30	**P0.6**	Port 0 bit 6.
		ADC_CH3	ADC input channel 3.
		UART0_TXD	UART0 transmit data output.
47	31	**P0.7**	Port 0 bit 7.
		ADC_CH2	ADC input channel 2.
		UART0_RXD	UART0 receive input.
30	22	**P1.0**	Port 1 bit 0.
		PWM0_CH2	PWM0 output channel 2.
		PWM2_CH0	PWM2 output channel 0.
		IC2	Input capture channel 2.
		SPI0_CLK	SPI0 clock.
		UART1_TXD	UART1 transmit data output.
29	21	**P1.1**	Port 1 bit 1
		ADC_CH7	ADC input channel 7.
		PWM0_CH1	PWM0 output channel 1.
		PWM1_CH1	PWM1 output channel 1.
		IC1	Input capture channel 1.
		UART3_RXD	UART3 receive input.
		SC1_DAT	Smart Card 1 data pin.
		CLKO	System clock output.
28	20	**P1.2**	Port 1 bit 2.
		PWM0_CH0	PWM0 output channel 0.
		PWM1_CH0	PWM1 output channel 0.
		IC0	Input capture channel 0.
		UART3_TXD	UART3 transmit data output.
		SC1_CLK	Smart Card 1 clock pin.
16	12	**P1.3**	Port 1 bit 3.
		ADC_CH13	ADC input channel 13.
		I2C0_SCL	I^2C0 clock.

Symbol		Multi-Function Description[1]	
LQFP48	QFN 33		
		STADC	External start ADC trigger
15	11	**P1.4**	Port 1 bit 4.
		ADC_CH14	ADC input channel 14.
		PWM0_CH1	PWM0 output channel 1.
		PWM1_CH1	PWM1 output channel 1.
		I2C0_SDA	I^2C0 data.
		PWM0_BRAKE	PWM0 Fault Brake input.
10	7	**P1.5**	Port 1 bit 5.
		PWM0_CH5	PWM0 output channel 5.
		PWM3_CH1	PWM3 output channel 1.
		IC7	Input capture channel 7.
		SPI0_SS	SPI0 slave select input.
		UART3_TXD	UART3 transmit data output.
		SC1_CLK	Smart card 2 clock pin
6	5	**P1.6**	Port 1 bit 6.
		I2C0_SDA	I^2C0 data.
		UART1_TXD	UART1 transmit data output.
		ICE_DAT	ICE data input or output.
4	3	**P1.7**	Port 1 bit 7.
		ADC_CH0	ADC input channel 0.
		PWM3_CH0	PWM3 output channel 0.
		SPI0_CLK	SPI0 clock.
		UART2_RXD	UART2 receive input.
		SC0_DAT	Smart Card 0 data pin
		INT1	External interrupt 1 input.
2	1	**P2.0**	Port 2 bit 0 input pin available when RPD (CONFIG0.2) is programmed as 0.
		nRESET	It is a Schmitt trigger input pin for hardware device reset. A low on this pin resets the device. nRESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to VSS.
20	16	**P2.1**	Port 2 bit 1.
		ADC_CH9	ADC input channel 9.
		PWM2_CH0	PWM2 output channel 0.
19	15	**P2.2**	Port 2 bit 2.
		ADC_CH10	ADC input channel 10.
		PWM1_CH1	PWM1 output channel 1.
		UART4_RXD	UART4 receive input.
		SC2_DAT6	Smart card 2 data pin
18	14	**P2.3**	Port 2 bit 3.
		ADC_CH11	ADC input channel 11.
		PWM1_CH0	PWM1 output channel 0.
		UART4_TXD	UART4 transmit data output.
		SC2_CLK6	Smart card 2 clock pin
17	13	**P2.4**	Port 2 bit 4.
		ADC_CH12	ADC input channel 12.
		T0	External count input to Timer/Counter 0 or its toggle output.
11	8	**P2.5**	Port 2 bit 5.
		ADC_CH15	ADC input channel 15.
		SPI0_MISO	SPI master input/slave output.
		UART3_RXD	UART3 receive input.
		SC1_DAT6	Smart card 1 data pin
3	2	**P3.0**	Port 3 bit 0.
		ADC_CH1	ADC input channel 1.

Symbol		Multi-Function Description[1]	
LQFP48	QFN 33		
		PWM2_CH1	PWM2 output channel 1.
		SPI0_MOSI	SPI master output/slave input.
		UART2_TXD	UART2 transmit data output.
		SC0_CLK6	Smart card 0 clock pin
		INT0	External interrupt 0 input.
		OSCIN	If the EXTEN[1:0] = 11b, OSCIN is the external clock input pin.
26	18	**P3.1**	Port 3 bit 1.
		PWM2_CH1	PWM2 output channel 1.
27	19	**P3.2**	Port 3 bit 2.
		PWM3_CH0	PWM3 output channel 0.
41	25	**P3.3**	Port 3 bit 3.
		PWM0_CH0	PWM3 output channel 0.
		CLK_OUT	System clock output.
		PWM0_BRAKE	PWM0 Fault Brake input.
48	32	**P3.4**	Port 3 bit 4.
		PWM3_CH1	PWM3 output channel 0.
		UART3_RXD	UART3 receive input.
		SC1_DAT	Smart card 0 data pin
25	17	**P3.5**	Port 3 bit 5.
		SPI0_SS	SPI0 slave select input.
13	9	**P3.6**	Port 3 bit 6.
		UART1_TXD	UART1 transmit data output.
14	10	**P3.7**	Port 3 bit 7.
		UART1_RXD	UART1 receive input.
21	-	**P4.0**	Port 4 bit 0.
22	-	**P4.1**	Port 4 bit 1.
23	-	**P4.2**	Port 4 bit 2.
24	-	**P4.3**	Port 4 bit 3.
31	-	**P4.4**	Port 4 bit 4.
32	-	**P4.5**	Port 4 bit 5.
33	-	**P4.6**	Port 4 bit 6.
34	-	**P4.7**	Port 4 bit 7.
37	-	**P5.0**	Port 5 bit 0.
38	-	**P5.1**	Port 5 bit 1.
39	-	**P5.2**	Port 5 bit 2.
40	-	**P5.3**	Port 5 bit 3.
1	-	**P5.4**	Port 5 bit 4.
8	-	**P5.5**	Port 5 bit 5.
9	-	**P5.6**	Port 5 bit 6.
12	-	**P5.7**	Port 5 bit 7.

Note:

1. All I/O pins can be configured as a interrupt pin. This feature is not listed in multi-function description.
2. UART0_TXD and UART0_RXD pins are software exchangeable by UART0PX (AUXR1.2).
3. [I2C] alternate function remapping option. I^2C pins is software switched by I2CPX (I2CON.0).
4. [STADC] alternate function remapping option. STADC pin is software switched by STADCPX(ADCCON1.6).
5. PIOx register decides which pins are PWM or GPIO.
6. UART2_TXD and UART2_RXD pin is defined by AUXR2 register. UART3_TXD, UART3_RXD, UART4_TXD and UART4_RXD pin defined by AUXR3 register.

5 BLOCK DIAGRAM

5.1 CM1003 Series Block Diagram

Figure 5.1-1 Functional Block Diagram shows the CM1003 functional block diagram and gives the outline of the device. User can find all the peripheral functions of the device in the diagram.

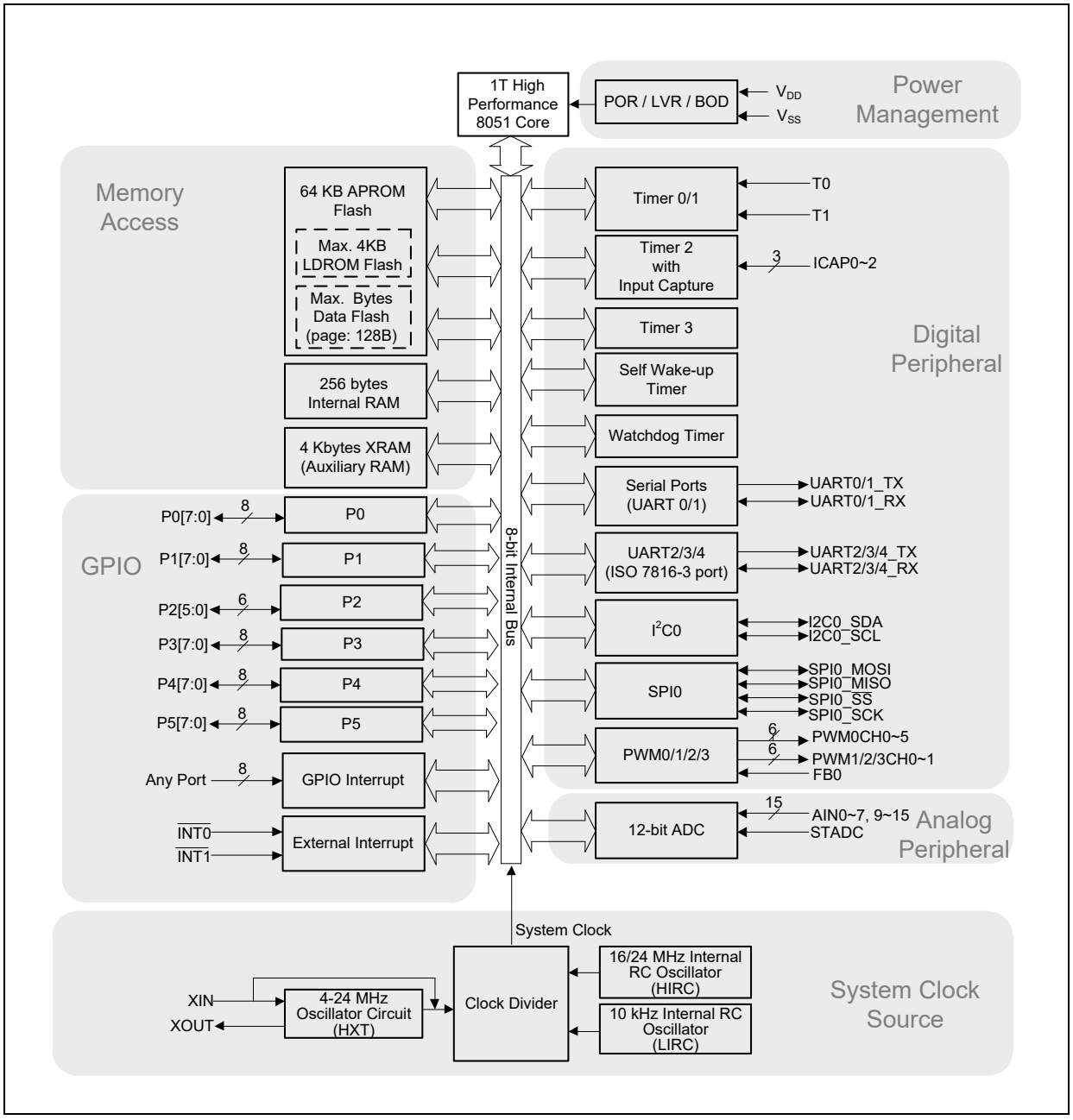


Figure 5.1-1 Functional Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 Memory Organization

6.1.1 Overview

A standard 80C51 based microcontroller divides the memory into two different sections, Program Memory and Data Memory. The Program Memory is used to store the instruction codes, whereas the Data Memory is used to store data or variations during the program execution.

The Data Memory occupies a separate address space from Program Memory. In CM1003, there are 256 bytes of internal scratch-pad RAM. For many applications those need more internal RAM, the CM1003 provides another on-chip 4 Kbytes of RAM, which is called XRAM, accessed by MOVX instruction.

The whole embedded Flash Memory, functioning as Program Memory, is divided into four blocks: Application ROM (APROM) normally for User Code, Loader ROM (LDROM) normally for Boot Code, Security protection ROM (SPROM) normally for Security Application, and CONFIG bytes for hardware initialization. Actually, APROM and LDROM function in the same way but have different size. Each block is accumulated page by page and the page size is 128 bytes. The Flash control unit supports Erase, Program, and Read modes. The external writer tools though specific I/O pins, In-Application-Programming (IAP), or In-System-Programming (ISP) can both perform these modes. The SPROM includes 128 bytes at location address FF80H ~ FFFFH and doesn't support "whole chip erase command". The last byte of SPROM (address: FFFFH) is used to identify the SPROM code is non-secured or secured mode.

6.2 System Manager

6.2.1 Clock System

6.2.1.1 Overview

The CM1003 has a wide variety of clock sources and selection features that allow it to be used in a wide range of applications while maximizing performance and minimizing power consumption. The CM1003 provides three options of the system clock sources including internal oscillator, or external clock from XIN pin via software. The CM1003 is embedded with two internal oscillators: one 10 kHz low-speed and one 16 MHz or 24 MHz high-speed, which is factory trimmed to ±2% under all conditions. A clock divider CKDIV is also available on CM1003 for adjustment of the flexibility between power consumption and operating performance.

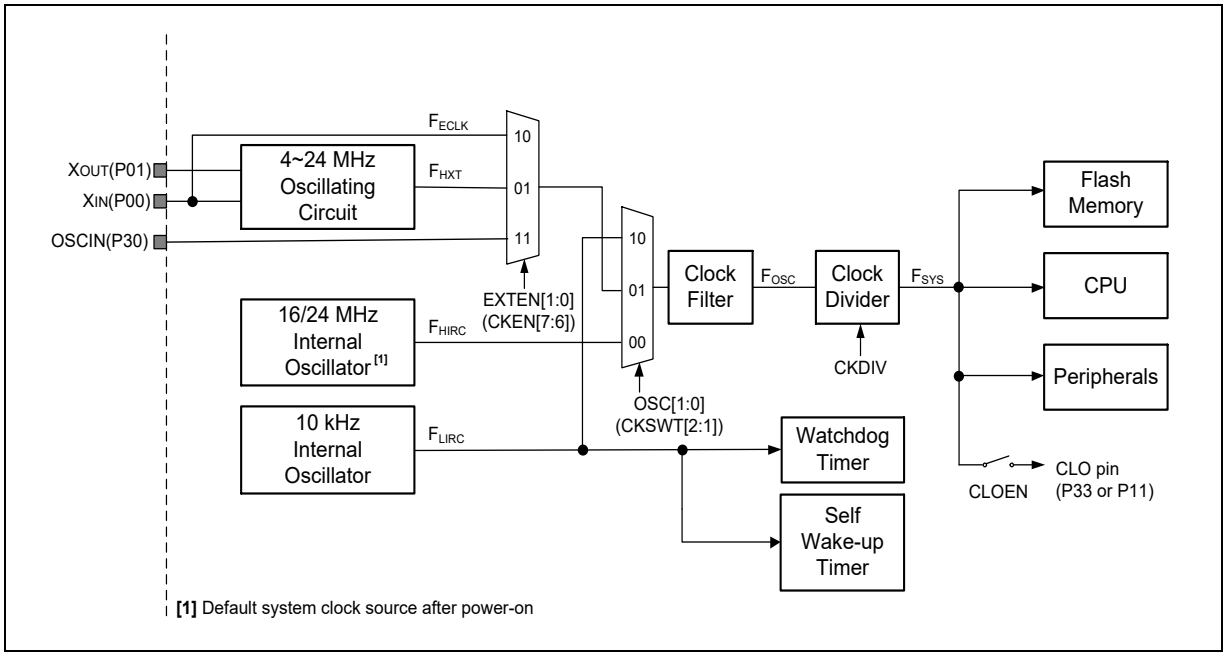


Figure 6.2-1 Clock System Block Diagram

6.2.1.2 System Clock Sources

There are a total of three system clock sources selectable in the CM1003 including high-speed internal oscillator, low-speed internal oscillator and external clock input. Each of them can be the system clock source in the CM1003. Different active system clock sources also affect multi-function of P0.0/XIN.

6.2.1.3 Internal Oscillators

There are two internal oscillators in the CM1003 – one high-speed internal oscillator (HIRC) 16 MHz or 24 MHz selectable base on HIRC24 (RCTRIM1.4) define. And one 10 kHz low-speed (LIRC). Both of them can be selected as the system clock. HIRC can be enabled by setting HIRCEN (CKEN.5). LIRC is enabled after device is powered up. User can set OSC[1:0] (CKSWT [2:1]) as [1,1] to select the HIRC as the system clock. By setting OSC[1:0] as [1,0], LIRC will be selected as the system clock. Note that after the CM1003 is powered, HIRC and LIRC will be both enabled and HIRC is default selected as the system clock source. While using internal oscillators, XIN automatically switch as one general purpose I/O P0.0 to expend the number of general purpose I/O. The I/O output mode of P0.0 can be selected by configuring P0M1 and P0M2 registers.

Since HIRC value defined by a 9-bit data, user can adjust SFR to modify HIRC value, each bit of this

value is about modify 40 kHz. Decrease this value will cause HIRC more quick and add one means HIRC speed slower about 40 kHz.

Following shows two Byte combine the 9-bit internal RC trim value. And HIRC 24 MHz define bit.

RCTRIM0 –High Speed Internal Oscillator Trim 0

Register	SFR Address	Reset Value
RCTRIM0	84H, SFR Page 0, TA protected	0000_0000b

7	6	5	4	3	2	1	0
HIRCTRIM[8:1]							
R/W							

RCTRIM1 –High Speed Internal Oscillator Trim 1

Register	SFR Address	Reset Value
RCTRIM1	85H, All SFR Pages, TA protected	0000_0000b

7	6	5	4	3	2	1	0
-	**-**	**-**	**HIRC24**	**-**	**-**	**-**	**HIRCTRIM.0**
-	-	-	R/W	-	-	-	R/W

Note: since defaut RCTRIM0 and RCTRIM1 value is base on 16 MHz, if base on this value then modify HIRC24(RCTIM1.4) to enable 24 MHz HIRC mode, the real HIRC deviation will more than 1%. Suggest reload the 24 MHz HIRC value from after UID, and check value bit 4 to confirm this value is suit for 24 MHz application.

6.2.1.4 External Crystal/Resonator or Clock Input

There are three possible clock source options of external clock sources – 4 MHz to 24 MHz high-speed crystal/resonator (HXT), and the external clock input (ECLK) through Xin pin. User should set OSC[1:0] as [1,0] then setting EXTEN[1:0] (CKEN[7:6]) to select external clock source. To select HXT as input source, define EXTEN[1:0] as [0,1]. To select ECLK as the system clock, when EXTEN[1:0] as [1,1], select external clock input via P3.0. Or as [1,0] input via P0.0.

When HXT is used as the system clock, X_{IN} and X_{OUT} are the input and output, respectively, of an internal inverting amplifier. A crystal or resonator should be connected between X_{IN} and X_{OUT} pins.

When enabling and selecting ECLK as the system clock source, the system clock is supplied via the X_{IN} pin. The common application is to drive X_{IN} with an active oscillator or clocks from another host device. Be aware that user should never feed any clock signal larger than voltage 2.4V to X_{IN} and give a DC voltage to X_{OUT} pin which value is half of X_{IN}, when ECLK mode is selected. Otherwise, it may break the device.

XTLCON – XLT Clock Control (TA Protected)

Register	SFR Address	Reset Value
XTLCON	D7H, SFR Page 2	0010_1000 b

7	6	5	4	3	2	1	0
-	HXSG						
-	R/W						

Bit	Name	Description
7	-	Reserved
6:0	HXSG	**HXT Gain Value Select** Gain control is used to enlarge the gain of crystal to make sure crystal work normally. If gain control is enabled, crystal will consume more power than gain control off. Suggestion: 000_0000 = L0. HXT frequency is 4 MHz (smallest value). 000_1100 = L1. Frequency is from 4 MHz to 12 MHz. 001_1000 = L2. Frequency is from 12MHz to 16 MHz. 010_1000 = L3. Frequency is from 16MHz to 24 MHz. 111_1111 = Reserved (Lagest value). Others = Reserved.

6.2.1.5 System Clock Switching

The CM1003 supports clock source switching on-the-fly by controlling CKSWT and CKEN registers via software. It provides a wide flexibility in application. Note that these SFRs are writing TA protected for precaution. With this clock source control, the clock source can be switched between the external clock source and the internal oscillator, even between the high and low-speed internal oscillator. However, during clock source switching, the device requires some amount of warm-up period for an original disabled clock source. Therefore, use should follow steps below to ensure a complete clock source switching. User can enable the target clock source by writing proper value into CKEN register, wait for the clock source stable by polling its status bit in CKSWT register, and switch to the target clock source by changing OSC[1:0] (CKSWT[2:1]). After these step, the clock source switching is successful and then user can also disable the original clock source if power consumption is concerned. Note that if not following the steps above, the hardware will take certain actions to deal with such illegal operations as follows.

1. If user tries to disable the current clock source by changing CKEN value, the device will ignore this action. The system clock will remain the original one and CKEN will remain the original value.
2. If user tries to switch the system clock source to a disabled one by changing OSC[1:0] value, OSC[1:0] value will be updated right away. But the system clock will remain the original one and CKSWTF flag will be set by hardware.
3. Once user switches the system clock source to an enabled but still instable one, the hardware will wait for stabilization of the target clock source and then switch to it in the background. During this waiting period, the device will continue executing the program with the original clock source and CKSWTF will be set as 1. After the stable flag of the target clock source (see CKSWT[7:3]) is set and the clock source switches successfully, CKSWTF will be cleared as 0 automatically by hardware.

CKSWT – Clock Switch

Register	SFR Address	Reset Value
CKSWT	96H, PAGE 0, TA protected	0011_0000 b

7	6	5	4	3	2	1	0
HXTST	ECKP00ST	HIRCST	LIRCST	ECKP30ST	OSC[1:0]		-
R	R	R	R	R	W		-

Bit	Name	Description
7	**HXTST**	**High-Speed External Crystal 4 MHz to 24 MHz Status** 0 = High-speed external crystal is not stable or disabled. 1 = High-speed external crystal is enabled and stable.
6	**ECKP00ST**	**External Clock P00 Input Status** 0 = External clock P00 input is not stable or disabled. 1 = External clock P00 input is enabled and stable.
5	**HIRCST**	**High-Speed Internal Oscillator 16 MHz Status** 0 = High-speed internal oscillator is not stable or disabled. 1 = High-speed internal oscillator is enabled and stable.
4	**LIRCST**	**Low-Speed Internal Oscillator 10 kHz Status** 0 = Low speed internal oscillator is not stable or is disabled. 1 = Low speed internal oscillator is enabled and stable.
3	**ECKP30ST**	**External Clock P30 Input Status** 0 = External clock P30 input is not stable or disabled. 1 = External clock P30 input is enabled and stable.
2:1	**OSC[1:0]**	**Oscillator Selection Bits** This field selects the system clock source. 00 = Internal 16 MHz oscillator. 01 = External clock source according to EXTEN[1:0] (CKEN[7:6]) setting. 10 = Internal 10 kHz oscillator. 11 = Reserved. Note that this field is write only. The read back value of this field may not correspond to the present system clock source.

CKEN – Clock Enable

Register	SFR Address	Reset Value
CKEN	97H, PAGE 0, TA protected	0011_0000 b

7	6	5	4	3	2	1	0
EXTEN[1:0]		HIRCEN	LIRCEN	-	-	-	CKSWTF
R/W		R/W	R/W	-	-	-	R

Bit	Name	Description
7:6	**EXTEN[1:0]**	**External Clock Source Enable** 11 = External clock input via OSCIN (P30) Enabled 10 = External clock input via HXTIN (P00) Enabled 01 = External crystal 4~24 MHz Enabled 00 = external clock input is disable. P30/P00/P01 work as general purpose I/O or other functions.
5	**HIRCEN**	**High-Speed Internal Oscillator 16 MHz Enable** 0 = The high-speed internal oscillator Disabled. 1 = The high-speed internal oscillator Enabled. Note that once IAP is enabled by setting IAPEN (CHPCON.0), the high-speed internal 16 MHz oscillator will be enabled automatically. The hardware will also set HIRCEN and HIRCST bits. After IAPEN is cleared, HIRCEN and EHRCST resume the original values.
4	**LIRCEN**	**Low Speed Internal Oscillator 10 kHz Enable** 0 = The low speed internal oscillator Disabled. 1 = The low speed internal oscillator Enabled. Note that when (1) WDT is enabled, (2) WKT is running by the clock source of the internal 10 kHz oscillator is enabled, a write 0 to LIRCEN will be ignored. LIRCEN is always 1 and the internal 10 kHz oscillator is always enabled.
3:1	-	Reserved
0	**CKSWTF**	**Clock Switch Fault Flag** 0 = The previous system clock source switch was successful. 1 = User tried to switch to an instable or disabled clock source at the previous system clock source switch. If switching to an instable clock source, this bit remains 1 until the clock source is stable and switching is successful.

6.2.1.6 System Clock Divider

The oscillator frequency (F_{OSC}) can be divided down, by an integer, up to 1/510 by configuring a dividing register, CKDIV, to provide the system clock (F_{SYS}). This feature makes it possible to temporarily run the MCU at a lower rate, reducing power consumption. By dividing the clock, the MCU can retain the ability to respond to events other than those that can cause interrupts (i.e. events that allow exiting the Idle mode) by executing its normal program at a lower rate. This can often result in lower power consumption than in Idle mode. This can allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of CKDIV may be changed by the program at any time without interrupting code execution.

CKDIV – Clock Divider

Register	SFR Address	Reset Value
CKDIV	95H, SFR Page 0	0000_0000b

7	6	5	4	3	2	1	0
CKDIV[7:0]							
R/W							

Bit	Name	Description
7:0	**CKDIV[7:0]**	**Clock Divider** The system clock frequency FSYS follows the equation below according to CKDIV value. $F_{SYS} = F_{OSC}$, while CKDIV = 00H, and $F_{SYS} = \frac{F_{OSC}}{2 \quad CKDIV}$, while CKDIV = 01H to FFH.

6.2.1.7 System Clock Output

The CM1003 provides a CLO pin that outputs the system clock. Its frequency is the same as F_{SYS}. The output enable bit is CLOEN (CKCON.1). CLO output stops when device is put in its Power-down mode because the system clock is turned off. Note that when noise problem or power consumption is important issue, user had better not enable CLO output.

CKCON – Clock Control

Register	SFR Address	Reset Value
CKCON	8EH, SFR Page 0	0000_0000b

7	6	5	4	3	2	1	0
-	PWMCKS	-	T1M	T0M	-	CLOEN	-
-	R/W	-	R/W	R/W	-	R/W	-

Bit	Name	Description
1	CLOEN	**System Clock Output Enable** 0 = System clock output Disabled. 1 = System clock output Enabled (from CLO pin). **Note:** CLO pin decide by AUXR5.7.

6.2.2 Power Management

6.2.2.1 Overview

The CM1003 has several features that help user to control the power consumption of the device. The power reduced feature has two option modes: Idle mode and Power-down mode, to save the power consumption. For a stable current consumption, the state and mode of each pin should be taken care of. The minimum power consumption can be attained by giving the pin state just the same as the external pulls for example output 1 if pull-high is used or output 0 if pull-low. If the I/O pin is floating, user is recommended to leave it as quasi-bidirectional mode. If P2.0 is configured as a input-only pin, it should have an external pull-up or pull-low, or enable its internal pull-up by setting P30UP (P3UP.0).

PCON – Power Control

Register	SFR Address	Reset Value
PCON	87H, All SFR Pages	POR: 0001_0000b Others: 000U _0000b

7	6	5	4	3	2	1	0
SMOD	SMOD0	Reserved	POF	GF1	GF0	PD	IDL
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
1	PD	**Power-down mode** Setting this bit puts CPU into Power-down mode. Under this mode, both CPU and peripheral clocks stop and Program Counter (PC) suspends. It provides the lowest power consumption. After CPU is woken up from Power-down, this bit will be automatically cleared via hardware and the program continue executing the interrupt service routine (ISR) of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction, which follows the instruction that put the system into Power-down mode. Note that If IDL bit and PD bit are set simultaneously, CPU will enter Power-down mode. Then it does not go to Idle mode after exiting Power-down.
0	IDL	**Idle mode** Setting this bit puts CPU into Idle mode. Under this mode, the CPU clock stops and Program Counter (PC) suspends but all peripherals keep activated. After CPU is woken up from Idle, this bit will be automatically cleared via hardware and the program continue executing the ISR of the very interrupt source that woke the system up before. After return from the ISR, the device continues execution at the instruction which follows the instruction that put the system into Idle mode.

6.2.2.2 Idle Mode

Idle mode suspends CPU processing by holding the Program Counter. No program code are fetched and run in Idle mode. It forces the CPU state to be frozen. The Program Counter (PC), Stack Pointer (SP), Program Status Word (PSW), Accumulator (ACC), and the other registers hold their contents during Idle mode. The port pins hold the logical states they had at the time Idle was activated. Generally, it saves considerable power of typical half of the full operating power.

Since the clock provided for peripheral function logic circuit like timer or serial port still remain in Idle mode, the CPU can be released from the Idle mode with any of enabled interrupt sources. User can put the device into Idle mode by writing 1 to the bit IDL (PCON.0). The instruction that sets the IDL bit is the last instruction that will be executed before the device enters Idle mode.

The Idle mode can be terminated in two ways. First, as mentioned, any enabled interrupt will cause an exit. It will automatically clear the IDL bit, terminate Idle mode, and the interrupt service routine (ISR) will be executed. After using the RETI instruction to jump out of the ISR, execution of the program will be the one following the instruction, which put the CPU into Idle mode. The second way to terminate Idle mode is with any reset other than software reset. Remember that if Watchdog reset is used to exit Idle mode, the WIDPD (WDCON.4) needs to be set 1 to let WDT keep running in Idle mode.

6.2.2.3 Power-Down Mode

Power-down mode is the lowest power state that the CM1003 can enter. It remain the power consumption as A ”Ma” level by stopping the system clock source. Both of CPU and peripheral functions like Timers or UART are frozen. Flash Memory is put into its stop mode. All activity is completely stopped and the power consumption is reduced to the lowest possible value. The device can be put into Power-down mode by writing 1 to bit PD (PCON.1). The instruction that does this action will be the last instruction to be executed before the device enters Power-down mode. In the Power-down mode, RAM maintains its content. The port pins output the values held by their own state before Power-down respectively.

There are several ways to exit the CM1003 from the Power-down mode. The first is with all resets except software reset. Brown-out reset will also wake up CPU from Power-down mode. Be sure that brown-out detection is enabled before the system enters Power-down. However, for least power consumption, it is recommended to enable low power BOD in Power-down mode. Of course the external pin reset and power-on reset will remove the Power-down status. After the external reset or power-on reset. The CPU is initialized and start executing program code from the beginning.

The second way to wake the CM1003 up from the Power-down mode is by an enabled external interrupt. The trigger on the external pin will asynchronously restart the system clock. After oscillator is stable, the device executes the interrupt service routine (ISR) for the corresponding external interrupt. After the ISR is completed, the program execution returns to the instruction after the one, which puts the device into Power-down mode and continues. Interrupts that allows to wake up CPU from Power-down mode includes external interrupt $\overline{INT0}$ and $\overline{INT1}$, pin interrupt, WDT interrupt, WKT interrupt, and brown-out interrupt.

6.2.3 Power Monitoring and Reset

6.2.3.1 Overview

To prevent incorrect execution during power up and power drop, The CM1003 provide three power monitor functions include power-on reset, low voltage reset and brown-out detection

The CM1003 has several options to place device in reset condition. It also offers the software flags to indicate the source, which causes a reset. In general, most SFR go to their Reset value irrespective of the reset condition, but there are several reset source indicating flags whose state depends on the source of reset. User can read back these flags to determine the cause of reset using software. There are five ways of putting the device into reset state. They are power-on reset, brown-out reset, external reset, WDT reset, and software reset.

6.2.3.2 Power-On Reset and Low Voltage Reset

The CM1003 incorporates an internal power-on reset (POR) and a low voltage reset (LVR). During a power-on process of rising power supply voltage V_{DD}, the POR or LVR will hold the MCU in reset mode when V_{DD} is lower than the voltage reference thresholds. This design makes CPU not access program Flash while the V_{DD} is not adequate performing the Flash reading. If an undetermined operating code is read from the program Flash and executed, this will put CPU and even the whole system in to an erroneous state. After a while, V_{DD} rises above the threshold where the system can work, the selected oscillator will start and then program code will execute from 0000H. At the same time, a power-on flag POF (PCON.4) will be set 1 to indicate a cold reset, a power-on process complete. Note that the contents of internal RAM will be undetermined after a power-on. It is recommended that user gives initial values for the RAM block.

The POF is recommended to be cleared to 0 via software to check if a cold reset or warm reset performed after the next reset occurs. If a cold reset caused by power off and on, POF will be set 1 again. If the reset is a warm reset caused by other reset sources, POF will remain 0. User may take a different course to check other reset flags and deal with the warm reset event. For detailed electrical characteristics.

PCON – Power Control

Register	SFR Address	Reset Value
PCON	87H, All SFR Pages	POR: 0001_0000b Others: 000U _0000b

7	6	5	4	3	2	1	0
SMOD	**SMOD0**	**LPR**	**POF**	**GF1**	**GF0**	**PD**	**IDL**
R/W	R/W	RW	R/W	R/W	R/W	R/W	R/W

Bit	Name	Description
4	**POF**	**Power-on Reset Flag** This bit will be set as 1 after a power-on reset. It indicates a cold reset, a power-on reset complete. This bit remains its value after any other resets. This flag is recommended to be cleared via software.

PORDIS – POR Disable

Register	SFR Address	Reset Value
PORDIS	FDH, SFR Page 0, TA protected	0000_0000 b

7	6	5	4	3	2	1	0
PORDIS[7:0]							
W							

Bit	Name	Description
7:0	**PORDIS[7:0]**	**POR Disable** To first writing 5AH to the PORDIS and immediately followed by a writing of A5H will disable POR.

LVRDIS – LVR disable

Register	SFR Address	Reset Value
EIPH1	FFH, SFR Page 1, TA protected	0000_0000 b

7	6	5	4	3	2	1	0
LVRDIS[7:0]							
W							

Bit	Name	Description
7:0	**LVRDIS[7:0]**	**LVR Disable** To first writing 5AH to the LVRDIS and immediately followed by a writing of A5H will disable LVR.

6.2.3.3 *Brown-Out Detection and Reset*

The other power monitoring function brown-out detection (BOD) circuit is used for monitoring the V_{DD} level during execution. There are eight CONFIG selectable brown-out trigger levels available for wide voltage applications. These 4 nominal levels are 2.2V, 2.7V, 3.7V and 4.4V selected via setting CBOV[2:0] (CONFIG2[6:4]). BOD level can also be changed by setting BOV[2:0] (BODCON0[6:4]) after power-on. When V_{DD} drops to the selected brown-out trigger level (V_{BOD}), the BOD logic will either reset the MCU or request a brown-out interrupt. User may decide to being reset or generating a brown-out interrupt according to different applications. V_{BOD} also can be set by software after power-on. Note that BOD output is not available until 2~3 LIRC clocks after software enabling.

The BOD will request the interrupt while V_{DD} drops below V_{BOD} while BORST (BODCON0.2) is 0. In this case, BOF (BODCON0.3) will be set as 1. After user cleared this flag whereas V_{DD} remains below V_{BOD}, BOF will not set again. BOF just acknowledge user a power drop occurs. The BOF will also be set as 1 after V_{DD} goes higher than V_{BOD} to indicate a power resuming. The BOD circuit provides an useful status indicator BOS (BODCON0.0), which is helpful to tell a brown-out event or power resuming event occurrence. If the BORST bit is set as 1, this will enable brown-out reset function. After a brown-out reset, BORF (BODCON0.1) will be set as 1 via hardware. It will not be altered by reset other than power-on. This bit can be cleared by software. Note that all bits in BODCON0 is writing protected by timed access (TA).

The CM1003 provides low power BOD mode for saving current consumption and remaining BOD functionality with limited detection response. By setting LPBOD[1:0] (BODCON1[2:1]), the BOD circuit can be periodically enabled to sense the power voltage nominally every 1.6 ms, 6.4 ms, or 25.6 ms. It saves much power but also provides low-speed power voltage sensing. Note that the hysteresis feature will disappear in low power BOD mode.

For a noise sensitive system, the CM1003 has a BOD filter which filters the power noise to avoid BOD event triggering unconsciously. The BOD filter is enabled by default and can be disabled by setting BODFLT (BODCON1.0) as 0 if user requires a rapid BOD response. The minimum brown-out detect pulse width is listed in LPBOD[1:0] (BODCON1)

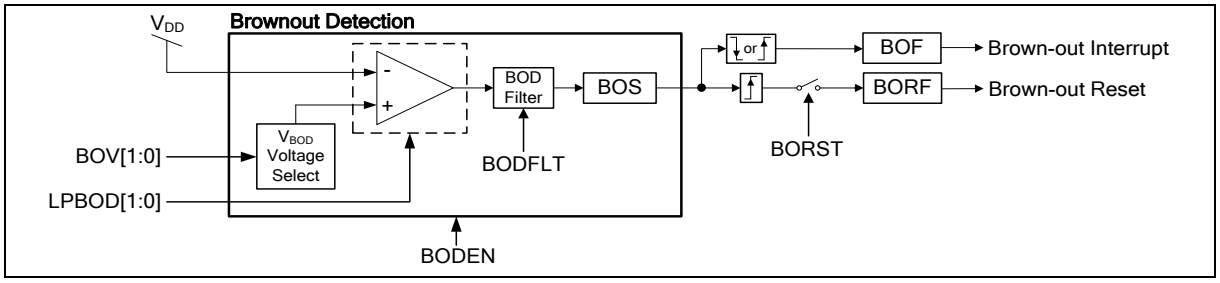


Figure 6.2-2 Brown-out Detection Block Diagram

CONFIG2

7	6	5	4	3	2	1	0
CBODEN	**-**	**CBOV[1:0]**		**BOIAP**	**CBORST**	**-**	**-**
R/W	-	R/W		R/W	R/W	-	-

Factory default value: 1111 1111b

Bit	Name	Description
7	**CBODEN**	**CONFIG Brown-Out Detect Enable** 1 = Brown-out detection circuit on. 0 = Brown-out detection circuit off.
5:4	**CBOV[1:0]**	**CONFIG Brown-Out Voltage Select** 11 = V_{BOD} is 2.2V. 10 = V_{BOD} is 2.7V. 01 = V_{BOD} is 3.7V. 00 = V_{BOD} is 4.4V.
2	**CBORST**	**CONFIG Brown-Out Reset Enable** This bit decides whether a brown-out reset is caused by a power drop below V_{BOD}. 1 = Brown-out reset Enabled. 0 = Brown-out reset Disabled.

CBODEN (CONFIG2.7)	CBORST (CONFIG2.2)	V_{DD} Level	BOF
1	1	> V_{BOD} always	0
1	0	< V_{BOD}	1
1	0	> V_{BOD}	0
0	X	X	0

Table 6.2-1 BOF Reset Value

BODCON0 – Brown-out Detection Control 0

Register	SFR Address	Reset Value
BODCON0	A3H, SFR Page 0, TA protected	POR,CCCC XC0X b BOD, UUUU XU1X b Others,UUUU XUUX b

7	6	5	4	3	2	1	0
BODEN[1]	**BOV[2:0]** [1]			**BOF**[2]	**BORST**[1]	**BORF**	**BOS**
R/W	R/W			R/W	R/W	R/W	R

Bit	Name	Description
7	**BODEN**	**Brown-Out Detection Enable** 0 = Brown-out detection circuit off. 1 = Brown-out detection circuit on. Note that BOD output is not available until 2~3 LIRC clocks after enabling.
6:4	**BOV[1:0]**	**Brown-Out Voltage Select** 11 = V_{BOD} is 2.2V. 10 = V_{BOD} is 2.7V. 01 = V_{BOD} is 3.7V. 00 = V_{BOD} is 4.4V.
3	**BOF**	**Brown-Out Interrupt Flag** This flag will be set as logic 1 via hardware after a V_{DD} dropping below or rising above V_{BOD} event occurs. If both EBOD (EIE.2) and EA (IE.7) are set, a brown-out interrupt requirement will be generated. This bit should be cleared via software.
2	**BORST**	**Brown-Out Reset Enable** This bit decides whether a brown-out reset is caused by a power drop below V_{BOD}. 0 = Brown-out reset when V_{DD} drops below V_{BOD} Disabled. 1 = Brown-out reset when V_{DD} drops below V_{BOD} Enabled.
1	**BORF**	**Brown-Out Reset Flag** When the MCU is reset by brown-out event, this bit will be set via hardware. This flag is recommended to be cleared via software.
0	**BOS**	**Brown-Out Status** This bit indicates the V_{DD} voltage level comparing with V_{BOD} while BOD circuit is enabled. It keeps 0 if BOD is not enabled. 0 = V_{DD} voltage level is higher than V_{BOD} or BOD is disabled. 1 = V_{DD} voltage level is lower than V_{BOD}. Note that this bit is read-only.

Bit	Name	Description
NOTE: 1. BODEN, BOV[2:0], and BORST are initialized by being directly loaded from CONFIG2 bit 7, [6:4], and 2 after all resets. 2. BOF reset value depends on different setting of CONFIG2 and V_{DD} voltage level. Please check Table 6.2-1 BOF Reset Value		

BODCON1 – Brown-out Detection Control 1

Register	SFR Address	Reset Value
BODCON1	ABH, SFR Page 0, TA protected	POR 0000 0001 b Others 0000 0UUU b

7	6	5	4	3	2	1	0
-	-	-	-	-	LPBOD[1:0]		BODFLT
-	-	-	-	-	R/W		R/W

Bit	Name	Description
7:3	-	Reserved
2:1	LPBOD[1:0]	**Low Power BOD Enable** 00 = BOD normal mode. BOD circuit is always enabled. 01 = BOD low power mode 1 by turning on BOD circuit every 1.6 ms periodically. 10 = BOD low power mode 2 by turning on BOD circuit every 6.4 ms periodically. 11 = BOD low power mode 3 by turning on BOD circuit every 25.6 ms periodically.
0	BODFLT	**BOD Filter Control** BOD has a filter which counts 32 clocks of FSYS to filter the power noise when MCU runs with HIRC, or ECLK as the system clock and BOD does not operates in its low power mode (LPBOD[1:0] = [0, 0]). In other conditions, the filter counts 2 clocks of LIRC. Note that when CPU is halted in Power-down mode. The BOD output is permanently filtered by 2 clocks of LIRC. The BOD filter avoids the power noise to trigger BOD event. This bit controls BOD filter enabled or disabled. 0 = BOD filter Disabled. 1 = BOD filter Enabled. (Power-on reset default value.)

BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-Out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 (1/FLIRC)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 (1/FLIRC)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 (1/ FLIRC)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 (1/FSYS) Idle mode: 32 (1/FSYS) Power-down mode: 2 (1/FLIRC)
		LIRC	2 (1/FLIRC)

BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-Out Detect Pulse Width
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 (1/FLIRC)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 (1/FLIRC)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 (1/ FLIRC)

Table 6.2-2 Minimum Brown-out Detect Pulse Width

6.2.3.4 External Reset and Hard Fault Reset

The external reset pin nRESET is an input with a Schmitt trigger. An external reset is accomplished by holding the nRESET pin low for at least 24 system clock cycles to ensure detection of a valid hardware reset signal. The reset circuitry then synchronously applies the internal reset signal. Thus, the reset is a synchronous operation and requires the clock to be running to cause an external reset.

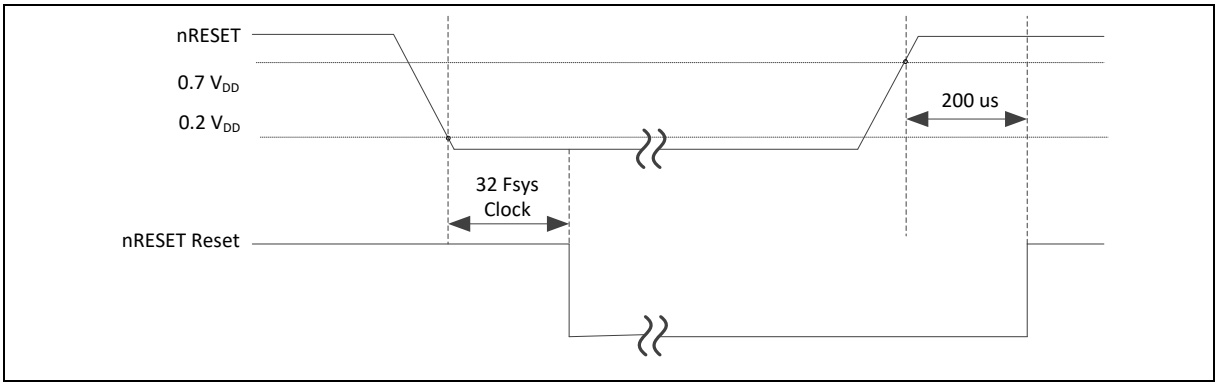


Figure 6.2-3 nRESET Reset Waveform

Once the device is in reset condition, it will remain as long as nRESET pin is low. After the nRESET high is removed, the MCU will exit the reset state and begin code executing from address 0000H. If an external reset applies while CPU is in Power-down mode, the way to trigger a hardware reset is slightly different. Since the Power-down mode stops system clock, the reset signal will asynchronously cause the system clock resuming. After the system clock is stable, MCU will enter the reset state.

There is a RSTPINF (AUXR1.6) flag, which indicates an external reset took place. After the external reset, this bit will be set as 1 via hardware. RSTPINF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software.

Hard Fault reset will occur if CPU fetches instruction address over Flash size, HardF (AUXR1.5) flag will be set via hardware. HardF will not change after any reset other than a power-on reset or the external reset itself. This bit can be cleared via software. If MCU run in OCD debug mode and OCDEN = 0, hard fault reset will be disabled. Only HardF flag be asserted.

AUXR1 – Auxiliary Register 1

Register	SFR Address	Reset Value
AUXR1	A2H , SFR Page 0	POR: 0000 0000b, Software reset: 1U00 0000b, nRESET pin: U100 0000b, Others: UUU0 0000b

7	6	5	4	3	2	1	0
SWRF	**RSTPINF**	**HardF**	**-**	**GF2**	**UART0PX**	**0**	**DPS**
R/W	R/W	R/W	-	R/W	R/W	R	R/W

Bit	Name	Description
6	**RSTPINF**	**External Reset Flag** When the MCU is reset by the external reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.
5	**HardF**	**Hard Fault Reset Flag** Once CPU fetches instruction address over Flash size while EHFI (EIE1.4)=0, MCU will reset and this bit will be set via hardware. It is recommended that the flag be cleared via software. **Note:** If MCU run in OCD debug mode and OCDEN = 0, Hard fault reset will disable. Only HardF flag be asserted.

6.2.3.5 *Watchdog Timer Reset*

The WDT is a free running timer with programmable time-out intervals and a dedicated internal clock source. User can clear the WDT at any time, causing it to restart the counter. When the selected time-out occurs but no software response taking place for a while, the WDT will reset the system directly and CPU will begin execution from 0000H.

Once a reset due to WDT occurs, the WDT reset flag WDTRF (WDCON.3) will be set. This bit keeps unchanged after any reset other than a power-on reset or WDT reset itself. User can clear WDTRF via software.

WDCON – Watchdog Timer Control

Register	SFR Address	Reset Value
WDCON	AAH, SFR Page 0, TA protected	POR 0000_0111 b WDT 0000_1UUU b Others 0000_UUUU b

7	6	5	4	3	2	1	0
WDTR	**WDCLR**	**WDTF**	**WIDPD**	**WDTRF**	**WDPS[2:0]**		
R/W	R/W	R/W	R/W	R/W	R/W		

Bit	Name	Description
3	**WDTRF**	**WDT Reset Flag** When the CPU is reset by WDT time-out event, this bit will be set via hardware. This flag is recommended to be cleared via software after reset.

6.2.3.6 *Software Reset*

The CM1003 provides a software reset, which allows the software to reset the whole system just similar to an external reset, initializing the MCU as it reset state. The software reset is quite useful in the end of an ISP progress. For example, if an ISP of Boot Code updating User Code finishes, a software reset can be asserted to re-boot CPU to execute new User Code immediately. Writing 1 to SWRST (CHPCON.7) will trigger a software reset. Note that this bit is writing TA protection. The instruction that sets the SWRST bit is the last instruction that will be executed before the device reset. See demo code below.

If a software reset occurs, SWRF (AUXR1.7) will be automatically set by hardware. User can check it as the reset source indicator. SWRF keeps unchanged after any reset other than a power-on reset or software reset itself. SWRF can be cleared via software.

CHPCON – Chip Control

Register	SFR Address	Reset Value
CHPCON	9FH, All SFR Pages, TA protected	Software 0000_00U0 b Others 0000_00C0 b

7	6	5	4	3	2	1	0
SWRST	**IAPFF**	**-**	**-**	**-**	**-**	**BS**	**IAPEN**
W	R/W	-	-	-	-	R/W	R/W

Bit	Name	Description
7	**SWRST**	**Software Reset** To set this bit as logic 1 will cause a software reset. It will automatically be cleared via hardware after reset is finished.

AUXR1 – Auxiliary Register 1

Register	SFR Address	Reset Value
AUXR1	A2H , SFR Page 0	POR: 0000 0000b, Software reset: 1U00 0000b, nRESET pin: U100 0000b, Others: UUU0 0000b

7	6	5	4	3	2	1	0
SWRF	**RSTPINF**	**HardF**	**-**	**GF2**	**UART0PX**	**0**	**DPS**
R/W	R/W	R/W	-	R/W	R/W	R	R/W

Bit	Name	Description
7	**SWRF**	**Software Reset Flag** When the MCU is reset via software reset, this bit will be set via hardware. It is recommended that the flag be cleared via software.

The software demo code is listed below.

```
    ANL  AUXR1,#01111111b ;software reset flag clear
    CLR  EA
    MOV  TA,#0Aah
    MOV  TA,#55h
    ORL  CHPCON,#10000000b  ;software reset
```

6.2.3.7 *Boot Select*

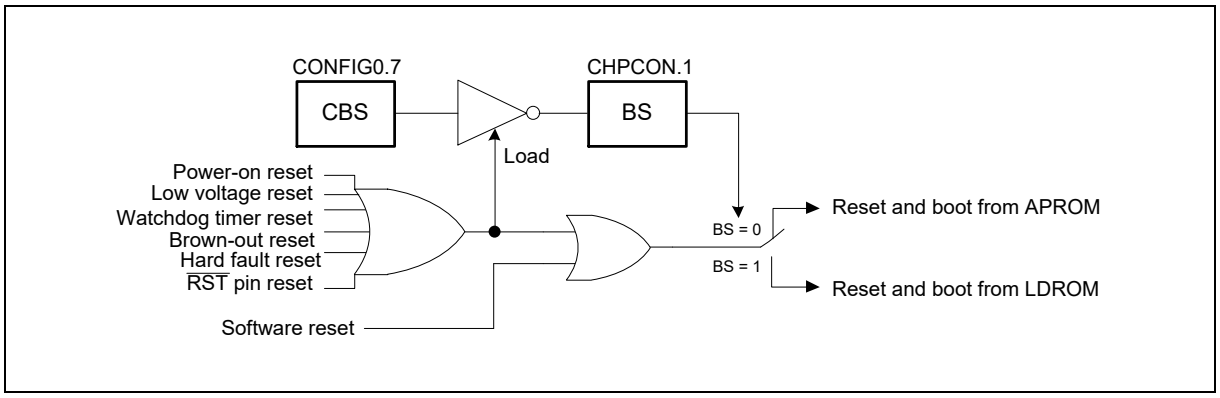


Figure 6.2-4 Boot Selecting Diagram

The CM1003 provides user a flexible boot selection for variant application. The SFR bit BS in CHPCON.1 determines MCU booting from APROM or LDROM after any source of reset. If reset occurs and BS is 0, MCU will reboot from address 0000H of APROM. Else, the CPU will reboot from address 0000H of LDROM. Note that BS is loaded from the inverted value of CBS bit in CONFIG0.7 after all resets except software reset.

CONFIG0

7	6	5	4	3	2	1	0
CBS	**-**	**OCDPWM**	**OCDEN**	**-**	**-**	**LOCK**	**-**
R/W	-	R/W	R/W	-	-	R/W	-

Factory default value: 1111 1111b

Bit	Name	Description
7	**CBS**	**CONFIG Boot Select** This bit defines from which block that MCU re-boots after resets except software reset. 1 = MCU will re-boot from APROM after resets except software reset. 0 = MCU will re-boot from LDROM after resets except software reset.

CHPCON – Chip Control

Register	SFR Address	Reset Value
CHPCON	9FH, All SFR Pages, TA protected	Software 0000_00U0 b Others 0000_00C0 b

7	6	5	4	3	2	1	0
SWRST	IAPFF	-	-	-	-	BS[1]	IAPEN
W	R/W	-	-	-	-	R/W	R/W

Bit	Name	Description
1	BS	**Boot Select** This bit defines from which block that MCU re-boots after all resets. 0 = MCU will re-boot from APROM after all resets. 1 = MCU will re-boot from LDROM after all resets.
Note: BS is initialized by being loaded from the inverted value of CBS bit in CONFIG0.7 after resets except software reset. It keeps unchanged after software reset.		

After the MCU is released from reset state, the hardware will always check the BS bit instead of the CBS bit to determine from which block that the device reboots.

6.2.3.8 Reset State

The reset state besides power-on reset does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. After the power-on reset the RAM contents will be indeterminate.

After a reset, most of SFR go to their initial values except bits, which are affected by different reset events.. The Program Counter is forced to 0000H and held as long as the reset condition is applied. Note that the Stack Pointer is also reset to 07H and thus the stack contents may be effectively lost during the reset event even though the RAM contents are not altered.

After a reset, all peripherals and interrupts are disabled. The I/O port latches resumes FFH and I/O mode input-only.

6.2.4 Interrupt System

6.2.4.1 Overview

The purpose of the interrupt is to make the software deal with unscheduled or asynchronous events. The CM1003 has a four-priority-level interrupt structure with 24 interrupt sources. Each of the interrupt sources has an individual priority setting bits, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled. When an interrupt occurs, the CPU is expected to service the interrupt. This service is specified as an Interrupt Service Routine (ISR). The ISR resides at a predetermined address as shown in Table 6.2-3 Interrupt Vectors. When the interrupt occurs if enabled, the CPU will vector to the respective location depending on interrupt source, execute the code at this location, stay in an interrupt service state until the ISR is done. Once an ISR has begun, it can be interrupted only by a higher priority interrupt. The ISR should be terminated by a return from interrupt instruction RETI. This instruction will force the CPU return to the instruction that would have been next when the interrupt occurred.

Source	Vector Addess	Vector Number	Source	Vector Address	Vector Number
Reset	0000H	-	Input capture interrupt	0063H	12
External interrupt 0	0003H	0	PWM0 interrupt	006BH	13
Timer 0 overflow	000BH	1	Fault Brake interrupt	0073H	14
External interrupt 1	0013H	2	Serial port 1 interrupt	007BH	15
Timer 1 overflow	001BH	3	Timer 3 overflow	0083H	16
Serial port 0 interrupt	0023H	4	Self Wake-up Timer interrupt	008BH	17
Timer 2 event	002BH	5	PWM1 interrupt	0093H	18
I^2C status/timer-out interrupt	0033H	6	PWM2 interrupt	009BH	19
Pin interrupt	003BH	7	PWM3 interrupt	00A3H	20
Brown-out detection interrupt	0043H	8	SC0 interrupt	00ABH	21
SPI interrupt	004BH	9	SC1 interrupt	00B3H	22
WDT interrupt	0053H	10	SC2 interrupt	00BBH	23
ADC interrupt	005BH	11			

Table 6.2-3 Interrupt Vectors

6.3 Flash Memory Control

6.3.1 In-Application-Programming (IAP)

Unlike RAM's real-time operation, to update Flash Data often takes long time. Furthermore, it is a quite complex timing procedure to erase, program, or read Flash Data. The CM1003 carried out the Flash operation with convenient mechanism to help user re-programming the Flash content by In-Application-Programming (IAP). IAP is an in-circuit electrical erasure and programming method through software.

After IAP enabling by setting IAPEN (CHPCON.0 with TA protected) and setting the enable bit in IAPUEN that allows the target block to be updated, user can easily fill the 16-bit target address in IAPAH and IAPAL, data in IAPFD, and command in IAPCN. Then the IAP is ready to begin by setting a triggering bit IAPGO (IAPTRG.0). Note that IAPTRG is also TA protected. At this moment, the CPU holds the Program Counter and the built-in IAP automation takes over to control the internal charge-pump for high voltage and the detail signal timing. The erase and program time is internally controlled disregard of the operating voltage and frequency. Nominally, a page-erase time is 5 ms and a byte-program time is 23.5 μs. After IAP action completed, the Program Counter continues to run the following instructions. The IAPGO bit will be automatically cleared. An IAP failure flag, IAPFF (CHPCON.6), can be check whether the previous IAP operation was successful or not. Through this progress, user can easily erase, program, and verify the Flash Memory by just taking care of pure software.

6.3.2 In-Circuit-Programming (ICP)

The Flash Memory can be programmed by "In-Circuit-Programming" (ICP). If the product is just under development or the end product needs firmware updating in the hand of an end customer, the hardware programming mode will make repeated programming difficult and inconvenient. ICP method makes it easy and possible without removing the microcontroller from the system. ICP mode also allows customers to manufacture circuit boards with un-programmed devices. Programming can be done after the assembly process allowing the device to be programmed with the most recent firmware or a customized firmware.

There are three signal pins, nRESET, ICE_DAT, and ICE_CLK, involved in ICP function. nRESET is used to enter or exit ICP mode. ICE_DAT is the data input and output pin. ICE_CLK is the clock input pin, which synchronizes the data shifted in to or out from MCU under programming. User should leave these three pins plus V_{DD} and VSS pins on the circuit board to make ICP possible.

Nuvoton provides ICP tool for CM1003, which enables user to easily perform ICP through Nuvoton ICP programmer. The ICP programmer developed by Nuvoton has been optimized according to the electric characteristics of MCU. It also satisfies the stability and efficiency during production progress. For more details, please visit Nuvoton 8-bit Microcontroller website: Nuvoton 80C51 Microcontroller Technical Support.

6.3.3 On-Chip-Debugger (OCD)

6.3.3.1 Overview

The CM1003 is embedded in an on-chip-debugger (OCD) providing developers with a low cost method for debugging user code, which is available on each package. The OCD gives debug capability of complete program flow control with eight hardware address breakpoints, single step, free running, and non-intrusive commands for memory access. The OCD system does not occupy any locations in the memory map and does not share any on-chip peripherals.

When the OCDEN (CONFIG0.4) is programmed as 0 and LOCK (CONFIG0.1) remains un-programmed as 1, the OCD is activated. The OCD cannot operate if chip is locked. The OCD system uses a two-wire serial interface, ICE_DAT and ICE_CLK, to establish communication between the

target device and the controlling debugger host. ICE_DAT is an input/output pin for debug data transfer and ICE_CLK is an input pin for synchronization with ICE_DAT data. The P2.0/nRESET pin is also necessary for OCD mode entry and exit. The CM1003 supports OCD with Flash Memory control path by ICP writer mode, which shares the same three pins of OCD interface.

6.3.4 96-Bit Unique Code

Before shipping out, each CM1003 chip was factory pre-programmed with a 96-bit width serial number, which is guaranteed to be unique. The serial number is called Unique Code. The user can read the Unique Code only by IAP command.

6.4 General Purpose I/O (GPIO)

6.4.1 Functional Description

6.4.1.1 GPIO Mode

The CM1003 has a maximum of 46 general purpose I/O pins which 45 bit-addressable general I/O pins grouped as 6 ports, P0 to P5, and 1 input only pin as P20. Each port has its port control register (Px register). The writing and reading of a port control register have different meanings. A write to port control register sets the port output latch logic value, whereas a read gets the port pin logic state. These four modes are quasi-bidirectional (standard 8051 port structure), push-pull, input-only, and open-drain modes. Each port spends two special function registers PxM1 and PxM2 to select the I/O mode of port Px. Note that the default configuration of is input-only (high-impedance) after any reset.

6.5 Timer

6.5.1 Timer/Counter 0 And 1

6.5.1.1 Overview

Timer/Counter 0 and 1 on CM1003 are two 16-bit Timers/Counters. Each of them has two 8-bit registers those form the 16-bit counting register. For Timer/Counter 0 they are TH0, the upper 8-bit register, and TL0, the lower 8-bit register. Similarly Timer/Counter 1 has two 8-bit registers, TH1 and TL1. TCON and TMOD can configure modes of Timer/Counter 0 and 1.

The Timer or Counter function is selected by the C/$\overline{T}$ bit in TMOD. Each Timer/Counter has its own selection bit. TMOD.2 selects the function for Timer/Counter 0 and TMOD.6 selects the function for Timer/Counter 1

When configured as a “Timer”, the timer counts the system clock cycles. The timer clock is 1/12 of the system clock (F_{SYS}) for standard 8051 capability or direct the system clock for enhancement, which is selected by T0M (CKCON.3) bit for Timer 0 and T1M (CKCON.4) bit for Timer 1. In the “Counter” mode, the countering register increases on the falling edge of the external input pin T0. If the sampled value is high in one clock cycle and low in the next, a valid 1-to-0 transition is recognized on T0 or T1 pin.

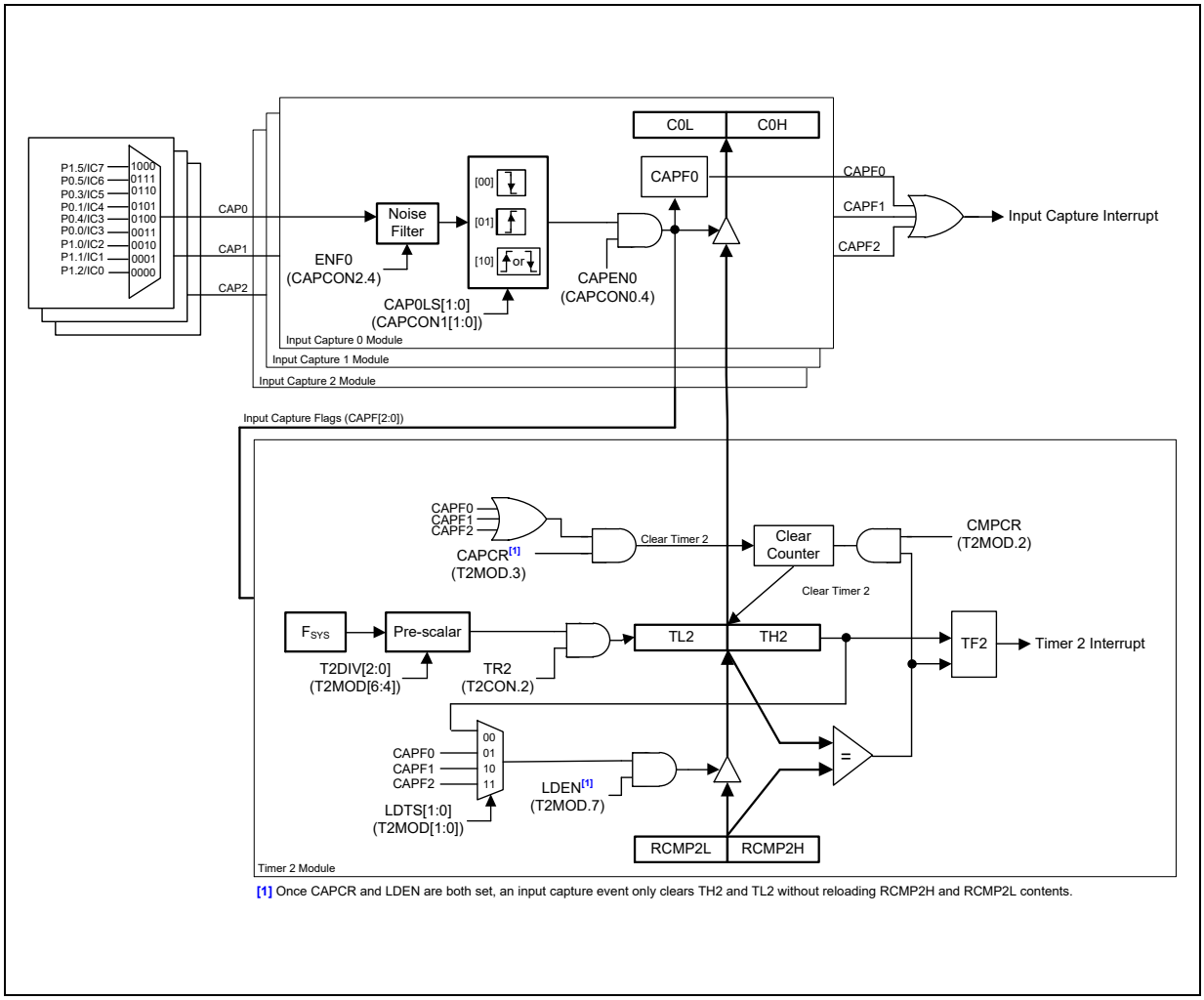
The Timers 0 and 1 can be configured to automatically to toggle output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. This function is enabled by control bits T0OE and T1OE in the CKCON register, and apply to Timer 0 and Timer 1 respectively. The port outputs will be logic 1 prior to the first timer overflow when this mode is turned on. In order for this mode to function, the C/$\overline{T}$ bit should be cleared selecting the system clock as the clock source for the timer.

Note that the TH0 (TH1) and TL0 (TL1) are accessed separately. It is strongly recommended that in mode 0 or 1, user should stop Timer temporally by clearing TR0 (TR1) bit before reading from or writing to TH0 (TH1) and TL0 (TL1). The free-running reading or writing may cause unpredictable result.

6.5.2 Timer2 And Input Capture

6.5.2.1 Overview

Timer 2 is a 16-bit up counter cascaded with TH2, the upper 8 bits register, and TL2, the lower 8 bit register. Equipped with RCMP2H and RCMP2L, Timer 2 can operate under compare mode and auto-reload mode selected by CM/$\overline{RL2}$ (T2CON.0). An 3-channel input capture module makes Timer 2 detect and measure the width or period of input pulses. The results of 3 input captures are stores in C0H and C0L, C1H and C1L, C2H and C2L individually. The clock source of Timer 2 is from the system clock pre-scaled by a clock divider with 8 different scales for wide field application. The clock is enabled when TR2 (T2CON.2) is 1, and disabled when TR2 is 0. The following registers are related to Timer 2 function.



[1] Once CAPCR and LDEN are both set, an input capture event only clears TH2 and TL2 without reloading RCMP2H and RCMP2L contents.

Figure 6.5-1 Timer 2 Block Diagram

6.5.3 Timer 3

6.5.3.1 Overview

Timer 3 is implemented simply as a 16-bit auto-reload, up-counting timer. The user can select the pre-scale with T3PS[2:0] (T3CON[2:0]) and fill the reload value into RH3 and RL3 registers to determine its overflow rate. User then can set TR3 (T3CON.3) to start counting. When the counter rolls over FFFFH, TF3 (T3CON.4) is set as 1 and a reload is generated and causes the contents of the RH3 and RL3 registers to be reloaded into the internal 16-bit counter. If ET3 (EIE1.1) is set as 1, Timer 3 interrupt service routine will be served. TF3 is auto-cleared by hardware after entering its interrupt service routine.

Timer 3 can also be the baud rate clock source of both UARTs.

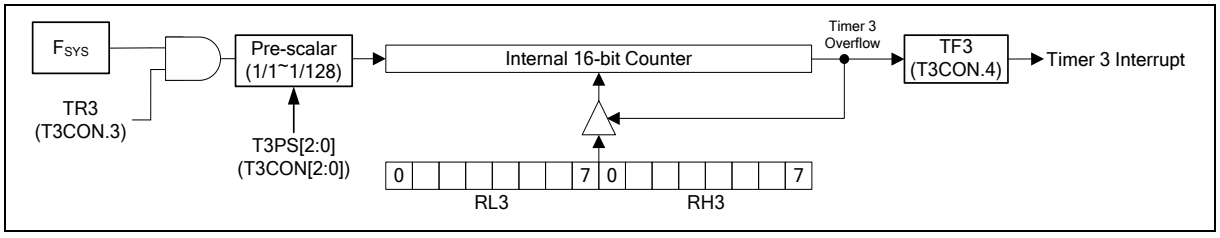


Figure 6.5-2 Timer 3 Block Diagram

6.6 Watchdog Timer (WDT)

6.6.1 Overview

The CM1003 provides one Watchdog Timer (WDT). It can be configured as a time-out reset timer to reset whole device. Once the device runs in an abnormal status or hangs up by outward interference, a WDT reset recover the system. It provides a system monitor, which improves the reliability of the system. Therefore, WDT is especially useful for system that is susceptible to noise, power glitches, or electrostatic discharge. The WDT also can be configured as a general purpose timer, of which the periodic interrupt serves as an event timer or a durational system supervisor in a monitoring system, which is able to operate during Idle or Power-down mode. WDTEN[3:0] (CONFIG4[7:4]) initialize the WDT to operate as a time-out reset timer or a general purpose timer.

The Watchdog time-out interval is determined by the formula $\frac{1}{F_{LIRC}} \text{ clock divider scalar } 64$, where F_{LIRC} is the frequency of internal 10 kHz oscillator. The following table shows an example of the Watchdog time-out interval with different pre-scales.

WDPS.2	WDPS.1	WDPS.0	Clock Divider Scale	WDT Time-Out Timing[1]
0	0	0	1/1	6.40 ms
0	0	1	1/4	25.60 ms
0	1	0	1/8	51.20 ms
0	1	1	1/16	102.40 ms
1	0	0	1/32	204.80 ms
1	0	1	1/64	409.60 ms
1	1	0	1/128	819.20 ms
1	1	1	1/256	1.638 s
Note: This is an approximate value since the deviation of LIRC.				

Table 6.6-1 Watchdog Timer-out Interval Under Different Pre-scalars

6.7 Self Wake-Up Timer (WKT)

6.7.1 Overview

The CM1003 has a dedicated Self Wake-up Timer (WKT), which serves for a periodic wake-up timer in low power mode or for general purpose timer. WKT remains counting in Idle or Power-down mode. When WKT is being used as a wake-up timer, a start of WKT can occur just prior to entering a power management mode. WKT has one clock source, internal 10 kHz. Note that the system clock frequency must be twice over WKT clock. If WKT starts counting, the selected clock source will remain active once the device enters Idle or Power-down mode. Note that the selected clock source of WKT will not automatically enabled along with WKT configuration. User should manually enable the selected clock source and waiting for stability to ensure a proper operation.

The WKT is implemented simply as a 8-bit auto-reload, up-counting timer with pre-scale 1/1 to 1/2048 selected by WKPS[2:0] (WKCON[2:0]). User fills the reload value into RWK register to determine its overflow rate. The WKTR (WKCON.3) can be set to start counting. When the counter rolls over FFH, WKTF (WKCON.4) is set as 1 and a reload is generated and causes the contents of the RWK register to be reloaded into the internal 8-bit counter. If EWKT (EIE1.2) is set as 1, WKT interrupt service routine will be served.

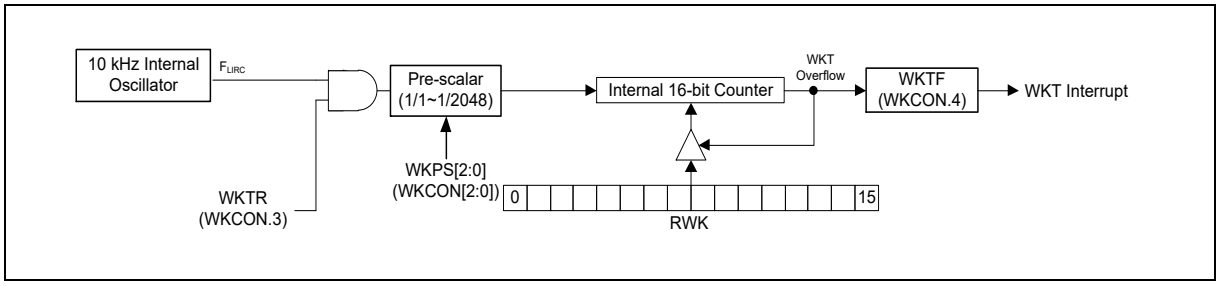


Figure 6.7-1 Self Wake-Up Timer Block Diagram

6.8 Pulse Width Modulated (PWM)

6.8.1 Overview

The PWM (Pulse Width Modulation) signal is a useful control solution in wide application field. It can used on motor driving, fan control, backlight brightness tuning, LED light dimming, or simulating as a simple digital to analog converter output through a low pass filter circuit.

The CM1003 PWM0 is especially designed for motor control by providing three pairs, maximum 16-bit resolution of PWM0 output with programmable period and duty. The architecture makes user easy to drive the one-phase or three-phase brushless DC motor (BLDC), or three-phase AC induction motor. Each of six PWM can be configured as one of independent mode, complementary mode, or synchronous mode. If the complementary mode is used, a programmable dead-time insertion is available to protect MOS turn-on simultaneously. The PWM waveform can be edge-aligned or center-aligned with variable interrupt points.

The CM1003 PWM1/2/3 provide individual configurable period and duty. maximum 16-bit resolution output. Each of two PWM1/2/3 can be configured as one of independent mode, complementary mode, or synchronous mode.The PWM1/2/3 waveform can be edge-aligned or center-aligned with variable interrupt points.

PWM output pin define and enable control register table.

PWM Channel	Output Pin	Control register 1			Control register2		
		SFR Byte Name	Bit name	Value	SFR Byte Name	Bit name	Value
PWM0_CH0	P1.2	PIOCON0	PIO12	1	AUXR4[1:0]	PWM1C0P	00
	P3.3	PIOCON2	PIO33	1	-	-	-
PWM0_CH1	P1.1	PIOCON0	PIO11	1	AUXR4[3:2]	PWM1C1P	00
	P1.4	PIOCON1	PIO14	1	AUXR4[3:2]	PWM1C1P	00
PWM0_CH2	P0.5	PIOCON1	PIO05	1	AUXR4[5:4]	PWM2C0P	00
	P1.0	PIOCON0	PIO10	1	-	-	-
PWM0_CH3	P0.4	PIOCON1	PIO04	1	AUXR4[7:6]	PWM2C1P	00
	P0.0	PIOCON0	PIO00	1	AUXR4[7:6]	PWM2C1P	00
PWM0_CH4	P0.1	PIOCON0	PIO01	1	AUXR5[1:0]	PWM3C0P	00
PWM0_CH5	P0.3	PIOCON0	PIO03	1	AUXR5[3:2]	PWM3C1P	00
	P1.5	PIOCON1	PIO15	1	AUXR5[3:2]	PWM3C1P	00
PWM1_CH0	P2.3	PIOCON2	PIO23	1	AUXR4[1:0]	PWM1C0P	01
	P1.2	PIOCON0	PIO12	1			10
PWM1_CH1	P2.2	PIOCON2	PIO22	1	AUXR4[3:2]	PWM1C1P	01
	P1.4	PIOCON1	PIO14	1			10
	P1.1	PIOCON0	PIO11	1			11
PWM2_CH0	P2.1	PIOCON2	PIO21	1	AUXR4[5:4]	PWM2C0P	00
	P1.0	PIOCON0	PIO10	1			01
	P0.5	PIOCON1	PIO05	1			10

PWM Channel	Output Pin	Control register 1			Control register2		
		SFR Byte Name	Bit name	Value	SFR Byte Name	Bit name	Value
PWM2_CH1	P3.0	PIOCON2	PIO30	1	AUXR4[7:6]	PWM2C1P	00
	P3.1	PIOCON2	PIO31	1			01
	P0.0	PIOCON0	PIO00	1			10
	P0.4	PIOCON1	PIO04	1			11
PWM3_CH0	P3.2	PIOCON2	PIO32	1	AUXR5[1:0]	PWM3C0P	01
	P0.1	PIOCON0	PIO01	1			10
	P1.7	PIOCON1	PIO17	1			-
PWM3_CH1	P3.4	PIOCON2	PIO34	1	AUXR5[3:2]	PWM3C1P	01
	P1.5	PIOCON1	PIO15	1			10
	P0.3	PIOCON0	PIO03	1			11

Table 6.8-1 PWM Pin Define and Enable Control Register

6.9 Serial Port (UART0 & UART1)

6.9.1 Overview

The CM1003 includes two enhanced full duplex serial ports enhanced with automatic address recognition and framing error detection. As control bits of these two serial ports are implemented the same. Generally speaking, in the following contents, there will not be any reference to serial port 1, but only to serial port 0.

Each serial port supports one synchronous communication mode, Mode 0, and three modes of full duplex UART (Universal Asynchronous Receiver and Transmitter), Mode 1, 2, and 3. This means it can transmit and receive simultaneously. The serial port is also receiving-buffered, meaning it can commence reception of a second byte before a previously received byte has been read from the register. The receiving and transmitting registers are both accessed at SBUF. Writing to SBUF loads the transmitting register, and reading SBUF accesses a physically separate receiving register. There are four operation modes in serial port. In all four modes, transmission initiates by any instruction that uses SBUF as a destination register.

6.10 ISO 7816-3 Interface (SC0~2 & UART2 ~ 4)

6.10.1 Overview

The CM1003 series provides ISO 7816-3 Interface controller (SC controller) with asynchronous protocal based on ISO/IEC 7816-3 standard. Software controls GPIO pins as the smartcard reset function and card detection function. This controller also provides UART emulation for high precision baud rate communication.

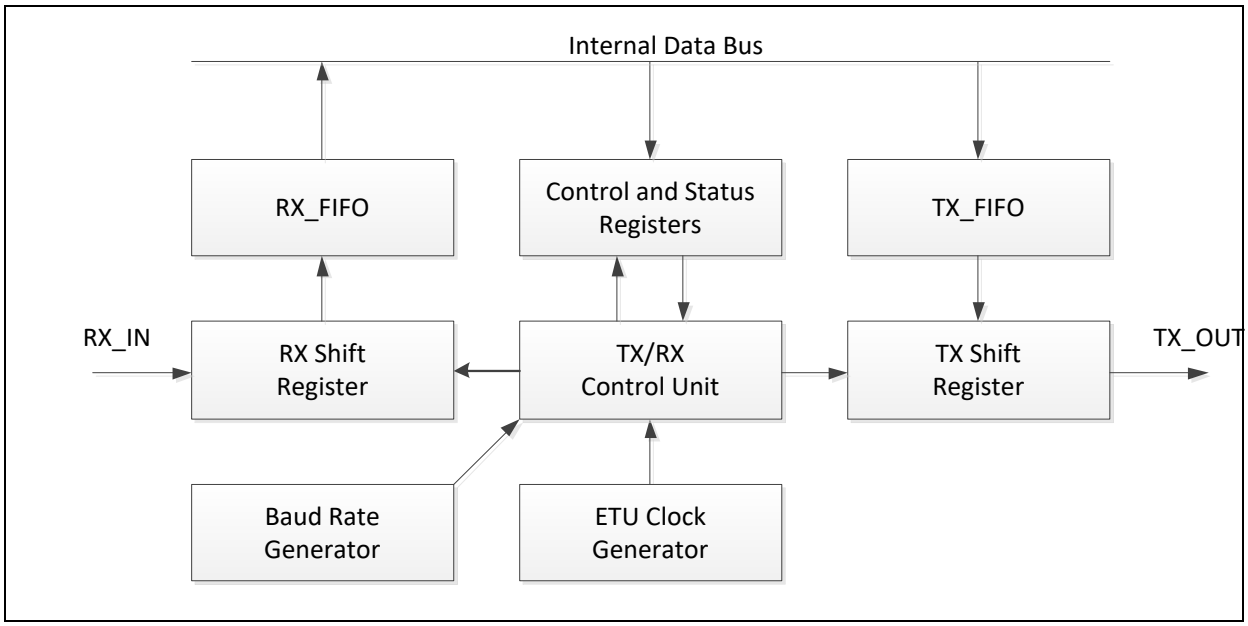


Figure 6.10-1 SC Controller Block Diagram

- ISO-7816-3 T = 0, T = 1 compliant
- Programmable transmission clock frequency
- Programmable extra guard time selection
- Supports auto inverse convention function
- Supports UART mode
  - Full duplex, asynchronous communications
  - Supports programmable baud rate generator for each channel
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting SCnEGT register
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1 or 2 stop bit generation

Following is the ISO 7816-3 multi function pin define

URAT Pin	SC Pin	Pin Name	SFR Define		
			SFR Byte Name	SFR Bit Name	Value
UART2_TXD	SC0_CLK	P0.3	AUXR2[7:6]	UART2TXP	01
		P3.0			10

URAT Pin	SC Pin	Pin Name	SFR Define		
			SFR Byte Name	SFR Bit Name	Value
UART2_RXD	SC0_DAT	P0.4	AUXR2[5:4]	UART2RXP	01
		P1.7			10
UART3_TXD	SC1_CLK	P1.2	AUXR3[3:2]	UART3TXP	01
		P1.5			10
		P0.5			11
UART3_RXD	SC1_DAT	P1.1	AUXR3[1:0]	UART3RXP	01
		P2.5			10
		P3.4			11
UART4_TXD	SC2_CLK	P2.3	AUXR3[7:6]	UART4TXP	01
UART4_RXD	SC2_DAT	P2.2	AUXR3[5:4]	UART4RXP	01

Table 6.10-1 Smart Card or UART Pin Define and Enable Control Register

6.11 Inter-Integrated Circuit (I^2C)

6.11.1 Overview

The CM1003 provides two Inter-Integrated Circuit (I^2C) bus to serves as an serial interface between the microcontrollers and the I^2C devices such as EEPROM, LCD module, temperature sensor, and so on. The I^2C bus used two wires design (a serial data line I2C0_SDA and a serial clock line I2C0_SCL) to transfer information between devices.

The I^2C bus uses bi-directional data transfer between masters and slaves. There is no central master and the multi-master system is allowed by arbitration between simultaneously transmitting masters. The serial clock synchronization allows devices with different bit rates to communicate via one serial bus. The I^2C bus supports four transfer modes including master transmitter, master receiver, slave receiver, and slave transmitter. The I^2C interface only supports 7-bit addressing mode. A special mode General Call is also available. The I^2C can meet both standard (up to 100kbps) and fast (up to 400k bps) speeds.

6.12 Serial Peripheral Interface (SPI)

6.12.1 Overview

The CM1003 provides two Serial Peripheral Interface (SPI) block to support high-speed serial communication. SPI is a full-duplex, high-speed, synchronous communication bus between microcontrollers or other peripheral devices such as serial EEPROM, LCD driver, or D/A converter. It provides either Master or Slave mode, high-speed rate up to $F_{SYS}/2$, transfer complete and write collision flag. For a multi-master system, SPI supports Master Mode Fault to protect a multi-master conflict.

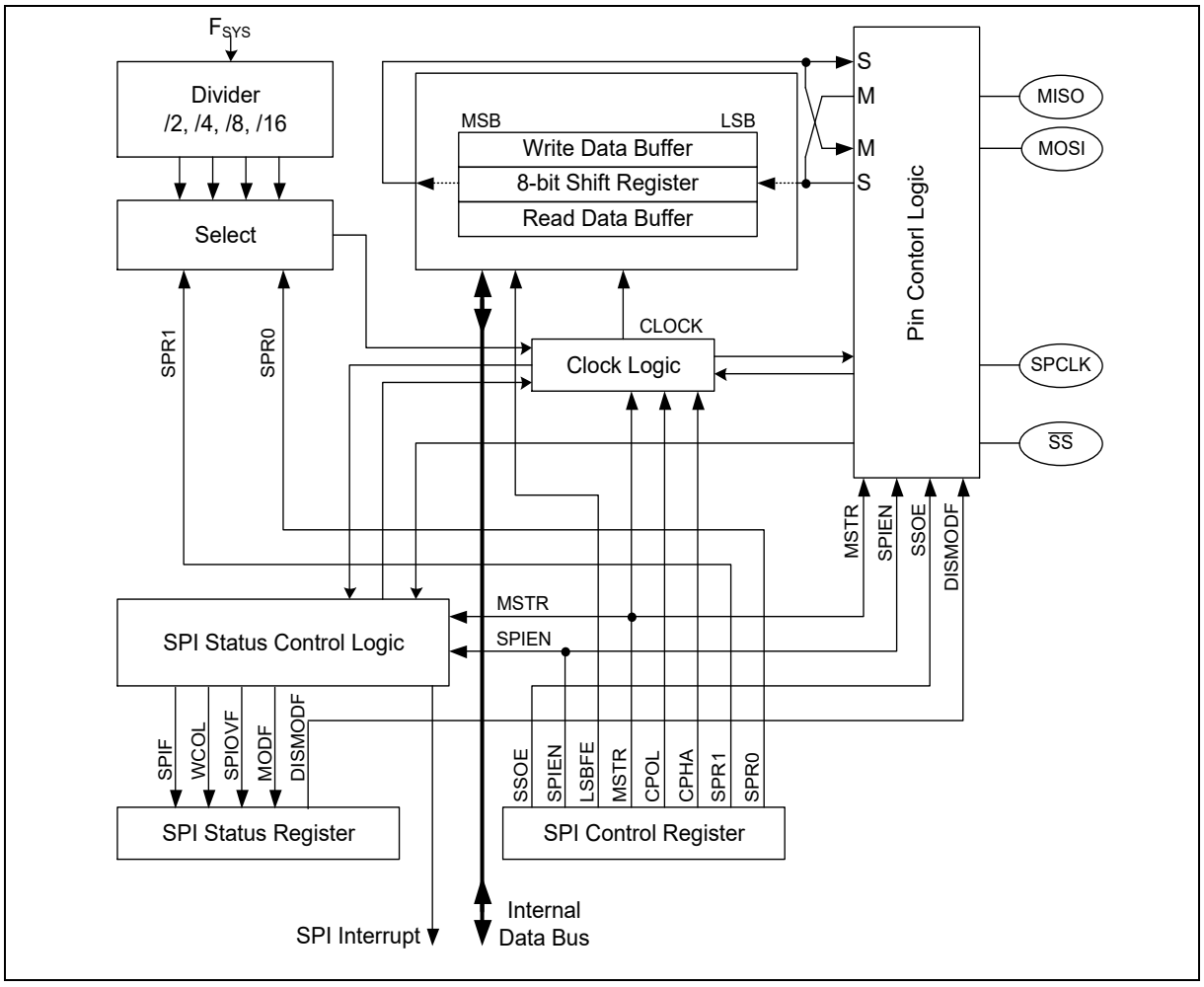


Figure 6.12-1 SPI Block Diagram

Figure15.1 SPI Block Diagram shows SPI block diagram. It provides an overview of SPI architecture in this device. The main blocks of SPI are the SPI control register logic, SPI status logic, clock rate control logic, and pin control logic. For a serial data transfer or receiving, The SPI block exists a write data buffer, a shift out register and a read data buffer. It is double buffered in the receiving and transmit directions. Transmit data can be written to the shifter until when the previous transfer is not complete. Receiving logic consists of parallel read data buffer so the shift register is free to accept a second data, as the first received data will be transferred to the read data buffer.

The four pins of SPI interface are Master-In/Slave-Out (MISO), Master-Out/Slave-In (MOSI), Shift

Clock (SPCLK), and Slave Select ($\overline{SS}$). The MOSI pin is used to transfer a 8-bit data in series from the Master to the Slave. Therefore, MOSI is an output pin for Master device and an input for Slave. Respectively, the MISO is used to receive a serial data from the Slave to the Master.

The SPCLK pin is the clock output in Master mode, but is the clock input in Slave mode. The shift clock is used to synchronize the data movement both in and out of the devices through their MOSI and MISO pins. The shift clock is driven by the Master mode device for eight clock cycles. Eight clocks exchange one byte data on the serial lines. For the shift clock is always produced out of the Master device, the system should never exist more than one device in Master mode for avoiding device conflict.

Each Slave peripheral is selected by one Slave Select pin ($\overline{SS}$). The signal should stay low for any Slave access. When $\overline{SS}$ is driven high, the Slave device will be inactivated. If the system is multi-slave, there should be only one Slave device selected at the same time. In the Master mode MCU, the $\overline{SS}$ pin does not function and it can be configured as a general purpose I/O. However, $\overline{SS}$ can be used as Master Mode Fault detection via software setting if multi-master environment exists. The CM1003 also provides auto-activating function to toggle $\overline{SS}$ between each byte-transfer.

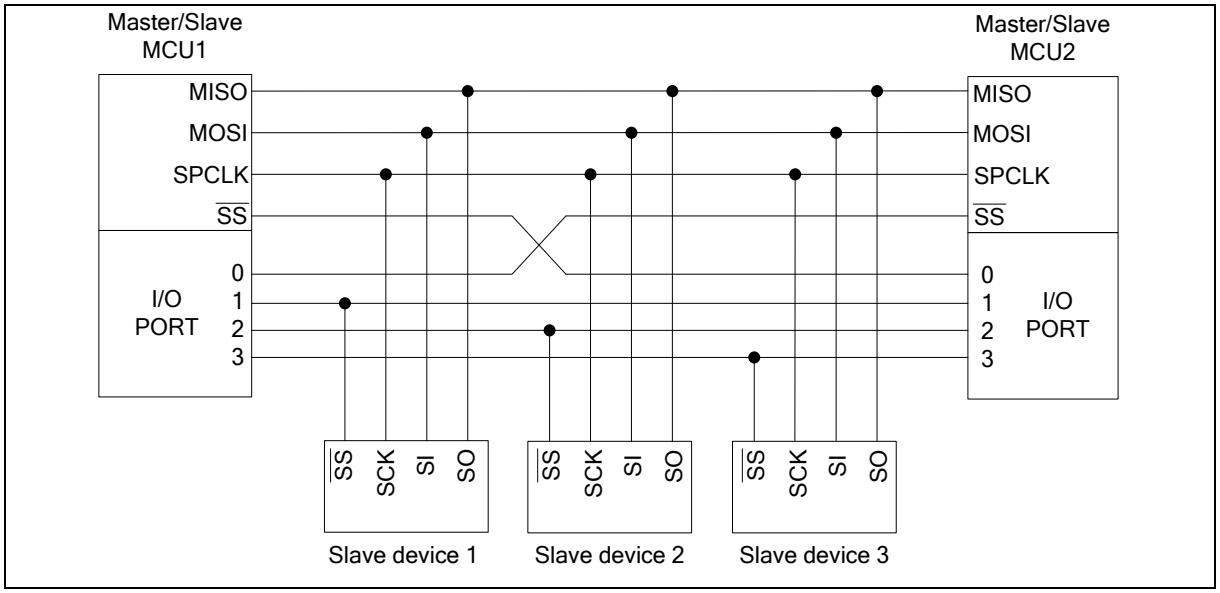


Figure 6.12-2 SPI Multi-Master, Multi-Slave Interconnection

Figure 6.12-2 shows a typical interconnection of SPI devices. The bus generally connects devices together through three signal wires, MOSI to MOSI, MISO to MISO, and SPCLK to SPCLK. The Master devices select the individual Slave devices by using four pins of a parallel port to control the four $\overline{SS}$ pins. MCU1 and MCU2 play either Master or Slave mode. The $\overline{SS}$ should be configured as Master Mode Fault detection to avoid multi-master conflict.

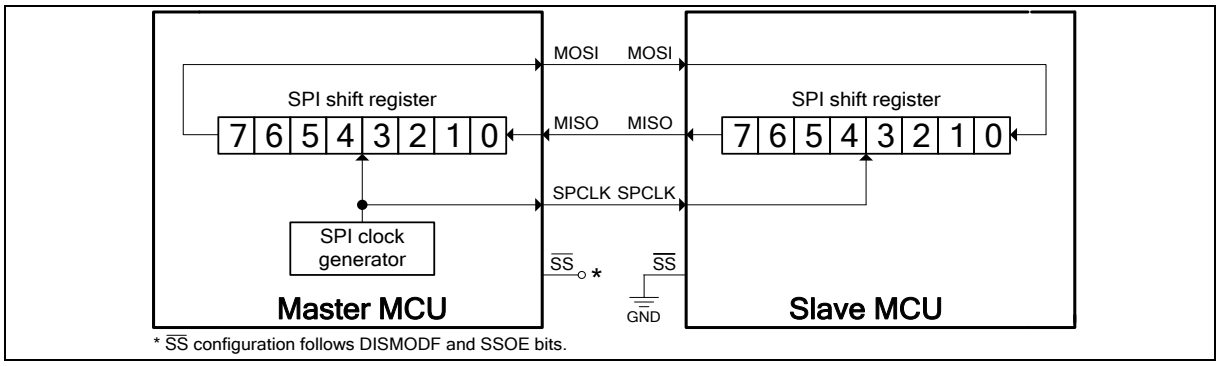


Figure 6.12-3 SPI Single-Master, Single-Slave Interconnection

Figure 6.12-3 shows the simplest SPI system interconnection, single-master and signal-slave. During a transfer, the Master shifts data out to the Slave via MOSI line. While simultaneously, the Master shifts data in from the Slave via MISO line. The two shift registers in the Master MCU and the Slave MCU can be considered as one 16-bit circular shift register. Therefore, while a transfer data pushed from Master into Slave, the data in Slave will also be pulled in Master device respectively. The transfer effectively exchanges the data, which was in the SPI shift registers of the two MCUs.

By default, SPI data is transferred MSB first. If the LSBFE (SPCR.5) is set, SPI data shifts LSB first. This bit does not affect the position of the MSB and LSB in the data register. Note that all the following description and figures are under the condition of LSBFE logic 0. MSB is transmitted and received first.

There are three SPI registers to support its operations, including SPI control register (SPCR), SPI status register (SPSR), and SPI data register (SPDR). These registers provide control, status, data storage functions, and clock rate selection. The following registers relate to SPI function.

6.13 12-Bit Analog-To-Digital Converter (ADC)

6.13.1 Overview

The CM1003 is embedded with a 12-bit SAR ADC. The ADC (analog-to-digital converter) allows conversion of an analog input signal to a 12-bit binary representation of that signal. The CM1003 is selected as 15-channel inputs in single end mode. The internal band-gap voltage also can be the internal ADC input. The analog input, multiplexed into one sample and hold circuit, charges a sample and hold capacitor. The output of the sample and hold capacitor is the input into the converter. The converter then generates a digital result of this analog level via successive approximation and stores the result in the result registers. The ADC controller also supports continuous conversion and storage result data into XRAM.

7 APPLICATION CIRCUIT

7.1 Power supply scheme

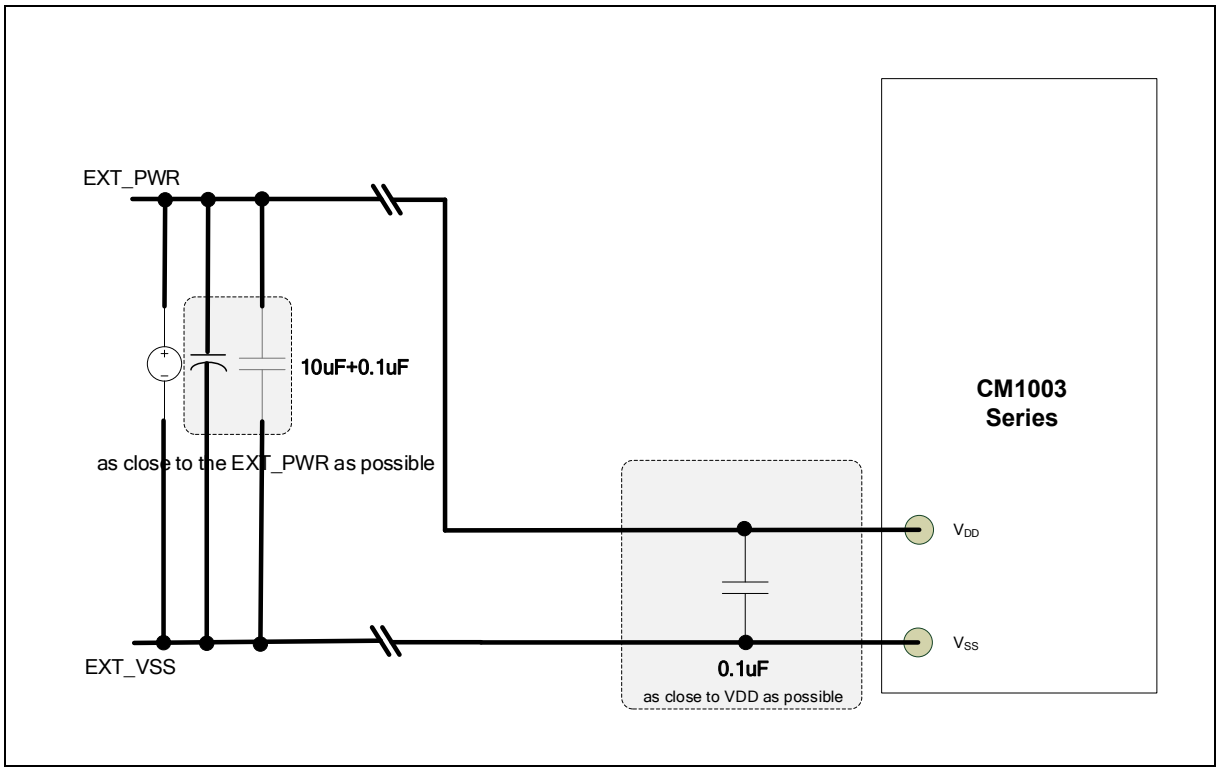
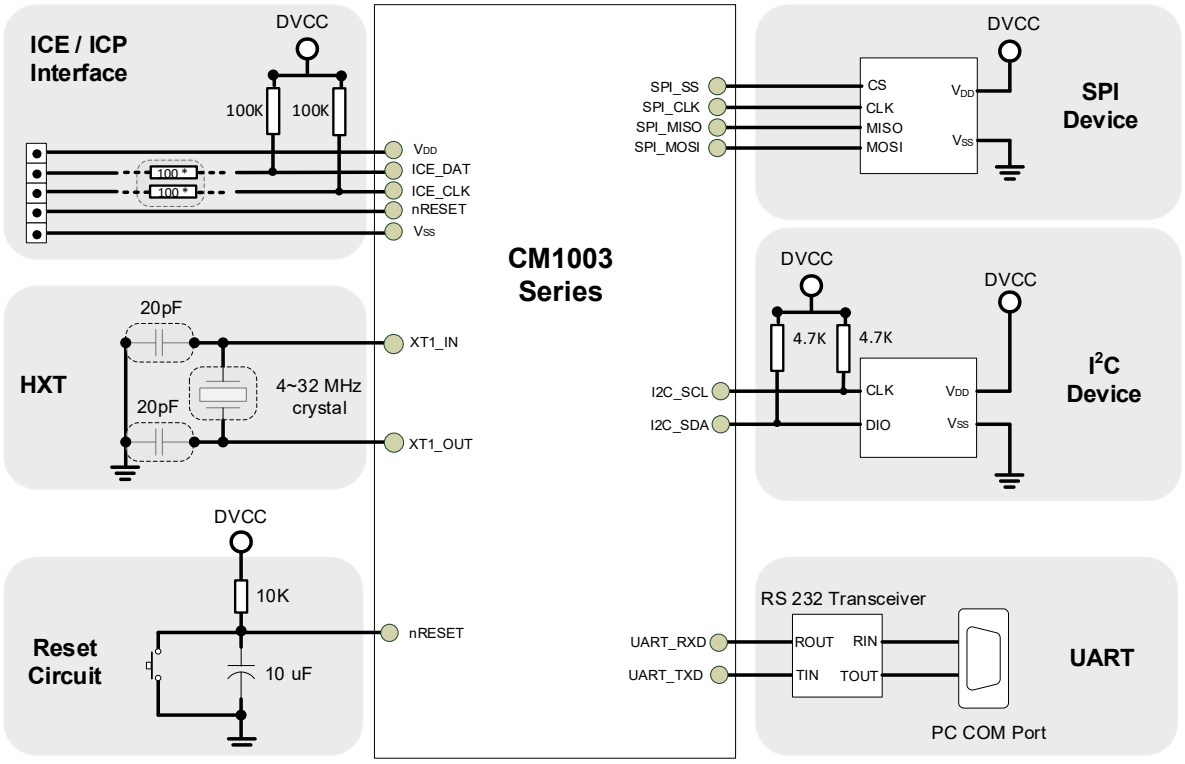


Figure 7.1-1 NuMicro® CM1003 Power supply circuit

7.2 Peripheral Application scheme



*ICE/ICP interface ICE_DAT/ICE_CLK pin 100ohm resister is selectable only for filter the disturb of noise on the circuit.

Note:

1. It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.
2. It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.
3. It is optional add 100ohm resistor series between ICE_DAT/ICE_CLK pin and writer pin to help filtering noise interference.
4. The HXT external capacitor value please reference Section 8.3.2.2Typical Crystal Application Circuits Capacitors Value

Figure 7.2-1 NuMicro® CM1003 Peripheral interface circuit

8 ELECTRICAL CHARACTERISTICS

Please refer to the relative Datasheet for detailed information about the CM1003 electrical characteristics.

8.1 General Operating Conditions

(V_{DD}-V_{SS} = 2.4V ~ 5.5V, T_A = 25°C, Fsys = 16 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
V_{DD}	Operation voltage	2.4	-	5.5	V	
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{BG}	Band-gap voltage[2]	1.15	1.2	1.30		T_A = 25°C
		1.14		1.33		T_A = -40°C to +105°C

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation.
2. All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.1-1 General Operating Conditions

8.2 DC Electrical Characteristics

8.2.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 2.4V ~ 5.5 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.
- $V_{DD} = AV_{DD}$
- When the peripherals clock base is the system clock Fsys.
- Program run “while (1);” in Flash Memory.

Symbol	Conditions	F_{HCLK}	Typ.		Max.			Unit
			T_A = 25 °C		T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
		V_{DD}	3.3 V	5.5 V	5.5 V			
I_{DD_RUN}	Normal run mode executed from Flash, all peripherals disable, HIRC or LIRC clock	24 MHz[1]	1.9	2.1	1.9	2.2	2.5	mA
		24 MHz[2]	1.7	1.8	1.8	1.8	2.0	
		16 MHz[3]	1.2	1.3	1.3	1.4	1.5	
		12 MHz[4]	1.3	1.4	1.4	1.5	1.6	
		6 MHz[4]	1.3	1.4	1.9	2.0	2.3	
		4 MHz[4]	1.5	1.6	1.6	1.8	2.0	
		1 MHz[4]	1	1.1	1	1.2	1.3	
		10 kHz[5]	0.20	0.24	0.21	0.25	0.34	
	Normal run mode executed from Flash, all peripherals enable, HIRC or LIRC clock.	24 MHz[1]	2.5	2.8	2.6	2.9	3.3	
		24 MHz[2]	2.3	2.5	2.5	2.6	2.7	
		16 MHz[3]	1.8	2.0	1.9	2.1	2.2	
		12 MHz[4]	1.7	1.9	1.9	2.0	2.1	
		6 MHz[4]	1.7	1.8	2.4	2.5	2.7	
		4 MHz[4]	1.8	2.0	2.1	2.2	2.4	
		1 MHz[4]	1.2	1.4	1.4	1.5	1.6	
		10 kHz[5]	0.41	0.55	0.54	0.57	0.66	

Note:

1. This value based on HXT enable, HIRC disable, LIRC enable.
2. This value based on HXT disable, HIRC enable reload 24MHz trim value, LIRC enable.
3. This value based on HXT disable, HIRC enable reload 16MHz trim value, LIRC enable.
4. This value based on HXT disable, HIRC enable and clock diveder enable, LIRC enable.
5. This value based on HIRC disable, LIRC enable.

6. All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.2-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ.		Max.			Unit
			T_A = 25 °C		T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
		V_{DD}	3.3 V	5.5 V	5.5 V			
I_{DD_IDLE}	Idle mode, executed from Flash, all peripherals disable	24 MHz[1]	1.2	1.3	1.2	1.4	1.7	mA
		24 MHz[2]	0.9	1.0	1.0	1.1	1.2	
		16 MHz[3]	0.7	0.8	0.7	0.9	1.0	
		12 MHz[4]	0.8	0.9	0.9	1.0	1.1	
		6 MHz[4]	0.8	0.9	0.8	0.9	1.0	
		4 MHz[4]	0.75	0.81	0.78	0.83	0.96	
		1 MHz[4]	0.74	0.79	0.76	0.81	0.92	
		10 kHz[5]	0.20	0.23	0.21	0.25	0.34	
	Idle mode, executed from Flash, all peripherals enable	24 MHz[1]	1.8	2.1	1.9	2.1	2.4	
		24 MHz[2]	1.6	1.7	1.7	1.8	1.9	
		16 MHz[3]	1.2	1.4	1.4	1.5	1.6	
		12 MHz[4]	1.3	1.4	1.4	1.5	1.6	
		6 MHz[4]	1.1	1.3	1.3	1.4	1.5	
		4 MHz[4]	1.1	1.2	1.2	1.3	1.4	
		1 MHz[4]	1	1.2	1.1	1.2	1.3	
		10 kHz[5]	0.40	0.55	0.53	0.57	0.65	

Note:

1. This value based on HXT enable, HIRC disable, LIRC enable.
2. This value based on HXT disable, HIRC enable reload 24MHz trim value, LIRC enable.
3. This value based on HXT disable, HIRC enable reload 16MHz trim value, LIRC enable.
4. This value based on HXT disable, HIRC enable and clock diveder enable, LIRC enable.
5. This value based on HIRC disable, LIRC enable.
6. All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.2-2 Current Consumption in Idle Mode

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
I_{DD_PD}	Power-down mode, all peripherals disable at 5.5V	9	7	8	20	μA
	Power-down mode, all peripherals disable at 3.3V	8				

Symbol	Test Conditions	Typ[1]	Max[2]			Unit
		T_A = 25 °C	T_A = -40 °C	T_A = 25 °C	T_A = 105 °C	
	Power-down mode, all peripherals disable at 2.4V	7				
	Power-down mode, LVR enable and other peripherals disable	8	9	10[3]	24	
	Power-down mode, LVR enable, WDT enable and other peripherals disable	8	9	11	25	
	Power-down mode, LVR enable BOD enable and other peripherals disable	160	210	250	310	

Note:

1. AV_{DD} = V_{DD} = 3.3V unless otherwise specified, LVR17 disabled, POR disabled and BOD disabled.
2. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
3. Based on characterization, tested in production.

Table 8.2-3 Chip Current Consumption in Power-down Mode

8.2.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- The system clock = 24 MHz.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	$I_{DD\ Base}$	I_{DD}[1]	Unit
ADC[2]	360		μA
PWM0	800		
PWM1	300		
PWM2	300		
PWM3	300		
SPI0	8		
UART0	7		
UART1	7		
I2C0	3		
SC0	28		
SC1	29		
SC2	28		
PIN Interrupt	1		
TIMER 0	40	4	
TIMER 1		5	
TIMER 2		5	
TIMER 3		8	
INT0	1		
INT1	1		
WDT	1		
WKT	1		
CAPTURE0	30	1	
CAPTURE1		1	
CAPTURE2		1	

Notes:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.

Table 8.2-4 Peripheral Current Consumption

8.2.3 Wakeup Time from Low-Power Modes

Symbol	Parameter		Typ	Max	Unit
t_{WU_IDLE}[1]	Wakeup from IDLE mode		5	6	cycles
t_{WU_NPD}[2][3]	Wakeup from Power-down mode	Fsys = HIRC @16MHz	-	40	µs
		Fsys = HIRC @ 24MHz		40	µs

Note:

1. Measured on a wakeup phase with a 16 MHz HIRC oscillator.
2. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
3. The wakeup times are measured from the wakeup event to the point in which the application code reads the first.

Table 8.2-5 Low-power Mode Wakeup Timings

8.2.4 I/O DC Characteristics

8.2.4.1 PIN Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IL}	Input low voltage (I/O with TTL input)	0	-	$0.3*V_{DD}$	V	
V_{IL1}	Input low voltage (I/O with Schmitt trigger input and Xin)	V_{SS}-0.3	-	$0.2V_{DD}$-0.1	V	
V_{IH}	Input high voltage (I/O with TTL input)	$0.2V_{DD}$+0.9	-	V_{DD}+0.3	V	
V_{IH1}	Input high voltage (I/O with Schmitt trigger input and Xin)	$0.7*V_{DD}$	-	V_{DD}	V	
V_{HY}[1]	Hysteresis voltage of schmitt input	-	$0.2*V_{DD}$	-	V	
I_{LK}[2]	Input leakage current	-1		1	µA	$V_{SS} < V_{IN} < V_{DD}$, Open-drain or input only mode
		-1		1		$V_{DD} < V_{IN} < 5.5$ V, Open-drain or input only mode

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. Leakage could be higher than the maximum value, if abnormal injection happens.
3. To sustain a voltage higher than V_{DD} +0.3 V, the internal pull-up resistors must be disabled. Leakage could be higher than the maximum value, if positive current is injected on adjacent pins

Table 8.2-6 I/O Input Characteristics

8.2.4.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[1] [2]	Source current for quasi-bidirectional mode and high level	-5	-8	-12	μA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-5	-8	-12	μA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-5	-8	-12	μA	V_{DD} = 2.4 V V_{IN} =(V_{DD}-0.4) V
		-45	-62	-87	μA	V_{DD} = 5.5 V V_{IN} = 2.4 V
	Source current for push-pull mode and high level	-7.1	-9	-13.5	mA	V_{DD} = 5.5 V V_{IN} =(V_{DD}-0.4) V
		-4.5	-6.2	-9.4	mA	V_{DD} = 3.3 V V_{IN} =(V_{DD}-0.4) V
		-3.5	-5.1	-7.8	mA	V_{DD} = 2.7 V V_{IN} =(V_{DD}-0.4) V
		-33	-39	-57	mA	V_{DD} = 5.5 V V_{IN} = 2.4 V
I_{SK}[1] [2]	Sink current for push-pull mode and low level	12.6	15.4	26.8	mA	V_{DD} = 5.5 V V_{IN} = 0.4 V
		7.8	10.5	17.7	mA	V_{DD} = 3.3 V V_{IN} = 0.4 V
		5.3	7.4	12.4	mA	V_{DD} = 2.4 V V_{IN} = 0.4 V
C_{IO}[1]	I/O pin capacitance	-	5	-	pF	

Notes:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.2-7 I/O Output Characteristics

8.2.4.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	0.3*V_{DD}	V	
V_{IHR}	Positive going threshold, nRESET	0.7*V_{DD}	-	-	V	
R_{RST}	Internal nRESET pull up resistor	45	50	60	KΩ	V_{DD} = 5.5 V
		45	50	65		V_{DD} = 2.4 V
t_{FR}	nRESET input response time	-	1.5	-	µs	Normal run and Idle mode
		24	-	40		Power-down mode

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.2-8 nRESET Input Characteristics

8.3 AC Electrical Characteristics

8.3.1 Internal High Speed RC Oscillator (HIRC)

8.3.1.1 16MHz RC Oscillator (HIRC)

The 16 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	16[1]	-	MHz	T_A = 25°C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25°C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C to +105°C, V_{DD} = 2.4 to 5.5V
		-4[4]		4[4]	%	T_A = -40°C to -20°C, V_{DD} = 2.4V to 5.5V
I_{HRC}[2]	Operating current	-	490	550	μA	
T_S[3]	Stable time	-	3	5	μs	T_A = -40°C to +105°C, V_{DD} = 2.4V to 5.5V

Note:

Default setting value for the product

Based on reload value.

Based on characterization, tested in production.

Guaranteed by characterization result, not tested in production.

Guaranteed by design.

Table 8.3-1 16 MHz Internal High Speed RC Oscillator(HIRC) Characteristics

8.3.1.2 24MHz RC Oscillator (HIRC)

The 24 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{HRC}	Oscillator frequnecy	-	24[1]	-	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1[3]	-	1[3]	%	T_A = 25 °C, V_{DD} = 3.3V
		-2[4]	-	2[4]	%	T_A = -20°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V
		-4[4]		4[4]	%	T_A = -40°C ~ -20 °C, V_{DD} = 2.4 ~ 5.5V
I_{HRC}[2]	Operating current	-	490	550	μA	
T_S[3]	Stable time	-	3	5	μs	T_A = -40°C ~ +105 °C, V_{DD} = 2.4 ~ 5.5V

Note:

1. Default setting value for the product

Based on reload value.

Based on characterization, tested in production.

Guaranteed by characterization result, not tested in production.

Guaranteed by design.

Table 8.3-2 24 MHz Internal High Speed RC Oscillator(HIRC) characteristics

8.3.2 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions[2]
V_{DD}	Operating voltage	205	-	5.5	V	
R_f	Internal feedback resister	-	200	-	kΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption[2]	-	350	950	μA	Gain = L0
		-	650	1650		Gain = L1
T_S	Stable time [3]	-	3075	-	μs	Gain = L0
		-	3420	-		Gain = L1
Du_{HXT}	Duty cycle	40	-	60	%	

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. L0 to L1 are defined by SFR XLTCON[6:0] HXSG. Based on the frequency selection of the Crystal, it is recommended to use L0 for frequencies between 4 MHz and 12 MHz, and L1 for frequencies between 12 MHz and 24 MHz. For ceramic resonator , use L0 for frequencies between 4 MHz and 24 MHz.
3. Based on SMD type crystals.

Table 8.3-3 External 4~24 MHz High Speed Crystal (HXT) Oscillator

8.3.2.2 Typical Crystal Application Circuits Capacitors Value

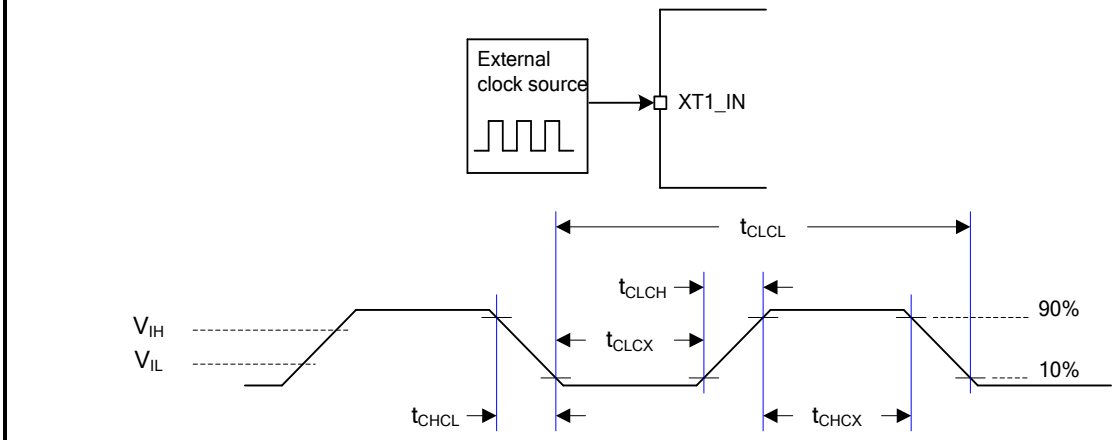
For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 25 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 25 pF	10 ~ 25 pF	without

8.3.3 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	4	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	ns	
t_{CLCX}	Clock low time	8	-	-	ns	
t_{CLCH}	Clock rise time	-	-	10	ns	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	ns	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Note:

1.All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.3-4 External 4~24 MHz High Speed Clock Input Signal

8.3.4 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	2.4	-	5.5	V	
F_{LRC}	Oscillator frequnecy	-	10	-	kHz	
	Frequency drift over temperarure and volatge	-10[2]	-	10[2]	%	T_A = 25 °C, V_{DD} = 5V
		-35	-	35	%	T_A=-40~105°C Without software calibration
I_{LRC}	Operating current	-	0.9	1	μA	V_{DD} = 3.3V
T_S	Stable time	-	500	-	μs	T_A=-40~105°C

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. Based on characterization and tested in production.

Table 8.3-5 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics

8.3.5 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[1].	Unit	Test Conditions[2]
$t_{f(IO)out}$	Normal mode [3] output high (90%) to low level (10%) falling time	5.6	8.4	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.5	5.2		C_L = 10 pF, V_{DD} >= 5.5 V
		8.6	13.3		C_L = 30 pF, V_{DD} >= 3.3 V
		5.3	8.1		C_L = 10 pF, V_{DD} >= 3.3 V
		12.3	19.0		C_L = 30 pF, V_{DD} >= 2.4 V
		7.6	11.8		C_L = 10 pF, V_{DD} >= 2.4 V
	High slew rate mode [4] output high (90%) to low level (10%) falling time	4.1	6.1	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.2	3.2		C_L = 10 pF, V_{DD} >= 5.5 V
		6.2	9.4		C_L = 30 pF, V_{DD} >= 3.3 V
		3.2	4.9		C_L = 10 pF, V_{DD} >= 3.3 V
		8.8	13.6		C_L = 30 pF, V_{DD} >= 2.4 V
		4.4	6.9		C_L = 10 pF, V_{DD} >= 2.4 V
$t_{r(IO)out}$	Normal mode [3] output low (10%) to high level (90%) rising time	6.1	8.7	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		3.6	5.3		C_L = 10 pF, V_{DD} >= 5.5 V
		9.0	13.6		C_L = 30 pF, V_{DD} >= 3.3 V
		5.5	8.5		C_L = 10 pF, V_{DD} >= 3.3 V
		12.6	19.3		C_L = 30 pF, V_{DD} >= 2.4 V
		7.8	12.3		C_L = 10 pF, V_{DD} >= 2.4 V
	High slew rate mode [4] output low (10%) to high level (90%) rising time	4.9	6.6	ns	C_L = 30 pF, V_{DD} >= 5.5 V
		2.4	3.3		C_L = 10 pF, V_{DD} >= 5.5 V
		7.0	10.1		C_L = 30 pF, V_{DD} >= 3.3 V
		3.5	5.1		C_L = 10 pF, V_{DD} >= 3.3 V
		9.5	14.1		C_L = 30 pF, V_{DD} >= 2.4 V
		4.7	7.1		C_L = 10 pF, V_{DD} >= 2.4 V
$f_{max(IO)out}$	Normal mode[3] I/O maximum frequency	16	16	MHz	C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V
	High slew rate[4] mode I/O maximum frequency	24	24		C_L = 30 pF, V_{DD} >= 2.4 V
					C_L = 10 pF, V_{DD} >= 2.4 V

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. PxSR.n bit value = 0, Normal output slew rate.
4. PxSR.n bit value = 1, high speed output slew rate.

Table 8.3-6 I/O AC Characteristics

8.4 Analog Characteristics

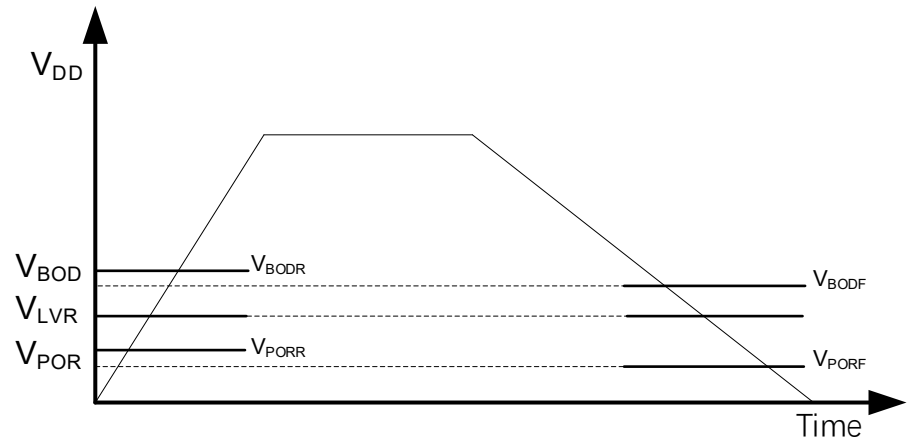
8.4.1 Reset and Power Control Block Characteristics

The parameters in the following table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}	POR operating current	10		20	μA	AV_{DD} = 5.5V
I_{LVR}	LVR operating current	0.5	-	1		AV_{DD} = 5.5V
I_{BOD}	BOD operating current	-	200	230		AV_{DD} = 5.5V
V_{PORR}	POR reset voltage (Power on rising threshold level)	1	1.15	1.3	V	-
V_{PORF}	POR reset voltage (Power off falling threshold level)	0.9	1.05	1.15		-
V_{LVR}	LVR reset threshold voltage	1.7	2.0	2.4		-
V_{BODR}	BOD brown-out detect voltage (Power on rising threshold level)	4.2	4.5	4.8		BOV[1:0] = [0,0]
		3.6	3.8	4.0		BOV[1:0] = [0,1]
		2.6	2.8	3.0		BOV[1:0] = [1,0]
		2.1	2.3	2.5		BOV[1:0] = [1,1]
V_{BODF}	BOD brown-out detect voltage (Power off falling threshold level)	4.1	4.4	4.7		BOV[1:0] = [0,0]
		3.5	3.7	3.9		BOV[1:0] = [0,1]
		2.5	2.7	2.9		BOV[1:0] = [1,0]
		2.0	2.2	2.4		BOV[1:0] = [1,1]
T_{LVR_SU}	LVR startup time	48	61	80	μs	-
T_{LVR_RE}	LVR respond time	-	-	30		Fsys = HIRC@16MHz
		-	-	30		Fsys = LIRC
T_{BOD_SU}	BOD startup time	180	-	320		Fsys = HIRC@16MHz
T_{BOD_RE}	BOD respond time	2.5	-	5		Fsys = HIRC@16MHz
R_{VDDR}	V_{DD} rise time rate	160	-	-	μS/V	POR Enabled
R_{VDDF}	V_{DD} fall time rate	160	-	-		POR Enabled, BOD Enabled, LVR Enabled

Note:
1.All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.4-1 Reset and Power Control Unit



Note: V_{POR} detect internal LDO voltage.

Figure 8.4-1 Power Ramp Up/Down Condition

BODFLT (BODCON1.1)	BOD Operation Mode	System Clock Source	Minimum Brown-out Detect Pulse Width
0	Normal mode (LPBOD[1:0] = [0,0])	Any clock source	Typ. 1μs
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	16 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	64 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	256 ($1/F_{LIRC}$)
1	Normal mode (LPBOD[1:0] = [0,0])	HIRC/ECLK	Normal operation: 32 ($1/F_{SYS}$) Idle mode: 32 ($1/F_{SYS}$) Power-down mode: 2 ($1/F_{LIRC}$)
		LIRC	2 ($1/F_{LIRC}$)
	Low power mode 1 (LPBOD[1:0] = [0,1])	Any clock source	18 ($1/F_{LIRC}$)
	Low power mode 2 (LPBOD[1:0] = [1,0])	Any clock source	66 ($1/F_{LIRC}$)
	Low power mode 3 (LPBOD[1:0] = [1,1])	Any clock source	258 ($1/F_{LIRC}$)

Table 8.4-2 Minimum Brown-out Detect Pulse Width

8.4.2 12-bit SAR Analog To Digital Converter (ADC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog Operating Voltage	2.4	-	5.5	V	$AV_{DD} = V_{DD}$
V_{REF}	Reference Voltage	2.4	-	AV_{DD}	V	$V_{REF} = AV_{DD}$
V_{IN}	ADC Channel Input Voltage	0	-	V_{REF}	V	
I_{ADC}[1]	Operating current (AV_{DD} + V_{REF} current)	-	-	418	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 5.5 V F_{ADCCOV} = 500 kHz
N_R	Resolution	12			Bit	
T_{ADCEC}	Encoding Time[2]	1.6			μs	This value is fixed by ADC module
F_{ADCLK}	ADC Sampling Clock Frequency	F_{SYS}/8		F_{SYS}		
T_{ADCSMP}	ADC Sampling Time[2]	0.4	-	17	μs	F_{SYS} = 16MHz
		0.417	-	11.3	μs	F_{SYS} = 24MHz
F_{ADCCOV}	Conversion Rate $F_{ADCCOV} = 1/T_{ADCCOV}$	53.7	-	500	kHz	F_{SYS} = 16MHz
		77.6	-	495	kHz	F_{SYS} = 24MHz
T_{ADCCOV}	Conversion Time[2] $T_{ADCCOV} = T_{ADCSMP} + T_{ADCEC}$	2	-	18.6	μs	F_{SYS} = 16MHz
		2.017	-	12.9	μs	F_{SYS} = 24MHz
T_{EN}	Enable To Ready Time	20	-	-	μs	
INL[1]	Integral Non-Linearity Error	-1	-	+3	LSB	$V_{REF} = AV_{DD} = V_{DD}$
DNL[1]	Differential Non-Linearity Error	-2	-	+4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_G[1]	Gain Error	-3.5	-	+0.4	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_{OT}[1]	Offset Error	-2	-	+2.8	LSB	$V_{REF} = AV_{DD} = V_{DD}$
E_A[1]	Absolute Error	-7	-	+7	LSB	$V_{REF} = AV_{DD} = V_{DD}$
R_S	Input Channel Equivalent Resistance	-	0.5	2.5	kΩ	
C_{IN}	Input Equivalent Capacitance	-	2.5	-	pF	
R_{IN}[1]	Internal Switch Resistance	-	0.5	-	kΩ	
R_{EX}[1]	External input impedance	-	-	33	kΩ	

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. ADC conversion time $T_{ADCCOV} = T_{ADCSMP} + T_{ADCEC}$. Encoding time is fixed, the fastest conversion rate is limited to 500k, so the sampling time has a minimum time constraint and must be greater than 400 μs.

   ADC Sampling Time $T_{ADCSMP} = \frac{4*ADCAQT+6}{F_{ADCCLK}}$, where ADCAQT is defined in ADCCON2[3:1] 3bit value from 0 ~ 7

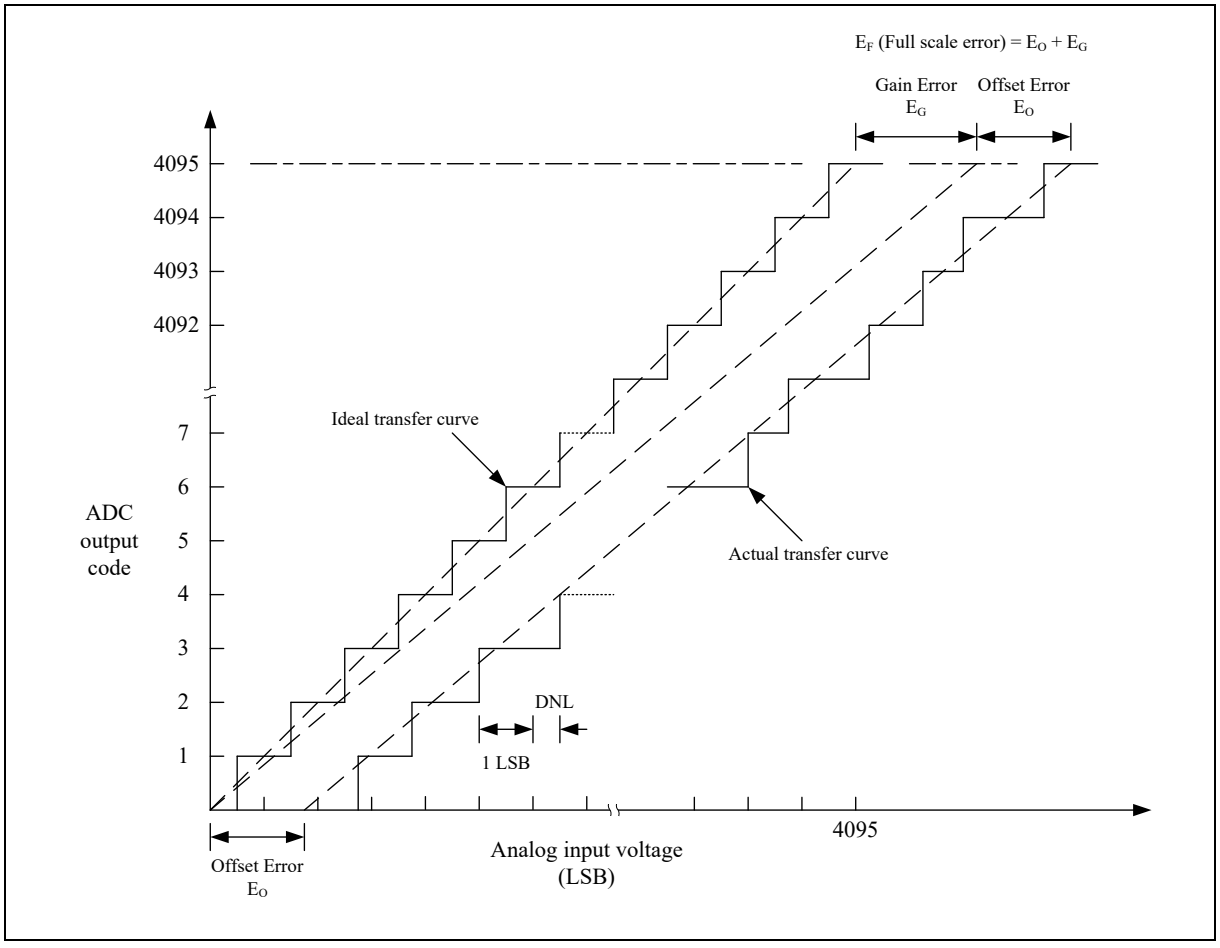
   and $F_{ADCCLK} = \frac{F_{SYS}}{ADCDIV}$, where ADCDIV is defined in ADCCON1[5:4] .

   When F_{SYS} = 16MHz, ADC Sampling Time Minimum value is $\frac{6}{16MHz}$ (ADCAQT = 0, ADCDIV = 0), ADC Sampling Time Maximum value is $\frac{4*7+6}{16MHz/8}$ (ADCAQT = 7, ADCDIV = 8) .

   When F_{SYS} = 24MHz, Due to limitations in sampling timing, we recommend setting ADCAQT to at least 1. ADC Sampling Time Minimum value is $\frac{4*1+6}{24MHz}$ (ADCAQT = 1, ADCDIV = 0), ADC Sampling Time Maximum value is $\frac{4*7+6}{24MHz/8}$ (ADCAQT = 7, ADCDIV = 8).
3. R_{EX} maximum formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (TSMP). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{F_{ADCCOV} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$

Table 8.4-3 ADC Characteristics



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

Figure 8.4-2 ADC Transfer Curve Characteristic

8.5 Communications Characteristics

8.5.1 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	$F_{SYS}/2$	MHz	2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			ns	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			ns	
t_{DS}	Data input setup time	2	-	-	ns	
t_{DH}	Data input hold time	$1/F_{SYS}$	-	-	ns	
t_V	Data output valid time	-	-	5	ns	Matser mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF
				$1/F_{SYS}$	ns	Slave mode 2.4 V ≤ V_{DD} ≤ 5.5 V, C_L = 30 pF

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.

Table 8.5-1 SPI Master Mode Characteristics

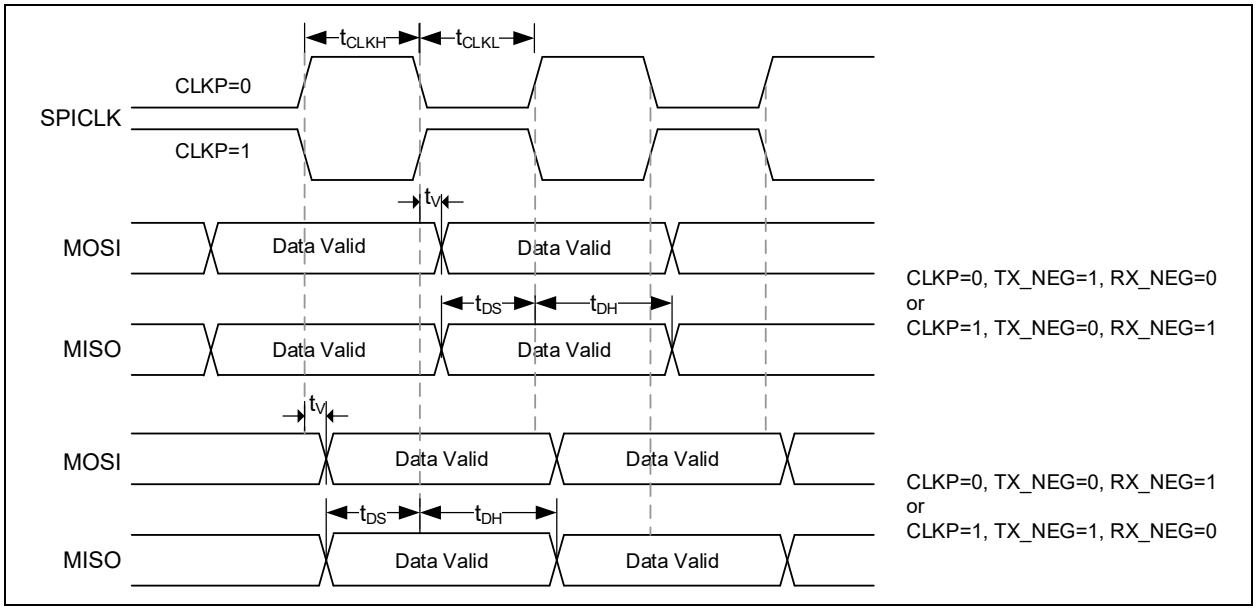


Figure 8.5-1 SPI Master Mode Timing Diagram

8.5.2 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min	Max	Min	Max	
t_{LOW}	SCL low period	4.7	-	1.3	-	μS
t_{HIGH}	SCL high period	4	-	0.6	-	μS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	0.6	-	μS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	μS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	μS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	μS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	μS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

Table 8.5-2 I²C Characteristics

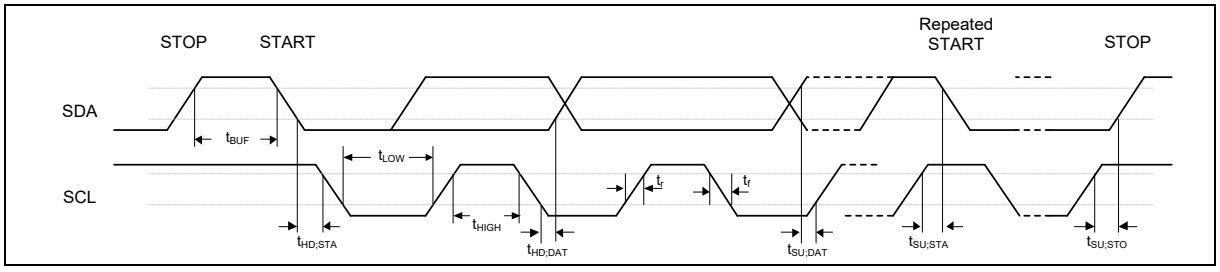


Figure 8.5-2 I²C Timing Diagram

8.6 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{ERASE}	Page erase time	-	5	-	ms	T_A = 25℃
T_{PROG}	Program time	-	20	-	μs	
I_{DD1}	Read current	-	4	-	mA	
I_{DD2}	Program current	-	2	-	mA	
I_{DD3}	Erase current	-	2	-	mA	
N_{ENDUR}	Endurance	100,000	-		cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	50	-	-	year	100 kcycle[2] T_A = 55℃
		25	-	-	year	100 kcycle[2] T_A = 85℃
		10	-	-	year	100 kcycle[2] T_A = 105℃

Note:

1. All data except as otherwise noted is guaranteed by characterization results, not tested in production.
2. Number of program/erase cycles.

Table 8.6-1 Flash Memory Characteristics

8.7 Absolute Maximum Ratings

Volrage Stesses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.7.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	6.5	V
ΔV_{DD}	Variations between different power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input voltage on I/O	V_{SS}-0.3	5.5	V

Note:

1. All main power (V_{DD}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.

Table 8.7-1 Voltage Characteristics

8.7.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
ΣI_{SS}	Maximum current out of V_{SS}	-	200	
I_{IO}	Maximum current sunk by a I/O Pin	-	22	
	Maximum current sourced by a I/O Pin	-	10	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by V_{IN}>A_{VDD} and a negative injection is caused by V_{IN}<V_{SS}. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.7-2 Current Characteristics

8.7.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (°C)
- θ_{JA} = thermal resistance junction-ambient (°C/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	°C
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 33-pin QFN(4x4 mm)		28	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.7-3 Thermal Characteristics

8.7.4 EMC Characteristics

8.7.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.7.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.7.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-7000	-	+7000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-1000	-	+1000	
LU[*3]	Pin current for latch-up[3]	-200	-	+200	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Note:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.7-4 EMC Characteristics

8.7.5 Soldering Profile

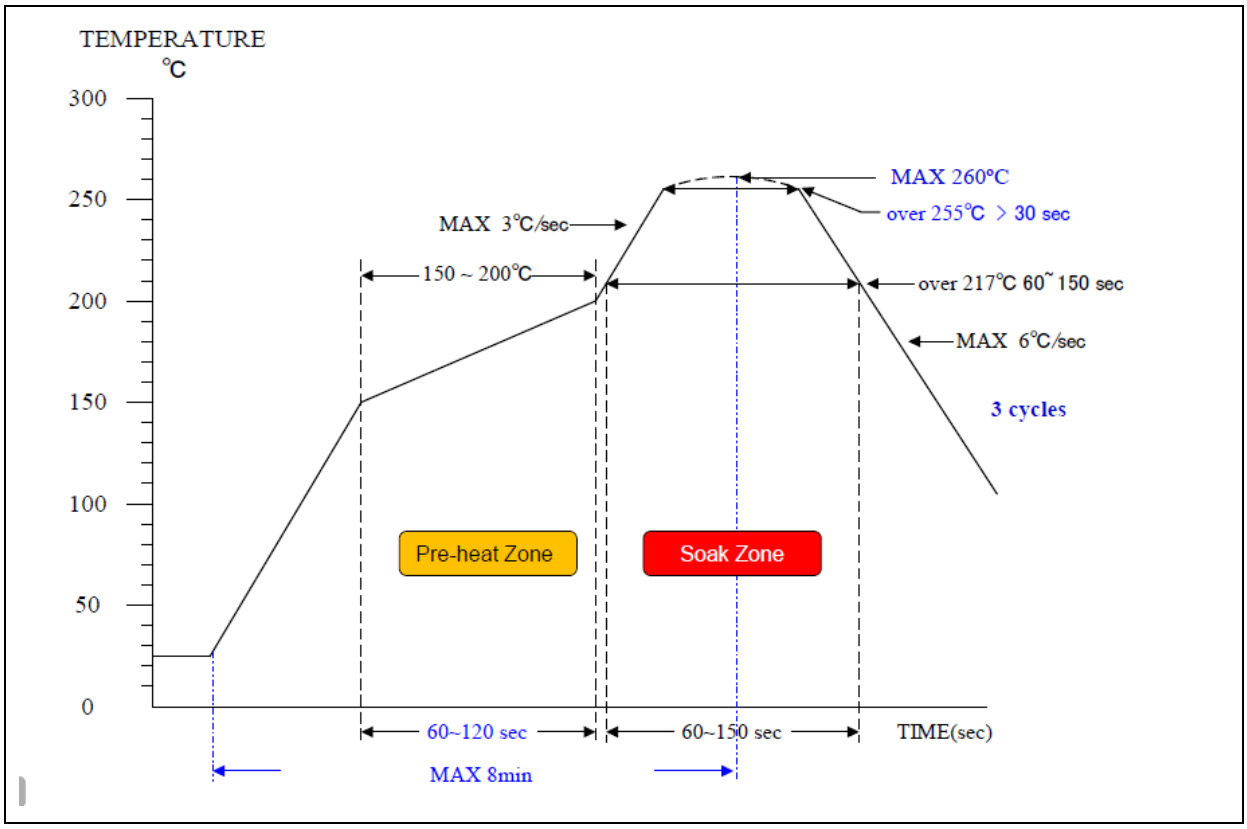


Figure 8.7-1 Soldering profile from J-STD-020C

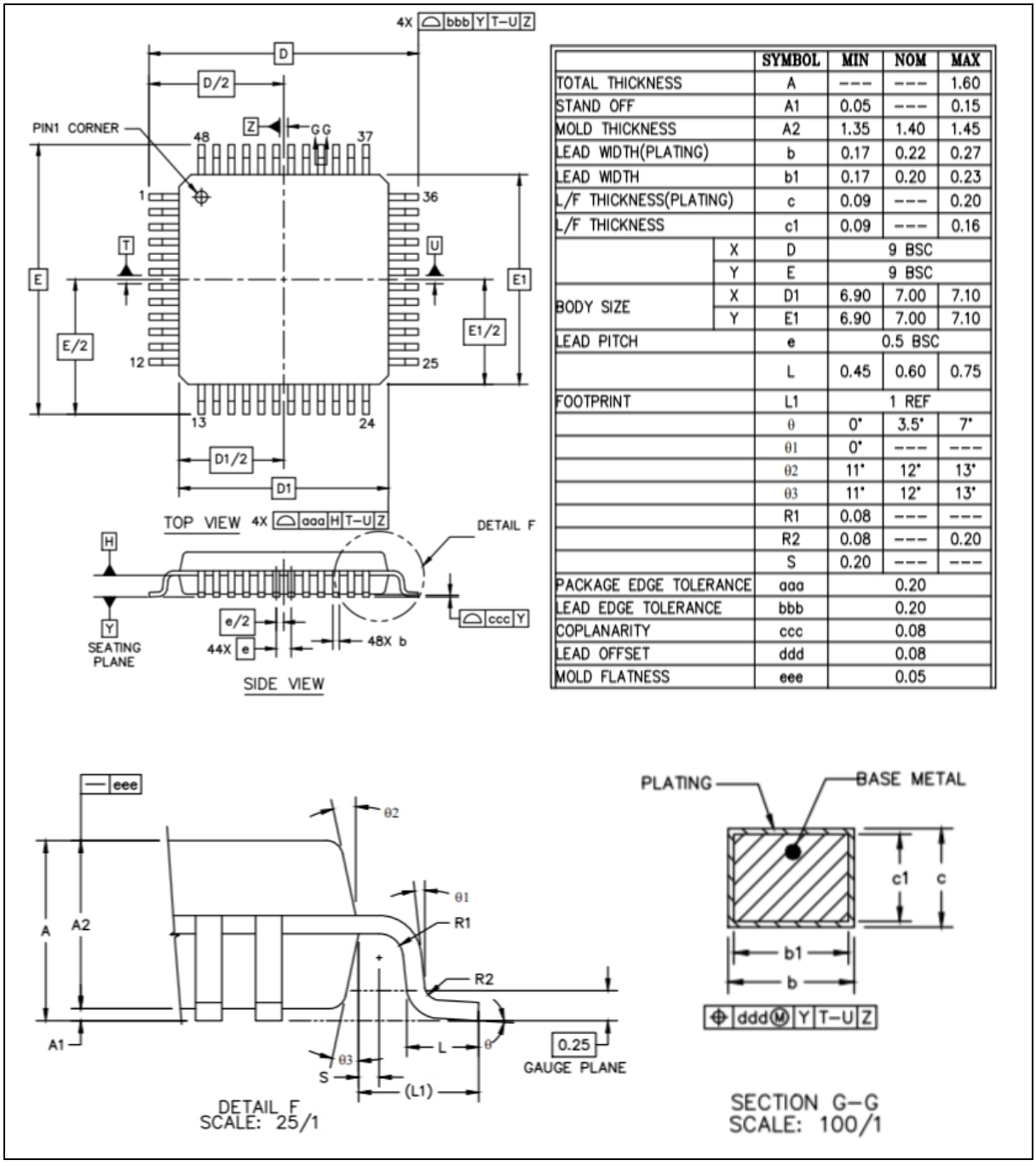
Porfile Feature	Pb Free Package
Average ramp-up rate (217°C to peak)	3°C/sec. max
Preheat temperature 150°C ~200°C	60 sec. to 120 sec.
Temperature maintained above 217°C	60 sec. to 150 sec.
Time with 5°C of actual peak temperature	> 30 sec.
Peak temperature range	260°C
Ramp-down rate	6°C/sec max.
Time 25°C to peak temperature	8 min. max
Note: 1.Determined according to J-STD-020C	

Table 8.7-5 Soldering Profile

9 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

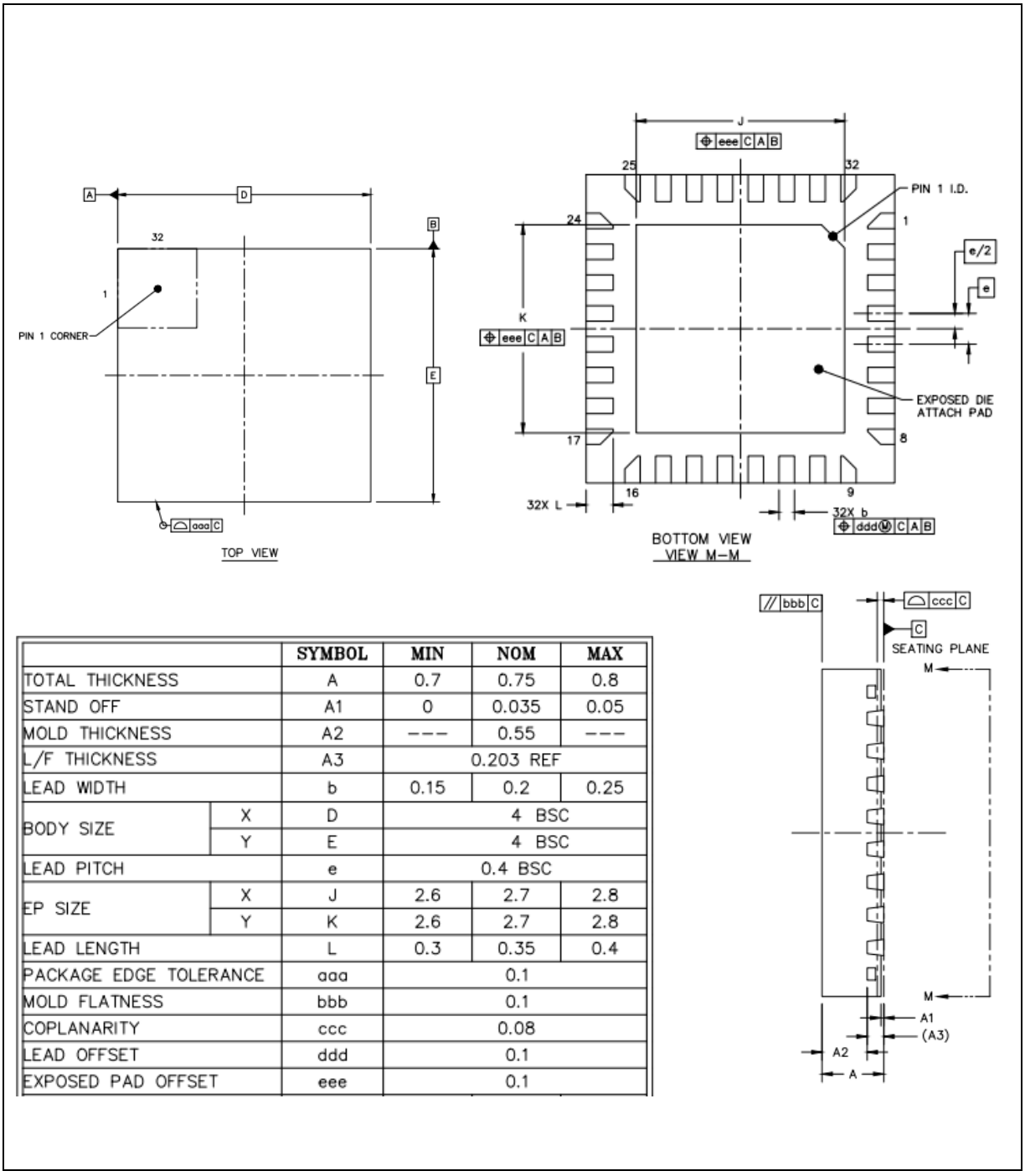
9.1 LQFP48-pin (7.0 x 7.0 x 1.4 mm^3)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.60
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.40	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.20	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.20
L/F THICKNESS		c1	0.09	---	0.16
	X	D	9 BSC		
	Y	E	9 BSC		
BODY SIZE	X	D1	6.90	7.00	7.10
	Y	E1	6.90	7.00	7.10
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.60	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.20
		S	0.20	---	---
PACKAGE EDGE TOLERANCE		aaa	0.20		
LEAD EDGE TOLERANCE		bbb	0.20		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

Figure 9.1-1 LQFP48 Package Dimension

9.2 QFN 33-pin (4.0 x 4.0 x 0.8 mm³)



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.6	2.7	2.8
	Y	K	2.6	2.7	2.8
LEAD LENGTH		L	0.3	0.35	0.4
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 9.2-1 QFN-33 Package Dimension

10 ABBREVIATIONS

10.1 Abbreviations List

Acronym	Description
ADC	Analog-to-Digital Converter
BOD	Brown-out Detection
GPIO	General-Purpose Input/Output
Fsys	Frequency of system clock
HIRC	12 MHz Internal High Speed RC Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIRC	10 kHz internal low speed RC oscillator (LIRC)
LVR	Low Voltage $eset
PDMA	Peripheral Direct Memory Access
POR	Power On Reset
PWM	Pulse Width Modulation
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
WKT	Wakeup Timer
WDT	Watchdog Timer

Table 10.1-1 List of Abbreviations

11 REVISION HISTORY

Date	Revision	Section	Description
2025-08-06	1.00		Initial version.
2025-10-11	1.01	Section 2	Modify the clock description in the section 2FEATURES
		Section 3.2	Modify 3.2 CM1003 Series Naming Rule
2026-01-19	1.02	Section 4.2.2	Modify CM1003 Series Pin Functional Description
		Section 1, 3.1, 3.3, 4.1,4.2, 6.10.1, 8.7.3, 9	Remove CM1003DJ8AE & LQFP32
2026-06-17	1.03	Section 3.3	Corrected the SRAM size of CM1003DL8AE.

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