Arm® Cortex®-M
32-bit Microcontroller

KM1M4BF22/23/24 Series

Datasheet

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1. Overview

1.1 Overview

This LSI is a 32-bit microcontroller with internal Flash memory. It is intended for development of the C programming language with object-oriented program and is easy to use. It has fast feedback processing required for control of motor.

This LSI adopts the Arm Cortex-M4F to the 32-bit microcontroller part and are equipped with internal memory to instruction / data, DMA controller, clock generator, bus controller, interrupt controller, standard peripheral circuits (timer and serial interface and so on), PWM control circuit specialized for motor control, and high accuracy / high speed analog circuit.

As system safety design, this LSI has the various safety mechanisms (Memory-ECC, clock error detection, power supply voltage detection, window watchdog timer, etc.).

1.2 Product Summary

The LSI shown in Table Table 1.2-1 is described in this manual.

Table 1.2-1 Product Summary

LSI series	LSI product name	Pins	ROM [KB]		RAM [KB]	VGA	Package
			Instruction	Data	Data		
KM1M4BF2 series	KM1M4BF22K	100	264	32	48	○	14 mm x 14 mm 0.5 mm pitch
	KM1M4BF23K	80	264	32	48	○	12 mm x 12 mm 0.5 mm pitch
	KM1M4BF24K	64	264	32	48	○	10 mm x 10 mm 0,5 mm pitch

Hint:

In this manual, the product names are classified as follows.

KM1M4BF2yK (y = 2,3,4)

1.2.1 Function Summary

Table 1.2-2 shows the functions of each product.

Table 1.2-2 The List of Function

Function		100 pins	80 pins	64 pins
CPU		Arm Cortex-M4F		
General purpose pin		86	66	52
Operation mode	Active mode	NORMAL		
	Standby mode	SLEEP, DEEPSLEEP		
Debugger I/F	Interface	SWD (1-wire/2-wire)		
DMA	CH number	8		
Interrupt	External interrupt	19	16	15
Timer	16-bit timer (Timer 0x)	8		
	16-bit timer (Timer 1x)	8		
	Power control PWM	8		
Noise filter	Target pin	External interrupt, Timer input		
Communication I/F	Clock synchronous/ SPI/UART/IIC	6		
12-bit A/D	AD0 CH number	8	8	8
	AD1 CH number	7	7	4
	AD2 CH number	8	5	4
	Total CH number	23	20	12
Programmable gain amplifier / Op-Amp	Module number/CH number	4 / 4		
Comparator	Module number/CH number	4 / 4		
8-bit D/A	Module number	8		
10-bit D/A	CH number	2		
Safety function	Flash memory	ECC, Data protection		
	RAM	ECC		
	Access area	MPU (Area management, Protection), Register protect (Protection)		
	System	Window watchdog timer		
	Clock	Clock monitoring (External oscillation, PLL error detection)		
	Communication	CRC caluculation function		
	A/D converter	A/D converter error detection		
	Power supply voltage	POR, Power supply voltage detection		
	Reset	Detection of reset factor immediately before by reset factor register		

1.3 Features

The features of this LSI are described.

Functions	Features
CPU	- Arm Cortex-M4F Equipped with FPU: Single precision floating point unit, IEEE754 compliant Equipped with MPU: Memory protect unit, 8 area can be set
Memory	- ROM access I-FLASH: 160 MHz 2 wait access(Min), selectable from 1 to 8 D-FLASH: 160 MHz 6 wait access(Min), selectable from 1 to 8 - RAM access 160 MHz 0 wait access - Swap Function I-Flash: Supports swap function of Boot area and Program area
Clock	- HXOCLK (External oscillation) frequency: 4 to 20 MHz - HRCCLK0 (Internal high-speed oscillation) frequency : 5 MHz - HRCCLK1 ((Internal high-speed oscillation) frequency : 40 MHz - PLLCLK PLL Input: HXOCLK and HRCCLK PLL Input frequency: 4 MHz to 20 MHz PLL Output frequency: 120 MHz to 240 MHz - BASECLK Selectable from HRCCLK0/HRCCLK1/HXOCLK/PLLCLK Start with HRCCLK0 when reset is released Switchable to HRCCLK1 when a clock error is detected - CPUCLK 1 to 8 dividing of BASECLK - IOCLK 2 to 16 dividing of CPUCLK Clock operation/stop can be selected for each peripheral module
Reset	- Hardware reset Power-On Reset - System Reset Reset by external pin(NRST) Reset by register setting Reset by error detection(WDT overflow, Clock error detection) - CPU Generation Reset Reset by writing to AIRCR - Reset factor can be monitored
Low power consumption	- SLEEP mode: Stop CPU clock only - DEEP SLEEP mode: Stop clocks including BASECLK
Interrupt	- Interrupt level: 16 levels - External interrupt: High/Low level, Rising/Falling/Both edge
DMA	- Transfer mode: Single word transfer mode, Burst transfer mode - Transfer unit: 8 bits/16 bits/32 bits - Maximum transfer count: 65535 words - Transfer factor: External interrupt, Peripheral module factor - Register reload count: Maximum 65535 times - Interrupt: DMA completion, reload count completion, bus error, transfer request overflow, invalid DMA transfer request
Noise filter	- Sampling type noise filter is inserted to external interrupt and timer input. - Select sampling clock

Functions	Features
16-bit timer (TM0x)	- Interval timer count, Event count, Up-down pulse count, Phase difference pulse count - Timer Output, PWM, 1-shot Output - Input capture by external input - Timer count start by start trigger - A/D conversion start trigger Output - 32-bit cascade connection - Output protection: H/L/Hi-z Output can be selected - Timer interrupt Output control
16-bit timer (TM1x)	- Interval timer count, Event count, Up-down pulse count, Phase difference pulse count - Timer Output, PWM/complement Output(wave mode: saw-tooth waves), 1-shot Output, Chopping waveform Output - Input capture by external input - Timer count start by start trigger - A/D conversion start trigger Output - 32-bit cascade connection - Output protection: H/L/Hi-z Output can be selected, reading edge blanking can be set - Timer interrupt Output control - Task overflow detection function - PWM Output: Dead time insert, Output shift, Duty cut, Period cut
Power control PWM (GPWMx)	- Complementary PWM Output (Wave mode: Triangular and saw-tooth waves) - Dead time insert, Output shift, H/L level Output can be set - Synchronous A/D conversion trigger - Interrupt Output control - Output protection: H/L/Hi-z Output can be select - Duty cut, period cut - Double buffer update
Synchronous SIF/SPI	- 2-wire/3-wire/4-wire - Transfer bits(2 bits to 8 bits) - MSB/LSB transfer - Clock polarity selection - Continuous communication - Output level after the final bit transmission(H/L/final data) - Maximum transfer rate: 10 Mbps (at master) / 5 Mbps (at slave)
UART	- 1-wire/2-wire - Character bits(5-bits to 8-bits) - Stop bits(1-bit/2-bit) - Parity bit: Enabled/Disabled, Parity bit type: 0/1/Even parity/Odd parity - MSB/LSB transfer - Maximum transfer rate: 3.3 Mbps - Built in Automatic Baud Rate adjustment function
IIC	- Master/Slave communication - Start condition selection: Enable/Disable - MSB/LSB transfer selection - Transfer format: 7-bit address format, 10-bit address format - Maximum transfer rate: Standard Mode: 100 kbps, Fast Mode: 400 kbps
12-bit A/D	- External Interrupt, TM0x, TM1x, GPWMx etc can be started synchronously - Conversion error detection - Conversion state Output - Start trigger reduction function - Individual Sample/Hold Circuit (SHC) selectable only for ADC0
VGA / OPA	- VGA mode and Op-Amp mode selectable -When used as VGA mode Gain selection(2, 3, 4, 5, 6, 8, 10, 20 times) Set Output reference voltage by 8-bit DAC

Functions	Features
Comparator	- Hysteresis ON/OFF - Set reference voltage by 8-bit DAC - Sampling type noise filter is inserted to comparator Output
8-bit D/A	- VGA Output reference voltage can be generated - Comparator reference voltage can be generated
10-bit D/A	- Output the set DC voltage
Multi feedback assist	- Set the start timing of TM1x, and GPWMx individually - Detect/Automatically avoid the competition of TM1x and GPWMx and AD conversion start - Mask(Blanking) the external interrupt detection, comparator of TM1x and GPWMx Output
CRC caluculation	- CRC-32/MPEG2, CRC-16-CCITT, CRC-16-IBM, CRC-8-ATM symbol can be generated
Safety function	- ECC function Check area: I-FLASH, D-FLASH, RAM 2 bit random error detection - Flash Erase/Program protect function - Function to protect write access to main register - Clock monitor function - Window watchdog timer(internal oscillation count) - Power supply voltage detection - ADC fault diagnosis function which is used for internal power supply

1.4 Pins

The specifications of pins in this LSI are described as follows.

- Pin configuration
- Pin function

1.4.1 Pin Configuration

Figure 1.4-1 shows the pin configuration of 100 pins.

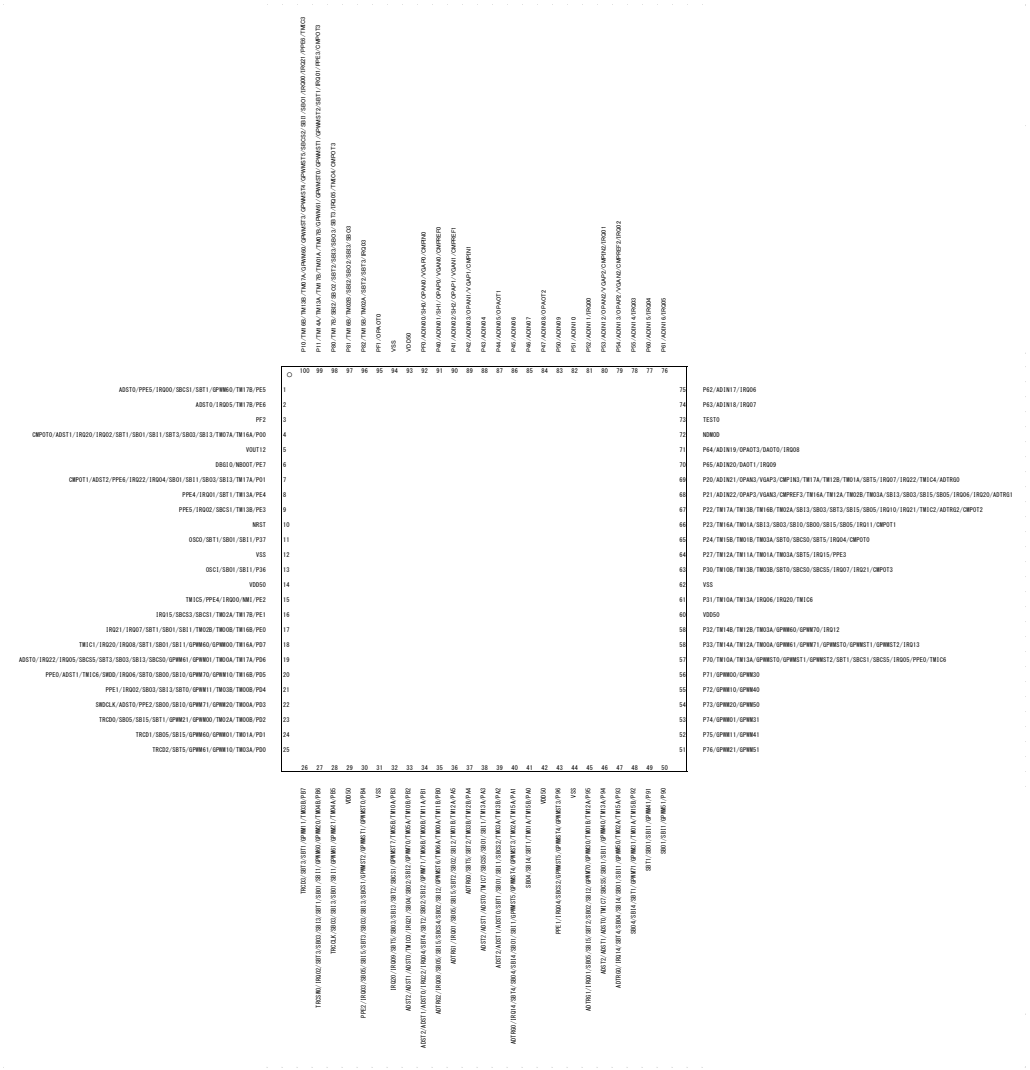


Figure 1.4-1 Pin Configuration Figure of 100 pins

Figure 1.4-2 shows the pin configuration of 80 pins.

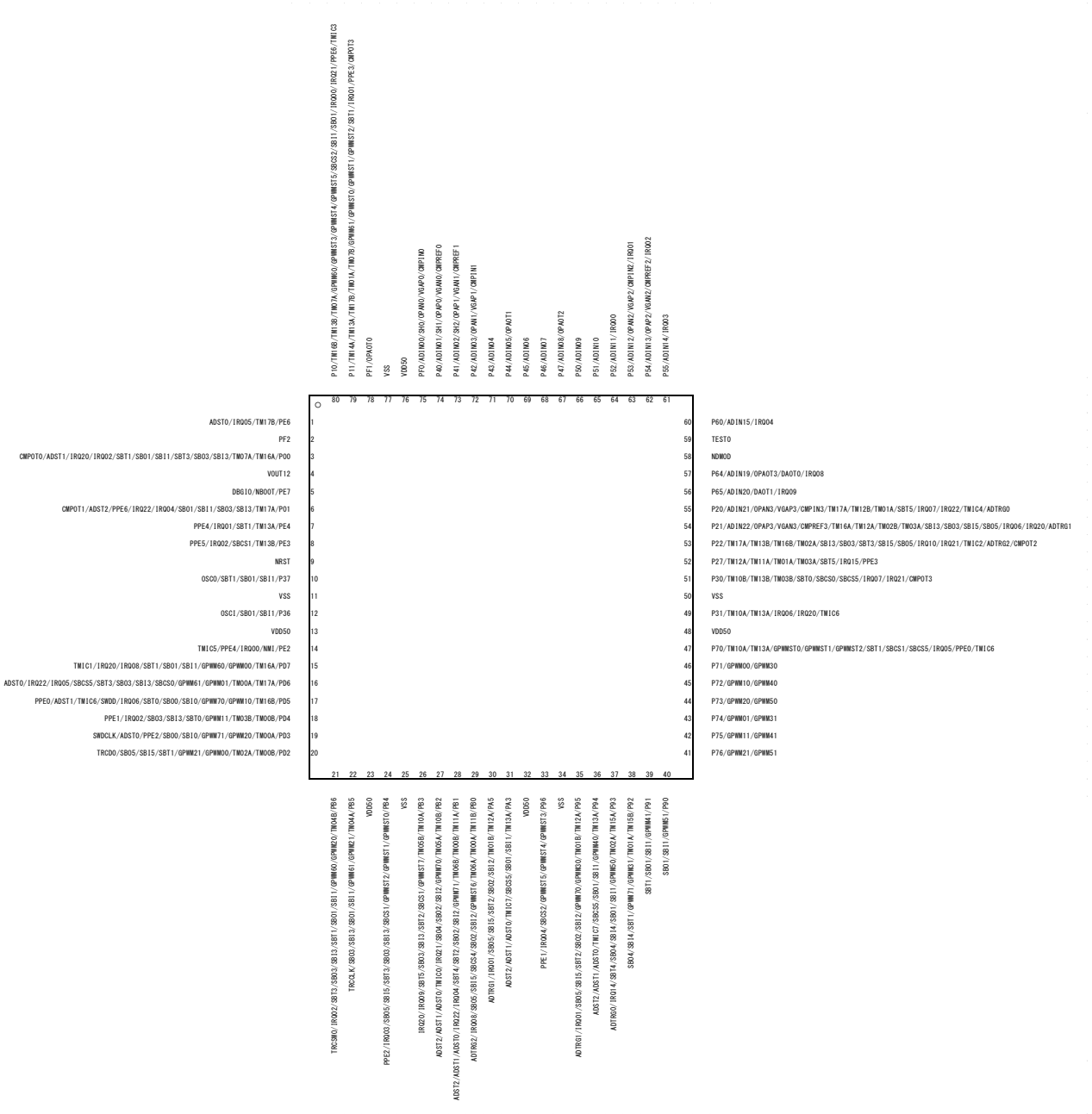


Figure 1.4-2 Pin Configuration Figure of 80 pins

Figure 1.4-3 shows the pin configuration of 64 pins.

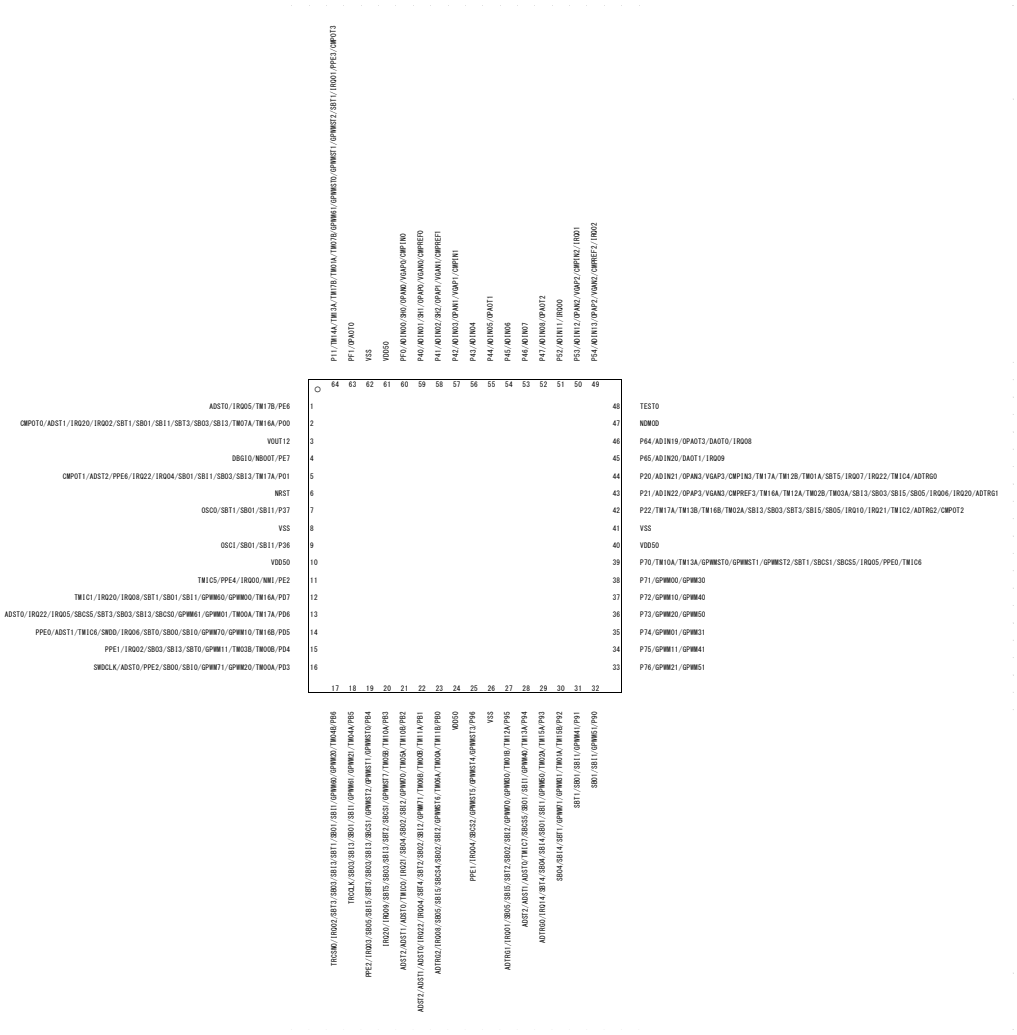


Figure 1.4-3 Pin Configuration Figure of 64 pins

1.4.2 Pin Functions

The pin functions are listed in Table 1.4-1 and Table 1.4-2 .

Table 1.4-1 Pin Functions (for each pin)

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
1	-	-	-	PE5	TM17B, GPWM60	SBT1, SBCS1	IRQ00, PPE5, ADST0
2	1	1	-	PE6	TM17B	-	IRQ05, ADST0
3	2		-	PF2	-	-	-
4	3	2	-	P00	TM16A, TM07A	SBI3, SBO3, SBT3, SBI1, SBO1, SBT1	IRQ02, IRQ20, ADST1, CMPOT0
5	4	3	VOUT12	-	-	-	-
6	5	4	NBOOT	PE7	-	-	DBGIO
7	6	5	-	P01	TM17A	SBI3, SBO3, SBI1, SBO1	IRQ04, IRQ22, PPE6, ADST2, CMPOT1
8	7	-	-	PE4	TM13A	SBT1	IRQ01, PPE4
9	8	-	-	PE3	TM13B	SBCS1	IRQ02, PPE5
10	9	6	NRST	-	-	-	-
11	10	7	OSCO	P37	-	SBI1, SBO1, SBT1	-
12	11	8	VSS	-	-	-	-
13	12	9	OSCI	P36	-	SBI1, SBO1	-
14	13	10	VDD50	-	-	-	-
15	14	11	-	PE2	-	-	NMI, IRQ00, TMIC5, PPE4
16	-	-	-	PE1	TM17B TM02A	SBCS1, SBCS3	IRQ15
17	-	-	-	PE0	TM16B, TM00B, TM02B	SBI1, SBO1, SBT1	IRQ07, IRQ21
18	15	12	-	PD7	TM16A, GPWM00, GPWM60	SBI1, SBO1, SBT1	IRQ08, IRQ20, TMIC1

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
19	16	13	-	PD6	TM17A, TM00A, GPWM01, GPWM61	SBCS0, SBI3, SBO3, SBT3, SBCS5	IRQ05, IRQ22, ADST0
20	17	14	-	PD5	TM16B, TMIC6, GPWM10, GPWM70	SBI0, SBO0, SBT0	IRQ06, SWDD, ADST1, PPE0
21	18	15	-	PD4	TM00B, TM03B, GPWM11	SBT0, SBI3, SBO3	IRQ02, PPE1
22	19	16	-	PD3	TM00A, GPWM20, GPWM71	SBI0, SBO0	PPE2, ADST0, SWDCLK
23	20	-	-	PD2	TM00B, TM02A, GPWM00, GPWM21	SBT1, SBI5, SBO5	TRCD0
24	-	-	-	PD1	TM01A, GPWM01, GPWM60	SBI5, SBO5	TRCD1
25	-	-	-	PD0	TM03A, GPWM10, GPWM61	SBT5	TRCD2
26	-	-	-	PB7	TM03B, GPWM11	SBT1, SBT3	TRCD3
27	21	17	-	PB6	TM04B, GPWM20, GPWM60	SBI1, SBO1, SBT1, SBI3, SBO3, SBT3	IRQ02, TRCSWO
28	22	18	-	PB5	TM04A, GPWM21, GPWM61	SBI1, SBO1 SBI3, SBO3	TRCCLK
29	23	-	VDD50	-	-	-	-
30	24	19	-	PB4	-	SBCS1, SBI3, SBO3, SBT3, SBI5, SBO5	IRQ03, PPE2, GPWMST0, GPWMST1, GPWMST2
31	25	-	VSS	-	-	-	-
32	26	20	-	PB3	TM10A, TM05B	SBCS1, SBT2, SBI3, SBO3, SBT5	GPWMST7, IRQ09, IRQ20

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
33	27	21	-	PB2	TM10B, TM05A, GPWM70	SBI2, SBO2, SBO4	IRQ21, TMIC0, ADST0, ADST1, ADST2
34	28	22	-	PB1	TM11A, TM00B, TM06B, GPWM71	SBI2, SBO2, SBT2, SBT4	IRQ04, IRQ22, ADST0, ADST1, ADST2
35	29	23	-	PB0	TM11B, TM00A, TM06A	SBI2, SBO2, SBCS4, SBI5, SBO5	GPWMST6, IRQ08, ADTRG2
36	30	-	-	PA5	TM12A, TM01B	SBI2, SBO2, SBT2, SBI5, SBO5	IRQ01, ADTRG1
37	-	-	-	PA4	TM12B, TM03B	SBT2, SBT5	ADTRG0
38	31	-	-	PA3	TM13A	SBI1, SBO1, SBCS5	TMIC7, ADST0, ADST1, ADST2
39	-	-	-	PA2	TM13B, TM03A	SBCS2, SBI1, SBO1, SBT1	ADST0, ADST1, ADST2
40	-	-	-	PA1	TM15A, TM02A,	SBI1, SBO1, SBI4, SBO4, SBT4	GPWMST3, GPWMST4, GPWMST5, IRQ14, ADTRG0
41	-	-	-	PA0	TM15B, TM01A,	SBT1, SBI1, SBO4	-
42	32	24	VDD50	-	-	-	-
43	33	25	-	P96	-	SBCS2	GPWMST3, GPWMST4, GPWMST5, IRQ04, PPE1
44	34	26	VSS	-	-	-	-
45	35	27	-	P95	TM12A, TM01B, GPWM30, GPWM70	SBI2, SBO2, SBT2, SBI5, SBO5	IRQ01, ADTRG1

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
46	36	28	-	P94	TM13A, GPWM40	SBI1, SBO1, SBCS5	TMIC7, ADST0, ADST1, ADST2
47	37	29	-	P93	TM15A, TM02A, GPWM50	SBI1, SBO1, SBI4, SBO4, SBT4	IRQ14, ADTRG0
48	38	30	-	P92	TM15B, TM01A, GPWM31, GPWM71	SBT1, SBI4, SBO4	-
49	39	31	-	P91	GPWM41	SBI1, SBO1, SBT1	-
50	40	32	-	P90	GPWM51	SBI1, SBO1	-
51	41	33	-	P76	GPWM21, GPWM51	-	-
52	42	34	-	P75	GPWM11, GPWM41	-	-
53	43	35	-	P74	GPWM01, GPWM31	-	-
54	44	36	-	P73	GPWM20, GPWM50	-	-
55	45	37	-	P72	GPWM10, GPWM40	-	-
56	46	38	-	P71	GPWM00, GPWM30	-	-
57	47	39	-	P70	TM10A, TM13A	SBT1, SBCS1, SBCS5	GPWMST0, GPWMST1, GPWMST2, IRQ05, PPE0, TMIC6
58	-	-	-	P33	TM14A, TM12A, TM00A, GPWM61, GPWM71	-	GPWMST0, GPWMST1, GPWMST2, IRQ13
59	-	-	-	P32	TM14B, TM12B, TM03A, GPWM60, GPWM70	-	IRQ12
60	48	40	VDD50	-	-	-	-
61	49	-	-	P31	TM10A, TM13A	-	IRQ06, IRQ20, TMIC6

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
62	50	41	VSS	-	-	-	-
63	51	-	-	P30	TM10B, TM13B, TM03B	SBT0, SBCS0, SBCS5	IRQ07, IRQ21, CMPOT3
64	52	-	-	P27	TM12A, TM11A, TM01A, TM03A	SBT5	IRQ15, PPE3
65	-	-	-	P24	TM15B, TM01B, TM03A	SBT0, SBCS0, SBT5	IRQ04, CMPOT0
66	-	-	-	P23	TM16A, TM01A	SBI3, SBO3, SBI0, SBO0, SBI5, SBO5	IRQ11, CMPOT1
67	53	42	-	P22	TM17A, TM13B, TM16B, TM02A	SBI3, SBO3, SBT3, SBI5, SBO5	IRQ10, IRQ21, TMIC2, ADTRG2, CMPOT2
68	54	43	-	P21	TM16A, TM12A, TM02B, TM03A	SBI3, SBO3, SBI5, SBO5	IRQ06, IRQ20, ADTRG1, ADIN22, OPAP3, VGAN3, CMPREF3
69	55	44	-	P20	TM17A, TM12B, TM01A	SBT5	IRQ07, IRQ22, TMIC4, ADTRG0, ADIN21, OPAN3, VGAP3, CMPIN3
70	56	45	-	P65	-	-	IRQ09, ADIN20, DAOT1
71	57	46	-	P64	-	-	IRQ08, ADIN19, OPAOT3, DAOT0
72	58	47	NDMOD	-	-	-	-
73	59	48	TEST0	-	-	-	-
74	-	-	-	P63	-	-	IRQ07, ADIN18
75	-	-	-	P62	-	-	IRQ06, ADIN17

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
76	-	-	-	P61	-	-	IRQ05, ADIN16
77	60	-	-	P60	-	-	IRQ04, ADIN15
78	61	-	-	P55	-	-	IRQ03, ADIN14
79	62	49	-	P54	-	-	IRQ02, ADIN13, OPAP2, VGAN2, CMPREF2
80	63	50	-	P53	-	-	IRQ01, ADIN12, OPAN2, VGAP2, CMPIN2
81	64	51	-	P52	-	-	IRQ00, ADIN11
82	65	-	-	P51	-	-	ADIN10
83	66	-	-	P50	-	-	ADIN09
84	67	52	-	P47	-	-	ADIN08, OPAOT2
85	68	53	-	P46	-	-	ADIN07
86	69	54	-	P45	-	-	ADIN06
87	70	55	-	P44	-	-	ADIN05, OPAOT1
88	71	56	-	P43	-	-	ADIN04
89	72	57	-	P42	-	-	ADIN03, OPAN1, VGAP1, CMPIN1
90	73	58	-	P41	-	-	ADIN02, SH2, OPAP1, VGAN1, CMPREF1
91	74	59	-	P40	-	-	ADIN01, SH1, OPAP0, VGAN0, CMPREF0
92	75	60	-	PF0	-	-	ADIN00, SH0, OPAN0, VGAP0 CMPIN00
93	76	61	VDD50	-	-	-	-
94	77	62	VSS	-	-	-	-
95	78	63	-	PF1	-	-	OPAOT0

100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
96	-	-	-	P82	TM15B, TM02A	SBT2, SBT3	IRQ03
97	-	-	-	P81	TM16B, TM02B	SBI2, SBO2, SBI3, SBO3	-
98	-	-	-	P80	TM17B	SBI2, SBO2, SBT2, SBI3, SBO3, SBT3	IRQ05, TMIC4, CMPOT3
99	79	64	-	P11	TM14A, TM13A, TM17B, TM01A, TM07B, GPWM61	SBT1	GPWMST0, GPWMST1, GPWMST2, IRQ01, PPE3, CMPOT3
100	80	-	-	P10	TM16B, TM13B, TM07A, GPWM60	SBCS2, SBI1, SBO1	GPWMST3, GPWMST4, GPWMST5, IRQ00, IRQ21, PPE6, TMIC3

Table 1.4-2 Pin Functions (for each function)

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
External power pin	VDD50	14, 29, 42, 60, 93	13, 23, 32, 48, 76	10, 24, 40, 61	Input
Power pin for internal circuit	VOUT12	5	4	3	Output
GND	VSS	12, 31, 44, 62, 94	11, 25, 34, 50, 77	8, 26, 41, 62	Input
Debugger	SWDCLK	22	19	16	Input
	SWDD	20	17	14	I/O
	TRCCLK	28	22	18	Output
	TRCSWO	27	21	17	Output
	TRCD0	23	20	-	Output
	TRCD1	24	-	-	Output
	TRCD2	25	-	-	Output
	TRCD3	26	-	-	Output
	DBGIO	6	5	4	I/O
External oscillation	OSCI	13	12	9	Input
	OSCO	11	10	7	Output
Reset	NRST	10	9	6	Input
Mode pin	NBOOT	6	5	4	Input
	NDMOD	72	58	47	Input
	TEST0	73	59	48	Input
External interrupt	NMI	15	14	11	Input
	IRQ00	1, 15, 81, 100	14, 64, 80	11, 51	Input
	IRQ01	8, 36, 45, 80, 99	7, 30, 35, 63, 79	27, 50, 64	Input
	IRQ02	4, 9, 21, 27, 79	3, 8, 18, 21, 62	2, 15, 17, 49	Input
	IRQ03	30, 78, 96	24, 61	19	Input
	IRQ04	7, 34, 43, 65, 77	6, 28, 33, 60	5, 22, 25	Input
	IRQ05	2, 19, 57, 76, 98	1, 16, 47	1, 13, 39	Input
	IRQ06	20, 61, 68, 75	17, 49, 54	14, 43	Input
	IRQ07	17, 63, 69, 74	51, 55	44	Input
	IRQ08	18, 35, 71	15, 29, 57	12, 23, 46	Input
	IRQ09	32, 70	26, 56	20, 45	Input
	IRQ10	67	53	42	Input
	IRQ11	66	-	-	Input
	IRQ12	59	-	-	Input
	IRQ13	58	-	-	Input
	IRQ14	40, 47	37	29	Input
	IRQ15	16, 64	52	-	Input
	IRQ20	4, 18, 32, 61, 68	3, 15, 26, 49, 54	2, 12, 20, 43	Input
	IRQ21	17, 33, 63, 67, 100	27, 51, 53, 80	21, 42	Input
	IRQ22	7, 19, 34, 69	6, 16, 28, 55	5, 13, 22, 44	Input

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
16-bit timer	TM00A	19, 22, 35, 58	16, 19, 29	13, 16, 23	I/O
	TM00B	17, 21, 23, 34	18, 20, 28	15, 22	I/O
	TM01A	24, 41, 48, 64, 66, 69, 99	38, 52, 55, 79	30, 44, 64	I/O
	TM01B	36, 45, 65	30, 35	27	I/O
	TM02A	16, 23, 40, 47, 67, 96	20, 37, 53	29, 42	I/O
	TM02B	17, 68, 97	54	43	I/O
	TM03A	25, 39, 59, 64, 65, 68	52, 54	43	I/O
	TM03B	21, 26, 37, 63	18, 51	15	I/O
	TM04A	28	22	18	I/O
	TM04B	27	21	17	I/O
	TM05A	33	27	21	I/O
	TM05B	32	26	20	I/O
	TM06A	35	29	23	I/O
	TM06B	34	28	22	I/O
	TM07A	4, 100	3, 80	2	I/O
	TM07B	99	79	64	I/O
	TM10A	32, 57, 61	26, 47, 49	20, 39	I/O
	TM10B	33, 63	27, 51	21	I/O
	TM11A	34, 64	28, 52	22	I/O
	TM11B	35	29	23	I/O
	TM12A	36, 45, 58, 64, 68	30, 35, 52, 54	27, 43	I/O
	TM12B	37, 59, 69	55	44	I/O
	TM13A	8, 38, 46, 57, 61, 99	7, 31, 36, 47, 49, 79	28, 39, 64	I/O
	TM13B	9, 39, 63, 67, 100	8, 51, 53, 80	42	I/O
	TM14A	58, 99	79	64	I/O
	TM14B	59	-	-	I/O
	TM15A	40, 47	37	29	I/O
	TM15B	41, 48, 65, 96	38	30	I/O
	TM16A	4, 18, 66, 68	3, 15, 54	2, 12, 43	I/O
	TM16B	17, 20, 67, 97, 100	17, 53, 80	14, 42	I/O
	TM17A	7, 19, 67, 69	6, 16, 53, 55	5, 13, 42 ,44	I/O
	TM17B	1, 2, 16, 98, 99	1, 79	1, 64	I/O

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
Input capture factor	TMIC0	33	27	21	Input
	TMIC1	18	15	12	Input
	TMIC2	67	53	42	Input
	TMIC3	100	80	-	Input
	TMIC4	69, 98	55	44	Input
	TMIC5	15	14	11	Input
	TMIC6	20, 57, 61	17, 47, 49	14, 39	Input
	TMIC7	38, 46	31, 36	28	Input
Power control PWM output	GPWM00	18, 23, 56	15, 20, 46	12, 38	Output
	GPWM01	19, 24, 53	16, 43	13, 35	Output
	GPWM10	20, 25, 55	17, 45	14, 37	Output
	GPWM11	21, 26, 52	18, 42	15, 34	Output
	GPWM20	22, 27, 54	19, 21, 44	16, 17, 36	Output
	GPWM21	23, 28, 51	20, 22, 41	18, 33	Output
	GPWM30	45, 56	35, 46	27, 38	Output
	GPWM31	48, 53	38, 43	30, 35	Output
	GPWM40	46, 55	36, 45	28, 37	Output
	GPWM41	49, 52	39, 42	31, 34	Output
	GPWM50	47, 54	37, 44	29, 36	Output
	GPWM51	50, 51	40, 41	32, 33	Output
	GPWM60	1, 18, 24, 27, 59, 100	15, 21, 80	12, 17	Output
	GPWM61	19, 25, 28, 58, 99	16, 22, 79	13, 18, 64	Output
	GPWM70	20, 33, 45, 59	17, 27, 35	14, 21, 27	Output
	GPWM71	22, 34, 48, 58	19, 28, 38	16, 22, 30	Output
Power control PWM monitor	GPWMST0	30, 57, 58, 99	24, 47, 79	19, 39, 64	Output
	GPWMST1	30, 57, 58, 99	24, 47, 79	19, 39, 64	Output
	GPWMST2	30, 57, 58, 99	24, 47, 79	19, 39, 64	Output
	GPWMST3	40, 43, 100	33, 80	25	Output
	GPWMST4	40, 43, 100	33, 80	25	Output
	GPWMST5	40, 43, 100	33, 80	25	Output
	GPWMST6	35	29	23	Output
	GPWMST7	32	26	20	Output
External Input for pin protection	PPE0	20, 57	17, 47	14, 39	Input
	PPE1	21, 43	18, 33	15, 25	Input
	PPE2	22, 30	19, 24	16, 19	Input
	PPE3	64, 99	52, 79	64	Input
	PPE4	8, 15	7, 14	11	Input
	PPE5	1, 9	8	-	Input
	PPE6	7, 100	6, 80	5	Input

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
Serial interface	SBCS0	19, 63, 65	16, 51	13	I/O
	SBI0	20, 22, 66	17, 19	14, 16	Input
	SBO0	20, 22, 66	17, 19	14, 16	I/O
	SBT0	20, 21, 63, 65	17, 18, 51	14, 15	I/O
	SBCS1	1, 9, 16, 30, 32, 57	8, 24, 26, 47	19, 20, 39	I/O
	SBI1	4, 7, 11, 13, 17, 18, 27, 28, 38, 39, 40, 46, 47, 49, 50, 100	3, 6, 10, 12, 15, 21, 22, 31, 36, 37, 39, 40, 80	2, 5, 7, 9, 12, 17, 18, 28, 29, 31, 32	Input
	SBO1	4, 7, 11, 13, 17, 18, 27, 28, 38, 39, 40, 46, 47, 49, 50, 100	3, 6, 10, 12, 15, 21, 22, 31, 36, 37, 39, 40, 80	2, 5, 7, 9, 12, 17, 18, 28, 29, 31, 32	I/O
	SBT1	1, 4, 8, 11, 17, 18, 23, 26, 27, 39, 41, 48, 49, 57, 99	3, 7, 10, 15, 20, 21, 38, 39, 47, 79	2, 7, 12, 17, 30, 31, 39, 64	I/O
	SBCS2	39, 43, 100	33, 80	25	I/O
	SBI2	33, 34, 35, 36, 45, 97, 98	27, 28, 29, 30, 35	21, 22, 23, 27	Input
	SBO2	33, 34, 35, 36, 45, 97, 98	27, 28, 29, 30, 35	21, 22, 23, 27	I/O
	SBT2	32, 34, 36, 37, 45, 96, 98	26, 28, 30, 35	20, 22, 27	I/O
	SBCS3	16	-	-	I/O
	SBI3	4, 7, 19, 21, 27, 28, 30, 32, 66, 67, 68, 97, 98	3, 6, 16, 18, 21, 22, 24, 26, 53, 54	2, ,5 13, 15, 17, 18, 19, 20, 42, 43	Input
	SBO3	4, 7, 19, 21, 27, 28, 30, 32, 66, 67, 68, 97, 98	3, 6, 16, 18, 21, 22, 24, 26, 53, 54	2, ,5 13, 15, 17, 18, 19, 20, 42, 43	I/O
	SBT3	4, 19, 26, 27, 30, 67, 96, 98	3, 16, 21, 24, 53	2, 13, 17, 19, 42	I/O
	SBCS4	35	29	23	I/O
	SBI4	40, 41, 47, 48	37, 38	29, 30	Input
	SBO4	33, 40, 41, 47, 48	27, 37, 38	21, 29, 30	I/O
	SBT4	34, 40, 47	28, 37	22, 29	I/O
	SBCS5	19, 38, 46, 57, 63	16, 31, 36, 47, 51	13, 28, 39	I/O
	SBI5	23, 24, 30, 35, 36, 45, 66, 67, 68	20, 24, 29, 30, 35, 53, 54	19, 23, 27, 42, 43	Input
	SBO5	23, 24, 30, 35, 36, 45, 66, 67, 68	20, 24, 29, 30, 35, 53, 54	19, 23, 27, 42, 43	I/O
	SBT5	25, 32, 37, 64, 65, 69	26, 52, 55	20. 44	I/O

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
A/D input	ADIN00	92	75	60	Input
	ADIN01	91	74	59	Input
	ADIN02	90	73	58	Input
	ADIN03	89	72	57	Input
	ADIN04	88	71	56	Input
	ADIN05	87	70	55	Input
	ADIN06	86	69	54	Input
	ADIN07	85	68	53	Input
	ADIN08	84	67	52	Input
	ADIN09	83	66	-	Input
	ADIN10	82	65	-	Input
	ADIN11	81	64	51	Input
	ADIN12	80	63	50	Input
	ADIN13	79	62	49	Input
	ADIN14	78	61	-	Input
	ADIN15	77	60	-	Input
	ADIN16	76	-	-	Input
	ADIN17	75	-	-	Input
	ADIN18	74	-	-	Input
	ADIN19	71	57	46	Input
	ADIN20	70	56	45	Input
	ADIN21	69	55	44	Input
	ADIN22	68	54	43	Input
A/D monitor	ADST0	1, 2, 19, 22, 33, 34, 38, 39, 46	1, 16, 19, 27, 28, 31, 36	1, 13, 16, 21, 22, 28	Output
	ADST1	4, 20, 33, 34, 38, 39, 46	3, 17, 27, 28, 31, 36	2, 14, 21, 22, 28	Output
	ADST2	7, 33, 34, 38, 39, 46	6, 27, 28, 31, 36	5, 21, 22, 28	Output
A/D triger input	ADTRG0	37, 40, 47, 69	37, 55	29, 44	Input
	ADTRG1	36, 45, 68	30, 35, 54	27, 43	Input
	ADTRG2	35, 67	29, 53	23, 42	Input
SH input	SH0	92	75	60	Input
	SH1	91	74	59	Input
	SH2	90	73	58	Input
VGA input	VGAP0	92	75	60	Input
	VGAN0	91	74	59	Input
	VGAP1	89	72	57	Input
	VGAN1	90	73	58	Input
	VGAP2	80	63	50	Input
	VGAN2	79	62	49	Input
	VGAP3	69	55	44	Input
	VGAN3	68	54	43	Input

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
OPA input	OPAP0	91	74	59	Input
	OPAN0	92	75	60	Input
	OPAP1	90	73	58	Input
	OPAN1	89	72	57	Input
	OPAP2	79	62	49	Input
	OPAN2	80	63	50	Input
	OPAP3	68	54	43	Input
	OPAN3	69	55	44	Input
OPA output	OPAOT0	95	78	63	Output
	OPAOT1	87	70	55	Output
	OPAOT2	84	67	52	Output
	OPAOT3	71	57	46	Output
Comarator input	CMPIN0	92	75	60	Input
	CMPREF0	91	74	59	Input
	CMPIN1	89	72	57	Input
	CMPREF1	90	73	58	Input
	CMPIN2	80	63	50	Input
	CMPREF2	79	62	49	Input
	CMPIN3	69	55	44	Input
	CMPREF3	68	54	43	Input
Comarator output	CMPOT0	4, 65	3	2	Output
	CMPOT1	7, 66	6	5	Output
	CMPOT2	67	53	42	Output
	CMPOT3	63, 98, 99	51, 79	64	Output
D/A output	DAOT0	71	57	46	Output
	DAOT1	70	56	45	Output

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
I/O port	P00	4	3	2	I/O
	P01	7	6	5	I/O
	P10	100	80	-	I/O
	P11	99	79	64	I/O
	P20	69	55	44	I/O
	P21	68	54	43	I/O
	P22	67	53	42	I/O
	P23	66	-	-	I/O
	P24	65	-	-	I/O
	P27	64	52	-	I/O
	P30	63	51	-	I/O
	P31	61	49	-	I/O
	P32	59	-	-	I/O
	P33	58	-	-	I/O
	P36	13	12	9	I/O
	P37	11	10	7	I/O
	P40	91	74	59	I/O
	P41	90	73	58	I/O
	P42	89	72	57	I/O
	P43	88	71	56	I/O
	P44	87	70	55	I/O
	P45	86	69	54	I/O
	P46	85	68	53	I/O
	P47	84	67	52	I/O
	P50	83	66	-	I/O
	P51	82	65	-	I/O
	P52	81	64	51	I/O
	P53	80	63	50	I/O
	P54	79	62	49	I/O
	P55	78	61	-	I/O
	P60	77	60	-	I/O
	P61	76	-	-	I/O
	P62	75	-	-	I/O
	P63	74	-	-	I/O
	P64	71	57	46	I/O
	P65	70	56	45	I/O

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
I/O port	P70	57	47	39	I/O
	P71	56	46	38	I/O
	P72	55	45	37	I/O
	P73	54	44	36	I/O
	P74	53	43	35	I/O
	P75	52	42	34	I/O
	P76	51	41	33	I/O
	P80	98	-	-	I/O
	P81	97	-	-	I/O
	P82	96	-	-	I/O
	P90	50	40	32	I/O
	P91	49	39	31	I/O
	P92	48	38	30	I/O
	P93	47	37	29	I/O
	P94	46	36	28	I/O
	P95	45	35	27	I/O
	P96	43	33	25	I/O
	PA0	41	-	-	I/O
	PA1	40	-	-	I/O
	PA2	39	-	-	I/O
	PA3	38	31	-	I/O
	PA4	37	-	-	I/O
	PA5	36	30	-	I/O
	PB0	35	29	23	I/O
	PB1	34	28	22	I/O
	PB2	33	27	21	I/O
	PB3	32	26	20	I/O
	PB4	30	24	19	I/O
	PB5	28	22	18	I/O
	PB6	27	21	17	I/O
	PB7	26	-	-	I/O
	PD0	25	-	-	I/O
	PD1	24	-	-	I/O
	PD2	23	20	-	I/O
	PD3	22	19	16	I/O
	PD4	21	18	15	I/O
	PD5	20	17	14	I/O
	PD6	19	16	13	I/O
	PD7	18	15	12	I/O

Functions	Pin name	100 pins Pin No.	80 pins Pin No.	64 pins Pin No.	I/O
I/O port	PE0	17	-	-	I/O
	PE1	16	-	-	I/O
	PE2	15	14	11	Input
	PE3	9	8	-	I/O
	PE4	8	7	-	I/O
	PE5	1	-	-	I/O
	PE6	2	1	1	I/O
	PE7	6	5	4	I/O
	PF0	92	75	60	I/O
	PF1	95	78	63	I/O
	PF2	3	2	-	I/O

Note:

For pins to which multiple functions can be assigned, set only one to be valid.

Example: For 100 pins, it is prohibited to select No.20 and No.22 as SBO0 pin at the same time.

1.5 Block Diagram

Figure 1.5-1 shows the block diagram.

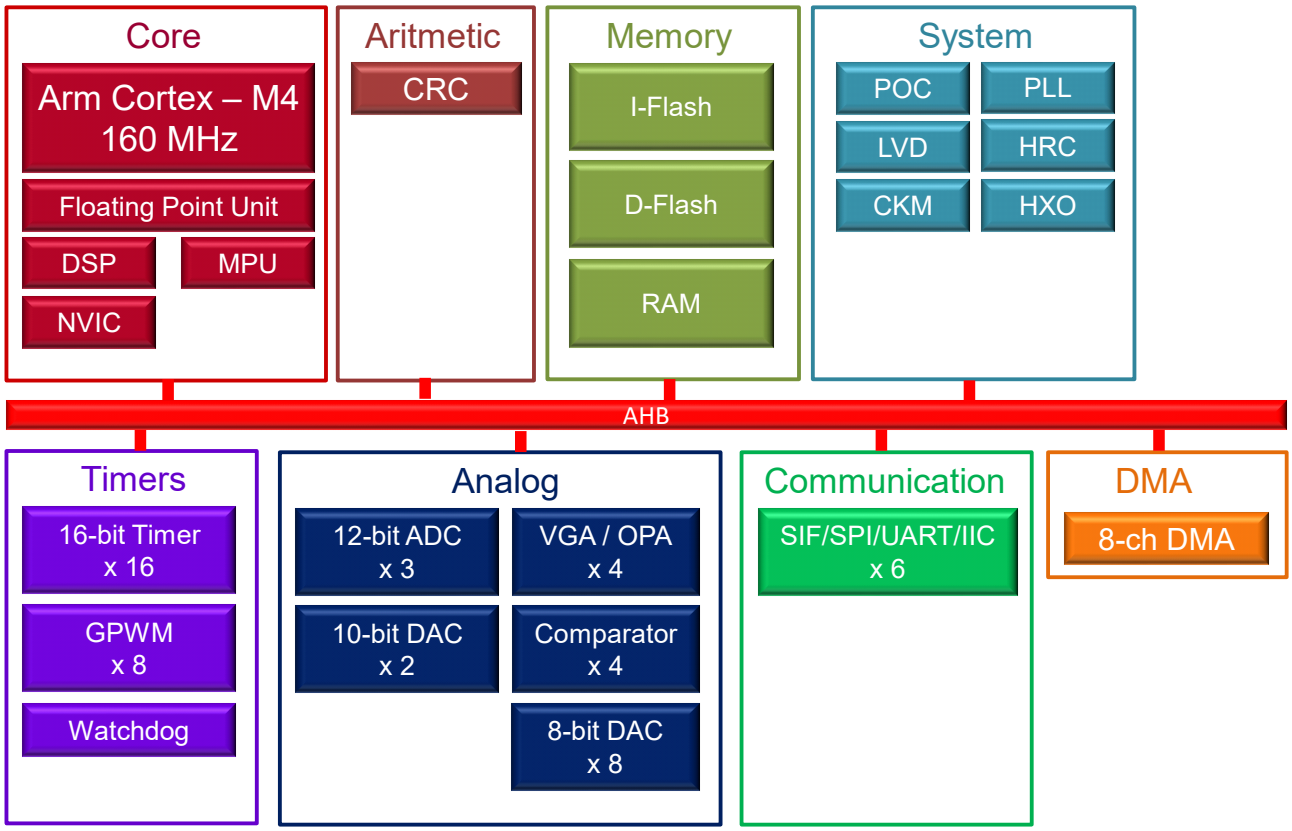


Figure 1.5-1 Block Diagram

1.6 Electrical Characteristics

About electrical specifications, standard specifications are described in the manual of this LSI. When using this LSI, consult the staff in our sales offices for the product specifications.

Hint:

T. B. D. is planned to update at the time of revising the manual.

1.6.1 Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD50A}	-0.3 to 7.0	V
A2	Internal power supply voltage		V_{OUT12A}	-0.3 to 1.6	V
A3	Input pin voltage		V_{I1}	-0.3 to V_{DD50} +0.3 (Upper limit: 7.0)	V
A4	I/O pin voltage		V_{I2}	-0.3 to V_{DD50} +0.3 (Upper limit: 7.0)	V
A5	Average Output current	I/O pin 1, 2 (*1)	I_{O1}(avg)	±12	mA
A6		I/O pin 3 (*2)	I_{O2}(avg)	±24	mA
A7		Total of all pins	I_{O3}	±70	mA
A8	Average injection current	By a I/O pin	I_{INJ1}	±2	mA
A9		By a total I/O pin	I_{INJ}	±20	mA
A10	Power dissipation		P_D	800	mW
A11	Operating case temperature		T_{copr}	-40 to +110	°C
A12	Operating junction temperature		T_j	-40 to +125	°C
A13	Storage temperature		T_{stg}	-40 to +125	°C

Note:

Although this LSI has internal ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gate.

This LSI may sustain permanent damage if it gets stress which is higher than the above stated absolute maximum rating even only for a second. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.

Note:

*1 I/O pins 1 and 2 is I/O pins 1 and 2 of 1.6.3 DC Characteristics.

Note:

*2 I/O pin 3 is I/O pin 3 of 1.6.3 DC Characteristics.

1.6.2 Operation Conditions

Power supply voltage during operation					V_{SS} = 0.0 V Tc = -40 °C to 110 °C	
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B1	External power supply voltage	V_{DD50}	V_{RST5N}	5.0	5.5	V
B2	Internal power supply voltage	V_{OUT12}	-	1.25	-	

Oscillation pin					V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc= -40 °C to 110 °C	
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B3	External oscillation frequency (Ceramic/Crystal)	F_{OSC}	4.0	-	20.0	MHz
B4	External oscillation Feedback resistor	R_{FB}	-	1.0	-	MΩ

Note:

Oscillation circuit characteristics and peripheral parts(load capacity, damping resister, and feedback resister) are different by each oscillator and substrate. To decide appropriate capacity value for circuit constant, please consult the oscillator manufacturer.

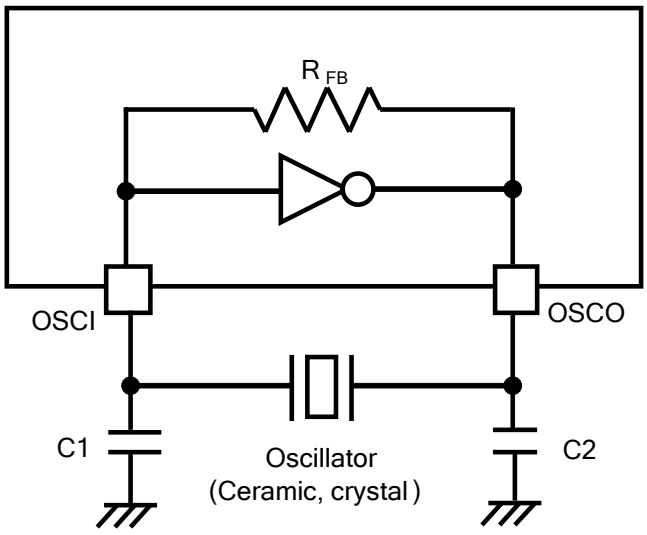


Figure 1.6-1 Oscillation Circuit

External clock input OSCI (OSCO left open)			V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B5	Clock frequency	F_{CP}	4.0	-	20.0	MHz
B6	High level pulse width	t_{wh1}	20	-	-	ns
B7	Low level pulse width	t_{wl1}	20	-	-	
B8	Rising time	t_{wr1}	-	-	5	
B9	Falling time	t_{wf1}	-	-	5	

Note:

It is necessary to set clock duty ratio from 45 % to 55 %.

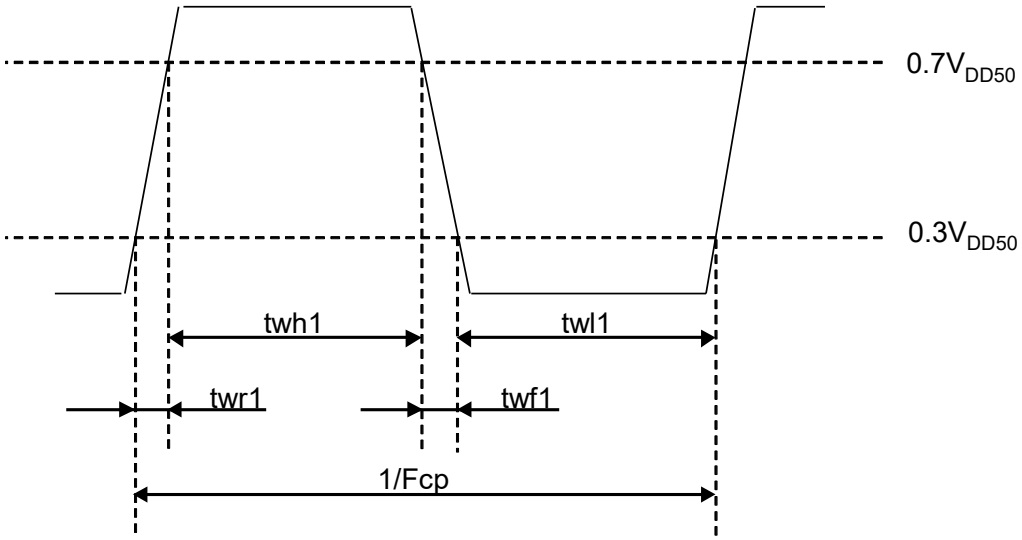


Figure 1.6-2 OSCI Timing Chart

1.6.3 DC Characteristics

Power supply current during operation			V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C Output pins left open			
Parameter		Sym-bol	Conditions	Rating		Unit
				TYP	MAX	
C1	NORMAL mode	I_{DD1}	HXOCLK = 10 MHz, PLL is used, CPUCLK = 160 MHz, IOCLK = 80 MHz CPU and Peripheral circuits are operating. Analog circuits are stopped.	T.B.D	T.B.D	mA
C2	SLEEP mode	I_{DD2}	HXOCLK = 10 MHz, PLL is used, CPUCLK = 160 MHz, IOCLK = 80 MHz CPU is stopped, Peripheral circuits are operating. Analog circuits are stopped.	T.B.D	T.B.D	
C3	DEEP SLEEP mode	I_{DD3}	HXOCLK = 10 MHz, PLLCLK is stopped, CPUCLK, IOCLK is stopped, CPU and Peripheral circuits are stopped. Analog circuits are stopped.	T.B.D	T.B.D	
C4		I_{DD4}	HXOCLK, PLLCLK, CPUCLK, IOCLK is stopped	T.B.D	T.B.D	

Note:

The measurement conditions are as follows.

- All I/O pins are output state. (No load)

Input pin 1 NDMOD				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C5	Input voltage "High level"	V_{IH1}		V_{DD50} × 0.7	-	V_{DD50}	V
C6	Input voltage "Low level"	V_{IL1}		V_{SS}	-	V_{DD50} × 0.3	
C7	Internal pull-up resistor	R_{IO1}	V_{IN} = 0 V	15	30	60	kΩ

Input pin 2 TEST0				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C8	Input voltage "High level"	V_{IH2}		V_{DD50} × 0.7	-	V_{DD50}	V
C9	Input voltage "Low level"	V_{IL2}		V_{SS}	-	V_{DD50} × 0.3	
C10	Internal pull-down resistor	R_{IO2}	V_{IN} = V_{DD50}	15	30	60	kΩ

Input pin 3 PE2				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C11	Input voltage "High level"	V_{IH3}		V_{DD50} × 0.7	-	V_{DD50}	V
C12	Input voltage "Low level"	V_{IL3}		V_{SS}	-	V_{DD50} × 0.3	
C13	Input leakage current	I_{LK3}	V_{IN} = 0 V to V_{DD50}	-	-	±5	μA

I/O pin 1 NRST				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C14	Input voltage "High level"	V_{IH5}		V_{DD50} × 0.7	-	V_{DD50}	V
C15	Input voltage "Low level"	V_{IL5}		V_{SS}	-	V_{DD50} × 0.3	
C16	Internal pull-up resistor	R_{IO5}	V_{IN} = 0 V	15	30	60	kΩ
C17	Output voltage "Low level"	V_{OL5}	V_{DD5} = V_{RST5P} I_{OL} = 3.0 mA	-	-	0.5	V

I/O pin 2 P00, P01, P20, P21, P22, P23, P24, P27, P30, P31, P36, P37, P40, P41, P42, P43, P44, P45, P46, P47, P50, P51, P52, P53, P54, P55, P60, P61, P62, P63, P64, P65, P70, P80, P81, P82, P96, PA0, PA1, PA2, PA3, PA4, PA5, PE0, PE1, PE3, PE4, PE6, PF0, PF1, PF2			V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110°C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C18	Input voltage "High level"	V_{IH6}		V_{DD50} × 0.7	-	V_{DD50}	V
C19	Input voltage "Low level"	V_{IL6}		V_{SS}	-	V_{DD50} × 0.3	
C20	Input leakage current	I_{LK6}	V_{IN} = 0 V to V_{DD50}	-	-	±5	µA
C21	Internal pull-up resistor	R_{IO6}	V_{IN} = 0 V	15	30	60	kΩ
C22	Output voltage "High level"	V_{OH6}	I_{OH} = -3.0 mA	4.5	-	-	V
C23	Output voltage "Low level"	V_{OL6}	I_{OL} = 3.0 mA	-	-	0.5	

I/O pin 3 P10, P11, P32, P33, P71, P72, P73, P74, P75, P76, P90, P91, P92, P93, P94, P95, PB0, PB1, PB2, PB3, PB4, PB5, PB6, PB7, PD0, PD1, PD2, PD3, PD4, PD5, PD6, PD7, PE5, PE7			V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C				
Parameter		Sym-bol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C24	Input voltage "High level"	V_{IH7}		V_{DD50} × 0.7	-	V_{DD50}	V
C25	Input voltage "Low level"	V_{IL7}		V_{SS}	-	V_{DD50} × 0.3	
C26	Input leakage current	I_{LK7}	V_{IN} = 0 V to V_{DD50}	-	-	±5	µA
C27	Internal pull-up resistor	R_{IO7}	V_{IN} = 0 V	15	30	60	kΩ
C28	Output voltage "High level"	V_{OH7}	I_{OH} = -6.0 mA	4.5	-	-	V
C29	Output voltage "Low level"	V_{OL7}	I_{OL} = 6.0 mA	-	-	0.5	

1.6.4 Analog Characteristics

The electrical characteristics of analog are shown below.

1.6.4.1 12-bit A/D Converter

ADC0, ADC1, ADC2 (When don't used in Individual SHC)				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution	-		-	-	12	Bits
D2	Conversion clock	-		10	-	40	MHz
D3	Integral non-linearity error	$INLE_{AD}$	Sampling time ≥ 150 ns Conversion clock = 40 MHz	-	-	±3	LSB
D4	Differential non-linearity error	$DNLE_{AD}$		-	-	±3	LSB
D5	Zero transition voltage	-		-20	-	20	mV
D6	Full-scale transition voltage	-		4980	-	5020	mV
D7	A/D conversion time	-		0.5	-	-	µs
D8	Input dynamic range	V_{IA}		V_{SS}	-	V_{DD50}	V
D9	Power supply current during operation	I_{AD}	Conversion clock = 40 MHz	-	2.5	-	mA/ unit

1.6.4.2 Programmable Gain Amplifier with Op-Amp (VGA)

VGA0, VGA1, VGA2, VGA3 (When used in VGA mode)				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D10	Gain	G_{VGA}		2	-	20	Times
D11	Gain error	G_{ERR}		-	±0.5	±2.0	%
D12	Output offset voltage	V_{OFFG1}	G_{VGA}=2 to 10 times	-	±80	±180	mV
D13		V_{OFFG2}	G_{VGA}=20 times	-	±80	±195	
D14	Output reference voltage range	V_{REFG}		1.0	-	4.0	V
D15	Output dynamic range	V_{OG}		1.0	-	4.0	
D16	Input dynamic range	V_{IG1}	G_{VGA}=2 times	-0.3	-	1.5	
		V_{IG2}	G_{VGA}=3 times	-0.3	-	1.0	
		V_{IG3}	G_{VGA}=4 times	-0.3	-	0.75	
		V_{IG4}	G_{VGA}=5 times	-0.3	-	0.6	
		V_{IG5}	G_{VGA}=6 times	-0.3	-	0.5	
		V_{IG6}	G_{VGA}=8 times	-0.3	-	0.375	
		V_{IG7}	G_{VGA}=10 times	-0.3	-	0.3	
		V_{IG8}	G_{VGA}=20 times	-0.3	-	0.15	
D17	Power supply current during operation	I_G	G_{VGA}=10 times, V_{INP}=V_{INN}=0.0 V	-	2.6	-	mA/ Unit

VGA0, VGA1, VGA2, VGA3 (When used in OPA mode)				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D18	Input offset voltage	V_{IOFF}		T.B.D	-	T.B.D	mV
D19	Output dynamic range	V_{OG}		1.0	-	4.0	V
D20	Input dynamic range	V_{I9}		-0.3	-	5	
D21	Power supply current during operation	I_G		-	1.5	-	mA/ Unit

1.6.4.3 Comparator

CMP0, CMP1, CMP2, CMP3				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D22	Input offset voltage	V_{OFFC}		-	-	±20	mV
D23	Input dynamic range	V_{IC}		50	-	4950	
D24	Input hysteresis width	V_{HYSC}	Reference voltage = 2.5 V	-	30	50	
D25	Minimum comparison voltage	V_{MINC}		20	-	-	
D26	Power supply current during operation	I_C		-	0.3	-	mA/ Unit

1.6.4.4 D/A Converter

8-bit D/A Converter DACI0, DACI1, DACI2, DACI3, DACV0, DACV1, DACV2, DACV3				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D27	Resolution			-	-	8	Bits
D28	Integral non-linearity error	$INLE_{DA1}$		-	-	±1	LSB
D29	Differential linearity error	$DNLE_{DA1}$		-	-	±1	
D30	Zero scale voltage	-		-20	-	20	mV
D31	Full scale voltage	-		4960	-	5020	
D32	Power supply current during operation	I_{DA1}		-	0.5	-	mA/ Unit

10-bit D/A Converter DACP0, DACP1				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D33	Resolution			-	-	10	Bits
D34	Integral non-linearity error	$INLE_{DA2}$		-	-	±3	LSB
D35	Differential linearity error	$DNLE_{DA2}$		-	-	±3	
D36	Zero scale voltage	-		-20	-	20	mV
D37	Full scale voltage	-		4980	-	5035	
D38	Power supply current during operation	I_{DA2}		-	0.5	-	mA/ Unit

1.6.4.5 Power Supply Voltage Detection (LVD)

				V_{SS} = 0.0 V Tc= -40 °C to110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D39	Power supply voltage detection level	V_{LVDP}	At rising	4.0	4.2	4.4	V
D40		V_{LVDN}	At falling	3.9	4.1	4.3	
D41	Change rate of power supply voltage	ΔV_{DD5P}	At rising			5	V/ms
D42		ΔV_{DD5N}	At falling			1	

1.6.4.6 Power-On Reset

				V_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D43	Power supply voltage detection level	V_{RST5P}	At rising	2.90	2.95	3.00	V
D44		V_{RST5N}	At falling	2.80	2.85	2.90	
D45	Change rate of power supply voltage	ΔV_{DD5P}	At rising	-	-	5	V/ms
D46		ΔV_{DD5N}	At falling	-	-	1	

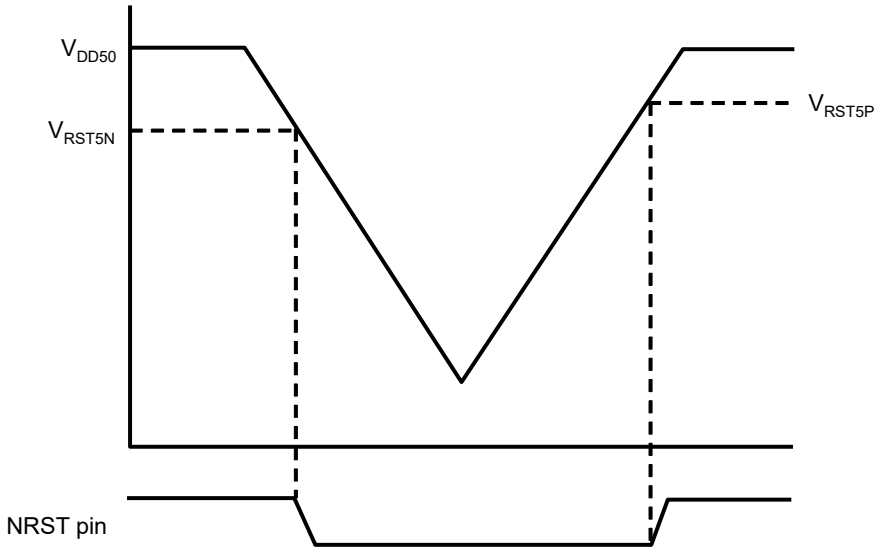


Figure 1.6-3 Characteristics of Power-On Reset Circuit

1.6.4.7 Internal Oscillation

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
			V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C				
D47	Oscillation frequency0	F_{RC0}	T_C = -20 °C to 60 °C	9.9	10	10.1	MHz
D48			T_C = -40 °C to 125 °C	9.8	10	10.2	MHz
D49	Oscillation frequency1	F_{RC1}		36	40	44	MHz

Note:

Factory calibrated, parts not soldered.

1.6.5 AC Characteristics

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
			V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C				
E1	Reset signal pulse width	t_{NRSTW}		1	-	-	µs

1.6.6 Flash EEPROM Characteristics

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
			V_{DD50}= V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C				
F1	Allowable time of rewriting: 1	E_{MAX1}	I-Flash, when the ECC function is enabled	10,000	-	-	times
F2	Allowable time of rewriting: 2	E_{MAX2}	D-Flash, when the ECC function is enabled	100,000	-	-	
F3	Data retention period 1 (*1)	T_{HLD1}	I-Flash After rewriting EMAX1 (MIN) times	20	-	-	years
F4	Data retention period 2 (*1)	T_{HLD2}	D-Flash After rewriting EMAX2 (MIN) times	5	-	-	
F5	Data retention period 3 (*1)	T_{HLD3}	D-Flash After rewriting 1,000 times	10	-	-	

Note:

*1 This includes the time when the power is off.

1.7 Package Dimension

The package dimension is shown in the following order.

- 100 pins 14mm * 14mm 0.5mm pitch Figure 1.7-1

Unit: mm

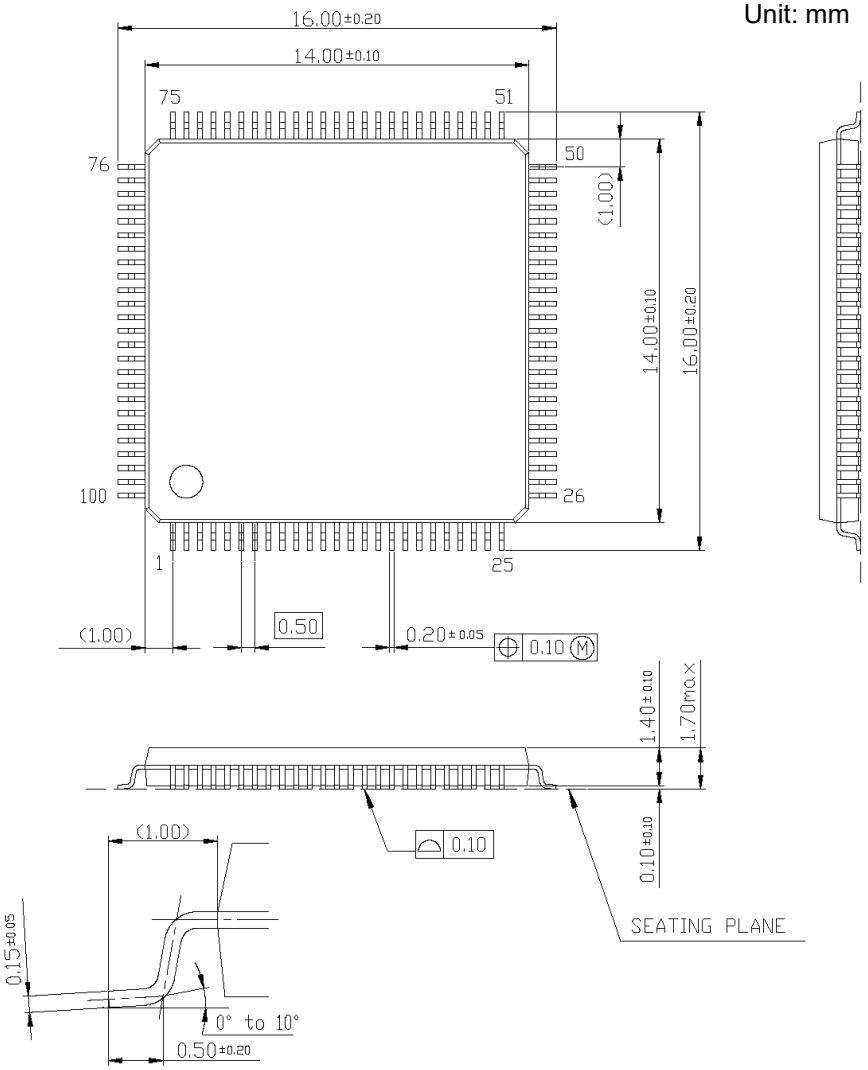


Figure 1.7-1 Package Dimension of 100 pins 14mm * 14mm 0.5mm pitch

- 80 pins 12mm * 12mm 0.5mm pitch Figure 1.7-2

Unit: mm

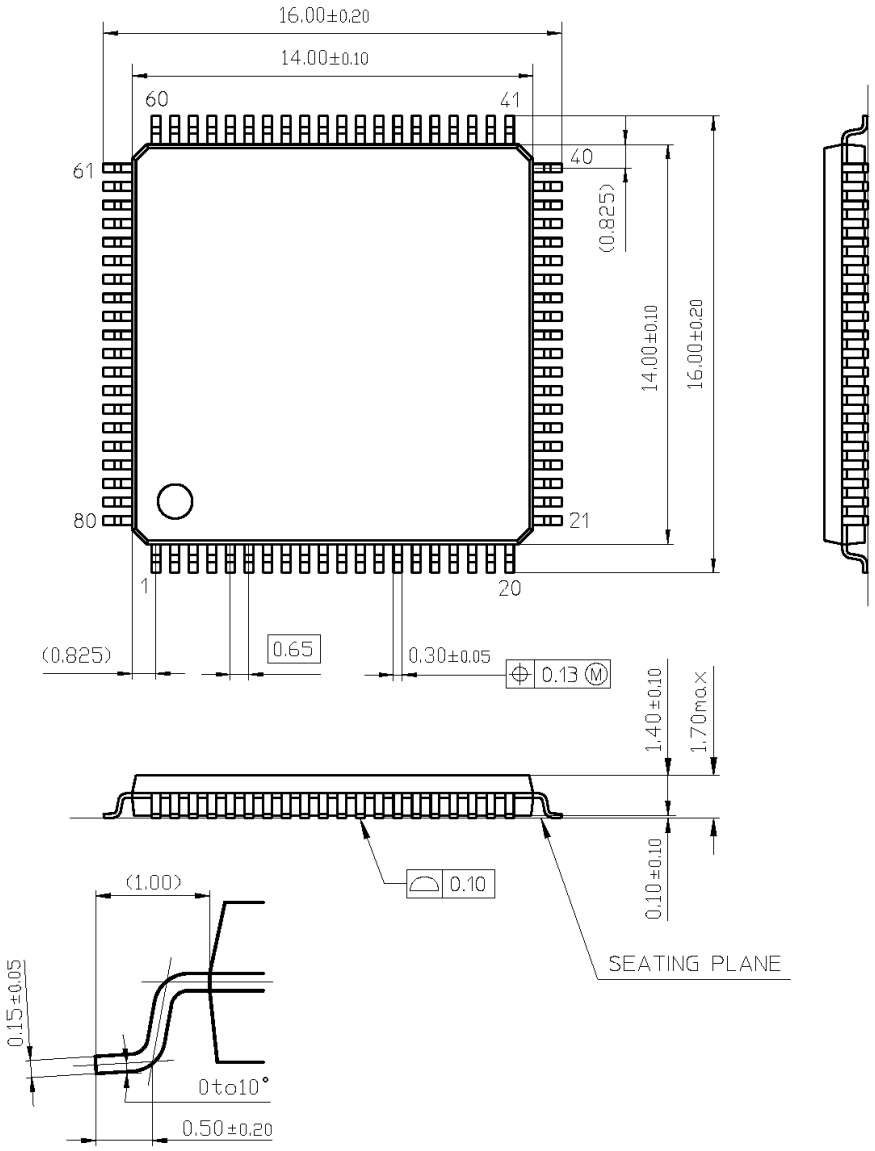
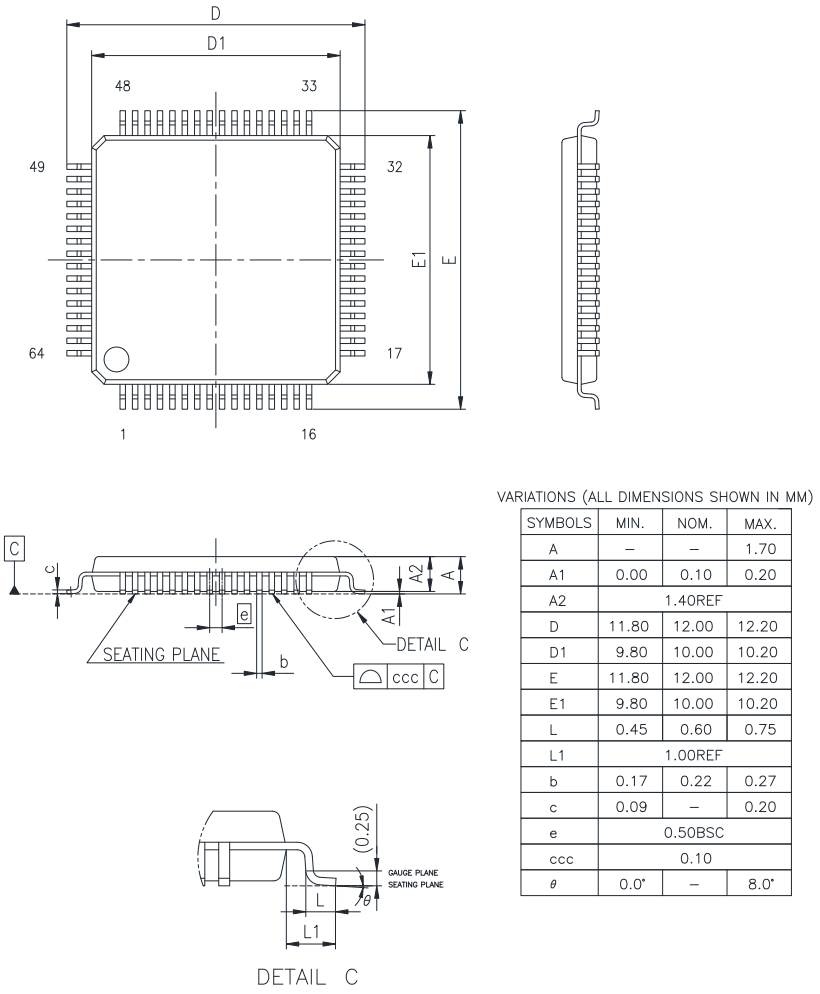


Figure 1.7-2 Package Dimension of 80 pins 12mm * 12mm 0.5mm pitch

- 64 pins 10mm * 10mm 0.5mm pitch Figure 1.7-3



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.70
A1	0.00	0.10	0.20
A2		1.40REF	
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
L	0.45	0.60	0.75
L1		1.00REF	
b	0.17	0.22	0.27
c	0.09	–	0.20
e		0.50BSC	
ccc		0.10	
θ	0.0°	–	8.0°

Figure 1.7-3 Package Dimension of 64 pins 10mm * 10mm 0.5mm pitch

Note:

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

1.8 Cautions for Circuit Setup

The cautions for circuit setup are described as follows.

- Cautions of Usage
- Pin Connections
- Unused Pin Connection
- Cautions of Power Supply
- Example of Oscillator Connection

1.8.1 Cautions of Usage

When using this LSI, obey the following cautions.

1. Operation temperature should be well considered. If the operation temperature is over the condition, improper operation can occur.
2. Operation voltage should be also well considered.

   - If the operation voltage is over the operating range, duration of the product can be shortened (e.g. the lifetime warranty of a transistor due to the change over time).

   - If the operation voltage is below the operating range, it may operate improperly.
3. If you install the product close to high electrical fields (just below the cathode ray tube, etc.), shield the package surface to ensure normal performance.

1.8.2 Pin Connections

Each pin connection is listed in Table 1.8-1 .

Table 1.8-1 Pin Connections

Pin name	Input/Output	Connection details
VDD50	Input	Connect to 5 V external power supply. Connect the bypass capacitors of 0.1 μF and the decoupling capacitor of 10 μF or more between each pin and VSS pins. (Put the capacitor near the pins)
VSS	Input	Short circuit with common GND.
VOUT12	Output	Connect the bypass capacitors of 0.1 μF and the used capacitor of 1 μF to 50 μF for stabilization between each pin and VSS pins. (Put the capacitor near the pins)
OSCI, OSCO	I/O pin	HXOCLK is generated by connecting the oscillator to OSCI and OSCO pins and starting external oscillation(HXO).
SWDCLK, SWDD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect to V_{DD50} with the resistor of 10 kΩ.
DBGIO	I/O pin	Insert a 100 Ω limit resistor between this pin and the external connector.
TRCSWO	Output	Insert a 100 Ω limit resistor between this pin and the external connector.
TEST0	Input	Pull-down connect to V_{SS} with the resistor of 2 kΩ.
NDMOD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect to V_{DD50} with the resistor of 2 kΩ.
NRST	I/O pin	Insert a 100 Ω limit resistor between this pin and the external connector. Connect the capacitor of 0.1 μF or more between each pin and VSS pins. (Put the capacitor near the pins)

Note:
Determine the processing method of each pin by evaluating enough in consideration of the effect of external noise.

Note:
VOUT12 is a pin to connect a capacity for the internal power supply stabilization.

Note:
For pins not listed in Table 1.8-1 , inserting a 100 Ω limit resistor is effetive for noise resistance.

1.8.3 Unused pins

It is recommended to use the following procedure to set unused I/O pins to general purpose port function.

First, set unused I/O pins to general purpose port function. Then, set the pins either to I/O disabled state(both input enable and output enable are OFF) or to output state(input enable is OFF and output enable is ON). After that, open the pins. The pins(only for input) which have general purpose port function are also recommended to be set like unused I/O pins. The details are shown in Figure 1.8-1 and Table 1.8-2 .

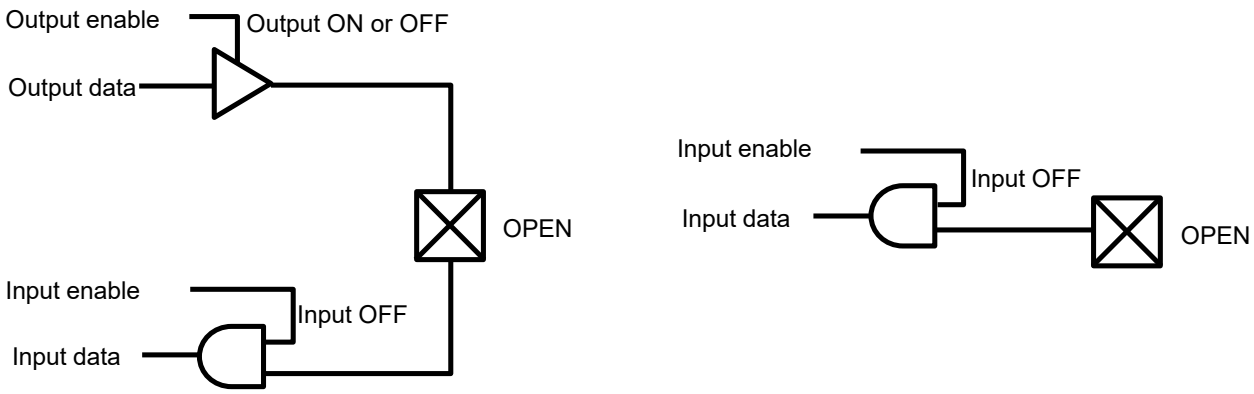


Figure 1.8-1 Unused I/O Pins

Table 1.8-2 Recommended Method of Unused I/O Pins

Pin	Input/ Output	Recommended method of unused pins
PE2	Input	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Connect the resistor for pull-down in VSS in the state of input with port control. - Connect the resistor for pull-up in VDD5 in the state of input with port control.
Other I/O pin	I/O pin	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Set pins to open in the state of "High-level" Output or "Low-level" Output with port control. - Connect the resistor for pull-down in VSS in the state of input with port control. - Connect the resistor for pull-up in VDD5 in the state of input with port control.

Note:

Determine how to process each pin by evaluating enough in consideration of the effect of external noise.

1.8.4 Cautions of Power Supply

The cautions of power supply are described as follows.

- Relations between Power Supply and Input Pin Voltage
- Restriction in Power-on
- Power Supply Circuit for LSI

1.8.4.1 Relations between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed, a latch up occurs inside of the LSI and the destruction of the LSI by a large current flow can occur.

Relations between power supply and input pin voltage are shown in Figure 1.8-2 .

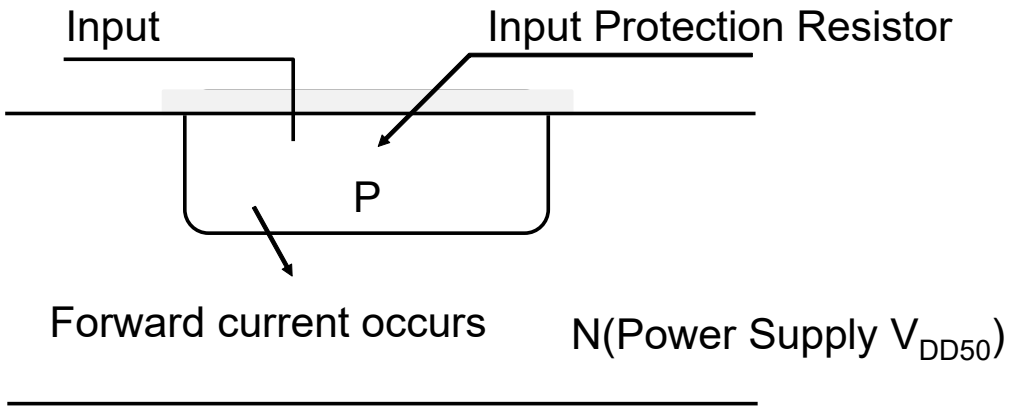


Figure 1.8-2 Relations between Power Supply and Input Pin Voltage

1.8.4.2 Restriction in Power-on

This LSI generates reset when power is applied by Power-On Reset and operates with the internal power supply generated by internal regulator. Therefore, design the circuit board so that the relations of NRST voltage, power supply voltage(VDD50), and internal power supply voltage(VOUT12) will comply with the following conditions.

- $\Delta V_{DD50P} \leq 5$ V/ms
- $t_{VOUT12} < t_{VRST}$
- $t_{NRSTW} \geq 1$ µs

ΔV_{DD50P} : The change rate of power supply voltage VDD50

t_{VOUT12} : The time when power supply voltage reaches 1.08 V

t_{VRST} : The time when power supply voltage reaches the lower limit of power supply voltage level (V_{RST5P})

t_{NRSTW} : The time that NRST pin maintains "L" level

Figure 1.8-3 shows the relations between power supply voltage and NRST voltage.

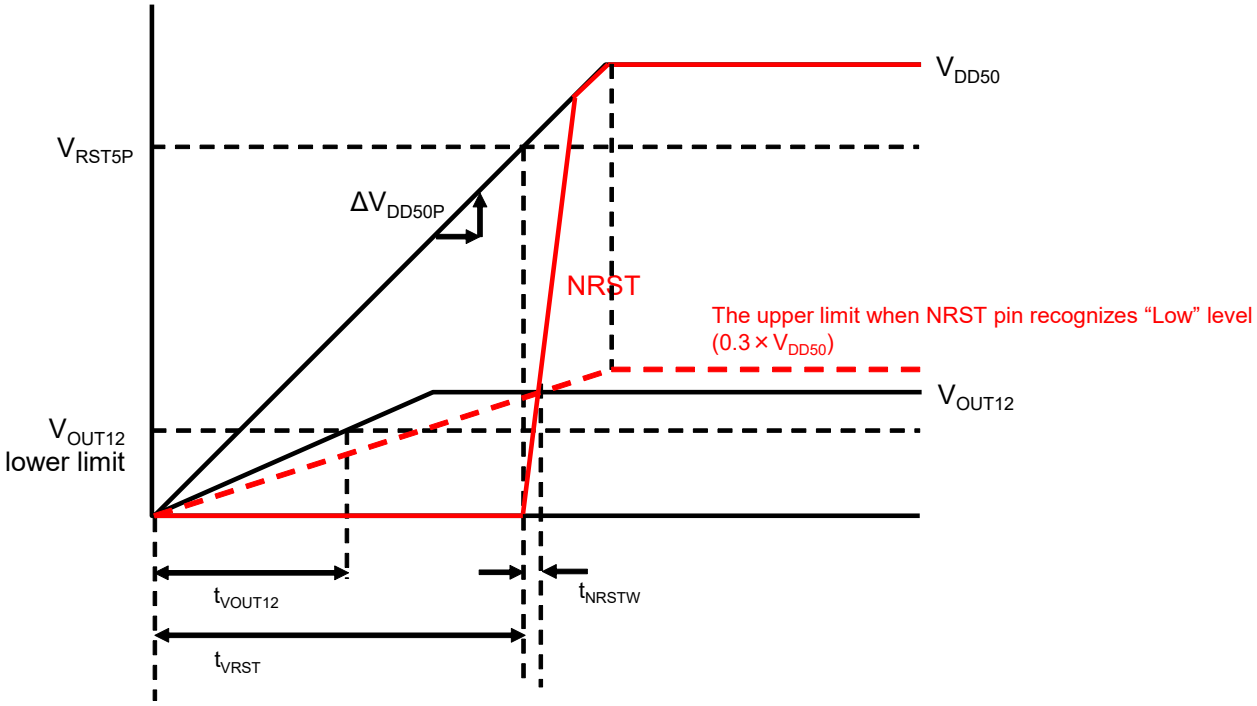


Figure 1.8-3 The Relations between LSI Power Supply and Reset Input Voltage

1.8.4.3 Power Supply Circuit for LSI

The power supply circuit should be designed with a sufficient margin, after checking AC line noise evaluation, and confirming the ripple when driving an LED and considering the power supply system.

Figure 1.8-4 shows an example for a power supply circuit. (Emitter follower type).

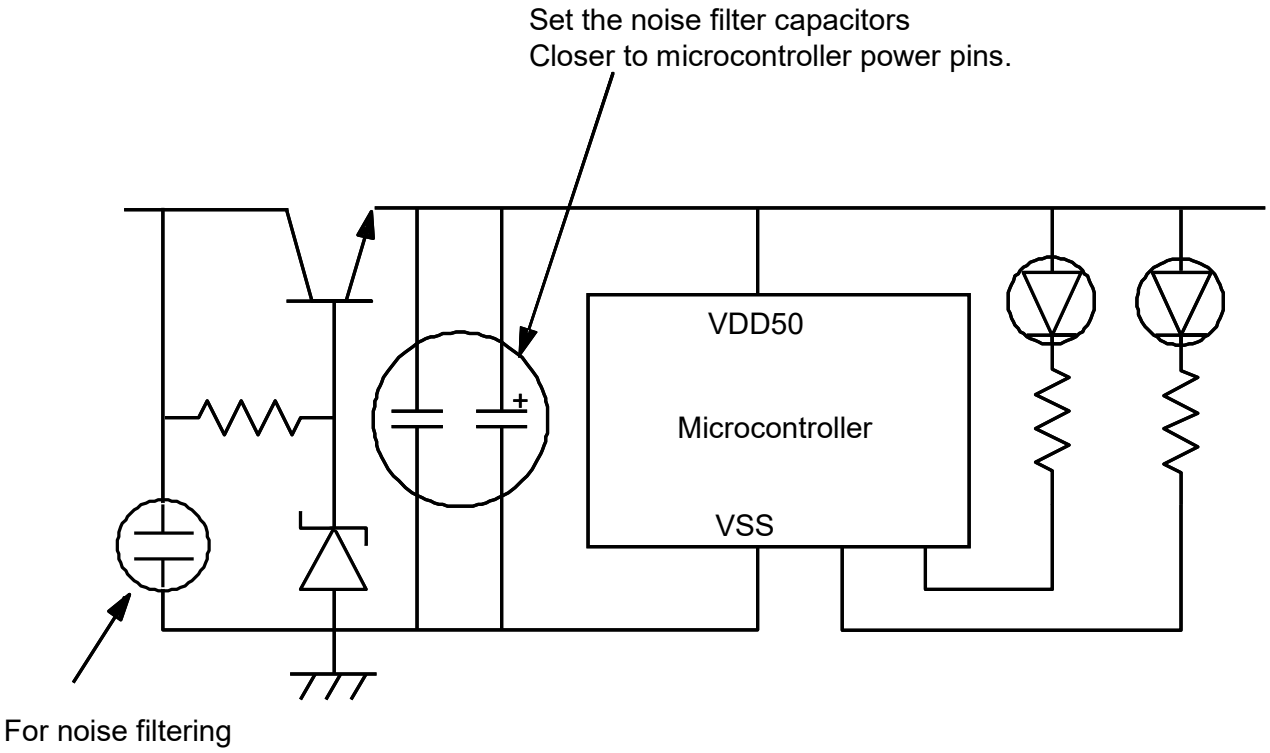


Figure 1.8-4 Power Supply Circuit Example(Emitter Follower Type)

1.8.5 Example of Oscillator Connection

Figure 1.8-5 shows the example of oscillator connection, and Table 1.8-3 shows recommended oscillators and the circuit constants.

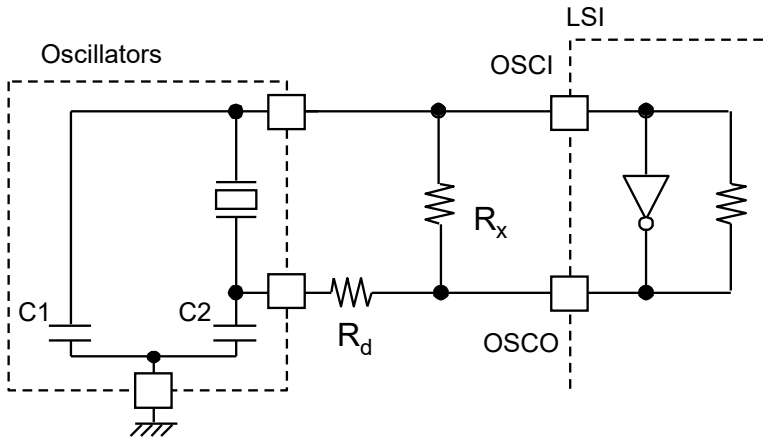


Figure 1.8-5 Example of Oscillator Connection

Table 1.8-3 Recommended Oscillators and The Circuit Constants

Oscillator maker	Frequency [MHz]	Type	Oscillator Product Number	Recommended circuit constant		
				Load capacity C1 = C2 [pF]	External feedback resistor R_X [Ω]	Dumping resistor R_d [Ω]
Murata	20	SMD	CSTNE20M0V530000R0	15	Open	150
		Lead	CSTLS20M0X53-B0	15	Open	0
	16	SMD	CSTNE16M0V530000R0	15	Open	150
		Lead	CSTLS16M0X53-B0	15	Open	0
	10	SMD	CSTNE10M0G550000R0	33	Open	220
		Lead	CSTLS10M0G56-B0	47	Open	220
	8	SMD	CSTNE8M00G550000R0	33	Open	330
		Lead	CSTLS8M00G56-B0	47	Open	330
	4	SMD	CSTCR4M00G55-R0	39	Open	330
		Lead	CSTLS4M00G56-B0	47	Open	330
Kyocera	20	Quartz Crystal Unit	CX3225CA	8	Open	1000
	16				Open	1500
	12				Open	1000
	10		CX5032GA	10	Open	0
	8			12	Open	330
	4		CX8045GA	20	Open	470

The recommended values above are based on the evaluation result of oscillator for a single unit of this LSI.

Note:

Consult the oscillator maker for the appropriate circuit constant because circuit constant of each oscillator, which is connected to OSCI/OSCO, depends on stray capacitance of the oscillator or on the mounting circuit.

Inquiries

If you have questions regarding technical information on this manual, please visit the following URL.

Nuvoton Technology Corporation Japan

URL: https://www.nuvoton.co.jp/en/contact/

- Microcomputer Home Page
  https://www.nuvoton.co.jp/en/products/

KM1M4BF22/23/24 Series
Datasheet

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