Arm® Cortex®-M
32-bit Microcontroller

KM1M4BF64/65/66/67 Series

Datasheet

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1. Overview

1.1 Overview

This LSI is a 32-bit microcontroller with internal Flash memory. It is intended for development of the C programming language with object-oriented program and is easy to use. It has fast feedback processing required for control of motor.

This LSI adopts the Arm Cortex-M4F to the 32-bit microcontroller part and are equipped with internal memory to instruction / data, DMA controller, clock generator, bus controller, interrupt controller, standard peripheral circuits (timer and serial interface and so on), PWM control circuit specialized for motor control, and high accuracy / high speed analog circuit.

As system safety design, this LSI has the various safety mechanisms (Memory-ECC, clock error detection, power supply voltage detection, window watchdog timer, etc.).

1.2 Product Summary

The LSI shown in Table Table 1.2-1 is described in this manual.

Table 1.2-1 Product Summary

LSI series	LSI product name	Pins	ROM [KB]		RAM [KB]	Package
			Instruction	Data	Data	
KM1M4BF6 series	KM1M4BF64G	64	136	8	16	10 mm x 10 mm 0.5 mm pitch
	KM1M4BF65G	48				7 mm x 7 mm 0.5 mm pitch
	KM1M4BF66G	44				10 mm x 10 mm 0.8 mm pitch
	KM1M4BF67G	32				7 mm x 7 mm 0.8 mm pitch

Hint:

In this manual, the product names are classified as follows.

KM1M4BFxyz (x = 6 y = 4,5,6,7 z = G)

1.2.1 Function Summary

Table 1.2-2 shows the functions of each product.

Table 1.2-2 The List of Function

Function		64 pins	48 pins	44 pins	32 pins
CPU		Arm Cortex-M4F			
General purpose pin		50	36	32	20
Operation mode	Active mode	NORMAL			
	Standby mode	SLEEP, DEEPSLEEP			
Debugger I/F	Interface	SWD			
DMA	CH number	8			
Interrupt	External interrupt	20	15	14	8
Timer	16-bit timer (timer 0 to 11)	12			
	Power control PWM (GPWM0 to 5)	6		4	
Noise filter	Target pin	External interrupt, Timer input			
Communication I/F	Clock synchronous/ SPI/UART/IIC (serial 0 to 5)	6			3
12-bit A/D	AD0 CH number	13	11	10	6
	AD1 CH number	13	11	10	6
	Total CH number	13	11	10	6
Programmable gain amplifier(VGA)	Module number/CH number	1/3			
Comparator	Module number/CH number	1/1			
8-bit D/A	Module number	2			
10-bit D/A	CH number	1			
Safety function	Flash memory	ECC, Data protection			
	RAM	ECC			
	Access area	MPU (Area management, Protection), Register protect (Protection)			
	System	Window watchdog timer			
	Clock	Clock monitoring (External oscillation, PLL error detection)			
	Communication	CRC calculation function			
	A/D converter	A/D converter error detection			
	Power supply voltage	POR, Power supply voltage detection			
	Reset	Detection of reset factor immediately before by reset factor register			

1.3 Features

The features of this LSI are described.

Functions	Features
CPU	- Arm Cortex-M4F Equipped with FPU: Single precision floating point unit, IEEE754 compliant Equipped with MPU: Memory protect unit, 8 area can be set
Memory	- ROM access I-FLASH: 120 MHz 2 wait access(Min), selectable from 2 to 7 D-FLASH: 120 MHz 5 wait access(Min), selectable from 2 to 7 - RAM access 120 MHz 0 wait access - Swap Function I-Flash: Supports swap function of Boot area and Program area
Clock	- HXOCLK (External oscillation) frequency: 4 to 20 MHz - HRCCLK (Internal high-speed oscillation) frequency : 10 MHz±5% - PLLCLK PLL Input: External high-speed oscillation PLL Input frequency: 4 MHz to 20 MHz PLL Output frequency: 120 MHz to 240 MHz - BASECLK Selectable from HRCCLK/HXOCLK/PLLCLK Start with Internal high-speed oscillation when reset is released Switchable to HRCCLK when a clock error is detected - CPUCLK 1 to 8 dividing of BASECLK - IOCLK 2 to 16 dividing of CPUCLK Clock operation/stop can be selected for each peripheral module
Reset	- Hardware reset Power-On Reset - System Reset Reset by external pin(NRST) Reset by register setting Reset by error detection(WDT overflow, Clock error detection) - CPU Generation Reset Reset by writing to AIRCR - Reset factor can be monitored
Low power consumption	- SLEEP mode: Stop CPU clock only - DEEP SLEEP mode: Stop clocks including BASECLK
Interrupt	- Interrupt level: 16 levels - External interrupt: High/Low level, Rising/Falling/Both edge
DMA	- Transfer mode: Single word transfer mode, Burst transfer mode - Transfer unit: 8 bits/16 bits/32 bits - Maximum transfer count: 65535 words - Transfer factor: External interrupt, Peripheral module factor - Register reload count: Maximum 65535 times - Interrupt: DMA completion, reload count completion, bus error, transfer request overflow, invalid DMA transfer request
Noise filter	- Sampling type noise filter is inserted to external interrupt and timer input. - Select sampling clock

Functions	Features
16-bit timer	- Interval timer count, Event count, Up-down pulse count, Phase difference pulse count - Timer Output, PWM, 1-shot Output - Input capture by external input - Timer count start by start trigger - A/D conversion start trigger Output - 32-bit cascade connection - Output protection: H/L/Hi-z Output can be selected - Timer interrupt Output control
Power control PWM	- Complementary PWM Output (Wave mode: Triangular and saw-tooth waves) - Dead time insert, Output shift, H/L level Output can be set - Synchronous A/D conversion trigger - Interrupt Output control - Output protection: H/L/Hi-z Output can be select - Duty cut, period cut - Double buffer update
Synchronous SIF/SPI	- 2-wire/3-wire/4-wire - Transfer bits(2 bits to 8 bits) - MSB/LSB transfer - Clock polarity selection - Continuous communication - Output level after the final bit transmission(H/L/final data) - Maximum transfer rate: 10 Mbps (at master) / 5 Mbps (at slave)
UART	- 1-wire/2-wire - Character bits(5-bits to 8-bits) - Stop bits(1-bit/2-bit) - Parity bit: Enabled/Disabled, Parity bit type: 0/1/Even parity/Odd parity - MSB/LSB transfer - Maximum transfer rate: 3.3 Mbps
IIC	- Master/Slave communication - Start condition selection: Enable/Disable - MSB/LSB transfer selection - Transfer format: 7-bit address format, 10-bit address format - Maximum transfer rate: Standard Mode: 100 kbps, Fast Mode: 400 kbps
12-bit A/D	- Timer 0 to 11, GPWM0 to 5 etc can be started synchronously - Conversion error detection - Conversion state Output - Start trigger reduction function
VGA	- Gain selection(2, 3, 4, 5, 6, 8, 10, 20 times) - Set Output reference voltage by 8-bit DAC
Comparator	- Hysteresis ON/OFF - Set reference voltage by 8-bit DAC - Sampling type noise filter is inserted to comparator Output
8-bit D/A	- VGA Output reference voltage can be generated - Comparator reference voltage can be generated
10-bit D/A	- Output the set DC voltage
Multi feedback assist	- Set the start timing of GPWM 0 to 5 individually - Detect/Automatically avoid the competition of GPWM 0 to 5 and AD conversion start - Mask(Blanking) the external interrupt detection, comparator of GPWM 0 to 5 Output
CRC calculation	- CRC-32/MPEG2, CRC-16-CCITT, CRC-16-IBM, CRC-8-ATM symbol can be generated

Functions	Features
Safety function	- ECC function Check area: I-FLASH, D-FLASH, RAM 2 bit random error detection - Flash Erase/Program protect function - Function to protect write access to main register - Clock monitor function - Window watchdog timer(internal oscillation count) - Power supply voltage detection - ADC fault diagnosis function which is used for internal power supply

1.4 Pins

The specifications of pins in this LSI are described as follows.

- Pin configuration
- Pin function

1.4.1 Pin Configuration (KM1M4BF6 Series)

Figure 1.4-1 shows the pin configuration of 64 pins.

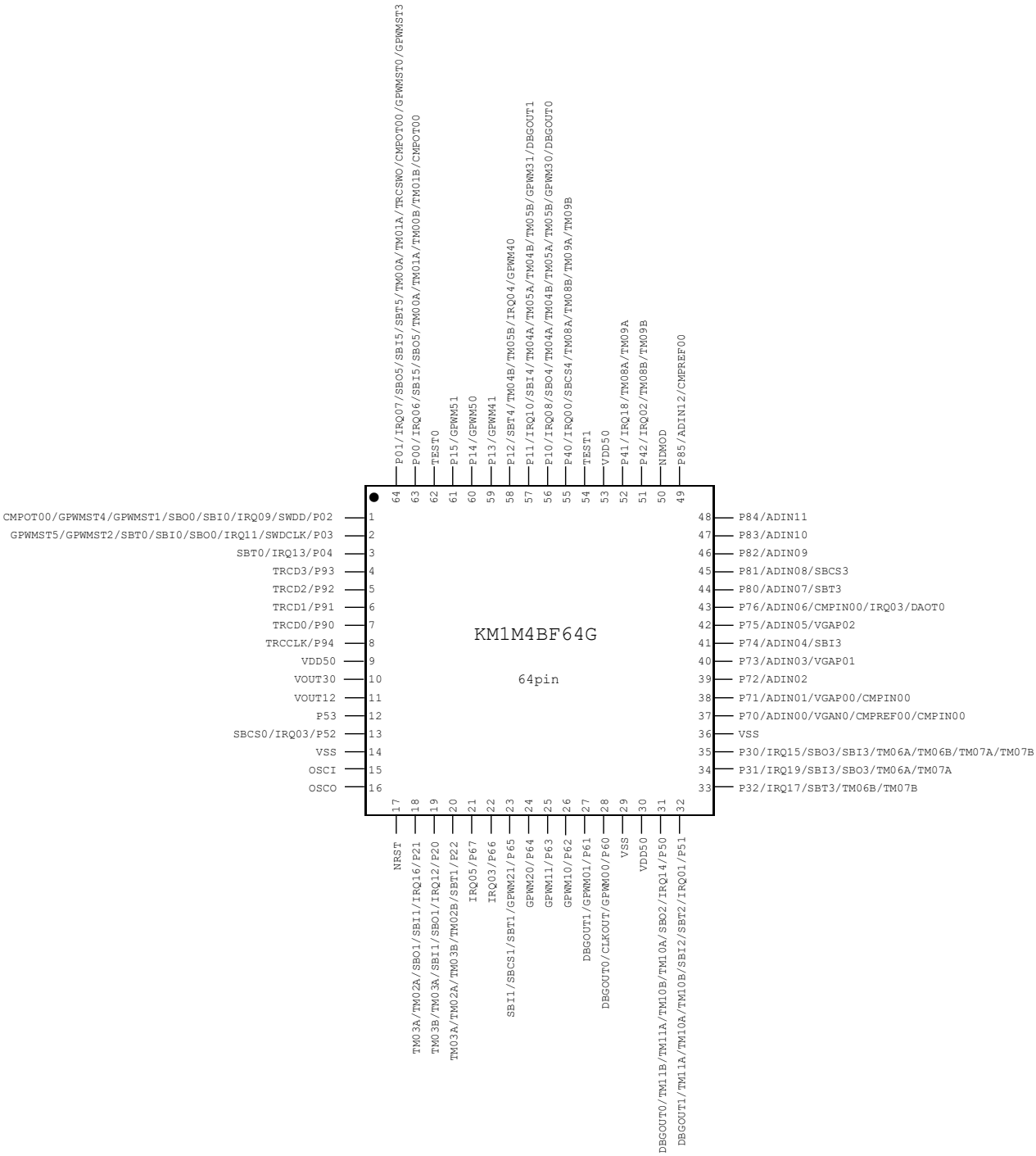


Figure 1.4-1 Pin Configuration Figure of 64 pins (KM1M4BF64G)

Figure 1.4-2 shows the pin configuration of 48 pins.

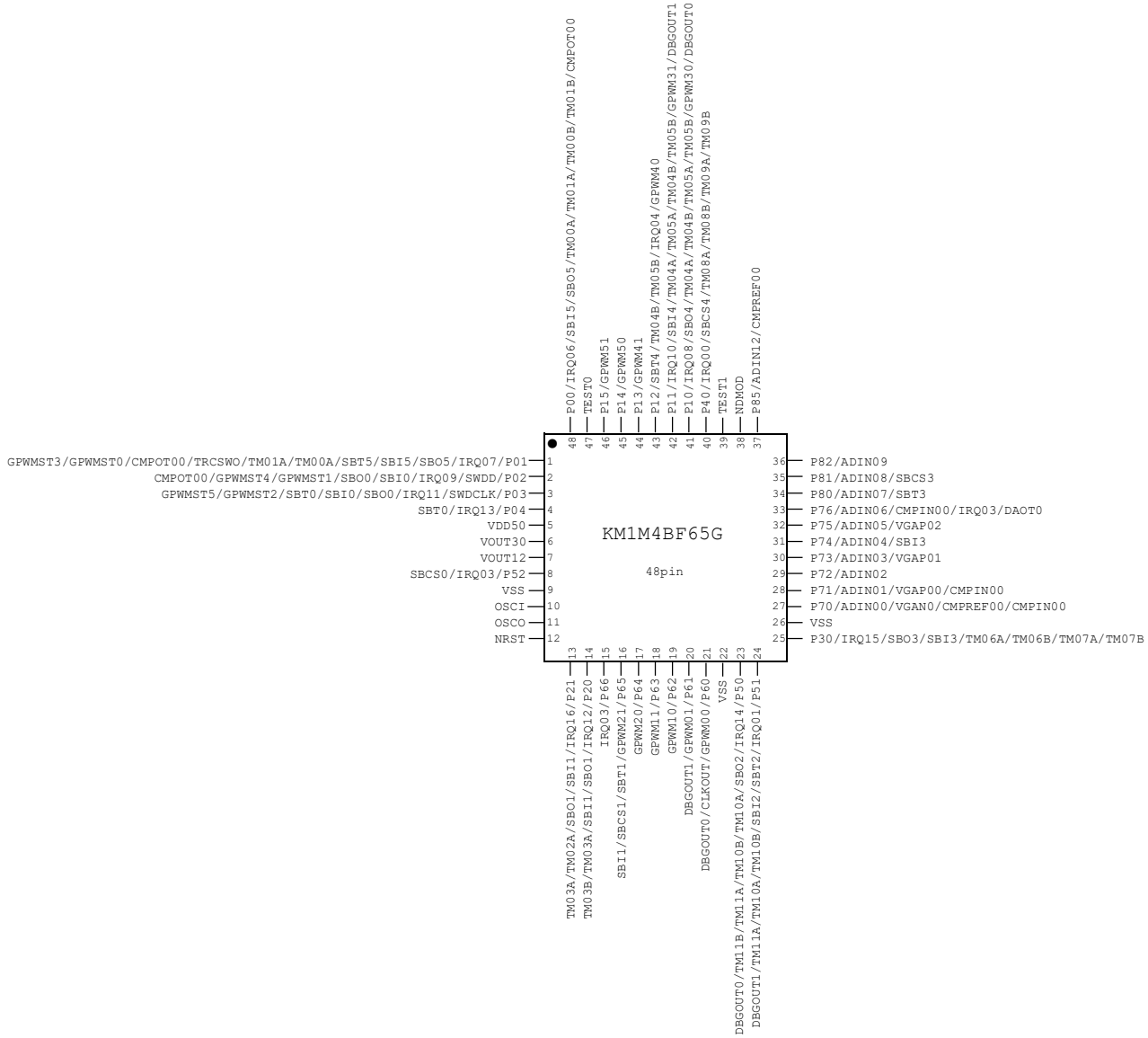


Figure 1.4-2 Pin Configuration Figure of 48 pins (KM1M4BF65G)

Figure 1.4-3 shows the pin configuration of 44 pins.

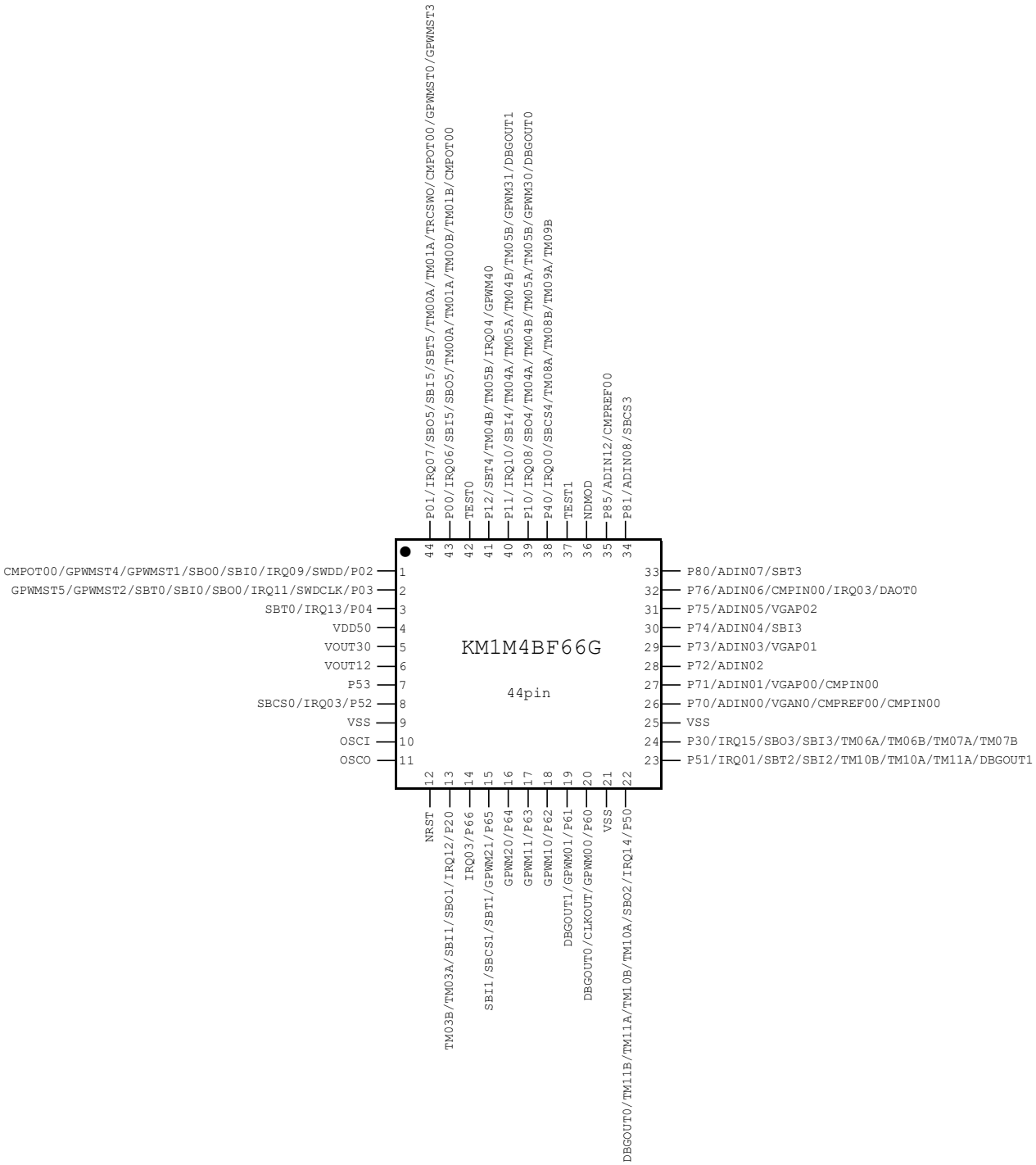


Figure 1.4-3 Pin Configuration Figure of 44 pins (KM1M4BF66G)

Figure 1.4-4 shows the pin configuration of 32 pins.

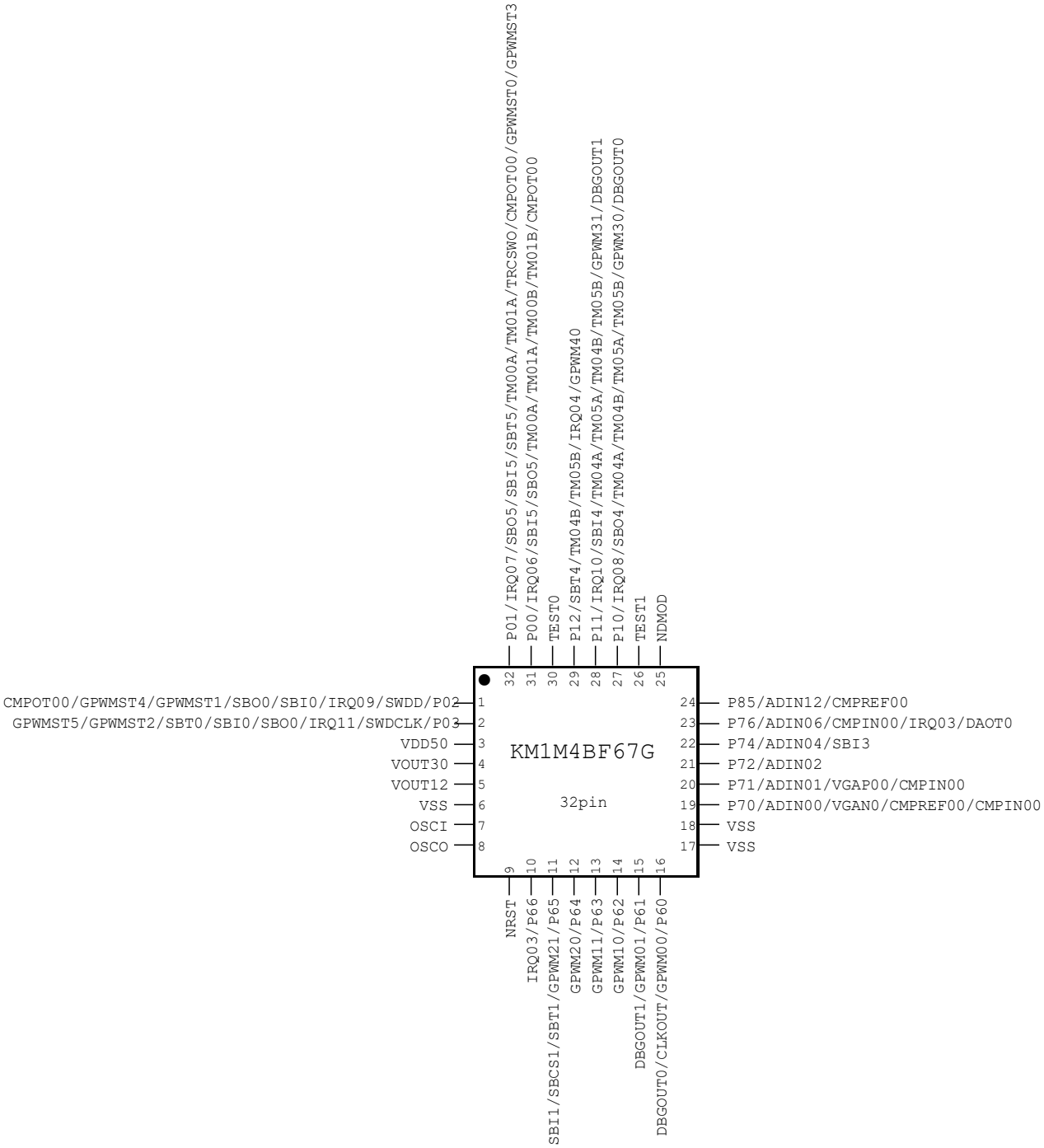


Figure 1.4-4 Pin Configuration Figure of 32 pins (KM1M4BF67G)

1.4.2 Pin Functions (KM1M4BF6 Series)

The pin functions are listed in Table 1.4-1 and Table 1.4-2 .

Table 1.4-1 Pin Functions (for each pin)

64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
1	2	1	1		P02	GPWMST1, GPWMST4	SBI0, SBO0	SWDD, IRQ09, CMPOT00
2	3	2	2		P03	GPWMST2, GPWMST5	SBO0, SBI0, SBT0	SWDCLK, IRQ11
3	4	3	-		P04		SBT0	IRQ13
4	-	-	-		P93			TRCD3
5	-	-	-		P92			TRCD2
6	-	-	-		P91			TRCD1
7	-	-	-		P90			TRCD0
8	-	-	-		P94			TRCCLK
9	5	4	3	VDD50				
10	6	5	4	VOUT30				
11	7	6	5	VOUT12				
12	-	7	-		P53			
13	8	8	-		P52		SBCS0	IRQ03
14	9	9	6	VSS				
15	10	10	7	OSCI				
16	11	11	8	OSCO				
17	12	12	9	NRST				
18	13	-	-		P21	TM02A, TM03A	SBI1(*), SBO1	IRQ16
19	14	13	-		P20	TM03A, TM03B	SBO1, SBI1(*)	IRQ12
20	-	-	-		P22	TM02B, TM03B, TM02A, TM03A	SBT1(*)	
21	-	-	-		P67			IRQ05
22	15	14	10	NBOOT	P66			IRQ03
23	16	15	11		P65	GPWM21	SBT1(*), SBCS1(*), SBI1(*)	
24	17	16	12		P64	GPWM20		
25	18	17	13		P63	GPWM11		
26	19	18	14		P62	GPWM10		
27	20	19	15		P61	GPWM01		DBGOUT1
28	21	20	16		P60	GPWM00		CLKOUT, DBGOUT0
29	22	21	17	VSS				

64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
30	-	-	-	VDD50				
31	23	22	-		P50	TM10A, TM10B, TM11A, TM11B	SBO2	IRQ14, DBGOUT0
32	24	23	-		P51	TM10B, TM10A, TM11A	SBT2, SBI2	IRQ01, DBGOUT1
33	-	-	-		P32	TM06B, TM07B	SBT3	IRQ17
34	-	-	-		P31	TM06A, TM07A	SBI3(*), SBO3	IRQ19
35	25	24	-		P30	TM06A, TM06B, TM07A, TM07B	SBO3, SBI3(*)	IRQ15
36	26	25	18	VSS				
37	27	26	19		P70			ADIN00, VGAN0, CMPREF00, CMPIN00
38	28	27	20		P71			ADIN01, VGAP00, CMPIN00
39	29	28	21		P72			ADIN02
40	30	29	-		P73			ADIN03, VGAP01
41	31	30	22		P74		SBI3(*)	ADIN04
42	32	31	-		P75			ADIN05, VGAP02
43	33	32	23		P76			ADIN06, CMPIN00, IRQ03, DAOT0
44	34	33	-		P80		SBT3	ADIN07
45	35	34	-		P81		SBCS3	ADIN08
46	36	-	-		P82			ADIN09
47	-	-	-		P83			ADIN10
48	-	-	-		P84			ADIN11
49	37	35	24		P85			ADIN12, CMPREF00
50	38	36	25	NDMOD				
51	-	-	-		P42	TM08B, TM09B		IRQ02
52	-	-	-		P41	TM08A, TM09A		IRQ18
53	-	-	-	VDD50				
54	39	37	26	TEST1				

64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	Power, Clock, System	Port	Timer	Communica-tion	Other
55	40	38	-		P40	TM08A, TM08B, TM09A, TM09B	SBCS4	IRQ00
56	41	39	27		P10	TM04A, TM04B, TM05A, TM05B, GPWM30	SBO4	IRQ08, DBGOUT0
57	42	40	28		P11	TM04A, TM05A, TM04B, TM05B, GPWM31	SBI4	IRQ10, DBGOUT1
58	43	41	29		P12	TM04B, TM05B, GPWM40	SBT4	IRQ04
59	44	-	-		P13	GPWM41		
60	45	-	-		P14	GPWM50		
61	46	-	-		P15	GPWM51		
62	47	42	30	TEST0				
63	48	43	31		P00	TM00A, TM01A, TM00B, TM01B	SBI5, SBO5	IRQ06, CMPOT00
64	1	44	32		P01	TM00A, TM01A, GPWMST0, GPWMST3	SBO5, SBI5, SBT5	IRQ07, TRCSWO, CMPOT00

Note:

* Only 64pins, 48pins and 44pins are included

Table 1.4-2 Pin Functions (for each function)

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
External power pin	VDD50	9, 30, 53	5	4	3	Input
Power pin for internal circuit	VOUT30	10	6	5	4	Output
	VOUT12	11	7	6	5	Output
GND	VSS	14, 29, 36	9, 22, 26	9, 21, 25	6, 17, 18	Input
Internal clock output	CLKOUT	28	21	20	16	Output
Debug outputs	DBGOUT0	28, 31, 56	21, 23, 41	20, 22, 39	16, 27	Output
	DBGOUT1	27, 32, 57	20, 24, 42	19, 23, 40	15, 28	Output
Debugger	SWDCLK	2	3	2	2	Input
	SWDD	1	2	1	1	I/O
	TRCCLK	8	-	-	-	Output
	TRCSWO	64	1	44	32	Output
	TRCD0	7	-	-	-	Output
	TRCD1	6	-	-	-	Output
	TRCD2	5	-	-	-	Output
	TRCD3	4	-	-	-	Output
External oscillation	OSCI	15	10	10	7	Input
	OSCO	16	11	11	8	Output
Reset	NRST	17	12	12	9	Input
Mode pin	NBOOT(P66)	22	15	14	10	Input
	NDMOD	50	38	36	25	Input
	TEST0	62	47	42	30	Input
	TEST1	54	39	37	26	Input

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
External interrupt	IRQ00	55	40	38	-	Input
	IRQ01	32	24	23	-	Input
	IRQ02	51	-	-	-	Input
	IRQ03	13, 22, 43	8, 15, 33	8, 14, 32	10, 23	Input
	IRQ04	58	43	41	29	Input
	IRQ05	21	-	-	-	Input
	IRQ06	63	48	43	31	Input
	IRQ07	64	1	44	32	Input
	IRQ08	56	41	39	27	Input
	IRQ09	1	2	1	1	Input
	IRQ10	57	42	40	28	Input
	IRQ11	2	3	2	2	Input
	IRQ12	19	14	13	-	Input
	IRQ13	3	4	3	-	Input
	IRQ14	31	23	22	-	Input
	IRQ15	35	25	24	-	Input
	IRQ16	18	13	-	-	Input
	IRQ17	33	-	-	-	Input
	IRQ18	52	-	-	-	Input
	IRQ19	34	-	-	-	Input

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
16-bit timer	TM00A	63, 64	1, 48	43, 44	31, 32	I/O
	TM00B	63	48	43	31	I/O
	TM01A	63, 64	1, 48	43, 44	31, 32	I/O
	TM01B	63	48	43	31	I/O
	TM02A	18, 20	13	-	-	I/O
	TM02B	20	-	-	-	I/O
	TM03A	18, 19, 20	13, 14	13	-	I/O
	TM03B	19, 20	14	13	-	I/O
	TM04A	56, 57	41, 42	39, 40	27, 28	I/O
	TM04B	56, 57, 58	41, 42, 43	39, 40, 41	27, 28, 29	I/O
	TM05A	56, 57	41, 42	39, 40	27, 28	I/O
	TM05B	56, 57, 58	41, 42, 43	39, 40, 41	27, 28, 29	I/O
	TM06A	34, 35	25	24	-	I/O
	TM06B	33, 35	25	24	-	I/O
	TM07A	34, 35	25	24	-	I/O
	TM07B	33, 35	25	24	-	I/O
	TM08A	52, 55	40	38	-	I/O
	TM08B	51, 55	40	38	-	I/O
	TM09A	52, 55	40	38	-	I/O
	TM09B	51, 55	40	38	-	I/O
	TM10A	31, 32	23, 24	22, 23	-	I/O
	TM10B	31, 32	23, 24	22, 23	-	I/O
	TM11A	31, 32	23, 24	22, 23	-	I/O
	TM11B	31	23	22	-	I/O
Power control PWM output	GPWM00	28	21	20	16	Output
	GPWM01	27	20	19	15	Output
	GPWM10	26	19	18	14	Output
	GPWM11	25	18	17	13	Output
	GPWM20	24	17	16	12	Output
	GPWM21	23	16	15	11	Output
	GPWM30	56	41	39	27	Output
	GPWM31	57	42	40	28	Output
	GPWM40	58	43	41	29	Output
	GPWM41	59	44	-	-	Output
	GPWM50	60	45	-	-	Output
	GPWM51	61	46	-	-	Output
Power control PWM monitor	GPWMST0	64	1	44	32	Output
	GPWMST1	1	2	1	1	Output
	GPWMST2	2	3	2	2	Output
	GPWMST3	64	1	44	32	Output
	GPWMST4	1	2	1	1	Output
	GPWMST5	2	3	2	2	Output

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
Serial interface	SBCS0	13	8	8	-	I/O
	SBI0	1, 2	2, 3	1, 2	1, 2	Input
	SBO0	1, 2	2, 3	1, 2	1, 2	I/O
	SBT0	2, 3	3, 4	2, 3	2	I/O
	SBCS1	23	16	15	11	I/O
	SBI1	18, 19, 23	13, 14, 16	13, 15	11	Input
	SBO1	18, 19	13, 14	13	-	I/O
	SBT1	20, 23	16	15	11	I/O
	SBI2	32	24	23	-	Input
	SBO2	31	23	22	-	I/O
	SBT2	32	24	23	-	I/O
	SBCS3	45	35	34	-	I/O
	SBI3	34, 35, 41	25, 31	24, 30	22	Input
	SBO3	34, 35	25	24	-	I/O
	SBT3	33, 44	34	33	-	I/O
	SBCS4	55	40	38	-	I/O
	SBI4	57	42	40	28	Input
	SBO4	56	41	39	27	I/O
	SBT4	58	43	41	29	I/O
	SBI5	63, 64	1, 48	43, 44	31, 32	Input
	SBO5	63, 64	1, 48	43, 44	31, 32	I/O
	SBT5	64	1	44	32	I/O
A/D input	ADIN00	37	27	26	19	Input
	ADIN01	38	28	27	20	Input
	ADIN02	39	29	28	21	Input
	ADIN03	40	30	29	-	Input
	ADIN04	41	31	30	22	Input
	ADIN05	42	32	31	-	Input
	ADIN06	43	33	32	23	Input
	ADIN07	44	34	33	-	Input
	ADIN08	45	35	34	-	Input
	ADIN09	46	36	-	-	Input
	ADIN10	47	-	-	-	Input
	ADIN11	48	-	-	-	Input
	ADIN12	49	37	35	24	Input
VGA input	VGAP00	38	28	27	20	Input
	VGAP01	40	30	29	-	Input
	VGAP02	42	32	31	-	Input
	VGAN0	37	27	26	19	Input
Comarator input	CMPIN00	37, 38, 43	27, 28, 33	26, 27, 32	19, 20, 23	Input
	CMPREF00	37, 49	27, 37	26, 35	19, 24	Input
Comarator output	CMPOT00	1, 63, 64	1, 2, 48	1, 43, 44	1, 31, 32	Output

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
D/A output	DAOT0	43	33	32	23	Output
I/O port	P00	63	48	43	31	I/O
	P01	64	1	44	32	I/O
	P02	1	2	1	1	I/O
	P03	2	3	2	2	I/O
	P04	3	4	3	-	I/O
	P10	56	41	39	27	I/O
	P11	57	42	40	28	I/O
	P12	58	43	41	29	I/O
	P13	59	44	-	-	I/O
	P14	60	45	-	-	I/O
	P15	61	46	-	-	I/O
	P20	19	14	13	-	I/O
	P21	18	13	-	-	I/O
	P22	20	-	-	-	I/O
	P30	35	25	24	-	I/O
	P31	34	-	-	-	I/O
	P32	33	-	-	-	I/O
	P40	55	40	38	-	I/O
	P41	52	-	-	-	I/O
	P42	51	-	-	-	I/O
	P50	31	23	22	-	I/O
	P51	32	24	23	-	I/O
	P52	13	8	8	-	I/O
	P53	12	-	7	-	I/O
	P60	28	21	20	16	I/O
	P61	27	20	19	15	I/O
	P62	26	19	18	14	I/O
	P63	25	18	17	13	I/O
	P64	24	17	16	12	I/O
	P65	23	16	15	11	I/O
	P66	22	15	14	10	Input
	P67	21	-	-	-	I/O
	P70	37	27	26	19	Input
	P71	38	28	27	20	Input
	P72	39	29	28	21	I/O
	P73	40	30	29	-	Input
	P74	41	31	30	22	I/O
	P75	42	32	31	-	Input
	P76	43	33	32	23	I/O

Functions	Pin name	64 pins Pin No.	48 pins Pin No.	44 pins Pin No.	32 pins Pin No.	I/O
I/O port	P80	44	34	33	-	I/O
	P81	45	35	34	-	I/O
	P82	46	36	-	-	I/O
	P83	47	-	-	-	I/O
	P84	48	-	-	-	I/O
	P85	49	37	35	24	I/O
	P90	7	-	-	-	I/O
	P91	6	-	-	-	I/O
	P92	5	-	-	-	I/O
	P93	4	-	-	-	I/O
	P94	8	-	-	-	I/O

Note:

For pins to which multiple functions can be assigned, set only one to be valid.

Example: For 64 pins, it is prohibited to select No.1 and No.2 as SBO0 pin at the same time.

1.5 Block Diagram

Figure 1.5-1 shows the block diagram.

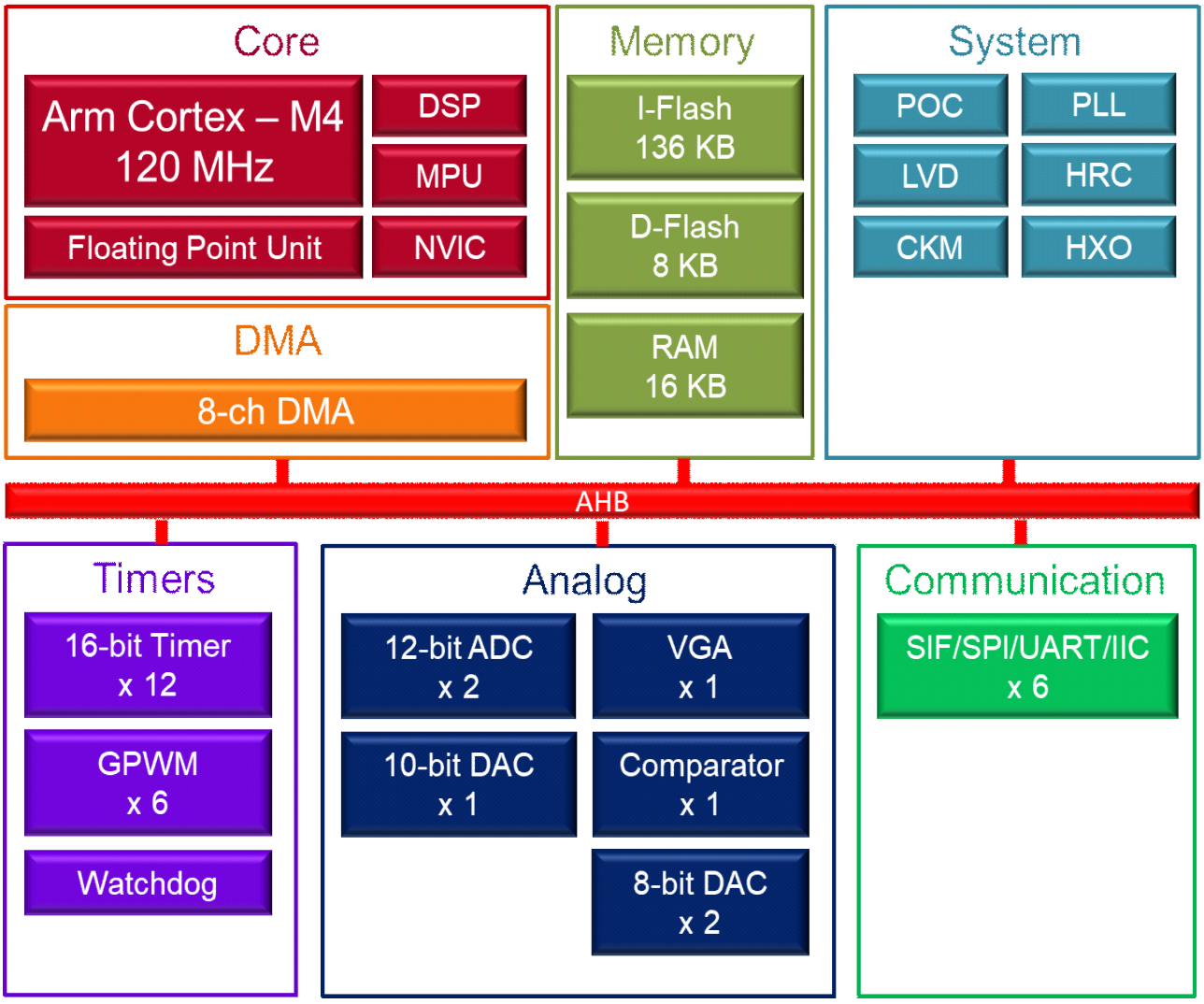


Figure 1.5-1 Block Diagram

1.6 Electrical Characteristics

About electrical specifications, standard specifications are described in the manual of this LSI. When using this LSI, consult the staff in our sales offices for the product specifications.

1.6.1 Absolute Maximum Ratings

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD50A}	-0.3 to 7.0	V
A2	Internal power supply voltage1		V_{OUT12A}	-0.3 to 1.6	V
A3	Internal power supply voltage2		V_{OUT30A}	-0.3 to 4.6	V
A4	Input pin voltage		V_{I1}	-0.3 to V_{DD50} +0.3 (Upper limit: 7.0)	V
A5	VGA input pin voltage		V_{I2}	-2.0 to V_{DD50} +0.3 (Upper limit: 7.0)	V
A6	I/O pin voltage		V_{I3}	-0.3 to V_{DD50} +0.3 (Upper limit: 7.0)	V
A7	Average Output current	I/O pin 1, 2 (*1)	I_{O1}(avg)	±12	mA
A8		I/O pin 3 (*2)	I_{O2}(avg)	±24	mA
A9		Total of all pins	I_{O3}	±70	mA
A10	Average injection current	By a I/O pin	I_{INJ1}	±2	mA
A11		By a total I/O pin	I_{INJ}	±20	mA
A12	Power dissipation		P_D	800	mW
A13	Operating case temperature		T_{copr}	-40 to +110	°C
A14	Operating junction temperature		T_j	-40 to +125	°C
A15	Storage temperature		T_{stg}	-40 to +125	°C

Note:

Although this LSI has internal ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gate.

This LSI may sustain permanent damage if it gets stress which is higher than the above stated absolute maximum rating even only for a second. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.

Note:

*1 I/O pins 1 and 2 is I/O pins 1 and 2 of 1.6.3 DC Characteristics.

Note:

*2 I/O pin 3 is I/O pin 3 of 1.6.3 DC Characteristics.

1.6.2 Operation Conditions

Power supply voltage during operation					V_{SS} = 0.0 V Tc = -40 °C to 110 °C	
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B1	External power supply voltage	V_{DD50}	V_{RST5N}	5.0	5.5	V
B2	Internal power supply voltage1	V_{OUT12}	-	1.25	-	
B3	Internal power supply voltage2	V_{OUT30}	-	2.90	-	

Oscillation pin					V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc= -40 °C to 110 °C	
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B4	External oscillation frequency (Ceramic/Crystal)	F_{OSC}	4.0	-	20.0	MHz
B5	External oscillation Feedback resistor	R_{FB}	-	1.0	-	MΩ

Note:

Oscillation circuit characteristics and peripheral parts(load capacity, damping resister, and feedback resister) are different by each oscillator and substrate. To decide appropriate capacity value for circuit constant, please consult the oscillator manufacturer.

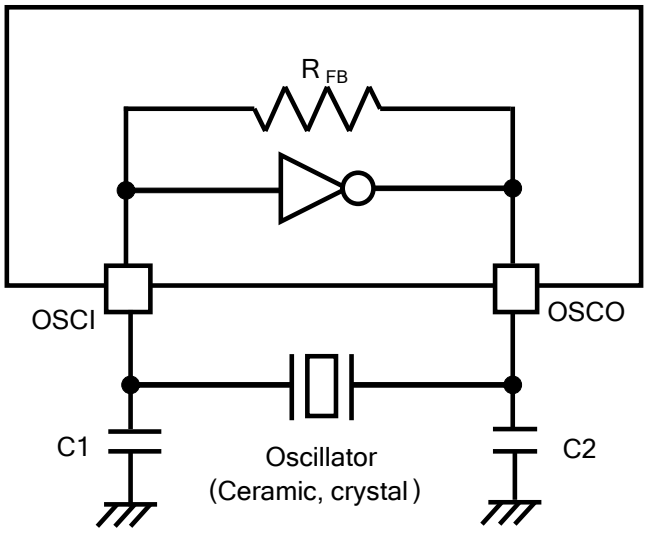


Figure 1.6-1 Oscillation Circuit

External clock input OSCI (OSCO left open)			V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Rating			Unit
			MIN	TYP	MAX	
B6	Clock frequency	F_{CP}	4.0	-	20.0	MHz
B7	High level pulse width	t_{wh1}	20	-	-	ns
B8	Low level pulse width	t_{wl1}	20	-	-	
B9	Rising time	t_{wr1}	-	-	5	
B10	Falling time	t_{wf1}	-	-	5	

Note:

It is necessary to set clock duty ratio from 45 % to 55 %.

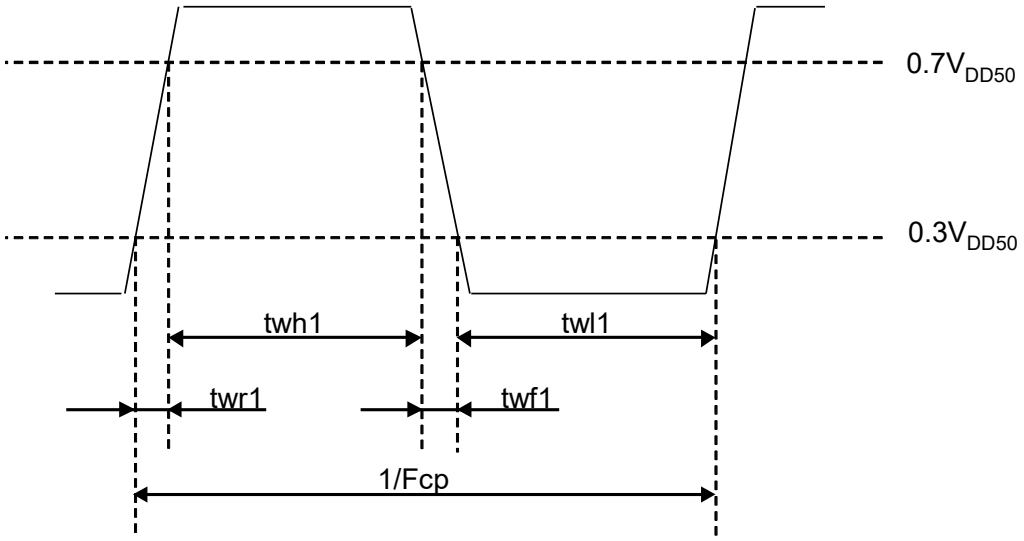


Figure 1.6-2 OSCI Timing Chart

1.6.3 DC Characteristics

Power supply current during operation				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C Output pins left open		
Parameter		Symbol	Conditions	Rating		Unit
				TYP	MAX	
C1	NORMAL mode	I_{DD1}	For the operating conditions of each function, refer to Table 1.6-1 .	35	52	mA
C2		I_{DD2}		29	-	
C3		I_{DD3}		24	-	
C4	SLEEP mode	I_{DD4}	HXOCLK = 10 MHz, PLL is used, CPUCLK = 120 MHz, IOCLK = 60 MHz CPU is stopped, Peripheral circuits are operating. Analog circuits are operating.	28	44	
C5	DEEP SLEEP mode	I_{DD5}	HXOCLK = 10 MHz, PLLCLK is stopped, CPUCLK is stopped, IOCLK is stopped, CPU and Peripheral circuits are stopped. Analog circuits are stopped.	5	16	
C6		I_{DD6}	HXOCLK, PLLCLK, CPUCLK, IOCLK is stopped	2	13	

Table 1.6-1 Conditions of NORMAL mode

Functions	I_{DD1}	I_{DD2}	I_{DD3}
CPUCLK	120MHz		80MHz
Flash	2 wait access ECC-ON	5 wait access ECC-ON	3 wait access ECC-ON
RAM	ECC-ON		
DMA	Operating		
16-bit timer	12ch operating		
Serial	6ch operating	4ch operating	
Power control PWM	6ch operating	3ch operating	
Multi feedback assist	Operating		
CRC calculation	Stopped		
Watchdog timer	Operating		
VGA	Operating		
12-bit A/D	AD0, AD1 operating		AD0 operating
10-bit D/A	Operating	Stopped	
Comparator	Operating	Stopped	

Note:

The measurement conditions are as follows.

- All I/O pins are output state. (No load)

Input pin 1 NDMOD				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C7	Input voltage "High level"	V_{IH1}		V_{DD50} × 0.7	-	V_{DD50}	V
C8	Input voltage "Low level"	V_{IL1}		V_{SS}	-	V_{DD50} × 0.3	
C9	Internal pull-up resistor	R_{IO1}	V_{IN} = 0 V	15	30	60	kΩ

Input pin 2 TEST0				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C10	Input voltage "High level"	V_{IH2}		V_{DD50} × 0.7	-	V_{DD50}	V
C11	Input voltage "Low level"	V_{IL2}		V_{SS}	-	V_{DD50} × 0.3	
C12	Internal pull-down resistor	R_{IO2}	V_{IN} = V_{DD50}	15	30	60	kΩ

Input pin 3 TEST1				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C13	Input voltage "High level"	V_{IH3}		V_{DD50} × 0.7	-	V_{DD50}	V
C14	Input voltage "Low level"	V_{IL3}		V_{SS}	-	V_{DD50} × 0.3	
C15	Input leakage current	I_{LK3}	V_{IN} = 0 V to V_{DD50}	-	-	±10	µA

Input pin 4 P66				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C16	Input voltage "High level"	V_{IH4}		V_{DD50} × 0.7	-	V_{DD50}	V
C17	Input voltage "Low level"	V_{IL4}		V_{SS}	-	V_{DD50} × 0.3	
C18	Internal pull-up resistor	R_{IO4}	V_{IN} = 0 V	15	30	60	kΩ
C19	Input leakage current	I_{LK4}	V_{IN} = 0 V to V_{DD50}	-	-	±10	µA

Input pin 5 P70, P71, P73, P75				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C20	Input voltage "High level"	V_{IH5}	VGA is not used	V_{DD50} × 0.7	-	V_{DD50}	V
C21	Input voltage "Low level"	V_{IL5}	VGA is not used	V_{SS}	-	V_{DD50} × 0.3	
C22	Input leakage current	I_{LK5}	V_{IN} = 0 V to V_{DD50}	-	-	±10	µA
C23	Input voltage range	V_{IN5}	VGA is used	-1.5	-	V_{DD50}	V

I/O pin 1 NRST				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C24	Input voltage "High level"	V_{IH6}		V_{DD50} × 0.7	-	V_{DD50}	V
C25	Input voltage "Low level"	V_{IL6}		V_{SS}	-	V_{DD50} × 0.3	
C26	Internal pull-up resistor	R_{IO6}	V_{IN} = 0 V	15	30	60	kΩ
C27	Output voltage "Low level"	V_{OL6}	V_{DD50} = V_{RST5P} I_{OL} = 3.0 mA	-	-	0.5	V

I/O pin 2 P00, P01, P03, P04, P20 to P22, P30 to P32, P40 to P42, P52, P53, P67, P72, P74, P76, P80 to P85, P90 to P94				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110°C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C28	Input voltage "High level"	V_{IH7}		V_{DD50} × 0.7	-	V_{DD50}	V
C29	Input voltage "Low level"	V_{IL7}		V_{SS}	-	V_{DD50} × 0.3	
C30	Input leakage current	I_{LK7}	V_{IN} = 0 V to V_{DD50}	-	-	±5	μA
C31	Internal pull-up resistor	R_{IO7}	V_{IN} = 0 V	15	30	60	kΩ
C32	Output voltage "High level"	V_{OH7}	I_{OH} = -3.0 mA	4.5	-	-	V
C33	Output voltage "Low level"	V_{OL7}	I_{OL} = 3.0 mA	-	-	0.5	

I/O pin 3 P02, P60 to P65, P50, P51, P10 to P15				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
C34	Input voltage "High level"	V_{IH8}		V_{DD50} × 0.7	-	V_{DD50}	V
C35	Input voltage "Low level"	V_{IL8}		V_{SS}	-	V_{DD50} × 0.3	
C36	Input leakage current	I_{LK8}	V_{IN} = 0 V to V_{DD50}	-	-	±5	μA
C37	Internal pull-up resistor	R_{IO8}	V_{IN} = 0 V	15	30	60	kΩ
C38	Output voltage "High level"	V_{OH8}	I_{OH} = -6.0 mA	4.5	-	-	V
C39	Output voltage "Low level"	V_{OL8}	I_{OL} = 6.0 mA	-	-	0.5	

1.6.4 Analog Characteristics

The electrical characteristics of analog are shown below.

1.6.4.1 12-bit A/D Converter

ADC0, ADC1				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution	-		-	-	12	Bits
D2	Conversion clock	-		10	-	40	MHz
D3	Integral non-linearity error	$INLE_{AD}$	Sampling time ≥ 150 ns Conversion clock = 40 MHz	-	-	±3	LSB
D4	Differential non-linearity error	$DNLE_{AD}$		-	-	±3	LSB
D5	Zero transition voltage	-		-20	-	20	mV
D6	Full-scale transition voltage	-		4980	-	5020	mV
D7	A/D conversion time	-		0.5	-	-	µs
D8	Input dynamic range	V_{IA}		V_{SS}	-	V_{DD50}	V
D9	Power supply current during operation	I_{AD}	Conversion clock = 40 MHz	-	2.5	-	mA/ unit

1.6.4.2 Programmable Gain Amplifier (VGA)

VGA0				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D10	Gain	G_{VGA}		2	-	20	Times
D11	Gain error	G_{ERR}		-	±0.5	±2.0	%
D12	Output offset voltage	V_{OFFG1}	G_{VGA}=2 to 10 times	-	±80	±180	mV
D13		V_{OFFG2}	G_{VGA}=20 times	-	±80	±195	
D14	Output reference voltage range	V_{REFG}		1.0	-	4.0	V
D15	Output dynamic range	V_{OG}		1.0	-	4.0	
D16	Input dynamic range	V_{IG1}	G_{VGA}=2 times	-1.5	-	1.5	
		V_{IG2}	G_{VGA}=3 times	-1.0	-	1.0	
		V_{IG3}	G_{VGA}=4 times	-0.75	-	0.75	
		V_{IG4}	G_{VGA}=5 times	-0.6	-	0.6	
		V_{IG5}	G_{VGA}=6 times	-0.5	-	0.5	
		V_{IG6}	G_{VGA}=8 times	-0.375	-	0.375	
		V_{IG7}	G_{VGA}=10 times	-0.3	-	0.3	
		V_{IG8}	G_{VGA}=20 times	-0.15	-	0.15	
D17	Power supply current during operation	I_G	G_{VGA}=10 times, V_{INP}=V_{INN}=0.0 V	-	2.6	-	mA/ Unit

1.6.4.3 Comparator

CMP00				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D18	Input offset voltage	V_{OFFC}		-	-	±20	mV
D19	Input dynamic range	V_{IC}		50	-	4950	
D20	Input hysteresis width	V_{HYSC}	Reference voltage = 2.5 V	-	30	50	
D21	Minimum comparison voltage	V_{MINC}		20	-	-	
D22	Power supply current during operation	I_C		-	0.3	-	mA/ Unit

1.6.4.4 D/A Converter

8-bit D/A Converter DACI00 DACV0				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D23	Resolution			-	-	8	Bits
D24	Integral non-linearity error	$INLE_{DA1}$		-	-	±1	LSB
D25	Differential linearity error	$DNLE_{DA1}$		-	-	±1	
D26	Zero scale voltage	-		-20	-	20	mV
D27	Full scale voltage	-		4960	-	5020	
D28	Power supply current during operation	I_{DA1}		-	0.5	-	mA/ Unit

10-bit D/A Converter DACP0				V_{DD50} = 5.0 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D29	Resolution			-	-	10	Bits
D30	Integral non-linearity error	$INLE_{DA2}$		-	-	±3	LSB
D31	Differential linearity error	$DNLE_{DA2}$		-	-	±3	
D32	Zero scale voltage	-		-20	-	20	mV
D33	Full scale voltage	-		4980	-	5035	
D34	Power supply current during operation	I_{DA2}		-	0.5	-	mA/ Unit

1.6.4.5 Power Supply Voltage Detection (LVD)

				V_{SS} = 0.0 V Tc= -40 °C to110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D35	Power supply voltage detection level	V_{LVDP}	At rising	4.0	4.2	4.4	V
D36		V_{LVDN}	At falling	3.9	4.1	4.3	
D37	Change rate of power supply voltage	ΔV_{DD5P}	At rising			5	V/ms
D38		ΔV_{DD5N}	At falling			1	

1.6.4.6 Power-On Reset

				V_{SS} = 0.0 V Tc= -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D39	Power supply voltage detection level	V_{RST5P}	At rising	2.90	2.95	3.00	V
D40		V_{RST5N}	At falling	2.80	2.85	2.90	
D41		V_{RST3P}	At rising	2.40	2.55	2.70	
D42		V_{RST3N}	At falling	2.35	2.50	2.65	
D43	Change rate of power supply voltage	ΔV_{DD5P}	At rising	-	-	5	V/ms
D44		ΔV_{DD5N}	At falling	-	-	1	

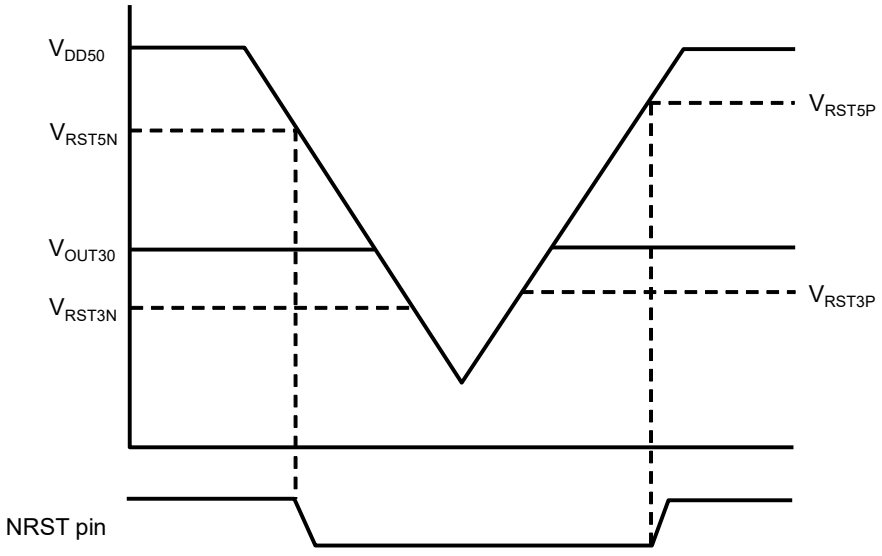


Figure 1.6-3 Characteristics of Power-On Reset Circuit

1.6.4.7 Internal Oscillation

				V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D45	Oscillation frequency	F_{RC}		9.5	10	10.5	MHz

Note:
Factory calibrated, parts not soldered.

1.6.5 AC Characteristics

				V_{DD50} = V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	Reset signal pulse width	t_{NRSTW}		1	-	-	µs

1.6.6 Flash EEPROM Characteristics

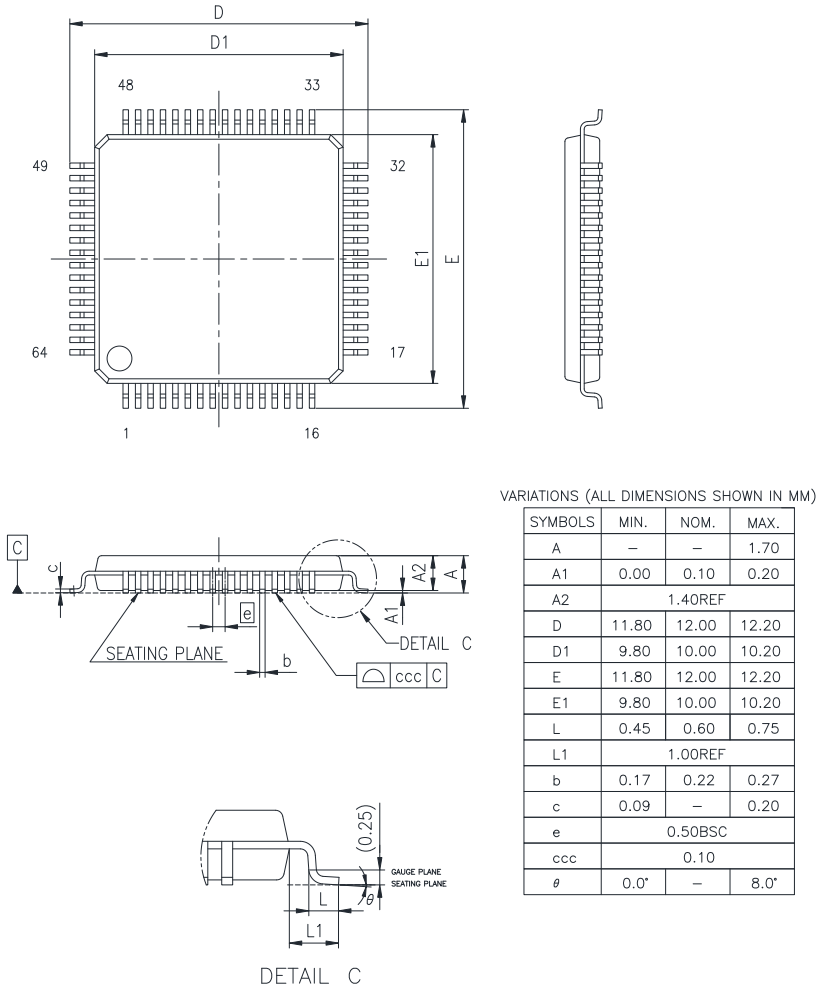
				V_{DD50}= V_{RST5N} to 5.5 V, V_{SS} = 0.0 V Tc = -40 °C to 110 °C			
Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Allowable time of rewriting: 1	E_{MAX1}	I-Flash, when the ECC function is enabled	10,000	-	-	times
F2	Allowable time of rewriting: 2	E_{MAX2}	D-Flash, when the ECC function is enabled	100,000	-	-	
F3	Data retention period 1 (*1)	T_{HLD1}	I-Flash After rewriting EMAX1 (MIN) times	20	-	-	years
F4	Data retention period 2 (*1)	T_{HLD2}	D-Flash After rewriting EMAX2 (MIN) times	5	-	-	
F5	Data retention period 3 (*1)	T_{HLD3}	D-Flash After rewriting 1,000 times	10	-	-	

Note:
*1 This includes the time when the power is off.

1.7 Package Dimension

The package dimension is shown in the following order.

- 64 pins 10mm * 10mm 0.5mm pitchFigure 1.7-1

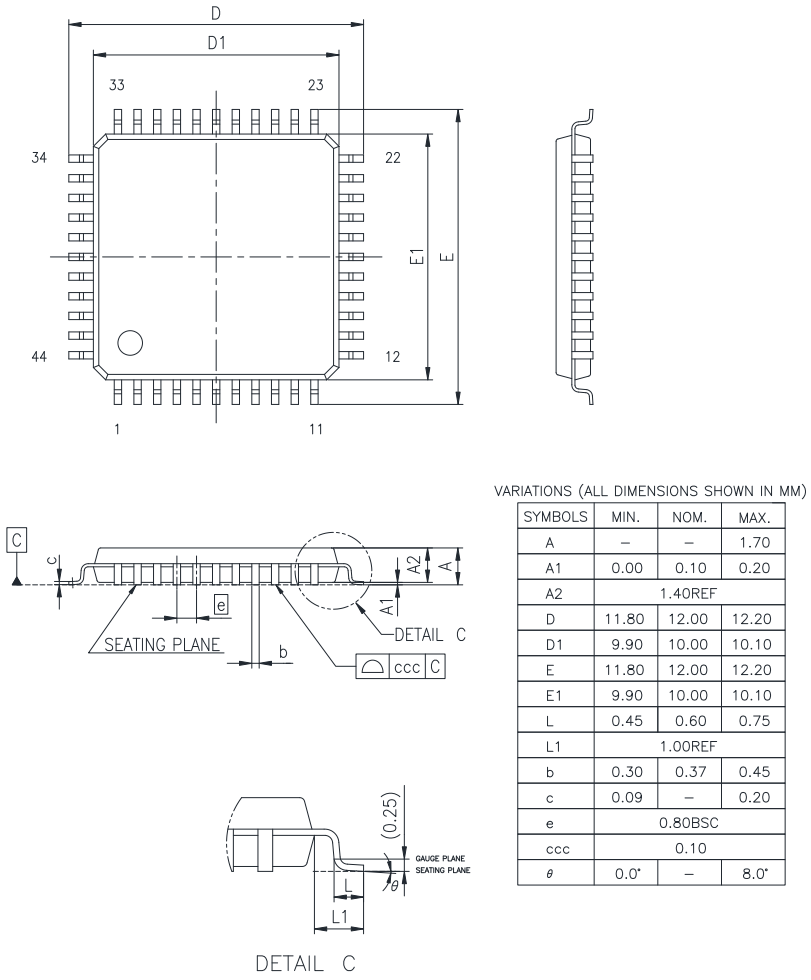


VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.70
A1	0.00	0.10	0.20
A2		1.40REF	
D	11.80	12.00	12.20
D1	9.80	10.00	10.20
E	11.80	12.00	12.20
E1	9.80	10.00	10.20
L	0.45	0.60	0.75
L1		1.00REF	
b	0.17	0.22	0.27
c	0.09	–	0.20
e		0.50BSC	
ccc		0.10	
θ	0.0°	–	8.0°

Figure 1.7-1 Package Dimension of 64 pins 10mm * 10mm 0.5mm pitch

- 44 pins 10mm * 10mm 0.8mm pitchFigure 1.7-2



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.70
A1	0.00	0.10	0.20
A2		1.40REF	
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
L	0.45	0.60	0.75
L1		1.00REF	
b	0.30	0.37	0.45
c	0.09	–	0.20
e		0.80BSC	
ccc		0.10	
θ	0.0°	–	8.0°

Figure 1.7-2 Package Dimension of 44 pins 10mm * 10mm 0.8mm pitch

Note:

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

1.8 Cautions for Circuit Setup

The cautions for circuit setup are described as follows.

- Cautions of Usage
- Pin Connections
- Unused Pin Connection
- Cautions of Power Supply
- Example of Oscillator Connection

1.8.1 Cautions of Usage

When using this LSI, obey the following cautions.

1. Operation temperature should be well considered. If the operation temperature is over the condition, improper operation can occur.
2. Operation voltage should be also well considered.

   - If the operation voltage is over the operating range, duration of the product can be shortened (e.g. the lifetime warranty of a transistor due to the change over time).

   - If the operation voltage is below the operating range, it may operate improperly.
3. If you install the product close to high electrical fields (just below the cathode ray tube, etc.), shield the package surface to ensure normal performance.

1.8.2 Pin Connections

Each pin connection is listed in Table 1.8-1 .

Table 1.8-1 Pin Connections

Pin name	Input/Output	Connection details
VDD50	Input	Connect to 5 V external power supply. Connect the bypass capacitors of 0.1 μF and the decoupling capacitor of 10 μF or more between each pin and VSS pins. (Put the capacitor near the pins)
VSS	Input	Short circuit with common GND.
VOUT30, VOUT12	Output	Connect the bypass capacitors of 0.1 μF and the used capacitor of 1 μF to 50 μF for stabilization between each pin and VSS pins. (Put the capacitor near the pins)
OSCI, OSCO	I/O pin	HXOCLK is generated by connecting the oscillator to OSCI and OSCO pins and starting external oscillation(HXO).
SWDCLK, SWDD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect toV_{DD50} with the resistor of 10 kΩ.
TRCSWO	Output	Insert a 100 Ω limit resistor between this pin and the external connector.
TEST0, TEST1	Input	Pull-down connect to V_{SS} with the resistor of 2 kΩ.
NDMOD	Input	Insert a 100 Ω limit resistor between this pin and the external connector. Pull-up connect to V_{DD50} with the resistor of 2 kΩ.
NRST	I/O pin	Insert a 100 Ω limit resistor between this pin and the external connector. Connect the capacitor of 0.1 μF or more between each pin and VSS pins. (Put the capacitor near the pins)
P70, P71, P73, P75	Input	When inserting a limit resistor while using VGA function, set it to 200 Ω or less.

Note:

Determine the processing method of each pin by evaluating enough in consideration of the effect of external noise.

Note:

VOUT30 and VOUT12 are pins to connect a capacity for the internal power supply stabilization.

Note:

For pins not listed in Table 1.8-1 , inserting a 100 Ω limit resistor is effetive for noise resistance.

Figure 1.8-1 shows the MCU peripheral recommended circuit. Table 1.8-2 shows the recommended external circuit constants.

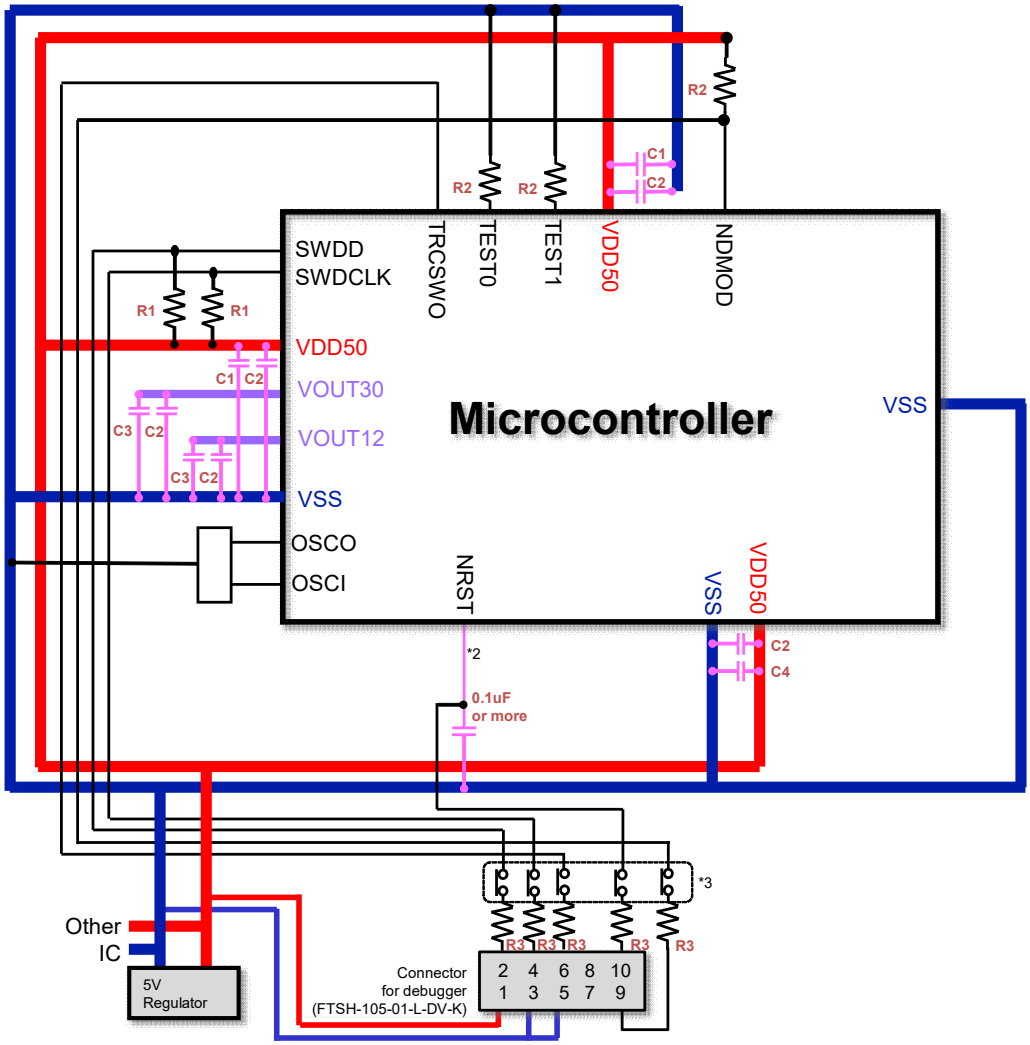


Figure 1.8-1 MCU Peripheral Recommended Circuit

Table 1.8-2 Recommended External Circuit Constants

Sign	Recommended Value	Objective
C1	10 μF	For noise filtering (*1)
C2	0.1 μF	
C3	10 μF	For the stabilization of internal regulator
C4	C3 or more	
R1	10 kΩ	For setting mode pin
R2	2 kΩ	
R3	100 Ω	For preventing noise of communication line

Note:

*1 Because the most suitable capacity value changes according to the frequency of noise, determine the value by the evaluation enough.

Note:

*2 When external reset IC is unused, do not add pull-up resistor to NRST pin.

Note:

*3 By attaching a jumper etc. near the microcontroller, it is possible to prevent noise coming from the connector and the wiring on the PCB.

Note:

Set the communication speed so that the time constant of the load on the communication path is less than half the communication cycle.

1.8.3 Unused pins

It is recommended to use the following procedure to set unused I/O pins to general purpose port function.

First, set unused I/O pins to general purpose port function. Then, set the pins either to I/O disabled state(both input enable and output enable are OFF) or to output state(input enable is OFF and output enable is ON). After that, open the pins. The pins(only for input) which have general purpose port function are also recommended to be set like unused I/O pins. The details are shown in Figure 1.8-2 and Table 1.8-3 .

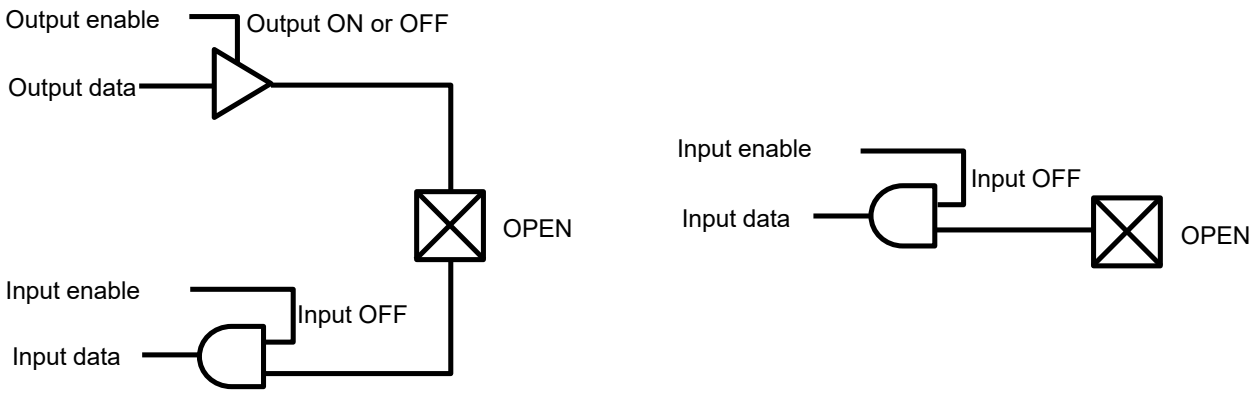


Figure 1.8-2 Unused I/O Pins

Table 1.8-3 Recommended Method of Unused I/O Pins

Pin	Input/ Output	Recommended method of unused pins
P66, P70, P71, P73, P75	Input	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Connect the resistor for pull-down in VSS in the state of input with port control. - Connect the resistor for pull-up in VDD5 in the state of input with port control.
Other I/O pin	I/O pin	Set it as general-purpose port function and perform one of the following processing. - Set pins to open in the state of Input/Output prohibition with port control. - Set pins to open in the state of "High-level" Output or "Low-level" Output with port control. - Connect the resistor for pull-down in VSS in the state of input with port control. - Connect the resistor for pull-up in VDD5 in the state of input with port control.

Note:
Determine how to process each pin by evaluating enough in consideration of the effect of external noise.

1.8.4 Cautions of Power Supply

The cautions of power supply are described as follows.

- Relations between Power Supply and Input Pin Voltage
- Restriction in Power-on
- Power Supply Circuit for LSI

1.8.4.1 Relations between Power Supply and Input Pin Voltage

Input pin voltage should be supplied only after power supply is on. If this order is reversed, a latch up occurs inside of the LSI and the destruction of the LSI by a large current flow can occur.

Relations between power supply and input pin voltage are shown in Figure 1.8-3 .

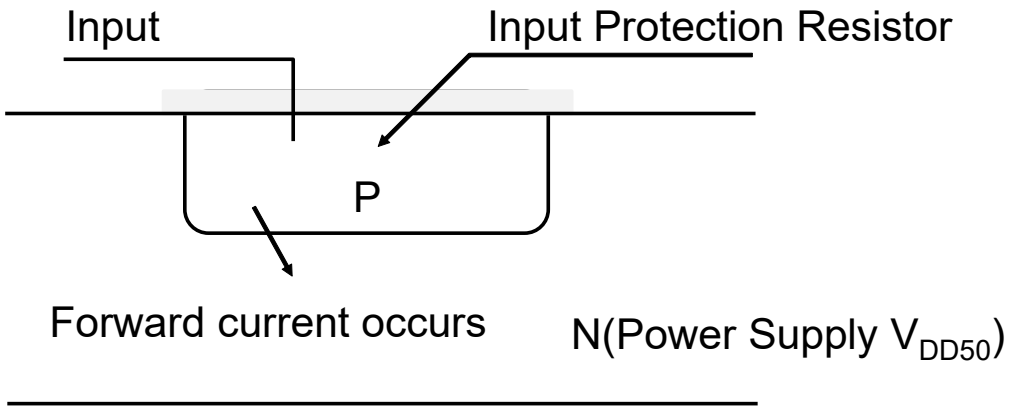


Figure 1.8-3 Relations between Power Supply and Input Pin Voltage

1.8.4.2 Restriction in Power-on

This LSI generates reset when power is applied by Power-On Reset and operates with the internal power supply generated by internal regulator. Therefore, design the circuit board so that the relations of NRST voltage, power supply voltage(VDD50), and internal power supply voltage(VOUT12) will comply with the following conditions.

- $\Delta V_{DD50P} \leq 5$ V/ms
- $t_{VOUT12} < t_{VRST}$
- $t_{NRSTW} \geq 1$ µs

ΔV_{DD50P} : The change rate of power supply voltage VDD50

t_{VOUT12} : The time when power supply voltage reaches 1.08 V

t_{VRST} : The time when power supply voltage reaches the lower limit of power supply voltage level (V_{RST5P})

t_{NRSTW} : The time that NRST pin maintains "L" level

Figure 1.8-4 shows the relations between power supply voltage and NRST voltage.

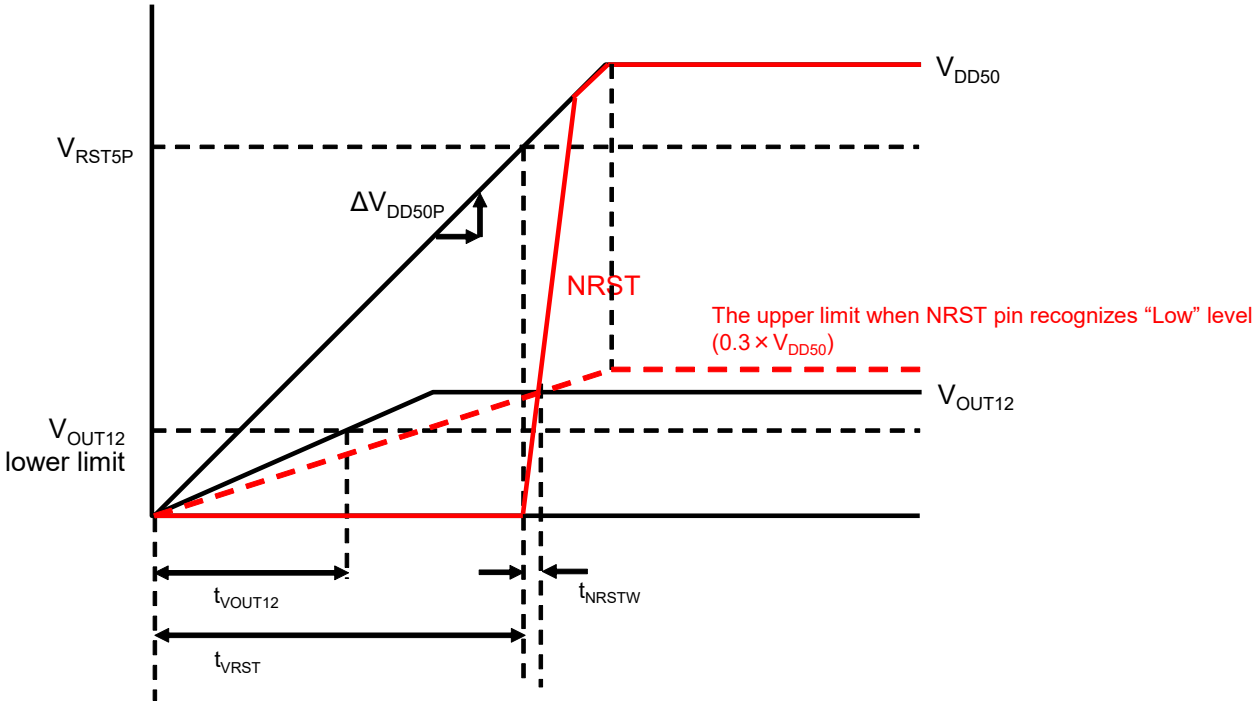


Figure 1.8-4 The Relations between LSI Power Supply and Reset Input Voltage

1.8.4.3 Power Supply Circuit for LSI

The power supply circuit should be designed with a sufficient margin, after checking AC line noise evaluation, and confirming the ripple when driving an LED and considering the power supply system.

Figure 1.8-5 shows an example for a power supply circuit. (Emitter follower type).

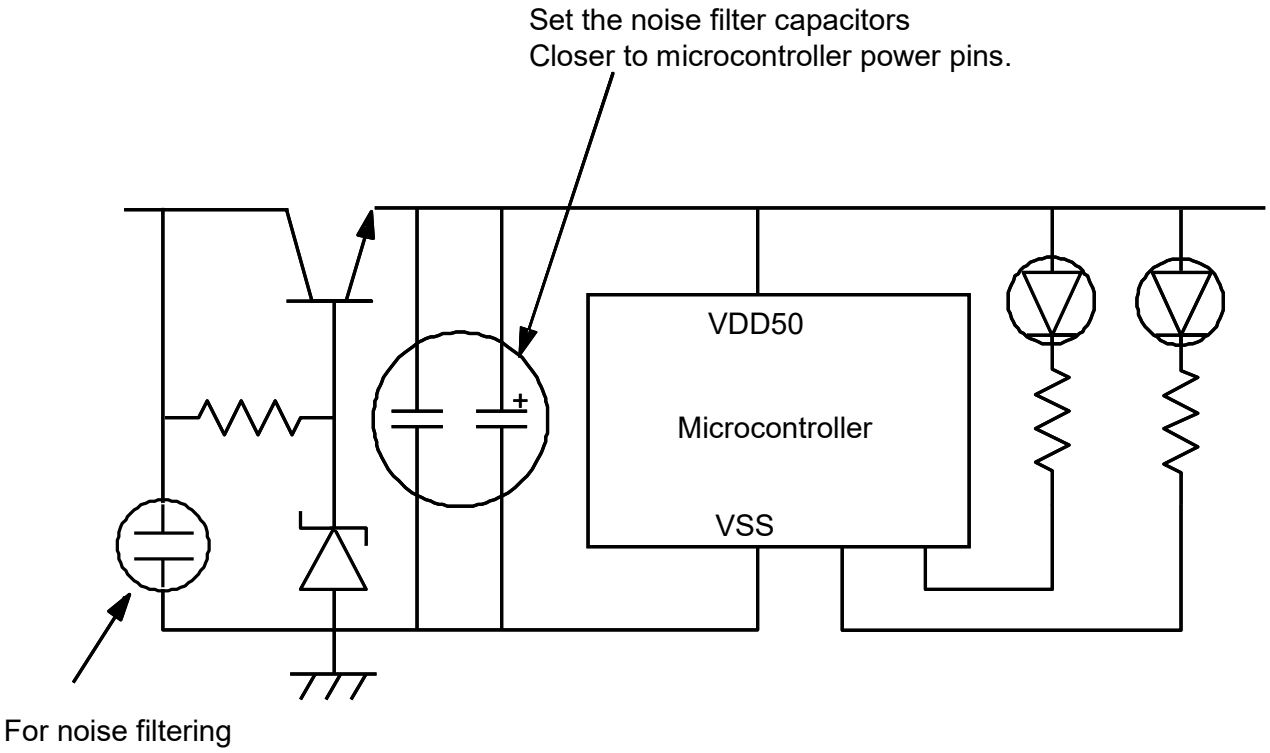


Figure 1.8-5 Power Supply Circuit Example(Emitter Follower Type)

1.8.5 Example of Oscillator Connection

Figure 1.8-6 shows the example of oscillator connection, and Table 1.8-4 shows recommended oscillators and the circuit constants.

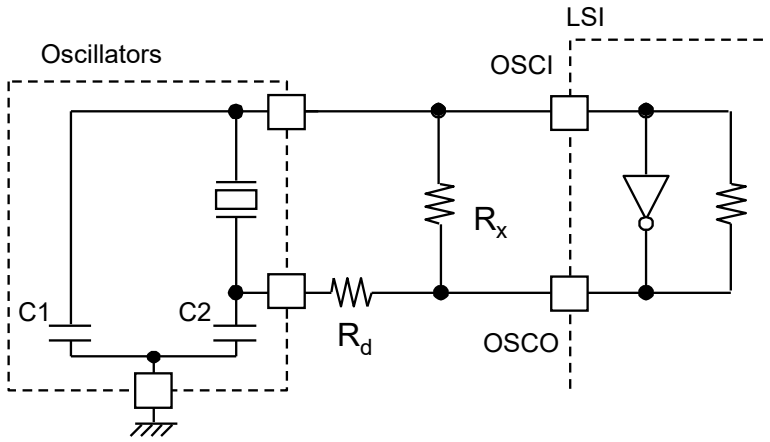


Figure 1.8-6 Example of Oscillator Connection

Table 1.8-4 Recommended Oscillators and The Circuit Constants

Oscillator maker	Frequency [MHz]	Type	Oscillator Product Number	Recommended circuit constant		
				Load capacity C1 = C2 [pF]	External feedback resistor R_X [Ω]	Dumping resistor R_d [Ω]
Murata	20	SMD	CSTNE20M0V530000R0	15	Open	150
		Lead	CSTLS20M0X53-B0	15	Open	0
	16	SMD	CSTNE16M0V530000R0	15	Open	150
		Lead	CSTLS16M0X53-B0	15	Open	0
	10	SMD	CSTNE10M0G550000R0	33	Open	220
		Lead	CSTLS10M0G56-B0	47	Open	220
	8	SMD	CSTNE8M00G550000R0	33	Open	330
		Lead	CSTLS8M00G56-B0	47	Open	330
	4	SMD	CSTCR4M00G55-R0	39	Open	330
		Lead	CSTLS4M00G56-B0	47	Open	330
Kyocera	20	Quartz Crystal Unit	CX3225CA	8	Open	1000
	16				Open	1500
	12				Open	1000
	10		CX5032GA	10	Open	0
	8			12	Open	330
	4		CX8045GA	20	Open	470

The recommended values above are based on the evaluation result of oscillator for a single unit of this LSI.

Note:

Consult the oscillator maker for the appropriate circuit constant because circuit constant of each oscillator, which is connected to OSCI/OSCO, depends on stray capacitance of the oscillator or on the mounting circuit.

Inquiries

If you have questions regarding technical information on this manual, please visit the following URL.

Nuvoton Technology Corporation Japan

URL: https://www.nuvoton.co.jp/en/contact/

- Microcomputer Home Page
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KM1M4BF64/65/66/67 Series
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