NuMicro® Family

ARM926EJ-S™-based Microprocessor

N9H31 Series
Datasheet

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1 GENERAL DESCRIPTION

The N9H31 series targeted for general purpose 32-bit microcontroller embeds an outstanding CPU core ARM926EJ-S, a RISC processor designed by Advanced RISC Machines Ltd., runs up to 300 MHz, with 16 KB I-cache, 16 KB D-cache and MMU, 56KB embedded SRAM and 16 KB IBR (Internal Boot ROM) for booting from USB, NAND and SPI FLASH.

The N9H31 series integrates one 10/100 Mb Ethernet MAC controller, USB 2.0 HS HOST/Device controller with HS transceiver embedded, TFT type LCD controller, CMOS sensor I/F controller, 2D graphics engine, I2S I/F controller, SD/MMC/NAND FLASH controller, GDMA and 4 channels 12-bit ADC controller with resistance touch screen functionality. It also integrates UART, SPI/MICROWIRE, I2C, CAN, LIN, PWM, Timer, WDT/Windowed-WDT, GPIO, Smart Card I/F, 32.768 KHz XTL and RTC (Real Time Clock).

In addition, the N9H31 series integrates a DRAM I/F, that runs up to 150MHz with supporting DDR2 type SDRAM.

2 FEATURES

2.1 N9H31 Series Features

- Core
  - Arm® ARM926EJ-S™ processor core runs up to 300 MHz
  - Supports 16 KB instruction cache and 16 KB data cache
  - Supports MMU
  - Supports JTAG Debug interface
- DDR SDRAM Controller
  - Supports LVDDR and DDR2 SDRAM
  - Clock speed up to 150 MHz
  - Supports 16-bit data bus width
  - Memory size depended on embedded SDRAM configuration by different part number.
- Embedded SRAM and ROM
  - Supports 56 Kbytes embedded SRAM
  - Supports 16 Kbytes Internal Boot ROM (IBR)
  - Supports up to four booting modes
  - Boot from USB
  - Boot from eMMC
  - Boot from NAND Flash
  - Boot from SPI Flash
- Clock Control
  - Supports two PLLs, up to 500 MHz, for high performance system operation
  - External 12 MHz high speed crystal input for precise timing operation
  - External 32.768 kHz low speed crystal input for RTC function and low speed clock source
- Ethernet MAC Controller
  - Supports one Ethernet MAC controller
  - Supports IEEE Std. 802.3 CSMA/CD protocol
  - Supports packet time stamping for IEEE Std. 1588 protocol
  - Supports 10 and 100 Mbps operations
  - Supports Half- and Full-duplex operations
  - Supports RMII interface to Ethernet physical layer PHY
  - Supports Ethernet physical layer PHY management through MDC and MDIO interface
  - Supports flow control in Full-duplex mode to receive, recognize and transmit PAUSE frame
  - Supports CAM-like function to recognize 48-bit Ethernet MAC address
  - Supports Wake-On-LAN by detecting Magic Packet
  - Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
  - Supports DMA function
  - Supports internal loop back mode for diagnostic
- USB 2.0 Controller
  - Supports USB Revision 2.0 specification
  - Supports one set of USB 2.0 High-Speed (HS) Device/Host with embedded transceiver
  - Supports one set of USB 2.0 High-Speed (HS) Host with embedded transceiver
  - Supports Control, Bulk, Interrupt, Isochronous and Split transfers
  - Supports USB host function compliant to Enhanced Host Controller Interface (EHCI) 1.0 specification to connect with USB 2.0 High-Speed (HS) device.
  - Supports USB host function compliant to Open Host Controller Interface (OHCI) 1.0 specification to connect with USB 1.1 Full-Speed (FS) and Low-Speed (LS) devices
  - Supports USB High-Speed (HS) and Full-Speed (FS) device function

- Supports USB device function with 1 endpoint for Control IN/OUT transfers and 12 programmable endpoints for Bulk, Interrupt and Isochronous IN/OUT transfers
- Supports suspend, resume and remote wake-up capability
- Supports DMA function
- Supports 2048 Bytes internal SRAM for USB host function and 4096 Bytes internal SRAM for USB device function

- Flash Memory Interface
  - Supports NAND Flash interface
  - Supports 8-bit data bus width
  - Supports SLC and MLC type NAND Flash device
  - Supports 512 B, 2 KB, 4 KB and 8 KB page size NAND Flash device
  - Supports ECC4, ECC8, ECC12, ECC15 and ECC24 BCH algorithm for ECC code generation, error detection and error correction.
  - Supports eMMC Flash interface
  - Supports DMA function to accelerate the data transfer between system memory and NAND and eMMC Flash.
- I^2S Controller
  - Supports I^2S interface
    - Supports both mono and stereo
    - Supports both record and playback
    - Supports 8-bit, 16-bit 20-bit and 24-bit data precision
    - Supports master and slave mode
  - Supports PCM interface
    - Supports 2 slots mode to connect 2 device
    - Supports 8-bit, 16-bit 20-bit and 24-bit data precision
    - Supports master mode
  - Supports four 8x24 (8 24-bit) buffer for left/right channel record and left/right playback
  - Supports DMA function to accelerate the data transfer between system memory and internal buffer
  - Supports 2 buffer address for left/right channel and 2 slots data transfer
- LCD Display Controller
  - Supports 8/9/16/18/24-bit data with to connect with 80/68 series MPU type LCD module
  - Supports resolution up to 1024x768
  - Supports data format conversion from RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 to RGB444, RGB565, RGB666, RGB888, YUV422 and YUV444 for display output
  - Supports CCIR-656 (with VSYNC, HSYNC and data enable sync signal) 8/16-bit YUV data output to connect with external TV encoder
  - Supports 8/16 bpp OSD data with video overlay function to facilitate the diverse graphic UI
  - Supports linear 1X to 8X image scaling up function
  - Supports Picture-In-Picture display function
  - Supports hardware cursor
- 2D Graphic Engine
  - Supports 2D Bit Block Transfer (BitBLT) functions defined in Microsoft GDI
  - Supports Host BLT
  - Supports Pattern BLT
  - Supports Color/Font Expanding BLT
  - Supports Transparent BLT
  - Supports Tile BLT
  - Supports Block Move BLT
  - Supports Copy File BLT

- Supports Color/Font Expansion
- Supports Rectangle Fill
- Supports RGB332/RGB565/RGB888 data format.
- Supports fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
- Supports both inside and outside clipping function
- Supports alpha-blending for source/destination picture overlaying
- Supports fast Bresenham line drawing algorithm to draw solid/textured line
- Supports rectangular border and frame drawing
- Supports picture re-sizing
- Supports down-scaling from 1/255 to 254/255
- Supports up-scaling from 1 to 1.996 (1+254/255)
- Supports object rotation with different degree
- Supports L45 (45 degree left rotation) and L90 (90 degree left rotation)
- Supports R45 (45 degree right rotation) and R90 (90 degree right rotation)
- Supports M180 (mirror/flop)
- Supports F180 (up-side-down (flip) and X180 (180 degree rotation)

- JPEG Codec
  - Supports Baseline Sequential mode JPEG codec function compliant with ISO/IEC 10918-1 international JPEG standard
  - Planar Format
  - Supports to encode interleaved YCbCr 4:2:2/4:2:0 and gray-level (Y only) format image
  - Supports to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
  - Supports to decode YCbCr 4:2:2 transpose format
  - Supports arbitrary width and height image encode and decode
  - Supports three programmable quantization-tables
  - Supports standard default Huffman-table and programmable Huffman-table for decode
  - Supports arbitrarily 1X~8X image up-scaling function for encode mode
  - Supports down-scaling function for encode and decode modes
  - Supports specified window decode mode
  - Supports quantization-table adjustment for bit-rate and quality control in encode mode
  - Supports rotate function in encode mode
  - Packet Format
  - Supports to encode interleaved YUYV format input image, output bit stream 4:2:2 and 4:2:0 format
  - Supports to decode interleaved YCbCr 4:4:4/4:2:2/4:2:0 format image
  - Supports decoded output image RGB555, RGB565 and RGB888 formats.
  - The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
  - Supports arbitrary width and height image encode and decode
  - Supports three programmable quantization-tables
  - Supports standard default Huffman-table and programmable Huffman-table for decode
  - Supports arbitrarily 1X~8X image up-scaling function for encode mode
  - Supports down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
  - Supports specified window decode mode
  - Supports quantization-table adjustment for bit-rate and quality control in encode mode
- GDMA (General DMA)
  - Supports 2 channels GDMA for memory-to-memory data transfer without CPU intervention
  - Supports increment and decrement for source and destination address calculation
  - Supports 8-bit, 16-bit and 32-bit width data transfer
  - Supports four 8-bit/16-bit/32-bit burst transfer
- UART

- Supports up to 8 UART controllers
- Supports 3 UART (UART 1/6/8) ports with flow control (TXD, RXD, CTS and RTS) and 64-byte FIFO
- Supports 5 TXD/RXD only UART ports (UART 0/3/4/9/10) with 16-byte FIFO for standard device
- Supports IrDA (SIR) and LIN function
- Supports RS-485 9-bit mode and direction control
- Supports programmable baud-rate generator up to 1/16 system clock

- C-CAN
  - Supports CAN protocol version 2.0 part A and B
  - Bit rates up to 1M bit/s
  - 32 Message Objects
  - Each Message Object has its own identifier mask
  - Programmable FIFO mode (concatenation of Message Object)
  - Maskable interrupt
  - Disabled Automatic Re-transmission mode for Time Triggered CAN applications
  - Supports power down wake-up function
- Smart Card Host (SC)
  - Compliant to ISO-7816-3 T=0, T=1
  - Supports up to two ISO-7816-3 ports
  - Separate receive / transmit 4 bytes entry FIFO for data payloads
  - Programmable transmission clock frequency
  - Programmable receiver buffer trigger level
  - Programmable guard time selection (11 ETU ~ 266 ETU)
  - One 24-bit and two 8-bit time-out counters for Answer to Request (ATR) and waiting times processing
  - Supports auto inverse convention function
  - Supports transmitter and receiver error retry and error limit function
  - Supports hardware activation sequence process
  - Supports hardware warm reset sequence process
  - Supports hardware deactivation sequence process
  - Supports hardware auto deactivation sequence when detecting the card removal
- Timer
  - Supports 5 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
  - Independent clock source for each timer
  - Supports one-shot, periodic, toggle and continuous operation modes
- Watchdog Timer
  - Multiple clock sources
  - 8 selectable time out period from 1.333us ~ 14.316sec (depends on clock source)
  - WDT can wake-up from power down or idle mode
  - Interrupt or reset selectable on watchdog timer time-out
- Windowed-Watchdog Timer
  - 6-bit down counter with 11-bit pre-scale for wide range window selected
  - Interrupt on windowed-watchdog timer time-out
  - Reset on windowed-watchdog timer time out or reload in an unexpected time window
- Real Time Clock (RTC)
  - Supports software compensation by setting frequency compensate register (FCR)
  - Supports RTC counter (second, minute, hour) and calendar counter (day, month, year)
  - Supports Alarm registers (second, minute, hour, day, month, year)
  - Selectable 12-hour or 24-hour mode
  - Automatic leap year recognition

- Supports periodic time tick interrupt with 8 period options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second
- Supports battery power pin (VBAT)

- PWM
  - Built-in up to two 16-bit PWM generators provide four PWM outputs
  - Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit pre-scale, two 16-bit counters, and one Dead-Zone generator
- SPI
  - Built-in up to two sets of SPI controllers
  - Supports SPI master mode
  - Supports single/dual/quad bit data bus width
  - Full duplex synchronous serial data transfer
  - Variable length of transfer data from 8 to 32 bits
  - MSB or LSB first data transfer
  - Supports burst mode operation that transmission and reception can be executed up to four times in a transfer
- I^2C
  - Up to two sets of I^2C devices
  - Supports master mode
  - Bidirectional data transfer between masters and slaves
  - Multi-master bus (no central master)
  - Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
  - Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
  - Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
  - Programmable clocks allow versatile rate control
  - Supports software mode to generate I^2C signaling
- Advanced Interrupt Controller
  - Supports 58 interrupt sources, including 8 external interrupt sources
  - Supports programmable normal or fast interrupt mode (IRQ, FIQ)
  - Supports programmable edge-triggered or level-sensitive for 8 external interrupt sources
  - Supports programmable low-active or high-active for 8 external interrupt sources
  - Supports encoded priority methodology to allow for interrupt daisy-chaining
  - Supports lower priority interrupt automatically mask out for nested interrupt
  - Supports to clear interrupt flag automatically if interrupt source is programmed as edge-triggered
- GPIO
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports pull-up and pull-down control
- ADC
  - 12-bit SAR ADC with 160K SPS
  - Up to 4-ch single-end input
  - Supports up to 160K SPS in all channels.
  - Supports 4-wire resistance touch screen interface
  - Supports touch pressure measurement for 4-wire touch screen application
  - Supports pen down detection
- Low Voltage Detect (LVD) and Low Voltage Reset (LVR)

  - Supports two, 2.6V and 2.8V, voltage detection levels
  - Interrupt when low voltage detected
  - Reset when low voltage detected
  - Low voltage reset threshold voltage levels: 2.4 V
- Power Management
  - Advanced power management including Power Down, Deep Standby, CPU Standby and Normal Operating modes
  - Normal Operating mode
    - CPU run normally and all clocks on, the current consumption of CORE_VDD is around 185 mA (at CPU/DRAM clock is 300/150 MHz CPU).
  - CPU Standby mode
    - CPU clock stop, and all other clocks on.
  - Deep Standby mode
    - All clocks stop, except LXT, with SRAM retention, and the current consumption of CORE_VDD is typicaly 3 mA
  - Power Down mode
    - All powers are off except RTC_VDD (3.3V) and the current consumption of RTC_VDD is typicaly 7uA with RTC functionality on.
- Operating Voltage
  - 1.2V for core logic operating
  - 1.8V for DDR2 SDRAM I/O operating
  - 3.3V for normal I/O operating
- Operating Temperature: -40℃ to 85℃
- Packages:
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant.
  - LQFP 128-pin

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 N9H31 Series Part Number Naming Guide

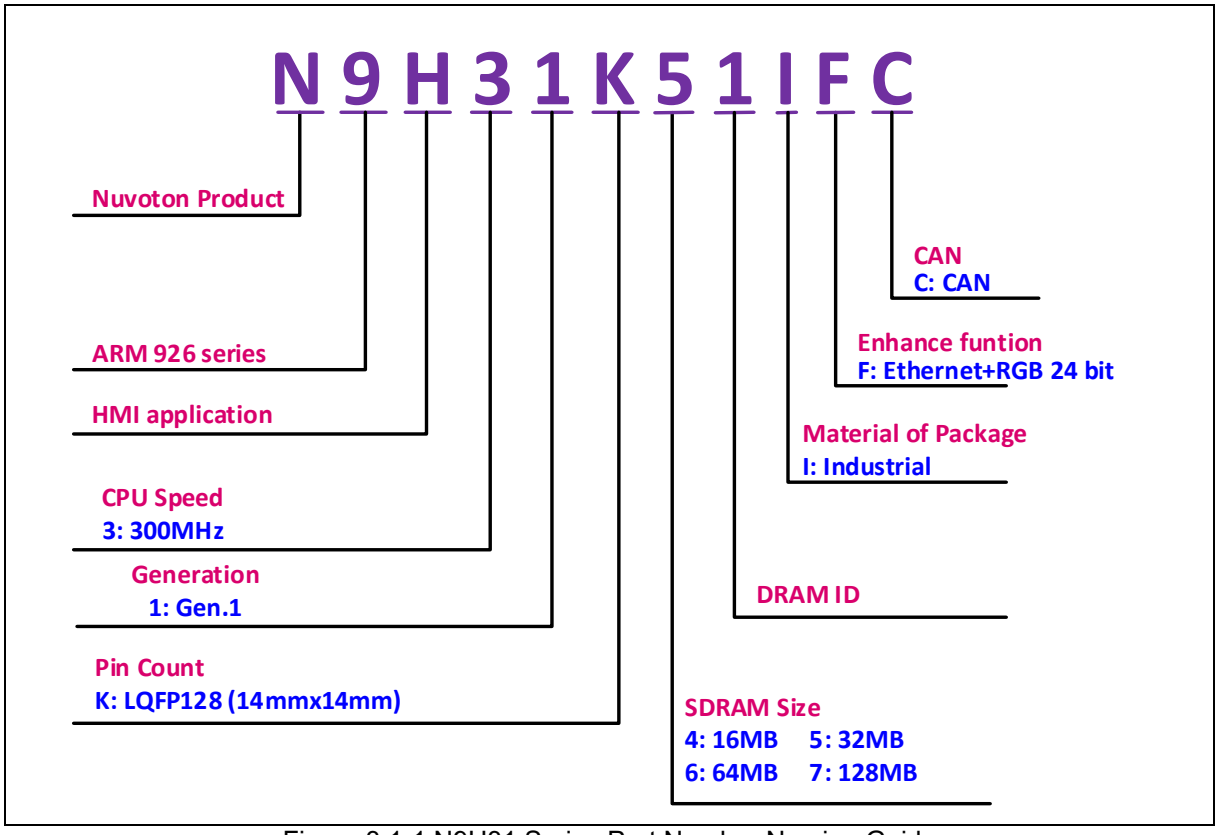


Figure 3.1-1 N9H31 Series Part Number Naming Guide

3.2 N9H31 Series Part Selection Guide

N9H31 series																														
Part No.	Memory		Storage			MAC	USB		GFX	LCD	Timer					Analog				Peripheral								Package	Operating Ambient Temp. Range1(℃)
																ADC													
	Stacked DDR2 RAM(MB)	SPI Flash, No. of I/O Pins	NAND Flash, No. of ECC bits	EMMC	SD / SDIO	Ethernet 10/100 MAC	USB 2.0 Host (480M bps)	USB 2.0 HS Device	2D Graphics	TFT LCD	Real-Time Clock(RTC)	Timer(32-bit)	Watchdog Timer	Window Watchdog Timer	PWM	Touch Screen Controller	No. of Channels	Speed (Samples per second)	LVD/LVR	GPIO(Max)	UART	CAN BUS	I²C(Master Only)	SPI	ISO-7816-3	CMOS Interface	I²S		
N9H31K63IFC	64	1	24	√	2	1	2	1	√	24-bit	√	5	√	√	2	√	4	200K	√	89	8	1	2	2	2	√	1	LQFP128	-40 to +85
N9H31K51IFC	32	1	24	√	2	1	2	1	√	24-bit	√	5	√	√	2	√	4	200K	√	89	8	1	2	2	2	√	1	LQFP128	-40 to +85

Table 3.2-1 Selection Guide

3.3 Pin Configuration

3.3.1 N9H31 Series Pin Diagram

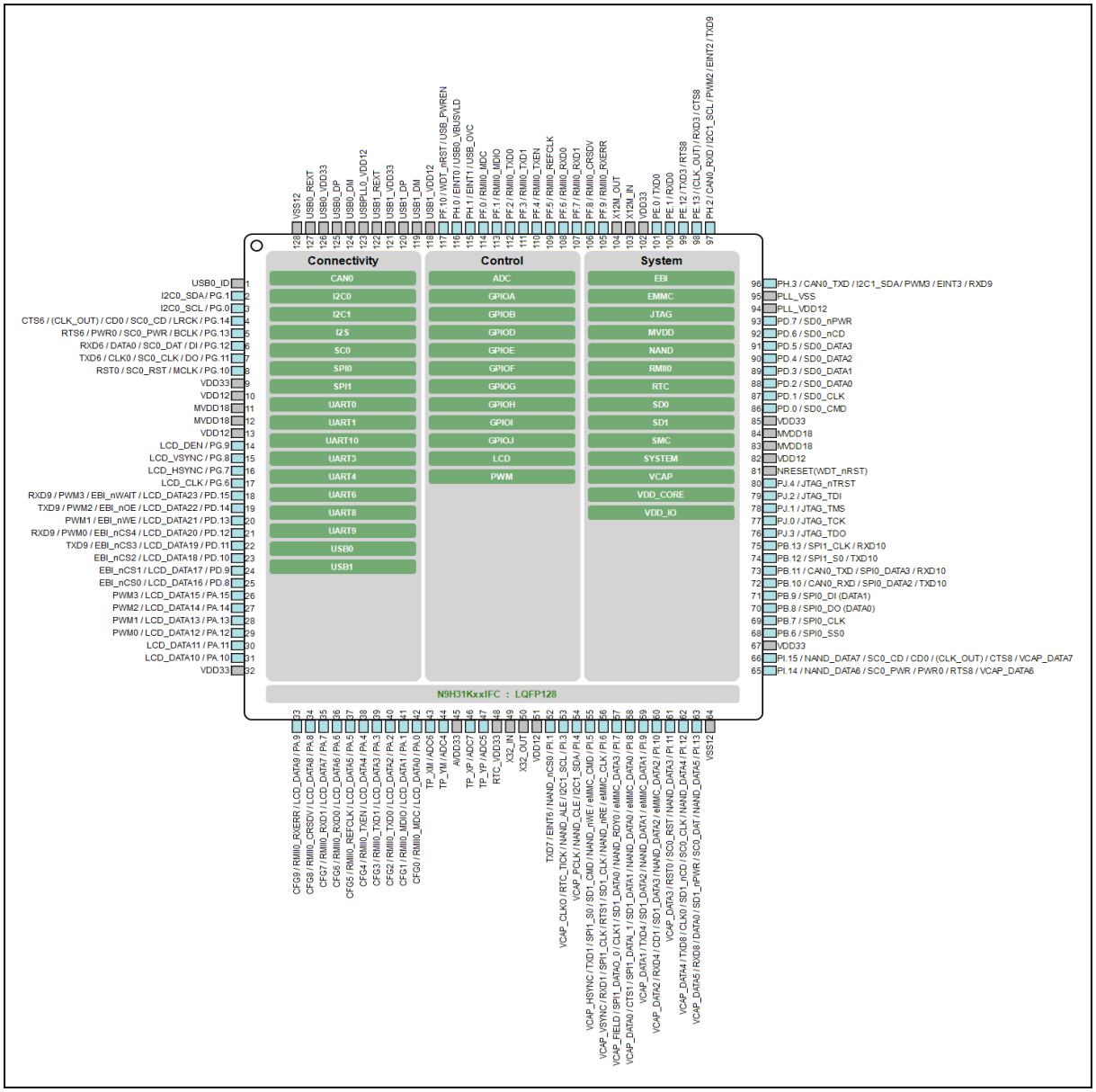


Figure 3.3-1 N9H31 Series LQFP 128-pin Pin Diagram

3.4 Pin Description

N9H31KxxIFC (LQFP128)	Pin Name	Pin Type	Description
1	USB0_ID	IU	USB0 Host/Device select.
2	PG.1	I/O	General purpose digital I/O pin Port G Pin 1.
	I2C0_SDA	I/O	I²C0 data input/output pin.
3	PG.0	I/O	General purpose digital I/O pin Port G Pin 0.
	I2C0_SCL	O	I²C0 clock pin.
4	PG.14	I/O	General purpose digital I/O pin Port G Pin 14.
	I2S_LRCK	O	I²S left right channel clock.
	UART6_CTS	I	Clear to send input pin for UART6.
	SC0_CD	I	SmartCard0 card detect pin.
	CLK_OUT	O	Reference Clock Output.
5	PG.13	I/O	General purpose digital I/O pin Port G Pin 13.
	I2S_BCLK	I	I²S bit clock pin.
	UART6_RTS	O	Request to send output pin for UART6.
	SC0_PWR	O	SmartCard0 power pin.
6	PG.12	I/O	General purpose digital I/O pin Port G Pin 12.
	I2S_DI	I	I²S data input.
	UART6_RXD	I	Data receiver input pin for UART6.
	SC0_DAT	I/O	SmartCard0 data pin.
7	PG.11	I/O	General purpose digital I/O pin Port G Pin 11.
	I2S_DO	O	I²S data output.
	UART6_TXD	O	Data transmitter output pin for UART6.
	SC0_CLK	O	SmartCard0 clock pin.
8	PG.10	I/O	General purpose digital I/O pin Port G Pin 10.
	I2S_MCLK	O	I²S master clock output pin.
	SC0_RST	O	SmartCard0 reset pin.
9	IO_VDD	P	MCU I/O power pin.
10	CORE_VDD	P	MCU internal core power pin.
11	DDR_VDD	P	DDR power pin.
12	DDR_VDD	P	DDR power pin.
13	CORE_VDD	P	MCU internal core power pin.
14	PG.9	I/O	General purpose digital I/O pin Port G Pin 9.
	LCD_DEN	O	Data enable or display control signal.
15	PG.8	I/O	General purpose digital I/O pin Port G Pin 8.
	LCD_VSYNC	O	Vertical sync or frame sync.

16	PG.7	I/O	General purpose digital I/O pin Port G Pin 7.
	LCD_HSYNC	O	Horizontal sync or line sync.
17	PG.6	I/O	General purpose digital I/O pin Port G Pin 6.
	LCD_CLK	O	Pixel clock output.
18	PD.15	I/O	General purpose digital I/O pin Port D Pin 15.
	LCD_DATA23	O	LCD pixel data output bit 23.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM3	O	PWM3 output pin.
19	PD.14	I/O	General purpose digital I/O pin Port D Pin 14.
	LCD_DATA22	O	LCD pixel data output bit 22.
	UART9_TXD	O	Data transmitter output pin for UART9.
	PWM2	O	PWM2 output pin.
20	PD.13	I/O	General purpose digital I/O pin Port D Pin 13.
	LCD_DATA21	O	LCD pixel data output bit 21.
	PWM1	O	PWM1 output pin.
21	PD.12	I/O	General purpose digital I/O pin Port D Pin 12.
	LCD_DATA20	O	LCD pixel data output bit 20.
	UART9_RXD	I	Data receiver input pin for UART9.
	PWM0	O	PWM0 output pin.
22	PD.11	I/O	General purpose digital I/O pin Port D Pin 11.
	LCD_DATA19	O	LCD pixel data output bit 19.
	UART9_TXD	O	Data transmitter output pin for UART9.
23	PD.10	I/O	General purpose digital I/O pin Port D Pin 10.
	LCD_DATA18	O	LCD pixel data output bit 18.
24	PD.9	I/O	General purpose digital I/O pin Port D Pin 9.
	LCD_DATA17	O	LCD pixel data output bit 17.
25	PD.8	I/O	General purpose digital I/O pin Port D Pin 8.
	LCD_DATA16	O	LCD pixel data output bit 16.
26	PA.15	I/O	General purpose digital I/O pin Port A Pin 15.
	LCD_DATA15	O	LCD pixel data output bit 15.
	PWM3	O	PWM3 output pin.
27	PA.14	I/O	General purpose digital I/O pin Port A Pin 14.
	LCD_DATA14	O	LCD pixel data output bit 14.
	PWM2	O	PWM2 output pin.
28	PA.13	I/O	General purpose digital I/O pin Port A Pin 13.
	LCD_DATA13	O	LCD pixel data output bit 13.
	PWM1	O	PWM1 output pin.

29	PA.12	I/O	General purpose digital I/O pin Port A Pin 12.
	LCD_DATA12	O	LCD pixel data output bit 12.
	PWM0	O	PWM0 output pin.
30	PA.11	I/O	General purpose digital I/O pin Port A Pin 11.
	LCD_DATA11	O	LCD pixel data output bit 11.
31	PA.10	I/O	General purpose digital I/O pin Port A Pin 10.
	LCD_DATA10	O	LCD pixel data output bit 10.
32	IO_VDD	P	MCU I/O power pin.
33	PA.9	I/O	General purpose digital I/O pin Port A Pin 9.
	LCD_DATA9	O	LCD pixel data output bit 9.
	PWRON_SET9	IU	Power On Setting bit 9.
34	PA.8	I/O	General purpose digital I/O pin Port A Pin 8.
	LCD_DATA8	O	LCD pixel data output bit 8.
	PWRON_SET8	IU	Power On Setting bit 8.
35	PA.7	I/O	General purpose digital I/O pin Port A Pin 7.
	LCD_DATA7	O	LCD pixel data output bit 7.
	PWRON_SET7	IU	Power On Setting bit 7.
36	PA.6	I/O	General purpose digital I/O pin Port A Pin 6.
	LCD_DATA6	O	LCD pixel data output bit 6.
	PWRON_SET6	IU	Power On Setting bit 6.
37	PA.5	I/O	General purpose digital I/O pin Port A Pin 5.
	LCD_DATA5	O	LCD pixel data output bit 5.
	PWRON_SET5	IU	Power On Setting bit 5.
38	PA.4	I/O	General purpose digital I/O pin Port A Pin 4.
	LCD_DATA4	O	LCD pixel data output bit 4.
	PWRON_SET4	IU	Power On Setting bit 4.
39	PA.3	I/O	General purpose digital I/O pin Port A Pin 3.
	LCD_DATA3	O	LCD pixel data output bit 3.
	PWRON_SET3	IU	Power On Setting bit 3.
40	PA.2	I/O	General purpose digital I/O pin Port A Pin 2.
	LCD_DATA2	O	LCD pixel data output bit 2.
	PWRON_SET2	IU	Power On Setting bit 2.
41	PA.1	I/O	General purpose digital I/O pin Port A Pin 1.
	LCD_DATA1	O	LCD pixel data output bit 1.
	PWRON_SET1	IU	Power On Setting bit 1.
42	PA.0	I/O	General purpose digital I/O pin Port A Pin 0.
	LCD_DATA0	O	LCD pixel data output bit 0.

	PWRON_SET0	IU	Power On Setting bit 0.
43	ADC6	AI	ADC input channel 6 or XM.
44	ADC4	AI	ADC input channel 4 or YM.
45	AVDD	AP	Power supply for internal analog circuit.
46	ADC7	AI	ADC input channel 7 or XP.
47	ADC5	AI	ADC input channel 5 or YP.
48	RTC_VDD	P	RTC power input. (*. or 3.3V)
49	X32_IN	AI	External 32.768 kHz crystal input.
50	X32_OUT	AO	External 32.768 kHz crystal output.
51	CORE_VDD	P	MCU internal core power pin.
52	PI.1	I/O	General purpose digital I/O pin Port I Pin 1.
	NAND_nCS0	O	NAND Flash chip select 0.
	UART7_TXD	O	Data transmitter output pin for UART7.
	INT6	I	External interrupt 6 input pin.
53	PI.3	I/O	General purpose digital I/O pin Port I Pin 3.
	VCAP_CLKO	O	Sensor interface system clock.
	NAND_ALE	O	NAND Flash address latch enable.
	I2C1_SCL	O	I^2C1 clock pin.
	CAN0_RXD	I	CAN bus receiver0 input.
	RTC_TICK	O	RTC tick output
54	PI.4	I/O	General purpose digital I/O pin Port I Pin 4.
	VCAP_PCLK	I	Sensor interface pixel clock.
	NAND_CLE	O	NAND Flash command latch enable.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
	CAN0_TX	O	CAN bus transmitter0 output.
55	PI.5	I/O	General purpose digital I/O pin Port I Pin 5.
	VCAP_HSYNC	I	Sensor interface HSYNC.
	NAND_nWE	O	NAND Flash write enable.
	eMMC_CMD	I/O	eMMC command/Response.
	SD1_CMD	O	SD/SDIO mode #1 – command/response.
	UART1_TXD	O	Data transmitter output pin for UART1.
	SPI1_SS0	O	1st SPI1 chip select pin.
56	PI.6	I/O	General purpose digital I/O pin Port I Pin 6.
	VCAP_VSYNC	I	Sensor interface VSYNC.
	NAND_nRE	O	NAND Flash read enable.
	eMMC_CLK	O	eMMC clock output.
	SC1_RST	O	SmartCard1 reset pin.

	SD1_CLK	O	SD/SDIO mode #1– clock.
	UART1_RXD	I	Data receiver input pin for UART1.
	SPI1_CLK	O	SPI1 serial clock pin.
57	PI.7	I/O	General purpose digital I/O pin Port I Pin 7.
	VCAP_FIELD	I	Sensor interface even/odd field indicator.
	NAND_RDY0	I	NAND Flash ready/busy channel 0.
	eMMC_DATA3	I/O	eMMC data line bit 3.
	SC1_CLK	O	SmartCard1 clock pin.
	SD1_DAT0	I/O	SD/SDIO mode #1 data line bit 0.
	UART1_RTS	O	Request to send output pin for UART1.
	SPI1_DO (SPI1_DATA0)	I (I/O)	SPI1 Data out pin. (SPI1 data 0 in dual/quad mode.)
58	PI.8	I/O	General purpose digital I/O pin Port I Pin 8.
	VCAP_DATA0	I	Sensor interface data bus bit 0.
	NAND_DATA0	I/O	NAND Flash data bus bit 0.
	eMMC_DATA0	I/O	eMMC data line bit 0.
	SC1_DAT	I/O	SmartCard1 data pin.
	SD1_DAT1	I/O	SD/SDIO mode #1 data line bit 1.
	UART1_CTS	I	Clear to send input pin for UART1.
	SPI1_DI (SPI1_DATA1)	I (I/O)	SPI1 Data input pin. (SPI1 data 1 in dual/quad mode.)
59	PI.9	I/O	General purpose digital I/O pin Port I Pin 9.
	VCAP_DATA1	I	Sensor interface data bus bit 1.
	NAND_DATA1	I/O	NAND Flash data bus bit 1.
	eMMC_DATA1	I/O	eMMC data line bit 1.
	SC1_PWR	O	SmartCard1 power pin.
	SD1_DAT2	I/O	SD/SDIO mode #1 data line bit 2.
	UART4_TXD	O	Data transmitter output pin for UART4.
60	PI.10	I/O	General purpose digital I/O pin Port I Pin 10.
	VCAP_DATA2	I	Sensor interface data bus bit 2.
	NAND_DATA2	I/O	NAND Flash data bus bit 2.
	eMMC_DATA2	I/O	eMMC data line bit 2.
	SC1_CD	I	SmartCard1 card detect pin.
	SD1_DAT3	I/O	SD/SDIO mode #1 data line bit 3.
	UART4_RXD	I	Data receiver input pin for UART4.
61	PI.11	I/O	General purpose digital I/O pin Port I Pin 11.
	VCAP_DATA3	I	Sensor interface data bus bit 3.

	NAND_DATA3	I/O	NAND Flash data bus bit 3.
	SC0_RST	O	SmartCard0 reset pin.
62	PI.12	I/O	General purpose digital I/O pin Port I Pin 12.
	VCAP_DATA4	I	Sensor interface data bus bit 4.
	NAND_DATA4	I/O	NAND Flash data bus bit 4.
	UART8_TXD	O	Data transmitter output pin for UART8.
	SC0_CLK	O	SmartCard0 clock pin.
	SD1_nCD	I	SD/SDIO mode #1 – card detect.
63	PI.13	I/O	General purpose digital I/O pin Port I Pin 13.
	VCAP_DATA5	I	Sensor interface data bus bit 5.
	NAND_DATA5	I/O	NAND Flash data bus bit 5.
	UART8_RXD	I	Data receiver input pin for UART8.
	SC0_DAT	I/O	SmartCard0 data pin.
	SD1_nPWR	O	SD/SDIO mode #1 – power enable.
64	IO_VSS	P	MCU I/O ground pin.
65	PI.14	I/O	General purpose digital I/O pin Port I Pin 14.
	VCAP_DATA6	I	Sensor interface data bus bit 6.
	NAND_DATA6	I/O	NAND Flash data bus bit 6.
	UART8_RTS	O	Request to send output pin for UART8.
	SC0_PWR	O	SmartCard0 power pin.
66	PI.15	I/O	General purpose digital I/O pin Port I Pin 15.
	VCAP_DATA7	I	Sensor interface data bus bit 7.
	NAND_DATA7	I/O	NAND Flash data bus bit 7.
	UART8_CTS	I	Clear to send input pin for UART8.
	SC0_CD	I	SmartCard0 card detect pin.
	CLK_OUT	O	Clock output pin.
67	IO_VDD	P	MCU I/O power pin.
68	PB.6	I/O	General purpose digital I/O pin Port B Pin 6.
	SPI0_SS0	O	1st SPI0 chip select pin.
69	PB.7	I/O	General purpose digital I/O pin Port B Pin 7.
	SPI0_CLK	O	SPI0 serial clock pin.
70	PB.8	I/O	General purpose digital I/O pin Port B Pin 8.
	SPI0_DO (SPI0_DATA0)	O (I/O)	SPI0 Data out pin. (SPI0 data 0 in dual/quad mode.)
71	PB.9	I/O	General purpose digital I/O pin Port B Pin 9.
	SPI0_DI (SPI0_DATA1)	I (I/O)	SPI0 Data input pin. (SPI0 data 1 in dual/quad mode.)

72	PB.10	I/O	General purpose digital I/O pin Port B Pin 10.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI0_DATA2	I/O	SPI0 data 2 in dual/quad mode.
	CAN0_RXD	I	CAN bus receiver0 input.
73	PB.11	I/O	General purpose digital I/O pin Port B Pin 11.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI0_DATA3	I/O	SPI0 data 3 in dual/quad mode.
	CAN0_TXD	O	CAN bus transmitter0 output.
74	PB.12	I/O	General purpose digital I/O pin Port B Pin 12.
	UART10_TXD	O	Data transmitter output pin for UART10.
	SPI1_SS0	O	1st SPI1 chip select pin.
75	PB.13	I/O	General purpose digital I/O pin Port B Pin 13.
	UART10_RXD	I	Data receiver input pin for UART10.
	SPI1_CLK	O	SPI1 serial clock pin.
76	PJ.3	I/O	General purpose digital I/O pin Port J Pin 3.
	JTAG_TDO	O	JTAG test data out.
77	PJ.0	I/O	General purpose digital I/O pin Port J Pin 0.
	JTAG_TCK	O	JTAG test clock.
78	PJ.1	I/O	General purpose digital I/O pin Port J Pin 1.
	JTAG_TMS	O	JTAG test mode select.
79	PJ.2	I/O	General purpose digital I/O pin Port J Pin 2.
	JTAG_TDI	I	JTAG test data in.
80	PJ.4	I/O	General purpose digital I/O pin Port J Pin 4.
	JTAG_nTRST	O	JTAG Reset.
81	nRESET	IU	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state.
	WDT_nRST	O	Watch dog timer external reset output pin. Open-drain.
82	CORE_VDD	P	MCU internal core power pin.
83	DDR_VDD	P	DDR power pin.
84	DDR_VDD	P	DDR power pin.
85	IO_VDD	P	MCU I/O power pin.
86	PD.0	I/O	General purpose digital I/O pin Port D Pin 0.
	SD0_CMD	O	SD/SDIO mode #0 command/response.
87	PD.1	I/O	General purpose digital I/O pin Port D Pin 1.
	SD0_CLK	O	SD/SDIO mode #0 clock.
88	PD.2	I/O	General purpose digital I/O pin Port D Pin 2.
	SD0_DAT0	I/O	SD/SDIO mode #0 data line bit 0.
89	PD.3	I/O	General purpose digital I/O pin Port D Pin 3.

	SD0_DAT1	I/O	SD/SDIO mode #0 data line bit 1.
90	PD.4	I/O	General purpose digital I/O pin Port D Pin 4.
	SD0_DAT2	I/O	SD/SDIO mode #0 data line bit 2.
91	PD.5	I/O	General purpose digital I/O pin Port D Pin 5.
	SD0_DAT3	I/O	SD/SDIO mode #0 data line bit 3.
92	PD.6	I/O	General purpose digital I/O pin Port D Pin 6.
	SD0_nCD	I	SD/SDIO mode #0 card detect.
93	PD.7	I/O	General purpose digital I/O pin Port D Pin 7.
94	PLL_VDD	P	PLL power input pin.
95	PLL_VSS	P	PLL ground.
96	PH.3	I/O	General purpose digital I/O pin Port H Pin 3.
	I2C1_SDA	I/O	I^2C1 data input/output pin.
	UART9_RXD	I	Data receiver input pin for UART9.
	CAN0_TXD	O	CAN bus transmitter0 output.
	PWM3	O	PWM3 output pin.
	INT3	I	External interrupt 3 input pin.
97	PH.2	I/O	General purpose digital I/O pin Port H Pin 2.
	I2C1_SCL	O	I^2C1 clock pin.
	UART9_TXD	O	Data transmitter output pin for UART9.
	CAN0_RXD	I	CAN bus receiver0 input.
	PWM2	O	PWM2 output pin.
	INT2	I	External interrupt 2 input pin.
98	PE.13	I/O	General purpose digital I/O pin Port E Pin 13.
	UART8_CTS	I	Clear to send input pin for UART8.
	UART3_RXD	I	Data receiver input pin for UART3.
	CLK_OUT	O	Reference Clock Output.
99	PE.12	I/O	General purpose digital I/O pin Port E Pin 12.
	UART8_RTS	O	Request to send output pin for UART8.
	UART3_TXD	O	Data transmitter output pin for UART3.
100	PE.1	I/O	General purpose digital I/O pin Port E Pin 1.
	UART0_RXD	I	Data receiver input pin for UART0.
101	PE.0	I/O	General purpose digital I/O pin Port E Pin 0.
	UART0_TXD	O	Data transmitter output pin for UART0.
102	IO_VDD	P	MCU I/O power pin.
103	XT1_IN	AI	External 12MHz crystal input pin.
104	XT1_OUT	AO	External 12MHz crystal output pin.
105	PF.9	I/O	General purpose digital I/O pin Port F Pin 9.

	RMII0_RXERR	I	RMII0 receive data error.
106	PF.8	I/O	General purpose digital I/O pin Port F Pin 8.
	RMII0_CRSDV	I	RMII0 carrier sense / receive data valid.
107	PF.7	I/O	General purpose digital I/O pin Port F Pin 7.
	RMII0_RXDATA1	I	RMII0 receive data bus bit 1.
108	PF.6	I/O	General purpose digital I/O pin Port F Pin 6.
	RMII0_RXDATA0	I	RMII0 receive data bus bit 0.
109	PF.5	I/O	General purpose digital I/O pin Port F Pin 5.
	RMII0_REFCLK	I	RMII0 reference clock.
110	PF.4	I/O	General purpose digital I/O pin Port F Pin 4.
	RMII0_TXEN	O	RMII0 transmit enable.
111	PF.3	I/O	General purpose digital I/O pin Port F Pin 3.
	RMII0_TXDATA1	O	RMII0 transmit data bus bit 1.
112	PF.2	I/O	General purpose digital I/O pin Port F Pin 2.
	RMII0_TXDATA0	O	RMII0 Transmit Data bus bit 0.
113	PF.1	I/O	General purpose digital I/O pin Port F Pin 1.
	RMII0_MDIO	I/O	RMII0 Management Data I/O
114	PF.0	I/O	General purpose digital I/O pin Port F Pin 0.
	RMII0_MDC	O	RMII0 Management Data Clock
115	PH.1	I/O	General purpose digital I/O pin Port H Pin 1.
	USB_OVRCUR	I	USB overcurrent
	INT1	I	External interrupt 1 input pin.
116	PH.0	I/O	General purpose digital I/O pin Port H Pin 0.
	USB0_VBUSVLD	I	USB0 VBUS valid.
	INT0	I	External interrupt 0 input pin.
117	PF.10	I/O	General purpose digital I/O pin Port F Pin 10.
	USB_PWREN	O	USB host output power control pin for LQFP128 package only.
118	USBPLL1_VDD	P	USB1 PLL power pin.
119	USB1_DM	I/O	USB1 differential signal D-.
120	USB1_DP	I/O	USB1 differential signal D+.
121	USB1_VDD	AP	USB1 I/O power pin.
122	USB1_REXT	I	USB1 module reference Resister.
123	USBPLL0_VDD	P	USB0 PLL power pin.
124	USB0_DM	I/O	USB0 differential signal D-.
125	USB0_DP	I/O	USB0 differential signal D+.
126	USB0_VDD	AP	USB0 I/O power pin.
127	USB0_REXT	I	USB0 module reference Resister.

128	IO_VSS	P	MCU I/O ground pin.

Note: Pin Type I=Digital Input, O=Digital Output; AI=Analog Input; P=Power Pin; AP=Analog Power

Table 3.4-1 Pin List Table

4 BLOCK DIAGRAM

4.1 N9H31 Series Block Diagram

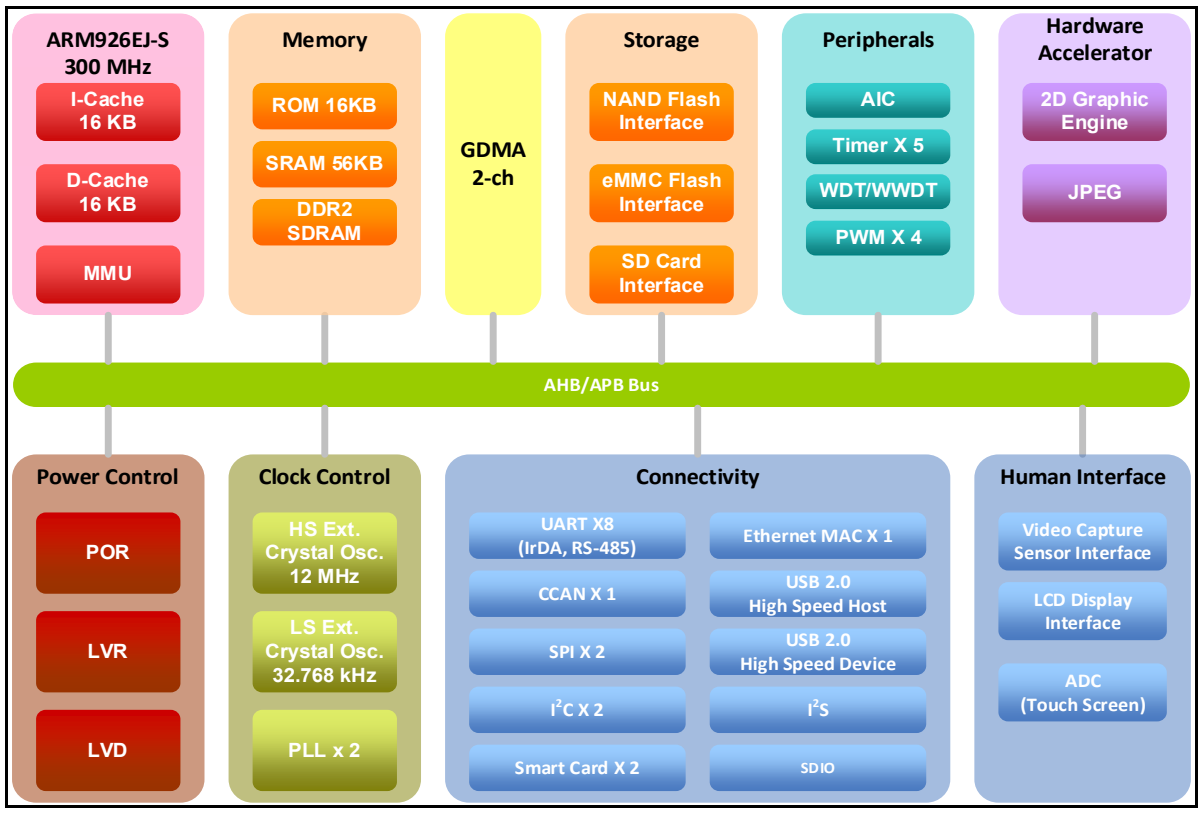


Figure 4.1-1 N9H31 Series Block Diagram

5 FUNCTIONAL DESCRIPTION

5.1 Arm® ARM926EJ-S™ Processor Core

5.1.1 Overview

The ARM926EJ-S™ processor core is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S™ processor core is targeted at multi-tasking applications where full memory management, high performance, and low power are all important.

The ARM926EJ-S™ CP processor U core supports the 32-bit ARM and 16-bit Thumb instruction sets, enabling the user to choose between high performance and high code density. The ARM926EJ-S™ processor core includes features for efficient execution of Java byte codes, providing Java performance similar to JIT, but without the associated code overhead.

The ARM926EJ-S™ processor provides support for external coprocessor enabling floating-point or other application-specific hardware acceleration to be added. The ARM926EJ-S™ processor core implements ARM architecture version 5TEJ.

The ARM926EJ-S™ processor has a Harvard cached architecture and provides a complete high-performance processor subsystem, including:

- An ARM9EJ-S integer core.
- A Memory Management Unit (MMU).
- Separate instruction and data cache.
- Separate instruction and data AMBA AHB bus interfaces.

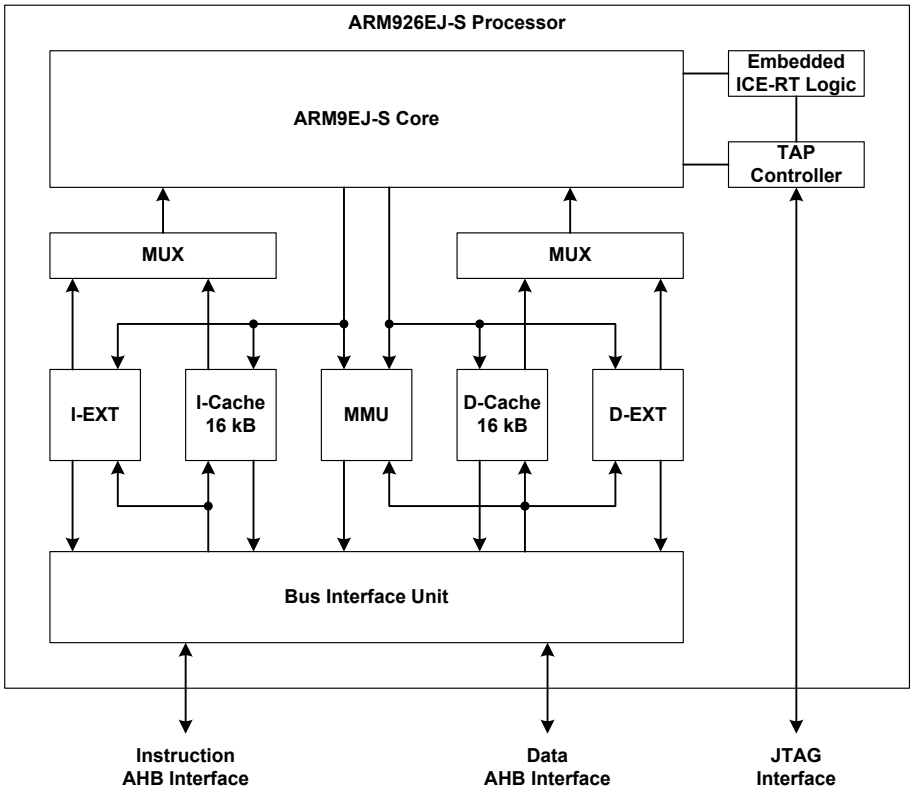


Figure 5.1-1 ARM926EJ-S Block Diagram

5.2 System Manager

5.2.1 Overview

The system management describes following information and functions.

- System Resets
- System Power Architecture
- System Memory Map
- System management registers for Product Identifier (PDID), Power-On Setting, System Wake-Up, Reset Control for on-chip controllers/peripherals, and multi-function pin control.
- System Control registers

5.2.2 System Reset

The system reset can be issued by one of the below listed events. For these reset event flags can be read by RSTSTS register.

- Power-On Reset
- Low level on the /RESET pin
- Watchdog Time Out Reset
- Low Voltage Reset
- CPU Reset
- System Reset

5.3 Clock Controller (CLK_CTL)

5.3.1 Overview

The clock controller generates all clocks for Video, Audio, CPU, AMBA and all the engine modules. This chip includes two PLL modules. The clock source for each module comes from the PLL, or from the external crystal input directly. For each clock there is bit on the CLKEN register to control the clock ON or OFF individually, and the divider setting is on the CLK_DIVCTL register. The register can also be used to control the clock enable or disable for power control.

5.3.2 Features

- Supports two PLLs, up to 500 MHz, for high performance system operation
- External 12 MHz high speed crystal input for precise timing operation
- External 32.768 kHz low speed crystal input for RTC function and low speed clock source

5.4 Advanced Interrupt Controller (AIC)

5.4.1 Overview

An interrupt temporarily changes the sequence of program execution to react to a particular event such as power failure, watchdog timer timeout, transmit/receive request from Ethernet MAC Controller, and so on. The CPU processor provides two modes of interrupt, the Fast Interrupt (FIQ) mode for critical session and the Interrupt (IRQ) mode for general purpose. The IRQ request is occurred when the nIRQ input is asserted. Similarly, the FIQ request is occurred when the nFIQ input is asserted. The FIQ has privilege over the IRQ and can preempt an ongoing IRQ. It is possible to ignore the FIQ and the IRQ by setting the F and I bits in the current program status register (CPSR).

The Advanced Interrupt Controller (AIC) is capable of processing the interrupt requests up to 64 different sources. Currently, 61 interrupt sources are defined. Each interrupt source is uniquely assigned to an interrupt channel. For example, the watchdog timer interrupt is assigned to channel 1. The AIC implements a proprietary eight-level priority scheme that categories the available 61 interrupt sources into eight priority levels. Interrupt sources within the priority level 0 is the highest priority and the priority level 7 is the lowest. In order to make this scheme work properly, a certain priority level must be specified to each interrupt source during power-on initialization; otherwise, the system shall behave unexpectedly. Within each priority level, interrupt source that is positioned in a lower channel has a higher priority. Interrupt source that is active, enabled, and positioned in the lowest channel with priority level 0 is promoted to the FIQ. Interrupt sources within the priority levels other than 0 are routed to the IRQ. The IRQ can be preempted by the occurrence of the FIQ. Interrupt nesting is performed automatically by the AIC.

Though interrupt sources originated from the chip itself are intrinsically high-level sensitive, the AIC can be configured as either low-level sensitive, high-level sensitive, negative-edge triggered, or positive-edge triggered to each interrupt source.

5.4.2 Features

- AMBA APB bus interface
- External interrupts can be programmed as either edge-triggered or level-sensitive
- External interrupts can be programmed as either low-active or high-active
- Flags to reflect the status of each interrupt source
- Individual mask for each interrupt source
- Support proprietary 8-level interrupt scheme to employ the priority scheme.
- Priority methodology is adopted to allow for interrupt daisy-chaining
- Automatically masking out the lower priority interrupt during interrupt nesting
- Automatically clearing the interrupt flag when the external interrupt source is programmed to be edge-triggered

5.5 SDRAM Interface Controller (SDIC)

5.5.1 Overview

The SDRAM Controller support SDR, DDR, Low-Power DDR and DDR2 type SDRAM. The memory device size type can be from 16M bit and up to 1G bits. Only 16-bit data bus width is supported. The total system memory size can be from 2M bytes and up to 256M bytes for different SDRAM configuration.

The SDRAM controller interface to three isolated AHB. All these AHB masters can access the memory independent. Except the memory access, the masters of AHB also could access the SDRAM control registers.

For performance and function issue, the SDRAM controller also supports the proprietary Enhanced-AHB. The EAHB add the down-count address mode, byte-enable signal and explicit burst access number. The explicit access number function is reached by modify the HBURST signal to EHBURST and it represent the access number. The maximum EAHB access number is 16. The SDRAM controller also builds a BIST module to test the external memory device.

An internal arbiter is used to schedule the access from the masters and the BIST request, the BIST request with the highest priority and the then the AHB3 master, AHB2 master and AHB1 master.

The SDRAM controller uses 3 pipe queues to improve the SDRAM command and data bus efficiency. The request in queue0 is the SDRAM active data access request. Simultaneous, the requests in queue1 can request the controller to issue the ACTIVE or PRECHARGE command to reduce the access latency for the later command. The queue1 also can issue the READ or WRITE command to close the SDRAM command when advance pipe queue

The SDRAM refresh rate is programmable. The Refresh and Power-on control module generate the refresh request signal and SDRAM power on sequence. The SDRAM controller also supports software reset, SDRAM self refresh and auto power down function.

5.5.2 Features

- Support DDR, DDR2 and LPDDR SDRAM
- Clock speed up to 150 MHz
- Support 16-bit data bus width
- Support two chip selects
- Support total memory size up to 256M bytes (each chip select for 128M bytes)

5.6 General Purpose I/O (GPIO)

5.6.1 Overview

The N9H31 series have up to 148 General-Purpose I/O (GPIO) pins and can be shared with other function pins depending on the chip configuration. These 148 pins are arranged in 10 ports named as PA, PB, PC, PD, PE, PF, PG, PH, PI and PJ. PA, PB, PD, PE, PF, PG, PH and PI have 16 pins on port, PC has 15 pins on port and PJ has 5 pins on port. Each of the 148 I/O pins is independent and can be easily configured by user to meet various system configurations and design requirements. After reset, all 148 I/O pins are configured in General-Purpose I/O Input mode.

When any of the 148 I/O pins used as a General-Purpose I/O, its I/O type can be configured by user individually as Input or Output mode. In Input mode, the input buffer type could be selected as CMOS input buffer or Schmitt trigger input buffer. Each I/O pin also equips a pull-up resistor (45 kΩ ~ 82 kΩ) and a pull-down resistor (37 kΩ ~ 91 kΩ). The enable of pull-up/pull-down resistor is controllable.

5.6.2 Features

- Support input and output mode.
- Support CMOS and Schmitt trigger input buffer.
- Support controllable pull-up and pull-down resistor.
- Support both edge and level interrupt.
- Support de-bounce circuit to filter the noise.

5.7 General DMA Controller (GDMA)

5.7.1 Overview

The chip has a two-channel general DMA controller with or without descriptor fetch operation, called the GDMA. The two-channel GDMA performs the memory-to-memory data transfers without the CPU intervention:

The on-chip GDMA can be started by the software. Software can also be used to restart the GDMA operation after it has been stopped. The CPU can recognize the completion of a GDMA operation by software polling or when it receives an internal GDMA interrupt. The GDMA controller can increment source or destination address, decrement them as well, and conduct 8-bit (byte), 16-bit (half-word), or 32-bit (word) data transfers.

5.7.2 Features

- AMBA AHB compliant
- Descriptor and Non-Descriptor based function
- Supports 8-data burst mode to boost performance
- Provides support for external GDMA device
- Demand mode speeds up external GDMA operations

5.8 Timer Controller (TMR)

5.8.1 Overview

The general timer controller includes five channels, TIMER0, TIMER1, TIMER2, TIMER3, and TIMER4, which allow user to easily implement a counting scheme or timing control for applications. The timer possesses features such as adjustable resolution, and programmable counting period. The timer can generate an interrupt signal upon timeout, or provide the current value of count during operation.

5.8.2 Features

- Independent Clock Source for each Timer channel (TMRx_CLK, x= 0, 1, 2, 3, 4).
- Five channels with a 24-bit up counter and an interrupt request each.
- Internal 8-bit pre-scale counter.
- Internal 24-bit up counter is readable through Timer Data Register, TDR (TMR_DR[23:0]).
- Supports One-shot, Periodic, and Continuous operation mode.
- Time-out period = (Period of timer clock input) * (8-bit pre-scale counter + 1) * (24-bit TCMP setting value).
- Maximum counting time = $\frac{1}{12\ \text{MHz}} \times 256 \times (2^{24} - 1)$, if TMRx_CLK = 12 MHz.

5.9 Pulse Width Modulation (PWM)

5.9.1 Overview

This chip has one PWM controller, and it has 4 independent PWM outputs, CH0~CH3, or as 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3) with 2 programmable dead-zone generators. Each PWM pair has one Prescaler, one clock divider, two clock selectors, two 16-bit PWM counters, two 16-bit comparators, and one Dead-Zone generator. They are all driven by APB system clock (PCLK) in chip. Each PWM channel can be used as a timer and issue interrupt independently.

Two channels PWM Timers in one pair share the same prescaler. The Clock divider provides each PWM channel with 5 divided clock sources (1, 1/2, 1/4, 1/8, 1/16). Each channel receives its own clock signal from clock divider which receives clock from 8-bit prescaler. The 16-bit down-counter in each channel receive clock signal from clock selector and can be used to handle one PWM period. The 16-bit comparator compares PWM counter value with threshold value in register CMR (PWM_CMR[15:0]) loaded previously to generate PWM duty cycle. The clock signal from clock divider is called PWM clock. Dead-Zone generator utilize PWM clock as clock source. Once Dead-Zone generator is enabled, two outputs of the corresponding PWM channel pair will be replaced by the output of Dead-Zone generator. The Dead-Zone generator is used to control off-chip power device.

To prevent PWM driving output pin with unsteady waveform, 16-bit down-counter and 16-bit comparator are implemented with double buffering feature. User can feel free to write data to counter buffer register and comparator buffer register without generating glitch. When 16-bit down-counter reaches zero, the interrupt request is generated to inform CPU that time is up. When counter reaches zero, if counter is set as periodic mode, it is reloaded automatically and start to generate next cycle. User can set PWM counter as one-shot mode instead of periodic mode. If counter is set as one-shot mode, counter will stop and generate one interrupt request when it reaches zero. The value of comparator is used for pulse width modulation. The counter control logic changes the output level when down-counter value matches the value of compare register.

5.9.2 Features

- 4 PWM channels with a 16-bit down counter and an interrupt each
- 2 complementary PWM pairs, (CH0, CH1), (CH2, CH3), with a programmable dead-zone generator each
- Internal 8-bit prescaler and a clock divider for each PWM paired channel
- Independent clock source selection for each PWM channel
- Internal 16-bit down counter and 16-bit comparator for each independent PWM channel
- PWM down-counter supports One-shot or Periodic mode

5.10 Watchdog Timer (WDT)

5.10.1 Overview

The purpose of Watchdog Timer (WDT) is to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake-up system from Idle/Power-down mode.

5.10.2 Features

- 18-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{18}) and the time-out interval is 0.48828125 ms ~ 8 s if WDT_CLK = 32.768 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026、130、18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting WDTON in PWRON register
- Supports WDT time-out wake-up function only if WDT clock source is selected as 32 kHz

5.11 Windowed Watchdog Timer (WWDT)

5.11.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software run to uncontrollable status by any unpredictable condition.

5.11.2 Features

- 6-bit down counter value (CNTDAT) and 6-bit compare value (CMPDAT) to make the WWDT time-out window period flexible.
- Supports 4-bit value (PSCSEL) to programmable maximum 11-bit prescale counter period of WWDT counter.

5.12 Real Time Clock (RTC)

5.12.1 Overview

The Real Time Clock (RTC) controller provides the real time clock and calendar information. The clock source of RTC controller is from an external 32.768 kHz low-speed crystal which connected at pins X32_IN and X32_OUT (refer to pin Description). The RTC controller provides the real time clock (hour, minute, second) in RTC_TIME (RTC Time Loading Register) as well as calendar information (year, month, day) in RTC_CAL (RTC Calendar Loading Register). It also offers RTC alarm function that user can preset the alarm time in RTC_TALM (RTC Time Alarm Register) and alarm calendar in RTC_CALM (RTC Calendar Alarm Register). The data format of RTC time and calendar message are all expressed in BCD (Binary Coded Decimal) format.

The RTC controller supports periodic RTC Time Tick and Alarm Match interrupts. The periodic RTC Time Tick interrupt has 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second which are selected by RTC_TICK (RTC_TICK[2:0] Time Tick Register). When real time and calendar message in RTC_TIME and RTC_CAL are equal to alarm time and calendar settings in RTC_TALM and RTC_CALM, the ALMIF (RTC_INTSTS [0] RTC Alarm Interrupt Flag) is set to 1 and the RTC alarm interrupt signal is generated if the ALMIEN (RTC_INTEN [0] Alarm Interrupt Enable) is enabled.

Both RTC Time Tick and Alarm Match interrupt signal can cause chip to wake-up from Idle or Power-down mode if the corresponding interrupt enable bit (ALMIEN or TICKIEN) is set to 1 before chip enters Idle or Power-down mode.

Real Time Clock (RTC) block can operate with independent power supply (RTC_VDD) while the system power is off.

5.12.2 Features

- Supports real time counter and calendar counter for RTC time and calendar check.
- Supports time (hour, minute, second) and calendar (year, month, day) alarm and alarm mask settings.
- Selectable 12-hour or 24-hour time scale.
- Supports Leap Year indication.
- Supports Day of the Week counter.
- Supports frequency compensation mechanism for 32.768 kHz clock source.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm match interrupt.
- Supports chip wake-up from Idle or Power-down mode while alarm or relative alarm interrupt is generated.
- Supports 64 bytes spare registers to store user's important information.
- Supports power on/off control mechanism to control system core power.

5.13 UART Interface Controller (UART)

This chip equips up to eight channels of Universal Asynchronous Receiver/Transmitters (UART). UART1/6/8 supports High-speed UART and UART0/3/4/9/10 perform Normal Speed UART, besides, all the UART channels support flow control function. The UART controller also supports IrDA (SIR), LIN Master/Slave and RS-485 function modes.

5.13.1 Overview

The Universal Asynchronous Receiver/Transmitter (UART) performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the CPU.

Each UART channel supports seven types of interrupts including (1). Transmitter FIFO empty interrupt (INT_THRE), (2). Receiver threshold level reaching interrupt (INT_RDA), (3). Line status interrupt (parity error or framing error or break interrupt) (INT_RLS), (4). Receiver buffer time-out interrupt (INT_TOUT), (5). MODEM/Wake-up status interrupt (INT_MODEM), (6). Buffer error interrupt (INT_BUF_ERR), and (7). LIN interrupt (INT_LIN).

The UART1/ 6/ 8 is built-in with a 64-byte transmitter FIFO (TX_FIFO) and a 64-byte receiver FIFO (RX_FIFO) that reduces the number of interrupts presented to the CPU and the UART0/ 3/ 4/ 9/ 10 are equipped 16-byte transmitter FIFO (TX_FIFO) and 16-byte receiver FIFO (RX_FIFO). The CPU can read the status of the UART at any time during the operation. The reported status information includes the type and condition of the transfer operations being performed by the UART, as well as 4 error conditions (parity error, framing error, break interrupt and buffer error) probably occur while receiving data.

The UART includes a programmable baud rate generator that is capable of dividing clock input by divisors to produce the serial clock that transmitter and receiver need.

All of the controllers support auto-flow control function that uses two low-level signals, /CTS (clear-to-send) and /RTS (request-to-send), to control the flow of data transfer between the UART and external devices (ex: Modem). When auto-flow is enabled, the UART is not allowed to receive data until the UART asserts /RTS to external device. When the number of bytes in the RX FIFO equals the value of RTS_TRI_LEV (UA_FCR [19:16]), the /RTS is de-asserted. The UART sends data out when UART controller detects /CTS is asserted from external device. If a valid asserted /CTS is not detected the UART controller will not send data out.

The UART controllers also provides Serial IrDA (SIR, Serial Infrared) function (The IrDA mode is selected by setting the (FUN_SEL(UA_FUN_SEL[2:0]) = 010) to select IrDA function). The SIR specification defines a short-range infrared asynchronous serial transmission mode with one start bit, 8 data bits, and 1 stop bit. The maximum data rate is 115.2 Kbps (half duplex). The IrDA SIR block contains an IrDA SIR Protocol encoder/decoder. The IrDA SIR protocol is half-duplex only. So it cannot transmit and receive data at the same time. The IrDA SIR physical layer specifies a minimum 10ms transfer delay between transmission and reception. This delay feature must be implemented by software.

The alternate function of UART controllers is LIN (Local Interconnect Network) function. The LIN mode is selected by setting the (FUN_SEL(UA_FUN_SEL[2:0]) = 001) to select LIN mode. In LIN mode, one start bit and 8-bit data format with 1-bit stop bit are required in accordance with the LIN standard.

For the N9H31 series, another alternate function of UART controllers is RS-485 9-bit mode function, and direction control provided by RTS pin to implement the function by software. The RS-485 mode is selected by setting the (FUN_SEL(UA_FUN_SEL[2:0]) = 011) to select RS-485 function. The RS-485 driver control is implemented using the RTS control signal from an asynchronous serial port to enable the RS-485 driver. In RS-485 mode, many characteristics of the RX and TX are the same as UART.

5.13.2 Features

- Full duplex, asynchronous communications

- Separate receive / transmit 64/16 bytes entry FIFO for data payloads
- Supports hardware auto flow control/flow control function (CTS, RTS) and programmable RTS flow control trigger level
- Programmable receiver buffer trigger level
- Supports programmable baud-rate generator for each channel individually
- Supports CTS wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next start bit by setting DLY(UA_TOR[15:8]) register
- Supports break error, frame error, parity error and receive / transmit buffer overflow detect function
- Fully programmable serial-interface characteristics
- Programmable number of data bit, 5-, 6-, 7-, 8-bit character
- Programmable parity bit, even, odd, no parity or stick parity bit generation and detection
- Programmable stop bit, 1, 1.5, or 2 stop bit generation
- Supports IrDA SIR function mode
- Supports LIN function mode
- Supports RS-485 function mode

5.14 Smart Card Host Interface (SC)

5.14.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal.

5.14.2 Features

- ISO-7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Up to two ISO-7816-3 ports
- Separates receive/transmit 4 byte entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- A 24-bit and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence, hardware warm reset sequence and hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes entry FIFO for data payloads
  - Supports programmable baud rate generator for each channel
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SC_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

5.15 I²C Synchronous Serial Interface Controller (I²C)

5.15.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

Serial, 8-bit oriented bi-directional data transfers can be up to 100 Kbit/s in Standard-mode, 400 Kbit/s in the Fast-mode, or 3.4 Mbit/s in the High-speed mode. Only 100kbps and 400kbps modes are supported directly in this chip.

Data transfer is synchronized to SCL signal between a Master and a Slave with byte-by-byte basis. Each data byte is 8 bits long. There is one SCL clock pulse for each data bit with the MSB being transmitted first. An acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP).

5.15.2 Features

- Compatible with Philips I²C standard, support master mode
- Multi Master Operation.
- Clock stretching and wait state generation.
- Provide multi-byte transmit operation, up to 4 bytes can be transmitted in a single transfer
- Software programmable acknowledge bit.
- Arbitration lost interrupt, with automatic transfer cancellation.
- Start/Stop/Repeated Start/Acknowledge generation.
- Start/Stop/Repeated Start detection.
- Bus busy detection.
- Supports 7 bit addressing mode.
- Fully static synchronous design with one clock domain.
- Software mode I²C.

5.16 SPI Interface Controller (SPI)

5.16.1 Overview

The SPI is a synchronous serial interface performs a serial-to-parallel conversion on data characters received from the peripheral, and a parallel-to-serial conversion on data characters received from CPU. This interface can drive up to 2 external peripherals and is seen as the master.

5.16.2 Features

- Support master mode
- Full duplex synchronous serial data transfer
- Variable length of transfer word up to 32 bits
- Provide burst mode operation, transmit/receive can be executed up to four times in one transfer
- MSB or LSB first data transfer
- Rx and Tx on both rising or falling edge of serial clock independently
- Support 2 slave/device select lines
- Support dual IO and quad mode for SPI Flash access

5.17 I²S Controller (I²S)

5.17.1 Overview

The I²S controller consists of I²S and PCM protocols to interface with external audio CODEC. The I²S and PCM interface supports 8, 16, 18, 20 and 24-bit left/right precision in record and playback. When operating in 18/20/24-bit precision, each left/right-channel sample is stored in a 32-bit word. Each left/right-channel sample has 24/20/18 MSB bits of valid data and other LSB bits are the padding zeros. When operating in 16-bit precision, right-channel sample is stored in MSB of a 32-bit word and left-channel sample is stored in LSB of a 32-bit word.

The following are the property of the DMA.

- When 16-bit precision, the DMA always 8-beat incrementing burst (FIFO_TH = 0) or 4-beat incrementing burst (FIFO_TH = 1).
- When 24/20/18-bit precision, the DMA always 16-beat incrementing burst (FIFO_TH = 0) or 8-beat incrementing burst (FIFO_TH = 1).
- Always bus lock when 4-beat or 8-beat or 16-beat incrementing burst.
- When reach eighth, quarter, middle and end address of destination address, a DMA_IRQ is triggered to CPU automatically.

An AHB master port and an AHB slave port are offered in I²S controller.

5.17.2 Features

- Support I²S interface record and playback
  - Left/right channel
  - 8, 16, 20, 24-bit data precision
  - Mater and slave mode
- Support PCM interface record and playback
  - Two slots
  - 8, 16, 20, 24-bit data precision
  - Master mode
- Use DMA to playback and record data, with interrupt
- Support two addresses for left/right channel data and different slots

5.18 Ethernet MAC Controller (EMAC)

5.18.1 Overview

This chip provides 1 Ethernet MAC Controller (EMAC) for Network application.

The Ethernet MAC controller consists of IEEE 802.3/Ethernet protocol engine with internal CAM function for recognizing Ethernet MAC addresses; Transmit-FIFO, Receive-FIFO, TX/RX state machine controller, time stamping engine for IEEE 1588, Magic Packet parsing engine and status controller.

The EMAC supports RMII (Reduced MII) interface to connect with external Ethernet PHY.

5.18.2 Features

- Supports IEEE Std. 802.3 CSMA/CD protocol
- Supports Ethernet frame time stamping for IEEE Std. 1588 – 2002 protocol
- Supports both half and full duplex for 10 Mbps or 100 Mbps operation
- Supports RMII interface
- Supports MII Management function to control external Ethernet PHY
- Supports pause and remote pause function for flow control
- Supports long frame (more than 1518 bytes) and short frame (less than 64 bytes) reception
- Supports 16 entries CAM function for Ethernet MAC address recognition
- Supports Magic Packet recognition to wake system up from power-down mode
- Supports 256 bytes transmit FIFO and 256 bytes receive FIFO
- Supports DMA function

5.19 USB 2.0 Device Controller (USBD)

5.19.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is complaint with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

5.19.2 Features

- USB Specification reversion 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- 4096 Bytes Configurable RAM used as endpoint buffer
- Supports Endpoint Maximum Packet Size up to 1024 bytes

5.20 USB Host Controller (USBH)

5.20.1 Overview

The Universal Serial Bus (USB) is a fast, bi-directional, isochronous, low-cost, dynamically attachable serial interface standard intended for modem, scanners, PDAs, keyboards, mice, and digital imaging devices. The USB is a 4-wire serial cable bus that supports serial data exchange between a Host Controller and a network of peripheral devices. The attached peripherals share USB bandwidth through a host-scheduled, token-based protocol. Peripherals may be attached, configured, used, and detached, while the host and other peripherals continue operation (i.e. hot plug and unplug is supported).

5.20.2 Features

- Fully compliant with USB Revision 2.0 specification.
- Enhanced Host Controller Interface (EHCI) Revision 1.0 compatible.
- Open Host Controller Interface (OHCI) Revision 1.0 compatible.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Integrated a port routing logic to route full/low speed device to OHCI controller.
- Built-in DMA for real-time data transfer.

5.21 Controller Area Network (CAN)

5.21.1 Overview

The C_CAN consists of the CAN Core, Message RAM, Message Handler, Control Registers and Module Interface. The CAN Core performs communication according to the CAN protocol version 2.0 part A and B. The bit rate can be programmed to values up to 1Mbit/s. For the connection to the physical layer, additional transceiver hardware is required.

For communication on a CAN network, individual Message Objects are configured. The Message Objects and Identifier Masks for acceptance filtering of received messages are stored in the Message RAM. All functions concerning the handling of messages are implemented in the Message Handler. These functions include acceptance filtering, the transfer of messages between the CAN Core and the Message RAM, and the handling of transmission requests as well as the generation of the module interrupt.

The register set of the C_CAN can be accessed directly by the software through the module interface. These registers are used to control/configure the CAN Core and the Message Handler and to access the Message RAM.

5.22 Flash Memory Interface (FMI)

5.22.1 Overview

The Flash Memory Interface (FMI) of this Chip has DMA unit and FMI unit. The DMA unit provides a DMA (Direct Memory Access) function for FMI to exchange data between system memory (I SDRAM) and shared buffer (128 bytes), and the FMI unit control the interface of eMMC or NAND Flash. The interface controller can support eMMC and NAND-type Flash and the FMI is cooperated with DMAC to provide a fast data transfer between system memory and cards.

5.22.2 Features

- Support single DMA channel and address in non-word boundary.
- Support hardware Scatter-Gather function.
- Support 128Bytes shared buffer for data exchange between system memory and Flash device. (Separate into two 64 bytes ping-pong FIFO).
- Support eMMC Flash device.
- Supports SLC and MLC NAND type Flash.
- Adjustable NAND page sizes. (512B+spare area, 2048B+spare area, 4096B+spare area and 8192B+spare area).
- Support up to 4bit/8bit/12bit/15bit/24bit hardware ECC calculation circuit to protect data communication.
- Support programmable NAND timing cycle.

5.23 Secure Digital Host Controller (SDH)

5.23.1 Overview

The Secure-Digital Card Host Controller (SDH) equips DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC/SDIO. The SDH controller supports SD/SDHC/SDIO card and cooperates with DMAC to provide a fast data transfer between system memory and cards.

5.23.2 Features

- Supports single DMA channel
- Supports hardware Scatter-Gather functionality.
- Supports 128 Bytes shared buffer for data exchange between system memory and cards.
- Supports SD, SDHC and SDIO card.

5.24 2D Graphic Engine (GE2D)

5.24.1 Overview

A 32-bit 2D Graphics Engine (GE2D) is specially designed to improve the performance of graphic processing. It can accelerate the operation of individual GUI functions such as BitBLTs and Bresenham Line Draw to operate at all pixel depths including 8/16/32 bit-per-pixel.

A pixel is the smallest addressable screen element as defined in Microsoft Windows, and lines and pictures are made up by a variety of pixels. GE2D is used to speed up graphic performance in pixel data moving and line drawing, as well as to accelerate almost all computer graphic Boolean operations by eliminating the CPU overhead. Meanwhile, the functions of rotation and scaling down are implemented for some special applications. In image scaling down function, both programmable horizontal and vertical N/M scaling down factors are provided for resizing the image. For the 2D rotation, it can rotate left or right 45, 90 or 180 degrees, and also supports the flip/flop, mirror or up-side-down pictures.

5.24.2 Features

- Support 2D Bit Block Transfer (BitBLT) functions defined in Microsoft GDI
- Support Host BLT
- Support Pattern BLT
- Support Color/Font Expanding BLT
- Support Transparent BLT
- Support Tile BLT
- Support Block Move BLT
- Support Copy File BLT
- Support Color/Font Expansion
- Support Rectangle Fill
- Support RGB332/RGB565/RGB888 data format.
- Support fore/background colors and all Microsoft 256 ternary raster-operation codes (ROP)
- Support both inside and outside clipping function
- Support alpha-blending for source/destination picture overlaying
- Support fast Bresenham line drawing algorithm to draw solid/textured line
- Support rectangular border and frame drawing
- Support picture re-sizing
- Support down-scaling from 1/255 to 254/255
- Support up-scaling from 1 to 1.996 (1+254/255)
- Support object rotation with different degree
- Support L45 (45 degree left rotation) and L90 (90 degree left rotation)
- Support R45 (45 degree right rotation) and R90 (90 degree right rotation)
- Support M180 (mirror/flop)
- Support F180 (up-side-down (flip) and X180 (180 degree rotation)

5.25 JPEG Codec (JPEG)

5.25.1 Overview

The JPEG Codec supports Baseline Sequential Mode JPEG still image compression and decompression that is fully compliant with ISO/IEC International Standard 10918-1 (T.81). The features and capability of the JPEG codec are listed below.

5.25.2 Features

If image data input or output by planar format (PLANAR_ON (JITCR[15])= 1), the features are as following:

- Support to encode interleaved YcbCr 4:2:2/4:2:0 and gray-level (Y only) format image
- Support to decode interleaved YcbCr 4:4:4/4:2:2/4:2:0/4:1:1 and gray-level (Y only) format image
- Support to decode YcbCr 4:2:2 transpose format
- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode (up to 8192x8192)
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function for encode and decode modes(Thumbnail/Primary)
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode
- Support rotate function in encode mode

If image data input or output by packet format (PLANAR_ON (JITCR[15])= 0), the feature are as following:

- Support to encode interleaved YUYV format input image, output bitstream 4:2:2 and 4:2:0 format
- Support to decode interleaved YcbCr 4:4:4/4:2:2/4:2:0 format image
- Support decoded output image YUYV422, RGB555, RGB565, RGB888 format (ORDER= 1).
- The encoded JPEG bit-stream format is fully compatible with JFIF and EXIF standards
- Support arbitrary width and height image encode and decode(Primary Only)
- Support three programmable quantization-tables
- Support standard default Huffman-table and programmable Huffman-table for decode
- Support arbitrarily 1X~8X image up-scaling function for encode mode
- Support down-scaling function 1X~ 16X for Y422 and Y420, 1X~ 8X for Y444 for decode mode
- Support specified window decode mode
- Support quantization-table adjustment for bit-rate and quality control in encode mode

5.26 LCD Display Interface Controller (LCM)

5.26.1 Overview

The main purpose of Display Controller is used to display the video/image data to LCD device or connect with external TV-encoder. The video/image data source may come from the image sensor, JPEG decoder and the OSD pattern which have been stored in system memory (SDRAM). The input data format of the display controller can be packet YUV422, packet YUV444, packet RGB444, packet RGB565, packet RGB666, and packet RGB888. The OSD (On Screen Display) function supports packet YUV422 and 8/16/24-bit direct-color mode. The LCD controller supports both sync-type and MPU-type LCDM. This LCD Controller is a bus master and can transfer display data from system memory (SDRAM) without CPU intervention.

5.26.2 Features

- Input data format
  - YUV422, YUV444
  - RGB444, RGB565, RGB666, RGB888
- Output format
  - YUV422, YUV444
  - RGB444, RGB565, RGB666, RGB888
- Input size: Maximum size 1024 * 768
- Image resize
  - Horizontal up-scaling 1~8X in fractional steps
  - Vertical up-scaling 1~8X in fractional steps
- Convert full range YUV to CCIR601
- Windowing support for three OSD graphic or text overlay
- Support CCIR-656 (with header), CCIR-601(with hsync and vsync) 8/16-bit YUV data output format to connect with external TV encoder
- Support both sync-type and MPU-type LCM
- Support the 8/9/16/18/24-bit data output to connect with 80/68 series MPU type LCM module

The LCD Controller includes the following main functions：

- Video post-processing
- Display & overlay control
- Video output control
- Hardware cursor control

5.27 Capture Sensor Interface Controller (CAP)

5.27.1 Overview

The Image Capture Interface is designed to capture image data from a sensor. After capturing or fetching image data, it will process the image data, and then FIFO output them into frame buffer.

5.27.2 Feature

- 8-bit RGB565 sensor
- 8-bit YUV422 sensor
- Supports CCIR601 YcbCr color range scale to full YUV color range
- Supports 4 packaging format for packet data output: YUYV, Y only, RGB565, RGB555
- Supports YUV422 planar data output
- Supports the CROP function to crop input image to the required size for digital application.
- Supports the down scaling function to scale input image to the required size for digital application.
- Supports frame rate control
- Supports field detection and even/odd field skip mechanism
- Supports packet output dual buffer control through hardware buffer controller
- Supports negative/sepia/posterization color effect

5.28 Analog to Digital Converter (ADC)

5.28.1 Overview

The NuMicro™ N9H31 series contains one 12-bit Successive Approximation Register analog-to-digital converter (SAR A/D converter) with four input channels. The A/D converter supports 4-wire mode. The ADC is especially suitable to act as touch screen controller. Battery voltage detection could be easily accomplished by the SAR ADC. It has keypad interrupt signal generator.

5.28.2 Features

- Resolution: 12-bit resolution.
- DNL: +/-1.5 LSB, INL: +/-3 LSB.
- Dual Data Rates: 160K SPS.
- Analog Input Range: VREF to AGND, could be rail-to-rail.
- Analog Supply: 2.7-3.6V.
- Digital Supply: 1.2V.
- 4 Single-Ended Analog inputs.
- Compatible with 4-wire Touch Screen Interface.
- Touch Pressure Measurement for 4-wire touch screen application.
- Direct Battery Measurement.
- Keypad Interrupt Generator.
- Auto Power Down.
- Low Power Consumption: 2170uW(@160k SPS), < 1uA

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN.	MAX	UNIT
V_{CORE_VDD}–V_{CORE_VSS}	Core DC Power Supply	-0.3	+1.26	V
V_{IO_VDD}–V_{IO_VSS}	I/O DC Power Supply	-0.3	+3.63	V
V_{DDR_VDD}–V_{DDR_VSS}	DDR I/O DC Power Supply	-0.3	+1.90	V
V_{IN}	Input Voltage	V_{IO_VSS}-0.3	+3.6	V
$1/t_{CLCL}$	Oscillator Frequency	4	24	MHz
T_A	Operating Temperature	-40	+85	°C
T_{ST}	Storage Temperature	-55	+150	°C
I_{DD}	Maximum Current into CORE_VDD	-	200	mA
I_{SS}	Maximum Current out of CORE_VSS	-	200	mA
I_{IO}	Maximum Current sunk by a I/O pin	-	20	mA
	Maximum Current sourced by a I/O pin	-	30	mA
	Maximum Current sunk by total I/O pins	-	200	mA
	Maximum Current sourced by total I/O pins	-	200	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

Table 6.1-1 Absolute Maximum Ratings

6.2 DC Electrical Characteristics

6.2.1 N9H31 Series DC Electrical Characteristics

(VDD-VSS=3.3 V, TA = 25°C, FOSC = 12 MHz unless otherwise specified.)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Core Operation voltage	V_{CORE_VDD}	1.14	1.2	1.26	V	
I/O Operation Voltage	V_{IO_VDD}	2.97	3.3	3.63	V	
DDR I/O Operation Voltage	V_{DDR_VDD}	1.70	1.8	1.90	V	
PLL Operation Voltage	V_{PLL_VDD}	1.14	1.2	1.26	V	
USB Operation Voltage (1)	$V_{USBPLL0_VDD}$ $V_{USBPLL1_VDD}$	1.14	1.2	1.26	V	
USB Operation Voltage (2)	V_{USB0_VDD} V_{USB1_VDD}	2.97	3.3	3.63	V	
RTC Operation Voltage	V_{RTC_VDD}	2.0	3.3	3.63	V	
Power Ground	Core_V_{SS} IO_V_{SS} DDR_V_{SS} USB0_V_{SS} USB1_V_{SS} AV_{SS}	-0.3			V	
Analog Operating Voltage	AV_{DD}	2.97	3.3	3.63	V	
Analog Reference Voltage	Vref	0		AV_{DD}	V	
Current Consumption of Normal Operating Mode 1	I_{CORE_VDD1}		185		mA	Frequency of CPUCLK/DDR_CLK is 300/150 MHz. The functionalities enabled are GE2D, LCD, JPEG, graphic Engine, EMAC, USBD, USBH and UART. Note. $I_{USBPLL_VDD1} = I_{USBPLL0_VDD1} + I_{USBPLL1_VDD1}$
	I_{DDR_VDD1}		40		mA	
	I_{USBPLL_VDD1}		15		mA	
	I_{USB0_VDD1}		35		mA	
	I_{USB1_VDD1}		35		mA	
	I_{RTC_VDD1}		100		uA	
Current Consumption of Normal Operating Mode 2	I_{CORE_VDD2}		165		mA	Frequency of CPUCLK/DDR_CLK is 264/132 MHz. The functionalities enabled are GE2D, LCD, JPEG, graphic Engine, EMAC, USBD, USBH and UART. Note. $I_{USBPLL_VDD2} = I_{USBPLL0_VDD2} + I_{USBPLL1_VDD2}$
	I_{DDR_VDD2}		35		mA	
	I_{USBPLL_VDD2}		15		mA	
	I_{USB0_VDD2}		35		mA	
	I_{USB1_VDD2}		35		mA	
	I_{RTC_VDD2}		100		uA	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Current Consumption of Deep Standby Mode	$I_{STDBY_CORE_VDD}$		3		mA	V_{CORE_VDD} = 1.2V
	$I_{STDBY_DDR_VDD}$		6		mA	V_{DDR_VDD} = 1.8V
	$I_{STDBY_IO_VDD}$		5		μA	V_{IO_VDD} = 3.3V
	$I_{STDBY_USB0_VDD}$		0		μA	V_{USB0_VDD} = 3.3V
	$I_{STDBY_USB1_VDD}$		0		μA	V_{USB1_VDD} = 3.3V
	$I_{STDBY_UPLL0_VDD}$		5		μA	$V_{USBPLL0_VDD}$ = 1.2V
	$I_{STDBY_UPLL1_VDD}$		5		μA	$V_{USBPLL1_VDD}$ = 1.2V
	I_{STDBY_AVDD}		25		μA	V_{AVDD} = 3.3V
	$I_{STDBY_RTC_VDD}$		100		μA	V_{RTC_VDD} = 3.3V
Current Consumption of Power Down Mode	$I_{PWD_RTC_VDD}$		7		uA	V_{RTC_VDD} = 3.0V
Input Leakage Current PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ	I_{LK1}	-10	-	10	μA	V_{IO_VDD} = 3.63V 0V < V_{IN} < 3.6V
Input Leakage Current with Pull-Down Resistor on PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ	I_{LK2}	40	-	160	μA	V_{IN} = V_{IO_VDD}
Input Leakage Current with Pull-Up Resistor on PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ	I_{LK3}	-160	-	40	μA	V_{IN} = 0
Input Low Voltage PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (TTL input)	V_{IL1}	-	-	0.8	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (TTL input)	V_{IH1}	2.0	-	-	V	
Input Low Voltage PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (Schmitt input)	V_{IL2}	0.9	1.05	1.2	V	
Input High Voltage PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (Schmitt input)	V_{IH2}	1.65	1.9	2.1	V	
Hysteresis voltage PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (Schmitt input)	V_{HY}	0.75	0.85	0.9	V	
Negative going threshold (Schmitt input), nRESET	V_{ILS}	0.75	-	0.9	V	
Positive going threshold (Schmitt input), nRESET	V_{IHS}	1.65	-	2.1	V	

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Source Current PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (Push-pull Mode)	I_{SR21}	8	-	28	mA	
Sink Current PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ (Push-pull Mode)	I_{SK1}	8	-	18	mA	
Input Pull-up Resistance PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ	R_{PU}	45	53	82	kΩ	V_{IN} = 0
Input Pull-down Resistance PA, PB, PC, PD, PE, PF, PG, PH, PI, PJ	R_{PD}	37	49	91	kΩ	V_{IN} = V_{IO_VDD}
Input Pull-up Resistance nRESET	R_{RST}	45	53	85	kΩ	

Note:

1. nRESET pin is a Schmitt trigger input.

2. Pins of PA, PB, PC, PD, PE, PF, PG, PH, PI and PJ can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=3.63 V, the transition current reaches its maximum value when V_{IN} approximates to 1.5 V.

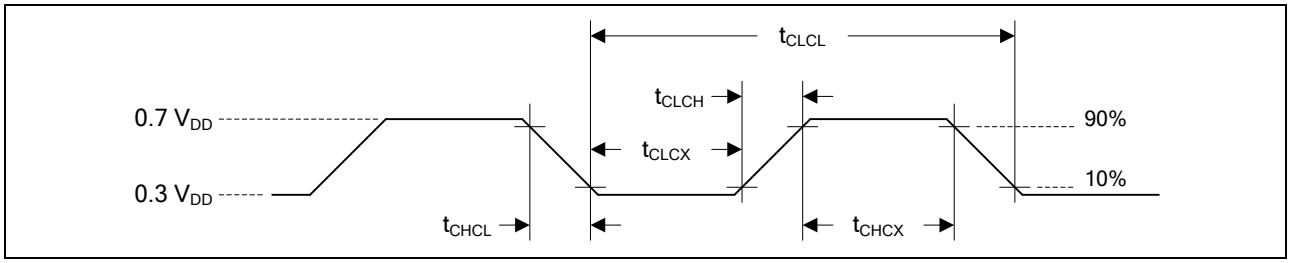
Table 6.2-1 DC Electrical Characteristics

6.3 AC Electrical Characteristics

6.3.1 External 12 MHz High Speed Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
t_{CHCX}	Clock High Time	20	-	-	ns	-
t_{CLCX}	Clock Low Time	20	-	-	ns	-
t_{CLCH}	Clock Rise Time	-	-	10	ns	-
t_{CHCL}	Clock Fall Time	-	-	10	ns	-

Table 6.3-1 External 12 MHz High Speed Oscillator Electrical Characteristics



Note: Duty cycle is 50%.

Figure 6.3-1 External 12 MHz High Speed Oscillator Timing Diagram

6.3.2 Power-on Sequence & RESET

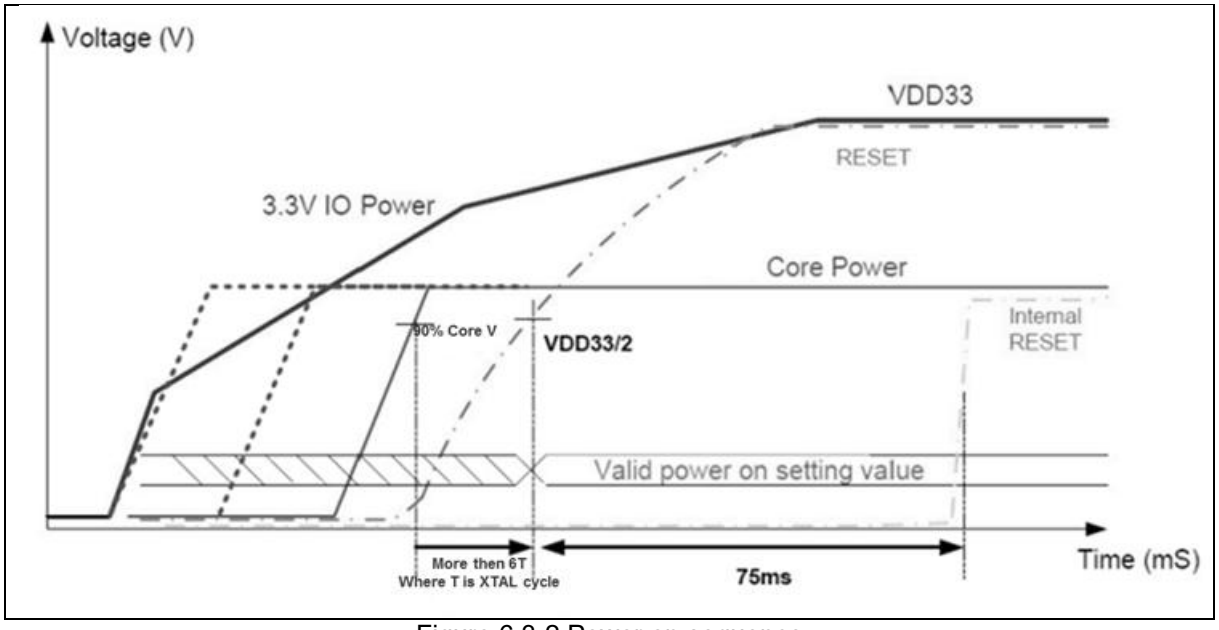


Figure 6.3-2 Power on sequence

6.3.2.1 Power up Sequence

- Higher Voltage (3.3V) First
- Sequence: T33 ≥ T18 ≥ T12, (The time delay gap between < 1mS is prefer, typical 0mS is recommend)

6.3.2.2 Power down Sequence,

- The lower voltage (1.2V) should be powered down first and then the higher one (3.3V)
- Sequence: T12 ≥ T18 ≥ T33

Note.

- T12 represents 1.2V powered time for Core power
- T18 represents 1.8V powered time for MVDD power
- T33 represents 3.3V powered time for I/O power

6.3.3 External 12 MHz High Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{HXT}	Operation Voltage	2.97	3.3	3.63	V	-
T_A	Temperature	-40	-	85	°C	-
f_{HXT}	Clock Frequency	4	-	24	MHz	-

6.3.3.1 Typical Crystal Application Circuits

Crystal	ESR (ohm)	C1, C2
12 MHz	< 50	14 pf

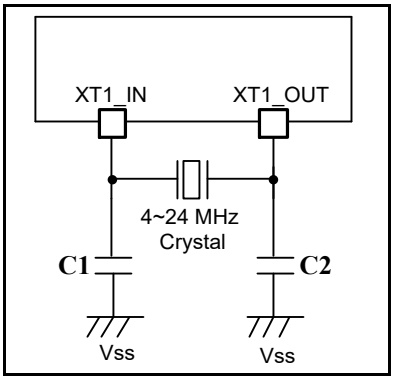


Figure 6.3-3 Typical HXT Crystal Application Circuit

6.3.4 External 32.768 kHz Low Speed Crystal

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{LXT}	Operation Voltage	2.97	3.3	3.63	V	-
T_A	Temperature	-40	-	85	°C	-
f_{LXT}	Clock Frequency	-	32.768	-	kHz	-

6.3.4.1 Typical Crystal Application Circuits

Crystal	C1	C2
32.768 kHz	20pf	20pf

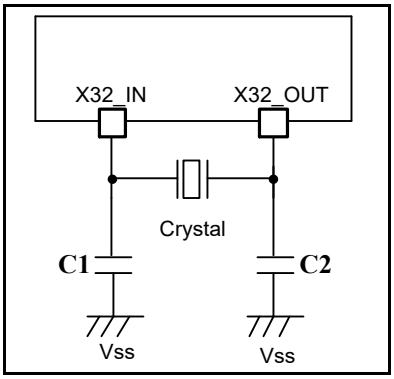


Figure 6.3-4 Typical LXT Crystal Application Circuit

6.3.5 I²C Interface Timing

Symbol	Parameter	100K		400K		Unit	Test Condition
		Min	Max	Min	Max		
T_{LOW}	I2C_SCL Low Period	4.7	-	1.2	-	us	-
T_{HIGH}	I2C_SCL High Period	4	-	0.6	-	us	-
T_{SU_STA}	Repeated START Condition Setup Time	4.7	-	1.2	-	us	-
T_{HD_STA}	START Condition Hold Time	4	-	0.6	-	us	-
T_{SU_STO}	STOP Condition Setup Time	4	-	0.6	-	us	-
T_{BUF}	Bus Free Time	4.7	-	1.2	-	us	-
T_{SU_DAT}	Data Setup Time	2	-	0.3	-	us	-
T_{HD_DAT}	Data Hold Time	0	4.2	0	0.8	us	-
T_R	I2C_SCL/I2C_SDA Rise Time	-	1000	20+0.1Cb	300	ns	-
T_F	I2C_SCL/I2C_SDA Fall Time	-	300	-	300	ns	-
C_b	Capacitive Load for Each Bus Line	-	400	-	400	pF	-

Table 6.3-2 I²C Interface Timing

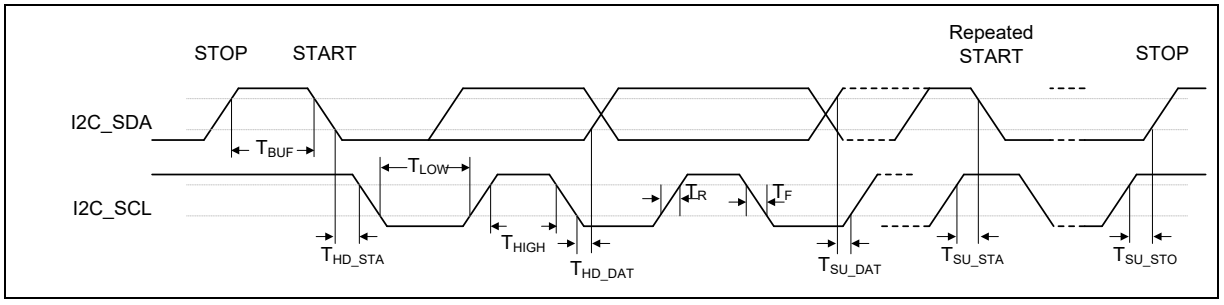


Figure 6.3-5 I²C Interface Timing Diagram

6.3.6 SPI Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SPI_CLK}$	SPI_CLK Period	56	-	-	ns	-
$T_{H_SPI_CLK}$	SPI_CLK High Time	28	-	-	ns	-
$T_{L_SPI_CLK}$	SPI_CLK Low Time	28	-	-	ns	-
$T_{SU_SPI_DI}$	SPI_DI or SPI_DATA[3:0] Setup Time to SPI_CLK Active Edge	11	-	-	ns	-
$T_{HD_SPI_DI}$	SPI_DI or SPI_DATA[3:0] Hold Time from SPI_CLK Active Edge	1	-	-	ns	-
$T_{DLY_SPI_DO}$	SPI_CLK Active Edge to Valid SPI_DO or SPI_DATA[3:0] Delay	-	-	4	ns	-
$T_{HD_SPI_DO}$	SPI_DO or SPI_DATA[3:0] Hold Time from SPI_CLK Active Edge	0.2			ns	

Table 6.3-3 SPI Interface Timing

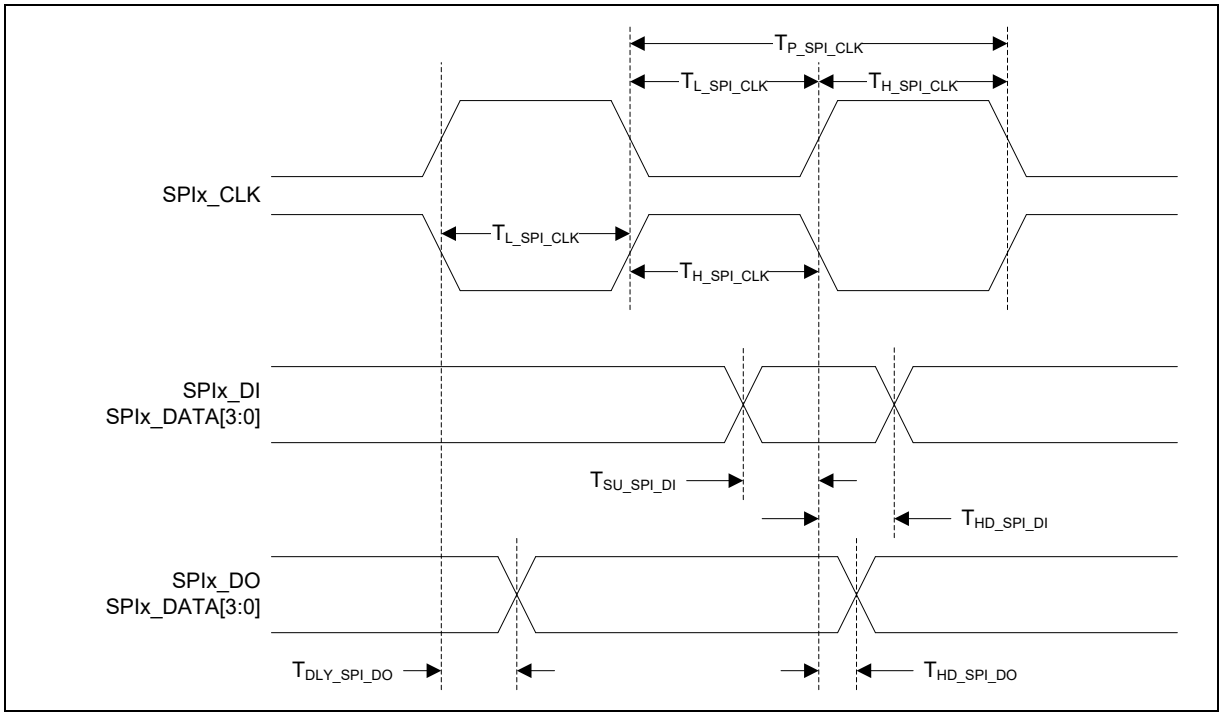


Figure 6.3-6 SPI Interface Timing Diagram

6.3.7 I²S Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_I2S_BITCLK}$	I2S_BITCLK Period	50	-	-	ns	-
$T_{H_I2S_BITCLK}$	I2S_BITCLK High Time	25	-	-	ns	-
$T_{L_I2S_BITCLK}$	I2S_BITCLK Low Time	25	-	-	ns	-
$T_{DLY_I2S_DO}$	I2S_BITCLK Rising to Valid I2S_WS or I2S_DATAO Delay	-	-	6	ns	-
$T_{HD_I2S_DO}$	I2S_WS or I2S_DATAO Hold Time from I2S_BITCLK Rising	1	-	-	ns	
$T_{SU_I2S_DI}$	I2S_DATAI Setup Time to I2S_BITCLK Rising	5	-	-	ns	-
$T_{HD_I2S_DI}$	I2S_DATAI Hold Time from I2S_BITCLK Rising	3	-	-	Ns	-

Table 6.3-4 I²S Interface Timing

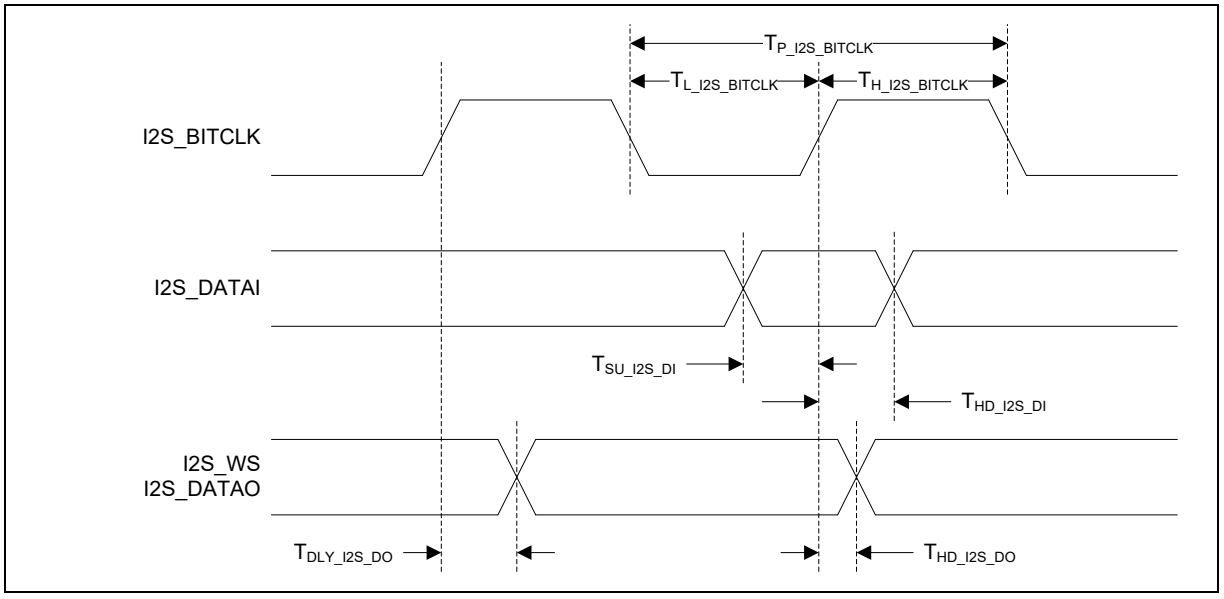


Figure 6.3-7 I²S Interface Timing Diagram

6.3.8 Ethernet Interface Timing

6.3.8.1 RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_RMII_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H_RMII_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L_RMII_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY_RMII_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	10	ns	-
$T_{SU_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD_RMII_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

Table 6.3-5 RMII Interface Timing

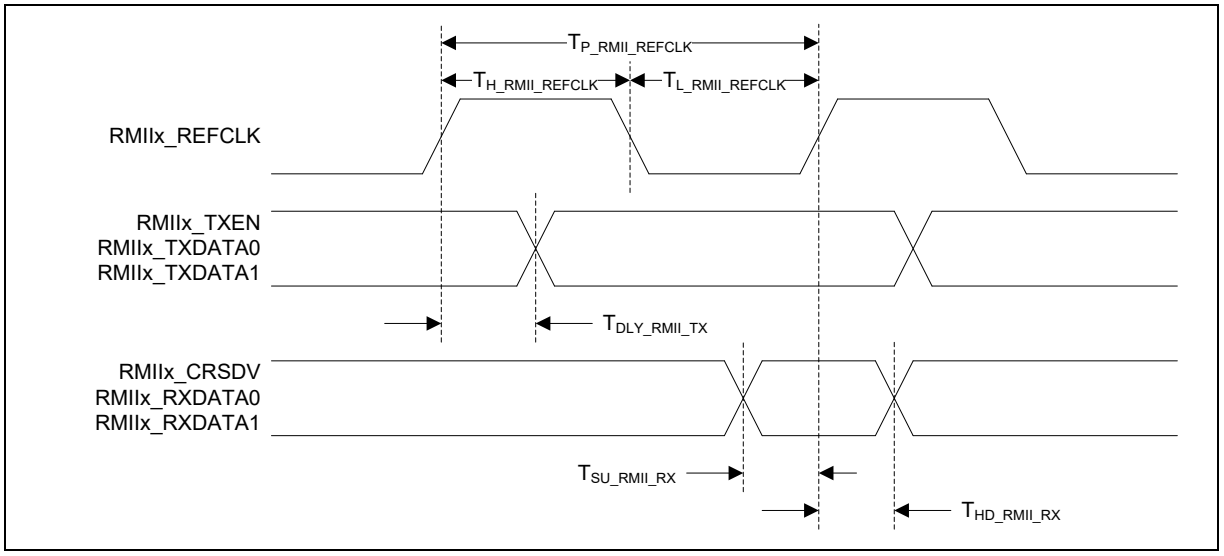


Figure 6.3-8 RMII Interface Timing Diagram

6.3.8.2 Ethernet PHY Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_RMII_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H_RMII_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L_RMII_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY_RMII_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU_RMII_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD_RMII_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

Table 6.3-6 Ethernet PHY Management Interface Timing

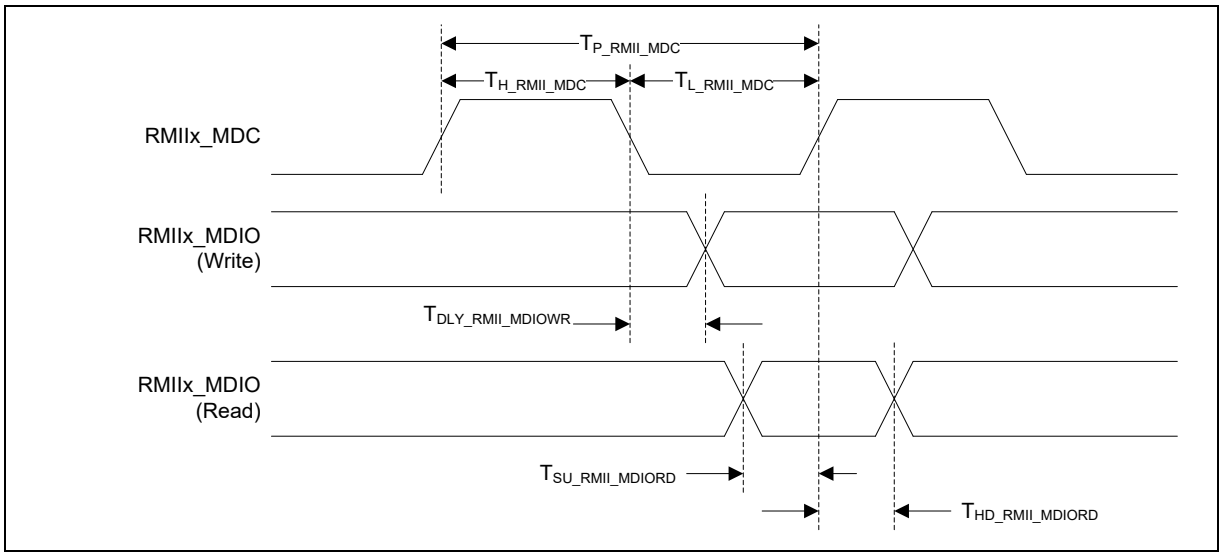


Figure 6.3-9 Ethernet PHY Management Interface Timing Diagram

6.3.9 NAND Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{H_NAND_nWE}$	NAND_nWE High Time	-	15[1]	-	Ns	-
$T_{L_NAND_nWE}$	NAND_nWE Low Time	-	45[2]	-	ns	-
$T_{DLY_DATA_OUT}$	NAND_nWE Falling to Valid NAND_DATA Delay	-	15[3]-		ns	-
$T_{HD_DATA_OUT}$	NAND_DATA Hold Time from NAND_nWE Rising	7.5[3]	-	-	Ns	-
$T_{SU_DATA_IN}$	NAND_DATA Setup Time to NAND_nRE Rising	15[3]	-	-	ns	-
$T_{HD_DATA_IN}$	NAND_DATA Hold Time from NAND_nRE Rising	7.5[3]	-	-	ns	-

Note 1: NAND controller operating clock is 132 MHz and HI_WID (FMI_NANDTMCTL[15:8]) is 0x1.

Note 2: NAND controller operating clock is 132 MHz and LO_WID (FMI_NANDTMCTL[7:0]) is 0x5.

Note 2: NAND controller operating clock is 132 MHz

Table 6.3-7 NAND Interface Timing

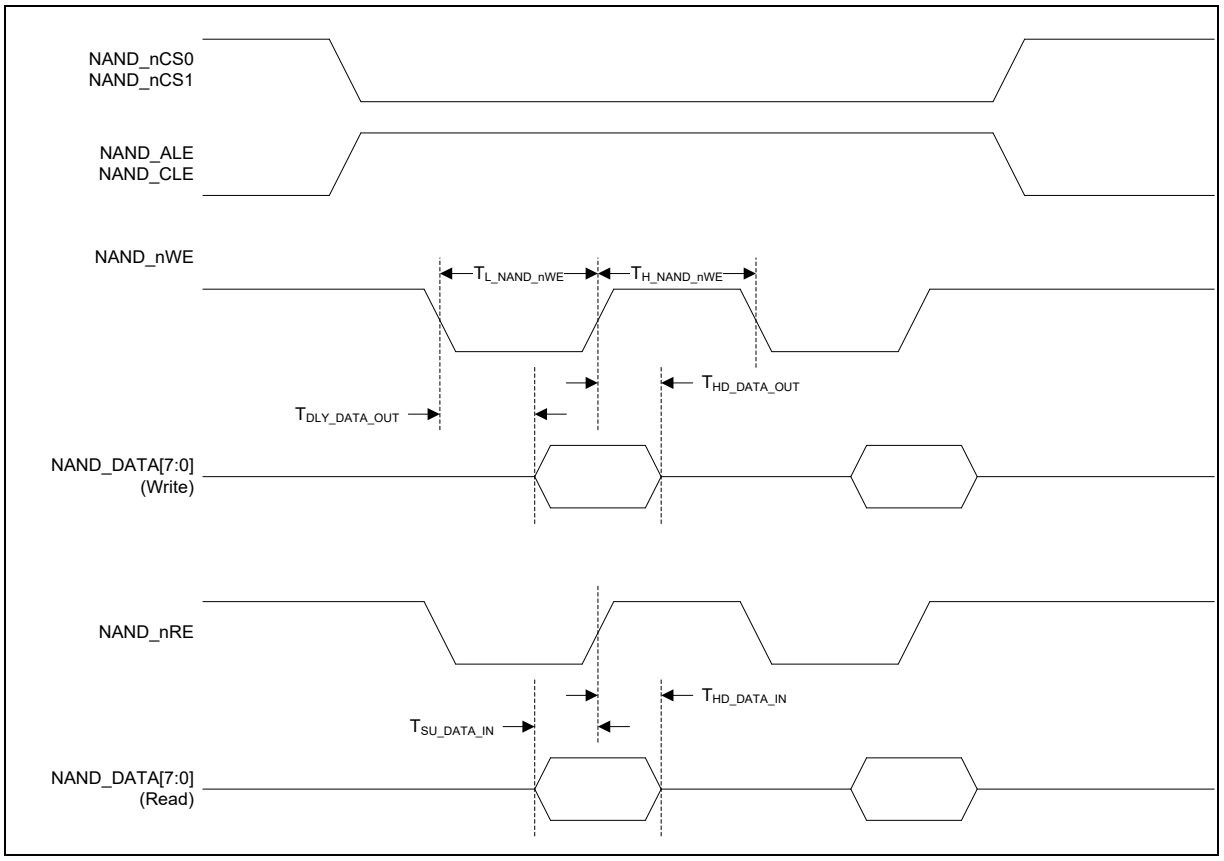


Figure 6.3-10 NAND Interface Timing Diagram

6.3.10 SD Interface Timing

6.3.10.1 Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P_SD_CLK_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H_SD_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Table 6.3-8 SD Interface Default Mode Timing

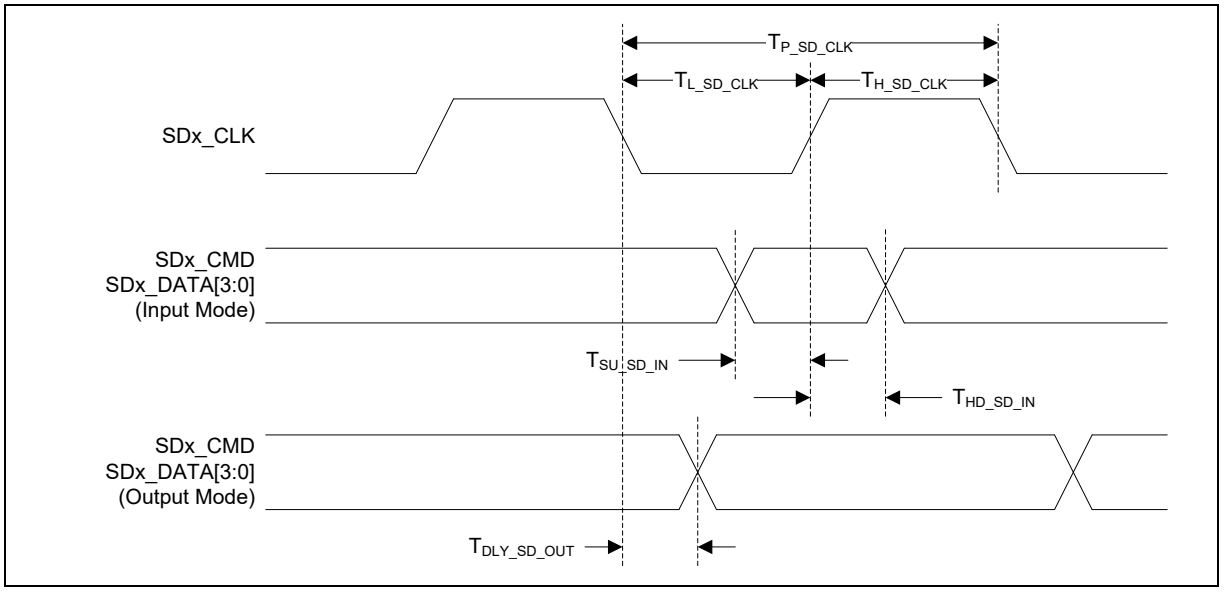


Figure 6.3-11 SD Interface Default Mode Timing Diagram

6.3.10.2 High-Speed Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_SD_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H_SD_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L_SD_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU_SD_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD_SD_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY_SD_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD_SD_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Table 6.3-9 SD Interface High-Speed Mode Timing

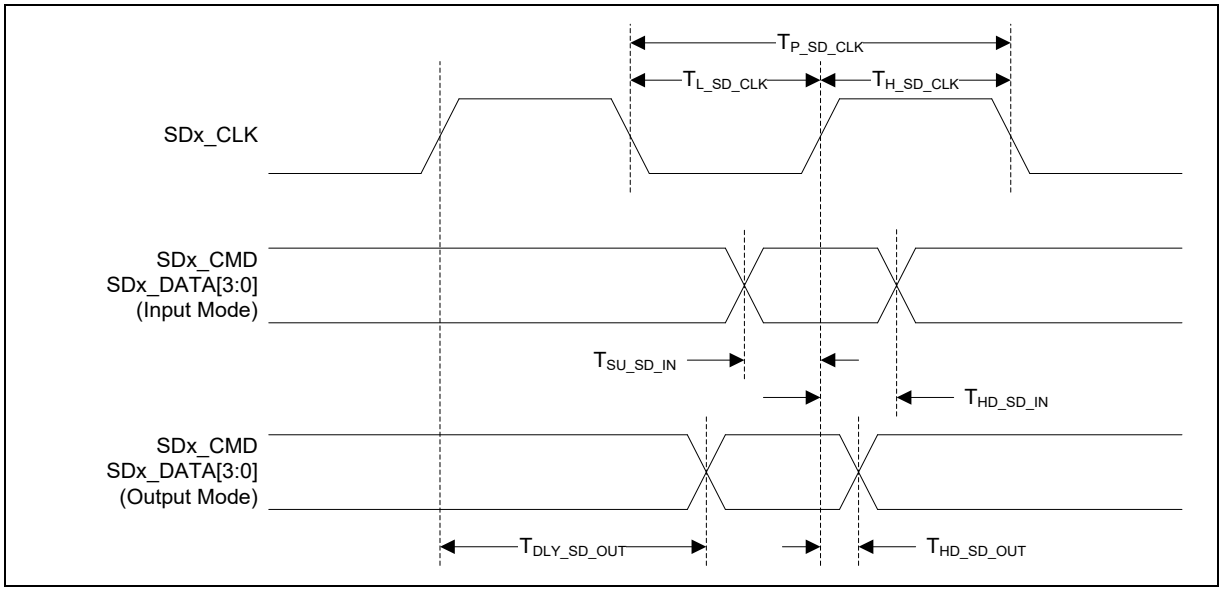


Figure 6.3-12 SD Interface High-Speed Mode Timing Diagram

6.3.11 LCD Display Interface Timing

6.3.11.1 SYNC Type Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_LCD_CLK}$	LCD_CLK Period	13	-	-	ns	-
$T_{H_LCD_CLK}$	LCD_CLK High Time	6.5	-	-	ns	-
$T_{L_LCD_CLK}$	LCD_CLK Low Time	6.5	-	-	ns	-
$T_{DLY_LCD_OUT}$	LCD_CLK Rising to Valid LCD_HSYNC, LCD_VSYNC, LCD_DEN and LCD_DATA Delay	-	-	6	ns	-
$T_{HD_LCD_OUT}$	LCD_HSYNC, LCD_VSYNC, LCD_DEN and LCD_DATA Hold Time from LCD_CLK Rising	1	-	-	ns	-

Table 6.3-10 LCD Display Interface SYNC Type Timing

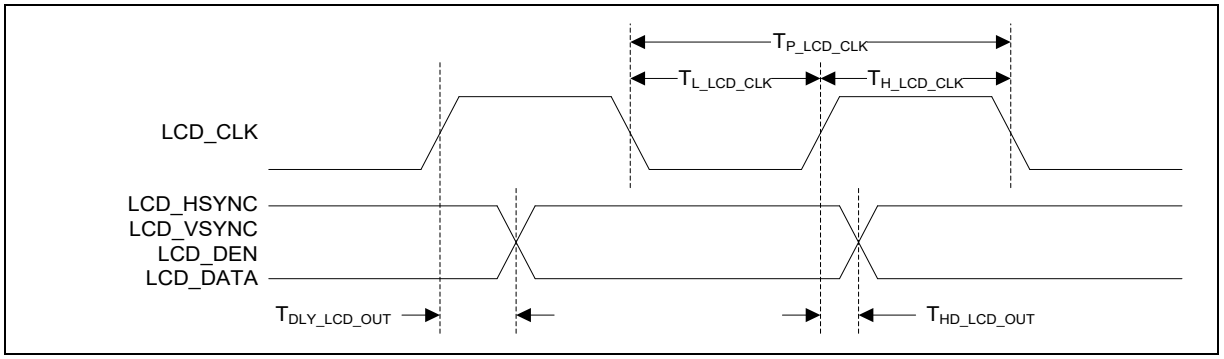


Figure 6.3-13 LCD Display Interface SYNC Type Timing Diagram

6.3.12 Capture Sensor Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P_VCAP_PCLK}$	VCAP_PCLK Period	20	-	-	ns	-
$T_{H_VCAP_PCLK}$	VCAP_PCLK High Time	-	10.0	-	ns	-
$T_{L_VCAP_PCLK}$	VCAP_PCLK Low Time	-	10.0	-	ns	-
$T_{SU_VCAP_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Setup Time to VCAP_PCLK Rising	4	-	-	ns	-
$T_{HD_VCAP_IN}$	VCAP_HSYNC, VCAP_VSYNC, VCAP_FIELD and VCAP_DATA Hold Time from VCAP_PCLK Rising	1	-	-	ns	-

Table 6.3-11 Capture Sensor Interface Timing

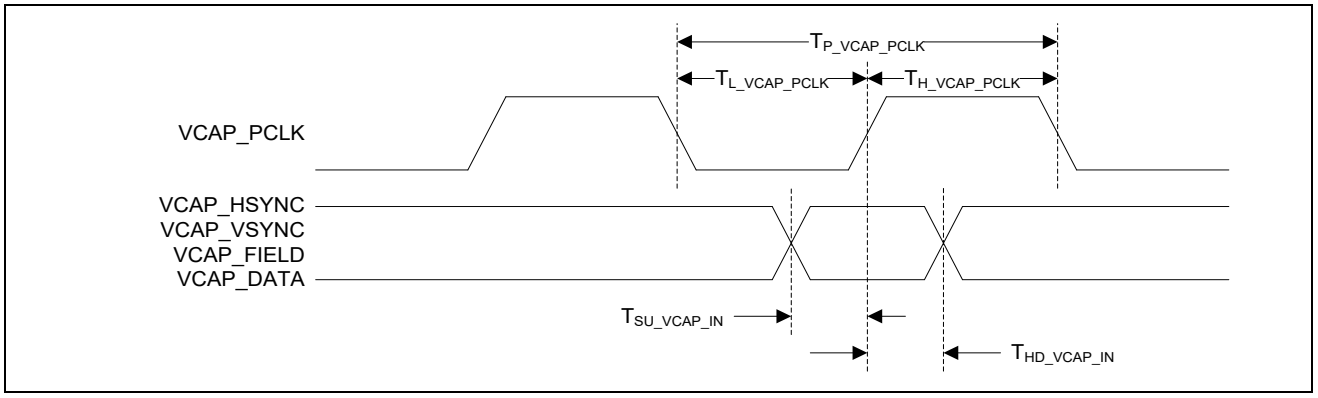


Figure 6.3-14 Capture Sensor Interface Timing Diagram

6.4 Analog Characteristics

6.4.1 12-bit SARADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
-	Resolution	-	12	-	Bit	
DNL	Differential Nonlinearity Error	-	±1	-	LSB	V_{REF} is external AVREF pin
INL	Integral Nonlinearity Error	-	-1.2	-	LSB	V_{REF} is external AVREF pin
E_O	Offset Error	-	+3.7	-	LSB	V_{REF} is external AVREF pin
E_G	Gain Error (Transfer Gain)	-	-6.6	-	LSB	V_{REF} is external AVREF pin
E_A	Absolute Error	-	4.2	-	LSB	V_{REF} is external AVREF pin
-	Monotonic	Guaranteed				
F_{ADC}	ADC Clock Frequency	-	-	16	MHz	
T_{CAL}	Calibration Time	-	3	-	Clock	
T_S	Sample Time	-	17	-	Clock	
T_{ADC}	Conversion Time	-	20		Clock	
F_S	Sample Rate	-	-	800[1]	k SPS	
V_{AVDD}	Supply Voltage	2.7	3.3	3.6	V	
I_{DDA1}	Supply Current (Avg.)	-	1.2		mA	ADC channel 1 high speed mode
I_{DDA2}	Supply Current (Avg.)	-	1.0		mA	ADC channel 1 low speed mode
I_{DDA3}	Supply Current (Avg.)	-	0.4		mA	
I_{LK}	Leakage Current	-	0.1	-	uA	
V_{REF}	Reference Voltage	2	-	V_{AVDD}	V	
V_{IN}	Analog Input Voltage	0	-	V_{REF}	V	
R_{IN}	Analog Input Impedance	-	-	2	MΩ	
C_{IN}	Capacitance	-	25.6		pF	

Note:

1. ADC channel 1 supports sample rate higher than 160k SPS. Other ADC channels support sampel rate up to 160k SPS.

Table 6.4-1 SAR ADC Characteristics

6.4.2 Low Voltage Detection (LVD) and Low Voltage Reset (LVR)

Symbol	Parameter	Min.	Typ.	Max	Unit	Test Conditions
V_{DD}	Operation Voltage	2.0	3.3	3.63	V	-
I_{DD}	Operating Current		21		uA	-
I_{LK}	Quiescent Current	-	0.1	0.5	uA	LVR_EN (SYS_LVRDCR[0]) = 0, LVD_EN (SYS_LVRDCR[8]) = 0
T_A	Temperature	-40	-	85	°C	-
V_{TH_LVD}	LVD Threshold Voltage	2.295	2.55	2.805	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		2.475	2.75	3.025	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{TH_LVR}	LVR Threshold Voltage	2.115	2.35	2.585	V	-
V_{HY_LVD}	LVD Hysteresis	0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 0
		0.045	0.05	0.055	V	LVD_SEL (SYS_LVRDCR[9]) = 1
V_{HY_LVR}	LVR Hysteresis	0.045	0.05	0.055	V	-

Table 6.4-2 LVD and LVR Characteristics

6.4.3 3.3V Power-On Reset (POR33)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	125	°C	-
V_{POR}	Reset Voltage	-	1.83	-	V	AVDD rising from 0V to 3.3V
I_{POR33}	Quiescent current	-	5	-	nA	Vin > reset voltage

Table 6.4-3 POR33 Characteristics

6.4.4 1.2V Power-On Reset (POR12)

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	125	°C	-
V_{POR}	Reset Voltage	-	0.76	-	V	CORE_VDD rising from 0V to 1.2V
I_{POR12}	Quiescent current	-	10	-	nA	Vin > reset voltage

Table 6.4-4 POR12 Characteristics

6.4.5 USB 2.0 PHY

6.4.5.1 Low/Full-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{OL}	Output Low (Driven)	-	-	0.3	V	1.5K RPU on DP to 3.6v
V_{OH}	Output High (Driven)	2.8	-	-	V	15K RPD on DP, DM to GND
V_{DI}	Differential Input Sensitivity	0.2	-	-	V	$\lvert V_{USB0_DP}–V_{USB0_DM}\rvert$
V_{CM}	Differential Common-Mode Range	0.8	-	2.5	V	
V_{IL}	Single-Ended Input Low	-	-	0.8	V	-
V_{IH}	Single-Ended Input High	2.0	-	-	V	-
R_{PU}	Pull-Up Resistor	1.35	1.5	1.65	kΩ	
R_{PD_DP}	D+ Pull-Down Resistor	13.5	15	16.5	kΩ	
R_{PD_DM}	D- Pull-Down Resistor	13.5	15	16.5	kΩ	
Z_{DRV}	Driver Output Resistance	28	-	44	Ω	Steady state drive[1]

Note:

1. Driver output resistance doesn't include series resistor resistance.

Table 6.4-5 Low/Full-Speed DC Electrical Specifications

6.4.5.2 High-Speed DC Electrical Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HSDI}	High Speed Differential Input Signal Level	150	-	-	mV	$\|V_{USB0_DP}–V_{USB0_DM}\|$
V_{HSQ}	High Speed Squelch Detection Threshold	100	125	150	mV	$\|V_{USB0_DP}–V_{USB0_DM}\|$
V_{HSCM}	High Speed Common Mode Voltage Range	-50	-	500	mV	
V_{HSOH}	High Speed Data Signaling High	300	400	440	mV	
V_{HSOL}	High Speed Data Signaling Low	-10	0	10	mV	
V_{CHIRPJ}	Chirp J Level	700	-	1100	mV	
V_{CHIRPK}	Chirp K Level	-900	-	-500	mV	
R_{HSDRV}	High Speed Driver Output Resistance	40.5	45	49.5	Ω	

Table 6.4-6 High-Speed DC Electrical Specifications

6.4.5.3 USB Low-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{LRISE}	Rise Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
T_{LFALL}	Fall Time	75	-	300	ns	CL=200pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{LCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Table 6.4-7 USB Low-Speed Driver AC Electrical Characteristics

6.4.5.4 USB Full-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FRISE}	Rise Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FFALL}	Fall Time	4	-	20	ns	CL=50pF, 10% to 90% of $\|V_{OH}-V_{OL}\|$
V_{FCR}	Crossover Voltage	1.3	-	2.0	V	Excluding the first transition from idle state

Table 6.4-8 USB Full-Speed Driver AC Electrical Characteristics

6.4.5.5 USB High-Speed Driver AC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{HRISE}	High Speed Driver Rise Time	500	-	900	ps	CL<10pF
V_{HFALL}	High Speed Driver Fall Time	500	-	900	ps	CL<10pF

Table 6.4-9 USB High-Speed Driver AC Electrical Characteristics

6.5 Thermal Characteristics of N9H31 Package

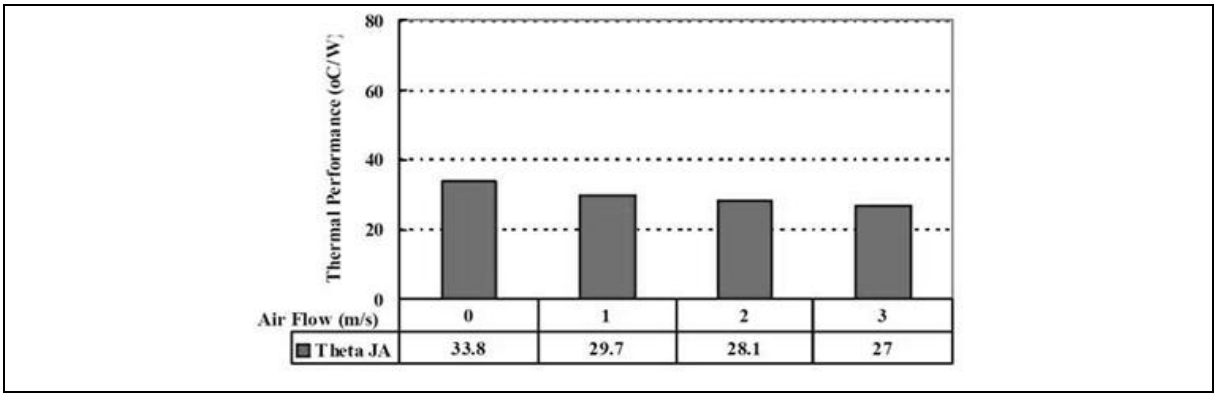


Figure 6.4-1 Thermal Performance of SLQFP under Forced Convection

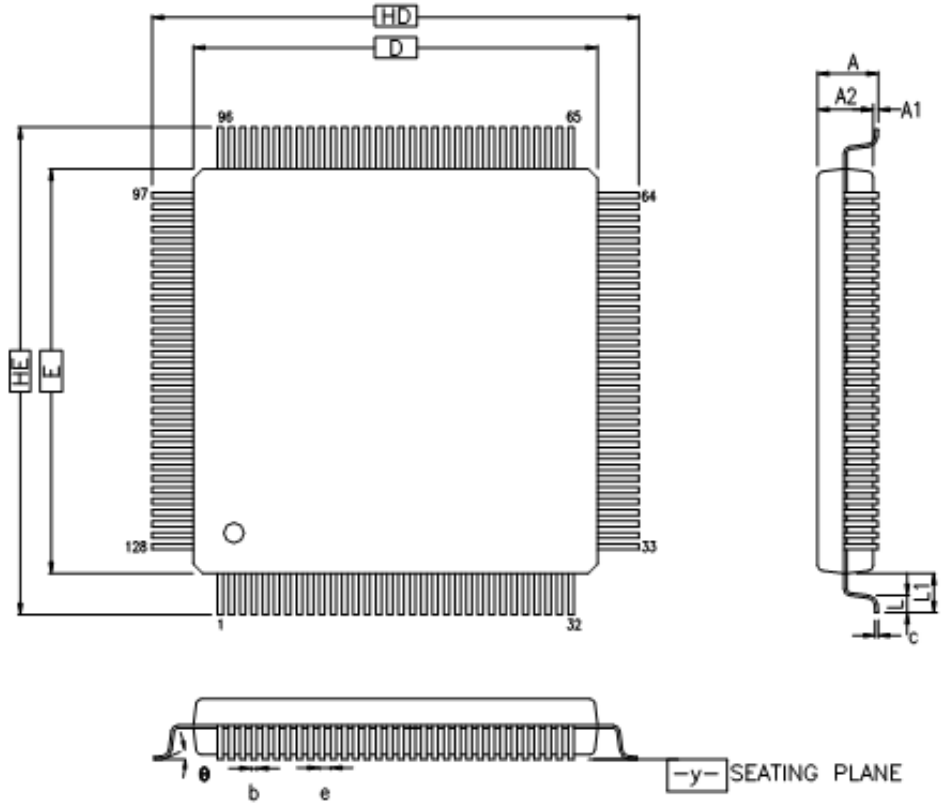
6.5.1 Simulation Conditions

Input Power	Top Die: 0.6W Bottom die: 0.6 W
Test Board (PCB)	4 layers
Control Condition	Air Flow = 0, 1, 2, 3 m/s

7 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

7.1 128L LQFP (14x14x1.4mm footprint)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
HD	16.00 BSC.			0.630 BSC.		
D	14.00 BSC.			0.551 BSC.		
HE	16.00 BSC.			0.630 BSC.		
E	14.00 BSC.			0.551 BSC.		
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
θ	0°	3.5°	7°	0°	3.5°	7°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
y	–	–	0.1	–	–	0.004

7.2 PCB Reflow Profile Suggestion

7.2.1 Reflow Profile Suggestion for N9H31 Series

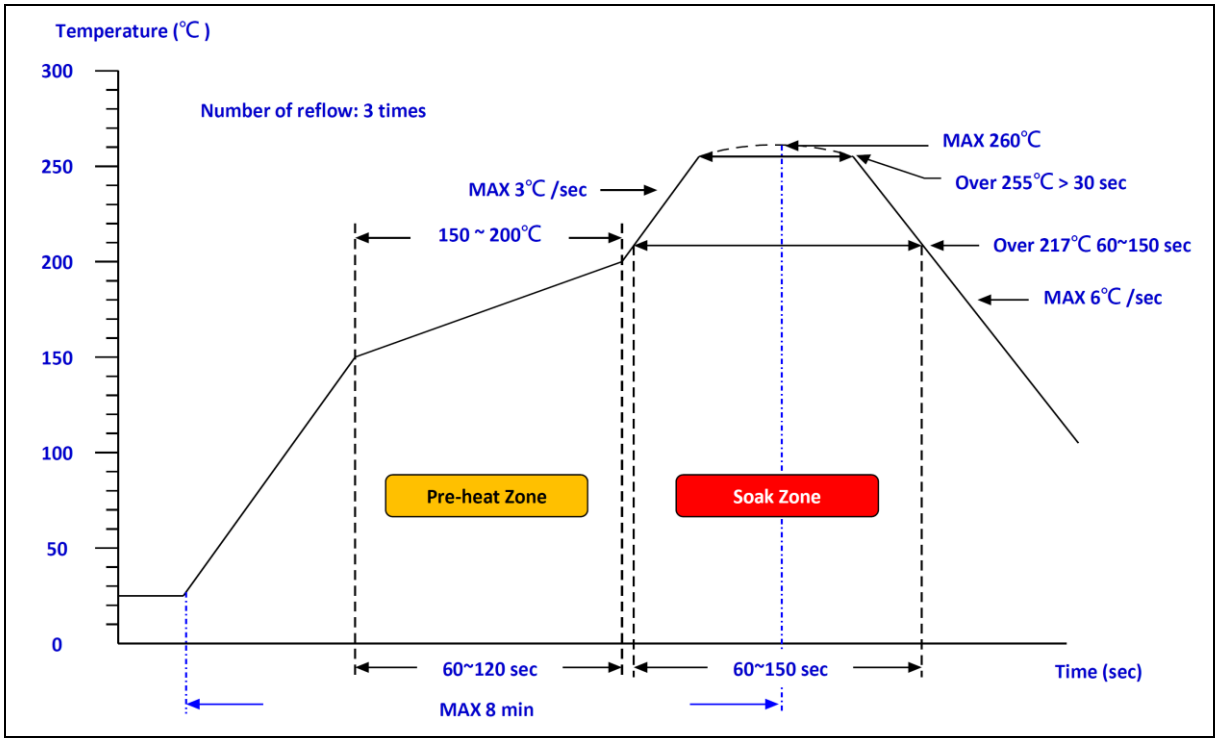


Figure 7.2-1 Profile Suggestion for N9H31 Series

8 REVISION HISTORY

Date	Revision	Description
2024.04.10	1.00	• Initial version.
2024.04.29	1.01	• Removed Enhance Timer in section 2.1, 3.2, 4.1 and 5.9. • Modified UART in section 2.1, 3.2, 4.1 and 5.13.
2024.07.29	1.02	• Removed EBI in chapter 1, 5, 6 and section 2.1, 3.2, 3.4, 4.1 and 5.9.
2026.5.28	1.03	• Add Part Number in section 3.2

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