NuMicro™ Family
NUC123 Series
Product Brief

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1 GENERAL DESCRIPTION

The NuMicro™ NUC123 series 32-bit microcontrollers are embedded with Cortex™-M0 core running up to 72 MHz, up to 36K/68K-byte embedded flash, 12K/20K-byte embedded SRAM, and 4K-byte loader ROM for the ISP. It also integrates Timers, Watchdog Timer, Windowed Watchdog Timer, PDMA with CRC calculation unit, UART, SPI/MICROWIRE, I^2C, I^2S, PWM Timer, GPIO, PS/2, USB 2.0 FS Device, 10-bit ADC, Low Voltage Reset Controller and Brown-out Detector.

Product Line	UART	SPI	I^2C	USB	LIN	CAN	PS/2	I^2S
NUC123	•	•	•	•	-	-	•	•

Table 1-1 Connectivity Support Table

2 FEATURES

2.1 NuMicro™ NUC123 Features

Core

- ARM® Cortex™-M0 core runs up to 72 MHz
- One 24-bit system timer
- Supports low power sleep mode
- Single-cycle 32-bit hardware multiplier
- NVIC for the 32 interrupt inputs, each with 4-levels of priority
- Supports Serial Wire Debug with 2 watchpoints/4 breakpoints

Built-in LDO for wide operating voltage ranges from 2.5 V to 5.5 V

Flash Memory

- 36K/68K bytes Flash for program code
- 4KB flash for ISP loader
- Supports In-system program (ISP) application code update
- 512 byte page erase for flash
- Configurable data flash address and size for both 36KB and 68KB system
- Supports 2 wire ICP update through SWD/ICE interface
- Supports fast parallel programming mode by external programmer

SRAM Memory

- 12K/20K bytes embedded SRAM
- Supports PDMA mode

PDMA (Peripheral DMA)

- Supports 6 channels PDMA for automatic data transfer between SRAM and peripherals such as SPI, UART, I^2S, USB 2.0 FS device, PWM and ADC
- Supports CRC calculation with four common polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32

Clock Control

- Flexible selection for different applications
- Built-in 22.1184 MHz high speed oscillator (Trimmed to 1%) for system operation, and low power 10 kHz low speed oscillator for watchdog and wake-up operation
- Supports one PLL, up to 144 MHz, for high performance system operation
- External 4~24 MHz high speed crystal input for precise timing operation

GPIO

- Four I/O modes:
  - Quasi bi-direction
  - Push-Pull output
  - Open-Drain output
  - Input only with high impendence
- TTL/Schmitt trigger input selectable

- I/O pin configured as interrupt source with edge/level setting
- Supports High Driver and High Sink IO mode

Timer

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit pre-scale counter
- Independent clock source for each timer
- Provides One-shot, Periodic, Toggle and Continuous Counting Operation modes
- Supports event counting function

Watchdog/Windowed-Watchdog Timer

- Multiple clock sources
- 8 selectable time out period from 1.6 ms ~ 26.0 sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog timer time-out
- Interrupt on windowed-watchdog timer time-out
- Reset on windowed-watchdog timer time out or reload in an unexpected time window

PWM/Capture

- Up to two built-in 16-bit PWM generators provide four PWM outputs or two complementary paired PWM outputs
- Each PWM generator equipped with one clock source selector, one clock divider, one 8-bit prescaler and one dead-zone generator for complementary paired PWM
- Up to four 16-bit digital Capture timers (shared with PWM timers) providing four rising/falling capture inputs
- Supports capture interrupt

UART

- Up to two UART controllers
- UART ports with flow control (TXD, RXD, CTS and RTS)
- UART0/1 with 16-byte FIFO for standard device
- Supports IrDA (SIR) function
- Supports RS-485 9-bit mode and direction control
- Programmable baud-rate generator up to 1/16 system clock
- Supports PDMA mode

SPI

- Up to three sets of SPI controller
- Master up to 32 MHz, and Slave up to 16 MHz (chip working at 3.3V)
- Supports SPI master/Slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 8 to 32 bits
- MSB or LSB first data transfer
- Two slave/device select lines when it is selected as the master, and one slave/device select line when it is selected as the slave
- Supports Byte Suspend mode in 16/24/32-bit transmission
- Supports PDMA mode

I^2C

- Up to two sets of I^2C device

- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allowing devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow versatile rate control
- Supports multiple address recognition (four slave address with mask option)
- Supports wake-up by address recognition (for 1st slave address only)

I^2S

- Interface with external audio CODEC
- Operate as either master or Slave mode
- Capable of handling 8-, 16-, 24- and 32-bit word sizes
- Supports Mono and stereo audio data
- Supports I^2S and MSB justified data format
- Provides two 8 word FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two DMA requests, one for transmitting and the other for receiving

PS/2 Device Controller

- Host communication inhibit and request to send detection
- Reception frame error detection
- Programmable 1 to 16 bytes transmit buffer to reduce CPU intervention
- Double buffer for data reception
- S/W override bus

USB 2.0 Full-Speed Device

- One set of USB 2.0 FS Device 12Mbps
- On-chip USB Transceiver
- Provides 1 interrupt source with 4 interrupt events
- Supports Control, Bulk In/Out, Interrupt and Isochronous transfers
- Auto suspend function when no bus signaling for 3 ms
- Provides 8 programmable endpoints
- Includes 512 bytes internal SRAM as USB buffer
- Provides remote wake-up capability

ADC

- 10-bit SAR ADC with 150K SPS
- Up to 8-ch single-end input
- Single scan/single cycle scan/continuous scan
- Each channel with individual result register
- Scan on enabled channels
- Threshold voltage detection
- Conversion start by software programming or external input
- Supports PDMA mode

Brown-out detector

- With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
- Supports Brown-out Interrupt and Reset option

Low Voltage Reset

- Threshold voltage levels: 2.0 V

One built-in LDO

Operating Temperature: -40℃~85℃

Packages:

- All Green package (RoHS)
- LQFP 64-pin
- LQFP 48-pin
- QFN 33-pin

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3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NuMicro™ NUC123xxxANx Selection Guide

3.1.1 NuMicro™ NUC123 Selection Guide

Part number	Flash	SRAM	ISP ROM	I/O	Timer	Connectivity						I²S	Comp.	PWM	ADC	RTC	EBI	ISP ICP IAP	Package
						UART	SPI	I²C	USB	LIN	PS/2								
NUC123ZD4AN0	68 KB	20 KB	4 KB	Up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	-	-	-	v	QFN33
NUC123ZC2AN1	36 KB	12 KB	4 KB	up to 20	4x32-bit	1	3	1	1	-	-	1	-	2	-	-	-	v	QFN33
NUC123LD4AN0	68 KB	20 KB	4 KB	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	LQFP48
NUC123LC2AN1	36 KB	12 KB	4 KB	up to 36	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	LQFP48
NUC123SD4AN0	68 KB	20 KB	4 KB	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	LQFP64
NUC123SC2AN1	36 KB	12 KB	4 KB	up to 47	4x32-bit	2	3	2	1	-	1	1	-	4	8x10-bit	-	-	v	LQFP64

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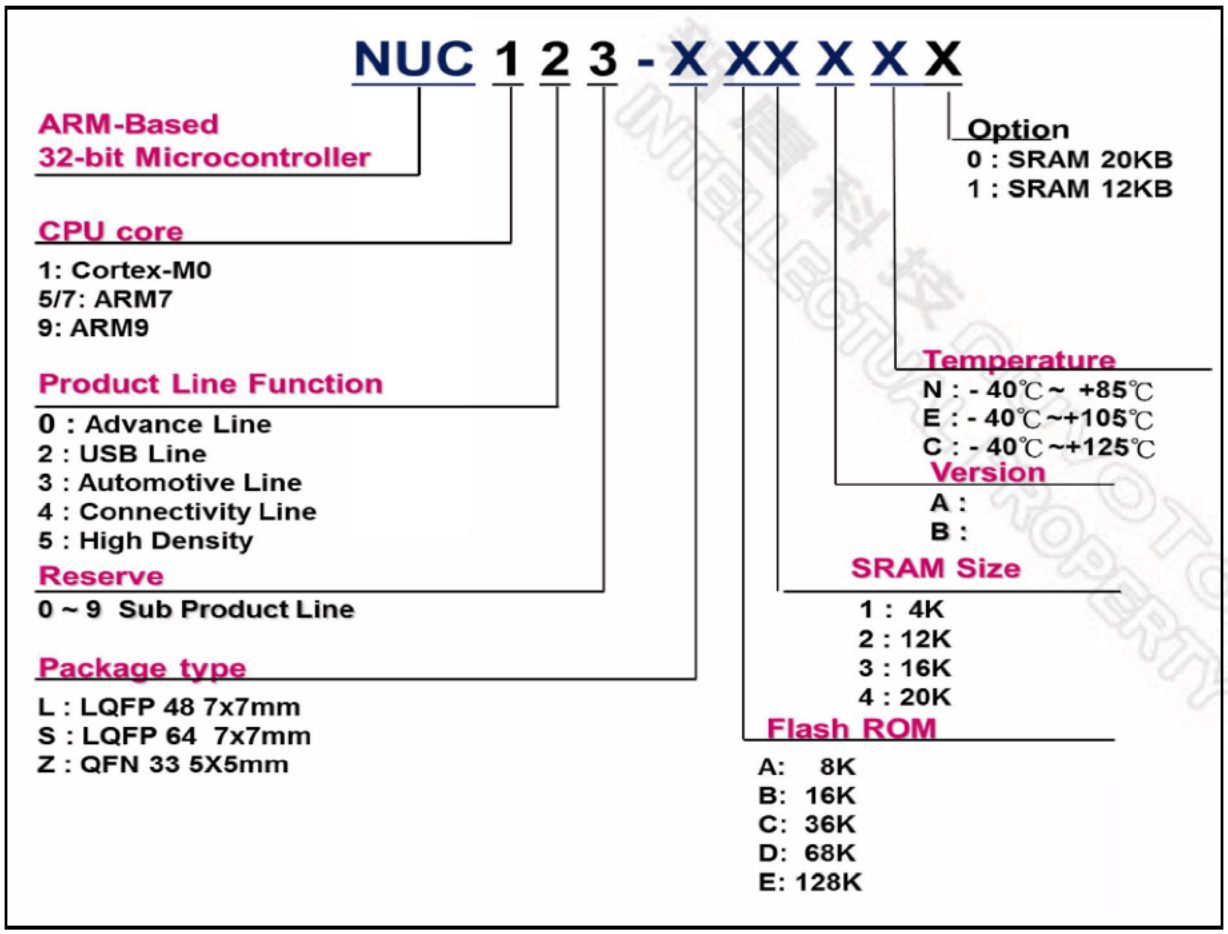


Figure 3-1 NuMicro™ NUC123 Series Selection Code

3.2 Pin Configuration

3.2.1 NuMicro™ NUC123 Pin Diagram

3.2.1.1 *NuMicro™ NUC123SxxANx LQFP 64 pin*

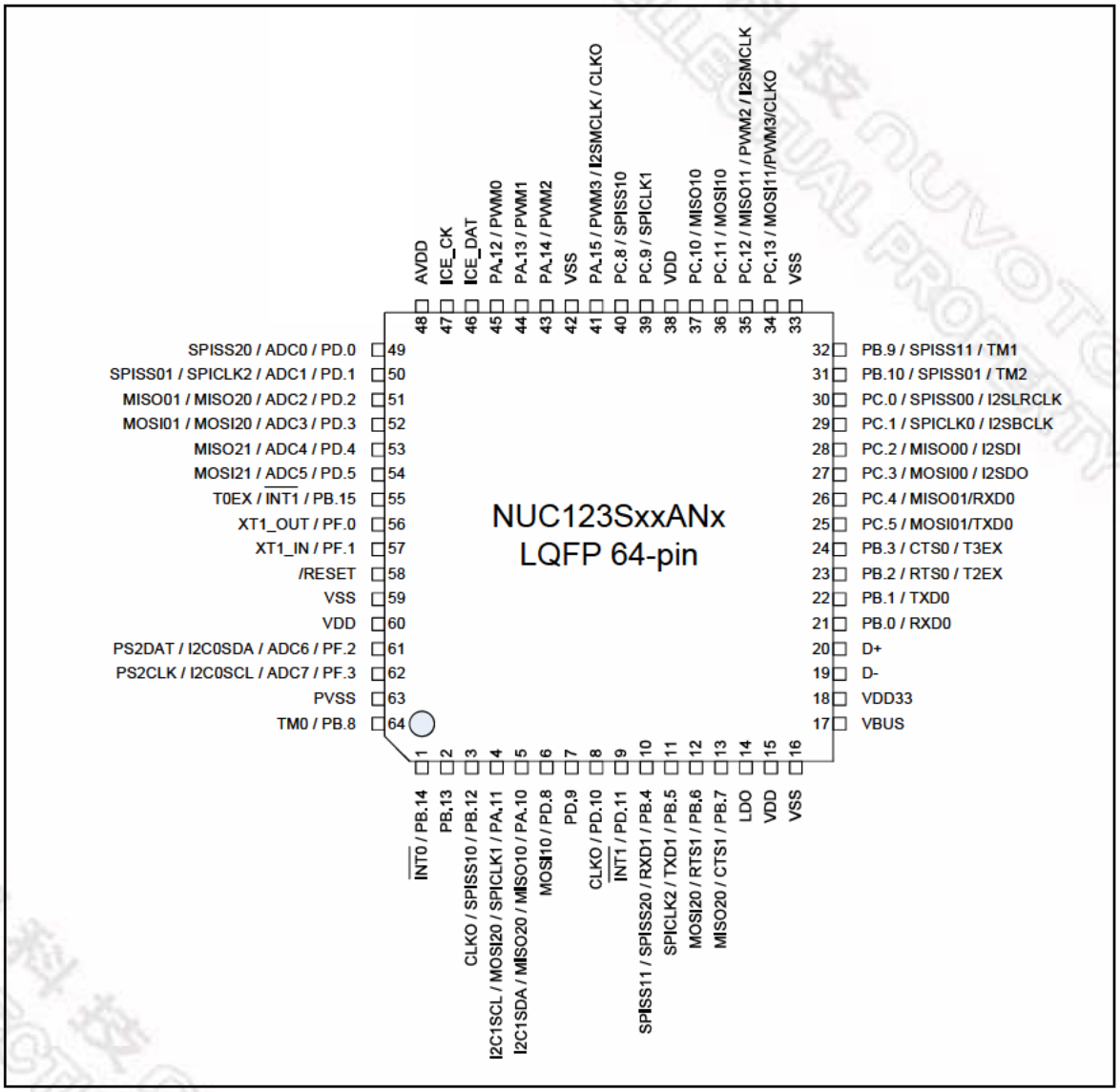


Figure 3-2 NuMicro™ NUC123SxxANx LQFP 64-pin Assignment

3.2.1.2 *NuMicro™ NUC123LxxANx LQFP 48 pin*

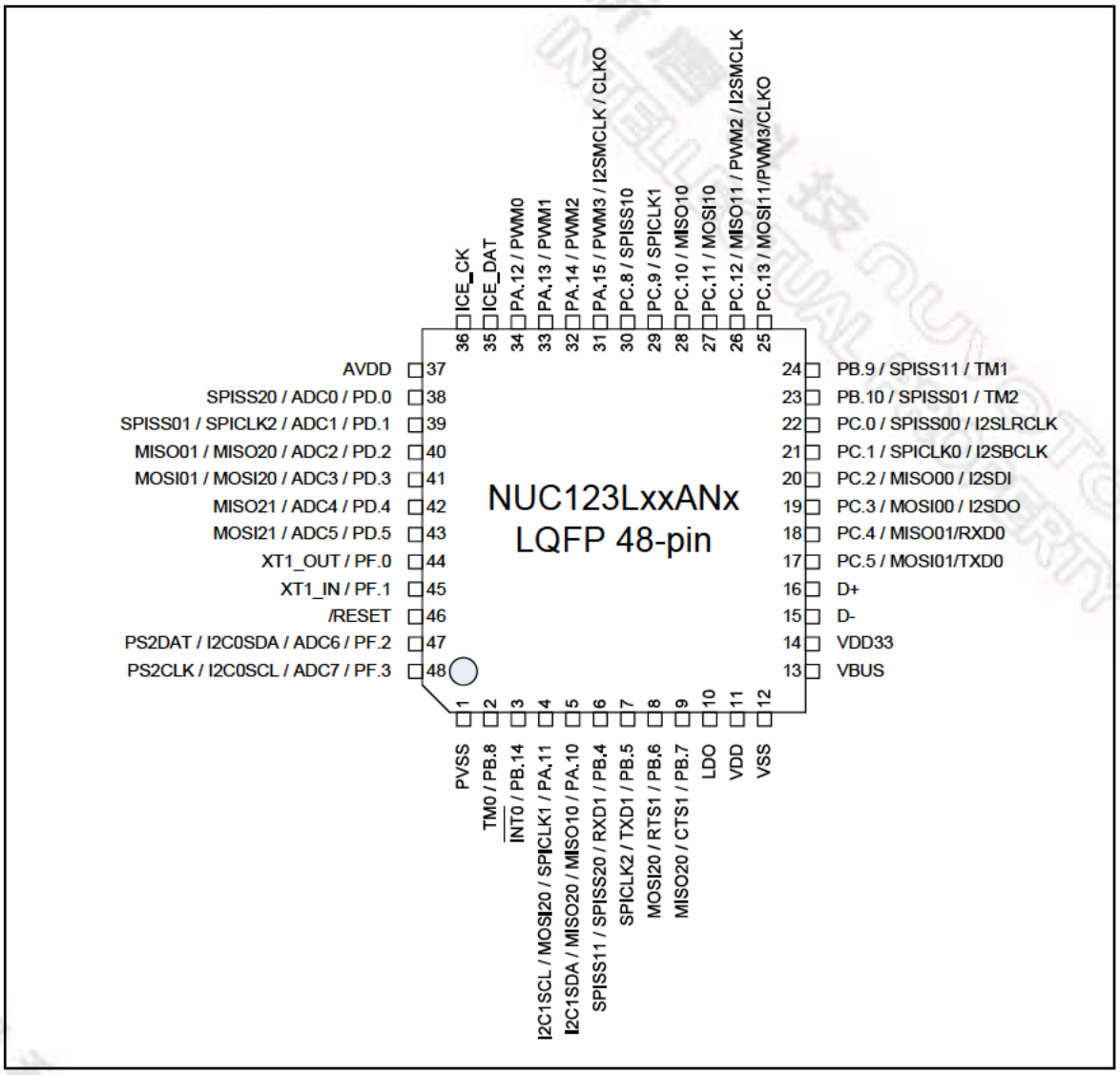


Figure 3-3 NuMicro™ NUC123LxxANx LQFP 48-pin Assignment

3.2.1.3 *NuMicro™ NUC123ZxxANx QFN 33 pin*

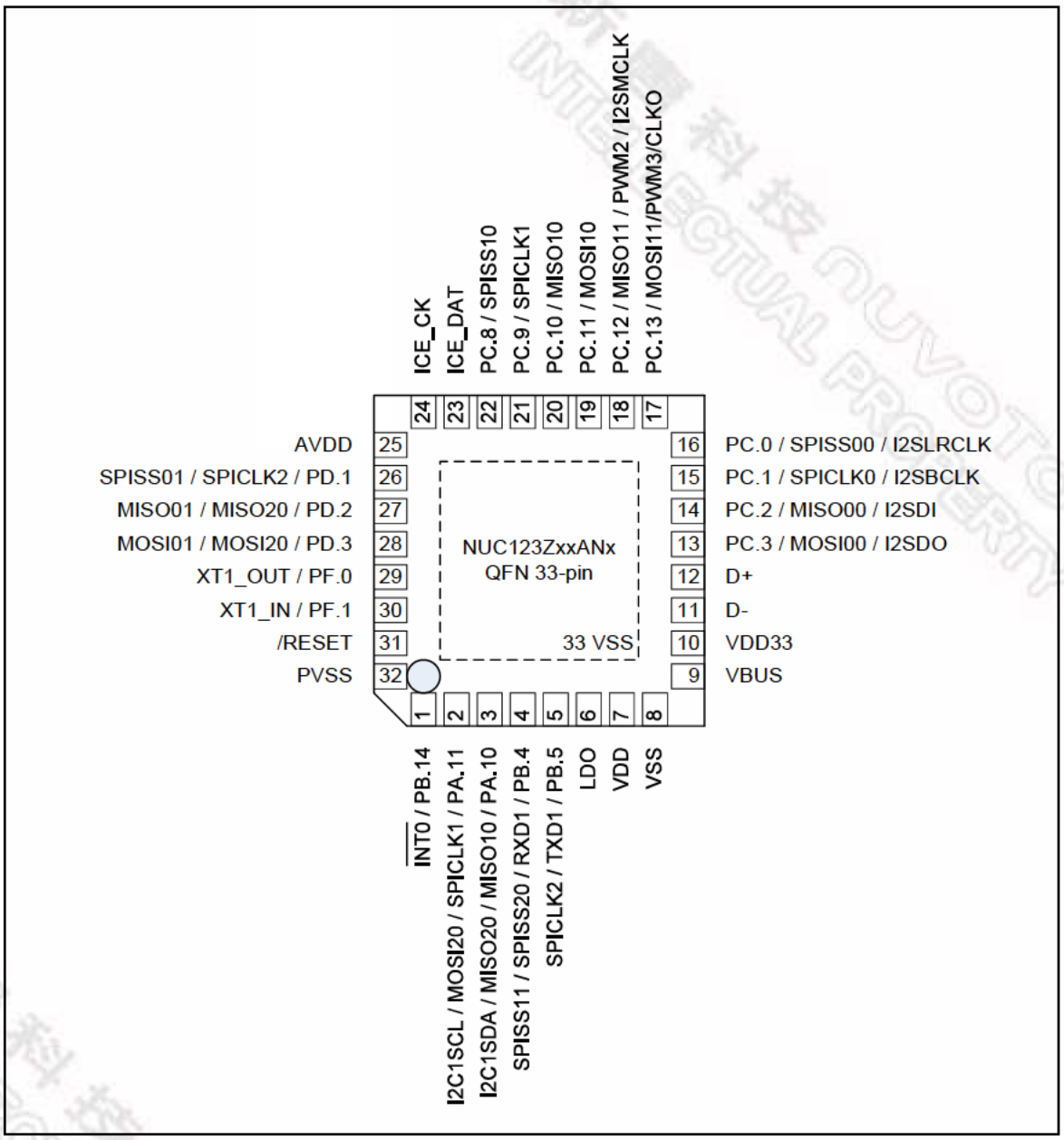


Figure 3-4 NuMicro™ NUC123ZxxANx QFN 33-pin Assignment

4 BLOCK DIAGRAM

4.1 NuMicro™ NUC123 Block Diagram

4.1.1 NuMicro™ NUC123 Block Diagram

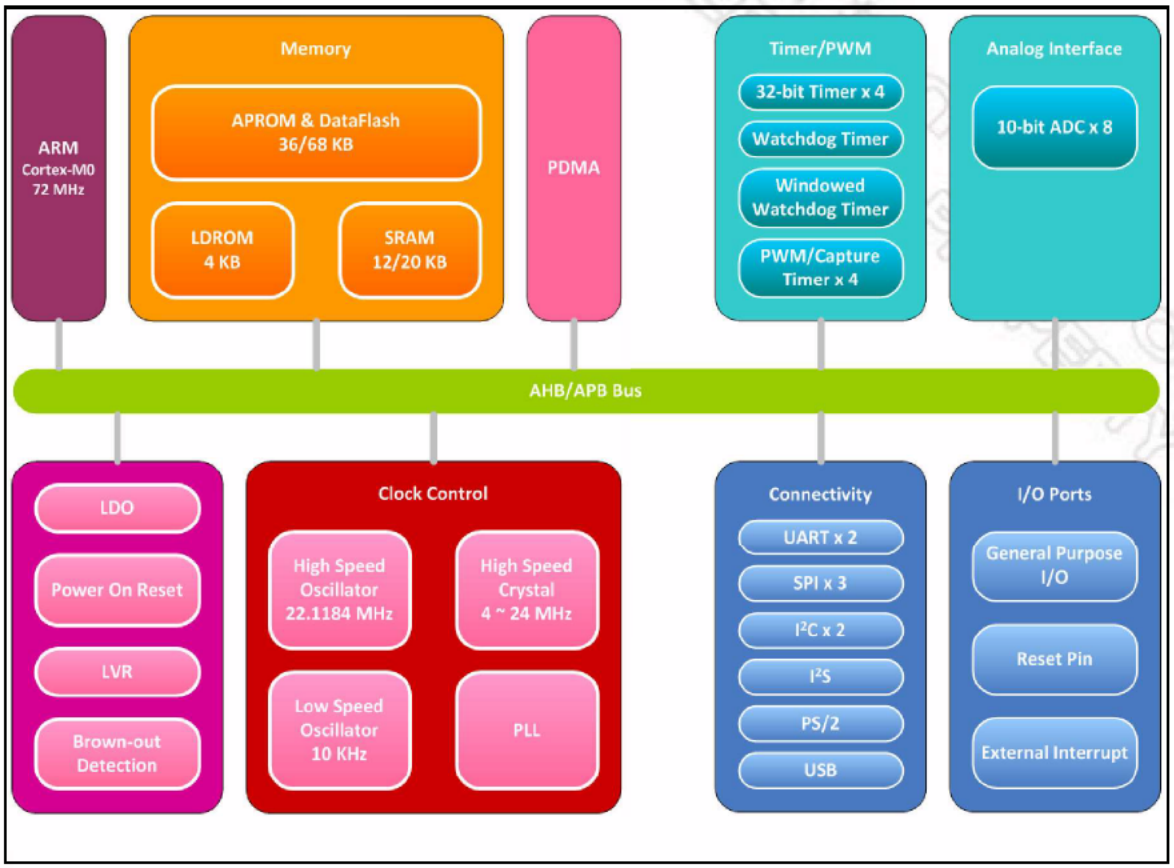


Figure 4-1 NuMicro™ NUC123 Block Diagram

5 ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}	V_{SS} -0.3	V_{DD} +0.3	V
Oscillator Frequency	$1/t_{CLCL}$	4	24	MHz
Operating Temperature	TA	-40	+85	°C
Storage Temperature	TST	-55	+150	°C
Maximum Current into VDD		-	120	mA
Maximum Current out of VSS			120	mA
Maximum Current sunk by an I/O pin			35	mA
Maximum Current sourced by an I/O pin			35	mA
Maximum Current sunk by total I/O pins			100	mA
Maximum Current sourced by total I/O pins			100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

5.2 DC Electrical Characteristics

5.2.1 NuMicro™ NUC123 DC Electrical Characteristics

(V_{DD} -V_{SS} = 5.5 V, TA = 25°C, FOSC = 72 MHz unless otherwise specified.)

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operation voltage	V_{DD}	2.5		5.5	V	V_{DD} = 2.5V ~ 5.5V up to 72 MHz
VDD rise rate to ensure internal operation correctly	V_{RISE}	0.05			V/ms	
Power ground	V_{SS} AV_{SS}	-0.3			V	
LDO output voltage	V_{LDO}	1.62	1.8	1.98	V	V_{DD} > 2.5V
Analog operating voltage	AV_{DD}	0	V_{DD}		V	When system used analog function, please refer to chapter 7.4 for corresponding analog operating voltage
Operating current Normal Run mode at 72 MHz	I_{DD1}		36		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{DD2}		21		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{DD3}		35		mA	V_{DD} = 3V at 72 MHz, All IP and PLL enabled, XTAL = 12 MHz
	I_{DD4}		20		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
Operating current Normal Run mode at 12 MHz	I_{DD5}		7		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD6}		4		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
	I_{DD7}		6		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{DD8}		3		mA	V_{DD} = 3V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Normal Run mode at 4 MHz	I_{DD9}		4		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD10}		3		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{DD11}		4		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{DD12}		2		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating current Idle mode at 72 MHz	I_{IDLE1}		29		mA	V_{DD} = 5.5V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE2}		14		mA	V_{DD} = 5.5V at 72 MHz, All IP Disabled and PLL Enabled, XTAL = 12 MHz
	I_{IDLE3}		28		mA	V_{DD} = 3V at 72 MHz, All IP and PLL Enabled, XTAL = 12 MHz
	I_{IDLE4}		13		mA	V_{DD} = 3V at 72 MHz, All IP Disabled and PLL Enabled, XTAL=12 MHz
Operating current Idle mode at 12 MHz	I_{IDLE5}		6		mA	V_{DD} = 5.5V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE6}		3		mA	V_{DD} = 5.5V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
	I_{IDLE7}		5		mA	V_{DD} = 3V at 12 MHz, All IP Enabled and PLL Disabled, XTAL = 12 MHz
	I_{IDLE8}		2		mA	V_{DD} = 3 V at 12 MHz, All IP and PLL Disabled, XTAL = 12 MHz
Operating current Idle mode at 4 MHz	I_{IDLE9}		3		mA	V_{DD} = 5V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE10}		2		mA	V_{DD} = 5V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
	I_{IDLE11}		2		mA	V_{DD} = 3V at 4 MHz, All IP Enabled and PLL Disabled, XTAL = 4 MHz
	I_{IDLE12}		1		mA	V_{DD} = 3V at 4 MHz, All IP and PLL Disabled, XTAL = 4 MHz
Operating current Idle mode at 10 kHz	I_{IDLE5}		131		uA	V_{DD} = 5.5V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE6}		129		uA	V_{DD} = 5.5V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE7}		125		uA	V_{DD} = 3V at 10 kHz, All IP Enabled and PLL Disabled, LIRC 10 kHz Enabled
	I_{IDLE8}		124		uA	V_{DD} = 3 V at 10 kHz, All IP and PLL Disabled, LIRC 10 kHz Enabled
Standby current Power-down mode	I_{PWD1}		12		µA	V_{DD} = 5.5V, No load when BOV function Disabled
	I_{PWD2}		9		µA	V_{DD} = 3.3V, No load when BOV function Disabled
Input Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional mode)	I_{IN1}		-64		µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN} = V_{DD}

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Input Current at /RESET[1]	I_{IN2}	-55	-45	-30	μA	V_{DD} = 3.3V, V_{IN} = 0.45V
Input Leakage Current PA, PB, PC, PD, PE, PF	I_{LK}	-2	-	+2	μA	V_{DD} = 5.5V, 0 < V_{IN} < V_{DD}
Logic 1 to 0 Transition Current PA~PF (Quasi-bidirectional mode)	I_{TL} [3]	-650	-	-200	μA	V_{DD} = 5.5V, V_{IN} < 2.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IL1}	-0.3	-	0.8	V	V_{DD} = 4.5V
		-0.3	-	0.6		V_{DD} = 2.5V
Input High Voltage PA, PB, PC, PD, PE, PF (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 3.0V
Input Low Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IL2}	-0.5	-	0.35 V_{DD}	V	
Input High Voltage PA, PB, PC, PD, PE, PF (Schmitt input)	V_{IH2}	0.65 V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage of PA~PE (Schmitt input)	V_{HY}		0.2 V_{DD}		V	
Input Low Voltage XT1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XT1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (Schmitt input), /RESET	V_{ILS}	-0.5	-	0.2 V_{DD}	V	
Positive going threshold (Schmitt input), /RESET	V_{IHS}	0.6 V_{DD}	-	V_{DD}+0.5	V	
Source Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional Mode)	I_{SR11}	-300	-370	-450	μA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR12}	-50	-70	-90	μA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR12}	-40	-60	-80	μA	V_{DD} = 2.5V, V_S = 2.0V
Source Current PA, PB, PC, PD, PE, PF (Push-pull Mode)	I_{SR21}	-20	-24	-28	mA	V_{DD} = 4.5V, V_S = 2.4V
	I_{SR22}	-4	-6	-8	mA	V_{DD} = 2.7V, V_S = 2.2V
	I_{SR22}	-3	-5	-7	mA	V_{DD} = 2.5V, V_S = 2.0V

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Sink Current PA, PB, PC, PD, PE, PF (Quasi-bidirectional and Push-pull Mode)	I_{SK1}	10	16	20	mA	V_{DD} = 4.5V, V_S = 0.45V
	I_{SK1}	7	10	13	mA	V_{DD} = 2.7V, V_S = 0.45V
	I_{SK1}	6	9	12	mA	V_{DD} = 2.5V, V_S = 0.45V
Brown-out voltage with BOV_VL [1:0] =00b	$V_{BO2.2}$	2.1	2.2	2.3	V	
Brown-out voltage with BOV_VL [1:0] =01b	$V_{BO2.7}$	2.6	2.7	2.8	V	
Brown-out voltage with BOV_VL [1:0] =10b	$V_{BO3.8}$	3.7	3.8	3.9	V	
Brown-out voltage with BOV_VL [1:0] =11b	$V_{BO4.5}$	4.4	4.5	4.6	V	
Hysteresis range of BOD voltage	V_{BH}	30	-	150	mV	V_{DD} = 2.5V - 5.5V

Notes:

1. /RESET pin is a Schmitt trigger input.

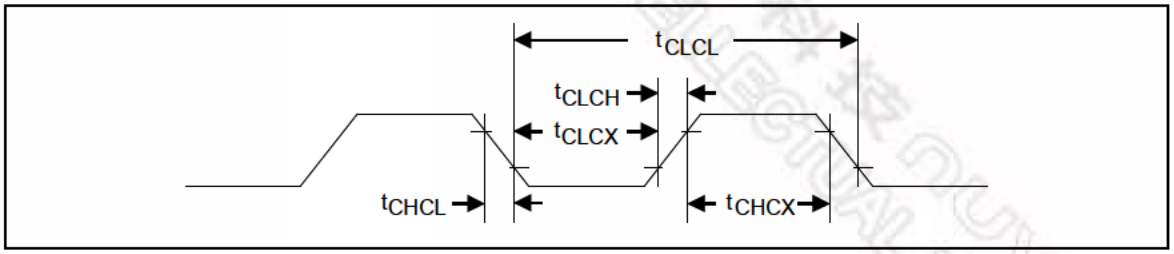
2. Crystal Input is a CMOS input.

3. Pins of PA, PB, PC, PD and PE can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5 V, 5he transition current reaches its maximum value when V_{IN} approximates to 2V.

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5.3 AC Electrical Characteristics

5.3.1 External 4~24 MHz High Speed Oscillator



Note: Duty cycle is 50%.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
t_{CHCX}	Clock High Time		20	-	-	nS
t_{CLCX}	Clock Low Time		20	-	-	nS
t_{CLCH}	Clock Rise Time		-	-	10	nS
t_{CHCL}	Clock Fall Time		-	-	10	nS

5.3.2 External 4~24 MHz High Speed Crystal

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input clock frequency	External crystal	4	12	24	MHz
Temperature	-	-40	-	85	℃
VDD	-	2.5	5	5.5	V

5.3.2.1 *Typical Crystal Application Circuits*

CRYSTAL	C1	C2	R
4 MHz ~ 24 MHz	without	without	without

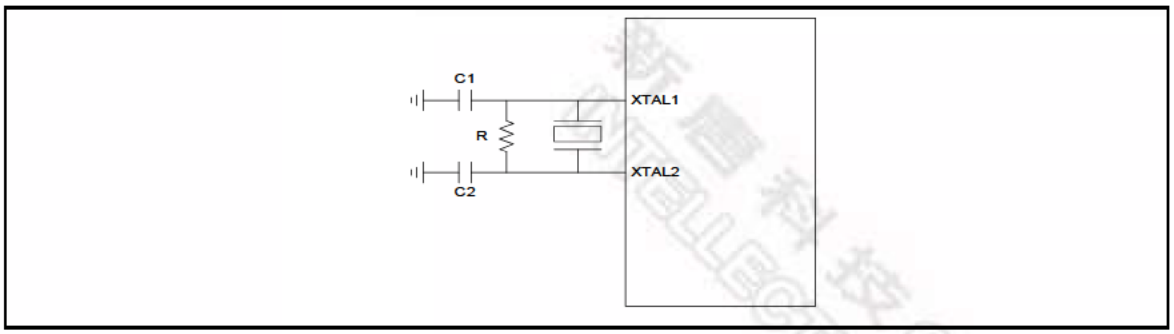


Figure 7-1 Typical Crystal Application Circuit

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5.3.3 Internal 22.1184 MHz High Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	22.1184	-	MHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-1	-	+1	%
	-40℃~+85℃; V_{DD} =2.5 V~5.5 V	-3	-	+3	%
Operation Current	V_{DD} =5 V	-	500	-	uA

5.3.4 Internal 10 kHz Low Speed Oscillator

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage[1]	-	2.5	-	5.5	V
Center Frequency	-	-	10	-	kHz
Calibrated Internal Oscillator Frequency	+25℃; V_{DD} =5 V	-30	-	+30	%
	-40℃~+85℃; V_{DD}=2.5 V~5.5 V	-50	-	+50	%

Note: Internal operation voltage comes from LDO.

5.4 Analog Characteristics

5.4.1 10-bit SARADC Specifications

PARAMETER	SYM	SPECIFICATIONS				TEST CONDITIONS
		MIN	TYP	MAX	UNIT	
Operating Voltage	AV_{DD}	2.7		5.5	V	$AV_{DD} = V_{DD}$
Operating Current	I_{ADC}			1.5	mA	$AV_{DD} = V_{DD} = 5V$, $F_{SPS} = 150K$
Resolution	R_{ADC}			10	bit	
Reference Voltage	V_{REF}		A_{VDD}		V	V_{REF} Connected to A_{VDD} in Chip
ADC input Voltage	V_{IN}	0		A_{VDD}	V	
Sampling Rate	F_{SPS}	150K			Hz	V_{DD} = 5V, ADC Clock = 6MHz Free Running Conversion
Integral Non-linearity Error (INL)	INL			±1	LSB	
Differential Non-linearity Error (DNL)	DNL			±1	LSB	
Gain Error	E_G			±2	LSB	
Offset Error	E_{OFFSET}		3		LSB	
Absolute Error	E_{ABS}		4		LSB	
ADC Clock Frequency	F_{ADC}	100K		6M	Hz	V_{DD} = 5V
Clock Cycle	AD_{CYC}	36			Cycle	
Bang-gap Voltage	V_{BG}	1.27	1.35	1.44	V	-40°C ~ +85°C

5.4.2 LDO and Power Management Specifications

PARAMETER	MIN	TYP	MAX	UNIT	NOTE
Input Voltage	2.5	5	5.5	V	V_{DD} input voltage
Output Voltage	1.62	1.8	1.98	V	V_{DD} > 2.5V
Temperature	-40	25	85	℃	
Cbp	-	1	-	uF	Resr = 1Ω

Notes:

1. It is recommended that a 10uF or higher capacitor and a 100nF bypass capacitor are connected between VDD and the closest VSS pin of the device.

2. To ensure power stability, a 1uF (Cbp) or higher capacitor must be connected between LDO pin and the closest VSS pin of the device.

5.4.3 Low Voltage Reset Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	1.7	-	5.5	V
Quiescent current	V_{DD} = 5.5 V	-	-	5	uA
Temperature	-	-40	25	85	℃
Threshold voltage	Temperature = 25℃	1.7	2.0	2.3	V
	Temperature = -40℃	-	2.4	-	V
	Temperature = 85℃	-	1.6	-	V
Hysteresis	-	0	0	0	V

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5.4.4 Brown-out Detector Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Operation voltage	-	2.5	-	5.5	V
Quiescent current	AV_{DD} = 5.5 V	-	-	125	μA
Temperature	-	-40	25	85	℃
Brown-out voltage	BOV_VL[1:0] = 11	4.4	4.5	4.6	V
	BOV_VL [1:0] = 10	3.7	3.8	3.9	V
	BOV_VL [1:0] = 01	2.6	2.7	2.8	V
	BOV_VL [1:0] = 00	2.1	2.2	2.3	V
Hysteresis	-	30	-	150	mV

5.4.5 Power-On Reset (5V) Specifications

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Temperature	-	-40	25	85	℃
Reset voltage	V+	-	2	-	V
Quiescent current	Vin>reset voltage	-	1	-	nA

5.4.6 USB PHY Specifications

5.4.6.1 *USB DC Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input high (driven)		2.0			V
V_{IL}	Input low				0.8	V
V_{DI}	Differential input sensitivity	|PADP-PADM|	0.2			V
V_{CM}	Differential common-mode range	Includes V_{DI} range	0.8		2.5	V
V_{SE}	Single-ended receiver threshold		0.8		2.0	V
	Receiver hysteresis			200		mV
V_{OL}	Output low (driven)		0		0.3	V
V_{OH}	Output high (driven)		2.8		3.6	V
V_{CRS}	Output signal cross voltage		1.3		2.0	V
R_{PU}	Pull-up resistor		1.425		1.575	kΩ
R_{PD}	Pull-down resistor		14.25		15.75	kΩ
V_{TRM}	Termination Voltage for upstream port pull up (RPU)		3.0		3.6	V
Z_{DRV}	Driver output resistance	Steady state drive*		10		Ω
C_{IN}	Transceiver capacitance	Pin to GND			20	pF

Note: Driver output resistance doesn't include series resistor resistance.

5.4.6.2 *USB Full-Speed Driver Electrical Characteristics*

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
T_{FR}	Rising time	C_L = 50p	4		20	ns
T_{FF}	Falling time	C_L = 50p	4		20	ns
T_{FRFF}	Rising and falling time matching	$T_{FRFF} = T_{FR}/T_{FF}$	90		111.11	%

5.4.6.3 *USB Power Dissipation*

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{VDDREG} (Full speed)	VDDD and VDDREG supply current (steady state)	Standby		50		uA
		Input mode				uA
		Output mode				uA

5.5 SPI Dynamic Characteristics

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
SPI Master mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	6	-	-	ns
t_V	Data output valid time	-	1.5	3	ns
SPI Master mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	5.5	-	-	ns
t_V	Data output valid time	-	1.5	3	ns
SPI Slave mode (VDD = 4.5V ~ 5.5V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	5	-	-	ns
t_V	Data output valid time	-	18.5	25	ns
SPI Slave mode (VDD = 3.0V ~ 3.6V, 30pF loading Capacitor)					
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	4.5	-	-	ns
t_V	Data output valid time	-	24	31.5	ns

TBD: To be defined.

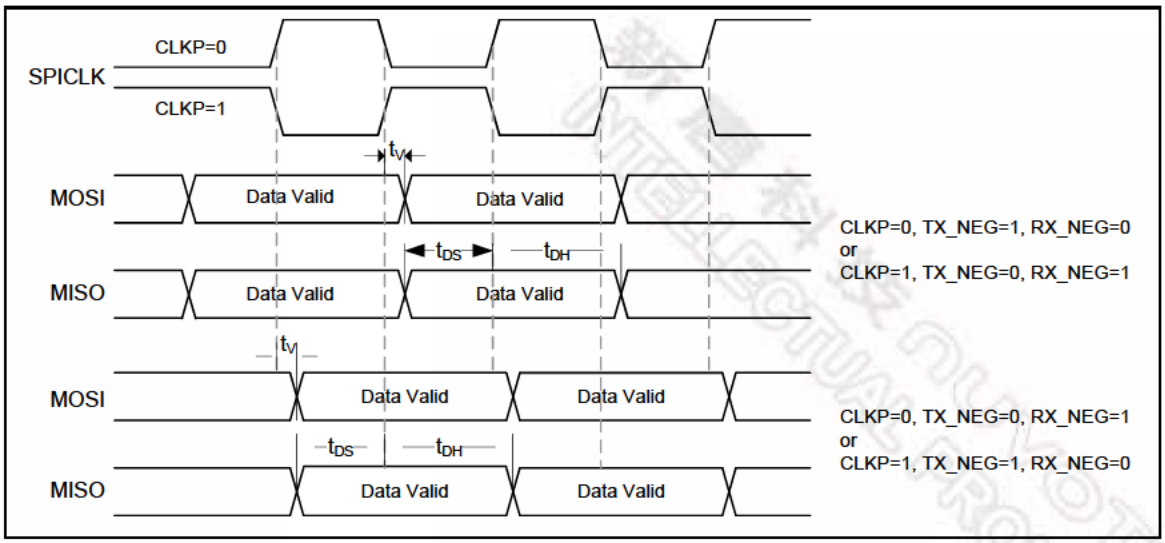


Figure 7-2 SPI Master Dynamic Characteristics Timing

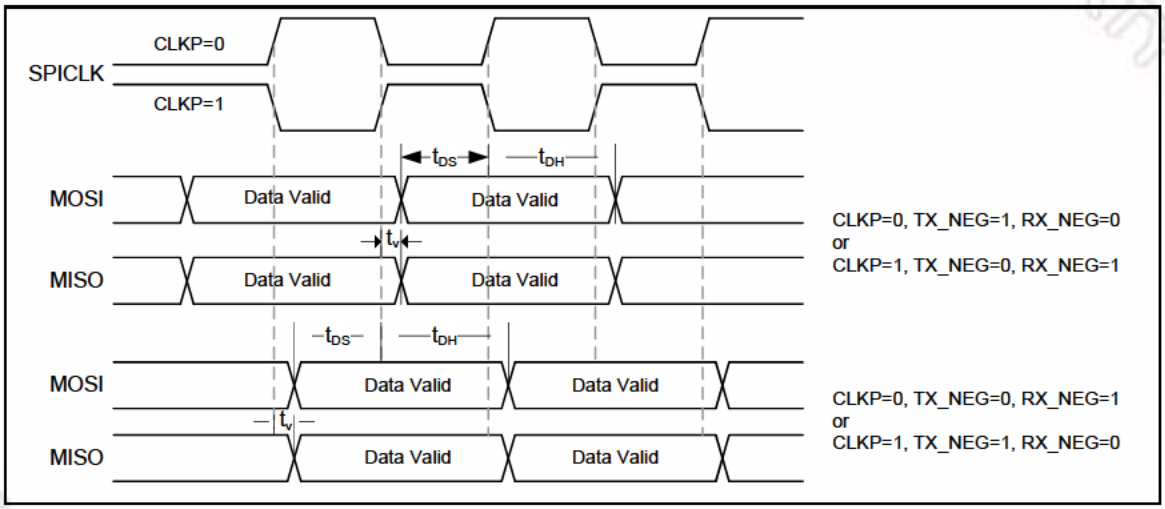


Figure 7-3 SPI Slave Dynamic Characteristics Timing

5.6 Flash DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
T_{ret}	Retention time	Temp=85 ℃	10			year
T_{erase}	Page erase time		19	20	21	ms
T_{mass}	Mass erase time		30	40	50	ms
T_{prog}	Program time		38	40	42	us

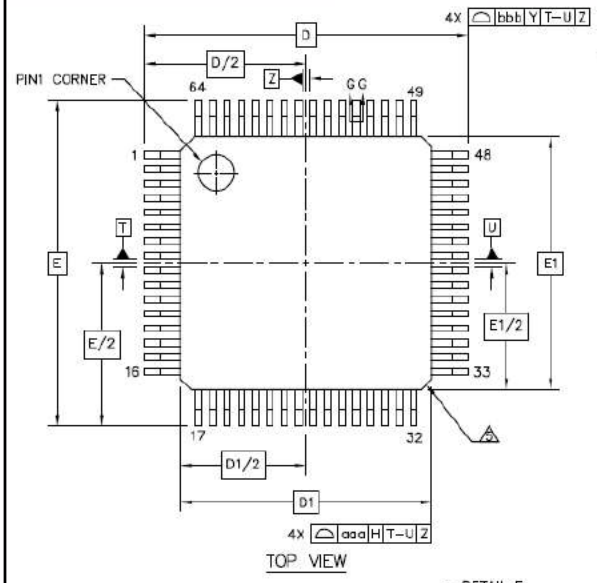
V_{DD}	Supply voltage		1.62	1.8	1.98	V[1]
I_{dd1}	Read current				0.25	mA
I_{dd2}	Program/Erase current				7	mA
I_{pd}	Power down current			1	20	uA

1. V_{DD} is source from chip LDO output voltage.

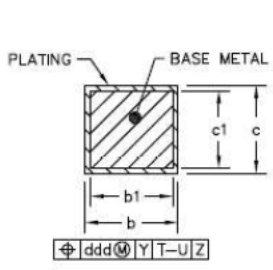
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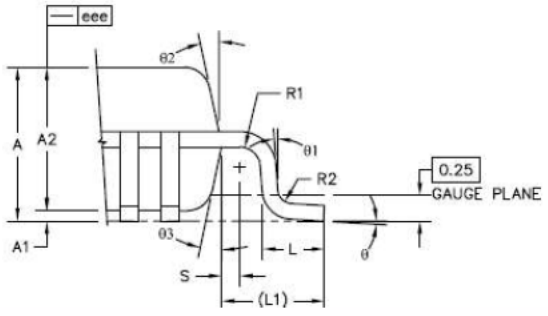
6 PACKAGE DIMENSIONS

6.1 64L LQFP (7x7x1.4 mm footprint 2.0 mm)

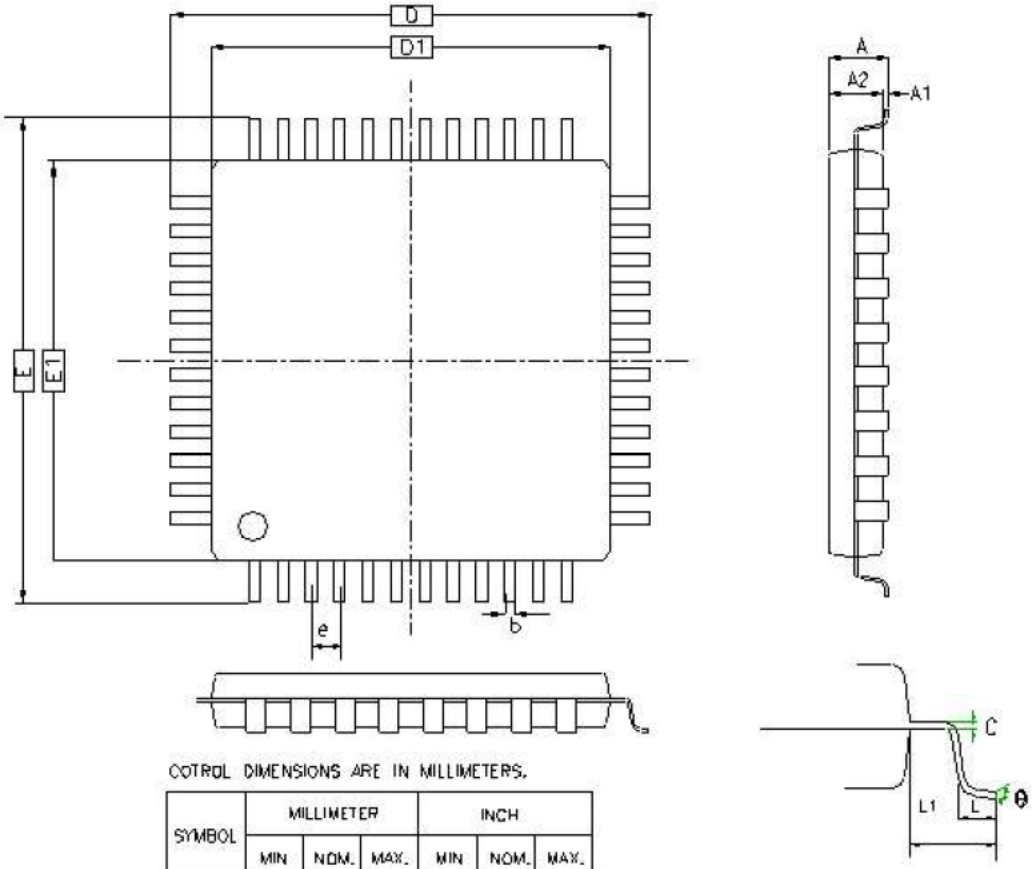


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		





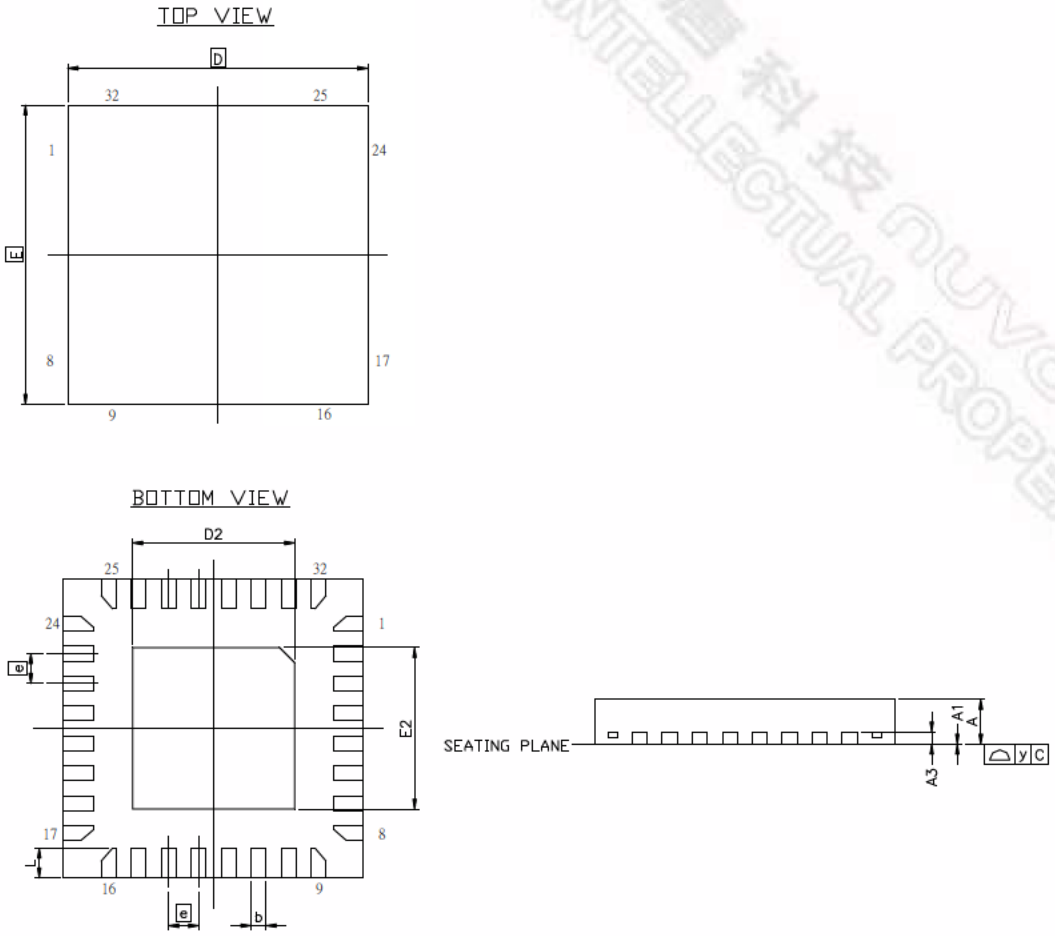
6.2 48L LQFP (7x7x1.4 mm footprint 2.0 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN	NOM.	MAX.	MIN	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D1	6.90	7.00	7.10	0.272	0.276	0.280
E1	6.90	7.00	7.10	0.272	0.276	0.280
e	0.35	0.50	0.65	0.014	0.020	0.280
D	8.9	9.00	9.10	0.350	0.354	0.358
E	8.9	9.00	9.10	0.350	0.354	0.358
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	—	1.00	—	—	0.039	—
C	0.09	—	0.20	0.0035	—	0.0079
θ	0°	—	7°	0°	—	7°
b	0.17	0.22	0.27	0.007	0.0087	0.011

6.3 33L QFN (5x5x0.8 mm)



SYMBOL	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0275	0.0295	0.0315
A1	0	0.02	0.05	0	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.18	0.25	0.30	0.007	0.010	0.012
D		5.00 BSC			0.197 BSC	
E		5.00 BSC			0.197 BSC	
e		0.50 BSC			0.0197 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020
y		0.10			0.0039	
D2	3.20	3.40	3.60	0.124	0.138	0.142
E2	3.20	3.40	3.60	0.124	0.138	0.142

7 REVISION HISTORY

VERSION	DATE	PAGE/ CHAPTER	DESCRIPTION
V1.00	Mar 27, 2012	-	Preliminary issued version
V1.01	May 2, 2012	Chap. 5	Updated Section 5.2 DC Electrical Characteristics
V1.02	May 7, 2012	Chap. 3	Updated Figure 3-1 NuMicro™ NUC123 Series Selection Code
V1.03	May 14, 2012	Chap. 3	Modified the Pin Assignment and Pin Description for LQFP 64-pin and LQFP 48-pin
V1.04	May 30, 2012	Chap. 3	Modified the Pin Assignment and Pin Description for PC.12 pin.
V1.05	July 20, 2012	Chap. 5	Removed 32.768kHz crystal characteristics in Section 5.3 AC Electrical Characteristics, Modified the capacitor value from 10uF to 1uF for the LDO pin in Section 5.4.2 LDO and Power Management Specifications.
V1.06	Aug. 21, 2012	Chap. 2 Chap. 4 Chap. 5	Updated the SPI item for "Master up to 32 MHz, and Slave up to 16 MHz" in Section 2.1 NuMicro™ NUC123 Features. Updated the Packages item for "LQFP 64-pin" in Section 2.1 NuMicro™ NUC123 Features. Updated Figure 4-1 NuMicro™ NUC123 Block Diagram. Updated the 10-bit SARADC Specifications in Section 5.4 Analog Characteristics.
V1.07	March 29, 2013	Chap. 3 Chap. 5	Removed the multi-function SPISS11 from PD.0 pin in Section 3.2.1 Pin Diagram. Corrected the output voltage 1.8V of LDO in Section 5.2.1 NuMicro™ NUC123 DC Electrical Characteristics and Section 5.4.2 LDO and Power Management Specifications. Added the new Section 5.6 Flash DC Electrical Characteristics.

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