



Nuvoton NuMicro™ Family

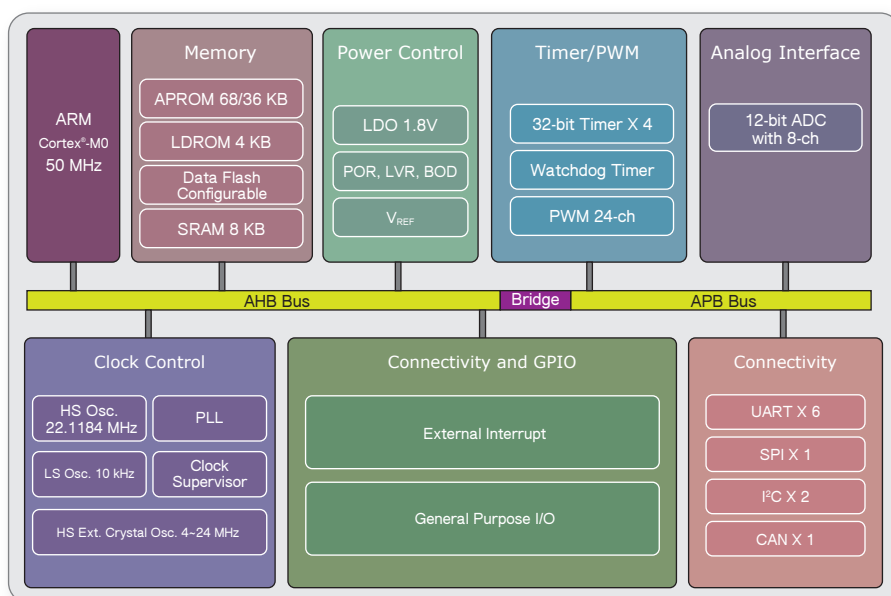
NuMicro™ NUC131 Series



Powerful Cortex®-M0 MCU with CAN
for Full Connectivity Applications

Applications

- ◆ Car Network Control
- ◆ Dashboard
- ◆ Elevator Network Control System
- ◆ Industrial and Auto-control



Selection Guide

| Part No. | Flash (Kbytes) | SRAM (Kbytes) | Data Flash | ISP ROM (Kbytes) | I/O | Timer (32-bit) | Connectivity | | | | | PWM (16-bit) | ADC (12-bit) | ICP ISP IAP | IRC 22 MHz | Package | Operating Temp. Range(°C) |
|------------------------|-------------------|------------------|---------------|------------------------|-----|-------------------|--------------|-----|-----|-----|-----|-----------------|-----------------|-------------------|------------------|---------|---------------------------------|
| | | | | | | | UART | SPI | I²C | LIN | CAN | | | | | | |
| NuMicro™ NUC131 Series | | | | | | | | | | | | | | | | | |
| NUC131LC2AE | 36 | 8 | Configurable | 4 | 42 | 4 | 6 | 1 | 2 | 3 | 1 | 24 | 8 | ✓ | ✓ | LQFP48 | -40 to +105 |
| NUC131LD2AE | 68 | 8 | Configurable | 4 | 42 | 4 | 6 | 1 | 2 | 3 | 1 | 24 | 8 | ✓ | ✓ | LQFP48 | -40 to +105 |
| NUC131SC2AE | 36 | 8 | Configurable | 4 | 56 | 4 | 6 | 1 | 2 | 3 | 1 | 24 | 8 | ✓ | ✓ | LQFP64* | -40 to +105 |
| NUC131SD2AE | 68 | 8 | Configurable | 4 | 56 | 4 | 6 | 1 | 2 | 3 | 1 | 24 | 8 | ✓ | ✓ | LQFP64* | -40 to +105 |

LQFP64*: 7x7mm

Contact us: NuMicro@nuvoton.com

❖ Features of NuMicro™ NUC131 Series

◆ ARM® Cortex®-M0 Core

- Runs up to 50 MHz
- One 24-bit system timer
- Single-cycle 32-bit hardware multiplier
- NVIC for the 32 interrupt inputs, each with 4-levels of priority
- Serial Wire Debug supports with 2 watchpoints/4 breakpoints

◆ Operating Voltage: 2.5 V ~ 5.5 V

◆ Memory

- 36/68 Kbytes Flash for program memory (APROM)
- 4 Kbytes Flash for ISP loader (LDROM)
- In-System-Program (ISP) and In-Application-Program (IAP) application code update
- 2-wired ICP update through SWD/ICE interface
- Supports fast parallel programming mode by external programmer

◆ SRAM

- 8 Kbytes SRAM

◆ Clock Control

- Built-in 22.1184 MHz high speed oscillator for system operation
 - Trimmed to $\pm 1\%$ at $+25^{\circ}\text{C}$ and $V_{DD} = 5\text{ V}$
 - Trimmed to $\pm 3\%$ at $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$ and $V_{DD} = 2.5\text{ V} \sim 5.5\text{ V}$
- Built-in 10 kHz low speed oscillator for Watchdog Timer and Wake-up operation
- Supports one PLL, up to 50 MHz, for high performance system operation
- External 4~24 MHz high speed crystal input

◆ GPIO

- Four I/O modes:
 - Quasi-bidirectional
 - Push-pull output
 - Open-drain output
 - Input only with high impedance
- TTL/Schmitt trigger input selectable
- I/O pin configured as interrupt source with edge/level setting

◆ Timer

- Four sets of 32-bit timers with 24-bit up-timer and one 8-bit prescale counter
- Independent clock source for each timer
- One-shot, Periodic, Toggle and Continuous Counting operation modes
- Event counting function and input capture function

◆ WDT

- Multiple clock sources:
 - System clock (HCLK)
 - Internal 10 kHz oscillator (LIRC)
- 8 selectable time-out period from 1.6 ms ~ 26.0 sec (depending on clock source)
- Wake-up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out

◆ WWDT

- 6-bit down counter with 11-bit prescale for wide range window time selection

◆ PWM/Capture

- Supports clock frequency up to 100 MHz
- Up to two PWM modules, each providing three 16-bit timers and six output channels
- Independent mode for PWM output/Capture input channels
- Complementary mode for three complementary paired PWM output channels:
 - Dead-time insertion with 12-bit resolution
 - Two compared values during one period

- 12-bit pre-scalar from 1 to 4096
- 16-bit resolution PWM counter
 - Up, down and up/down counter operation type
- Mask function and tri-state enable for each PWM pin
- Supports brake function:
 - Brake source from pin and system safety events (clock failed, Brown-out detection and CPU lockup)
 - Noise filter for brake source from pin
 - Edge detect brake source to control brake state until brake interrupt cleared
 - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
 - PWM counter matches zero, period value or compared value
 - Brake condition happened
- Supports trigger ADC on the following events:
 - PWM counter match zero, period value or compared value
- Up to 12 capture input channels with 16-bit resolution
- Rising edges, falling edges or both edges capture condition
- Input rising edges, falling edges or both edges capture interrupt
- Rising edges, falling edges or both edges capture with counter reload option

◆ UART

- Up to six UART controllers
- UART0 and UART1 ports with flow control (TXD, RXD, nCTS and nRTS)
- Auto baud-rate generator

◆ SPI

- One set of SPI controller
- SPI Master/Slave mode

◆ I²C

- Up to two sets of I²C devices
- Master/Slave mode

◆ CAN 2.0

- One set of CAN device
- CAN protocol version 2.0 part A and B
- Bit rates up to 1 Mbps
- 32 Message Objects
- Each Message Object has its own identifier mask
- Programmable FIFO mode (concatenation of Message Object)
- Maskable interrupt
- Disabled Automatic Re-transmission mode for Time Triggered CAN applications
- Power-down wake-up function

◆ ADC

- 12-bit SAR ADC with 1 MSPS
- Up to 8 channels single-end input or 4 channels differential input

◆ 96-bit unique ID (UID)

◆ Brown-out Detector and Low Voltage Reset

- With 4 levels: 4.4 V/3.7 V/2.7 V/2.2 V
- Brown-out Interrupt and Reset option
- Threshold voltage level: 2.0 V

◆ Operating Temperature: $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$

◆ Packages

- All Green package (RoHS)
- LQFP 64-pin / 48-pin