



Nuvoton NuMicro™ Family

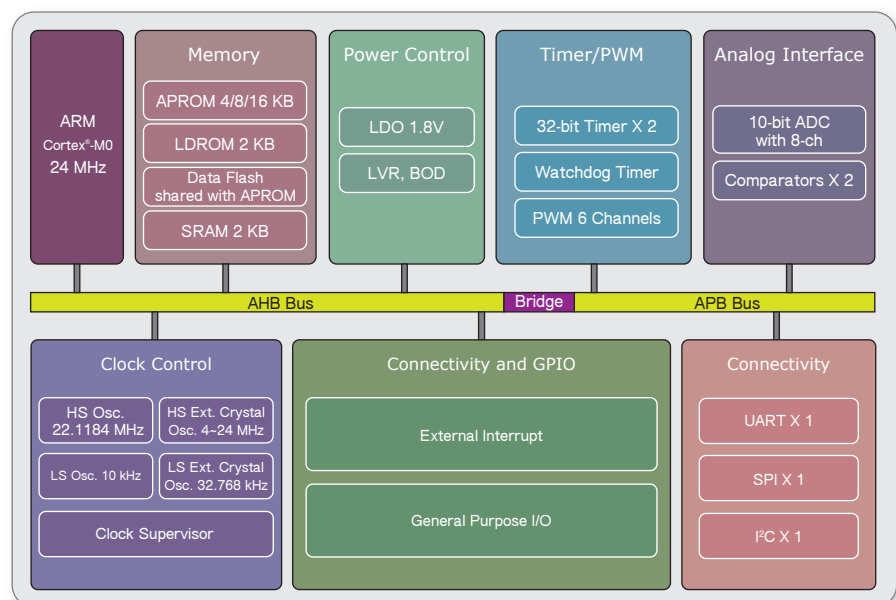
NuMicro™ Mini51 Series



High Performance Low Cost 32-bit Cortex®-M0
MCU with Rich Peripheral Functions

Applications

- ◆ Industrial Control
- ◆ Motor/Fan Control
- ◆ Aircraft Model
- ◆ Data Communication
- ◆ Auto-control System



Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash (Kbytes)	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity			PWM (16-bit)	ADC (10-bit)	Comparator	ICP ISP IAP	IRC 22 MHz	Package	Operating Temp. Range(°C)
							UART	SPI	I²C							
NuMicro™ Mini51 Base Series																
MINI51FDE	4	2	Configurable	2	17	2	1	1	1	3	4	-	√	√	TSSOP20	-40 to +105
MINI52FDE	8	2	Configurable	2	17	2	1	1	1	3	4	-	√	√	TSSOP20	-40 to +105
MINI54FDE	16	2	Configurable	2	17	2	1	1	1	3	4	-	√	√	TSSOP20	-40 to +105
MINI54FHC*	16	2	Configurable	2	17	2	1	1	1	6	3	-	√	√	TSSOP20	-40 to +105
MINI51TDE	4	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33*	-40 to +105
MINI52TDE	8	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33*	-40 to +105
MINI54TDE	16	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33*	-40 to +105
MINI51ZDE	4	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33**	-40 to +105
MINI52ZDE	8	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33**	-40 to +105
MINI54ZDE	16	2	Configurable	2	29	2	1	1	1	6	8	2	√	√	QFN33**	-40 to +105
MINI51LDE	4	2	Configurable	2	30	2	1	1	1	6	8	2	√	√	LQFP48	-40 to +105
MINI52LDE	8	2	Configurable	2	30	2	1	1	1	6	8	2	√	√	LQFP48	-40 to +105
MINI54LDE	16	2	Configurable	2	30	2	1	1	1	6	8	2	√	√	LQFP48	-40 to +105

PS: MINI54FHC for special module, are not compatible with MINI54FDE pin

QFN33*: 4x4mm
QFN33**: 5x5mm

Contact us: NuMicro@nuvoton.com

❖ Features of NuMicro™ Mini51 Series

◆ Core

- ARM® Cortex®-M0 core running up to 24 MHz
- One 24-bit system tick timer
- Low-power Idle mode
- Single-cycle 32-bit hardware multiplier
- NVIC for the 32 interrupt inputs, each with four levels of priority
- Serial Wire Debug (SWD) interface and two watch points/four breakpoints

◆ Built-in LDO for wide operating voltage from 2.5 V to 5.5 V

◆ Memory

- 4/8/16 Kbytes Flash memory for program memory (APROM)
- Configurable Flash memory for data memory (Data Flash)
- 2 Kbytes Flash for loader (LDROM)
- 2 Kbytes SRAM for internal scratch-pad RAM (SRAM)

◆ Clock Control

- Programmable system clock source
 - Switch clock sources on-the-fly
- 4 ~ 24 MHz external crystal input (HXT)
- 32.768 kHz external crystal input (LXT) for idle wake-up and system operation clock
 - Dynamically calibrating the HIRC OSC to 22.1184 MHz $\pm 1\%$ from -40°C to $+105^{\circ}\text{C}$ by external 32.768 kHz crystal oscillator (LXT)
- 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and idle wake-up

◆ I/O Port

- Up to 30 general-purpose I/O (GPIO) pins for LQFP-48 package
- Four I/O modes:
 - Quasi-bidirectional input/output
 - Push-Pull output
 - Open-Drain output
 - Input only with high impedance
- Optional Schmitt trigger input

◆ Timers

- 2 channels 32-bit timers; one 8-bit pre-scaler counter with 24-bit up-timer for each timer
 - Event Counter mode
 - Toggle Output mode
 - External trigger in Pulse Width Measurement mode
 - Supports external trigger in Pulse Width Capture mode

◆ Watchdog Timer

- Programmable clock source and time-out period
- Supports wake-up function in Power-down mode and Idle mode
- Interrupt or reset selectable on watchdog time-out

◆ PWM

- Up to three built-in 16-bit PWM generators, providing six PWM outputs or three complementary paired PWM outputs
- Individual clock source, clock divider, 8-bit pre-scalar and dead-zone generator for each PWM generator
- PWM interrupt synchronized to PWM period
- Supports edge alignment or center alignment
- Supports fault detection

◆ UART

- One UART device
- Buffered receiver and transmitter, each with 16-byte FIFO
- Optional flow control function (CTS_n and RTS_n)
- IrDA (SIR) function
- Programmable baud-rate generator up to 1/16 system clock
- RS-485 function

◆ SPI

- One SPI device
- Master up to 12 MHz, and Slave up to 4 MHz
- Master/Slave mode
- Full-duplex synchronous serial data transfer
- Variable length of transfer data from 1 to 32 bits
- MSB or LSB first data transfer
- RX latching data can be either at rising edge or at falling edge of serial clock
- TX sending data can be either at rising edge or at falling edge of serial clock
- Supports Byte Suspend mode in 32-bit transmission

◆ I²C

- Master/Slave mode
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- Programmable clocks allow for versatile rate control
- Multiple address recognition (four slave addresses with mask option)

◆ ADC

- 10-bit SAR ADC with 250 KSPS
- Up to 8 channels single-end input and one internal input from band-gap
- Conversion started either by software trigger or external pin trigger

◆ Analog Comparator

- Two analog comparators with programmable 16-level internal voltage reference
- Built-in CRV (comparator reference voltage)

◆ ISP (In-System Programming) , ICP (In-Circuit Programming) and IAP (In-Application Programming)

◆ Brown-out Detector

- With 4 programmable threshold levels: 4.4V/3.7V/2.7V/2.2V
- Supports Brown-out interrupt and reset option

◆ 96-bit unique ID

◆ Low Voltage Reset

- Threshold voltage level: 2.0V

◆ Operating Temperature

- $-40^{\circ}\text{C} \sim +105^{\circ}\text{C}$

◆ Reliability

- EFT $> \pm 4\text{KV}$, ESD HBM pass 4KV

◆ Code Security and Series Number

- 96-bit unique ID
- 128-bit unique customer ID

◆ Packages

- Green package (RoHS)
- 48-pin LQFP (7x7), 33-pin QFN (5x5) , 33-pin QFN (4x4), 20-pin TSSOP