



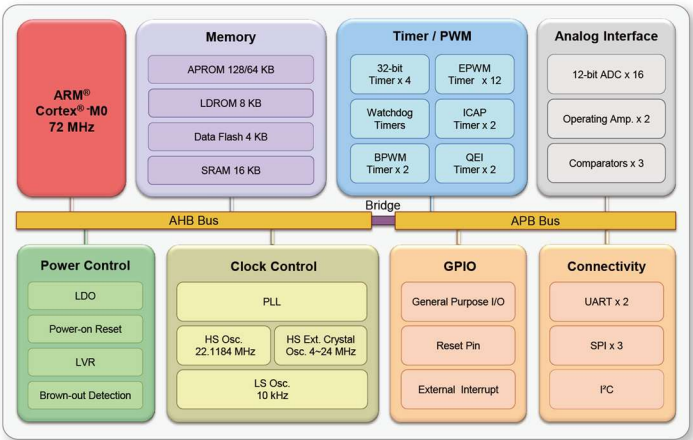
Nuvoton NuMicro® Family

NuMicro® M0519 Series

High Performance MCU with Two Embedded OPAs and Independent ADCs

Applications

- ◆ Electrical Power control
- ◆ Industrial Control
- ◆ Industrial Automation
- ◆ Robotic Toys



Selection Guide

Part No.	Flash (Kbytes)	SRAM (Kbytes)	Data Flash (Kbytes)	ISP ROM (Kbytes)	I/O	Timer (32-bit)	Connectivity				QEI	PWM (16-bit)	ADC (12-bit)	Comparator	OPA	Capture	ICP (AP/ISP)	IRC 22 MHz	Package	Operating Temp. Range (°C)
							UART	SPI	I2C	LIN										
M0519LD3AE	64	16	4	8	38	4	2	1	1	2	-	6	x2, 16-ch	2	2	-	√	√	LQFP48	-40 to +105
M0519LE3AE	128	16	4	8	38	4	2	1	1	2	-	6	x2, 16-ch	2	2	-	√	√	LQFP48	-40 to +105
M0519SD3AE	64	16	4	8	51	4	2	2	1	2	1	10	x2, 16-ch	2	2	-	√	√	LQFP64*	-40 to +105
M0519SE3AE	128	16	4	8	51	4	2	2	1	2	1	10	x2, 16-ch	2	2	-	√	√	LQFP64*	-40 to +105
M0519VE3AE	128	16	4	8	82	4	2	3	1	2	2	14	x2, 16-ch	3	2	6	√	√	LQFP100	-40 to +105

LQFP64*: 7x7mm

Contact us: NuMicro@nuvoton.com

❖ Features of NuMicro® M0519 Series

◆ Core

- ARM® Cortex® -M0 core running up to 72 MHz
- One 24-bit system timer
- Supports Low Power Sleep mode by WFI instructions
- Single-cycle 32-bit hardware multiplier
- Supports programmable 4 level priorities of Nested Vectored Interrupt Controller (NVIC)

◆ Built-in LDO for wide operating voltage from 2.5V to 5.5V

◆ Memory

- 128/64 KB Flash for program memory (APROM)
- 4 KB Flash for data memory (Data Flash)
- 8 KB Flash for loader (LDROM)
- 16 KB embedded SRAM

◆ Clock Control

- Built-in 22.1184 MHz internal high speed RC oscillator (HIRC) for system operation (variation < 2% at -40°C ~ +105°C)
- Built-in 10 kHz internal low-speed RC oscillator (LIRC) for Watchdog Timer and wake-up operation
- Built-in 4~24 MHz external high-speed crystal oscillator (HXT) for precise timing operation
- Supports one PLL up to 72 MHz for high performance system operation, sourced from HIRC and HXT Embedded Hardware divider
- Supports signed 32-bit dividend, 16-bit divisor operation

◆ GPIO

- Four I/O modes
- TTL/Schmitt trigger input selectable
- Bit control available
- I/O pin configured as interrupt source with edge/level trigger setting
- Supports high driver and high sink current I/O (up to 16 mA at 5V)
- INT0 and INT1 pins with individual interrupt vectors
- Supports up to 82/51/38 GPIOs for LQFP100/64/48 respectively

◆ Timers

- Supports 4 sets of 32-bit timers with 24-bit up-timer and one 8-bit prescaler counter
- Provides One-shot, Periodic, Toggle and Continuous Counting operation modes
- Supports event counting function to count the event from external pin

◆ Watchdog Timer

- Supports multiple clock sources from LIRC (default selection) and HCLK/2048
- 8 selectable time-out periods from 1.6ms ~ 26.0 sec (depending on clock source)
- Able to wake up from Power-down or Idle mode
- Interrupt or reset selectable on watchdog time-out
- Selectable time-out reset delay period time

◆ Window Watchdog Timer

- Supports multiple clock sources from HCLK/2048 (default selection) and LIRC
- Window set by 6-bit counter with 11-bit prescale
- Able to wake up from Power-down or Idle mode

◆ Basic PWM

- Up to 2-channel basic PWM outputs with 16-bit resolution
- Alternative function as input capture timer

◆ Enhanced PWM

- Up to two 6-channel enhanced PWM outputs with 16-bit resolution with dead-zone control, brake and polarity control for motor drive
- Default tri-state during any reset

◆ Enhanced Input Capture

- Up to 2 units of 24-bit input capture
- Each unit has 3 inputs: IC0, IC1 and IC2

◆ QEI (Quadrature Encoder Interface)

- Up to 2 units of Quadrature Encoder Interface
- Each unit has 3 inputs: QEIA, QEIB and IDX

◆ UART

- Up to two 16550 compatible UART devices
- Programmable baud-rate generator
- Buffered receiving and transmitting, each with 16 bytes FIFO
- Supports flow control (TX, RX, CTS and RTS)
- Supports IrDA (SIR) function
- Supports RS-485

◆ SPI

- Up to three sets of SPI devices
- Supports SPI master/slave mode
- Full duplex synchronous serial data transfer
- Variable length of transfer data from 8 to 32 bits

◆ I²C

- Master/Slave up to 1 Mbit/s
- Bi-directional data transfer between masters and slaves
- Multi-master bus (no central master)
- Arbitration between simultaneously transmitting masters
- Programmable clocks allowing for versatile rate control
- Multiple address recognition (four slave address with mask option)

◆ ADC

- Two A/D converters with up to 8 channels, 12-bit resolution respectively
- 16 result registers
- Sampling rate up to 800 KSPS
- Two operating modes

◆ Up to three Analog Comparators

◆ Up to two OPAs (operational amplifiers)

◆ Brown-out detector

- 4 levels: 4.4V/3.7V/2.7V/2.2V
- Brown-out interrupt or reset (optional)

◆ Built-in LDO for wide operating voltage from 2.5V to 5.5V

◆ Low Voltage Reset

◆ 96-bit unique ID

◆ Operating Temperature: -40°C ~ +105°C

◆ Packages:

- All Green package (RoHS)
- LQFP 100/64/48-pin