

# Interworking of MA35D1 RTP and Linux

Application Note for 64-bit MPU Family

#### **Document Information**

Abstract	This document introduces the interworking between programs running at MA35D1 RTP M4 and Linux kernel. It also introduces the development environment of RTP M4.
Apply to	NuMicro <sup>®</sup> MA35D1 series.

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## 1. Overview

The NuMicro MA35D1 series microprocessor (MPU) platform is based on dual 64/32-bit Arm<sup>®</sup> Cortex-A35 cores at Armv8-A architecture and an Arm Cortex-M4 core at ARMv7-M architecture. The MA35D1 series microprocessor system allows users to run independent firmware on each CPU core according to different needs.

The software currently provided by MA35D1 runs Linux on the Cortex-A35, and can run RTOS or bare-metal application on the RTP M4 which is a Cortex-M4 core. In this document, RTP M4 refers to the Cortex-M4 core in MA35D1.

The RTP M4 is not equipped with any non-volatile storage, such as Flash. The Cortex-M4 executable image always executes from the internal SRAM of the RTP M4. The MA35D1 supports mapping RTP M4 memory space 0x20000 ~ 0x3FFFFF to DDR offset 0x2000 ~ 0x3FFFFF. But in Linux, RTP M4 can only use 0x20000 ~ 0x7FFFF because Linux kernel image starts from DDR 0ffset 0x80000. The maximum size of RTP M4 executable area is 0x80000 which includes the run-time memory.

The Cortex-A35 can load executable images into the dedicated 128 KB SRAM of RTP M4 simply by memory copy. For images larger than 128 KB, the portion over 128 KB will be loaded to DDR offset 128 KB.

Nuvoton provides Nu-Link2-Pro ICE plugin for Keil, Eclipse, and IAR, in which users can also load executable images into RTP M4 and perform debug or run code. MA35D1 adopts the Linux remoteproc framework to load the RTP M4 firmware to RTP M4 SRAM. From the Cortex-A35 view, RTP M4 SRAM is mapped to address space 0x24000000 ~ 0x2401FFFF. From the RTP M4 view, the SRAM is mapped to address space 0x00000000 ~ 0x0001FFFF. Related instructions will be detailed in section 2.1.1.

The MA35D1 Wormhole Controller (WHC) supports bi-dir4ectional data exchange between Cortex-A35 and RTP M4. WHC is a controller provided by MA35D1 to handle the interprocessor communication between Cortex-A35 and RTP M4. MA35D1 Linux RTP ecosystem uses WHC to transfer simple commands, and uses share memory to transfer a larger amount of data. However, it should be noted that the current MA35D1 software only provides a way to use share memory to transfer data, not provide a way to directly let the user control WHC to send command.

The MA35D1 Linux BSP supports the driver for Linux rpmsg framework for Cortex-A35 to send and receive data to RTP M4. And MA35D1 RTP BSP supports for building software code running under the OpenAMP framework, which can support send and receive data to Cortex-A35. OpenAMP is a standardized embedded multi-core framework, whose purpose is to enable RTOS and bare metal programs developed in AMP (Asymmetric Multiprocessing) system design to communicate with the interface provided by the open source Linux community. Related instructions detail in section 2.1.2 and 2.2.1.

In addition, due to the memory space shared between different cores, it is necessary to implement a synchronization mechanism to prevent different cores from accessing the same memory space and causing unpredictable behavior. The Hardware Semaphore module of MA35D1 provides eight hardware semaphores, by which users can manage the synchronization between different processors with semaphore keys. Related instructions detail in section 2.1.4 and 2.2.2.

The MA35D1 also provides a system security peripheral configuration controller (SSPCC), which can configure the security attribute of all peripherals, such as SRAM and GPIO. The user determines a peripheral resource be allocated to Cortex-A35 or Cortex-M4 by programming SPPCC. In the MA35D1 Linux platform, only Secure Monitor of TF-A can program SSPCC because SSPCC is secure-only while Linux kernel in running under non-secure mode. Related instructions detail in section 2.1.3. For detailed introduction of Trusted Firmware-A (TF-A), please refer to "NuMicro<sup>®</sup> Family MA35D1 TF-A User Manual".

# 2. Cortex-A35 and Cortex-M4 Management

## 2.1 Cortex-A35

### 2.1.1 Loading Cortex-M4 Firmware

Since the RTP M4 does not have its own Flash, the required firmware needs to be loaded from outside of RTP M4. In addition to using Nu-Link2-Pro ICE, the MA35D1 supports to load executable images into RTP M4 SRAM from the Cortex-A35 side using the Linux built-in remoteproc framework. Of course, the user needs to copy the compiled firmware to the Linux file system before using the Cortex-A35 to load the RTP M4 images. Currently Linux only supports loading firmware in ELF format. Users can also use the remoteproc driver to start/stop RTP M4 CPU execution.

Figure 2-1 is a schematic diagram of Cortex-A35 loading Cortex-M4 executable image and starting/stopping RTP M4 by Cortex-A35.



Figure 2-1 Load and Start/Stop RTP M4 Image

To support RTP M4 applications that require memory larger than 128 KB, the MA35D1 supports to map RTP M4 memory space 0x20000 ~ 0x3FFFFF to DDR offset 0x20000 ~ 0x3FFFFF. However, due to Linux kernel image locates at DDR offset 0x80000, available DDR memory is reduced to 0x20000 ~ 0x7FFFF under Linux. As a result, the maximum memory available for a RTP M4 application is 512 KB under MA35D1 Linux platform.

Figure 2-2 shows the memory map of MA35D1 Cortex-A35 and RTP M4. For an image small than 128 KB, Linux will always load it to RTP M4 internal SRAM. For an image larger than 128 KB, Linux will load the first 128 KB to RTP M4 SRAM, and load the remaining to DDR offset 0x20000, which is 0x80020000 from Linux view.



Figure 2-2 Linux RTP Memory Map

The following introduces how users can use Linux's remoteproc framework to load RTP M4 images and start/stop RTP M4.

Before starting to run the Linux kernel, users need to set up the kernel configuration and device tree. After the setting is complete, you need to recompile and run the Linux kernel.

The following are the kernel configuration and device tree settings:

1. Set the Linux kernel configuration to enable the MA35D1 remoteproc driver.

```
Device Drivers --->
Remoteproc drivers --->
[*] Support for Remote Processor subsystem
<*> MA35D1 remoteproc support
```

2. Device tree configuration.

The device tree node setting of remoteproc:

```
rproc {
    compatible = "nuvoton, ma35d1-rproc";
    mboxes = <&wormhole 1>;
    resets = <&reset MA35D1_RESET_CM4>;
};
```

After starting the Linux kernel, user can load and start/stop the remote processor firmware through the sysfs interface. (The sysfs filesystem is a pseudo-filesystem which provides an interface to kernel data structures).

The sysfs interface description is as follows:

#### 1. Add a new firmware path

The firmware components are stored in the file system, by default in the /lib/firmware/ folder. Optionally another location can be set. In this case, the remoteproc framework parses this new path in priority. The below command adds a new path for firmware parsing:

\$> echo -n <firmware\_path> > /sys/module/firmware\_class/parameters/path

#### 2. Rename the firmware file name

If the firmware elf filename differs from the default one (rproc-%s-fw), set the name with the following command: (replace X with remoteproc instance number: 0 by default)

\$> echo -n <firmware\_name.elf> > /sys/class/remoteproc/remoteprocX/firmware

3. Load and start the firmware

Users can use the following command to load and start the firmware:

\$> echo start > /sys/class/remoteproc/remoteprocX/state

4. Stop the firmware

Users can use the following command to stop the firmware:

\$> echo stop > /sys/class/remoteproc/remoteprocX/state

#### 2.1.2 Communication with Cortex-M4

The MA35D1 can load RTP M4 firmware from Cortex-A35, and provide WHC and shared memory. Cortex-A35 and RTP M4 perform command handshaking through WHC and exchange mass data through the shared memory. The MA35D1 provides (4M - 128K) bytes share memory of which memory address space is 0x8002\_0000 ~ 0x803F\_FFFF from the Cortext-A35 view. From the RTP M4 view, shared memory address space is 0x0002\_0000 ~ 0x003F\_FFFF.

The MA35D1 and RTP M4 communicate with each other using the message passing mechanism of Linux RPMsg framework. The Linux RPMsg framework can set the address and size of shared memory and use the file system for messages that the user wants to receive/transmit to remote CPUs via shared memory. That is to say, users can easily communicate with the remote processor by means of read/write files.

Figure 2-3 is a schematic diagram of Cortex-A35 using RPMsg framework to communicate with RTP M4.



Figure 2-3 Linux RPMsg Framework

The following introduces how users can use Linux's RPMsg framework to communicate with RTP M4.

Before starting to run the Linux kernel, users need to set up the kernel configuration and device tree. After the setting is complete, you need to recompile and run the Linux kernel.

The following are the kernel configuration and device tree settings:

1. kernel configuration to enable the MA35D1 rpmsg driver

```
Device Drivers --->

Rpmsg drivers --->

-*- RPMSG device interface

<*> MA35D1 Shared Memory Driver
```

2. Device tree configuration

The device tree node setting of rpmsg:

"compatible" should be set to "nuvoton, ma35d1-rpmsg", which can load the rpmsg driver.

compatible = "nuvoton, ma35d1-rpmsg";

"share-mem-addr" defines share memory address and should be 0x2401FF00.

share-mem-addr = <0x2401FF00>;

"tx-smem-size" defines tx share memory size and should be 128.

rpmsg {

tx-smem-size = <128>;

"rx-smem-size" defines rx share memory size and should be 128.

```
rx-smem-size = <128>;
```

};

After starting the Linux kernel, users can follow the steps below to send/receive messages to/from a remote CPU via shared memory:

1. Open rpmsg control device, for example:

open("/dev/rpmsg\_ctrl0", 0\_RDWR | 0\_NONBLOCK);

2. Create rpmsg end point, for example:

ioctl(rpfd, RPMSG\_CREATE\_EPT\_IOCTL, eptinfo);

and open rpmsg endpoint, for example:

```
open("/dev/rpmsg0", O_RDWR | O_NONBLOCK);
```

3. Use write/read function to send/receive messages to/from a remote CPU via shared memory, for example:

```
write(fd, Tx_Buffer, 128); // send message
read(fd, Rx Buffer, 128); // read message
```

4. In addition to the above steps, the user can also use the polling function to confirm that the write function has sent a message to the shared memory and RTP M4 has received the message, or use the polling function to confirm that there is a message from RTP M4 in the shared memory. Shared memory, and then use the read function to read the message.

The following is an example of a program that uses rpmsg to communicate between the master and slave processors.

```
struct rpmsg_endpoint_info {
    char name[32];
    __u32 src;
    __u32 dst;
};
static int rpmsg_create_ept(int rpfd, struct rpmsg_endpoint_info *eptinfo)
{
    int ret;
    ret = ioctl(rpfd, RPMSG_CREATE_EPT_IOCTL, eptinfo);
    if (ret)
        perror("Failed to create endpoint.\n");
    return ret;
}
```

```
int main(int argc, char **argv)
{
     char *dev[10]={"/dev/rpmsg_ctrl0", " "};
     unsigned int i;
     int rev1, rev2;
     struct rpmsg_endpoint_info eptinfo;
     int ret;
     int err;
     unsigned char Tx_Buffer[130];
     unsigned char Rx_Buffer[130];
     fd[0] = open("/dev/rpmsg_ctr10", O_RDWR | O_NONBLOCK);
     if (fd[0] < 0) {
           perror("Failed to open \n");
           return 0;
     }
     strcpy(eptinfo.name, "rpmsg-test");
     eptinfo.src = 0;
     eptinfo.dst = 0xFFFFFFF;
     ret = rpmsg create ept(fd[0], &eptinfo);
     if (ret) {
           perror("Failed to create RPMsg endpoint.\n");
           return -EINVAL;
     }
     fd[1] = open("/dev/rpmsg0", O_RDWR | O_NONBLOCK);
     if (fd[1] < 0) {
           perror("Failed to open rpmsg0 \n");
           return -EINVAL;
     }
     while(1)
     {
           struct pollfd fds[] = {
                {
                      .fd = fd[1],
                      .events
                                 = POLLOUT,
                },
```

```
};
     for(i = 0; i < 128; i++)
     {
          Tx_Buffer[i] = (255-i);
     }
     rev1 = write(fd[1], Tx_Buffer, 10);
     if (rev1 < 0) {
           perror("Failed to write \n");
           return -EINVAL;
     }
     while(1) // wait send message finish
     {
           err = poll(fds, 1, 10000);
           if((err == -1) || (err == 0))
           {
           }
           else
          {break;}
     }
    break;
}
while(1)
{
     struct pollfd fds[] = {
          {
                .fd = fd[1],
                .events = POLLIN,
          },
     };
     while(1) // wait share memory receive message
     {
          err = poll(fds, 1, 10000);
           if((err == -1) || (err == 0))
           {
           }
           else
```

```
{break;}
}
rev1 = read(fd[1], Rx_Buffer, 128);
if (rev1 < 0) {
    perror("Failed to read \n");
    return -EINVAL;
}
printf("\n Receive %d bytes data from M4: \n", rev1);
for(i = 0; i < rev1; i++)
{
    printf(" 0x%x, \n", Rx_Buffer[i]);
}
return 0;</pre>
```

### 2.1.3 Assigning Internal Peripheral Resources

Users can assign internal peripheral resources to the master processor or slave processor by programming SSPCC with TF-A (Trusted Firmware-A).

On assigning the ownership of a peripheral device, the user must also assign the corresponding ownerships of GPIO pins used by that device.

The following is the device node sample, which describes the attribute of SSPCC.

sspcc: sspcc@404F0000 {

"compatible" must set to "nuvoton,ma35d1-sspcc". Register base address of System security peripheral configuration controller (SSPCC) is 0x404F0000.

```
compatible = "nuvoton,ma35d1-sspcc";
reg = <0x0 0x404F0000 0x0 0x1000>;
```

"config" sets all peripherals' attribution. It includes NAND, SDH, UART, Timer, SPI, Crypto, etc. The secure attribute of each peripheral is one of TZS (secure), TZNS (non-secure), and subM (RTP M4). The secure attribute of all peripherals are defined in *plat/nuvoton/ma35d1/includes/sspcc.h*. This header file lists all the peripherals whose attribute to be changed. The attribute of peripherals not listed here remains power-on by default. The following example assigns UART1 secure attribute to subM (RTP M4).

AN0064

};

As to the configuration of SRAM0, the 128 KB SRAM0 is for RTP M4 to retain code and data. By default, the whole SRAM0 is shared between RTP M4 and Cortex-A35. To prevent the SRAM0 from being unexpectedly modified by Cortex-A35 after RTP M4 is powered up and executed, SSPCC provides a feature that can configure certain range of SRAM to be that only RTP M4 has access right.

The SR0BOUND(SSPCC\_SRAMSB[4:0]) is used to set a 16 Kbytes-aligned boundary region starting from offset 0 of SRAM0 that can only access by RTP M4. The region above the boundary will be the share memory between Cortex-A35 and RTP M4.

### 2.1.4 Hardware Semaphore

Since some memory area are shared by different cores, it is necessary to implement a synchronization mechanism to prevent from concurrent accessing to the same memory area and resulting in memory inconsistence. The MA35D1 Hardware Semaphore provides eight hardware semaphores, which can support synchronization between different cores by the semaphore keys.

The driver for MA35D1 hardware semaphore is:

• drivers/hwspinlock/ma35d1\_hwsem.c

Please follow the setting below to enable MA35D1 hardware semaphore support.

```
Device Drivers --->
```

[\*] Hardware Spinlock drivers --->

<\*> MA35D1 Hardware Semaphore support

The followings describe the hardware semaphore node in the MA35D1 device tree.

The base address of hwsem controller is 0x40380000.

hwsem: hwspinlock@40380000 {

"compatible" must be set to "nuvoton,ma35d1-hwsem".

compatible = "nuvoton,ma35d1-hwsem";

"reg" defines the base address and size of hardware semaphore control register.

reg = <0x0 0x40380000 0x0 0x1000>;

Set "okay" to enable hardware semaphore; otherwise, set to "disable".

```
status = "okay";
```

};

Also, users can learn more about Hardware Spinlock Framework using the following links. <u>https://www.kernel.org/doc/Documentation/hwspinlock.txt</u>

### 2.1.5 Power Down / Wakeup

The MA35D1 can make Cortex-A35 and RTP M4 enter Power-down mode respectively. Under Linux command shell, using the following command can make Cortex-A35 enter the Power-down mode, which writes "mem" into /sys/power/state.

#### \$ echo mem > /sys/power/state

After Cortex-A35 core enters Power-down mode, internal interrupts generated from MA35D1 peripheral devices, for example WHC and RTC, and external interrupts generated from external devices, for example USB, can wake up the Cortex-A35 core. Users need to refer to the MA35D1 user manual to know how to use different devices to wake up the Cortex-A35 core. Likewise, after the RTP M4 enters Power-down mode, interrupts generated by those MA35D1 devices with "subM" security attribute can wake up RTP M4.

It is also worth noting that when the Cortex-A35 enters Power-down mode, the DDR will enter self-refresh mode. At this time, the DDR cannot be accessed. Therefore, the firmware running on the RTP M4 should never access the shared memory located in the DDR. However, when the RTP-M4 goes into Power-down mode, the Cortex-A35 does not have this limitation.

### 2.2 RTP M4

### 2.2.1 Using OpenAMP Control Share Memory

OpenAMP (Open Asymmetric Multi-Processing) is a framework providing the software components needed to enable the development of software applications for AMP systems. It allows operating systems to interact within a broad range of complex homogeneous and heterogeneous architectures and allows asymmetric multiprocessing applications to leverage parallelism offered by the multicore configuration.

The MA35D1 RTP M4 supports OpenAMP framework for users to use this framework to communicate with Cortex-A35.

The OpenAMP architecture on the RTP M4 side of the MA35D1 is very similar to that of the Linux rpmsg framework. Users can refer to Figure 2-3.

Follow the steps below to send data to or receive data from share memory:

1. Execute MA35D1\_OpenAMP\_Init(int RPMsgRole, rpmsg\_ns\_bind\_cb ns\_bind\_cb) to initialize mailbox (WHC) and share memory.

The parameter "RPMsgRole" should be "RPMSG\_REMOTE" and "ns\_bind\_cb" be "NULL", for example,

MA35D1\_OpenAMP\_Init(RPMSG\_REMOTE, NULL);

2. Execute OPENAMP\_create\_endpoint(struct rpmsg\_endpoint \*ept, const char \*name, uint32\_t dest, rpmsg\_ept\_cb cb, rpmsg\_ns\_unbind\_cb unbind\_cb) to create rpmsg endpoint.

Users create a struct rpmsg\_endpoint and set the address of this struct to the parameter "\*ept". Users can also set endpoint name to parameter "\*name". The parameter "dest" should be "RPMSG\_ADDR\_ANY". The parameter "cb" is the call back function. When the endpoint data received, the call back function will be called. Then users can get share

memory data in this call back function.

```
static int rx_callback(struct rpmsg_endpoint *rp_chnl, void *data, size_t len, uint32_t
src, void *priv)
{
    uint8_t received_rpmsg[128];
    //Users can get shared memory data from address "src" and size is "len"
    memcpy((void *)received_rpmsg, (const void *)src, len);
}
int32_t main (void)
{
    struct rpmsg_endpoint resmgr_ept;
    OPENAMP_create_endpoint(&resmgr_ept, "rpmsg-sample", RPMSG_ADDR_ANY, rx_callback,
NULL);
```

3. Use OPENAMP\_check\_for\_message() to wait for new data from linux.

```
struct rpmsg_endpoint resmgr_ept;
OPENAMP_check_for_message(&resmgr_ept);
```

4. Use OPENAMP\_send\_data() to send new data to Linux and use OPENAMP\_check\_TxAck() to wait for a response from Linux, which means Linux has received new data.

```
struct rpmsg_endpoint resmgr_ept;
uint8_t transmit_rpmsg[128];
// Send data to Cortex-A35
OPENAMP_send_data(&resmgr_ept, transmit_rpmsg, 5);
while(1)
{
    // check Cortex-A35 response ack
    if(OPENAMP_check_TxAck(&resmgr_ept) == 1)
      break;
}
```

5. The following is an example of controlling shared memory:

```
#define M4_COMMAND_ACK 0x81
static uint32_t rx_status = 0;
#define tx_rx_size 128
uint8_t received_rpmsg[tx_rx_size];
```

{

{

```
uint8 t transmit rpmsg[tx rx size];
static int rx callback(struct rpmsg endpoint *rp chnl, void *data, size t len, uint32 t
src, void *priv)
{
    uint32_t *u32Command = (uint32_t *)data;
    uint32_t i;
    if(*u32Command == COMMAND RECEIVE A35 MSG)
    {
        memcpy((void *)received rpmsg, (const void *)src, len > sizeof(received rpmsg) ?
sizeof(received_rpmsg) : len);
        printf("\n Receive %d bytes data from Cortex-A35: \n", len);
        for(i = 0; i < len; i++)</pre>
        {
            printf(" 0x%x \n", received_rpmsg[i]);
        }
        rx status = 1;
    }
    else
    {
        printf("\n unknow command!! \n");
    }
    return 0;
}
int32_t main (void)
{
    struct rpmsg_endpoint resmgr_ept;
    uint32_t i;
    int ret;
    MA35D1 OpenAMP Init(RPMSG REMOTE, NULL);
    OPENAMP_create_endpoint(&resmgr_ept, "rpmsg-sample", RPMSG_ADDR_ANY, rx_callback,
NULL);
    while(1) // wait message from A35
    {
        OPENAMP_check_for_message(&resmgr_ept);
```

```
if(rx_status)
        {
            rx_status = 0;
            break;
        }
    }
    for(i = 0; i < tx_rx_size; i++)</pre>
    {
       transmit_rpmsg[i] = i;
    }
   // send message to Cortex-A35
    ret = OPENAMP_send_data(&resmgr_ept, transmit_rpmsg, 5);
    if (ret < 0)
    {
        printf("Failed to send message\r\n");
    }
    printf("\n Transfer %d bytes data to Cortex-A35 \n", ret);
    while(1) // wait send message finish and Cortex-A35 response ack
    {
        if(OPENAMP_check_TxAck(&resmgr_ept) == 1)
        break;
    }
    while(1);
}
```

## 3. Hardware Semaphore

The hardware semaphores on the RTP M4 side can be controlled by setting the HWSEM\_SEM0 ~ HWSEM\_SEM7 registers.

Registers HWSEM\_SEM0 ~ HWSEM\_SEM7 can be accessed by both Cortex-A35 and RTP M4, and are used to control the eight semaphores for synchronization. A write to these register will try to hold the semaphore. ID (HWSEM\_SEMx[3:0]) indicates the current owner of the semaphore and a write to these with the same KEY (HWSEM\_SEMx[15:8]) unlock the semaphore.

## 4. Debugging RTP M4 with Nu-Link2-Pro

In addition to loading RTP M4 firmware using the method described in section <u>2.1.1</u>, the MA35D1 can also use Nu-Link2-Pro to program and debug M4 firmware.

Nu-Link2-Pro supports using Keil uVision, IAR Embedded Workbench and NuEclipse as firmware debugging environment.

### **4.1 Preliminary Preparation**

Before debugging, use the Nu-Link2-Pro and enable the CMSIS-DAP feature by the following steps:

- 1. Upgrade the Nu-Link2-Pro firmware with version later than v7174.
- 2. Open NU\_CFG.txt file located in the NuMicro MCU disk folder.
- 3. Set CMSIS-DAP=1 and re-plug the Nu-Link2-Pro.

NU_CFG.TXT - Notepad
File Edit Format View Help
[Build] Version=7174r
[Interface configuration] CMSIS-DAP=1
; 0 = disable ; 1 = enable

Figure 4-1 Enable CMSIS-DAP Feature

## 4.2 Keil uVision

To open the Keil project, double-click the uvproj file under the Keil/ directory, or open the uvproj file from the "Project" pull-down menu after launching the Keil uVision as shown in Figure 4-2.

New ?Vision Project New Multi-Project Works Open Project Close Project	pace	
Export Manage		+ +
Select Device for Target Remove Item		Alt+F7
Clean Targets Build Target Rebuild all target files		F7
Batch Build Translate Stop build		Ctrl+F7

Figure 4-2 Open Keil Project

In "**Options for Target – Linker**" tab, modify "**R/O Base**" and "**R/W Base**" value as shown in Figure 4-3.

Device       Target       Output       Listing       User       C/C++       Asm       Linker       Debug       Utilities         Use       Memory Layout from Target Dialog       X/O Base:	🔣 Options for Target 'Template'	×
Use Memory Layout from Target Dialog       X/O Base:         Make RW Sections Position Independent       R/O Base:         Make RO Sections Position Independent       R/W Base         Don't Search Standard Libraries       diable Warriege	Device   Target   Output   Listing   User   C/C++   Asm	Linker Debug Utilities
Make RW Sections Position Independent     R/O Base:     Make RO Sections Position Independent     Don't Search Standard Libraries	Use Memory Layout from Target Dialog	X/O Base:
Make RO Sections Position Independent     R/W Base     Don't Search Standard Libraries     datable Wassinger	Make RW Sections Position Independent	R/O Base: 0x0000000
	Don't Search Standard Libraries	R/W Base

Figure 4-3 Linker Configuration

To build the project click the "Build" icon shown in Figure 4-4.

|--|--|

Figure 4-4 Build Keil Project

In "Options for Target – Debug" tab, select CMSIS-DAP Debugger Driver as shown in Figure 4-5 and click settings.

🖁 Options for Target 'Template'		×
Device Target Output Listing User	C/C++ Asm Linker Debug Utilities	
<ul> <li>Use Simulator with restrictions</li> <li>Limit Speed to Real-Time</li> </ul>	Settings © Use: CMSIS-DAP Debugger •	Settings
✓ Load Application at Startup ✓ Rur Initialization File:	un to main() I Load Application at Startup I Run to Initialization File:	to main()
	Edit	. Edit

Figure 4-5 Select Debugger Driver

Select SW adapter "Nu-Link 2 CMSIS-DAP" and check IDCODE for device connection and set AP to 0x02 as shown in Figure 4-6.

Debug Trace Rash Download		1
CMSIS-DAP - JTAG/SW Adapter	SW Device           IDCODE         Device Name         Move           SWDIO	
SWJ Port: SW  Max Clock: 1MHz	Add Delete Update	
Debug Connect & Reset Options Connect: Normal	Autodetect <ul> <li>Cache Options</li> <li>Cache Code</li> <li>Verify Code Download</li> <li>Download to Flash</li> <li>Download to Flash</li></ul>	

### Figure 4-6 CMSIS-DAP Debug Settings

In "Options for Target – Utilities" tab, uncheck "Update Target before Debugging" option as shown in Figure 4-7.

Device Target Output Listing User C/C++ Asm Linker Debug Utilities Configure Flash Menu Command © Use Target Driver for Flash Programming CMSIS-DAP Debugger Settings Update Target before Debugging Init File: Edit	🔣 Options for Target 'Template'	×
Configure Flash Menu Command  Use Target Driver for Flash Programming  CMSIS-DAP Debugger  Settings Update Target before Debugging  Init File:  Edit	Device   Target   Output   Listing   User   C/C++   Asm	Linker Debug Utilities
Use Target Driver for Flash Programming     Use Debug Driver     CMSIS-DAP Debugger     Settings     Use Debug Driver     Use Debug Driver     Use Debug Driver     Driver     CMSIS-DAP Debugger     Settings     Use Debug Driver     Lings     Settings     Settings     Settings     Settings     Settings	Configure Flash Menu Command	
CMSIS-DAP Debugger     Settings     Update Target before Debugging       Init File:      Edit	Use Target Driver for Flash Programming	Use Debug Driver
Init File:	CMSIS-DAP Debugger	Settings Update Target before Debugging
	Init File:	Edit

Figure 4-7 CMSIS-DAP Utilities Settings

uVision will load the built image and enter debug mode after click the "**Start/Stop Debug Session**" icon as shown in Figure 4-8.

Figure 4-8 Debug Keil Project

## 4.3 IAR Embedded Workbench

To open the IAR workspace, double-click the eww file under IAR/ directory or open the eww file from the "File" pull-down menu after launching the IAR Embedded Workbench as shown in Figure 4-9.

New Open Close	
Save Workspace Close Workspace	e ce
Save Save As Save All	Ctrl+S
Page Setup Print	Ctrl+P
Recent Files Recent Workspaces	aces >
Exit	

### Figure 4-9 Open IAR Workspace

Open Options to modify setting as shown in Figure 4-10.

Workspace
Release
Files
E Template
-⊡ ■ Library -⊡ ■ User -⊡ ■ Output

Figure 4-10 Workspace Options

Select Cortex-M4F or Cortex-M4 with floating point option as shown in Figure 4-11.

Options for node "Template"	×
Options for node "Template" Category: General Options Static Analysis Runtime Checking C/C++ Compiler Assembler Output Converter Custom Build Build Actions Linker	Library Options 2 MISRA-C:2004 MISRA-C:1998 Target Output Library Configuration Library Options 1 Processor variant © Core Cortex-M4
Linker Debugger Simulator CADI CMSIS DAP GDB Server I-jet J-Link/J-Trace TL Stellaris	O Device     Nuvoton M451AE series (M451AE.)       O CMSIS-Pack     None       Endian mode     Floating point settings       Image: Display the series of the

Figure 4-11 General Options

Click "Override default" option to edit linker configuration for debugging on SRAM address as shown in Figure 4-12.

Category:	Factory Settings Linker configuration file editor	Linker configuration file editor
General Options Static Analysis Runtime Checking	Vector Table Memory Regions Stack/Heap Sizes	Vector Table Memory Regions Stack/Heap Sizes
Assembler	Config Library Input Optimizations Advanced Output List	IROM1 0x0000000 0x0000FFFF
Output Converter Custom Build	Linker configuration file	IROM2 0x0 0x0
Linker	\$PROJ_DIR\$\Template.icf	EROM1 0x0 0x0
Debugger Simulator	Edt	EROM2 0x0 0x0
CADI	· · · · · · · · ·	EROM3 0x0 0x0
		IRAM1 0x00010000 0x0001FFFF

### Figure 4-12 Linker Options

### Select CMSIS-DAP driver and uncheck "Use flash loader" option as shown in Figure 4-13.

Figure 4-13 Debugger Options

### Select SWD interface for CMSIS-DAP setting as shown in Figure 4-14.

Calcyuly.		Factory Settings
General Options Static Analysis Runtime Checking		
C/C++ Compiler	Setup Interface Breakpoints	
Assembler	Probe config Probe configuration	n file
Output Converter	Auto     Override defau	lt
Custom Build Build Actions	O From file	
Linker		Coloct
Debugger		Select
Simulator	Interface Explicit probe conf	iguration
CADI	O JTAG Multi-target det	bug system
CMSIS DAP CDB Server	SWD Target number	(TAP or Multidrop ID): 0
I-iet	Target with	multiple CPUs
J-Link/J-Trace	CPU.num	ber on target: 0
TI Stellaris	Interface speed	
Nu-Link		
PE micro	Add deleter -	
Third-Party Driver		

Figure 4-14 CMSIS-DAP Interface Setting

To build the workspace click the "Make" icon as shown in Figure 4-15.

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Figure 4-15 Build IAR Workspace

Modify "CMSIS-DAP Memory Configuration" based on SRAM address range as shown in Figure 4-16.

	00		while Dehermony Control	4								
orkspace			sable Debugger Cache	It is important for	C-SPY that the target m	emory is described fu	illy and accurately. Your pro	ject settings normally	specify this, as fol	lows.		OK
elease			sable interrupts when stepping									Course
iles			ave larget Running	Fasteriore								Lance
Template - Re	lea	E	M Trace Settings	Selected devi	e description file in Proi	ect Options:						
- CMSIS		E	M Trace Save									
-H Library -H Library	- 1	E	M Trace									
- 🗉 🖬 Output	1	F	nction Trace	It specifies the I	ollowing default memory	ranges:						
	_	V	ctor Catch	Zone	Nane		Start End	i Ty	pe	Size	Extra	
		Ti	neline									
	_	F	nction Profiler	5								
		S	ssion Overview									
		В	eakpoint Usage									
			PUB SEC Reset_Handle LDR ; UI	EA ICI r 10 Used ranges —								
			LDR	This is the men	iory configuration that w	ill be used. You can r	modify this as needed.					
			LDR STR LDR	This is the men Zone	ory configuration that w Start	ill be used. You can r End	nodify this as needed. Cache Type	Size	Extra	Connent		New
			LDR STR LDR STR LDR STR	This is the men Zone <u>Hemory</u> Hemory	ory configuration that w Start 0x24000000 0xE0000000	Il be used. You can r End 0x2403FFFF 0xFFFFFFFF	modify this as needed. Cache Type RAM Uncached/SFR	Size 256 kbytes 512 Mbytes	Extra	Connent Private p	peripheral	Edit

Figure 4-16 CMSIS-DAP Memory Configuration

IAR will load the built image and enter debug mode after click the "Download and Debug" icon as shown in Figure 4-17.

🗋 📽 🖬 🕼 🎒 🐇 🖻 🛍 🗠 어	~ ~ * *	: 🔁 🗟 🍽 🏟 🖗 🆓 🏠	🔤 😲 🕅 🕭 🕭

Figure 4-17 Debug IAR Project

## 4.4 NuEclipse

To use open the NuEclipse project, first launch the NuEclipse tool, select "**Import...**" from the File menu as shown in Figure 4-18.



	New	Alt+Shift+N >
	Open File	
	Close	Ctrl+W
	Close All	Ctrl+Shift+W
	Save	Ctrl+S
	Save As	
G	Save All	Ctrl+Shift+S
	Revert	
	Move	
	Rename	F2
8	Refresh	F5
	Convert Line Delimiters To	>
۵	Print	Ctrl+P
	Switch Workspace	>
	Restart	
2	Import	
2	Export	
	Properties	Alt+Enter
	1 gcc_arm.ld [Template/CMSI	IS/CMSIS/GCC]
	2 startup_nua3500_m4.S [Tem	nplate//GCC]
	3 main.c [Template/User]	
	4 mbedtls_config.h [LwIP_MQ	[TT/User/]
	Exit	
	2 startup_nua3000_m4.5 [lem 3 main.c [Template/User] 4 mbedtls_config.h [LwIP_MQ Exit	iplate//GCC] 2TT/User/]

### Figure 4-18 NuEclipse Import Project

Next, select import existing project to workspace and click "**Next** >" button as shown in Figure 4-19.

➡ Import
Select Create new projects from an archive file or directory.
Select an import source:
Archive File Existing Projects into Workspace File System Preferences C/C++ So Git So Install So Oomph Se Remote Systems Se RPM Se Run/Debug Tasks Tasks Team Tracing V
Court Nette Court

Figure 4-19 NuEclipse Import Existing Project

The last step is to select the project file, and then click "Finish" button.

🖨 Import				
Import Projects Select a directory to sear	h for existing Eclipse projects.			
Select root directory:     Select archive file:	C:\M4_RTP\SampleCode\Template\GC	x ~	Browse	
Projects:	RTP\SampleCode\Template\GCC)		Select All Deselect All Refresh	
Options     Search for nested pro     Copy projects into w     Close newly imported     Hide projects that alr	jects orkspace d projects upon completion eady exist in the workspace	>		
Working sets	ing sets	~	New Select	
?	< Back Next > Fin	iish	Cancel	

Figure 4-20 NuEclipse Select Project

To build NuEclipse project, click the Build icon as shown in Figure 4-21 or use the Ctrl + B hotkey.

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Figure 4-21 Build NuEclipse Project

Click "Debug Configurations" as shown in Figure 4-22.

🕹   🖦	🏘 🕇 🔘 🖛 💁 🖉 🖌 🍠
tartup_nua3	(no launch history)
t to crea	Debug As >
ject sett	Debug Configurations
ce and co on based o	Organize Favorites

Figure 4-22 Debug Configuration

Double-click on the "**GDB Nuvoton Nu-Link Debugging**" group. The Nuvoton Nu-Link debug configuration appears on the right-hand side.

Debug Configurations Create, manage, and run configuration	ions				-	- □ > ***
Image: Second Secon	Name: Template Release Main Debugger Project: Template C/C++ Application: Release\Template.elf Build (if required) before lau <u>Build Configuration</u> : Select O Enable auto build O Use workspace settings	Startup 🦻 Source 🔲 Commor	) O Disable a Configure )	Variables auto build Workspace Settin	Search Project	Browse
Filter matched 11 of 11 items					Revert	Apply
	]				Debug	Close

Figure 4-23 GDB Nuvoton Nu-Link Debugging

The value of GDB client port is set to 3334.

) B 🕫 🗈 🗙 🖻 🏹 🔹	Name: Template R	elease			
type filter text	Main 🕸 Deb	ugger	Startup) 😜 Source) 🔲 Common)		
<ul> <li>C/C++ Application</li> <li>C/C++ Attach to Application</li> <li>C/C++ Container Launcher</li> <li>C/C++ Pestmortem Debugger</li> <li>C/C++ Remote Application</li> <li>C/C++ Unit</li> <li>GDB Hardware Debugging</li> <li>C GDB Hardware Debugging</li> <li>C GDB Nuvoton Nu-Link Debuggin</li> <li>C Template Release</li> <li>C Launch Group</li> </ul>	OpenOCD Setup	CD locally S(opend	d_nulink_path}/openocd_cmsis-dap.exe	Browse	Variables
	GDB port: Telnet port: Config options:	3333 4444	tr/interface/cmsis-dap.cfn.cf./scrints/tarnet/numicroMA35D1.cfn		
	Allocate con	sole for 0	enOCD Allocate console for the teln	et connection	Ŷ
	GDB Client Setup	,			
	Executable:	\${cross_p	efix}gdb\${cross_suffix}	Browse	Variables
	Client port:	3334			
	Other options:				
	Commands:	set mem	naccessible-by-default off		< >
	Remote Target Host name or IP Port number:	address:	localhost 3333		
	Force thread lis	t update	suspend		Restore defau
۲ ک				Revert	Apply

Figure 4-24 GDB Client Port

\_

Check the startup debug setting shown in Figure 4-25, and then click "**Debug**" button. NuEclipse will load the built image and enter debug mode.

📑 🖻 💫 🗎 🗙 📄 🍸 🗸	Name: Template Release
type filter text	📄 Main 🕸 Debugger 🕟 Startup 🔖 Source 🔲 Common
C/C++ Application	Initialization Commands
C/C++ Attach to Application	☑ Initial Reset Type: init
C/C++ Container Launcher	^
C/C++ Remote Application	
Cti C/C++ Unit	v
GDB Hardware Debugging	Enable ARM semihosting
C Template Release	Erase chip
🚭 Launch Group	Chip Series: NuMicro A35 🗸
	Write Config0: 0x FFFFFFF Config1: 0x FFFFFFFF Config2: 0x FFFFFFFF Config3: 0x FFFFFFFF
	Load Symbols and Executable
	✓ Load symbols
	Use project binary: Template.elf
	O Use file: Workspace File System
	Symbols offset (hex):
	Load executable to flash
	Use project binary: Template.bin
	O Use file: Workspace File System
	Executable offset (hex):
	☑ Load executable to SRAM
	Use project binary: Template.bin
	O Use file: Workspace File System
	Executable offset (hex):
	Run/Restart Commands
	Pre-run/Restart reset Type: init (always executed at Restart)
	A
	· · · · · · · · · · · · · · · · · · ·
	Set program counter at (hex):
	Set breakpoint at: main
	Continue

Figure 4-25 Startup Debug Setting

## **Revision History**

Date	Revision	Description
2022.09.19	1.00	Initial version.

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