NAU88L20

Ultra-Low Power Audio CODEC Stereo Differential Lineout Driver

GENERAL DESCRIPTION

The NAU88L20 is an ultra-low power high performance audio codec that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital mixer, two high quality DACs and ADCs, and stereo differential line outputs. The advanced on-chip signal processing engine includes dynamic range compressor (DRC), programmable biquad filter.

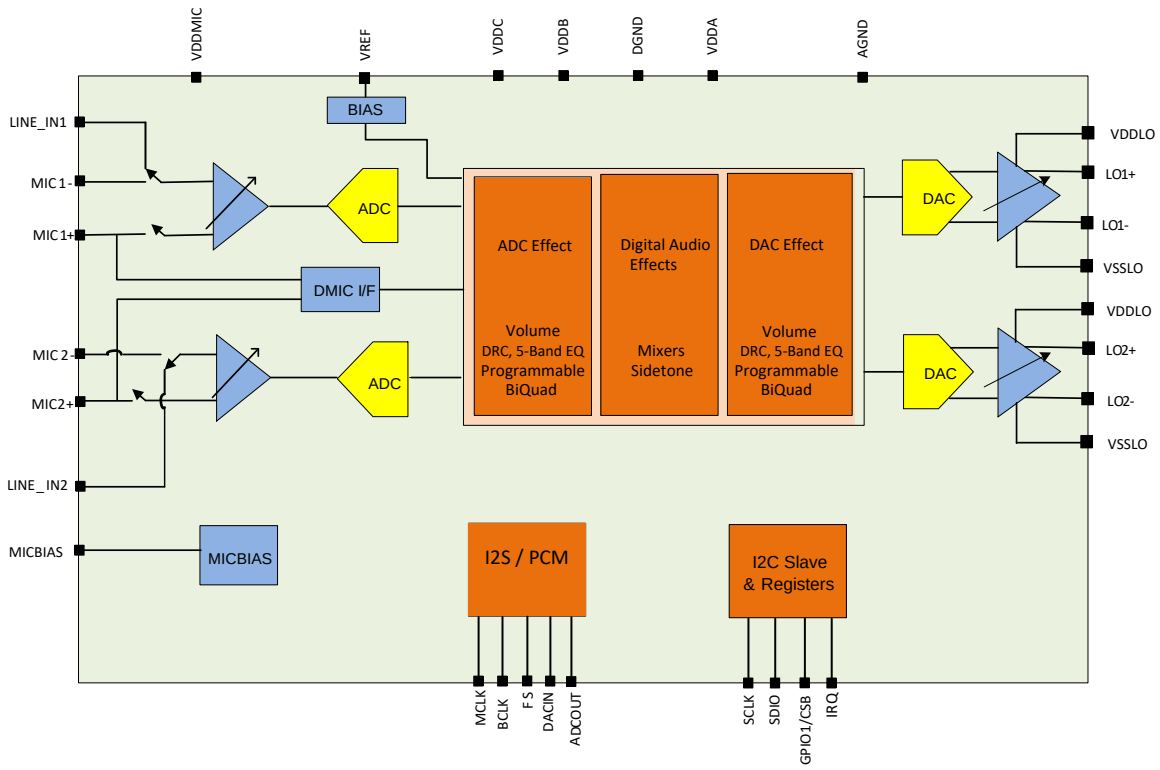
FEATURES

- DAC SNR: 101dB SNR, (A-weighted) @ 0dB gain, 1.8V and -84dB THD with 100mW into R_L= 16Ω, DAC playback to lineout output mode
- ADC: 103dB SNR (A-weighted) @ 0dB MIC gain, 1.8V, Fs = 48KHz and -89dB THD, 1.8V, MIC gain 0dB, OSR 128x
- 1 Digital I2S/PCM I/O port
- Two Line inputs
- Two mono differential or one stereo differential analog microphone inputs, two single-ended microphone inputs
- Class AB Lineout Driver
- Sampling rate from 8KHz to 96KHz
- Dynamic Range Compressor (DRC)
- Programmable Biquad filter
- Integrated DSP with specific functions:
  - Input automatic level control (ALC/AGC)/limiter
  - Output dynamic-range-compressor/limiter
  - 5-Band Equalizer
  - Notch filter and high pass filter
- Package:
  - 32 Pin QFN package
  - Package is Halogen-free, RoHS-compliant and TSCA-compliant

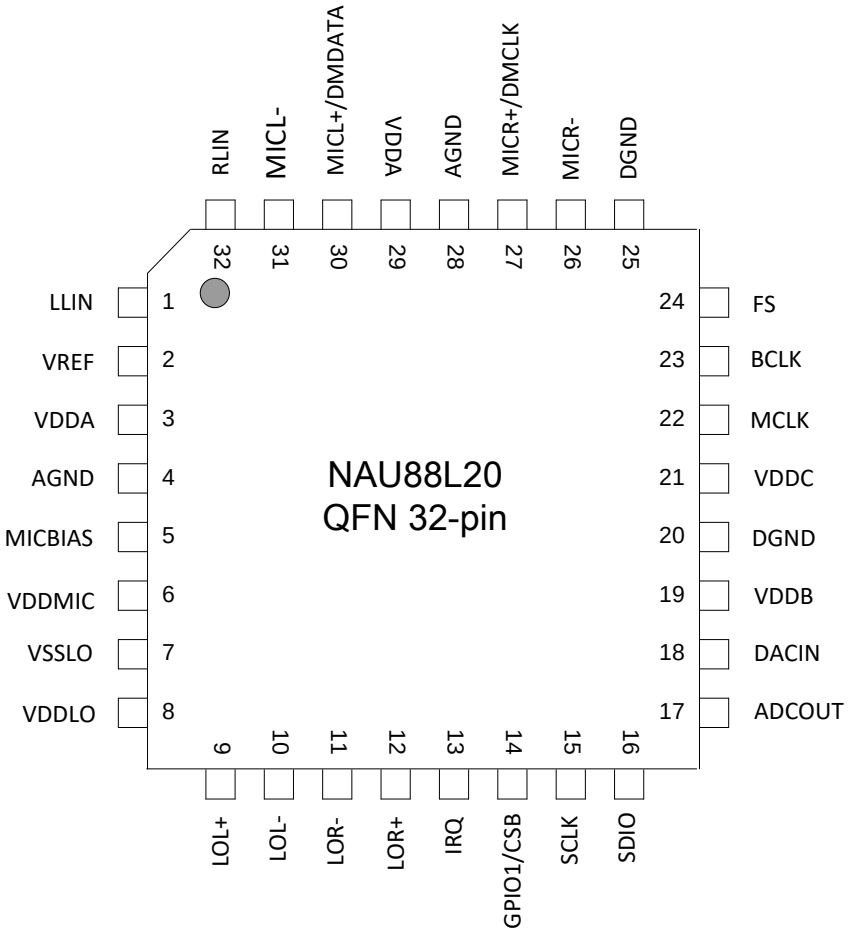
Applications

- Gaming controller
- Wireless Headset
- Smart Remote Controller

Block Diagram



Pin Diagram :


NAU88L20
QFN 32-pin
1 LLIN
2 VREF
3 VDDA
4 AGND
5 MICBIAS
6 VDDMIC
7 VSSLO
8 VDDLO
9 +LOL
10 -LOL
11 LOR-
12 LOR+
13 IRQ
14 GPIO1/CSB
15 SCLK
16 SDIO
17 ADCOUT
18 DACIN
19 VDDB
20 DGND
21 VDDC
22 MCLK
23 BCLK
24 FS
25 DGND
26 MICR-
27 MICR+/DMCLK
28 AGND
29 VDDA
30 MICL+/DMDATA
31 MICL-
32 RLIN

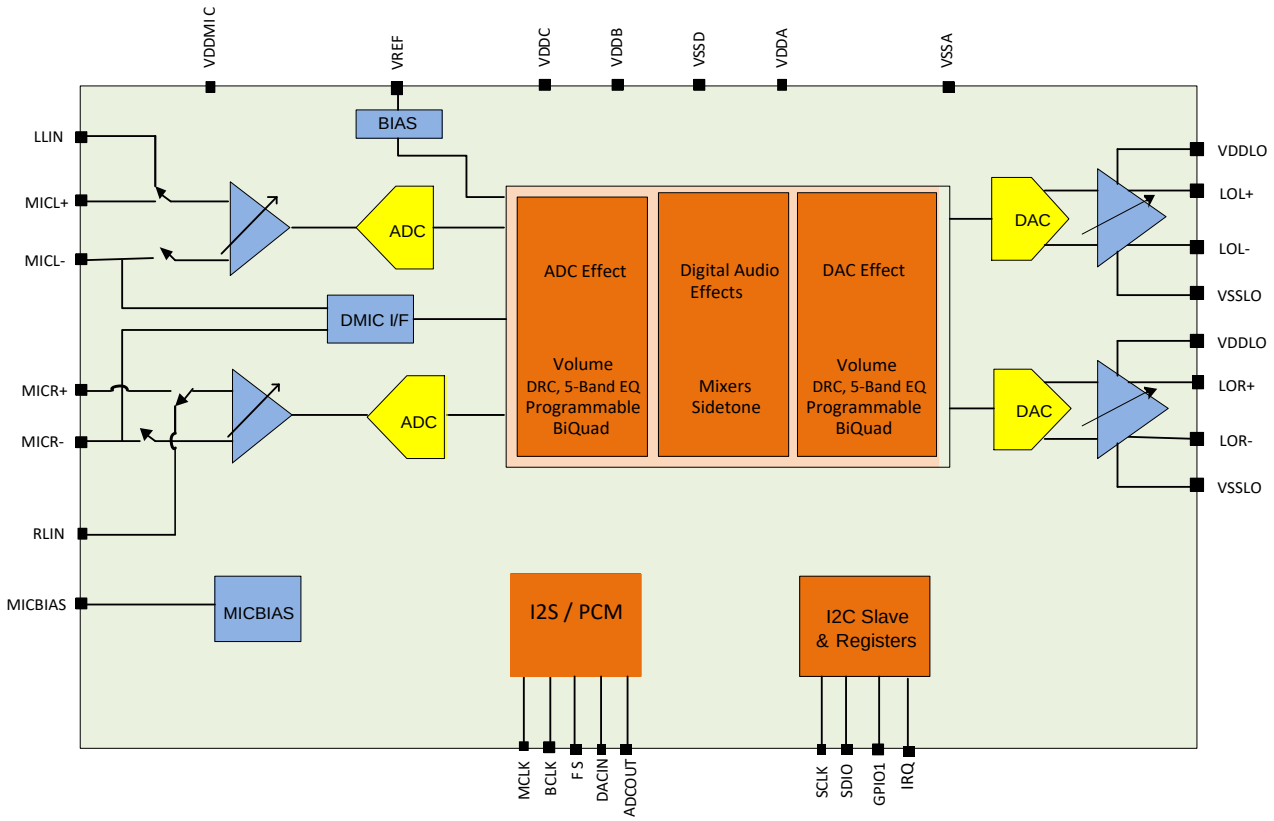
Pin Description

Pin #	Name	Type	Functionality
1	LLIN	Analog Input	Left Channel Analog Line Input
2	VREF	Analog I/O	Internal DAC & ADC voltage reference decoupling I/O
3	VDDA	Supply	Analog Power Supply
4	AGND	Ground	Analog Ground
5	MICBIAS	Microphone Bias Output	Microphone Reference
6	VDDMIC	Supply	MICBIAS Analog Supply
7	VSSLO	Ground	Lineout Ground
8	VDDLO	Supply	Lineout Power Supply
9	LOL+	Analog Output	Lineout1 Positive Output
10	LOL-	Analog Output	Lineout1 Negative Output
11	LOR-	Analog Output	Lineout2 Negative Output
12	LOR+	Analog Output	Lineout2 Positive Output
13	IRQ	Digital I/O	Interrupt Output
14	GPIO1/CSB	Digital I/O	General Purpose IO/CSB
15	SCLK	Digital Input	Serial Data Clock for I2C
16	SDIO	Digital I/O	Serial Data for I2C
17	ADCOUT	Digital Output	Serial Audio data Output for I2S or PCM data
18	DACIN	Digital Input	Serial Audio data input for I2S or PCM data
19	VDDB	Supply	Digital IO Power Supply
20	DGND	Ground	Digital GND
21	VDDC	Supply	Digital Core Power Supply
22	MCLK	Digital Input	CODEC Master clock input
23	BCLK	Digital I/O	Serial data bit clock input or output for I2S or PCM data
24	FS	Digital I/O	Frame Sync input or output for I2S or PCM data
25	DGND	Ground	Digital GND
26	MICR-	Analog Input	PGA MICR- Analog Input (Connect to Line-In ground through a capacitor when take right channel Line-In input)
27	MICR+/DMCLK	Analog Input/Digital Output	PGA MICR+ Analog Input / Digital Microphone CLK output
28	AGND	Ground	Analog Ground
29	VDDA	Supply	Analog Power Supply
30	MICL+/DMDATA	Analog Input/Digital Input	PGA MICL+ Analog Input / Digital Microphone DATA output
31	MICL-	Analog Input	PGA MICL- Analog Input (Connect to Line-In ground through a capacitor when take left channel Line-In input)
32	RLIN	Analog Input	Right Channel Analog Line Input

Notes:

1. Center pad underneath should be connected to AGND.

Functional Block Diagram



Electrical Characteristics

Conditions: VDDA = VDDC = VDDB = VDDMIC = VDDLO = 3.3V
f = 1kHz, MCLK=12.88MHz, unless otherwise specified. Limits apply for T_A = 25°C

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
I_{SB}	Standby Current	V_{DVDD} = 3.3V	7		µA
I_Q	Quiescent Current	f_S = 48kHz, DAC On, Linout Driver On, P_{OUT} = 0mW. R_L = 16Ω	20		mA
DAC/ Lineout Driver					
P_O	Output Power	Stereo, R_L = 16Ω, DAC Input, f=1kHz, 22kHz BW, THD+N = 1%, (QFN Package)	100		mW
FS_{out}	Full-scale output	P_{OUT} = 100mW, R_L = 16Ω	1.26		Vrms
THD+N	Total Harmonic Distortion + Noise	0dBFS input, VDDLO = 3.3V, R_L = 0	-80		dB
		-5dBFS input, VDDLO = 3.3V, R_L = 0	-84		dB
SNR	Signal to Noise Ratio	Sig-Ref= 1VRMS, DAC digital Input= -60dB, DAC_Gain = 0dB, Lineout Gain = 0dB, f=1kHz, A-Weighted)	101		dB
PSRR	Power Supply Rejection Ratio	f_{RIPPLE} = 217Hz, V_{RIPPLE} = 200mV_{P_P} Input Referred, Lineout gain = 0dB DAC Input, DAC_Gain = 0dB Ripple Applied to V_{DD}	90		dB
	Frequency Response	F = 20Hz ~ 20kHz	+0.1/-0.2		dB
X_{TALK}	Channel Crosstalk	Left Channel to Right Channel, 1dBFS, Gain = 0dB, f = 1kHz	110		dB
	Fs Accuracy (44.1 / 48 kHz)		+/- 0.02%		
	Pop Noise	Power-up supply, Vout =Vcm, Line_out C=2.2uF, R=10k	-69		dB
Line_In/Mic_in/ PGA/ ADC					
FS	Mic In FS differential Input signal level to PGA	V_{DD}= 1.8V, PGA-Gain = 0dB	1.16		V_{RMS}
	Line In FS single-ended input signal level to PGA	V_{DD}= 1.8V, PGA-Gain = 6dB	0.58		V_{RMS}
Rin	Mic-In minimum Input Impedance		18.7		kΩ
Rin	Line-In minimum Input Impedance		49.2		kΩ
fin	Frequency Response	f = 20Hz ~ 20kHz	+0.1/-0.2		dB
A_{pga}	Programmable Input Gain	MIC-in Gain range = -1dB to +36dB	-1.0 to 36		dB

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
		Line-in Gain range = -12dB to 25dB	-12.0 to 25		dB
P_{FE}	Power Consumption	No Signal, ADC on f_s = 44.1kHz	7.9		mW
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1kHz, fs = 48kHz, Mono Differential Input	-89		dB
		MIC Input, MIC_GAIN = 30dB, Volume = 0dB, Vin=32mVrms, f=1kHz, Digital Gain = 0dB, Mono Differential Input fs=16kHz	-81		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 48kHz, Mono Differential Input	103		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6 dB,fs = 48kHz, Mono Differential Input	101		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{PP} applied to V_{DD}A, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	90		dB
CMRR	Common Mode Rejection Ratio	Differential Input 100mVrms, PGA gain = 20dB, frequency sweep from 20Hz to 20KHz	81		dB
MICBIAS					
I_{OUT}	Output Current	Low Noise Mode		4	mA
		Low power Mode		1	mA
e_{os}	Output Noise	Low Noise Mode, f = 20Hz ~ 20kHz	4	10	uVrms

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	VDDB = 3.3V			0.37* VDDB	V
Input HIGH level	V_{IH}	VDDB = 3.3V		0.63* VDDB		V
Output HIGH level	V_{OH}	I_{Load}= 1mA	VDDB = 3.3V	0.95* VDDB		V
Output LOW level	V_{OL}	I_{Load}= 1mA	VDDB =3.3V		0.05* VDDB	V

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital I/O Supply Range	VDDB	2.7	3.3	3.6	V
Analog Supply Range	VDDA	2.7	3.3	3.6	V
Digital Supply Range	VDDC	2.7	3.3	3.6	V
Line-out Driver Supply Range	VDDLO	2.7	3.3	3.6	V
Microphone Bias Supply Voltage	VDDMIC	3.0	3.3	3.6	V
Temperature Range	T_A	-40		+85	°C

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital I/O Supply Range	-0.3	4.0	V
Speaker Driver Supply Range	-0.3	4.0	V
Microphone Bias Supply Voltage	-0.3	4.0	V
Voltage Input Digital Range	DGND - 0.3	VDDC + 0.3	V
Voltage Input Analog Range	AGND - 0.3	VDDC + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

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1. General Description

The NAU88L20 is an ultra-low power high performance audio codec that supports both analog and digital audio functions. It includes one I2S/PCM interface, one digital mixer, two high quality DACs and ADC's, and stereo differential line outputs. The advanced on-chip signal processing engine that includes dynamic range compressor (DRC), programmable biquad filter.

1.1 Inputs

The NAU88L20 provides analog inputs to acquire and process audio signals from two microphones and/or two Line-in inputs with high fidelity and flexibility. Microphones can be configured to capture signals from single-ended or differential sources.

A Digital Microphone interface is also supported. The channel can connect two digital microphones and has a fully differential programmable gain amplifier (PGA). The outputs of the PGA connects to the ADC block.

1.2 Outputs

NAU88L20 has one pair of Lineout amplifier/drivers fed by two DACs. These are very flexible outputs and can be used individually or as a stereo pair. These outputs are optimized for Lineout functions.

1.3 ADC, DAC and Digital Signal Processing

The NAU88L20 has independent high quality ADC and DACs for the two channels. These are high performance 24-bit sigma-delta converters, are suitable for a very wide range of applications.

The ADC and DACs have functions that individually support analog mixing and routing. The ADC and DACs blocks also support advanced digital signal processing subsystems that enable a very wide range of programmable signal conditioning and signal optimizing functions. All digital processing is done with 24-bit precision to minimize processing artifacts and maximize the audio dynamic range supported by the NAU88L20.

The ADC and DACs digital signal process can support two point dynamic range compressors (DRCs), programmable biquad filters configurable for low pass filters, high pass filters, Notch filter, Bell, low shelf, and high shelf-filters with various gain, Q, and frequency controls. Two points DRCs can be programmed to limit the maximum output level and/or boost a low output level. The biquad filters can configure high pass filters intending for DC-blocking or low frequency noise reduction, such as reducing unwanted ambient noise or "wind noise" on a microphone input. Notch filters can also be configured to greatly reduce a specific frequency band or frequency.

1.4 Digital Interfaces

Command and control of the device is accomplished by using a 2-wire I2C serial control interface. This simple, but highly flexible interface is compatible with most commonly used command and control serial data protocols and host drivers.

The digital audio I/O data streams transfer separately from command and control using either I2S or PCM audio data protocols. These simple but highly flexible interface protocols are compatible with most commonly used serial data protocols, host drivers, and industry standard I2S and PCM devices.

2. Power Supply

This NAU88L20 has been designed to operate reliably using separate 3.3V typical supplies for analog(VDDA), digital(VDDC), micbias(VDDMIC), IO buffers(VDDB) and Line-out amplifiers (VDDLO). Since all voltage supplies are the same value, there are no special requirements for the sequence or rate at which the various power supply pins change.

2.1 Power on and off Reset

The NAU88L20 includes a power on and off reset circuit on chip. The circuit resets the internal logic control on the digital VDDC supply power up and this reset function is automatically generated internally when power supply is too low for reliable operation. The reset threshold is approximately 1.0Vdc for VDDC and, it should be noted that this value is much lower than the required voltage for normal operation of the chip.

The reset is held on while the power level for VDDC is below the threshold. Once the power levels rise above the reset threshold, the reset is released and the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6μs.

For reliable operation, it is recommended to write SOFTWARE_RST, REG 0x5A upon power up. This will reset all registers to the known default state. Note that when VDDA is below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

2.2 Standby to Active Mode Powerup Sequence

When the chip is first powered up, it should be in operating in standby mode where all the analog blocks are turned-off. In the standby mode, the leakage current in drawn only from the DVDD=3.3V pin and is < 10uA. To go from standby mode to active mode, the bandgap and internal LDOs need to be turned-on. The sequence to bring up the BG and LDOs is as follows:

1) Power up Bandgap from off to normal mode
2) Power up the Digital LDO from standby to normal mode
3) Power up the Analog LDOs from off to normal mode
4) Power up the VMID and Bias circuits from off to normal mode

3. Input Path Detailed Descriptions

NAU88L20 is designed for low noise, high common mode rejection ratio analog microphone differential input. The microphone inputs MIC+ & MIC- are followed by a -1dB to 36dB PGA gain stage with a fixed 13kOhm input impedance.

Inputs are maintained at a DC bias of approximately ½ of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of external DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

3.1 Analog Microphone Inputs

The analog microphone input are followed by input stage before they are routed to a Front End Programmable Gain Amplifier(FEPGA). The input stage can be configured in different modes by using FEPGA_MODE in **REG 0x77**. The FEPGA gain can be varied from -1dB to 36dB in 1dB steps. The gain stage has a fixed 13kΩ input impedance and can be individually enabled or disabled using the powerup control signal, LPGA_EN, RPGA_EN, **REG 0x7F[15:14]**.

3.2 Digital Microphone Inputs

The MICL+/DMDATA and MICR+/DMCLK pins can be used for the digital microphone input. MICR+/DMCLK is the clock output pin for the digital microphone and the MICL+/DMDATA is the data in pin.

3.3 VREF

The NAU88L20 includes a mid-supply, reference circuit that produces voltage close to VDDA/2 that is decoupled to AGND through the VREF pin by means of an external bypass capacitor. Because VREF is used as a reference voltage for the majority of the NAU88L20, a large capacitance is required to achieve good power supply rejection at low frequency, typically 4.7µF is used.

VMIDSEL	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50kOhm	25kOhm
10	250kOhm	125kOhm
11	5kOhm	2.5kOhm

Table 1: VREF Impedance Selection

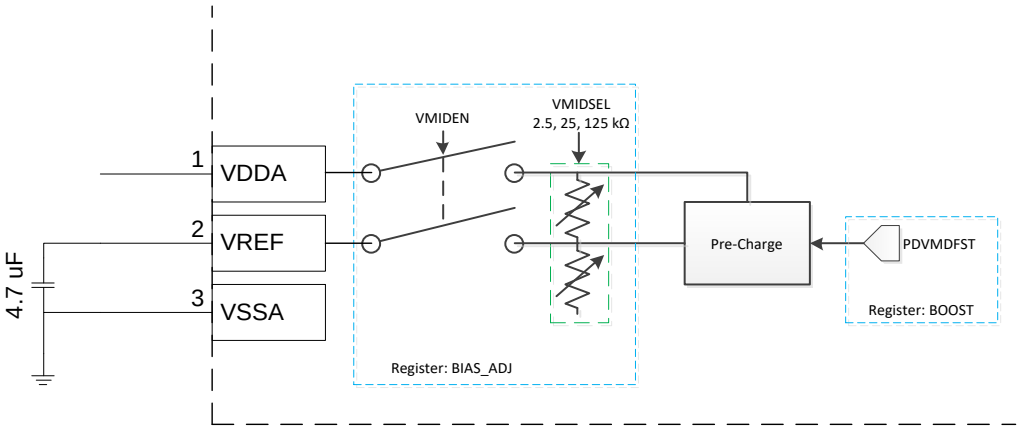


Figure 2: VREF Circuitry

3.4 MIC Bias

The NAU88L20 provides a MICBIAS pin to power the electret type microphones. The MICBIAS is the low impedance output of the MIC Bias LDO. An external 2kOhm resistor should be used if an analog microphone is to be biased by this pin. Micbias has two modes of operation, each selected by MICBIAS_LPMODE, **REG 0x74[4:3]** and the level can be set by using MICBIAS_LVL, **REG 0x74[2:0].** It can operate in a low noise mode or a low power mode. Low power mode is ideally suited for digital MIC applications. See electrical characteristics for expected operating values.

4. ADC Digital Block

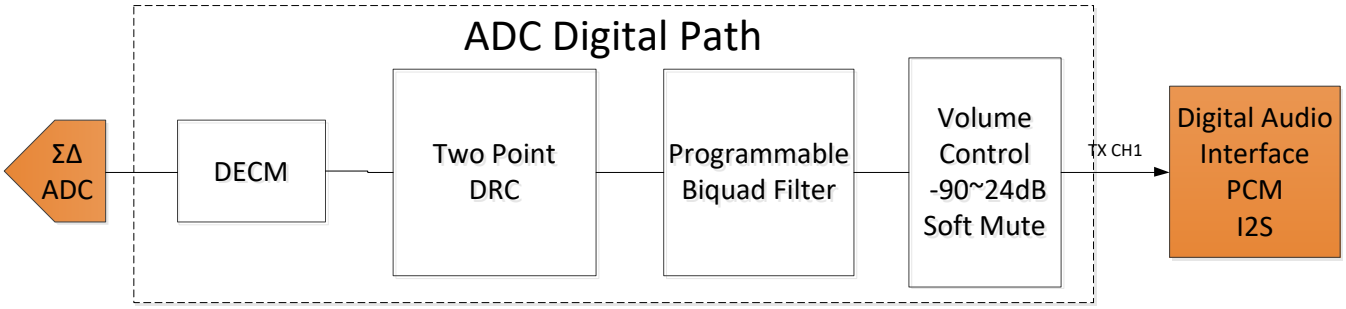


Figure 1 ADC Digital Path

The two ADC digital paths receive the output of the 24-bit Analog-to-Digital converter. The paths are capable of performing signal processing such that a high quality audio sample bit stream can then be passed to the audio path digital interface. The figure above shows the functional blocks associated with each ADC digital path.

Oversampling rate is used to improve noise and distortion performance; however this does not affect the final audio sample rate. The ADC_RATE, **REG 0x2B[1:0]** can be used to set the ADC OSR and SMPL_RATE, **REG 0x2B[7:5]** should be set to the value closest to the actual sample rate. The polarity of the ADC output signal can be controlled independently. This data management feature can help minimize subsequent audio processing that may be otherwise required, as the data is passed through stages in the system. The full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0VRMS.

4.1 ADC Dynamic Range Compressors (DRC)

Each ADC in the digital signal path supports a dynamic range compressor (DRC) for advanced signal processing. The DRC's can be programmed to limit the maximum output level and/or boost a low output level signals. The DRC's function consists of level estimation and static curve control.

4.1.1 ADC Level Estimation

The DRC uses Peak level estimation that depends on pre-set attack and decay times. The attack times are set by using register DRC_PK_COEF1_ADC. The decay time is set using register DRC_PK_COEF2_ADC.

BITS	DRC_PK_COEF1_ADC	DRC_PK_COEF2_ADC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

Table 2: ADC Level Estimation - Attack and Decay Time Register Settings

Please note that Ts is the sampling time given by 1/(Sampling Frequency)

4.1.2 Static Curve

The DRC static curve supports five programmable sections which can be enabled using register DRC_ENA_ADC. The figure below shows the five programmable sections.

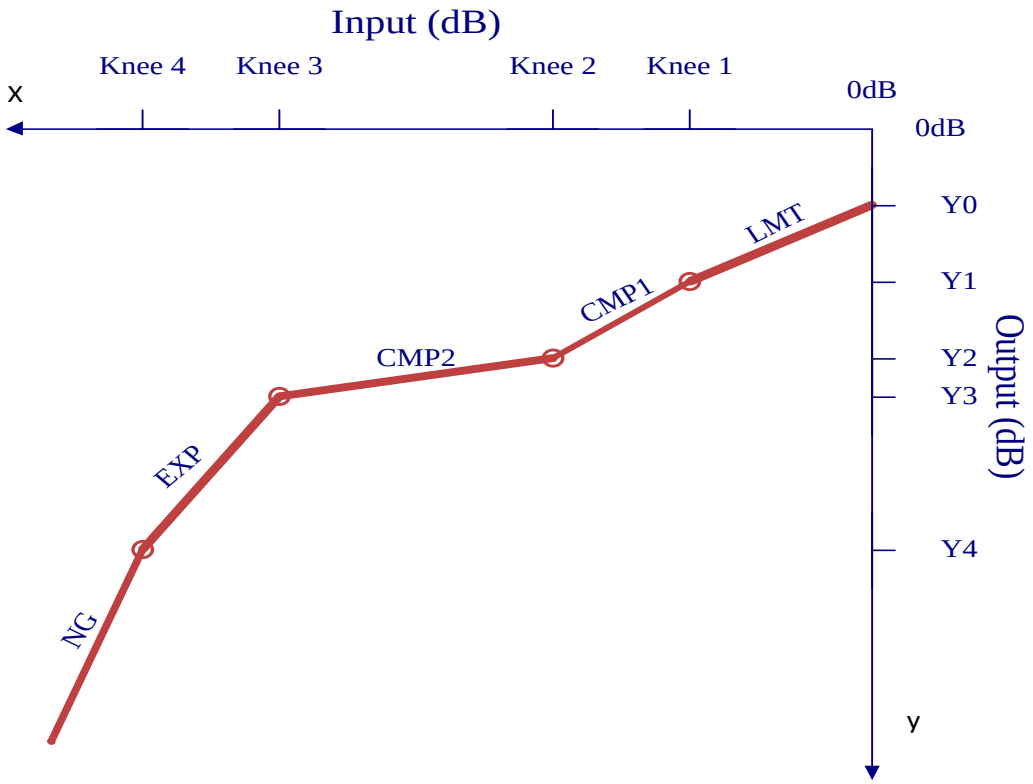


Figure 2 DRC Static Characteristic

Each section on the characteristic (labeled NG, EXP, CMP2, CMP1, and LMT) can be controlled by setting the slope and knee point values, in their respective registers. The table below provides the corresponding register locations.

Static Curve Section	Slope	Knee Point
LMT	**ADC_DRC_SLOPES.DRC_LMT_SLP_ADC**	
CMP1	**ADC_DRC_SLOPES.DRC_CMP1_SLP_ADC**	**ADC_DRC_KNEE_IP12.DRC_KNEE1_IP_ADC**
CMP2	**ADC_DRC_SLOPES.DRC_CMP2_SLP_ADC**	**ADC_DRC_KNEE_IP12.DRC_KNEE2_IP_ADC**
EXP	**ADC_DRC_SLOPES.DRC_EXP_SLP_ADC**	**ADC_DRC_KNEE_IP34.DRC_KNEE3_IP_ADC**
NG	**ADC_DRC_SLOPES.DRC_NG_SLP_ADC**	**ADC_DRC_KNEE_IP34.DRC_KNEE4_IP_ADC**

Table 3: ADC DRC Static Curve control registers

The output Y values can be determined based on the slopes and knee points selected. Y1 is always equal to Knee 1, as an initial and default condition.

Y1 = Knee 1
Y0 = Y1 - (Knee 1) * (LMT Slope)
Y2 = (Knee 2 - Knee 1) * (CMP1 Slope) + Y1
Y3 = (Knee 3 - Knee 2) * (CMP2 Slope) + Y2
Y4 = (Knee 4 - Knee 3) * (EXP Slope) + Y3

4.2 ADC Digital Volume Control

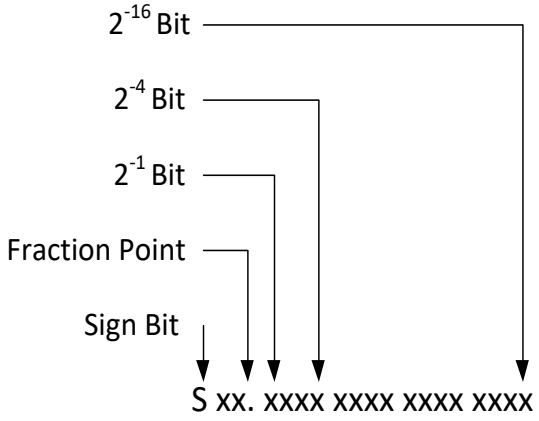
The digital volume control feature allows adjustment of the audio volume coming from ADC using a two-stage volume control. This allows the gain to be adjusted from -66dB to +24dB. Also included is a mute value that will reduce the output signal of the ADCs to zero. To adjust the channel volume controls, use DGAINL_ADC and/or DGAINR_ADC in **REG 0x35**.

4.3 ADC Programmable Biquad Filter

The NAU88L20 has 4 dedicated digital biquad filters. Two for the ADC path, and two for the DAC path. The biquad filter is a second-order recursive linear filter with two poles and two zeros. Its transfer function is the Z-domain consists of two quadratic functions:

$$H(z) = \frac{B_0 + B_1 Z^{-1} + B_2 Z^{-2}}{1 + A_1 Z^{-1} + A_2 Z^{-2}}$$

The coefficients A_1, A_2, B_0, B_1, B_2 are represented in the 3.16 format described below



Each Biquad Coefficient has 19 bits in total, as formatted below

- S is the sign bit (1 bit),
- xx are integers (2bits)
- 16 fractional bits (16 bits)

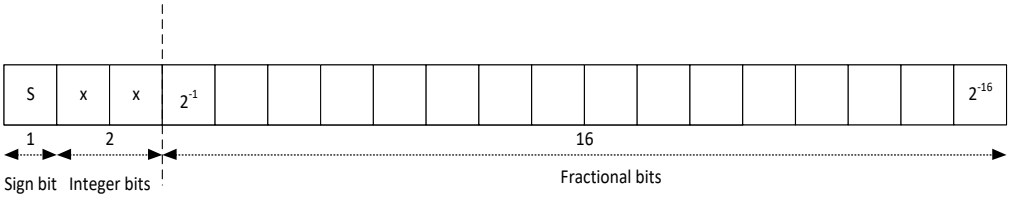


Figure 5: Number format description for biquad filters coefficients

Application Notes:

- Biquad filter coefficients for the ADC with 3.16 format for A1, A2, B0, B1, and B3 are located in below registers.
    - BIQ0_COF2.BIQ_A1_H and BIQ0_COF1.BIQ_A1_L
    - BIQ0_COF4.BIQ_A2_H and BIQ0_COF3.BIQ_A2_L
    - BIQ0_COF6.BIQ_B0_H and BIQ0_COF5.BIQ_B0_L
    - BIQ0_COF8.BIQ_B1_H and BIQ0_COF7.BIQ_B1_L
    - BIQ0_COF10.BIQ_B2_H and BIQ0_COF9.BIQ_B2_L

- To program the biquad filter in the ADC path, write BIQ0_COF1 to BIQ0_COF10 for coefficients.

- To turn on the biquad filter in the ADC path, write '1' to BIQ0_COF10.BIQ0_EN.

4.4 ADC Companding

Companding can be used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L20 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and µ-law. The A-law algorithm primarily used in European communication systems and the µ-law algorithm primarily used by North America, Japan, and Australia.

5. DAC Digital Block

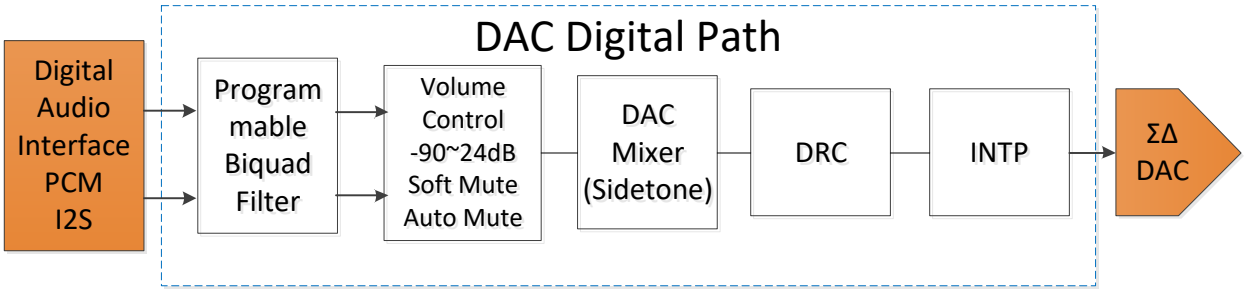


Figure 3 DAC Digital Path

The DAC digital block uses 24-bit signal processing to generate analog audio with a 16-bit digital sample stream input. This block consists of a sigma-delta modulator, digital decimator/filter, programmable biquad filter, and a DRC. The full-scale output level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0 VRMS. The oversampling feature of the DAC can be changed from 32x to 256x for improved audio performance at higher power consumption. The DAC output signal polarity can be changed using register setting. This can help minimize any audio processing that may be required as the data is passed from other stages of the system. The DAC channel is enabled by signal DIG_LDAC_EN and/or DIG_ RDAC_EN in REG 0x01.

5.1 DAC Dynamic Range Compressor (DRC)

The DAC DRC functions in the same way as the ADC DRC explained in Section 4.1. However, different control registers are used.

5.1.1 DAC Level estimation

To set the attack and decay times for the peak level estimation, use registers DRC_PK_COEF1_DAC and DRC_PK_COEF2_DAC respectively.

BITS	DRC_PK_COEF1_DAC	DRC_PK_COEF2_DAC
0000	Ts	63*Ts
0001	3*Ts	127*Ts
0010	7*Ts	255*Ts
0011	15*Ts	511*Ts
0100	31*Ts	1023*Ts
0101	63*Ts	2047*Ts
0110	127*Ts	4095*Ts
0111	255*Ts	8191*Ts

5.1.2 DAC static Curve

The DRC static curve supports five programmable sections enabled by using DRC_ENA_DAC. The table below shows the related control registers.

Static Curve Section	Slope	Knee Point
LMT	DAC_DRC_SLOPES.DRC_LMT_SLP_DAC	
CMP1	DAC_DRC_SLOPES.DRC_CMP1_SLP_DAC	DAC_DRC_KNEE_IP12.DRC_KNEE1_IP_DAC
CMP2	DAC_DRC_SLOPES.DRC_CMP2_SLP_DAC	DAC_DRC_KNEE_IP12.DRC_KNEE2_IP_DAC
EXP	DAC_DRC_SLOPES.DRC_EXP_SLP_DAC	DAC_DRC_KNEE_IP34.DRC_KNEE3_IP_DAC
NG	DAC_DRC_SLOPES.DRC_NG_SLP_DAC	DAC_DRC_KNEE_IP34.DRC_KNEE4_IP_DAC

5.2 DAC Digital Volume Control, Mute and Channel selection

The DAC's each have digital volume controls that allow the user to adjust the gains from -66dB to +24dB in 0.5dB steps, in DGAIN_DAC, **REG 0x34**. Also included are mute settings that will reduce each path gain to a minimum, control is through register DGAIN_DAC. When using fullscale input or DGAIN_DAC above 0dB, it is recommended for best performance to set the DAC control bit, CICCLP_OFF as 0, in **REG 0x2C** and set CIC_GAIN_ADJ for optimal output amplitude.

5.3 DAC Soft Mute

The soft mute function works for both the DAC's and the ADC's and gradually attenuates the volume of the signal to zero. The soft mute ramps the DAC's digital volume down to zero when enabled by register SMUTE_EN, **REG 0x31[9]**. When disabled, the volume increases to the specified volume level immediately. This soft mute feature provides for pop and click reduction in the DAC signal paths when the chip powers up.

5.4 DAC Auto Mute

The auto mute feature is only available for the DAC paths. In the "automatic" mode, the signal AMUTE_EN, **REG 0x31[11]** needs to be enabled. When 1024 consecutive zeros samples are detected, the ANALOG_MUTE register, **REG 0x59[10]** is flagged. As soon as the first non-zero sample is detected, ANALOG_MUTE is de-assert. If at any time there is a non-zero sample value, the DAC's will be un-muted, and the 1024 count will be reinitialized to zero.

5.5 DAC Path with Sidetone

For each channel left (0) and right (1), the Sidetone source can be selected from either ADC0 output or ADC1 output, then mixing with DAC0 data and DAC1 data with applied gain control. The mixed data becomes the final DAC output for that channel. The figure below shows a block diagram of how this works along with the related registers.

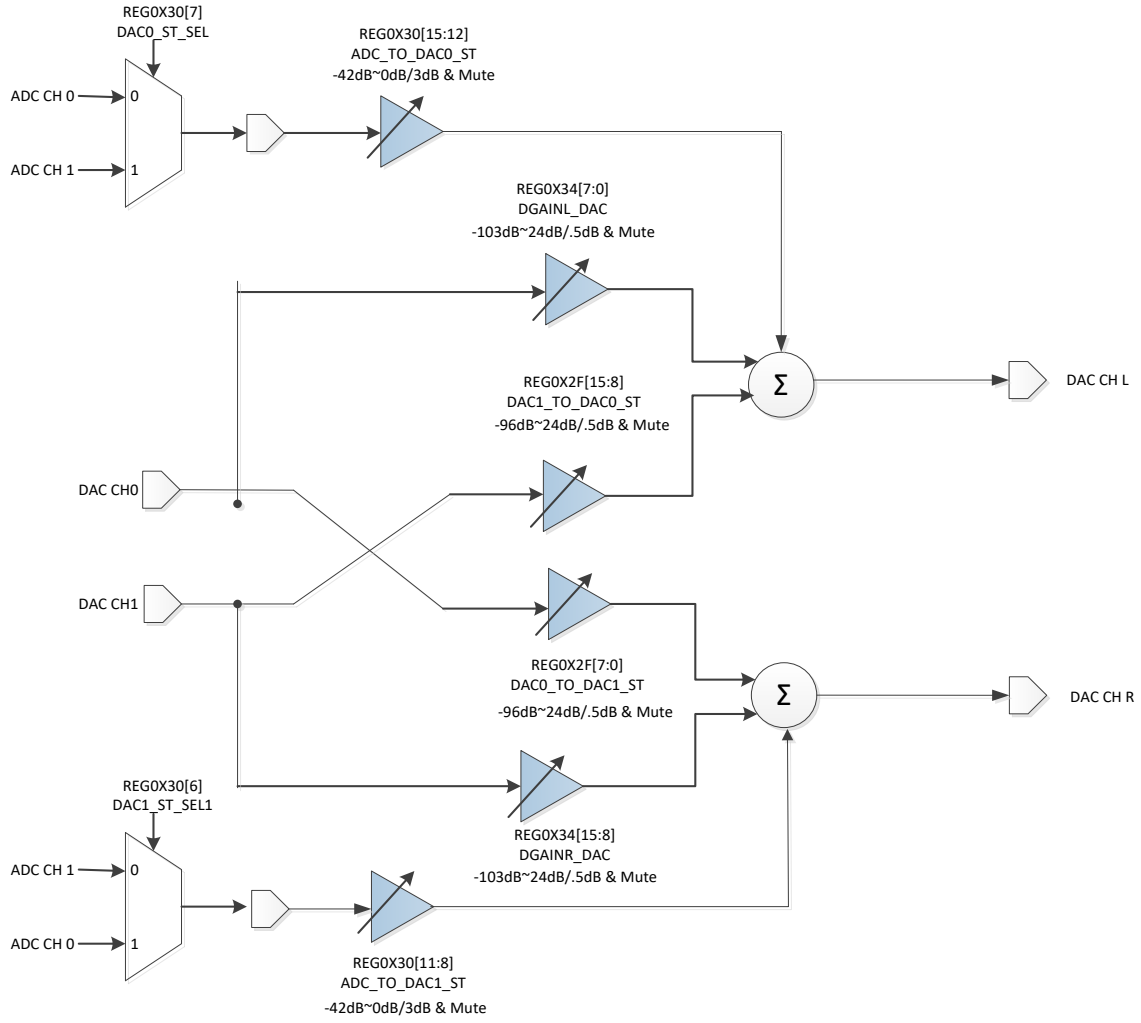


Figure 4 DAC Path Digital Mixer with Sidetone

Sidetone calculation formula is listed below:

DAC CH0 Mixer = DAC CH0 Data * DGAINL_DAC + DAC CH1 Data * DAC1_TO_DAC0_ST +
(ADC CH0 Data or ADC CH1 Data) * ADC_TO_DAC0_ST
DAC CH1 Mixer = DAC CH1 Data * DGAINR_DAC + DAC CH0 Data * DAC0_TO_DAC1_ST +
(ADC CH1 Data or ADC CH0 Data) * ADC_TO_DAC1_ST

5.6 DAC Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates using non-linear algorithms. The NAU88L20 supports the two main telecommunications companding standards on both transmit and receive sides: A-law and μ-law. The A-law algorithm is primarily used in European communication systems and the μ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 14 bits (μ-law) or 13 bits (A-law) to 8 bits using non-linear quantization resulting in 1 sign bit, 3 exponent bits and 4 mantissa bits. This option, enabled for the DAC's and ADC's by using DACCM0 register and ADCCM0 register respectively. When the companding mode is enabled, CMB8_0

bit **REG 0x1C[10]** must be enabled for 8 bit operation. This will disable the word length selection in WLEN0 bits **REG 0x1C[3:2]** for this port and allow the companding functions to use an 8 bit word length. The compression equations set by the ITU-T G.711 standard implemented in the NAU88L20.

5.6.1 DAC Companding

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

5.6.2 DAC Companding

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \qquad 0 < x < \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|)}{(1 + \ln(A))}, \qquad \frac{1}{A} \leq x \leq 1$$

$$A = 87.6$$

6. Clocking and Sample Rates

SR	MIPS	OSR	external clock
8000	256	128	2,048,000
8000	256	256	2,048,000
8000	400	100	19,200,000
8000	500	100	24,000,000
8000	500	100	4,000,000
16000	256	64	12,288,000
16000	256	128	12,288,000
16000	400	100	19,200,000
16000	500	100	24,000,000
16000	500	100	8,000,000
24000	256	64	12,288,000
24000	256	128	12,288,000
24000	400	100	19,200,000
24000	500	100	12,000,000
32000	256	64	24,576,000
32000	256	128	24,576,000
32000	400	100	38,400,000
32000	500	100	48,000,000
32000	500	100	16,000,000
48000	256	64	12,288,000
48000	256	128	12,288,000
48000	400	100	19,200,000
48000	500	100	24,000,000
96000	256	64	24,576,000

7. Control Interfaces

The NAU88L20 includes a serial control bus that provides access to all the device control registers, it may be configured as a 2-wire interface that conforms to industry standard implementations of the I2C serial bus protocol.

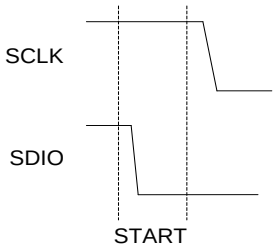
7.1 2-Wire-Serial Control Mode (I2C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and any device receiving data as the receiver (or slave). The NAU88L20 can function only as a slave when in the 2-wire interface configuration.

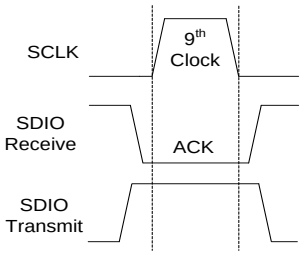
7.2 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

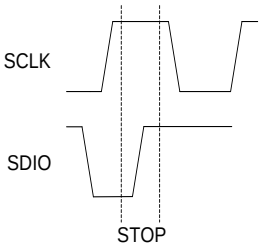
An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data. Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.



Valid START Condition



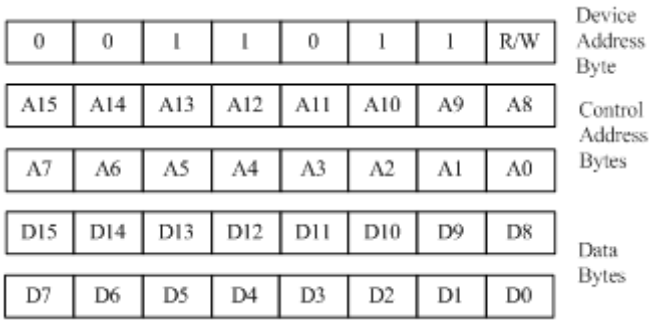
Valid Acknowledge



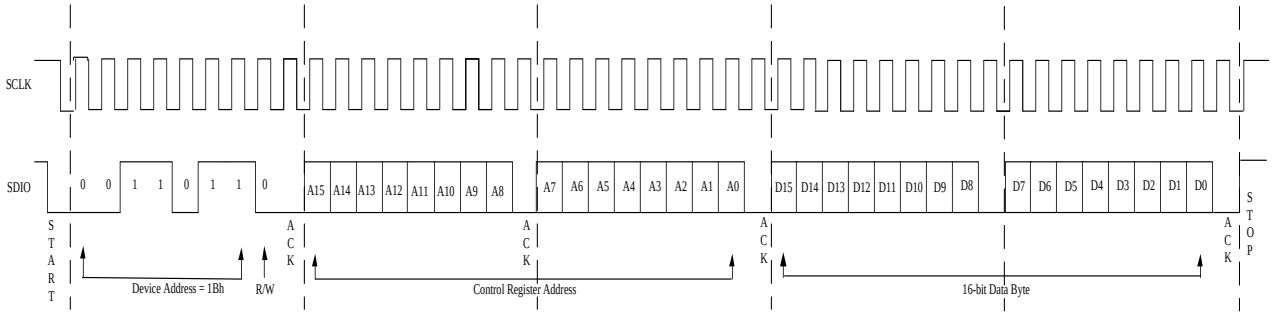
Valid STOP Condition

7.3 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition. The Device Address of the NAU88L20 is fixed to **0x1B**. If the Device Address matches this value, the NAU88L20 will respond with the expected ACK signaling as it accepts the data being transmitted to it.



NAU88L20 Slave Address Byte 0x1B, Control Address Byte, and Data Byte



2-Wire Write Sequence

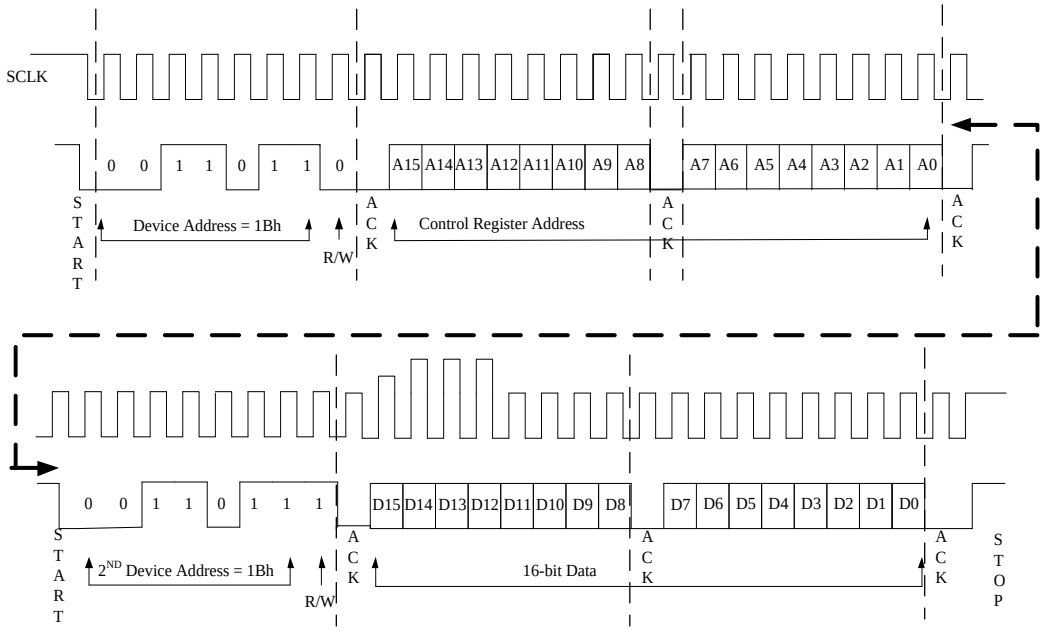
7.4 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers are to be accessed.

If the device address matches this value, the NAU88L20 will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted to it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

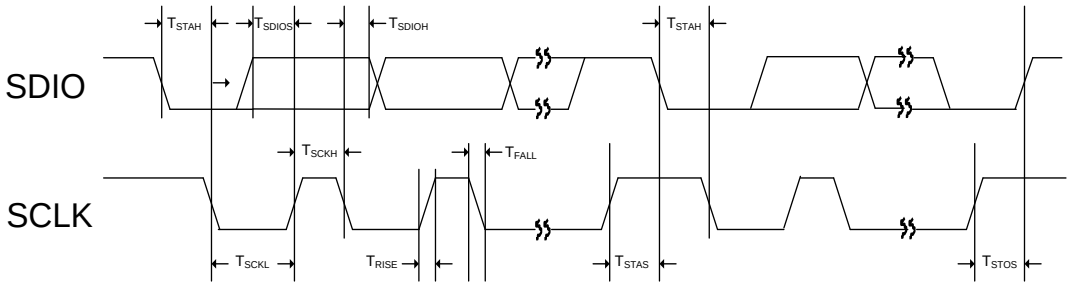
After again recognizing its device address, the NAU88L20 transmits an ACK, followed by a two-byte value containing the 16 bits of data from the selected control register inside the NAU88L20. During this phase, the master generates the ACK signaling with each byte transferred from the NAU88L20. If there is no STOP signal from the master, the NAU88L20 will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU88L20 reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.



I2C 2-Wire Read Sequence

7.5 Digital Serial Interface Timing



Two-wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

8. Software Reset

The NAU88L20 and all of its control registers can be reset to “default”, initial conditions by writing any value to **REG 0x00** using the two-wire interface mode.

9. Digital Audio Interfaces

The NAU88L20 can be configured as either the master or the slave, by setting MS0 bit **REG 0x1D[3]** to 1 for master mode and to 0 for slave mode. Slave mode is the default if this bit is not written. In master mode, NAU88L20 outputs both Frame Sync (FS) and the audio data bit clock (BCLK) and has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK; SDO clocks out ADC data, while SDI clocks in data for the DACs.
When not transmitting data, SDO pulls LOW in the default state. Depending on the application, the output can be configured to pull up or pull down. When the time slot function is enabled. There are additional output state modes including controlled tristate capability. NAU88L20 supports eight audio formats including left justified, I2S, PCMA, PCMB, and PCM Time Slot.

PCM Mode	I2S_PCM_CTRL1.AIFMT0	I2S_PCM_CTRL1.LRP0	I2S_PCM_CTRL2.PCM_TS_EN0
Left Justified	01	0	0
I2S	10	0	0
PCMA	11	0	0
PCMB	11	1	0
PCM Time Slot	11	Don’t care	1

9.1 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel_0 data is transmitted and when FS is LOW, channel_1 data is transmitted. This can be seen below in Figure 9.1.

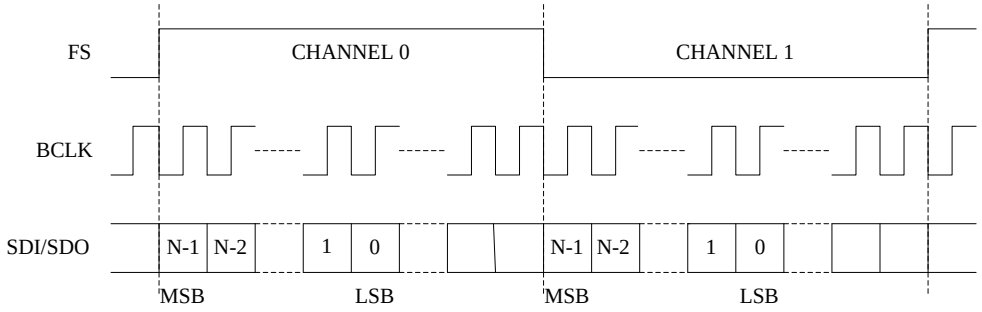


Figure 9.1 Left-Justified Audio Interface

9.2 I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This can be seen below in Figure 9.2.

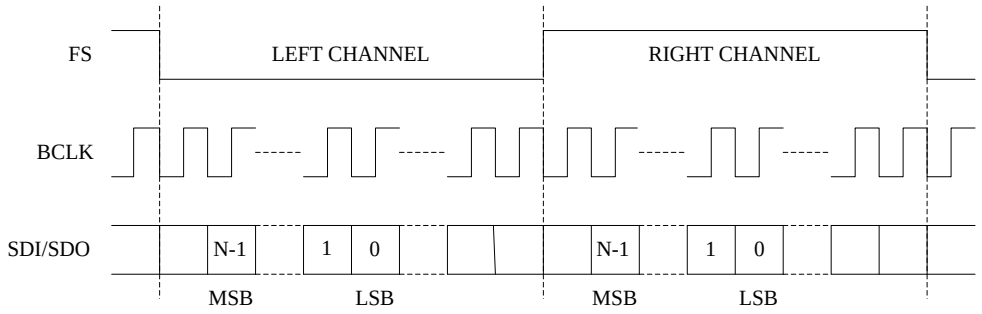


Figure 9.2 I2S Audio Interface

9.3 I2S Audio Data

In the PCM A mode, channel 0 data is transmitted first followed immediately by channel 1 data. The channel 0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and channel 1 MSB is clocked on the next BCLK after the left channel LSB. This can be seen below in Figure 9.3.

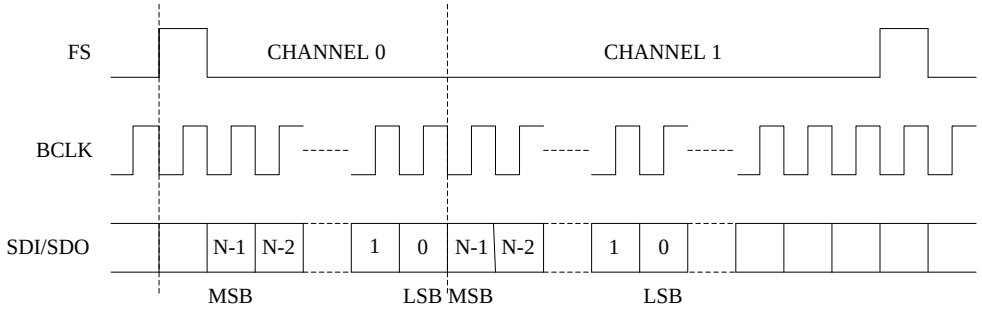


Figure 9.3 PCMA Audio Interface

9.4 PCM B Audio Data

In the PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. Channel 0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next BCLK after channel_0 LSB. This can be seen below in Figure 9.4.

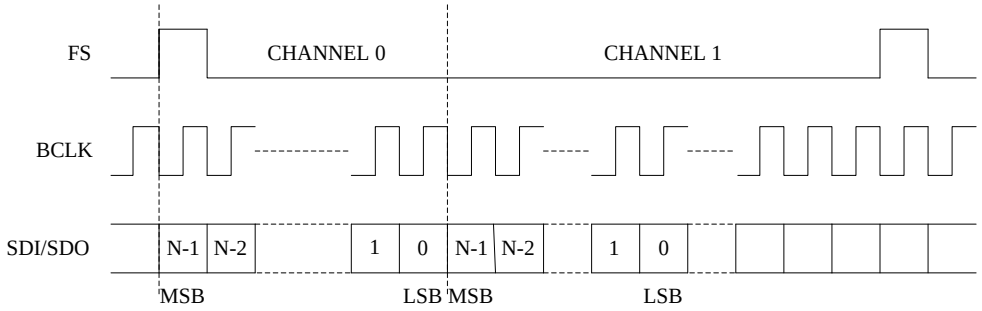


Figure 9.4 PCMB Audio Interface

9.5 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at which the DAC and/or ADC data are clocked. This can be useful when multiple NAU88L20 chip or other devices are sharing the same audio bus. This will allow each chip's audio to be delayed around each other without interference.

Normally, the DAC and ADC data are clocked immediately after the Frame Sync (FS), however, in the PCM time slot mode, the audio data can be delayed by for example for Left channel TSLOT_L0 bits **REG 0x1E[9:0]** and with
PCM_TS_EN0 bit **REG 0x1D[10]** set to 1. These delays can be seen leading the MSB in the illustration below.

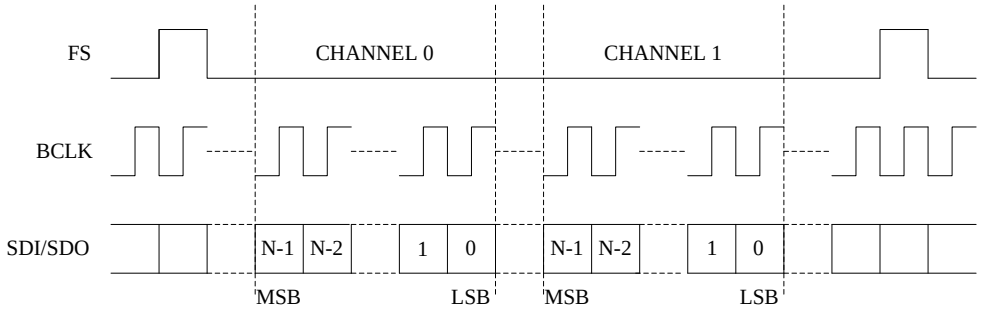


Figure 9.5 PCM Time Slot Audio Interface

Note this mode can be used to swap channel 0 and channel 1 audio or cause both channels to use the same data.

9.6 TDM PCMA Audio Data

In the PCMA mode, channel_0 data is transmitted first followed sequentially by channel_1, 2, and 3 immediately after. The channel_0 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the Figure 9.6 below.

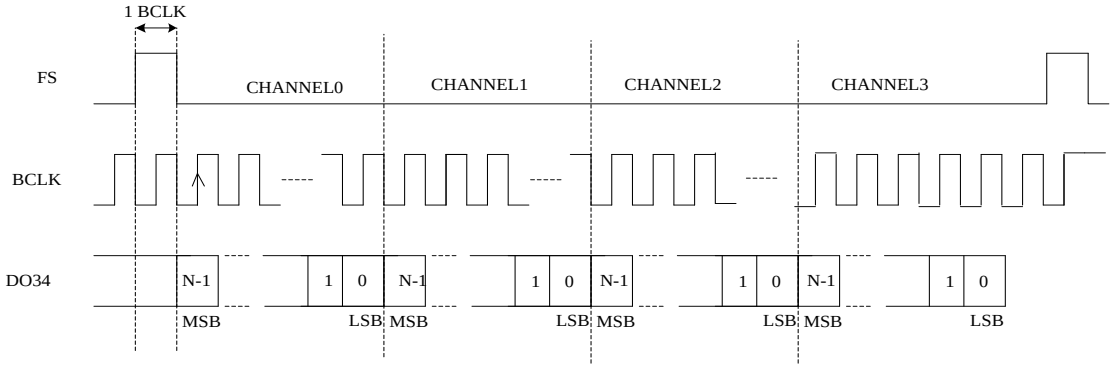


Figure 9.6: TDM PCMA Audio Format

9.7 TDM PCMB Audio Data

In TDM PCMB mode, channel_0 data is transmitted first followed immediately by channel_1 data. The channel_0 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and channel_1 MSB is clocked on the next SCLK after channel_0 LSB.

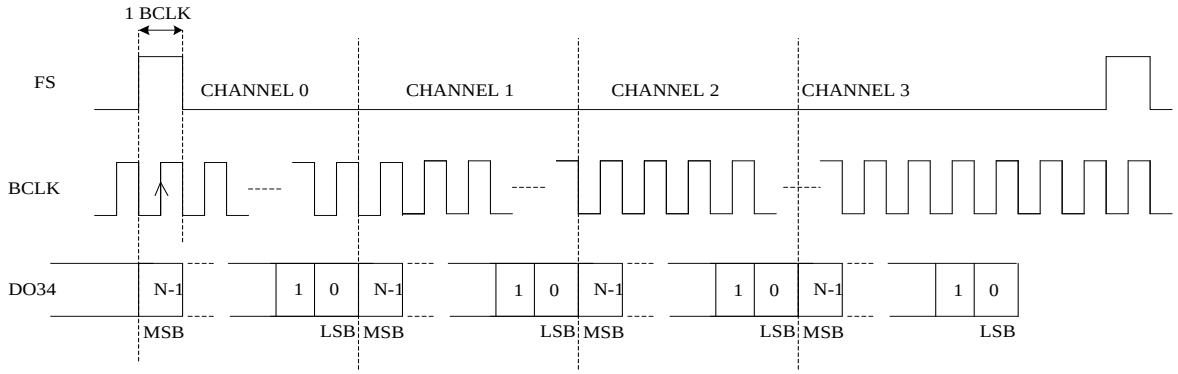


Figure 9.7: TDM PCMB Audio Format

9.8 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which DAC data is clocked. This increases the flexibility of the NAU88L20 to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU88L20 or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data. TDM bit **REG 0X1B[15]** and PCM_OFFSET_MODE_CTRL bit **REG 0X1B[14]** must beset to 1 for this application.

Normally, the DAC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. For each channel MSB is clocked on the BCLK rising edge defined by the delay count set in TSLOT_L0 bits **REG0X1E[9:0]** for left channel 0, and TSLOT_R0 bits **REG0X1F[9:0]** for right channel 1. The subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This can be seen in the figure below.

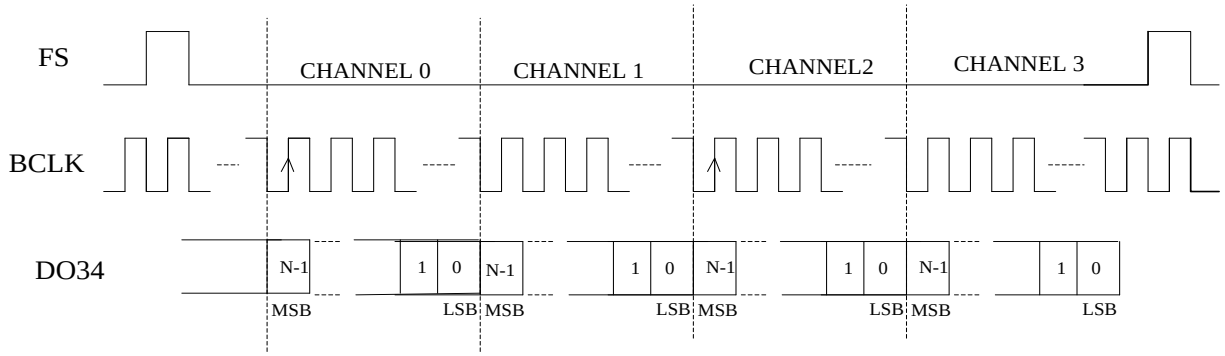


Figure 9.8: TDM PCM Offset Audio Format

10. Outputs

The NAU88L20 features a differential speaker output (SPKOUT+ and SPKOUT-). The speaker amplifier is designed to drive a load differentially; a configuration referred to as Bridge-Tied Load (BTL). The gain of the speaker driver can be set using the 2bit gain control SPK_GAIN_CNTRL bits **REG 0x52[1:0]** for left channel, and SPK_GAIN_CNTRR bits **REG 0x52[3:2]** for right channel. For gain values can be selected: -6dB, 0dB (default), +6dB and +12dB.

The differential speaker outputs can drive a single 16Ω speaker or two headphone loads of 32Ω or 64Ω or a line output. Driving the load differentially doubles the output voltage. The output of the speaker can be manipulated by changing attenuation and the volume (loudness of the output signal).
The output stage is powered by the speaker supply, VDDLO, which are capable of driving up to 1.3VRMS signals. The speaker outputs can be controlled and can be muted individually. The output pins are at reference DC level when the output is muted.

10.1 Lineout Driver

The Class AB amplifier includes a control circuit used in Lineout mode to precharge the amplifier output to the common mode voltage VCM (default 1.65V @ 3.3V). The precharge control smoothly charges the amplifier output towards VCM with negligible pop noise. Below is the code sequence to enable the precharge control and charge the output to VCM level and minimum pop noise.

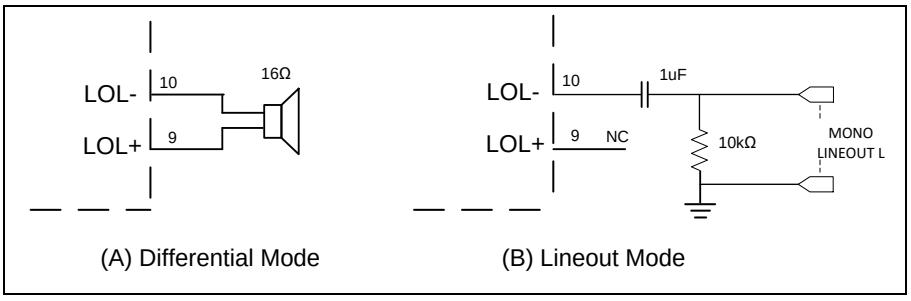


Figure 10.1: Output Load diagram (a) differential (b) Lineout

Step	**Reg	Value	Comments
1	0076	2000	[13] = 1 to keep slow rising VREF
2	002C	0072	[7:4] = 0x7 to turn on CIC and set CIC_GAIN_ADJ = x7, OSR128
	delay		//600ms by I2C dummy write
3	0073	3308	[12] = 1 to enable DAC, [8] = 1 to enable DAC clock, [3:2] = 2'b10 to select DAC VREF = 1.61V
4	0066	0062	[6] = 1 to enable VMID, [5:4]= 2b'10 VMID tie-off selection options
5	0076	3000	[13] = 1 to keep slow rising VREF; [12] = 1 for global bias enable
6	0051	0220	[9:6] VCM = 1.65V, [5] = 1 to enable VCM buffer, [4] = 0 to enable precharge, [3:2] = 2'b00 R-bias
	delay		//600ms by I2C dummy write
7	0001	0FF8	enable DAC, ADC in digital domain
8	0052	0200	[9:8] = 2b'10 bias current
9	007F	0003	[1:0] = 1 to power up the main speaker driver
10	0051	0230	[4] = 1 to disable precharge

Table 10: Lineout configuration for minimizing pop/click noise

11. Clock Detection

The NAU88L20 includes a Clock Detection circuit that can be used to enable and disable the audio path, based on an initialized audio path setting. If MCLK is detected on the input, a status flag in MCLK_DET_INT bit **REG 0x10[5]** will be set, when MCLKDETECT signal going active, as described by the block diagram below.

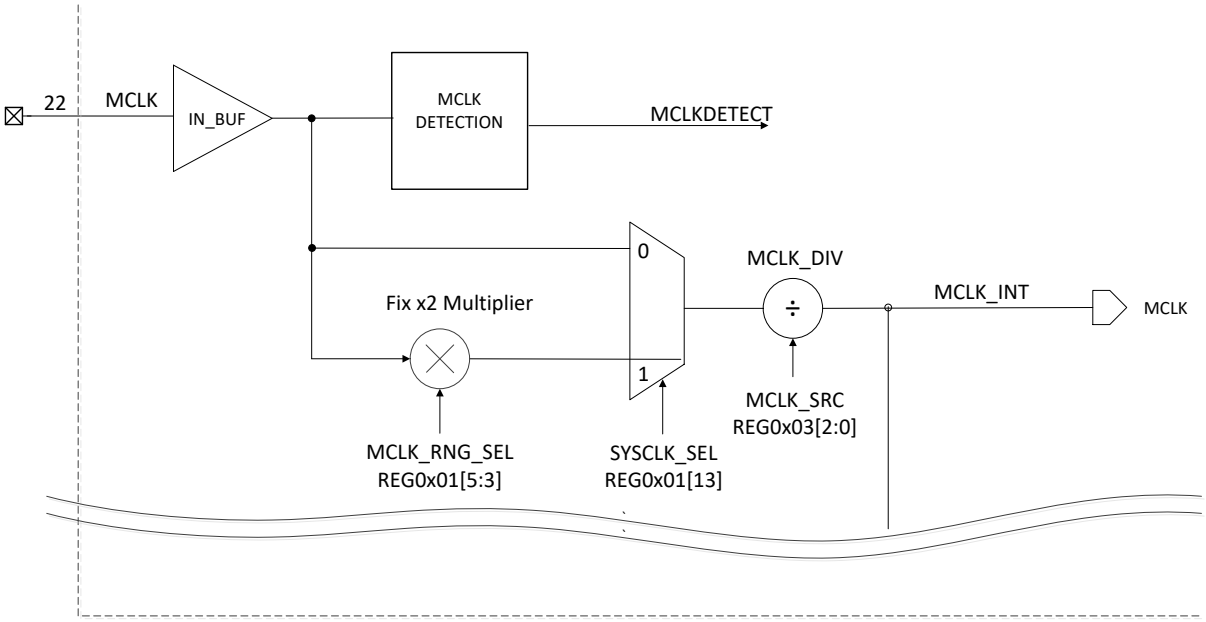


Figure 11: NAU88L20 Clock Detection

For MCLK/FS input pin in slave mode, the range of input frequency are defined here.

Input Signal	Pin Name	Min	Max	Unit
Frame Sync	FS	8	96	KHz
Master Clock	MCLK	2.048	24.576	MHz

Table 11 Range of MCLK/FS for Slave Mode

System design should be checked that MCLK/FS adhere to the frequency range, then follow the later section to pick out the correct setting, and supported combinations.

From MCLK input pin, the MCLK signal can be routed for two path, controlled by SYSCLK_SEL bit **REG 0x01[13].** Aside from the direct path (x1), the multiplier path applies a fix multiplier to double the MCLK frequency. In order to adjust for 50% duty cycle, MCLK_RNG_SEL bits **REG 0x01[5:3]** is a required frequency range setting while the multiplier path is selected. The MCLK input frequency range is divided into three bands, from 2.048MHz to 15.74MHz, 15.74MHz to 21.6MHz and, 21.6MHz to 24.576MHz by setting MCLK_RNG_SEL.

11.1 MCLK / FS Clock Setting in Slave Mode

For slave mode, the NAU88L20 can accept exteral clocks from MCLK/FS input pin. Based on the MCLK and FS input with internal logic to derive MCLK_INT, and CLK_DAC, CLK_ADC for related internal ADC/DAC, DSP, Digital Audio Interface and other internal subsystems.

The figure below provides the full clock distribution diagram, and the key registers are liste here:
MCLK_DIV, REG 0x03[2:0]
CLK_DAC_SRC, REG 0x03[5:4]
CLK_ADC_SRC, REG 0x03[7:6]

The NAU88L20 Clock distribution and subsystem is designed to minimize design effort with simplified setting. The relationship of MCLK/FS input frequency combinations will be described in details below.

The MCLK/FS input frequency range is described in previous section where MCLK input frequency should be between 2.048MHz ~ 24.567MHz and, FS should be between 8KHz ~ 96KHz.

The internal clock distribution of NAU88L20 is designed support 3 MCLK_INT/FS ratios, which are 256, 400, 500. Please note MCLK_INT refers to the, internal MCLK frequency after MCLK Divider. This means the MCLK/FS input frequency combination should consider the Multiplier/direct path selected by SYSCLK_SEL and, the MCLK_DIV divider. The table below are the key criterion for MCLK/FS input frequencies supported organized by the MCLK_INT/FS Ratio into 3 groups shown in Table 11.1.

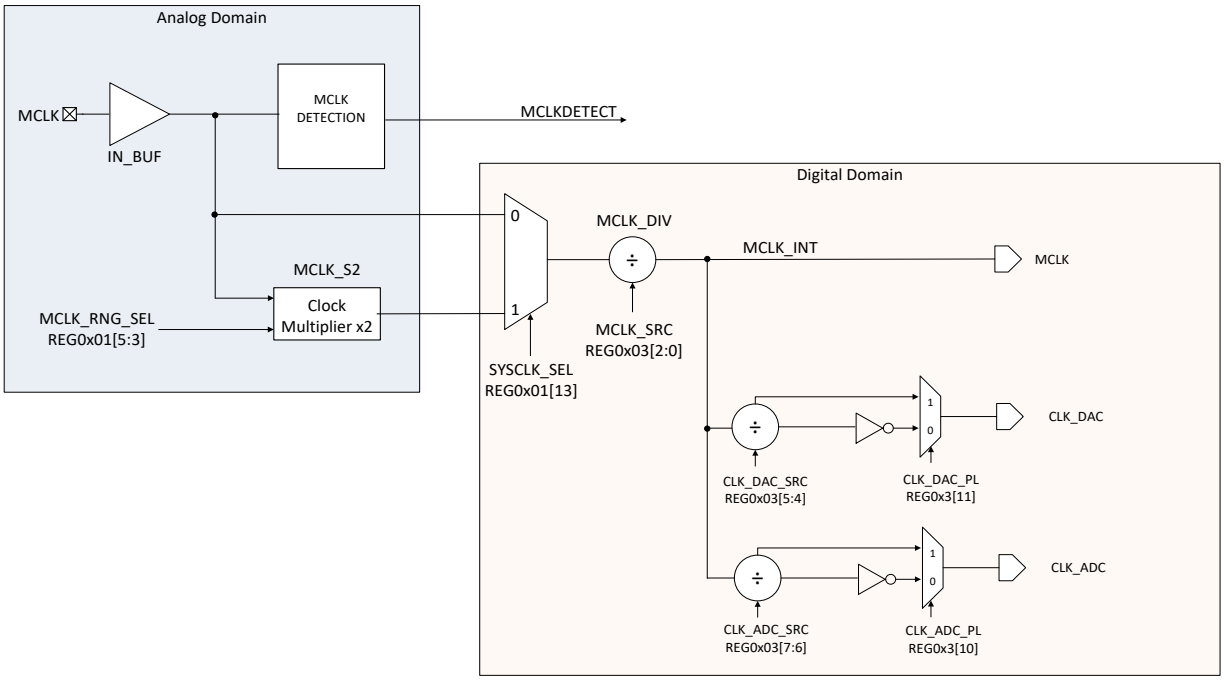


Figure 11.1 NAU88L20 MCLK and Clock Distribution

Following the above table, one more limit is added, from generating CLK_ADC, CLK_DAC, which should be less than or equal to 6.144MHz.
CLK_DAC = MCLK_INT * CLK_DAC_SRC
CLK_ADC = MCLK_INT * CLK_ADC_SRC

Below table are the key criterion for MCLK/FS input frequencies supported organized by the MCLK_INT/FS Ratio into 3 group.

Group1: MCLK_INT/FS Ratio of 256	
SYSCLK_SEL set x1 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***256
Register Related	**MCLK_DIV**, **SYSCLK_SEL**
SYSCLK_SEL set x2 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * MCLK_DIV*256/2
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL**
Group2: MCLK_INT/FS Ratio of 400	
SYSCLK_SEL set x1 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***400
Register Related	**MCLK_DIV**, **SYSCLK_SEL** **CLK_ADC_SRC, CLK_DAC_SRC** must set as 1/4
SYSCLK_SEL set x2 path	
Target FS	8/16/24 ..44.1/96KHz
MCLK	Target FS * **MCLK_DIV***400/2
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL** **CLK_ADC_SRC, CLK_DAC_SRC** must set as 1/4
Group 3: MCLK_INT/FS Ratio of 500	
SYSCLK_SEL x1/x2	
Notes	• Support list is provided in appendix • No need to set **CLK_DAC_SRC, CLK_DAC_SRC** is fixed
Register Related	**MCLK_DIV**, **MCLKSEL**, **SYSCLK_SEL**

Table 11.1 Criterion for supported MCLK/FS for slave mode

Following the 3 groups of criterion to pick out the correct MCLK/FS combinations is essential for system design.

11.2 ADC/DAC Oversampling Rate

ADC/DAC Oversample rate setting is used in the NAU88L20 ADC/DAC blocks beyond the CLK_DAC, CLK_ADC signal described in previous clock distribution figure.

The conditions to set OSR_ADC_RATE, OSR_DAC_RATE for MCLK_INT/FS ratio of 256 is listed below.

- CLK_ADC = OSR_ADC_RATE * FS (<=6.144MHz)
- CLK_DAC = OSR_DAC_RATE * FS (<=6.144MHz)

For MCLK_INT/FS ratios of 400/500, oversample rate is fixed at 100, therefore no need to set OSR_ADC_RATE/OSR_DAC_RATE

Example 1: MCLK=24.576MHz, FS=96KHz

- The Ratio here is picked as 24.576MHz = 256 * 96KHz
  - SYSCLK_SEL can be set either x1 or x2 path
  - For x1 path, MCLK_DIV is set as divid by 1, MCLK_INT=24.576MHz
  - For x2 path, MCLK_DIV is set as divid by 2, MCLK_INT=24.575MHz

- Based on CLK_ADC = MCLK_INT * CLK_ADC_SRC (<=6.144MHz)
  - Avialble OSR_ADC_RATE option for each CLK_ADC_SRC are listed below in Green for each CLK_ADC
  - For CLK_ADC as 6.144MHz, the ORS_ADC_RATE should be set as 64, so the clock would match as below table in green
  - For CLK_ADC as 3.072 MHz, the ORS_ADC_RATE should be set as 32, so the clock would match as below table in green

		CLK_ADC=MCLK_INT*CLK_ADC_SRC (<=6.144MHz)			
		24.576	12.288	6.144	3.072
FS*OSR (<=6.144MHz)	32			3.072	3.072
	64			6.144	6.144
	128			12.288	12.288
	256			24.576	24.576

Table 11.2 Criterion for supported ADC Oversampling rate

Example 2: MCLK=19.2MHz, FS=32KHz

The Ratio here is picked as 19.2MHz = 400 * 32KHz

o SYSCLK_SEL is set as x2 path

o For x2 path, MCLK_DIV is set as divid by 3, MCLK_INT=12.8MHz

With MCLK_INT/FS Ratio of 400.

o CLK_ADC_SRC/CLK_DAC_SRC must be set as divide by 4.

o No need to set OSR_ADC_RATE/OSR_DAC_RATE

12. Control and Status Registers

This section describes all the registers used in the NAU88L20. Here are couple of convention that needs to be aware of when you read this document:

- All base buffer addresses are on the 2-Byte boundary

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
0	HARDWARE_RST	HARDWARE_RESET																	**Hardware Reset** (Write any value ***once*** to reset all the registers.)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000 R/W**
1	ENA_CTRL	CMLCK_ENB																	**PGA Common Mode Lock Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		CLK_DAC_INV																	**DAC Clock Inversion In Analog Domain Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		SYSCLK_SEL																	**Master Clock Source Select** 0 = MCLK_PIN (DEFAULT - from Analog) 1 = MCLK_S2 (Clk multiplier path from Analog)
		DIG_RDAC_EN																	**RDAC Digital Power Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DIG_LDAC_EN																	**LDAC Digital Power Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DIG_RADC_EN																	**RADC Digital Power Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DIG_LADC_EN																	**LADC Digital Power Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DIG_CLK_ADC_EN																	**ADC Digital Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DIG_CLK_DAC_EN																	**DAC Digital Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		CLK_I2S_EN																	**I2S Clock Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		CLK_DRC_EN																	**DRC Clock Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MCLK_RNG_SEL																	**MCLK Input Frequency Range Select** (Mclksel) 000 = 12MHz, 12.288 MHz 100 = 19.2MHz 111 = 24.0 MHz, 24.576 MHz
		DEFAULT	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	**0x0FF0 R/W**
3	CLK_DIVIDER	CLK_CODEC_SRC																	**ADC & DAC Clock Source Select** 0 = from internal MCLK (DEFAULT) 1 = from MCLK_PIN or ½ DCO_CLK
		CLK_DAC_PL																	**DAC Clock Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted
		CLK_ADC_PL																	**ADC Clock Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		CLK_ADC_SRC																	**Scaling Divider For ADC Clock From CODEC_SRC** 00 = 1 01 = 1/2 (DEFAULT) 10 = 1/4 11 = 1/8
		CLK_DAC_SRC																	**Scaling Divider For DAC Clock From CODEC_SRC** 00 = 1 01 = 1/2 (DEFAULT) 10 = 1/4 11 = 1/8
		MCLK_SRC																	**Scaling Divider For MCLK From SYSCLK_SRC** 000 = 1 (DEFAULT) 001 = 1 and Inverted 010 = 1/2 011 = 1/3 100 = 1/4 110 = 1/6
		DEFAULT	0	0	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0x0050 R/W
F	INTERRUPT_MASK	IRQ_PL																	**IRQ Logic Select** 0 = Active low (DEFAULT) 1 = Active high
		IRQ_PS																	**IRQ Pin Pull Select** 0 = Pull down (DEFAULT) 1 = Pull up
		IRQ_PE																	**IRQ Pin Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		IRQ_DS																	**IRQ Drive Current Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		IRQ_OE																	**IRQ Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MCLKDET_INTP_MASK																	**Missing MCLK Detection Interrupt Mask** 0 = Unmask (DEFAULT) 1 = Mask the interrupt
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
10	IRQ_STATUS	MCLK_DET_INT																	**Missing MCLK Detection IRQ Status**
		DEFAULT	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	0x0000 READ ONLY
12	INTERRUPT_DIS_CTRL (WRITE MODE)	MCLKDET_INT_DIS																	**Missing MCLK Detection Interrupt Disable Control** 0 = Enable 1 = Disable
		DEFAULT	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	0xFFFF R/W
13	DMIC_CTRL	DMIC_DS																	**DMIC Drive Current Select** (For high ***Cload*** > 20pF, enable high drive current.) 0 = Low drive current (DEFAULT) 1 = High drive current
		DMIC_SLEW																	**DMIC Slew Rate Select** (For high ***Cload*** > 20pF, use faster slew rate.) 000 = Slowest slew rate (DEFAULT) ▼ 111 = Fastest slew rate
		CLK_DMIC_SRC																	**DMIC Clock Speed Select** 00 = ADC clock (DEFAULT) 01 = ADC clock / 2 10 = ADC clock / 4 11 = ADC clock / 8
		DMICEN																	**Digital Microphone Mode Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
14	CICI_ADJ	CICI_ADJ																	**ADC/DAC Digital Filter Control** (DEFAULT)
		DEFAULT	1	0	1	0	0	1	0	0	0	0	0	1	1	1	1	1	**0xA41F R/W**
15	CICD_ADJ	CICD_ADJ																	**ADC/DAC Digital Filter Control** (DEFAULT)
		DEFAULT	1	0	1	1	0	1	1	1	1	1	0	0	1	1	0	1	**0xB7CD R/W**
16	DITHER_CTRL	SDSEL																	**Dither Control** (DEFAULT)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0080 R/W**
1A	GPIO_CTRL	GPIO1POL																	**GPIO1 Polarity** 0 = Non-inverted (DEFAULT) 1 = Inverted logic of the CSB/GPIO1 function output selected by GPIO1SEL
		GPIO1SEL																	**CSB/GPIO1 Function Select** 000 = Output 0 (DEFAULT) 001 = Jack status from the AND/OR logic 010 = SCLK_I 011 = SD_I 100 = output divided FLL clock 101 = FLL locked condition (logic 1 = PLL locked) 110 = SD_O 111 = OSC_CLK
		GPIO1_PS																	**GPIO1CSB Pull Select** (If PE=1, OE=1) 0 = Pull up (DEFAULT) 1 = Pull down
		GPIO1_DS																	**GPIO1CSB Drive Current Select** 0 = Low drive current (DEFAULT) 1 = High drive current
		GPIO1_PE																	**GPIO1CSB Pin Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		GPIO1_OE																	**GPIO1CSB Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
1B	TDM_CTRL	TDM																	**TDM Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PCM_OFFSET_MODE_CTRL																	**PCM Offset In TDM Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADCPHS0																	**ADC Audio Data Left-right Ordering Select** 0 = Left ADC data in left phase of LRP (DEFAULT) 1 = Left ADC data in right phase of LRP (left-right reversed)
		DACPHS1																	**DAC Right Channel Audio Data Left-right Ordering Select** 0 = Right DAC data in right phase of LRP (DEFAULT) 1 = Right DAC data in left phase of LRP (left-right reversed)
		DACPHS0																	**DAC Left Channel Audio Data Left-right Ordering Select** 0 = Left DAC data in left phase of LRP (DEFAULT) 1 = Left DAC data in right phase of LRP (left-right reversed)
		DAC_LEFT_SEL																	**DAC Left Channel Source Under TDM Mode** I2S : 000 : From Slot 0 (DEFAULT) 001: From Slot 1 010 : From Slot 2 011: From Slot 3 100 : RESERVED 101: RESERVED 110 : RESERVED 111: RESERVED PCM: 000: From slot 0 001: From slot 1

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			(DEFAULT) 010: From slot 2 011: From slot 3 100: From slot 4 101: From slot 5 110: From slot 6 111: From slot 7
		DAC_RIGHT_SEL																	**DAC Right Channel Source Under TDM Mode** I2S: 000 : From Slot 0 (DEFAULT) 001: From Slot 1 010 : From Slot 2 011: From Slot 3 100 : RESERVED 101: RESERVED 110 : RESERVED 111: RESERVED PCM: 000: From slot 0 (DEFAULT) 001: From slot 1 010: From slot 2 011: From slot 3 100: From slot 4 101: From slot 5 110: From slot 6 111: From slot 7
		ADC_TX_SEL_L																	**ADC Left Channel Source Under TDM/I2S Mode** 00: From slot 0 (DEFAULT) 01: From slot 2 10: From slot 4 11: From slot 6
		ADC_TX_SEL_R																	**ADC Right Channel Source Under TDM/I2S Mode** 00: From slot 1 (DEFAULT) 01: From slot 3 10: From slot 5 11: From slot 7
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000 R/W**
1C	I2S_PCM_CTRL1	DACCM0																	**DAC Companding Mode Select** 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding
		ADCCM0																	**ADC Companding Mode Select** 00 = Off (DEFAULT - Normal linear operation) 01 = RESERVED 10 = μ-law companding 11 = A-law companding
		ADDAP0																	**ADC Output Data Stream Directly Routed To DAC Input Data Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CMB8_0																	**8-bit Word For Companding Mode Of Operation Enable Control** 0 = Normal operation (DEFAULT - No companding) 1 = 8-bit operation for companding mode
		UA_OFFSET																	**uLaw Offset Select** 0 = 1's complement (DEFAULT) 1 = 2's complement
		BCP0																	**Bit Clock Phase Inversion Option For BCLK** 0 = Non-inverted (DEFAULT) 1 = Inverted
		LRP0																	**PCMA & PCMB Left/right Word Ordering Select** 0 = Right Justified/Left Justified/I2S/PCMA mode (DEFAULT) 1 = PCMB Mode Enable: MSB is valid on 1st rising edge of BCLK after rising edge of FS
		WLEN0																	**Word Length of Audio Data Stream Select** 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length (DEFAULT) 11 = 32-bit word length
		AIFMT0																	**Audio Interface Data Format Select** 00 = Right justified 01 = Left justified 10 = Standard I2S format (DEFAULT) 11 = PCMA or PCMB audio data format option
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	**0x000A R/W**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
1D	I2S_PCM_CTRL2	I2S_TRI																	**I2S Tri-state Enable Control** 0 = Normal mode 1 = Output high Z (DEFAULT)
		I2S_DRV																	**I2S Drive Enable Control** 0 = Normal mode (DEFAULT) 1 = Always out
		LRC_DIV																	**LRC(FS) Divider From BCLK Frequency** 00 = 1/256 (DEFAULT) 01 = 1/128 10 = 1/64 11 = 1/32
		PCM_TS_EN0																	**PCM Time Slot Function Enable Control** (Only PCM_A_MODE or PCM_B_MODE (STEREO Only) can be used when PCM Mode is selected.) 0 = Disable time slot function for PCM mode (DEFAULT) 1 = Enable time slot function for PCM mode
		TRI0																	**Without TDM Mode** 0 = Drive the full clock of LSB (DEFAULT) 1 = Tri-state the 2nd half of LSB
		PCM8BIT0																	**PCM 8 Bit Select** 0 = Use I2S_PCM_CTRL.WLEN to select word length (DEFAULT) 1 = PCM select 8-bit word length
		ADCDAT0_PE																	**ADCDAT IO Pull Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADCDAT0_PS																	**ADCDAT IO Pull Up/Down Enable Control** 0 = Pull down (DEFAULT) 1 = Pull up
		ADCDAT0_OE																	**ADCDAT IO Output Enable Control** 0 = ADCDAT not always out (DEFAULT - when no data out, ADCOUT pin becomes high.) 1 = ADCDAT always out
		MS0																	**Master/Slave Mode Enable Control** 0 = Slave mode (DEFAULT) 1 = Master mode
		BCLKDIV																	**BCLK Divider From MCLK Frequency** 000 = 1 (DEFAULT) 001 = 1/2 010 = 1/4 011 = 1/8 100 = 1/16 101 = 1/32
		DEFAULT	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x8000 R/W**
1E	LEFT_TIME_SLOT	FS_ERR_CMP_SEL																	**Triggers Short Frame Sync Signal** (If frame sync is less than) 00 = 252 x MCLK (DEFAULT) 01 = 253 x MCLK 10 = 254 x MCLK 11 = 255 x MCLK
		DIS_FS_SHORT_DET																	**Short Gram Sync Detection Logic Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		TSLOT_L0																	**Left channel PCM Time Slot Start Value / PCM TDM Offset Mode Slot Start Value** (Each slot interval is equal to word length.) if word length is 8bit: slot0: 0x01, slot1: 0x09, slot2: 0x11, ... Each slot interval is equal to 8. if word length is 16bit: slot0: 0x01, slot1: 0x11, slot2: 0x21, ... Each slot interval is equal to 16. if word length is 20bit: slot0: 0x01, slot1: 0x15, slot2: 0x29, ... Each slot interval is equal to 20. if word length is 24bit: slot0: 0x01, slot1: 0x19, slot2: 0x31, ... Each slot interval is equal to 24. if word length is 32bit: slot0: 0x01, slot1: 0x21, slot2: 0x41, ...

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			Each slot interval is equal to 32.
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
1F	RIGHT_TIME_SLOT	TSLOT_R0																	**Right channel PCM Time Slot Start Value / unused for PCM TDM Offset Mode** (Each slot interval is equal to word length.) if word length is 8bit: slot0: 0x01, slot1: 0x09, slot2: 0x11, ... Each slot interval is equal to 8. if word length is 16bit: slot0: 0x01, slot1: 0x11, slot2: 0x21, ... Each slot interval is equal to 16. if word length is 20bit: slot0: 0x01, slot1: 0x15, slot2: 0x29, ... Each slot interval is equal to 20. if word length is 24bit: slot0: 0x01, slot1: 0x19, slot2: 0x31, ... Each slot interval is equal to 24. if word length is 32bit: slot0: 0x01, slot1: 0x21, slot2: 0x41, ... Each slot interval is equal to 32.
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
21	BIQ0_COF1	BIQ0_A1_L																	Program DAC BIQ0_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
22	BIQ0_COF2	BIQ0_A1_H																	Program DAC BIQ0_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
23	BIQ0_COF3	BIQ0_A2_L																	Program DAC BIQ0_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
24	BIQ0_COF4	BIQ0_A2_H																	Program DAC BIQ0_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
25	BIQ0_COF5	BIQ0_B0_L																	Program DAC BIQ0_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
26	BIQ0_COF6	BIQ0_B0_H																	Program DAC BIQ0_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
27	BIQ0_COF7	BIQ0_B1_L																	Program DAC BIQ0_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
28	BIQ0_COF8	BIQ0_B1_H																	Program DAC BIQ0_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
29	BIQ0_COF9	BIQ0_B2_L																	Program DAC BIQ0_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
2A	BIQ0_COF10	BIQ0_EN																	**BIQ DAC Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BIQ0_B2_H																	Program DAC BIQ0_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
2B	ADC_RATE	ADC_L_SRC																	**In Non-DMIC Mode** 0 = Latch left channel analog data input into the left channel filter (DEFAULT) 1 = Latch right channel analog data input into the left channel filter **In DMIC Mode** 0 = Left channel in rising edge (DEFAULT) 1 = Left channel in falling edge

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		ADC_R_SRC																	**In Non-DMIC Mode** 0 = Latch right channel analog data input into the right channel filter (DEFAULT) 1 = Latch left channel analog data input into the right channel filter **In DMIC Mode** 0 = Right channel in falling edge (DEFAULT) 1 = Right channel in rising edge
		SMPL_RATE																	**Generating 2.048MKHz Based On Sample Rates** 000 = 48K (DEFAULT) 001 = 32K 110 = 96K 111 = 192K
		ADC_RATE																	**ADC SINC Down Select** 00 = Down 32 01 = Down 64 10 = Down 128 11 = Down 256 (DEFAULT)
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0x0002 R/W
2C	DAC_CTRL1	CIC_GAIN_ADJ																	For Fine Tuning SDAC Output
		DACOSR32																	**DAC Oversample Rate Select @ 32** **DAC Oversample Rate Select @ 128** **DAC Oversample Rate Select @ 256** (If **DAC_CTRL1**[2:0] = 000, will get DAC Oversample Rate Select @ 64. If multiple bits are set, the priority is DACOSR256>DACOSR32>DACOSR128.) 000 = DAC Oversample Rate Select @ 64 001 = DAC Oversample Rate Select @ 256 010 = DAC Oversample Rate Select @ 128 011 = DAC Oversample Rate Select @ 256 100 = DAC Oversample Rate Select @ 32 101 = DAC Oversample Rate Select @ 256 110 = DAC Oversample Rate Select @ 32 111 = DAC Oversample Rate Select @ 256
		DACOSR128																	
		DACOSR256																	
		DEFAULT	0	0	0	0	0	0	0	0	0	1	1	1	0	0	1	0	0x0072 R/W
2D	DAC_CTRL2	DEM_DITHER																	**Probability Of First Order Dynamic Element Matching+Dithering** (Step size is 1/16.) (Set the probability of each of the 32 DAC elements being selected used in calibration of the DEM. A higher value increases the probability, so less toggling.) 0000=No dithering 0001=1/16 0010=2/16 0011=3/16 0100=4/16 0101=5/16 0110=6/16 0111=7/16 1000=8/16 1001=9/16 1010=10/16 1011=11/16 1100=12/16 1101=13/16 1110=14/16 1111=15/16

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		SDMOD_DITHER																	**Bit Numbers Of Dithering On SD Modulator** (Step size is 1bit.) 00000 = No dithering (DEFAULT) 00001 = 1 00010 = 2 00011 = 3 00100 = 4 00101 = 5 00110 = 6 00111 = 7 01000 = 8 01001 = 9 01010 = 10 01011 = 11 01100 = 12 01101 = 13 01110 = 14 01110 = 15
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
2F	**DAC_DGAIN_CTRL**	DAC1_TO_DAC0_ST																	**DAC CH1 to DAC CH0 Crosstalk Suppression Sidetone Select** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB ▼ 0x43 = -70dB 0x42 = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute (DEFAULT)
		DAC0_TO_DAC1_ST																	**DAC CH0 to DAC CH1 Crosstalk Suppression Sidetone Select** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB ▼ 0x43 = -70dB 0x42 = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute (DEFAULT)
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
30	**ADC_DGAIN_CTRL**	ADC0_TO_DAC0_ST																	**ADC to DAC CH0 Sidetone Select** (Step size is 3dB.) 0x00 = Mute (DEFAULT) 0x01 = -42dB ▼ 0x0E = -3dB 0x0F = 0dB
		ADC1_TO_DAC1_ST																	**ADC to DAC CH1 Sidetone Select** (Step size is 3dB.) 0x00 = Mute (DEFAULT) 0x01 = -42dB ▼ 0x0E = -3dB 0x0F = 0dB
		DAC0_ST_SEL																	**DAC CH0 Sidetone Source Select** 0 = Select ADC CH0 as the side tone source of the DAC CH0 (DEFAULT) 1 = Select ADC CH1 as the side tone source of the DAC CH0
		DAC1_ST_SEL																	**DAC CH1 Sidetone Source Select** 0 = Select ADC CH1 as the side tone source of the DAC CH1 (DEFAULT) 1 = Select ADC CH0 as the side tone source of the DAC CH1

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
31	MUTE_CTRL	PGA_SMUTE_STEP																	**Analog Attn Mute Step Select** 00 = 128 sample 01 = 32 sample (DEFAULT) 10 = 16 sample 11 = 1 sample
		DAC_SLOW_UM																	**DAC Slow Soft Unmute Enable Control** 0 = Disable (16 MCLK per step soft unmute) (DEFAULT) 1 = Enable (512 MCLK per step soft unmute)
		DAC_ZC_UP_EN																	**DAC Zero Crossing Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		AMUTE_EN																	**Auto Mute Enable Control** (Generate null output to analog circuitry when 1024 consecutive zeros are detected. De-assert as soon as first non-zero sample is detected.) 0 = Disable (DEFAULT) 1 = Enable
		AMUTE_CTRL																	**Auto Mute Control** 0 = Both DAC channels must have 0 values for 1024 samples before AMUTE turns on (DEFAULT) 1 = Either Ch0 or Ch1 must have 1024 consecutive zero samples
		SMUTE_EN																	**DAC Soft Mute Enable Control** 0 = Release DAC volume by **SMUTE_CTRL** (DEFAULT - 0 to Gain) 1 = Gradually mute DAC volume (Gain to 0)
		SMUTE_CTRL																	**DAC Soft Release Enable Control** 0 = Immediately release DAC volume (DEFAULT) 1 = Gradually release DAC volume
		DAC_SVOL_EN																	**DAC Soft Volume Change Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADC_SVOL_EN																	**ADC Soft Volume Change Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADC_ZC_UP_EN																	**ADC Zero Crossing Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ADC_SMUTE_EN																	**ADC Soft Mute Enable Control** 0 = Release ADC volume by **ADC_SMUTE_CTRL** (DEFAULT - 0 to Gain) 1 = Gradually mute ADC volume (Gain to 0)
		ADC_SMUTE_CTRL																	**ADCSoft Release Enable Control** 0 = Immediately release ADC volume (DEFAULT) 1 = Gradually release ADC volume
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
32	DRC_GAIN_LADC	DRC_GAIN_LADC																	**DRC LADC Gain Control**
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0x0200 READ ONLY
33	DRC_GAIN_RADC	DRC_GAIN_RADC																	**DRC RADC Gain Control**
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0x0200 READ ONLY
34	DAC_DGAIN_CTRL1	DGAINR_DAC																	**DAC Right Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x4B = -66dB 0x4A = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DGAINL_DAC																	**DAC Left Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x4B = -66dB 0x4A = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute
		DEFAULT	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0xCFCF R/W**
35	ADC_DGAIN_CTRL1	DGAINR_ADC																	**ADC Right Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x4B = -66dB 0x4A = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute
		DGAINL_ADC																	**ADC Left Volume Control** (Step size is 0.5dB.) 0xFF = +24dB 0xFE = +23.5dB ▼ 0xCF = 0dB (DEFAULT) ▼ 0x4B = -66dB 0x4A = RESERVED ▼ 0x0F = RESERVED 0x0E = Mute 0x00 = Mute
		DEFAULT	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0xCFCF R/W**
36	ADC_DRC_KNEE_IP12	DRC_ENA_ADC																	**DRC ADC Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_IP_ADC																	**DRC ADC Knee Point 2 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x3E = -62dB 0x3F = -63dB
		DRC_SMTH_ENA_ADC																	**DRC ADC Smooth Filter Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_IP_ADC																	**DRC ADC Knee Point 1 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x1486 R/W**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
37	ADC_DRC_KNEE_IP34	DRC_KNEE4_IP_ADC																	**DRC ADC Knee Point 4 Select** (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_IP_ADC																	**DRC ADC Knee Point 3 Select** (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	0	0	0	0	1	1	1	1	0	0	0	1	0	0	1	0	**0x0F12 R/W**
38	ADC_DRC_SLOPES	DRC_NG_SLP_ADC																	**DRC ADC Noise Gate Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_ADC																	**DRC ADC Expansion Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = RESERVED
		DRC_CMP2_SLP_ADC																	**DRC ADC Compressor Slope (Lower Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_ADC																	**DRC ADC Compressor Slope (Higher Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101-110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_ADC																	**DRC ADC Limiter Slope** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1 (DEFAULT)
		DEFAULT	0	0	1	0	0	1	0	1	1	1	1	1	1	1	1	1	**0x25FF R/W**
39	ADC_DRC_ATKDCY	DRC_PK_COEF1_ADC																	**DRC ADC Peak Detection Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1001= 511*Ts
		DRC_PK_COEF2_ADC																	**DRC ADC Peak Detection Release Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts (DEFAULT) 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1001= 16383*Ts

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_ATK_ADC																	**DRC ADC Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_ADC																	**DRC ADC Decay Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 =4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 = 32757*Ts 1010 = 65535*Ts
		DEFAULT	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0x3457 R/W**
3A	DAC_DRC_KNEE_IP12	DRC_ENA_DAC																	**DRC DAC Channel Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DRC_KNEE2_IP_DAC																	**DRC DAC Knee Point 2 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x14 = -20dB (DEFAULT) ▼ 0x1E = -62dB 0x1F = -63dB
		DRC_SMTH_ENA_DAC																	**DRC DAC Smooth Filter Enable Control** 0 = Disable 1 = Enable (DEFAULT)
		DRC_KNEE1_IP_DAC																	**DRC DAC Knee Point 1 Select** (Step size is 1dB.) 0x00 = 0dB 0x01 = -1dB ▼ 0x06 = -6dB (DEFAULT) ▼ 0x1E = -30dB 0x1F = -31dB
		DEFAULT	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**	**0**	**0x1486 R/W**
3B	DAC_DRC_KNEE_IP34	DRC_KNEE4_IP_DAC																	**DRC DAC Knee Point 4 Select** (Step size is 1dB.) 0x00 = -35dB 0x01 = -36dB ▼ 0x0F = -50dB (DEFAULT) ▼ 0x1E = -97dB 0x1F = -98dB
		DRC_KNEE3_IP_DAC																	**DRC DAC Knee Point 3 Select** (Step size is 1dB.) 0x00 = -18dB 0x01 = -19dB ▼ 0x12 = -36dB (DEFAULT) ▼ 0x1E = -80dB 0x1F = -81dB
		DEFAULT	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0x0F12 R/W**
3C	DAC_DRC_SLOPES	DRC_NG_SLP_DAC																	**DRC DAC Noise Gate Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1
		DRC_EXP_SLP_DAC																	**DRC DAC Expansion Slope** 00 = 1:1 01 = 2:1 10 = 4:1 (DEFAULT) 11 = 8:1

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		DRC_CMP2_SLP_DAC																	**DRC DAC Compressor Slope (Lower Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = RESERVED 110 = RESERVED 111 = 1 (DEFAULT)
		DRC_CMP1_SLP_DAC																	**DRC DAC Compressor Slope (Higher Region)** 000 = 0 001 = 1:2 010 = 1:4 011 = 1:8 100 = 1:16 101 = RESERVED 110 = RESERVED 111 = 1 (DEFAULT)
		DRC_LMT_SLP_DAC																	**DRC DAC Limiter Slope** 000 = 0 001 = 1:2 (DEFAULT) 010 = 1:4 011 = 1:8 100 = 1:16 101 = 1:32 110 = 1:64 111 = 1
		DEFAULT	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**0**	**1**	**0x25F9 R/W**
3D	**DAC_DRC_ATKDCY**	DRC_PK_COEF1_DAC																	**DRC DAC Peak Detection Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts (DEFAULT) 0100 = 31*Ts 0101 = 63*Ts 0110 = 127*Ts 0111 = 255*Ts 1XXX = RESERVED
		DRC_PK_COEF2_DAC																	**DRC DAC Peak Detection Release Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts (DEFAULT) 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts 1XXX = RESERVED
		DRC_ATK_DAC																	**DRC DAC Attack Time** (Ts = 1/SMPL_RATE) 0000 = Ts 0001 = 3*Ts 0010 = 7*Ts 0011 = 15*Ts 0100 = 31*Ts 0101 = 63*Ts (DEFAULT) 0110 = 127*Ts 0111 = 255*Ts 1000 = 511*Ts 1001 = 1023*Ts 1010 = 2047*Ts 1011 = 4095*Ts 1100 = 8191*Ts
		DRC_DCY_DAC																	**DRC DAC Decay Time** (Ts = 1/SMPL_RATE) 0000 = 63*Ts 0001 = 127*Ts 0010 = 255*Ts 0011 = 511*Ts 0100 = 1023*Ts 0101 = 2047*Ts 0110 = 4095*Ts 0111 = 8191*Ts (DEFAULT) 1000 = 16383*Ts 1001 =32757*Ts 1010 = 65535*Ts
		DEFAULT	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	**1**	**1**	**0x3457 R/W**
41	**BIQ1_COF1**	**BIQ1_A1_L**																	**Program ADC BIQ1_A1 Parameter Bit[15:0]**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
42	**BIQ1_COF2**	**BIQ1_A1_H**																	**Program ADC BIQ1_A1 Parameter Bit[18:16]**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
43	BIQ1_COF3	BIQ1_A2_L																	Program ADC BIQ1_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
44	BIQ1_COF4	BIQ1_A2_H																	Program ADC BIQ1_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
45	BIQ1_COF5	BIQ1_B0_L																	Program ADC BIQ1_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
46	BIQ1_COF6	BIQ1_B0_H																	Program ADC BIQ1_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
47	BIQ1_COF7	BIQ1_B1_L																	Program ADC BIQ1_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
48	BIQ1_COF8	BIQ1_B1_H																	Program ADC BIQ1_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
49	BIQ1_COF9	BIQ1_B2_L																	Program ADC BIQ1_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
4A	BIQ1_COF10	BIQ1_EN																	**BIQ ADC Path Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BIQ1_B2_H																	Program ADC BIQ1_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
4C	IMM_MODE_CTRL	DACIN_SRC																	**DAC Filter Input Source Select** (IMM_MODE enabled from built-in sine generator) 00: From DRC DAC Output (DEFAULT) 01: From DAC Mixer Output 10: From u/A-law decode output 11: None
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
51	VCM_BUF	VCM_GAIN_CTRL																	**VCM Buffer Gain Control** (For VDDLO = 3.3V) 1000 = 1.65V (DEFAULT)
		PDB_VCMBUF																	**VCM Buffer Power Enable Control** 0 = Disable (DEFAULT) 1 = Enabless
		VOUT_PRE_DISB																	**eFuse Output VCM Pre-charge Enable Control** 0 = Enable (DEFAULT) 1 = Disable
		IB_CTRL																	**VCM Pre-charge R-bias Control** (Step size is 5K.) 00 = 75K 01 = 70K 10 = 65K 11 = 60K
		CURR_BOOST																	**Pre-charge 2X Slew Rate Enable Control** (For Cout = 4.7uF) 0 = Disable (DEFAULT) 1 = Enable
		TURBO_BOOST																	**Pre-charge 4X Slew Rate Enable Control** (For Cout = 4.7uF) 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0x0200 R/W
52	SPK_CTRL	PULL_SPKR_DWN																	**Class-AB Output Pulled Down to GND Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_SPKR																	**Right Speaker Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		MUTE_SPKL																	**Left Speaker Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MDRV_IB_SEL																	**Class-AB Amplifier Bias Current Select** 00 = No current (DEFAULT) 01 = 0.5uA 10 = 1.0uA 11 = 1.5uA
		SPK_GAIN_CTRLR																	**Right Speaker 2-bit Gain Select** 00 = 0dB (DEFAULT) 01 = +6dB 10 = +12dB 11 = -6dB
		SPK_GAIN_CTRLL																	**Left Speaker 2-bit Gain Select** 00 = 0dB (DEFAULT) 01 = +6dB 10 = +12dB 11 = -6dB
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000 R/W**
55	MISC_CTRL	RESERVED																	**RESERVED**
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000 R/W**
58	I2C_DEVICE_ID	I2C_DEVICE_ID [6:1]																	**I2C Device ID Read In**
		SILICON REVISION ID																	**Silicon Revision Bits**
		DEFAULT	X	0	0	1	1	0	1	1	0	0	1	1	1	1	0	0	**0x1BF0 READ ONLY**
59	SARDOUT_RAM_STATUS	RAM_TEST_FINISH																	**RAM Test Status** 0 = Test not finished 1 = Test finished
		RAM_TEST_FAIL																	**RAM Test Result** 0 = Test passed 1 = Test failed
		ANALOG_MUTE																	**Analog Mute Enable Control** 0 = Disable 1 = Enable
		DEFAULT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**0x2000 READ ONLY**
5A	SOFTWARE_RST	SW_RESET																	**Software Reset** (Write any value ***twice*** to reset all internal states without resetting the config registers.)
66	BIAS_ADJ	DAC_VREF_CAP																	**DAC VREF-ground Capacitor Select** 00 = None (DEFAULT) 11 = Add all 3 capacitors
		VMIDEN																	**VMID Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		VMIDSEL																	**VMID Tie-off Impedance Select** 00 = Open (DEFAULT) 01 = 25k Ohm 10 = 125k Ohm 11 = 2.5k Ohm
		BIASADJ																	**PGA Master Bias Current Power Select** 00 = Normal operation (DEFAULT) 01 = 9% reduced bias current from normal 10 = 17% reduced bias current from normal 11 = 11% increased bias current from normal
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000 R/W**
69	ANALOG_CONTROL_1	LDO_GAIN_CTRL																	**LDO Gain Select** 00 = 1.8V (DEFAULT) 01 = 1.6V 10 = 1.5V 11 = 1.9V
		LIN_MUX_SEL																	**Input Mode Select** 0 = Microphone mode (DEFAULT) 1 = Line-in mode
		BYPASS_DIG_LDO																	**Digital LDO Bypass Mode Select** 0 = Normal mode (DEFAULT) 1 = Bypass mode

REG	Function	Name	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
		EN_BG					■												**Bandgap Power Enable Control** (Bandgap needs to be on before LDOs can be enabled. In standby mode BG&LDOs are off.) 0 = Disable (DEFAULT) 1 = Enable
		DIG_LDO_EN						■											**Digital LDO Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ANA_LDO_EN							■										**Analog LDO Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		THD_BOOST								■									**DAC To Output Path THD Boost Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
6B	MUTE_PGA_CTRL	MUTE_LPGAN											■						**LPGA Negative Input Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_RPGAN												■					**RPGA Negative Input Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_LPGAP													■				**LPGA Positive Input Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_RPGAP														■			**RPGA Positive Input Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_LPGA															■		**LPGA Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		MUTE_RPGA																■	**RPGA Mute Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
72	ADC_CTRL	ADC_UPL			■														**LPGA Bias Current Increase Enable Control** (For driving ADC at high sample rates) 0 = Disable (DEFAULT) 1 = Enable
		ADC_UPR				■													**RPGA Bias Current Increase Enable Control** (For driving ADC at high sample rates) 0 = Disable (DEFAULT) 1 = Enable
		BIAS					■	■											**ADC Bias Current Select** 00 = Nominal (DEFAULT) 01 = Double 10 = Half 11 = Quarter
		VREFSEL							■	■									**ADC VREF Select** 00 = Analog supply (DEFAULT) 01 = VMID 10 = VMID + 0.5dB 11 = VMID + 1dB
		ANA_LADC_EN										■							**LADC Analog Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ANA_RADC_EN												■					**RADC Analog Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
73	DAC_CTRL3	ANA_RDAC_EN			■														**RDAC Analog Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ANA_LDAC_EN				■													**LDAC Analog Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		ANA_CLK_DAC_EN							■	■									**DAC Analog Clock Enable Control** 0 = Disable (DEFAULT) 1 = Enable Bit0 = Left DAC Bit1 = Right DACs

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
		FC_CTR																	**DAC Smoothing Filter On HS Output Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		CLK_DAC_DELAY																	**DAC Clock Delay Setting**
		DACVREFSEL																	**DAC Full Scale Reference Voltage Select** (By setting this value, it will change DAC full scale output. For best performance, use default value.) 00 = External VDDA 01 = 1.5V 10 = 1.6V (DEFAULT) 11 = 1.7V
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0x0008 R/W**
74	MIC_BIAS	MICBIAS_POWERUP																	**MICBIAS Power Enable** 0 = Disable (DEFAULT) 1 = Enable
		MICBIAS_LPMODE																	**MICBIAS Power Mode Select** 00 = Low noise mode (DEFAULT) 01 = Low power mode
		MICBIAS_LVL																	**MICBIAS Output Level Select** 000 = VDDA 001 = 1.1x VDDA 010 = 1.2x VDDA 011 = 1.3x VDDA 100 = 1.4x VDDA (DEFAULT) 101 = 1.53x VDDA
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0x0004 R/W**
76	BOOST	STG2_SEL																	**PGA In Class-A Mode Of Operation Enable Instead Of Class-AB Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		PDVMDFST																	**VMID Pre-charge Disable Control** 0 = Disable (DEFAULT) 1 = Enable
		BIASEN																	**Global Analog Bias Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DISCHRG																	**Charge Input Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BYPS_IBCTR																	**Bypass PGA Current Control Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		BOOSTDIS																	**HP Boost Driver Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		BOOSTGDIS																	**HP Boost Driver In Class-G Mode Disable Control** 0 = Enable (DEFAULT) 1 = Disable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
77	FEPGA	ACDC_CTRL																	**Input Pin DC State Enable Control** (Effective when DISCHRG = 1) 0 = Disable (DEFAULT) 1 = Enable Bit0 = Charges MICP to VREF Bit1 = Charges MICN to VREF
		CMLCK_ADJ																	**PGA Common Mode Threshold Lock Adjust** 00 = (DEFAULT)
		IB_LOOP_CTR																	**PGA Current Trim** 0 = (DEFAULT)
		IBCTR_CODE																	**PGA Current Trim** 000 = (DEFAULT)
		FEPGA_MODEL																	**Left PGA Mode Select** 0 = Disable (DEFAULT) 1 = Enable MODE[0] = Anti-aliasing filter adjust

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
																			MODE[1] = Disconnects LLIN, MICL+, MICL- MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially
		FEPGA_MODER																	**Right PGA Mode Select** 0 = Disable (DEFAULT) 1 = Enable MODE[0] = Anti-aliasing filter adjust MODE[1] = Disconnects RLIN, MICR+, MICR- MODE[2] = No function MODE[3] = Shorts the inputs and terminates with 12kOhm differentially
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
7E	PGA_GAIN	PGA_GAIN_L																	**Left PGA Gain** (Step size is 1dB.) 000000 = -1dB (DEFAULT) 000001 = 0dB ▼ 100100 = 35dB 100101 = 36dB
		PGA_GAIN_R																	**Right PGA Gain** (Step size is 1dB.) 000000 = -1dB (DEFAULT) 000001 = 0dB ▼ 100100 = 35dB 100101 = 36dB
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
7F	POWER_UP_CTRL	LPGA_EN																	**LPGA Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		RPGA_EN																	**RPGA Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		RSPK_EN																	**RSPK Driver Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		LSPK_EN																	**LSPK Driver Power Enable Control** 0 = Disable (DEFAULT) 1 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
80	IO_DRIVE_STRENGTH_CTRL	BCLK_DS																	**BCLK IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		FS_DS																	**FS IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		ADCDAT_DS																	**ADCDAT IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		SDA_DS																	**SDA IO Drive Strength Control** 0 = Normal (DEFAULT) 1 = Stronger
		PDB_DAC																	**DAC Right / Left Power Down Bar Enable Control** 00 = Disable (DEFAULT) 11 = Enable
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
81	BIQ02_COF1	BIQ02_A1_L																	**Program DAC BIQ02_A1 Parameter Bit[15:0]**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
82	BIQ02_COF2	BIQ02_A1_H																	**Program DAC BIQ02_A1 Parameter Bit[18:16]**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**
83	BIQ02_COF3	BIQ02_A2_L																	**Program DAC BIQ02_A2 Parameter Bit[15:0]**
		DEFAULT	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000 R/W**

REG	Function	Name	Bit																Description
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
84	BIQ02_COF4	BIQ02_A2_H																	Program DAC BIQ02_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
85	BIQ02_COF5	BIQ02_B0_L																	Program DAC BIQ02_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
86	BIQ02_COF6	BIQ02_B0_H																	Program DAC BIQ02_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
87	BIQ02_COF7	BIQ02_B1_L																	Program DAC BIQ02_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
88	BIQ02_COF8	BIQ02_B1_H																	Program DAC BIQ02_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
89	BIQ02_COF9	BIQ02_B2_L																	Program DAC BIQ02_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
8A	BIQ02_COF10	BIQ02_B2_H																	Program DAC BIQ02_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
91	BIQ12_COF1	BIQ12_A1_L																	Program ADC BIQ12_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
92	BIQ12_COF2	BIQ12_A1_H																	Program ADC BIQ12_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
93	BIQ12_COF3	BIQ12_A2_L																	Program ADC BIQ12_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
94	BIQ12_COF4	BIQ12_A2_H																	Program ADC BIQ12_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
95	BIQ12_COF5	BIQ12_B0_L																	Program ADC BIQ12_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
96	BIQ12_COF6	BIQ12_B0_H																	Program ADC BIQ12_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
97	BIQ12_COF7	BIQ12_B1_L																	Program ADC BIQ12_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
98	BIQ12_COF8	BIQ12_B1_H																	Program ADC BIQ12_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
99	BIQ12_COF9	BIQ12_B2_L																	Program ADC BIQ12_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
9A	BIQ12_COF10	BIQ12_B2_H																	Program ADC BIQ12_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A1	BIQ03_COF1	BIQ03_A1_L																	Program DAC BIQ03_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A2	BIQ03_COF2	BIQ03_A1_H																	Program DAC BIQ03_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A3	BIQ03_COF3	BIQ03_A2_L																	Program DAC BIQ03_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A4	BIQ03_COF4	BIQ03_A2_H																	Program DAC BIQ03_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A5	BIQ03_COF5	BIQ03_B0_L																	Program DAC BIQ03_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W

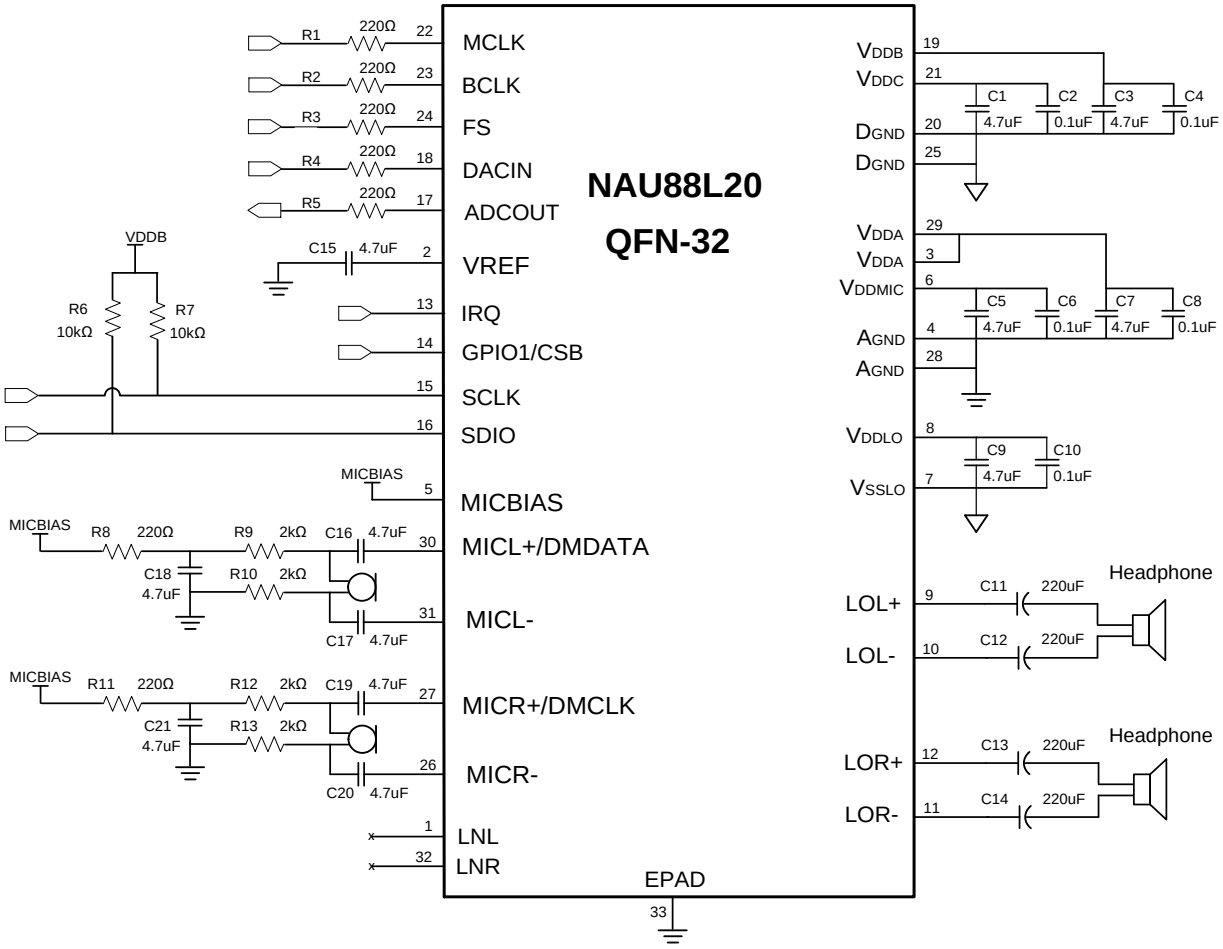
A6	BIQ03_COF6	BIQ03_B0_H																	Program DAC BIQ03_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A7	BIQ03_COF7	BIQ03_B1_L																	Program DAC BIQ03_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A8	BIQ03_COF8	BIQ03_B1_H																	Program DAC BIQ03_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
A9	BIQ03_COF9	BIQ03_B2_L																	Program DAC BIQ03_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
AA	BIQ03_COF10	BIQ03_B2_H																	Program DAC BIQ03_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B1	BIQ13_COF1	BIQ13_A1_L																	Program ADC BIQ13_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B2	BIQ13_COF2	BIQ13_A1_H																	Program ADC BIQ13_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B3	BIQ13_COF3	BIQ13_A2_L																	Program ADC BIQ13_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B4	BIQ13_COF4	BIQ13_A2_H																	Program ADC BIQ13_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B5	BIQ13_COF5	BIQ13_B0_L																	Program ADC BIQ13_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B6	BIQ13_COF6	BIQ13_B0_H																	Program ADC BIQ13_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B7	BIQ13_COF7	BIQ13_B1_L																	Program ADC BIQ13_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B8	BIQ13_COF8	BIQ13_B1_H																	Program ADC BIQ13_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
B9	BIQ13_COF9	BIQ13_B2_L																	Program ADC BIQ13_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
BA	BIQ13_COF10	BIQ13_B2_H																	Program ADC BIQ13_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C1	BIQ04_COF1	BIQ04_A1_L																	Program DAC BIQ04_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C2	BIQ04_COF2	BIQ04_A1_H																	Program DAC BIQ04_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C3	BIQ04_COF3	BIQ04_A2_L																	Program DAC BIQ04_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C4	BIQ04_COF4	BIQ04_A2_H																	Program DAC BIQ04_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C5	BIQ04_COF5	BIQ04_B0_L																	Program DAC BIQ04_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C6	BIQ04_COF6	BIQ04_B0_H																	Program DAC BIQ04_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C7	BIQ04_COF7	BIQ04_B1_L																	Program DAC BIQ04_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C8	BIQ04_COF8	BIQ04_B1_H																	Program DAC BIQ04_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
C9	BIQ04_COF9	BIQ04_B2_L																	Program DAC BIQ04_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W

CA	BIQ04_COF10	BIQ04_B2_H																	Program DAC BIQ04_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D1	BIQ14_COF1	BIQ14_A1_L																	Program ADC BIQ14_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D2	BIQ14_COF2	BIQ14_A1_H																	Program ADC BIQ14_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D3	BIQ14_COF3	BIQ14_A2_L																	Program ADC BIQ14_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D4	BIQ14_COF4	BIQ14_A2_H																	Program ADC BIQ14_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D5	BIQ14_COF5	BIQ14_B0_L																	Program ADC BIQ14_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D6	BIQ14_COF6	BIQ14_B0_H																	Program ADC BIQ14_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D7	BIQ14_COF7	BIQ14_B1_L																	Program ADC BIQ14_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D8	BIQ14_COF8	BIQ14_B1_H																	Program ADC BIQ14_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
D9	BIQ14_COF9	BIQ14_B2_L																	Program ADC BIQ14_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
DA	BIQ14_COF10	BIQ14_B2_H																	Program ADC BIQ14_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E1	BIQ05_COF1	BIQ05_A1_L																	Program DAC BIQ05_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E2	BIQ05_COF2	BIQ05_A1_H																	Program DAC BIQ05_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E3	BIQ05_COF3	BIQ05_A2_L																	Program DAC BIQ05_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E4	BIQ05_COF4	BIQ05_A2_H																	Program DAC BIQ05_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E5	BIQ05_COF5	BIQ05_B0_L																	Program DAC BIQ05_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E6	BIQ05_COF6	BIQ05_B0_H																	Program DAC BIQ05_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E7	BIQ05_COF7	BIQ05_B1_L																	Program DAC BIQ05_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E8	BIQ05_COF8	BIQ05_B1_H																	Program DAC BIQ05_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
E9	BIQ05_COF9	BIQ05_B2_L																	Program DAC BIQ05_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
EA	BIQ05_COF10	BIQ05_B2_H																	Program DAC BIQ05_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F1	BIQ15_COF1	BIQ15_A1_L																	Program ADC BIQ15_A1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F2	BIQ15_COF2	BIQ15_A1_H																	Program ADC BIQ15_A1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F3	BIQ15_COF3	BIQ15_A2_L																	Program ADC BIQ15_A2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W

F4	BIQ15_COF4	BIQ15_A2_H																	Program ADC BIQ15_A2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F5	BIQ15_COF5	BIQ15_B0_L																	Program ADC BIQ15_B0 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F6	BIQ15_COF6	BIQ15_B0_H																	Program ADC BIQ15_B0 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F7	BIQ15_COF7	BIQ15_B1_L																	Program ADC BIQ15_B1 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F8	BIQ15_COF8	BIQ15_B1_H																	Program ADC BIQ15_B1 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
F9	BIQ15_COF9	BIQ15_B2_L																	Program ADC BIQ15_B2 Parameter Bit[15:0]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W
FA	BIQ15_COF10	BIQ15_B2_H																	Program ADC BIQ15_B2 Parameter Bit[18:16]
		DEFAULT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0x0000 R/W

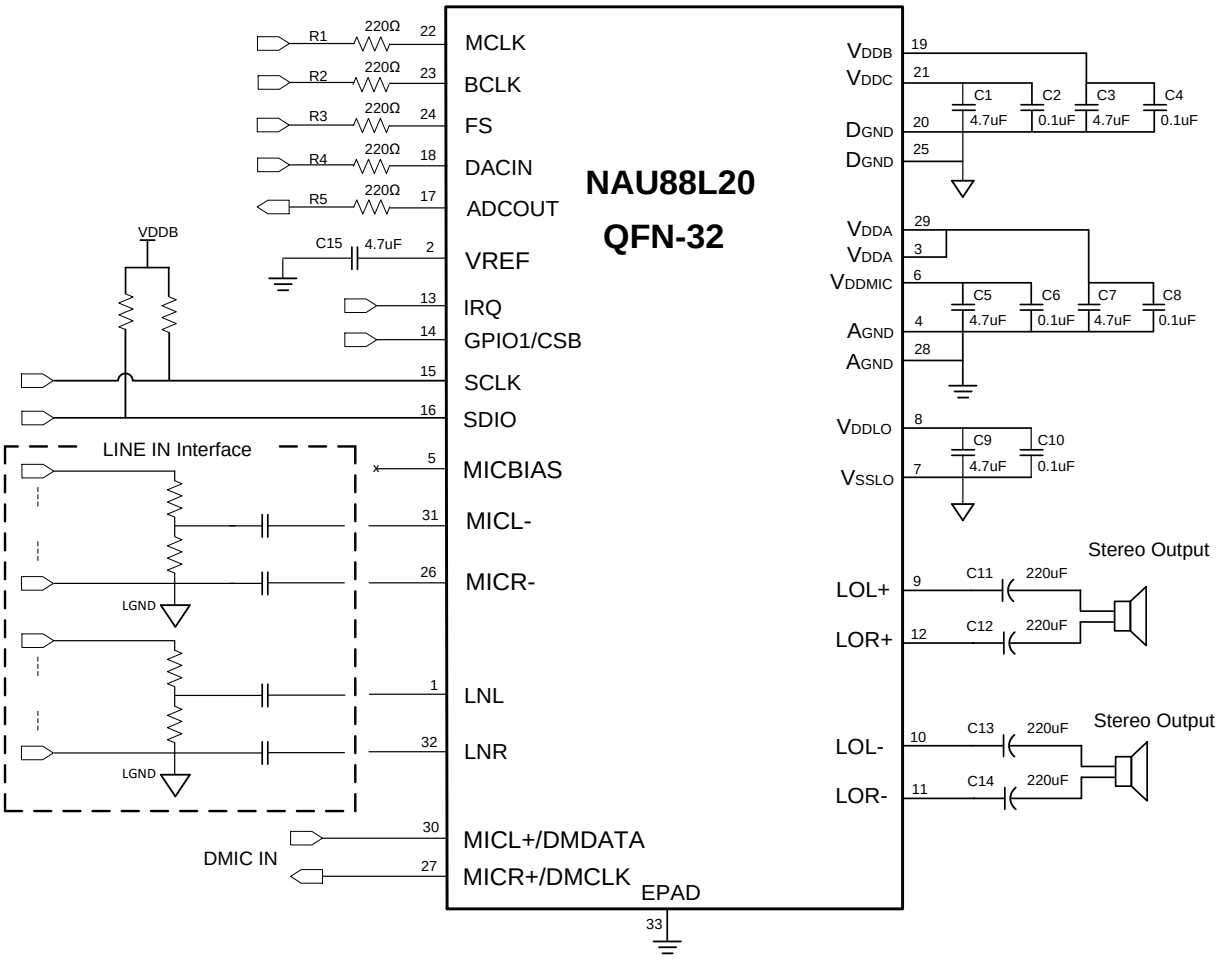
13. Typical Application Diagram

13.1 Typical Application Diagram with Analog Microphone



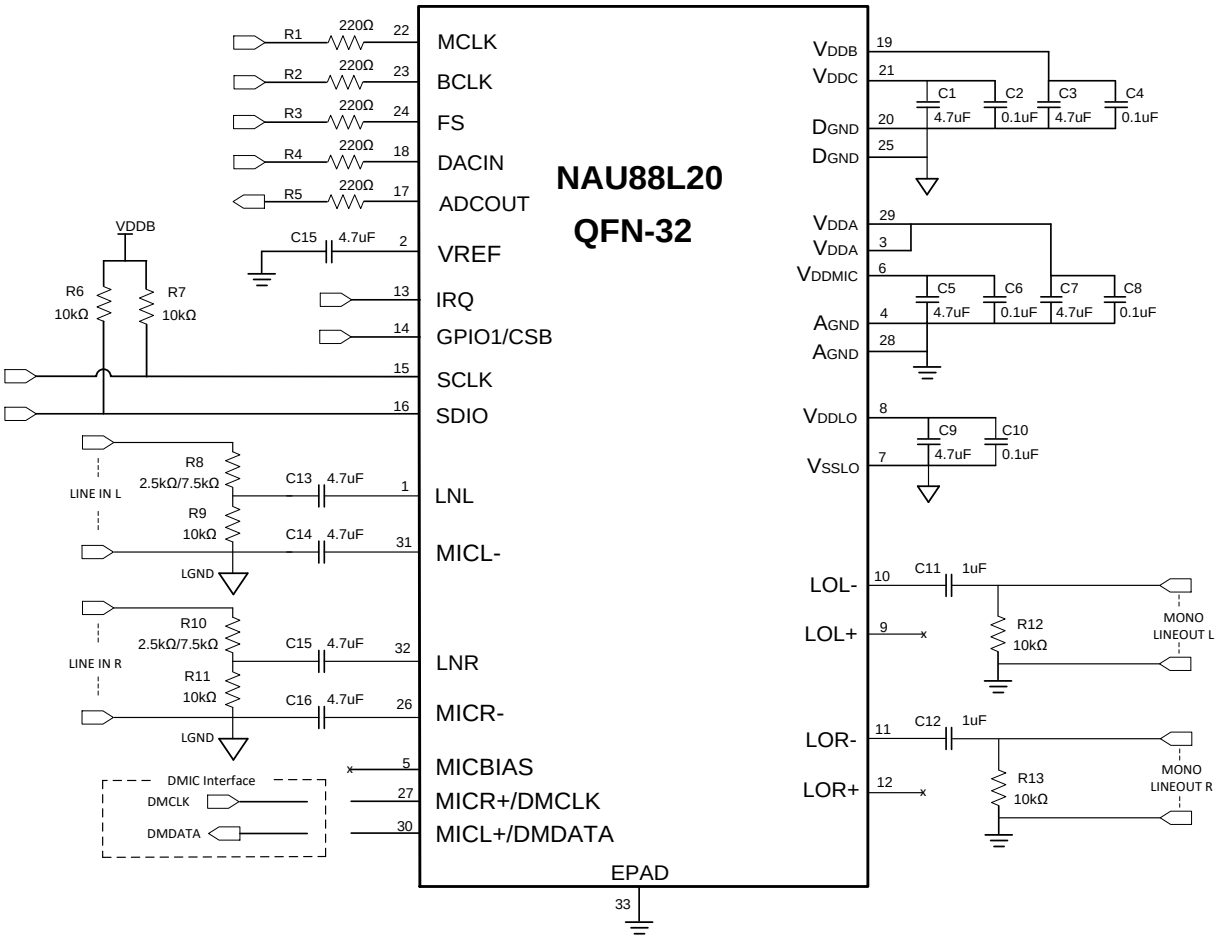
Note: Pin#33 the center pad underneath should be connected to AGND.

13.2 Typical Application Diagram with Digital Microphone



Note: Pin#33 the center pad underneath should be connected to AGND.

13.3 Typical Application Diagram with Line-In and Line-Out

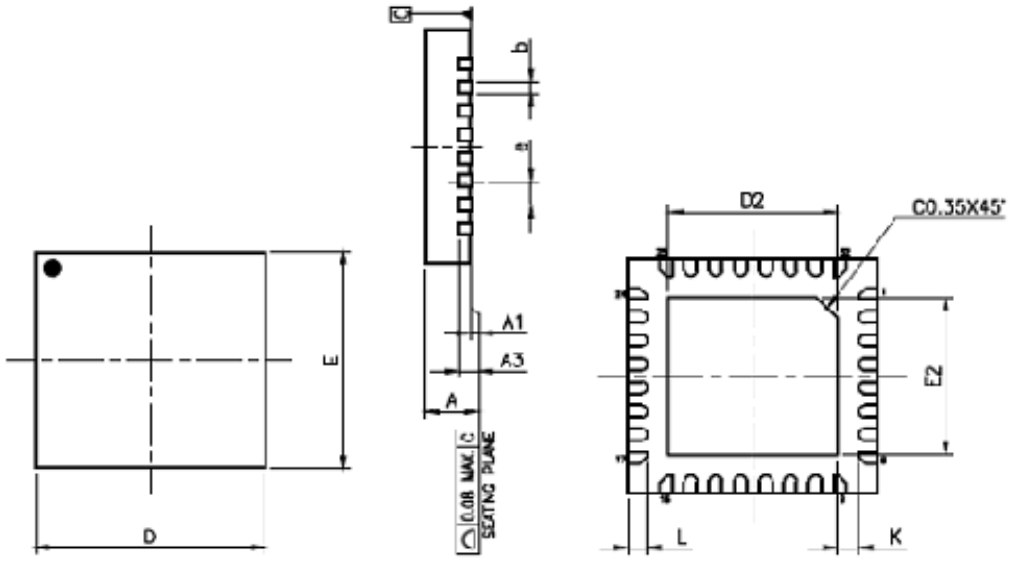


Note:

- Pin#33 the center pad underneath should be connected to AGND.
- For R8 and R10: use 2.5kΩ for max. 1Vrms input, use 7.5kΩ for max. 2Vrms input.

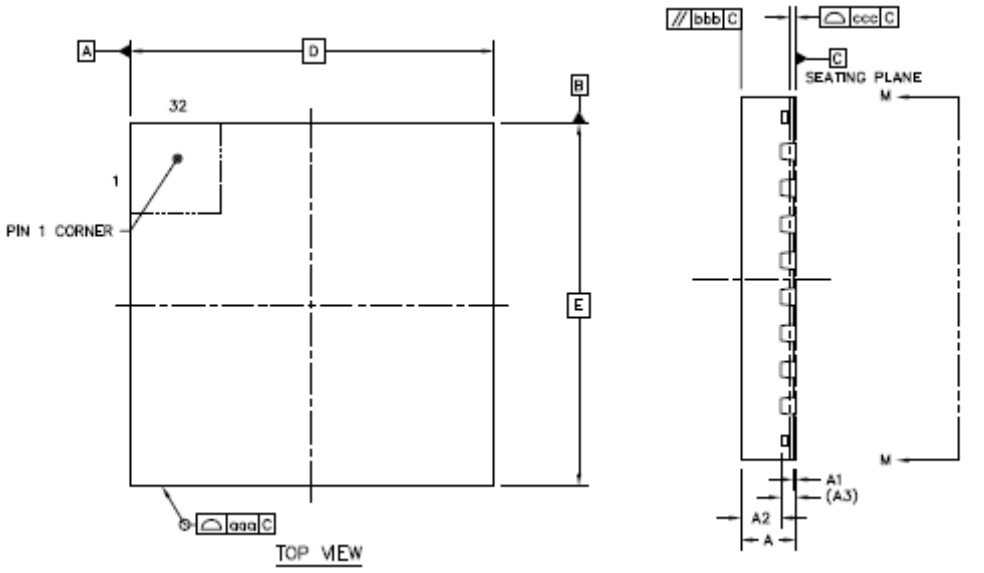
14. Package Information

QFN 32L 4x4 mm^2, Thickness: 0.8mm(Max), Pitch:0.4 mm



SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D		4.00 BSC	
L		4.00 BSC	
e		0.40 BSC	
L	0.25	0.30	0.35
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
K	0.20	—	—

QFN 32L 5x5 mm^2, Thickness: 0.8mm(Max), Pitch:0.5 mm



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	0.57
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		5 BSC	
	Y	E		5 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	3.4	3.5	3.6
	Y	K	3.4	3.5	3.6
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

15. ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU88L20IG	4x4 mm	QFN-32	Green
NAU88L20YG	5x5 mm	QFN-32	Green

NAU88L20 _ _

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

I = QFN-32

Y = QFN-32

16. REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Dec 19, 2022	Initial Release
1.1	Dec 22, 2022	Update Halogen-free, RoHS-compliant and TSCA-compliant description
1.2	Jan 3, 2023	Update 0x2C register description
1.3	Feb 1, 2023	Update format

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All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.