NAU85L40B
Quad Audio ADC with Integrated FLL and Microphone Preamplifier

GENERAL DESCRIPTION

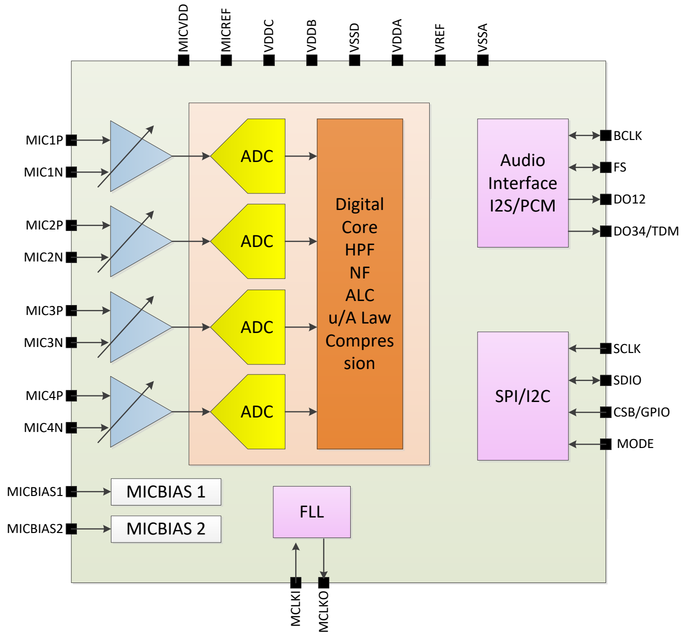
The NAU85L40B is a low power, high quality, 4-channel ADC for microphone array application. The NAU85L40B integrates programmable gain preamplifiers for quad differential microphones, significantly reducing external component requirements. A fractional FLL is available to accurately generate any audio sample rate using any commonly available system clock source from 8KHz through 33MHz. Audio data can be directed to two I2S data out lines or onto a single time division multiplexed (TDM) PCM data output.

The NAU85L40B operates with analog supply voltages from 1.6V ~ 2V, while the digital core can operate down to 1.2V to conserve power. Internal register controls enable flexible power saving modes by powering down sub-sections of the chip under software control. The NAU85L40B is specified for operation from -40°C ~ +85°C, and is available in a QFN-28 package.

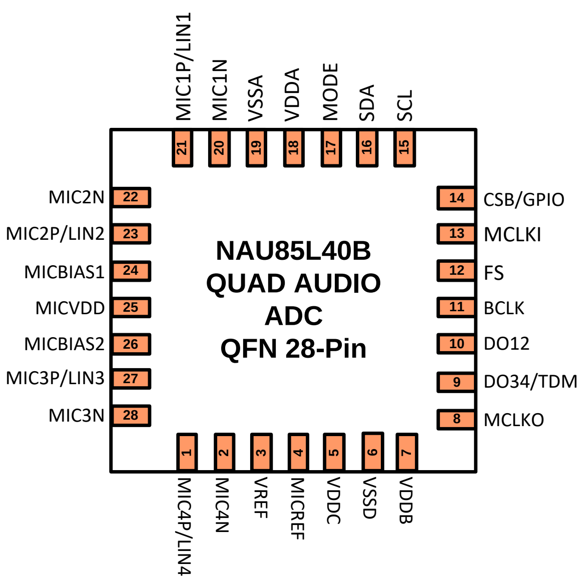
FEATURES

- 101dB SNR (A-weighted) @ 0dB gain, VDDA=1.8V, Fs = 48 kHz, OSR=128x
- 92dB THD+N @ 0dB gain, 0.8Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x
- -124dB Channel Crosstalk @ 0dB gain, 0.9Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x
- Integrated programmable gain microphone amplifier
- On-chip FLL
- I2C Serial control interface with read/write capability
- Supports sample rates from 8 kHz to 96 kHz at 24-bit resolution
- Two separate microphone bias supplies for low noise microphone biasing
- Standard audio data bus interfaces: I2S, Left or Right justified, TDM (4 channel), Two's compliment, MSB first
- 32-bit audio sub frames
- Package: QFN-28
  Package is Halogen-free, RoHS-compliant and TSCA-compliant
- Temperature range: -40 ~ 85°C

Block Diagram



Pin Diagram



Ordering Information

Part Number	Dimension	Package	Package Material
NAU85L40YGB	4 x 4 mm	QFN-28	Green

Table of Contents

Pin Description

Pin #	Name	Type	Functionality
1	MIC4P/LIN4	Analog Input	MICP Input 4 / Line In Input 4
2	MIC4N	Analog Input	MICN Input 4
3	VREF	Reference	Decoupling for Mid-rail Reference Voltage
4	MICREF	Analog Output	Decoupling for MIC Reference Voltage
5	VDDC	Supply	Digital Core Supply
6	VSSD	Supply	Digital Ground
7	VDDB	Supply	Digital Buffer (Input/Output) Supply
8	MCLKO	Digital Output	Output from PLL
9	DO34	Digital Output	Digital Audio ADC Data Output for ADC 3 and 4 or TDM
10	DO12	Digital Output	Digital Audio ADC Data Output for ADC 1 and 2
11	BCLK	Digital I/O	Digital Audio Bit Clock
12	FS	Digital I/O	Digital Audio Frame Sync
13	MCLKI	Digital Input	Master Clock Input
14	CSB/GPIO	Digital Input	3-Wire MPU Chip Select/I2C address LSB
15	SCL	Digital Input	3-Wire MPU Clock Input/I2C Clock (SCL)
16	SDA	Digital I/O	3-Wire MPU Data Input/I2C Data I/O (SDA)
17	MODE	Digital Input	Control Interface Mode Selection Pin (I2C=1, SPI=0)
18	VDDA	Supply	Analog Power Supply
19	VSSA	Supply	Analog Ground
20	MIC1N	Analog Input	MICN Input 1
21	MIC1P/LIN1	Analog Input	MICP Input 1 / Line In Input 1
22	MIC2N	Analog Input	MICN Input 2
23	MIC2P/LIN2	Analog Input	MICP Input 2 / Line In Input 2
24	MICBIAS1	Analog Output	Microphone Bias for Microphone ADC 1 and 2
25	MICVDD	Supply	Microphone Supply
26	MICBIAS2	Analog Output	Microphone Bias for Microphone ADC 3 and 4
27	MIC3P/LIN3	Analog Input	MICP Input 3 / Line In Input 3
28	MIC3N	Analog Input	MICN Input 3

Electrical Characteristics

Conditions: VDDA = VDDC=1.8V, VDDB = 3.3V, MICVDD=3.3V, MCLK = 12.88MHz, T_A = +25°C, 1 kHz signal, Fs = 48 kHz, 24-bit audio data, with differential inputs unless otherwise stated.

Symbol	Parameter	Conditions	Typical	Limit	Units (Limit)
Isd	Shutdown Current	$V_{DD}A$	0.5	1	µA
		$V_{DD}A$ When $V_{DD}C$=1.2V	16.7		
		$V_{DD}B$	0.2	1	
		$V_{DD}C$	2	10	
		$V_{DD}MIC$	0.5	1	
ADC					
THD+N	ADC Total Harmonic Distortion + Noise	MIC Input, MIC_GAIN = 6dB, f=1KHz, Fs = 16KHz, OSR=128X	-92	-80	dB
		Reference= @ 0dB gain, 0.8Vrms in, VDDA=1.8V, Fs=48 kHz, OSR=128x	-92		dB
SNR	Signal to Noise Ratio	Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 0dB,fs = 8KHz, Mono Differential Input	101		dB
		Reference = VOUT(0dBFS), A-Weighted, MIC Input, MIC Gain = 6dB,fs = 8KHz, Mono Differential Input	100		dB
		Reference = VOUT(0dBFS), A-Weighted, Quad Input, Gain = 12dB,fs = 16KHz	97		dB
		Reference= MIC Gain= 0dB gain, (A-weighted) VDDA=1.8V, Fs = 48 kHz, OSR=128x	101		dB
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mVP_P applied to AVDD, f_{RIPPLE} = 217Hz, Input Referred, MIC_GAIN = 0dB Differential Input	65		dB
Xtalk	ADC channel cross talk	MIC Input, MIC_GAIN = 0dB, VIN = 0.8Vrms, f=1KHz, Fs = 48KHz , Channel 1(3) to Channel 2 (4)	-124		dB
FS_{ADC}	ADC Full Scale Differential Input Level (see Note 1)	V_{REF} = 1.6V (Reg 0x65[9:8] = b'10) DGAIN = 1.25dB (Reg 0x40/0x41/0x42/0x43) FEPGA = 0dB (Reg 0x6B/0x6C) VDDA = 1.8V	1		V_{RMS}

	ADC Full Scale Single-end Input Level (see Note 1)	V_{REF} = 1.6V (Reg 0x65[9:8] = b'10) DGAIN = 1.25dB (Reg 0x40/0x41/0x42/0x43) FEPGA = 6dB (Reg 0x6B/0x6C) VDDA = 1.8V	0.5		V_{RMS}
MICBIAS					
V_{BIAS}	Output Voltage	Programmable 2.1V to 2.8V in 0.1V Steps	2.5		V
I_{OUT}	Output Current			4	mA
e_{OS}	Output Noise	A-weighted 20Hz-20kHz	-115		dBV

Notes

1. Full Scale input level is relative to the magnitude of VDDA and can be calculated as FS = $1V_{rms}$*VDDA/1.8.
2. Distortion is measured in the standard way as the combined quantity of distortion products plus noise. The signal level for distortion measurements is at 3dB below full scale, unless otherwise noted.
3. Unused analog input pins should be left as no-connection.
4. Unused digital input pins should be tied to ground.

Digital I/O

Parameter	Symbol	Comments/Conditions		Min	Max	Units
Input LOW level	V_{IL}	VDDB = 1.8V			0.33 * VDDB	V
		VDDB = 3.3V			0.37 * VDDB	
Input HIGH level	V_{IH}	VDDB = 1.8V		0.67 * VDDB		V
		VDDB = 3.3V		0.63 * VDDB		
Output HIGH level	V_{OH}	I_{Load} = 1mA	VDDB = 1.8V	0.9 * VDDB		V
			VDDB = 3.3V	0.95 * VDDB		
Output LOW level	V_{OL}	I_{Load} = 1mA	VDDB = 1.8V		0.1 * VDDB	V
			VDDB = 3.3V		0.05 * VDDB	

Recommended Operating Conditions

Condition	Symbol	Min	Typical	Max	Units
Digital Supply Range with sample rate > 48 kHz or FLL enabled	VDDC	1.62	1.8	1.98	V
Digital Supply Range with sample rate <= 48kHz and FLL disabled	VDDC	1.2	1.8	1.98	V
Digital I/O Supply Range	VDDB	1.62	1.8	3.6	V

Analog Supply Range	VDDA	1.62	1.8	1.98	V
Microphone Bias Supply Voltage	VDDMIC	2.5	4.2	5.5	V
Temperature Range	T_A	-40		+85	°C

CAUTION: Below conditions needed to be followed for regular operation: VDDB > VDDC – 0.6V.

Absolute Maximum Ratings

Parameter	Min	Max	Units
Digital Supply Range (VDDC)	-0.3	2.2	V
Digital I/O Supply Range (VDDB)	-0.3	6.0	V
Analog Supply Range (VDDA)	-0.3	2.2	V
Microphone Bias Supply Voltage (MICVDD)	-0.3	6.0	V
Voltage Input Digital Range	VSSD - 0.3	VDDB + 0.3	V
Voltage Input Analog Range	VSSA - 0.3	VDDA + 0.3	V
Junction Temperature, T_J	-40	+150	°C
Storage Temperature	-65	+150	°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods. Exposure to such conditions may adversely influence product reliability and result in failures not covered by warranty.

CAUTION: The following condition need to be followed for maximum ratings: VDDB > VDDC – 0.6V.

1 General Description

The NAU85L40B is a low power, high quality, 4-channel ADC for microphone array applications. There are eight analog inputs with individual input PGA gain stages and are passed to the ADC path for signal processing. A low noise microphone bias circuit supplies a programmable voltage reference for one or more electret microphones on two buffered MICBIAS outputs that are available to separately supply microphones associated with channels 1 & 2 and channels 3 & 4. The digital audio data from the ADC's can be processed by a Volume Control, High Pass filter, and ALC before it is passed on to the serial I2S or TDM PCM interface. This digital serial output data can be available in two separate dual channel formats on ADCOUT12 for channel 1 & 2 and ADCOUT34 for channel 3 & 4. The 4-channel serial digital audio can also be combined into one serial bit stream on ADCOUT34 in TDM mode. The device clock can be locked to an external clock reference or generated internally by the on-chip FLL. The registers that control the NAU85L40B can be programmed through standard I2C or SPI interface.

2 Analog Inputs

NAU85L40B has four low noise, high common mode rejection ratio analog microphone differential inputs – MIC1/MIC1P together are MIC.1, MIC2N/MIC2P together are MIC.2, MIC3N/MIC3P together are MIC.3, MIC4N/MIC4P together are MIC.4. Each of these microphone inputs are followed by a -1dB to 36dB PGA gain stage with a fixed 12kOhm input impedance.

All inputs are maintained at a DC bias at approximately 1/2 of the VDDA supply voltage. Connections to these inputs should be AC-coupled by means of DC blocking capacitors suitable for the device application.

The differential microphone input structure is essential in noisy digital systems where amplification of low-amplitude analog signals is necessary such as in portable digital media devices and cell phones. Differential inputs are also very useful to reduce ground noise in systems in which there are ground voltage differences between different chips and components. When properly implemented, the differential input architecture offers an improved power-supply rejection ratio (PSRR) and higher ground noise immunity.

A detailed diagram of the input PGA connections and associated registers is shown in Figure 1. The PGA inputs can also be disconnected from the amplifier for applications where the inputs are shared with other devices. In addition, there is a pre-charge circuit that can speed up charging the external coupling capacitor set with **FEPGA2.ACDC_CTRL REG0X6A[15:8]**. The PGA gain can be set from -1dB to 36dB in 1dB steps and the embedded antialiasing filter also has a single bit adjustment to shift the cut-off frequency.

A detailed register description is available in registers **FEPGA1 REG0X69** to **FEPGA4 REG0X6C**.

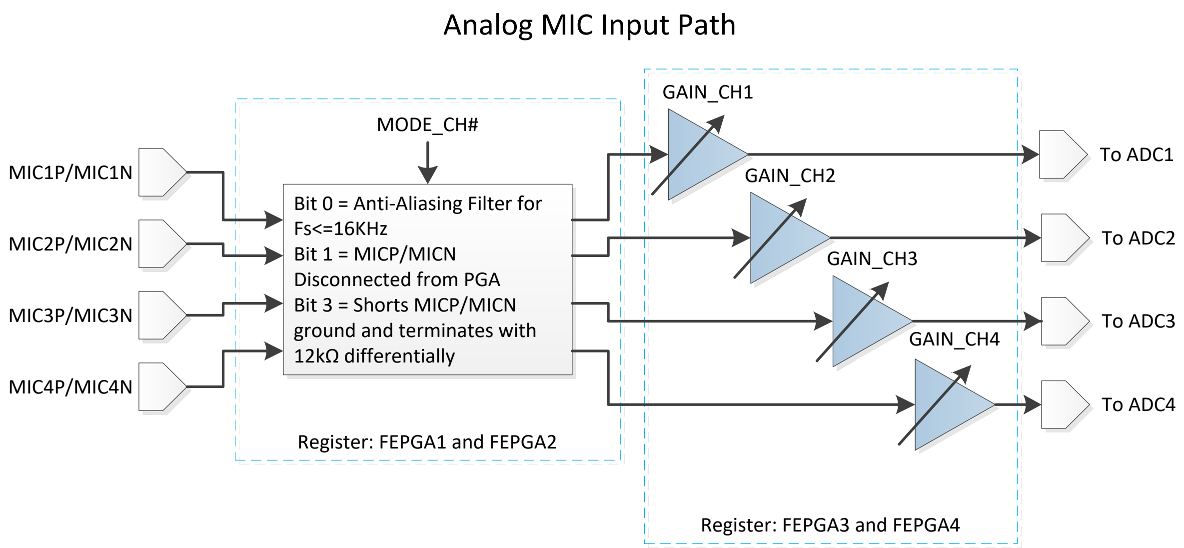


Figure 1: Analog Input Structure

2.1 ADC and Digital Signal Processing

The NAU85L40B has four independent high quality ADCs. These are high performance 24-bit sigma-delta converters that are suitable for a very wide range of applications. All digital processing is with 24-bit precision minimizing processing artifacts and maximizing the audio dynamic range supported by the NAU84L04.

The ADCs are supported by a wide range mixed-mode Automatic Level Control (ALC), a high pass filter, and a notch filter. All of which are optional and programmable. The high pass filter function is intended for DC-blocking or low frequency noise reduction, such as to reduce unwanted ambient noise or "wind noise" on a microphone input. The notch filter may be programmed to greatly reduce a specific frequency band or frequency, such as a 50Hz, 60Hz, or 217Hz unwanted noise. The 4-channel ADC TDM interface also provides for flexible routing options.

2.2 ADC Digital Block

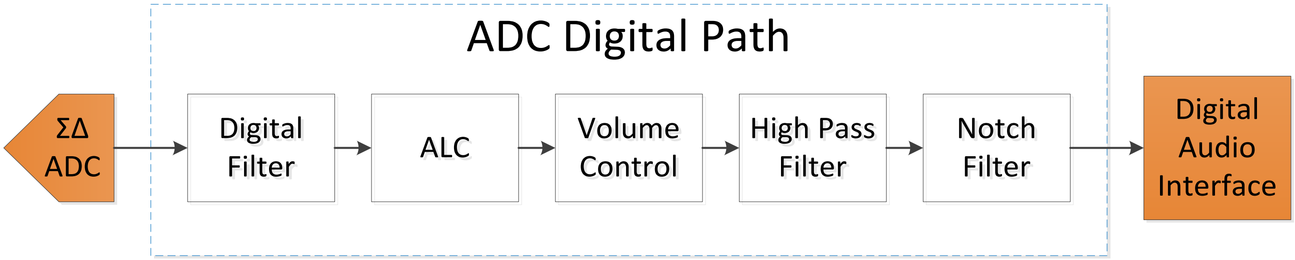


Figure 2: ADC Digital Path

The ADC digital block performs 24-bit analog-to-digital conversion and signal processing, making available a high quality audio sample stream the audio path digital interface. This block consists of a sigma-delta modulator, digital decimator/ filter, ALC, volume control, high pass filter, and a notch filter.

In order to enable the ADCs, POWER_MANAGEMENT.ADC1_EN REG0x01[0] through POWER_MANAGEMENT.ADC4_EN REG0x01[3] must all be set to 1. The audio sample rate of the ADC is set by CLOCK_SRC.CLK_ADC_SRC REG0x03[7:6], which is derived from the MCLK. (See Section CLOCKING AND SAMPLE RATES).

The polarity of either ADC output signal can be changed independently on either ADC logic output which can be sometimes useful in management of the audio phase. This feature can help minimize any audio processing that may be otherwise required as the data are passed to other stages in the system. The ADC coding scheme is in twos complement format and the full-scale input level is proportional to VDDA. For example, with a 1.8V supply voltage, the full-scale level is 1.0VRMS.

2.2.1 Input Limiter / Automatic Level Control (ALC)

The ADC digital path of the NAU85L40B is supported by the digital Automatic Level Control (ALC) function. This can be used to automatically manage the gain to optimize the signal level at the output of the ADC by automatically amplifying input signals that are too small or decreasing the amplitude of the signals that are too loud.

The ALC monitors the output of the ADC, measured after the digital decimator. The ADC output is fed into a peak detector, which updates the measured peak value whenever the absolute value of the input signal is higher than the current measured peak. The measured peak gradually decays to zero unless a new peak is detected, allowing for an accurate measurement of the signal envelope. The peak value is then used by a logic algorithm to determine whether the gain should be increased, decreased, or remain the same.

In normal mode, when sudden peaks occur above the desired gain settings, the ALC reduces volume at a register determined rate and step size. This continues until the output level of the ADC is again at the desired target level. If the input signal suddenly becomes quiet, the ALC increases volume at a register determined rate and step size until the output level from the ADC reaches the target level. If the input gain stays within the target level, the ALC will remain in a steady state.

In addition to the normal operation mode, the ALC may be operated in a special limiter mode that functions similarly to the normal mode but with faster attack times. This mode is primarily used to quickly ramp down signals that are too loud.

2.2.1.1 ALC Peak Limiter Function

Both normal and limiter mode include a peak limiter function. This implements an emergency gain reduction when the ADC output level exceeds a set gain value. When the ADC output exceeds 87.5% of full scale, the ALC block ramps down the gain at the maximum ALC Attack Time rate. This is regardless of the mode and attack rate settings. This continues until the ADC output level has been reduced to below the emergency limit threshold. This action limits ADC clipping if there is a sudden increase in the input signal level.

2.2.1.2 ALC Parameter Definitions

ALC Maximum Gain (ALCMAX): This sets the maximum allowed gain during normal mode ALC operation. In the Limiter mode of ALC operation, the ALCMXGAIN value is not used, instead, the maximum gain allowed is set equal to the pre-existing gain value that was in effect at the moment in time that the Limiter mode is enabled. See **ALC_CONTROL_2 REG0X21** for details.

ALC Minimum Gain (ALCMIN): This sets the minimum allowed gain during all modes of ALC operation. This is useful to keep the ALC operating range close to the desired range for a given application scenario. See **ALC_CONTROL_2 REG0X21** for details.

ALC Target Value (ALCLVL): Determines the value used by the ALC logic decisions comparing this fixed value with the output of the ADC. This value is expressed as a fraction of Full Scale (FS) output from the ADC. Depending on the logic conditions, either the output value used in the comparison may be the instantaneous value of the ADC, or a time weighted average of the ADC peak output level. See **ALC_CONTROL_2 REG0X21** for details.

ALC Attack Time (ALCATK): Attack time refers to how quickly a system responds to an increasing volume level that is greater than some defined threshold. Typically, attack time is much faster than decay time. In the NAU85L40B, when the absolute value of the ADC output exceeds the ALC Target Value, the gain will be reduced at a step size and rate determined by this parameter. When the peak ADC output is at least 1.5dB lower than the ALC Target Value, the stepped gain reduction will halt. See **ALC_CONTROL_3 REG0X22** for details.

ALC Decay Time (ALCDCY): Decay time refers to how quickly a system responds to a decreasing volume level. Typically, decay time is much slower than attack time. When the ADC output level is below the ALC Target value by at least 1.5dB, the gain will increase at a rate determined by this parameter.   In Limiter mode, the time constants are faster than in ALC mode. See **ALC_CONTROL_3 REG0X22** for details.

ALC Hold Time (ALCHLD): Hold time refers to the duration of time when no action is taken. This is typically to avoid undesirable sounds that can happen when an ALC responds too quickly to a changing input signal. In the NAU85L40B, the hold time value is the duration of time that the ADC output peak value must be less than the target value before there is an actual gain increase. See **ALC_CONTROL_2 REG0X21** for details.

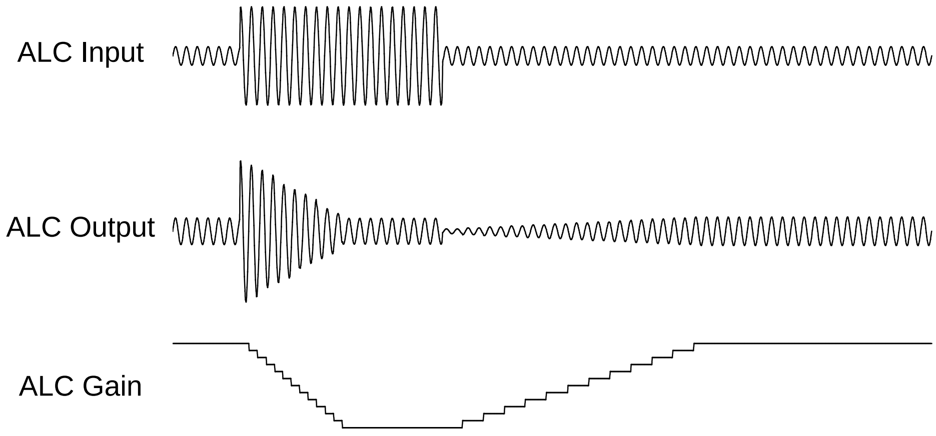


Figure 3: ALC Operation

2.2.1.3 ALC Normal Mode Example Using ALC Hold Time Feature

Input signals with different characteristics (e.g., voice vs. music) may require different settings for this parameter for optimum performance. Increasing the ALC hold time prevents the ALC from reacting too quickly to brief periods of silence such as those that may appear in music recordings. Having a shorter hold time may be useful in voice applications where a faster reaction time helps to adjust the volume setting for speakers with different volumes. The waveform below shows the operation of the **ALC_CONTROL_2.ALCHLD REG0X21[7:4]** parameter.

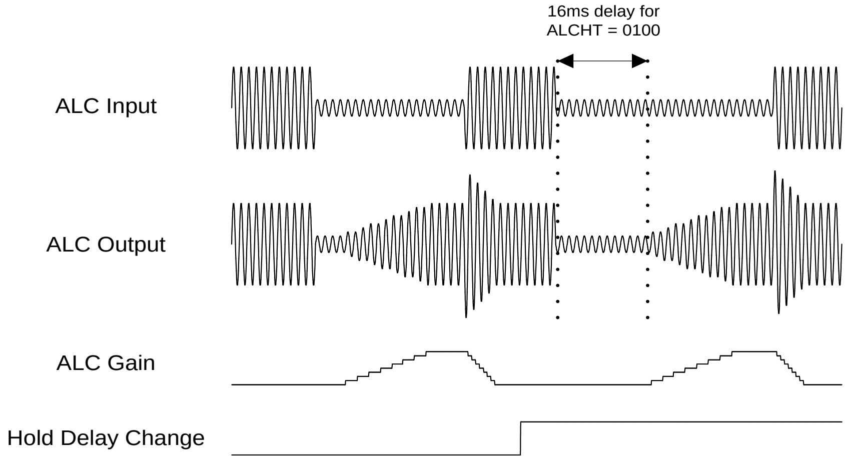


Figure 4: ALC using Hold time

2.2.1.4 Noise Gate (Normal Mode Only)

A noise gate threshold prevents ALC amplification of noise when there is no input signal or no signal above an expected background noise level. The noise gate is enabled by setting ALC_CONTROL_1.ALC_NGEN REG0X20[4] and the threshold level is set by ALC_CONTROL_1.ALC_NGTH REG0X20[3:0]. When there is no signal or a very quiet signal (pause) composed mostly of noise, the ALC holds the gain constant instead of amplifying the signal towards the target threshold. The NAU85L40B accomplishes this by comparing the input signal level against the noise gate threshold. The noise gate only operates in conjunction with the ALC and only in Normal mode.

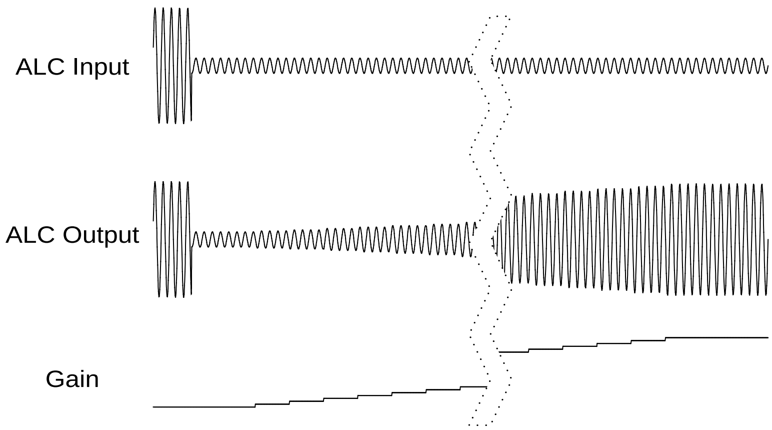


Figure 5: ALC without Noise gate

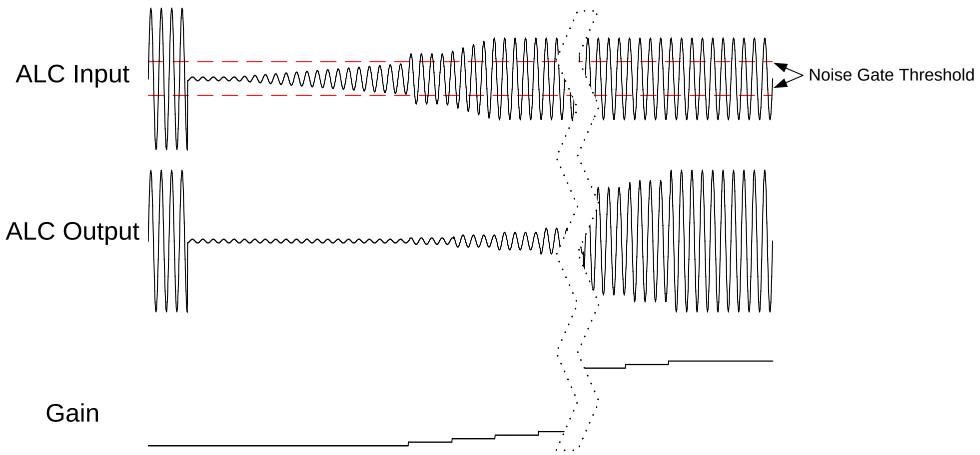
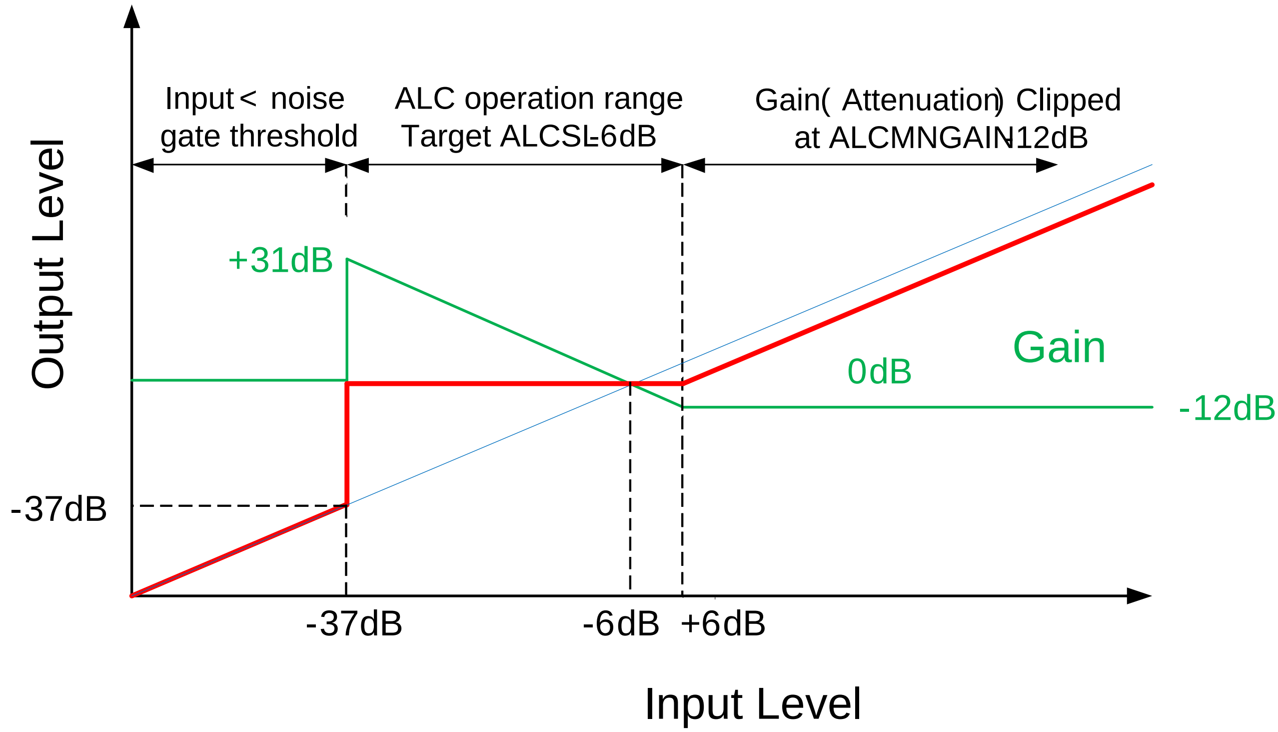


Figure 6: ALC with noise gate

2.2.1.5 ALC Example with ALC Min/Max Limits and Noise Gate Operation

The drawing below shows the effects of ALC operation over the full scale signal range. The drawing is color coded as follows:

Blue Original Input signal (linear line from zero to maximum)
Green PGA gain value over time (inverse to signal in target range)
Red Output signal (held to a constant value in target range)



Register	Bits	Name	Value	Description
22	12-15	ALCCH(1-4)E	1111	ALC enabled all channels
21	12-14	ALCMAXGAIN	111	Max ALC gain@ 35.25dB
21	8-10	ALCMINGAIN	000	Min ALC gain@-12dB
21	0-3	ALCLVL	1011	Target ALC gain@-6 dBFS
20	4	NGEN	1	Noise gate enabled
20	0-3	NGTH	0100	Noise gate@-37dB

Figure 7: ALC Response Envelope

2.2.2 ADC Digital Volume Control

The effective output audio volume of each ADC can be changed from +36dB through -128dB in 0.125dB steps using the digital volume control feature. Included in the volume control is a “digital mute” value that will completely mute the signal output of the ADC.

In addition, the ADC has an analog gain control, which can be set from -1dB to 36dB.

Registers DIGITAL_GAIN_CH1 REG0X40 through DIGITAL_GAIN_CH4 REG0X43 control the digital gain of each channel. These registers can also select the ADC source of each output channel.

2.2.3 ADC Programmable High Pass Filter

A high pass filter in the digital output path optionally supports each ADC. The High Pass filter can be enabled by setting HPF_FILTER_CH12.HPF_EN_CH1 REG0X38[4], HPF_FILTER_CH12.HPF_EN_CH2 REG0X38[12], HPF_FILTER_CH34.HPF_EN_CH3 REG0X39[4], and HPF_FILTER_CH34.HPF_EN_CH4 REG0X39[12].

The high pass filter has two different operating modes. In the audio mode, the filter is a simple first order DC blocking filter, with a cut-off frequency of 3.7Hz. In the application specific mode, the filter is a second order audio frequency filter, with a programmable cut-off frequency. The cutoff frequency of the high pass filter is scaled depending on the sampling frequency indicated to the system by the setting in register ADC_SAMPLE_RATE.SMPL_RATE REG0X3A[7:5].

The following table provides the exact cutoff frequencies with different sample rates. These cutoff frequencies can be selected by setting HPF_FILTER_CH12.HPF_CUT_CH1 REG0X38[2:0], HPF_FILTER_CH12.HPF_CUT_CH2 REG0X38[10:8], HPF_FILTER_CH34.HPF_CUT_CH3 REG0X39[2:0], and HPF_FILTER_CH34.HPF_CUT_CH4 REG0X39[10:8].

HPF_CUT	SMPL_RATE REG0X3A[7:5] in kHz (FS)								
	101 or 100			011 or 010			001 or 000		
	8	11.025	12	16	22.05	24	32	44.1	48
000	82	113	122	82	113	122	82	113	122
001	102	141	153	102	141	153	102	141	153
010	131	180	156	131	180	156	131	180	156
011	163	225	245	163	225	245	163	225	245
100	204	281	306	204	281	306	204	281	306
101	261	360	392	261	360	392	261	360	392
110	327	450	490	327	450	490	327	450	490
111	408	563	612	408	563	612	408	563	612

Table 1: High Pass Filter Cut-off Frequencies in Hz (with HPF_AM = 1)

2.2.4 Programmable Notch Filter

A notch filter in the digital output path optionally supports each ADC. The notch filter is used to stop a very narrow band of frequencies around a center frequency. This function can be enabled by setting NFEN in NOTCH_FIL1_CH1.NFEN REG0X30[14] to NOTCH_FIL1_CH4.NFEN REG0X36[14]. The center frequency is programmed by setting NFA1 of registers NOTCH_FIL1_CH1.NFA1 REG0X30[13:0] to NOTCH_FIL1_CH4.NFA1 REG0X36[13:0] with two's compliment coefficient values calculated using Table 2 as shown below.

It is important to note that the register update bits are write-only bits. The update bit function is important so that all filter coefficients actively being used are changed simultaneously; even though the register values must be written sequentially. When there is a write operation to any of the filter coefficient settings, but the update bit is not set (value = 0), the value is stored as pending a future update, but does not go into effect. When there is a write operation to any coefficient register, and the update bit is set (value = 1), then the new value in the register being written is immediately put into effect, and any other pending coefficient value is put into effect at the same time.

A_0	A_1	Notation	Register Value (DEC)
$\dfrac{1-\tan\frac{2\pi f_b}{2f_s}}{1+\tan\frac{2\pi f_b}{2f_s}}$	$-(1+A_0) \times \cos\frac{2\pi f_c}{f_s}$	f_c = center frequency (Hz) f_b = -3dB bandwidth (Hz) f_s = sample frequency (Hz)	NFCA0 = $-A_0 \times 2^{13}$ NFCA1 = $-A_1 \times 2^{12}$ Note: Values are rounded to the nearest whole number and converted to 2's complement

Table 2: Equations to calculate notch filter coefficients

2.3 Audio Data Companding

Companding is used in digital communication systems to optimize signal-to-noise ratios with reduced data bit rates, using non-linear algorithms. The NAU85L40B supports the two main telecommunications companding standards: A-law and µ-law. The A-law algorithm is primarily used in European communication systems and the µ-law algorithm is primarily used by North America, Japan, and Australia.

Companding converts 13 bits (µ-law) or 12 bits (A-law) to 8 bits using non-linear quantization. The companded signal is an 8bit word containing sign (1-bit), exponent (3-bits) and mantissa (4-bits)

Following are the data compression equations set in the ITU-T G.711 standard and implemented in the NAU85L40B.

2.3.1 µ-law

$$F(x) = \frac{\ln(1 + \mu \times |x|)}{\ln(1 + \mu)}, \qquad -1 < x < 1$$

$$\mu = 255$$

2.3.2 A-law

$$F(x) = \frac{A \times |x|}{(1 + \ln(A))}, \qquad x \le \frac{1}{A}$$

$$F(x) = \frac{(1 + \ln(A \times |x|)}{(1 + \ln(A))}, \qquad \frac{1}{A} \le x \le 1$$

$$A = 87.6$$

When companding is enabled, the PCM interface must be set to an 8-bit word length by setting PCM_CTRL0.CMB8 REG0X10[10]. When in 8-bit mode, the Register word length controls in PCM_CTRL0.WLEN REG0X10[3:2] are ignored.

2.4 Digital Interfaces

Command and control of the device is accomplished using a 2-wire/3-wire serial control interface. This simple, but highly flexible, interface is compatible with many commonly used command and control serial data protocols and host drivers. See CONTROL INTERFACES for more detail.

Digital audio input/output data streams are transferred to and from the device separately for command and control. The digital audio data interface supports either I2S or PCM audio data protocols, and is compatible with commonly used industry standard devices that follow either of these two serial data formats. See DIGITAL AUDIO INTERFACE for more detail.

3 Power Supply

The NAU85L40B has been designed to operate reliably using a wide range of power supply conditions and power-on/power-off sequences. However, because of existence of ESD protection diodes between the supplies, that will have impact on the application of the supplies. Because of these diodes, the following conditions need to be met:

VDDB > VDDC – 0.6V.

3.1 Power on and off reset

The NAU85L40B includes a power on and off reset circuit on chip. The circuit resets the internal logic control at VDDC and VDDA supply power up and this reset function is automatically generated internally when power supplies are too low for reliable operation. The reset threshold is approximately 0.55Vdc and 1.0Vdc for VDDC and VDDA, respectively. It should be noted that these values are much lower than the required voltage for normal operation of the chip.

The reset is held on while the power levels for both VDDC and VDDA are below their respective thresholds. Once the power levels rise above their thresholds, the reset is released. Once the reset is released, the registers are ready to be written to. It is also important to note that all the registers should be kept in their reset state for at least 6µs.

An additional internal RC filter based circuit is added which helps the circuit respond for fast ramp rates (~10µs) and generate the desired reset period width (~10µs at typical corner). This filter is also used to eliminate supply glitches which can generate a false reset condition, typically 50ns.

For reliable operation, it is recommended to write to register **SW_RESET REG0X00** upon power up. This will reset all registers to the known default state.

Note that when VDDA and/or VDDC are below the power on reset threshold, then the digital IO pins will go into a tri-state condition.

Application Notes:

- VDDA ramp up time for a guaranteed power on reset needs to be less than 50msec. The VDDA ramp down time for a guaranteed power off reset needs to be less than 125msec. If the ramp down rate is too slow (no pull down), then we can enable the minimum VREF impedance by **VMID_CTRL.VMIDSEL REG0X66[5:4]=11** with **VMID_CTRL.VMIDEN REG0X66[6]=1**, before shutdown in order to discharge VDDA quickly.

3.2 Reference Voltage Generation

The NAU85L40B includes a mid-supply reference circuit that is decoupled to VSS through the VREF pin by means of a bypass capacitor. The VREF voltage is used as the reference for the majority of the circuits inside NAU85L40B. Therefore, the bypass capacitor needs to be large in order to achieve good power supply rejection at low frequencies. Typically, a 4.7uF capacitor can be used. However, a larger value can be chosen but it will increase the rise time of VREF and therefore it will delay the valid line output signal. However, a pre-charge circuit can pre-charge the capacitor close to VDDA/2 at power up in order to reduce the rise time for fast line out availability. This bypass capacitor should also be low leakage due to the high impedance nature of the VREF pin

The VREF voltage can be enabled by setting **VMID_CTRL.VMIDEN REG0X60[6]**. Once VREF has been enabled, the voltage will quickly ramp up due to the pre-charge circuit. The pre-charge circuit can then be disabled in order to save power or to prevent it from adjusting the VREF voltage when the supply varies. This can be done by setting **REFERENCE.PDVMDFST REG0X68[13]** to 1. Once the VREF voltage has settled to VDDA/2, the output impedance on the VREF pin is determined by setting the bits **VMID_CTRL.VMIDSEL REG0X60[5:4]**. The output impedance is set as per the following table.

VMIDSEL REG0X60[5:4]	VREF Resistor Selection	VREF Impedance
00	Open, no resistor selected	Open, no impedance installed
01	50kOhm	25kOhm
10	250kOhm	125kOhm
11	5kOhm	2.5kOhm

Table 3: V_{REF} Impedance

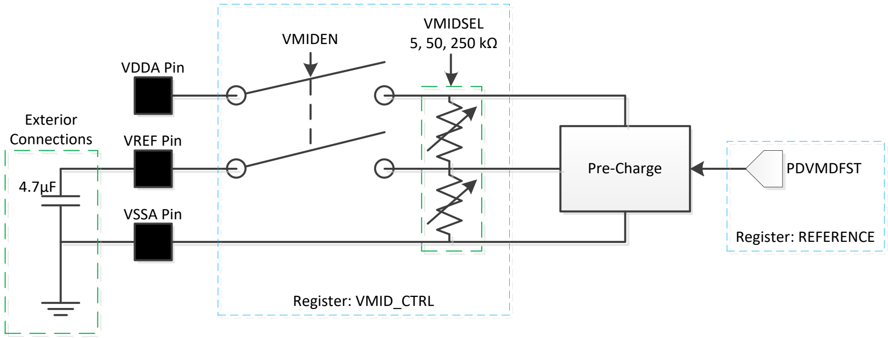


Figure 8: V_{REF} Circuitry

3.3 Microphone Bias Generation

The NAU85L40B provides two microphone bias pins which can be used in various stereo applications. The microphone bias can be used to power electret microphones. In order to ensure safe operation of the device, it is recommended that the microphones do not draw more than 4mA of current from each MICBIAS pin. Register MIC_BIAS REG0X67 provides the control for powering up the MICBIAS circuitry. It should be noted that the two MICBIAS outputs both have the same voltage level.

4 Clocking and Sample Rates

The internal clocks for the NAU85L40B are derived from a common internal clock source, MCLK. This clock is the reference for the ADCs and DSP core functions, digital audio interface and other internal functions.

MCLK can be derived directly from MCLKI pin or may be generated from a Frequency Locked Loop (FLL) using MCLKI, BCLK or FS as a reference. The FLL provides additional flexibility for a wide range of MCLK frequencies and can be used to generate a free-running clock in the absence of an external reference source. See FREQUENCY LOCKED LOOP (FLL)

for further details.

It should be noted that the internal clock frequency MCLK must be running at 256*Fs (Fs = sample rate in Hz) in order to achieve the best performance. For example, when targeting 48 kHz sample rate audio, the MCLK must be set to 256*48k = 12.288MHz. When the input clock MCLKI is higher than this speed, CLOCK_SRC.MCLK_SRC REG0X03[4:0] provides flexible division selection to meet the requirement.

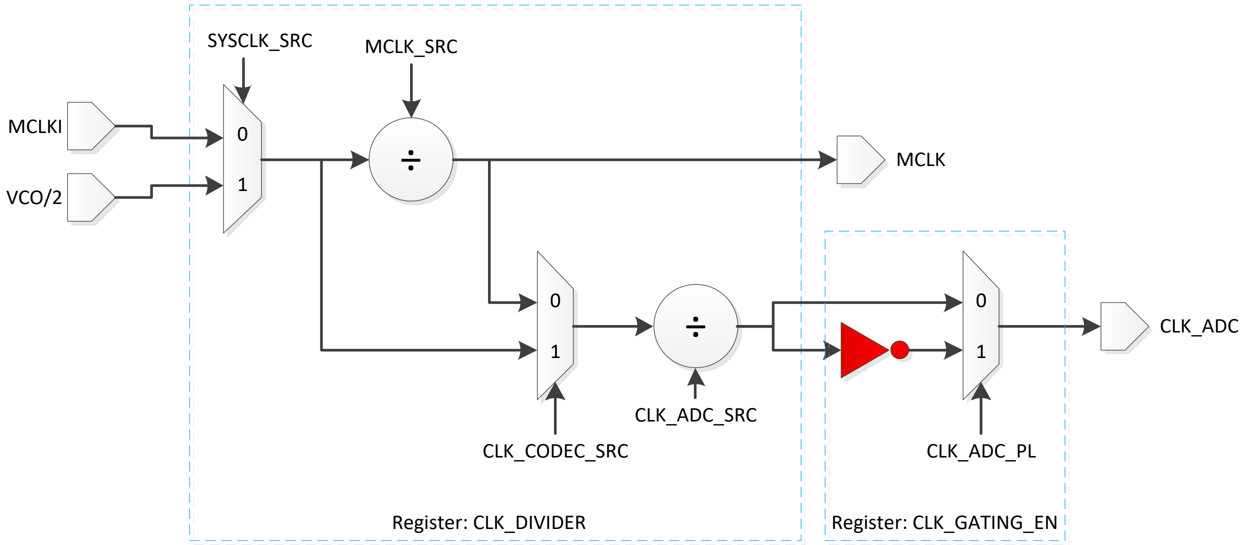


Figure 9: Clock Generation

Bits	MCLK_SRC REG0x03[4:0]
0000	Divide by 1
0001	Invert
0010	Divide by 2
0011	Divide by 4
0100	Divide by 8
0101	Divide by 16
0110	Divide by 32
0111	Divide by 3
1001	Invert
1010	Divide by 6
1011	Divide by 12
1100	Divide by 24

Table 4: CLOCK_SRC.MCLK_SRC REG0x03[4:0] Register Settings

Bits	CLK_ADC_SRC REG0x03[7:6]
00	Divide by 1
01	Divide by 2
10	Divide by 4
11	Divide by 8

Table 5: CLOCK_SRC.CLK_ADC_SRC REG0x03[7:6] Register Settings

The OSR (over sampling rate) is defined as CLK_ADC frequency divided by the audio sample rate.

$$OSR = \frac{CLK\_ADC}{Fs}$$

Available over-sampling rates are 32, 64, 128 or 256 as set in the ADC_SAMPLE_RATE.OSR REG0x3A[1:0] register. CLK_ADC frequency is set by CLOCK_SRC.CLK_CODEC_SRC REG0x03[13] and CLOCK_SRC.CLK_ADC_SRC REG0x03[7:6] registers.

It should be noted that the OSR and Fs must be selected so that the max frequency of CLK_ADC is less than 6.144MHz. When CLK_ADC is determined, ADC_SAMPLE_RATE.OSR REG0x3A[1:0] should be set to provide appropriate down sampling through digital filters.

Example 1:

To configure Fs = 48 kHz, MCLK = (256*Fs) = 12.288MHz, and CLK_ADC = 6.144MHZ

Set:

- CLOCK_SRC.CLK_CODEC_SRC REG0X03[13] = 1'b0, CLOCK_SRC.CKL_ADC_SRC REG0X03[7:6] = 2'b01, and OSR = 2'b10 (128)

Example 2:

To configure Fs = 16 kHz, MCLKI = 12.288MHz, and CLK_ADC = 4.096MHz

Set:

- CLOCK_SRC.MCLK_SRC REG0X03[4:0] = 3'b111 (Divide MCLKI by 3) to get MCLK = (256*Fs) = 4.096MHz
- CLOCK_SRC.CLK_CODEC_SRC REG0X03[13] = 1'b0, CLOCK_SRC.CLK_ADC_SRC REG0X03[7:6] = 2'b00, and OSR = 2'b11 (256)

4.1 PCM Clock Generation

In master mode, BCLK is derived from MCLK via a programmable divider set by PCM_CTRL1.BCLK_DIV REG0X11[2:0] and the FS is derived from BCLK via a programmable divider PCM_CTRL1.LRC_DIV REG0X11[13:12].

To select specific Fs values, PCM_CTRL1.BCLK_DIV REG0X11[2:0] and PCM_CTRL1.LRC_DIV REG0X11[13:12] must be set according to the block diagram seen in Figure 10 and the equation below.

$$BCLK = Fs \times data\ length \times channels$$

Example 1:

If we want an Fs of 48 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 48000*16*2 = 1.536MHz and MCLK = 48000*256 = 12.288MHz
- Set PCM_CTRL1.BCLK_DIV REG0X11[2:0]= 3'b011 (8) and PCM_CTRL1.LRC_DIV REG0X11[13:12]= 2'b11 (32)

Or 32 bit data is to be sent

- BCLK = 48000*32*2 = 3.073MHz and MCLK = 48000*256 = 12.288MHz
- Set PCM_CTRL1.BCLK_DIV REG0X11[2:0]= 3'b010 (4) and PCM_CTRL1.LRC_DIV REG0X11[13:12]= 2'b10 (64)

Example 2:

If we want an Fs of 16 kHz and 16 bit data is to be sent to the I2S bus (2 channel)

- BCLK = 16000*16*2 = 512kHz and MCLK = 16000*256 = 4.096MHz
- Set PCM_CTRL1.BCLK_DIV REG0X11[2:0]= 3'b011 (8) and PCM_CTRL1.LRC_DIV REG0X11[13:12]= 2'b11 (32)

32 bit data is to be sent,

- BCLK = 16000*32*2 = 1.024MHz and MCLK = 16000*256 = 4.096MHz
- Set PCM_CTRL1.BCLK_DIV REG0X11[2:0]= 3'b100 (4) and PCM_CTRL1.LRC_DIV REG0X11[13:12]= 2'b10 (64)

Example 3:

If we want an Fs of 16 kHz and 32 bit data is to be sent to the I2S TDM bus (4 channels)

- BCLK = 16000*32*4 = 2.048MHz and MCLK = 16000*256 = 4.096MHz
- Set PCM_CTRL1.BCLK_DIV REG0X11[2:0]= 3'b001 (2) and PCM_CTRL1.LRC_DIV

REG0x11[13:12]= 2’b01 (128)

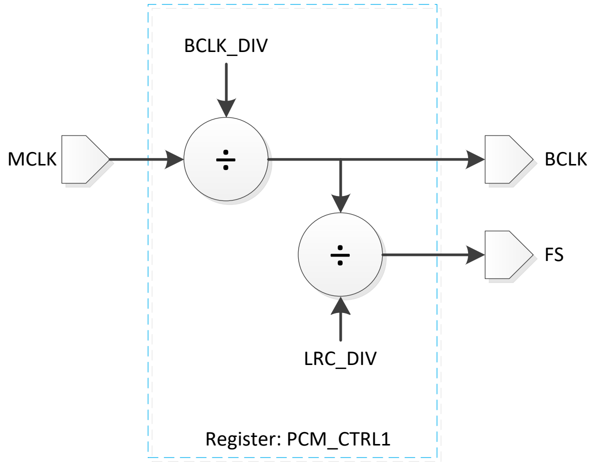


Figure 10: Master Mode PCM Clock Generation

Bits	BCLK_DIV REG0x11[2:0]
000	Divide by 1
001	Divide by 2
010	Divide by 4
011	Divide by 8
100	Divide by 16
101	Divide by 32

Table 6: PCM_CTRL1.BCLK_DIV REG0x11[2:0] Register Settings

Bits	LRC_DIV REG0x11[13:12]
00	Divide by 256
01	Divide by 128
10	Divide by 64
11	Divide by 32

Table 7: PCM_CTRL1.LRC_DIV REG0x11[13:12] Register Settings

4.2 Frequency Locked Loop (FLL)

The integrated FLL can be used to generate a master system clock, MCLK, from MCLKI, BCLK or FS as a reference. Because of the FLL’s tolerance of jitter, it may be used to generate a stable MCLK from less stable input clock sources or it can be used to generate a free-running clock in the absence of an external reference clock source. To run as a free running clock, enable FLL6.DCO_EN REG0x09[15] and set FLL_VCO_RSV.DOUT2VCO_RSV REG0x0A[15:0] to 16’hF13C.

The FLL is enabled using CLOCK_SRC.SYSCLK_SRC REG0x03[15] and it is recommended that the FLL be disabled before any setting changes via CLOCK_SRC.SYSCLK_SRC REG0x03[15] and then re-enabled after the register settings have been updated. To select between sources, use FLL3.FLL_CLK_REF_SRC REG0x06[11:10] and use FLL4.FLL_CLK_REF_DIV REG0x07[11:10] to divide the reference source by 1, 2, 4 or 8 to bring the frequency down to 13.5MHz or below.

To control the internal gain loop of the FLL, FLL3.GAIN_ERR REG0X06[15:13] and FLL4.FLL_REF_DIV_4CHK REG0X07[14:12] can be used. However, it is recommended that only the default settings be used in these registers.

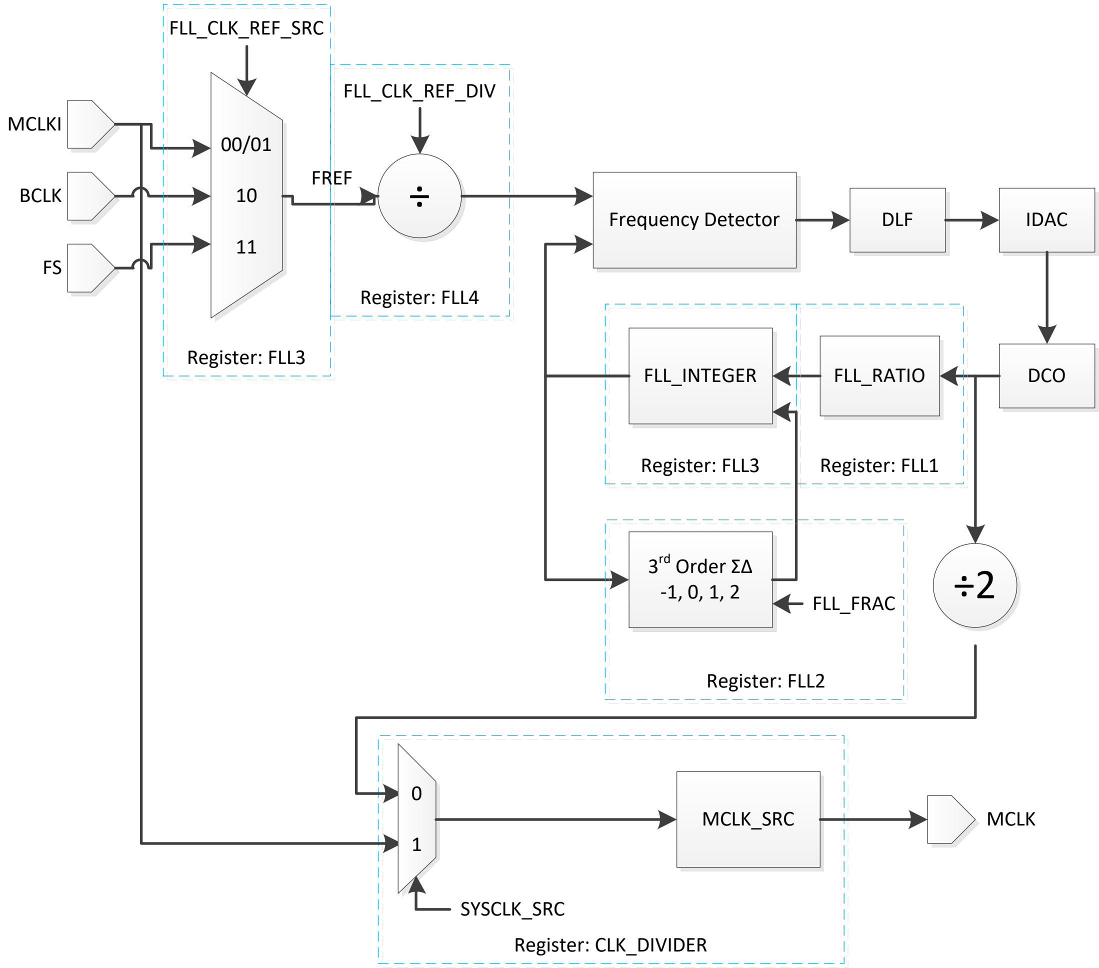


Figure 11: FLL Block diagram

The FLL output frequency is determined by the following parameters:

- FLL1.FLL_RATIO REG0X04[6:0]
- CLOCK_SRC.MCLK_SRC REG0X03[4:0]
- FLL3.FLL_INTEGER REG0X06[9:0]
- FLL2.FLL_FRAC REG0X05[15:0]

To determine these settings, the following output frequency equations are used:

1. FDCO = FREF × FLL_INTEGER REG0X06[9:0] . FLL_FRAC REG0X05[15:0] ÷ FLL4.FLL_CLK_REF_DIV REG0X07[14:12]
2. MCLK = (FDCO × MCLK_SRC REG0X03[4:0])/2

Where FREF is the reference clock frequency, MCLK is the desired system clock frequency, and FDCO is the frequency of DCO in decimal. It should also be noted that the values in the above equations are the decimal values of the registers.

Example:

If the reference frequency (FREF) is 12MHz, the desired sampling rate (Fs) is 48 kHz, and MCLK = 256*Fs, what are the output frequency parameters?

Using these requirements, the following can be determined.

- MCLK = 256 × 48kHz = 12.288MHz
- Using Equation 2:
  - FDCO = (2 × 12.288MHz) / MCLK_SRC
    - For FDCO to remain between 90MHz – 100MHz, MCLK_SRC must be chosen to be 1/4. This and other values for MCLK_SRC REG0X03[4:0] can be seen on the register tables.
  - FDCO = (2 × 12.288MHz) / (1/4) = 98.304MHz
- Using Equation 1:
  - FLL_INTEGER REG0X06[9:0] . FLL_FRAC REG0X05[15:0] = FDCO / FREF × FLL4.FLL_CLK_REF_DIV REG0X07[14:12]
  - FLL_RATIO REG0X04[6:0] = 1 because FREF ≥ 512 kHz. This and other values for FLL_RATIO REG0X04[6:0] can be seen on the register tables.
  - FLL_INTEGER REG0X06[9:0] . FLL_FRAC REG0X05[15:0] = 98.304MHz / (12MHz × 1) = 8.192
    - FLL_INTEGER REG0X06[9:0] . FLL_FRAC REG0X05[15:0] represents an integer and fractional number in decimal
  - FLL_INTEGER REG0X06[9:0] = 8
  - FLL_FRAC REG0X05[15:0] = 0.192
- Now retrieve or convert the parameter values into their corresponding HEX values
  - FLL_RATIO REG0X04[6:0] = 7'h1 (this value is taken from the register chart for FREF ≥ 512kHz)
  - MCLK_SRC REG0X03[4:0] = 4'h3 (this value is taken from the register chart for MCLK_SRC REG0X03[4:0] = 1/4)
  - FLL_INTEGER REG0X06[9:0] = 8 = 10'h8
  - FLL_FRAC REG0X05[15:0] = 0.192 × 2^16 = 12583=16'h3126

If low power consumption is required, then FLL settings must be chosen where FLL_INTEGER REG0X06[9:0] . FLL_FRAC REG0X05[15:0] is an integer (i.e. FLL_FRAC REG0X05[15:0] = 0). In this case, the fractional mode can be turned off by disabling register setting FLL6.SDM_EN REG0X09[14].

Application Notes:

- FLL4.FLL_CLK_REF_DIV REG0X07[11:10] can be used to reduce the reference frequency for SYSMCLK by dividing the input by 1, 2, 4, or 8. Use this to ensure the reference clock frequency is less than or equal to 13.5MHz.
- FLL3.GAIN_ERR REG0X06[14:12] and FLL5.FLL_CLK_REF_DIV_4CHK REG0X07[14:12] are used to control the gain and resolution, respectively. It is recommended that the default settings are used for these parameters.
- FDCO must be within the 90MHz – 100MHz or the FFL cannot be guaranteed across the full range of operation.
- FLL2.FLL_FRAC REG0X05[15:0] must be set to 0 for low power mode.
- FLL6.SDM_EN REG0X09[14] to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption.
- When FLL uses free running mode, chip needs to be set as a master in PCM_CTRL1 REG0X11[3]=1
- Set FLL6.CHB_FILTER_EN REG0X08[14] = '1' to enable FLL Loop Filter. Select filter clock source by FLL6.CHB_FILTER¬_EN REG0X08[13]. Select DCO input by FLL6.FILTER_SW REG0X08[12]. FLL6.CUTOFF500 REG0X09[13] & FLL6.CUTOFF600 REG0X09[12] can be used to define FLL cuttoff frequency at 500KHz or 600KHz. 500KHz will provide the best FLL performance but consume more power.

- set **FLL6.FLL_FLTR_DITHER_SEL REG0X09[7:6]** = ‘01’ or ‘10’ or ‘11’ as 1LSB / 2LSB / 3LSB random bits to Randomize the number of Filter Output Bits to average out output noise. If ‘00’, there is no dither.

5 Control Interfaces

5.1 Selection of Control Mode

The NAU85L40B features include a serial control bus that provides access to all of the device control registers. This bus may be configured either as a 2-wire interface that is interoperable with industry standard implementations of the I2C serial bus, or as a 3-wire bus compatible with commonly used industry implementations of the SPI (Serial Peripheral Interface) bus.

Mode selection is accomplished by means of combination of the MODE control logic pin and **MISC_CTRL.SPI3_EN REG0X51[15]**. The following table shows the three functionally different modes that are supported.

MODE Pin	SPI3_EN Reg0x51[15]	Description
1	x	2-Wire Interface, Read/Write operation
0	0	SPI Interface 3-Wire Write-only operation

Table 8: Control Interface Selection

The timing in all three bus configurations is fully static resulting in good compatibility with standard bus interfaces and software simulated buses. A software simulated bus can be very simple and low cost, such as by utilizing general purpose I/O pins on the host controller and software “bit banging” techniques to create the required timing.

5.2 2-Wire-Serial Control Mode (I²C Style Interface)

The 2-wire bus is a bidirectional serial bus protocol. This protocol defines any device that sends data onto the bus as a transmitter (or master), and the receiving device as the receiver (or slave). The NAU85L40B can function only as a slave device when in the 2-wire interface configuration.

5.3 2-Wire Protocol Convention

All 2-Wire interface operations must begin with a START condition, which is a HIGH-to-LOW transition of SDIO while SCLK is HIGH. All 2-Wire interface operations are terminated by a STOP condition, which is a LOW to HIGH transition of SDIO while SCLK is HIGH. A STOP condition at the end of a read or write operation places the device in a standby mode.

An acknowledge (ACK), is a software convention used to indicate a successful data transfer. To allow for the ACK response, the transmitting device releases the SDIO bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDIO line LOW to acknowledge the reception of the eight bits of data.

Following a START condition, the master must output a device address byte. This consists of a 7-bit device address, and the LSB of the device address byte is the R/W (Read/Write) control bit. When R/W=1, this indicates the master is initiating a read operation from the slave device, and when R/W=0, the master is initiating a write operation to the slave device. If the device address matches the address of the slave device, the slave will output an ACK during the period when the master allows for the ACK signal.

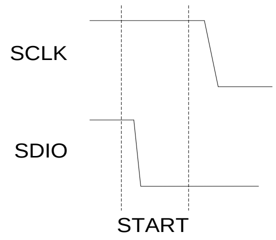


Figure 12: Valid START Condition

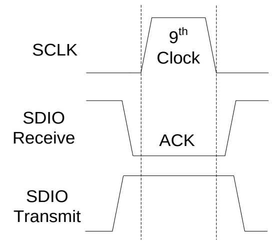


Figure 13: Valid Acknowledge

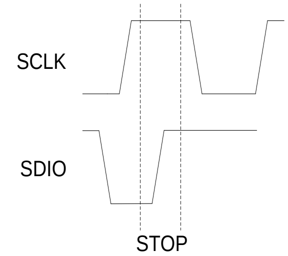


Figure 14: Valid STOP Condition

0	0	1	1	1	0	csb	R/W	Device Address Byte
A15	A14	A13	A12	A11	A10	A9	A8	Control Address Bytes
A7	A6	A5	A4	A3	A2	A1	A0	
D15	D14	D13	D12	D11	D10	D9	D8	Data Bytes
D7	D6	D5	D4	D3	D2	D1	D0	

Figure 15: Slave Address Byte, Control Address Bytes, and Data Byte Order

5.4 2-Wire Write Operation

A Write operation consists of a three-byte instruction followed by one or more Data Bytes. A Write operation requires a START condition, followed by a valid device address byte with R/W=0, a valid control address byte, data byte(s), and a STOP condition.

The Device Address of the NAU85L40B is either 0x1C (CSB=0) or 0x1D (CSB=1). In I2C mode the CSB pin will set the LSB of the Slave Address. If the Device Address matches this value, the NAU85L40B will respond with the expected ACK signaling as it accepts the data being transmitted to it.

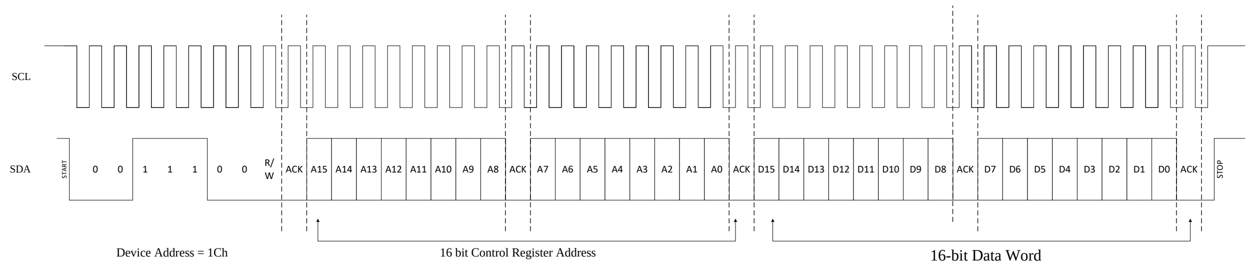


Figure 16: Byte Write Sequence

5.5 2-Wire Read Operation

A Read operation consists of a three-byte Write instruction followed by a Read instruction of one or more data bytes. The bus master initiates the operation issuing the following sequence: a START condition, device address byte with the R/W bit set to “0”, and a Control Register Address byte. This indicates to the slave device which of its control registers is to be accessed.

If the device address matches this value, the NAU85L40B will respond with the expected ACK signaling as it accepts the Control Register Address being transmitted into it. After this, the master transmits a second START condition, and a second instantiation of the same device address, but now with R/W=1.

After again recognizing its device address, the NAU85L40B transmits an ACK, followed by a two byte value containing the 16 bits of data from the selected control register inside the NAU85L40B.

During this phase, the master generates the ACK signaling with each byte transferred from the NAU85L40B. If there is no STOP signal from the master, the NAU85L40B will internally auto-increment the target Control Register Address and then output the two data bytes for this next register in the sequence.

This process will continue as long as the master continues to issue ACK signaling. If the Control Register Address being indexed inside the NAU85L40B reaches the value 0xFFFF (hexadecimal) and the value for this register is output, the index will roll over to 0x0000. The data bytes will continue to be output until the master terminates the read operation by issuing a STOP condition.

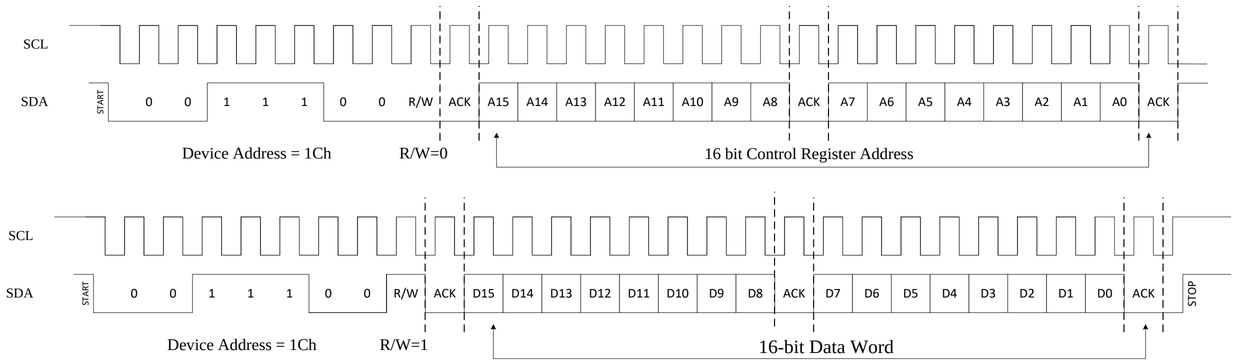


Figure 17: Read Sequence

5.6 Digital Serial Interface Timing

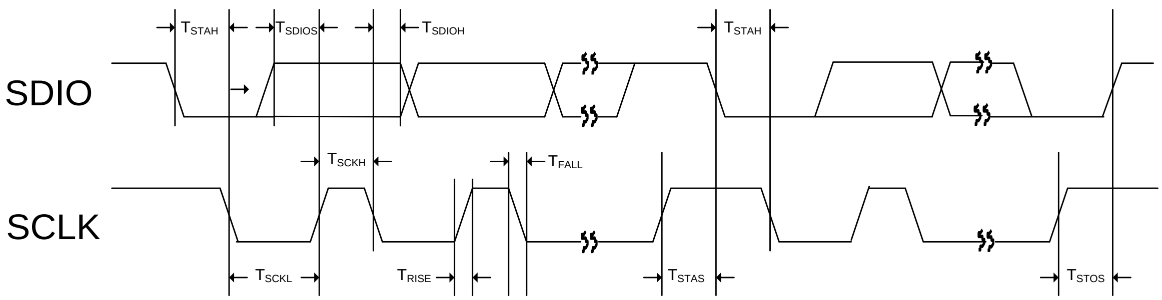


Figure 18: Two-Wire Control Mode Timing

Symbol	Description	min	typ	max	unit
T_{STAH}	SDIO falling edge to SCLK falling edge hold timing in START / Repeat START condition	600	-	-	ns
T_{STAS}	SCLK rising edge to SDIO falling edge setup timing in Repeat START condition	600	-	-	ns
T_{STOS}	SCLK rising edge to SDIO rising edge setup timing in STOP condition	600	-	-	ns
T_{SCKH}	SCLK High Pulse Width	600	-	-	ns
T_{SCKL}	SCLK Low Pulse Width	1,300	-	-	ns
T_{RISE}	Rise Time for all 2-wire Mode Signals	-	-	300	ns
T_{FALL}	Fall Time for all 2-wire Mode Signals	-	-	300	ns
T_{SDIOS}	SDIO to SCLK Rising Edge DATA Setup Time	100	-	-	ns
T_{SDIOH}	SCLK falling Edge to SDIO DATA Hold Time	0	-	600	ns

5.7 Software Reset

The entire NAU85L40B and all of its control registers can be reset to default initial conditions by writing any value to **SW_RESET REG0X00**, using any of the control interface modes. Writing to any other valid register address terminates the reset condition, but all registers will now be set to their power-on default values.

6 Digital Audio Interface

The NAU85L40B can be configured as either the master or the slave, by setting **PCM_CTRL1.MS REG0X11[3]**, 1 for master mode and 0 for slave mode. By default, the NAU85L40B is in Slave mode. In master mode, NAU85L40B outputs both Frame Sync (FS) and the audio data bit clock (BCLK) which has full control of the data transfer. In the slave mode, an external controller supplies BCLK and FS. Data is latched on the rising edge of BCLK.

In master mode, the BCLK and FS are generated from MCLK according to the clock division specified in **PCM CLOCK GENERATION**.

There are two data ports DO12 and DO34 used. The DO12 port only supports normal mode. DO34 can be configured in normal mode and TDM mode setting by **PCM_CTRL4.TDM_MODE REG0X14[15]**. The DO12/DO34 default setting is normal mode with PCM A format.

When DO12 or DO34 are not driving PCM data, they can be configured to drive a low output, be tri-state, or have a weak pull-up or pull-down. If **PCM_CTRL1.DO12_DRV REG0X11[14]** is set then DO12 will drive an output low when not transmitting data. Likewise **PCM_CTRL2.DRO34_DRV REG0X12[14]** performs the same function for DO34. When DO12_TRI and DO34_TRI are set DO12/DO34 will be tri-state when not transmitting. Pull-up or pull-down devices can be added to the DO12/DO34 pins by setting pull enable (DO12_PE/DO34_PE) bits and selecting up or down with DO12_PS/DO34_PS where 1 = pull-up and 0 = pull-down. This enables user to configure for wired-OR type bus sharing. All of these controls can be found in register **PCM_CTRL1 REG0X11** and **PCM_CTRL2 REG0X12**.

If PE and PS are both logic=0, DO12/DO34 are high impedance, except when actively transmitting left and right channel audio data. After outputting audio channel data, DO12/DO34 will return to high impedance on the BCLK negative edge during the LSB data period if **PCM_CTRL1.TRI REG0X11[9]**, is HIGH, or on the BCLK positive edge of LSB if **PCM_CTRL1.TRI REG0X11[9]** is LOW. Tri-stating on the negative edge allows the transmission of data by multiple sources in adjacent timeslots with reduced risk of bus driver contention.

There are six types of data formats in normal mode, which is entered with **PCM_CTRL4.TDM_MODE REG0X14[15]** = 0.

PCM Mode	PCM_CTRL0.AIFMT REG0x10[1:0]	PCM_CTRL0.LRP REG0x10[6]	PCM_CTRL1.PCM_TS_EN REG0x11[10]	PCM_CTRL4.TDM_OFFSET_EN REG0x14[14]
Right Justified	00	0	0	0
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Time Slot	11	Don't care	1	0

Table 9: Digital Audio Interface Normal Modes

6.1 Right-Justified Audio Data

In right-justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below where N is the word length.

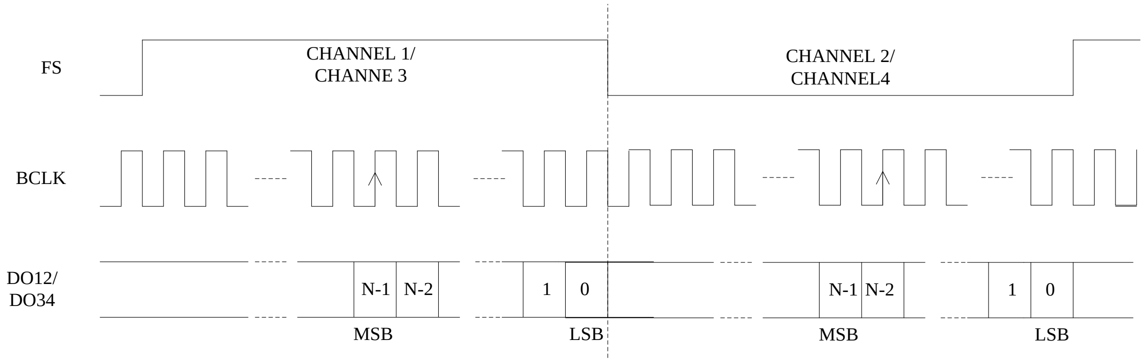


Figure 19: Right Justified Audio Format

6.2 Left-Justified Audio Data

In left-justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, left channel data is transmitted and when FS is LOW, right channel data is transmitted. This is shown in the figure below.

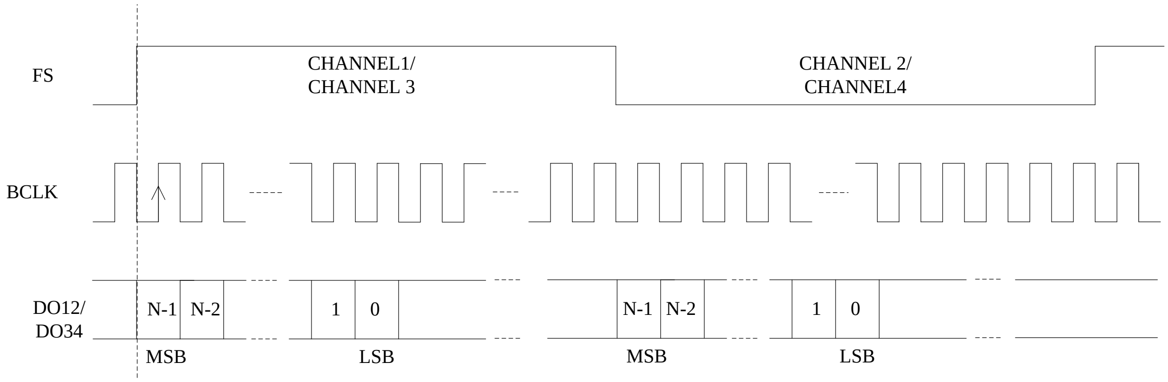


Figure 20: Left Justified Audio Format

6.3 I2S Audio Data Mode

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, left channel data is transmitted and when FS is HIGH, right channel data is transmitted. This is shown in the figure below.

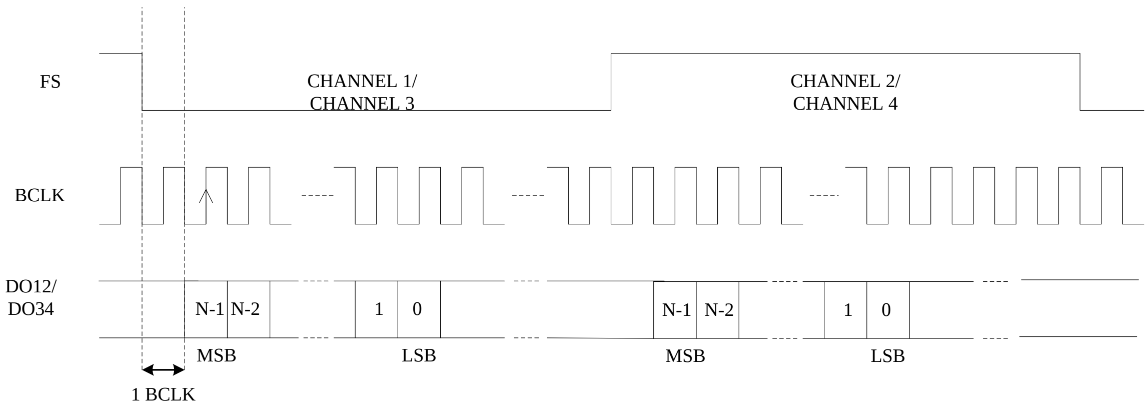


Figure 21: I2S Audio Format

6.4 PCM A Audio Data

In the PCM A mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

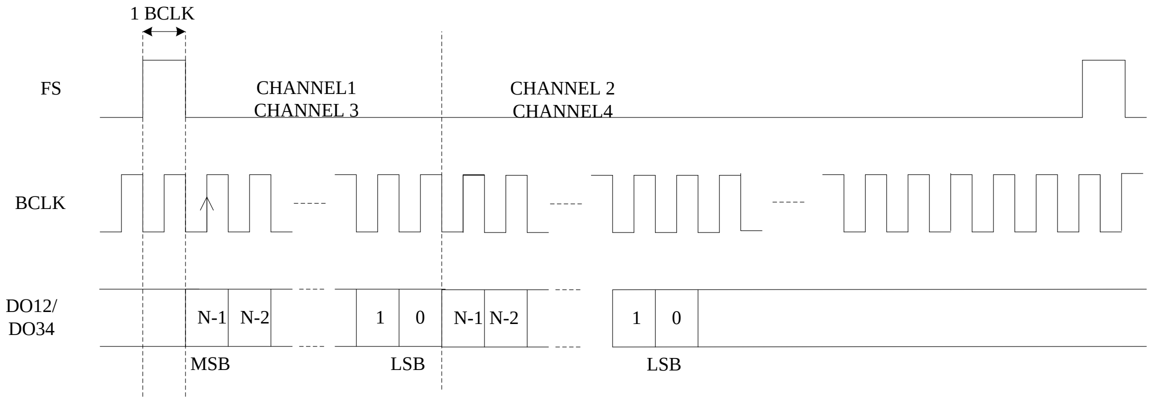


Figure 22: PCM A Audio Format

6.5 PCM B Audio Data

In the PCM B mode, left channel data is transmitted first followed immediately by right channel data. The left channel MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the right channel MSB is clocked on the next SCLK after the left channel LSB. This is shown in the figure below.

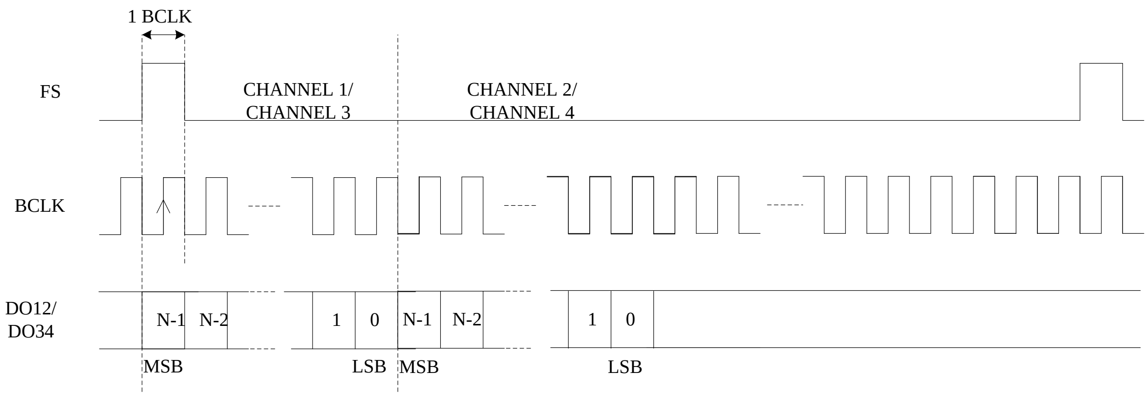


Figure 23: PCM B Audio Format

6.6 PCM Time Slot Audio Data

The PCM time slot mode is used to delay the time at ADC data are clocked. This increases the flexibility of the NAU85L40B to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40B or other devices to share the audio data bus, thus enabling more than two channels of audio. This feature may also be used to swap left and right channel data, or to cause both the left and right channels to use the same data.

Normally, the ADC data are clocked immediately after the Frame Sync (FS). In the PCM time slot mode, the audio data are delayed by a delay count specified in the device control registers. The left channel MSB is clocked on the BCLK rising edge defined by the delay count set in PCM_CTRL2.TSLOT_L REG0X12[9:0]. The right channel MSB is clocked on the BCLK rising edge defined by the delay count set in PCM_CTRL3.TSLOT_R REG0X13[9:0].

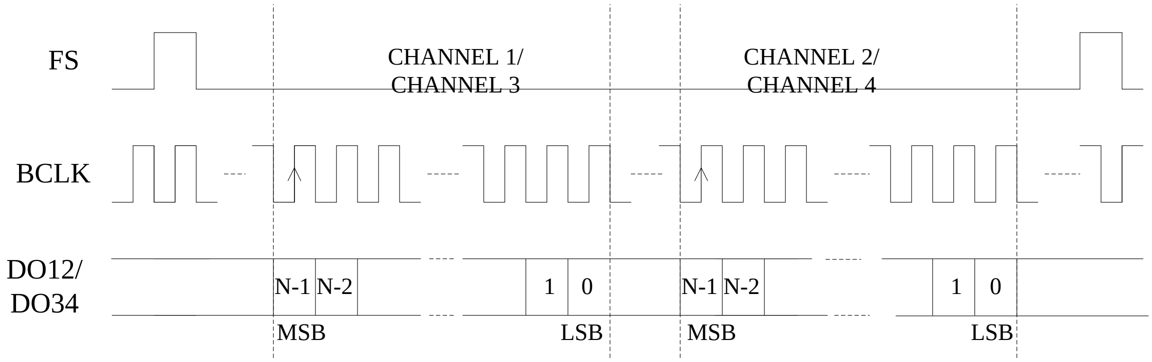


Figure 24: PCM Time Slot Audio Format

There are six types of data formats in TDM mode, entered by setting TDM_MODE, PCM_CTRL4.TDM_MODE REG0X14[15] = 1.

PCM Mode	PCM_CTRL0.AIFMT REG0X10[1:0]	PCM_CTRL0.LRP REG0X10[6]	PCM_CTRL1.PCM_TS_EN REG0X11[10]	PCM_CTRL4.TDM_OFFSET_EN REG0X14[14]
Right Justified	00	0	0	0
Left Justified	01	0	0	0
I2S	10	0	0	0
PCM A	11	0	0	0
PCM B	11	1	0	0
PCM Time Slot	11	Don’t care	0	1

Table 10: Digital Audio Interface TDM Modes.

6.7 AUDIO INTERFACE TIMING DIAGRAM

I2S timing diagram shows the audio timing diagram among BCLK, FS, DACIN, and ADCOUT. For NAU85L40B, the timing parameters are shown in TABLE 11:AUDIO INTERFACE TIMING PARAMETERS

6.7.1 AUDIO INTERFACE IN SLAVE MODE

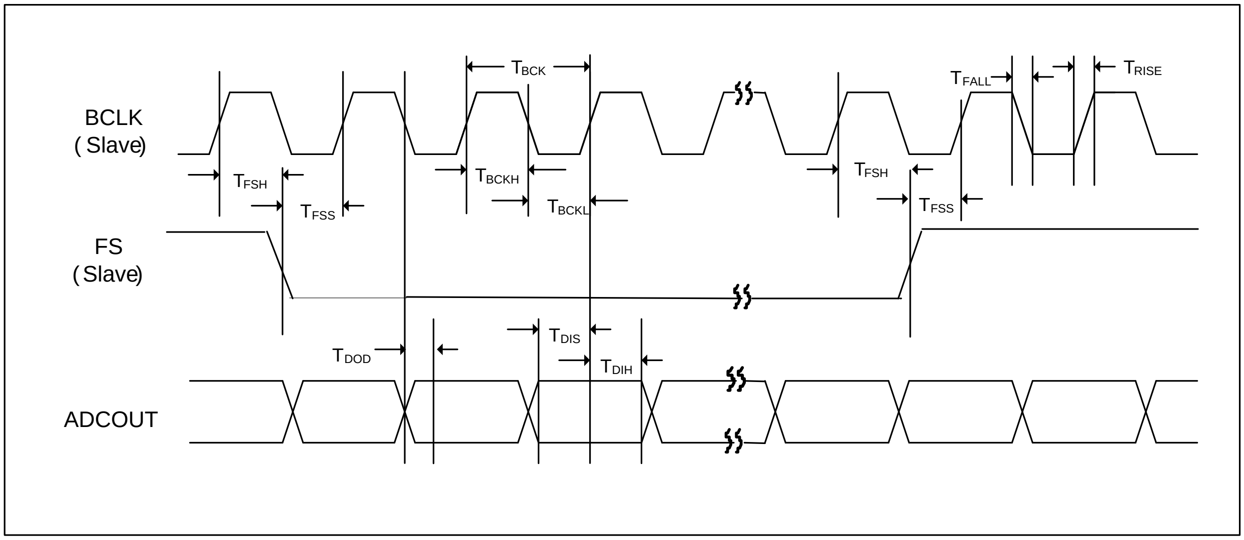


Figure 25:Audio Interface Slave Mode Timing Diagram

6.7.2 AUDIO INTERFACE IN MASTER MODE

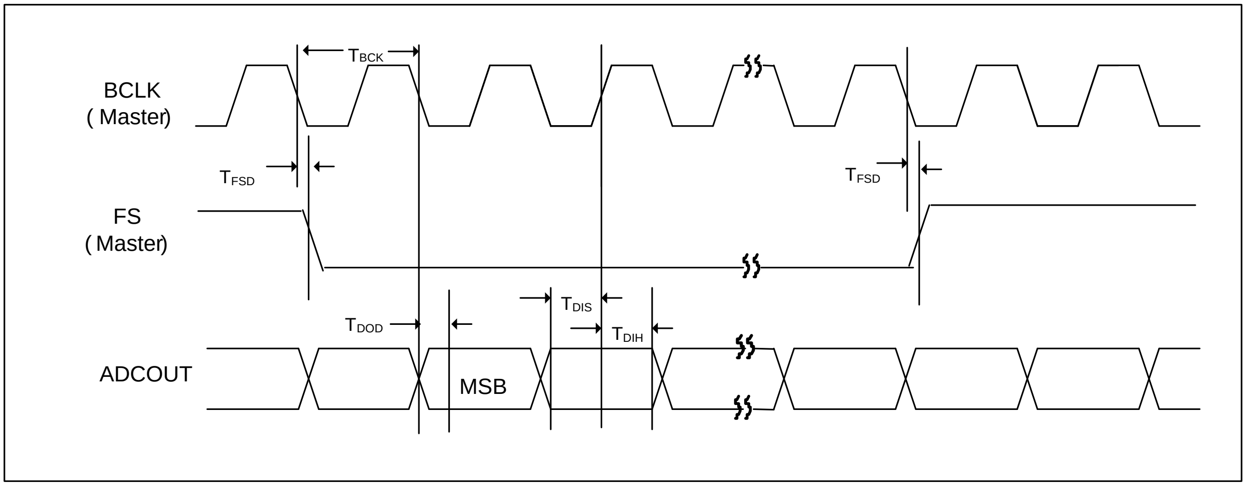


Figure 25: Audio Interface in Master Mode Timing Diagram

6.7.3 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Audo Data)

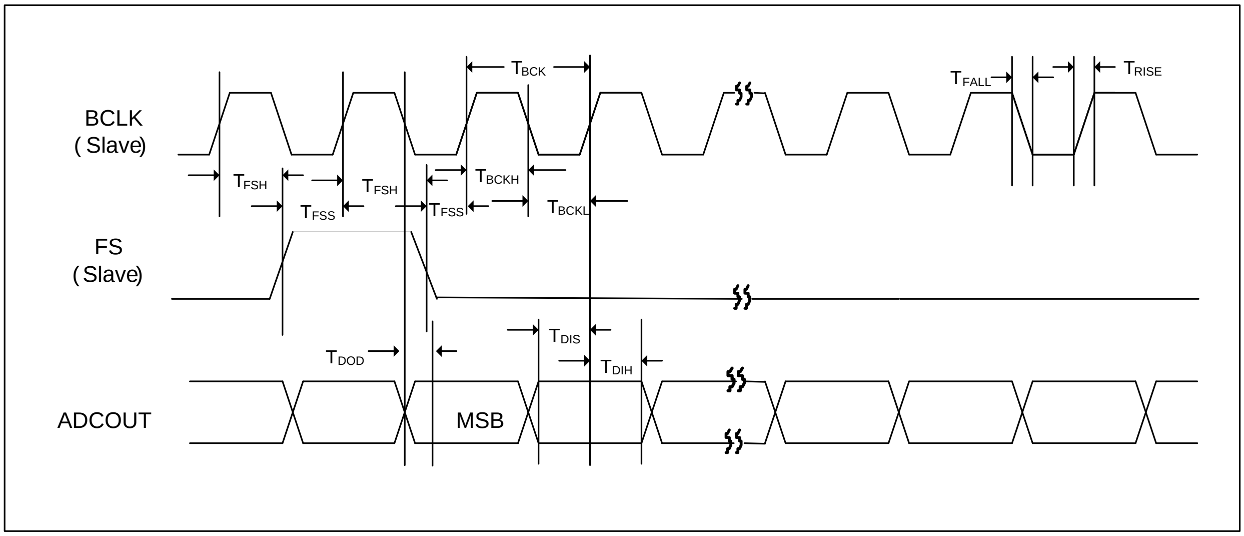


Figure 26:PCM Audio Interface Slave Mode Timing Diagram

6.7.4 PCM AUDIO INTERFACE IN MASTER MODE

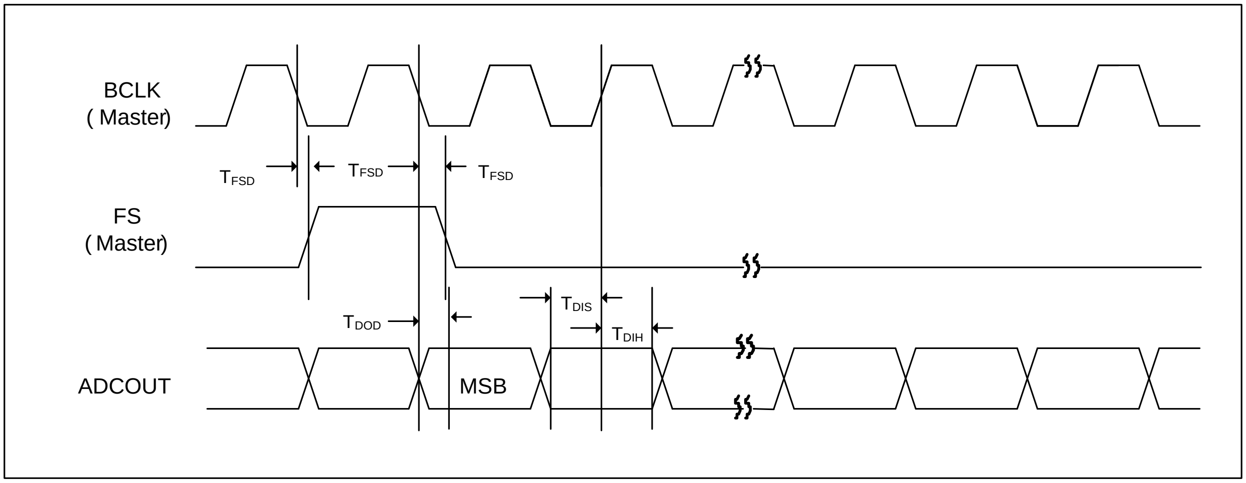


Figure 28:PCM AUDIO Interface Master Mode Timing Diagram

6.7.5 PCM AUDIO INTERFACE IN SLAVE MODE (PCM Time Slot Mode)

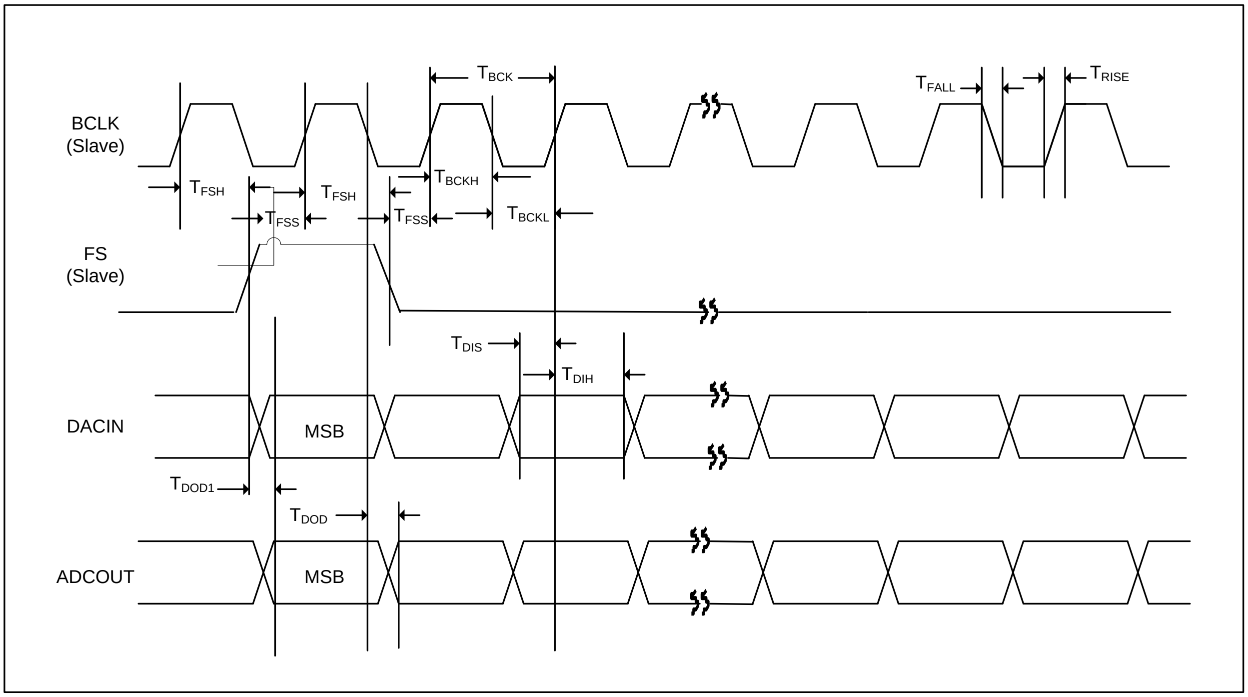


Figure 29:PCM Audio Interface Slave Mode (PCM Time Slot Mode)

6.7.6 PCM AUDIO INTERFACE IN MASTER MODE (PCM Time Slot Mode)

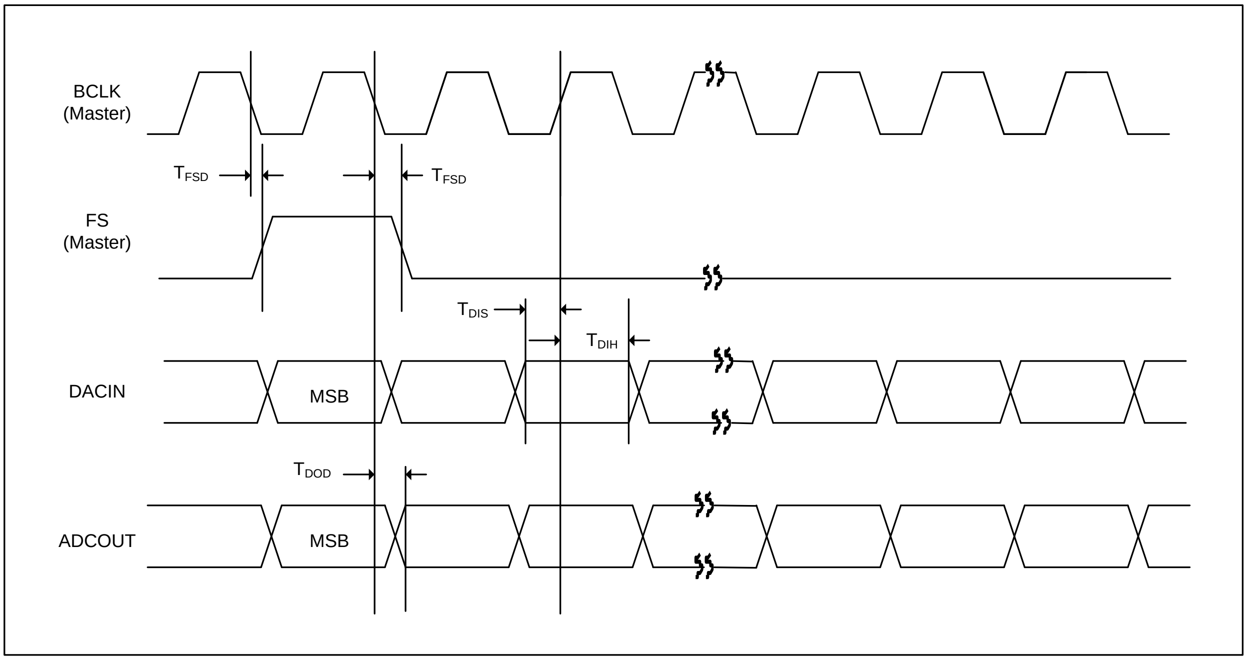


Figure 27:PCM Audio Interface Master Mode (PCM Time Slot Mode)Timing Diagram

6.7.7 AUDIO Timing Parameter

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{BCK}	BCLK Cycle Time in Slave Mode	50	---	---	ns
T_{BCKH}	BCLK High Pulse Width in Slave Mode	20	---	---	ns
T_{BCKL}	BCLK Low Pulse Width in Slave Mode	20	---	---	ns
T_{FSS}	FS to BCLK Rising Edge Setup Time in Slave Mode	20	---	---	ns
T_{FSH}	BCLK Rising Edge to FS Hold Time in Slave Mode	20	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{DIS}	ADCIN to BCLK Rising Edge Setup Time	15	---	---	ns
T_{DIH}	BCLK Rising Edge to ADCIN Hold Time	15	-	-	ns
T_{DOD}	BCLK Falling Edge to DACOUT Delay Time	---	-	80^*	ns

Table 11:AUDIO Interface Timing Parameters (Slave Mode)

Symbol	**Description**	**min**	**typ**	**max**	**unit**
T_{BCK}	BCLK Cycle Time	50	---	---	ns
T_{RISE}	Rise Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{FALL}	Fall Time for All Audio Interface Signals	---	---	$0.135T_{BCK}$	ns
T_{FSD}	BCLK Falling Edge to FS Delay Time in Master Mode	-	-	10	ns
T_{DIS}	ADCIN to BCLK Rising Edge Setup Time	15	-	-	ns
T_{DIH}	BCLK Rising Edge to ADCIN Hold Time	15	-	-	ns
T_{DOD}	BCLK Falling Edge to DACOUT Delay Time	-	-	80^*	ns

Table 12: AUDIO Interface Timing Parameters (Master Mode)

Note: *ADCOUT pin has no loading.

6.8 TDM Right Justified Audio Data

In right justified mode, the LSB is clocked on the last BCLK rising edge before FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 data is transmitted. This is shown in the figure below.

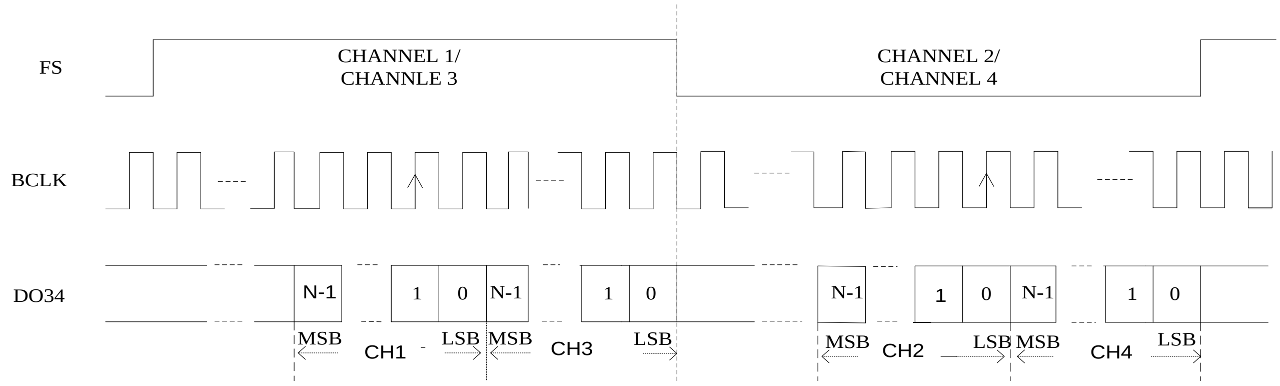


Figure 31: TDM Right Justified Audio Format

6.9 TDM Left Justified Audio Data

In left justified mode, the MSB is clocked on the first BCLK rising edge after FS transitions. When FS is HIGH, channel 1 then channel 3 data is transmitted and when FS is LOW, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

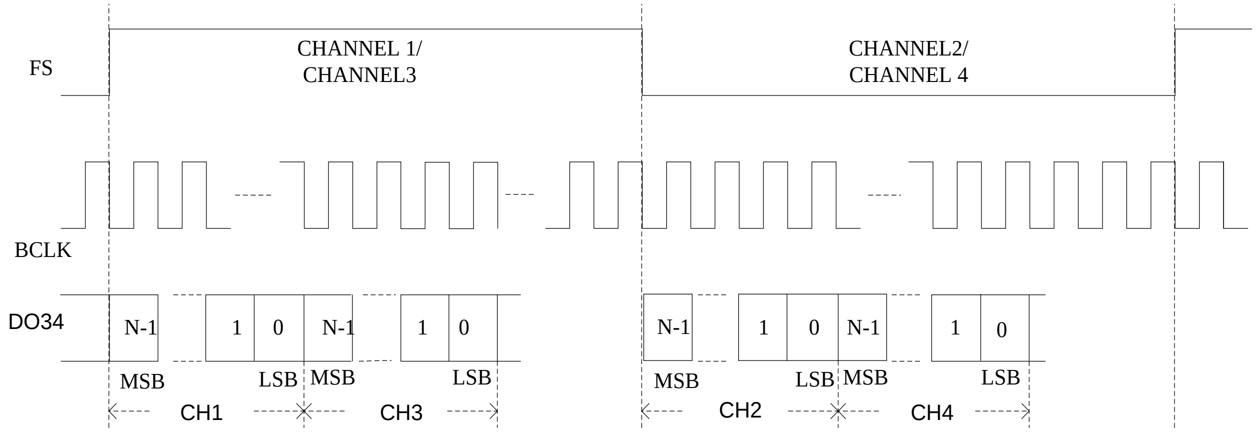


Figure 32: TDM Left Justified Audio Format

6.10 TDM I2S Audio Data

In I2S mode, the MSB is clocked on the second BCLK rising edge after FS transitions. When FS is LOW, channel 1 then channel 3 channel data is transmitted and when FS is HIGH, channel 2 then channel 4 channel data is transmitted. This is shown in the figure below.

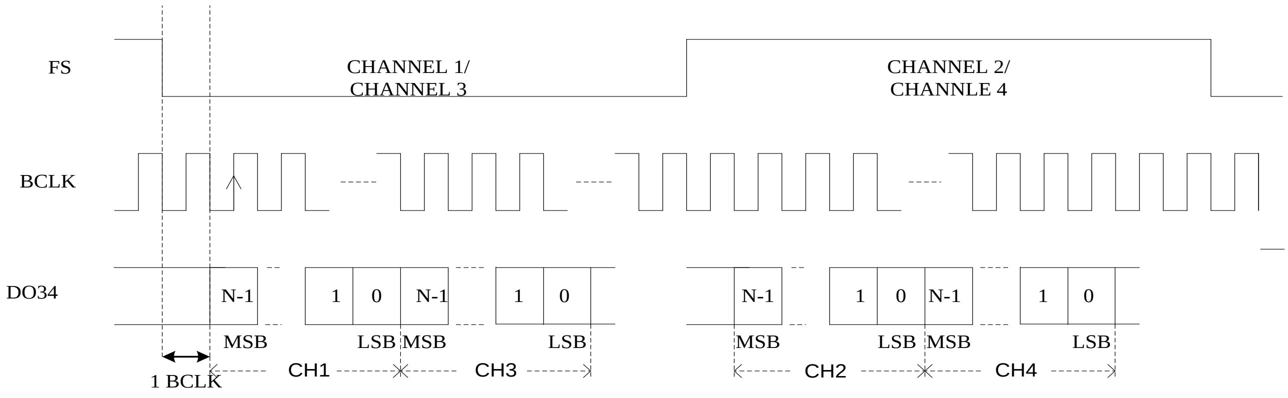


Figure 33: TDM I2S Audio Format

6.11 TDM PCM A Audio Data

In the PCM A mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the second BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

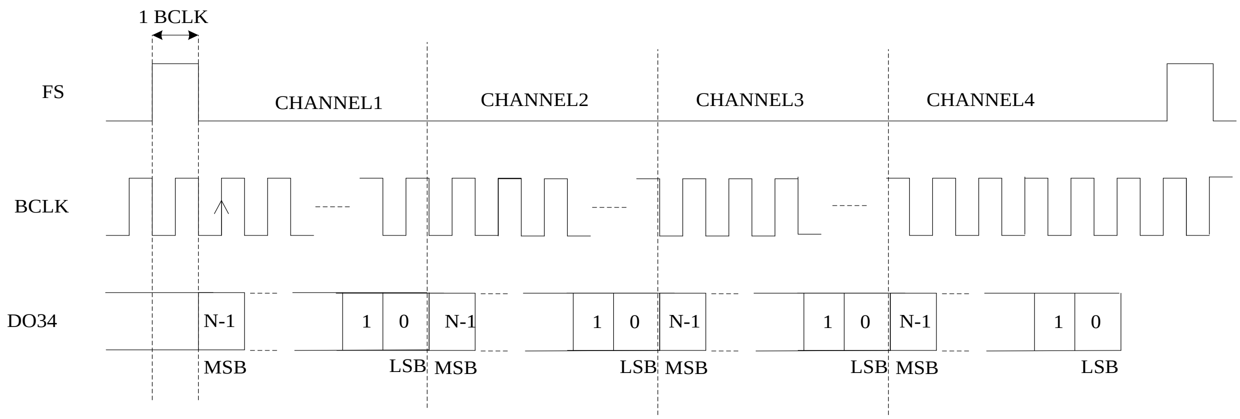


Figure 34: TDM PCM A Audio Format

6.12 TDM PCM B Audio Data

In the PCM B mode, channel 1 data is transmitted first followed sequentially by channel 2, 3, and 4 immediately after. The channel 1 MSB is clocked on the first BCLK rising edge after the FS pulse rising edge, and the subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This is shown in the figure below.

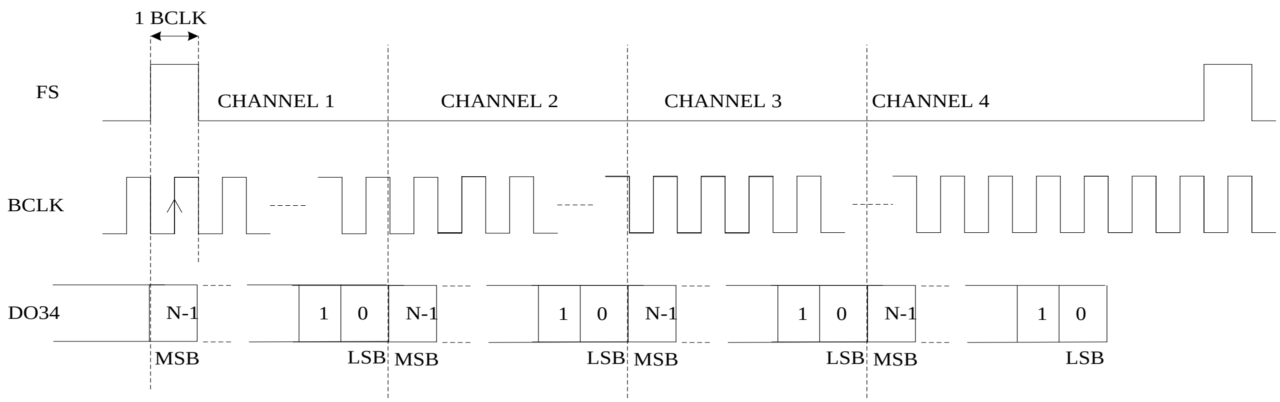


Figure 35: TDM PCM B Audio Format

6.13 TDM PCM Offset Audio Data

The PCM offset mode is used to delay the time at which the ADC data is clocked. This increases the flexibility of the NAU85L40B to be used in a wide range of system designs. One key application of this feature is to enable multiple NAU85L40B or other devices to share the audio data bus, thus enabling more than four channels of audio. This feature may also be used to swap channel data, or to cause multiple channels to use the same data.

Normally, the ADC data are clocked immediately after the Frame Sync (FS). In this mode audio data is delayed by a delay count specified in the device control registers. The channel 1 MSB is clocked on the BCLK rising edge defined by the delay count set in PCM_CTRL2.TSLOT_L REG0X12[9:0]. The subsequent channel's MSB is clocked on the next BCLK after the previous channel's LSB. This can be seen in the figure below.

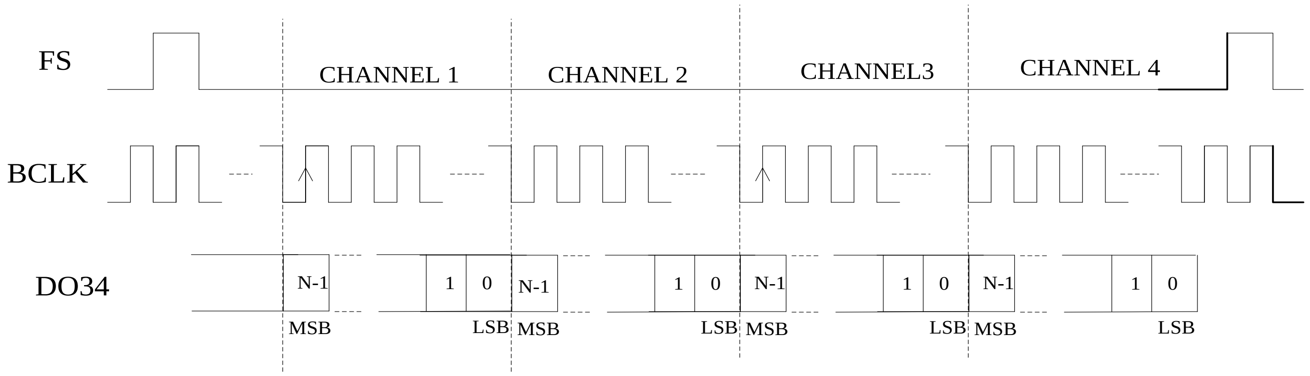


Figure 36: TDM PCM Offset Audio Format

Application Notes:

- When using PCM_CTRL2.TSLOT_L REG0X12[9:0] for time slot shift in TDM mode, the four channels will shift together for the same chip. The shift number should be N* Word Lenghth +1, and available channels should be > N+4, where N is desired channel width shift.

7 Register Map

REG	Function
0	SW_RESET
1	POWER_MANAGEMENT
2	CLOCK_CTRL
3	CLOCK_SRC
4	FLL1
5	FLL2
6	FLL3
7	FLL4
8	FLL5
9	FLL6
A	FLL_VCO_RSV
10	PCM_CTRL0
11	PCM_CTRL1
12	PCM_CTRL2
13	PCM_CTRL3
14	PCM_CTRL4
20	ALC_CONTROL_1
21	ALC_CONTROL_2
22	ALC_CONTROL_3
23	ALC_CONTROL_4
24	ALC_CONTROL_5
2D	ALC_GAIN_CH12
2E	ALC_GAIN_CH34
2F	ALC_STATUS
30	NOTCH_FIL1_CH1
31	NOTCH_FIL2_CH1
32	NOTCH_FIL1_CH2
33	NOTCH_FIL2_CH2
34	NOTCH_FIL1_CH3
35	NOTCH_FIL2_CH3
36	NOTCH_FIL1_CH4
37	NOTCH_FIL2_CH4
38	HPF_FILTER_CH12

REG	Function
39	HPF_FILTER_CH34
3A	ADC_SAMPLE_RATE
40	DIGITAL_GAIN_CH1
41	DIGITAL_GAIN_CH2
42	DIGITAL_GAIN_CH3
43	DIGITAL_GAIN_CH4
44	DIGITAL_MUX
48	P2P_CH1
49	P2P_CH2
4A	P2P_CH3
4B	P2P_CH4
4C	PEAK_CH1
4D	PEAK_CH2
4E	PEAK_CH3
4F	PEAK_CH4
50	GPIO_CTRL
51	MISC_CTRL
52	I2C_CTRL
58	I2C_DEVICE_ID
5A	RST
60	VMID_CTRL
61	MUTE
64	ANALOG_ADC1
65	ANALOG_ADC2
66	ANALOG_PWR
67	MIC_BIAS
68	REFERENCE
69	FEPGA1
6A	FEPGA2
6B	FEPGA3
6C	FEPGA4
6D	PWR

REG	Function	Name	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Description
0	SW_RESET	SW_RESET																	Software reset register. Resets chip to POR state.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
1	POWER_MANAGEMENT	ADC4_EN																	Channel 4 analog-to-digital converter power control 0 = ADC4 stage OFF 1 = Enabled
		ADC3_EN																	Channel 3 analog-to-digital converter power control 0 = ADC3 stage OFF 1 = Enabled
		ADC2_EN																	Channel 2 analog-to-digital converter power control 0 = ADC2 stage OFF 1 = Enabled
		ADC1_EN																	Channel 1 analog-to-digital converter power control 0 = ADC1 stage OFF 1 = Enabled
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
2	CLOCK_CTRL	CLK_ALC_SLOW_EN																	Enable ALC slow clock (only works with CLK_ALC_EN) 0 = Disable 1 = Enable
		CLK_ALC_EN																	Enable ALC clock 0 = Disable 1 = Enable
		CLK_I2S_GEN_EN																	Enable I2S/PCM clock 0 = Disable 1 = Enable
		CLK_ADC_POL																	ADC Clock Polarity 0 = Pass through 1 = Invert
		MCLKO_PS																	MCLKO_PS: =1 Selects the MCLKO pin pull-up. '0' selects the MCLKO pin pull-down
		MCLKO_PE																	MCLKO_PE: = 1 Turns on the MCLKO pin pull-up/down
		MCLKO_TRI																	MCLKO_TRI =1 Turns of clock output driver on MCLKO pin and sets MCLKO pin in tri-state condition.
		ADC_DSP_EN																	enable for ADC DSP path for high pass, ALC, and notch filter
		Default	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x8000**
3	CLOCK_SRC	SYSCLK_SRC																	Master System Clock Source 0 = MCLKI pin 1 = FLL VCO/2 as source
		CLK_CODEC_SRC																	CODEC Clock Source 0 = Internal MCLK (MCLK_SRC output) 1 = SYSCLK (SYSCLK_SRC output)
		CLK_GPIO_SRC																	MCLK Scaling for GPIO clock divider 00 = Divide by 8 01 = MCLK 10 = Divide by 2 11 = Divide by 4
		CLK_ADC_SRC																	ADC Clock Source 00 = Pass through 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8
		MCLK_SRC																	Master Clock (MCLK) Source 0000 = Pass through; 0001 = Invert 0010 = Divide by 2; 0011 = Divide by 4 0100 = Divide by 8; 0101 = Divide by 16 0110 = Divide by 32; 0111 = Divide by 3 1001 = Invert; 1010 = Divide by 6 1011 = Divide by 12; 1100 = Divide by 24
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**

4	FLL1	FLLISELDAC																	Recommended default 000
		ICTRL_LATCH																	FLL DSP speed capability control. When FLL running at high frequency with long decimal number, DSP needs to operate at high speed. By adjusting ICTRL_LATCH, FLL DSP can optimize between performance and power consumption (111 has highest power consumption for FLL DSP.) On the other hand, (DCO frequency)/(FLL input reference frequency)=integer, default setting can be used to reduce power. The strength of This register is using thermometer coding. 000 = Default 001 = 1x 010 = 1.5x 011 = 2x 110 = 2.5x 111 = 3x
		ICTRL_V2I																	**Amplifier Half Bias-Current Selector** Amp bias current must be reduced to 50% of its nominal value 00 = No Power Reduction 01 = Half Bias Current on FLL_BIAS_AMP2X 10 = Half Bias Current on FLL_BIAS_AMP 11 = Half Current on Both Amps
		FLL_LOCK_BP																	Manually force FLL to lock. 0 = Default setting 1 = Force lock enabled
		FLL_RATIO [6:0]																	0000001 = for input clock frequency >= 512Khz, 0000010 = for input clock frequency >= 256Khz 0000100 = for input clock frequency >= 128Khz 0001000 = for input clock frequency >= 64Khz 0010000 = for input clock frequency >= 32Khz 0100000 = for input clock frequency >= 8Khz 1000000 = for input clock frequency >= 4Khz
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0x0001**
5	FLL2	FLL_FRAC																	FLL 16-bit fractional input
		Default	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**0x3126**
6	FLL3	GAIN_ERR																	**FLL Gain Error correction threshold setting;** the threshold is comparison between DCO and target frequency.1111 has the most accurate DCO to target frequency. However, the gain error setting conditionally and inversely depends on FLL input reference clock rate. Higher FLL reference input frequency can only set lower gain error, such as 0000 for input reference from MCLK=12.288MHz. On the other side, if FLL reference input is from Frame sync, 48KHz, higher error gain can apply such as 1111. 000 = recommended 001 = x2 010 = x4 011 = x8 100 = x16 101 = x32 110 = x64
		FLL_CLK_REF_SRC																	FLL Reference CLK Source Select 00 & 01 = MCLK Pin 10 = BCLK Pin 11 = FS Pin
		FLL_INTEGER																	10-bit integer DCO output frequency divider for FLL filter clock: the value is in orders of 2. When 0x8[13]=1, it selects DCO clock as FLL filter clock. The filter clock rate needs to be less than 1Mhz. With setting proper value, filter clock can be divided down from DCO clock. For example, DCO runs at 96Mhz, by setting value 0x60=96, filter clock becomes 1Mhz
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0x0008**
7	FLL4																		Reserved
		FLL_CLK_REF_DIV_4CHK																	FLL Clock Reference divider for accurate lock detection 000 = recommended 001 = div by 2 010 = div by 4 011 = div by 8 100 = div by 16 101 = div by 32

		FLL_CLK_REF_DIV																	FLL pre-scalar 00 = Divide by 1 01 = Divide by 2 10 = Divide by 4 11 = Divide by 8
		FLL_N2																	FLL 10-bit integer VCO divider for FLL Filter Clock
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0x0010**
8	FLL5	PD_DACICTRL																	0 = Disable the drive strength control block of FLL DAC 1 = Enable the drive strength control block of FLL DAC
		CHB_FILTER_EN																	FLL Loop Filter enable to reduce FLL output noise, especially, (DCO frequency)/(FLL input reference frequency) is not a integer 1 = Enable; if enable, two different loop bandwidth can select from 0x9[13:12] 0 = Disable
		CLK_FILTER_SW																	**Select filter clock source selection** 1 = Select Divided VCO Clock based on Reg.FLL_N2 0 = Select REFCLK
		FILTER_SW																	DCO input selection 1 = Select unfiltered output 0 = Select filter output for lower noise performance
																			Set FLL Lock-In Length Sets the time that FLL must stay within the lock-in range before lock signal goes HIGH
		Default	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0xC000**
9	FLL6	DCO_EN																	**FLL Free-Running Mode Enable** 1 = Enable 0 = Disable Need to enable for FLL Free Running Mode
		SDM_EN																	**FLL Sigma Delta Modulator Enable** to create decimal part of frequency, if (DCO frequency)/(FLL input reference frequency) is not a integer . If the ratio is integer, it still can be on for lower noise output but higher power consumption 1 = Enable 0 = Disable
		CUTOFF500																	**FLL 500 Khz Cutoff Frequency Enable** If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give the best FLL performance with highest power consumption 1 = Enable 0 = Disable
		CUTOFF600																	**FLL 600 Khz Cutoff Frequency Enable** If 0x8[14]=1, it sets loop filter cutoff frequency at 600Khz. It will give a moderate FLL performance with moderate power consumption 1 = Enable 0 = Disable
		DLR																	FLL dynamic lock range. 0000 = recommended
		Default	**0**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x6000**
A	FLL_VCO_RSV	DOUT2VCO_RSV																	Set the FLL DCO frequency in free-running mode.
		Default	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**0**	**0xF13C**

10	PCM_CTRL0	ADCCM																	ADC companding mode control 00 = Off (normal linear operation) 01 = Reserved 10 = u-law companding 11 = A-law companding
		CMB8																	8-bit word enable for companding mode of operation 0 = Normal operation (no companding) 1 = 8-bit operation for companding mode
		UA_OFF																	Companding Offset Mode.
		BCP																	Bit clock phase inversion option for BCLK 0 = Normal phase 1 = Input logic sense inverter
		LRP																	Phase control for I2S audio data bus interface 0 = Normal phase operation 1 = Inverted phase operation PCMA and PCMB left/right word order control 0 = MSB is valid on 2nd rising edge of BCLK after rising edge of FS 1 = MSB is valid on 1st rising edge of BCLK after rising edge of FS
		WLEN																	Word length (24-bits default) of audio data stream 00 = 16-bit word length 01 = 20-bit word length 10 = 24-bit word length 11 = 32-bit word length
		AIFMT																	Audio interface data format (default setting is I2S) 00 = Right justified 01 = Left justified 10 = Standard I2S format 11 = PCMA or PCMB audio data format option
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**1**	**0x000B**
11	PCM_CTRL1	DO12_TRI																	ADCDO12 tri state 0 = Normal mode (Check DO12_OE) 1 = Output high Z (DO12 pad output disable)
		DO12_DRV																	ADCDO12 drive enable 0 = Normal mode (check DO12_TRI) 1 = Always out
		LRC_DIV																	LRC DIVIDE Coefficient Setting 00 = BCLK/2^8 (256) 01 = BCLK/2^7 (128) 10 = BCLK/2^6 (64) 11 = BCLK/2^5 (32)
		PCM_TS_EN																	Normal mode(not TDM mode) 1 = Time slot function enable for PCM mode 0 = Only PCM_A_MODE or PCM_B_MODE(STEREO Only) can be used when PCM Mode is selected
		TRI																	normal mode for ADCDAT12 and ADCDAT34 1 = Tri-State the 2nd half of LSB 0 = Drive the full Clock of LSB
		PCM8_BIT																	1 = Select 8-bit word length 0 = Use WLEN to select Word Length
		DO12_PE																	ADCDO12 pin pull-enable Enable (When DO12_TRI=0, set ADCDO12 output pull condition.) 1 = Enable 0 = Disable
		DO12_PS																	ADCDO12 pin pull Up/Down Enable (After DO12_PE=1) 1 = Pull Up 0 = Pull Down
		DO12_OE																	0 = ADCDO12 is output buffer when no data out, ADCDO12 pin becomes high Z 1 = ADCDO12 is output buffer all time
		MS																	Master Mode Enable 0 = Slave Mode 1 = Master Mode
		BCLKDIV																	BCLK DIVIDE Coefficient Setting BCLK=MCLK/BCLKDIV 000 = No Divide 001 = Divided 2 010 = Divided 4 011 = Divided 8 100 = Divided 16 101 = Divided 32
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0x0002**
		DO34_TRI																	ADCDO34 tri state

12	PCM_CTRL2																		0 = Normal mode (Check DO34_OE) 1 = Output high Z (DO34 pad output disable)
		DO34_DRV																	ADCDO34 drive enable 0 = Normal mode (check DO34_TRI) 1 = Always out
		DO34_PE																	ADCDO34 pin pull-enable Enable (When DO34_TRI=0, set ADCDO34 output pull condition.) 1 = Enable 0 = Disable
		DO34_PS																	ADCDO34 pin pull Up/Down Enable (After DO34_PE=1) 1 = Pull Up 0 = Pull Down
		DO34_OE																	0 = ADCDO34 is not always out (when no data out, ADCDO34 pin becomes high Z) 1 = ADCDO34 always out
		TSLOT_L																	ADC1, ADC3 PCM time slot start value when PCM_TS_EN =1, both TSLOT_L0 and TSLOT_R0 need to set different values: N*WordLength+1 Or PCM TDM Offset Mode Slot start value when in PCM_CTRL4 both TDM and PCM_OFFSET_MODE_CTRL both are 1 Shift value= N*WordLength+1. 4 channels will shift together and need have enough channels available > 4 channels
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
13	PCM_CTRL3	FS_ERR_CMP_SE																	Triggers short Frame Sync signal if Frame Sync is less than 00 = 255*MCLK 01 = 253*MCLK 10 = 254*MCLK 11 = 255*MCLK
		DIS_FS																	0 = Enable short frame sync detection logic 1 = Disable short frame sync detection logic
		TSLOT_R																	ADC2, ADC4 output channel PCM time slot start value when PCM_TS_EN =1 both TSLOT_L0 and TSLOT_R0 need to set different values: N*WordLength+1 And unused for PCM TDM Offset Mode
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
14	PCM_CTRL4	TDM_MODE																	1 = TDM mode 0 = Normal mode
		TDM_OFFSET_EN																	PCM Time slots under TDM mode 1 = Time slot function enable for PCM mode
		ADC_TXEN																	ADC TX out enable for channel 1,2,3,4 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
20	ALC_CONTROL_1	ALCTABLESEL																	0 = ALC target range -28.5~ -6dB 1 = ALC target range -22.5 ~-1.5dB
		ALC_GRP[2:0]																	000=Channel 1234 are independent 001 = Channel 12 as one group, channel 1 as target. Channel34 are independent 010 = Channel 34 grouped, channel 3 as target. Channel12 are independent 011= Channel 12 as a group; channel34 as a group. Channel 1, 3 is target respectively. 100 = channel 1234 group, channel 1 as target
		ALC_NG_ADJ																	1= Enable ALC Noise Gate adjustment 0= Default
		ALC_PK_DET_HOLD																	peak detect hold 1 = Keep peak 0 = Peak decay
		ALC_PKDET_CLR																	1 = If peak hold is "1" clear peak value 0 = Don't clear
		ALC_MODE																	1 = Limiter mode 0 = Normal mode
		ALC_PK_LIM_EN																	
		ALC_NGSEL																	0 = Use peak_peak calculation output for noise gate threshold 1 = Use rectified peak detector output for noise gate threshold
		ALC_PKSEL																	1 = Use peak_peak calculation 0 = Use rectified peak detector
		ALC_NGEN																	1= enable ALC NG

		ALC_NGTH																	ALC noise gate threshold level 0000 = -19dB 0001 = -23.5dB 0010 = - 28dB ▼ steps = -4.5dB ▼ 1110 = -82dB 1111 = -86.5dB
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0x0070**
21	ALC_CONTROL_2	ALCMAX																	Maximum ALC gain setting 000 = -6.75 dB 001 = -0.75 dB 010 = +5.25 dB 011 = +11.25 dB 100 = +17.25 dB 101 = +23.25 dB 110 = +29.25 dB 111 = +35.25 dB
		ALCMIN																	Minimum ALC gain setting 000 = -12 dB 001 = -6 dB 010 = 0 dB 011 = +6 dB 100 = +12 dB
		ALCHLD																	Hold time before ALC automated gain increase 0000 = 0.00ms (default) 0001 = 2.00ms 0010 = 4.00ms ▼ - time value doubles with each bit value increment ▼ 1001 = 512ms 1010 through 1111 = 1000ms
		ALCLVL																	ALC target level ALCTABLESEL = 0 / 1 0000 -28.5 dBFS -22.5 dBFS 0001 -27 dBFS -21 dBFS 0010 -25.5 dBFS -19.5 dBFS 0011 -24 dBFS -18 dBFS 0100 -22.5 dBFS -16.5 dBFS 0101 -21 dBFS -15 dBFS 0110 -19.5 dBFS -13.5 dBFS 0111 -18 dBFS -12 dBFS 1000 -16.5 dBFS -10.5 dBFS 1001 -15 dBFS -9 dBFS 1010 -13.5 dBFS -7.5 dBFS 1011 -12 dBFS -6 dBFS 1100 -10.5 dBFS -4.5 dBFS 1101 -9 dBFS -3 dBFS 1110 -7.5 dBFS -1.5 dBFS 1111 -6 dBFS -1.5 dBFS
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
22	ALC_CONTROL_3	ALC_CH4EN																	1 = Channel 4 ALC enable 0 = Disable
		ALC_CH3EN																	1 = Channel 2 ALC enable 0 = Disable
		ALC_CH1EN																	1 = Channel 2 ALC enable 0 = Disable
		ALC_CH1EN																	1 = Channel 1 ALC enable 0 = Disable
		ALCDCY																	ALC Decay Timer (0.75dB / adjustment step) Normal Mode: 0000 = 500 us / step 0001 = 1 ms / step 0010 = 2 ms / step ▼ - each subsequent setting doubles the decay timer ▼ 1001 = 256 ms / step 1010 = 512 ms / step Limiter Mode: 0000 = 125 us / step 0001 = 250 us / step 0010 = 500 us / step

																			▼ - each subsequent setting doubles the decay timer ▼ 1001 = 64 ms / step 1010 = 128 ms / step
		ALCTK																	ALC Attack Timer (0.75dB / adjustment step) Normal Mode: 0000 = 125 us / step 0001 = 250 us / step 0010 = 500 us / step ▼ - each subsequent setting doubles the decay timer ▼ 1001 = 64 ms / step 1010 = 128 ms / step Limiter Mode: 0000 = 31 us / step 0001 = 63 us / step 0010 = 125 us / step ▼ - each subsequent setting doubles the decay timer ▼ 001 = 16 ms / step 1010 = 32 ms / step
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
23	ALC_CONTROL_4	ALC_UPEN_CH2																	1 = Channel 2 Gain Update Enable 0 = Disable
		ALC__ZCD_CH2																	1 = Channel 2 ALC Gain updates on zero crossing. 0 = Channel 2 ALC Gain updates whenever
		ALC_INIT_GAIN_CH2																	Channel 2 Initial Gain. Increments in .75dB steps 000000 = -12dB 000001 = -11.25dB ▼ 010000 = 0dB ▼ 111111 = 35.25dB
		ALC_UPEN_CH1																	1 = Channel 1 Gain Update Enable 0 = Disable
		ALC__ZCD_CH1																	1 = Channel 1 ALC Gain updates on zero crossing. 0 = Channel 1 ALC Gain updates whenever
		ALC_INIT_GAIN_CH1																	Channel 1 Initial Gain. Increments in .75dB steps 000000 = -12dB 000001 = -11.25dB ▼ 010000 = 0dB ▼ 111111 = 35.25dB
		Default	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0x1010**
24	ALC_CONTROL_5	ALC_UPEN_CH4																	1 = Channel 4 Gain Update Enable 0 = Disable
		ALC__ZCD_CH4																	1 = Channel 4 ALC Gain updates on zero crossing. 0 = Channel 4 ALC Gain updates whenever
		ALC_INIT_GAIN_CH4																	Channel 4 Initial Gain. Increments in .75dB steps 000000 = -12dB 000001 = -11.25dB ▼ 010000 = 0dB ▼ 111111 = 35.25dB
		ALC_UPEN_CH3																	1 = Channel 3 Gain Update Enable 0 = Disable
		ALC__ZCD_CH3																	1 = Channel 3 ALC Gain updates on zero crossing. 0 = Channel 3 ALC Gain updates whenever
		ALC_INIT_GAIN_CH3																	Channel 3 Initial Gain. Increments in .75dB steps 000000 = -12dB 000001 = -11.25dB ▼ 010000 = 0dB ▼ 111111 = 35.25dB
		Default	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0x1010**
2D	ALC_GAIN_CH12																		Reserved
		ALC_GAIN_CH2																	Readout channel 2 ALC gain setting

		ALC_GAIN_CH1																	Readout channel 1 ALC gain setting
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
2E	ALC_GAIN_CH34																		Reserved
		ALC_GAIN_CH4																	Readout channel 4 ALC gain setting
		ALC_GAIN_CH3																	Readout channel 3 ALC gain setting
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
2F	ALC_STATUS	FAST_DEC																	
		NOISE																	
		CLIP																	
		Default	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	**Read Only**
30	NOTCH_FIL1_CH1	NFU1																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
		NFEN																	Notch filter control bit 0 = Disabled 1 = Enabled
		NFA0																	Notch filter A0 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
31	NOTCH_FIL2_CH1	NFU2																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
																			Reserved
		NFA1																	Notch filter A1 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
32	NOTCH_FIL1_CH2	NFU1																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
		NFEN																	Notch filter control bit 0 = Disabled 1 = Enabled
		NFA0																	Notch filter A0 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
33	NOTCH_FIL2_CH2	NFU2																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do Nothing
																			Reserved
		NFA1																	Notch filter A1 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
34	NOTCH_FIL1_CH3	NFU1																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
		NFEN																	Notch filter control bit 0 = Disabled 1 = Enabled
		NFA0																	Notch filter A0 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
35	NOTCH_FIL2_CH3	NFU2																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
																			Reserved
		NFA1																	Notch filter A1 coefficient least significant bits.
		Default	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	**0x0000**
36	NOTCH_FIL1_CH4	NFU1																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
		NFEN																	Notch filter control bit 0 = Disabled 1 = Enabled
		NFA0																	Notch filter A0 coefficient least significant bits.

		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
37	NOTCH_FIL2_CH4	NFU2																	Update bit feature for simultaneous change of all notch filter parameters. Write-only bit. 1 = Update 0 = Do nothing
																			Reserved
		NFA1																	Notch filter A1 coefficient least significant bits.
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
38	HPF_FILTER_CH12	FLUSH_MEM																	1 = flush filter memory
		HPF_EN_CH2																	Channel 2 HPF filter control bit 0 = Disabled 1 = Enabled
		HPF_AM_CH2																	Select audio mode or application mode. 0 = Audio mode (1st order, fc = ~3.7Hz). 1 = Application mode (2nd order, fc = HPFCUT, reference TABLE 1,)
		HPF_CUT_CH2																	Channel 2 HPF Cut-off Frequency, reference TABLE 1
		HPF_EN_CH1																	Channel 1 HPF filter control bit 0 = Disabled 1 = Enabled
		HPF_AM_CH1																	Select audio mode or application mode. 0 = Audio mode (1st order, fc = ~3.7Hz). 1 = Application mode (2nd order, fc = HPFCUT, reference TABLE 1)
		HPF_CUT_CH1																	Channel 1 HPF Cut-off Frequency, reference TABLE 1
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
39	HPF_FILTER_CH34	HPF_EN_CH4																	Channel 4 HPF filter control bit 0 = Disabled 1 = Enabled
		HPF_AM_CH4																	Select audio mode or application mode. 0 = Audio mode (1st order, fc = ~3.7Hz). 1 = Application mode (2nd order, fc = HPFCUT, reference TABLE 1,)
		HPF_CUT_CH4																	Channel 4 HPF Cut-off Frequency. reference TABLE 1 for more details.
		HPF_EN_CH3																	Channel 3 HPF filter control bit 0 = Disabled 1 = Enabled
		HPF_AM_CH3																	Select audio mode or application mode. 0 = Audio mode (1st order, fc = ~3.7Hz). 1 = Application mode (2nd order, fc = HPFCUT, reference TABLE 1)
		HPF_CUT_CH3																	Channel 3 HPF Cut-off Frequency. reference TABLE 1 for more details
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
3A	ADC_SAMPLE_RATE	Channel_sync																	Channels time alignment bit. When it is enabled, All 4 channels have timing alignment output when all 4 channels have same input during NAU85L40 startup or reset. 0 = Disabled 1 = Enabled
		SMPL_RATE																	ADC Sample Rate selection for HPF coefficients: 000 = 48kHz/96kHz 001 = 32kHz 010 = 24kHz 011 = 16kHz 100 = 12kHz 101 = 8kHz 110=96kHz
		SINC4																	Reserved keep 0
		GAIN_CMP																	Reserved keep 0
		OSR384																	Reserved keep 0
		OSR																	ADC OSR selection. Controls SINC filter down sample ratio. Must be set such that ADC_CLK = Fs * OSR. 00 = 32 01 = 64 (When Fs=96KHZ, it gets better THD.) 10 = 128 11 = 256.
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0x0002**

40	DIGITAL_GAIN_CH1	CH1_DGAIN																	ADC channel 1 digital gain. Increments in -0.125dB steps 0x520 = + 36dB 0x400 = 0dB ▼ 0x000 = -128dB
		Default	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0400**
41	DIGITAL_GAIN_CH2	CH2_DGAIN																	ADC channel 2 digital gain. Increments in -0.125dB steps 0x520 = + 36dB 0x400 = 0dB ▼ 0x000 = -128dB
		Default	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x1400**
42	DIGITAL_GAIN_CH3	CH3_DGAIN																	ADC channel 3 digital gain. Increments in -0.125dB steps 0x520 = + 36dB 0x400 = 0dB ▼ 0x000 = -128dB
		Default	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x2400**
43	DIGITAL_GAIN_CH4	CH4_DGAIN																	ADC channel 4 digital gain. Increments in -0.125dB steps 0x520 = + 36dB 0x400 = 0dB ▼ 0x000 = -128dB
		Default	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0400**
44	DIGITAL_MUX	DG_ZCEN																	Digital Gain change zero cross enable 1 = Enable 0 = Disable
		CH4_SEL																	Channel MUX ADC output selection 00 = ADC channel 1 IN 01 = ADC channel 2 IN 10 = ADC channel 3 IN 11 = ADC channel 4 IN
		CH3_SEL																	
		CH2_SEL																	
		CH1_SEL																	
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**1**	**1**	**0**	**0**	**1**	**0**	**0**	**0x00E4**
48	P2P_CH1	P2P CH1																	Channel 1 P2P value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
49	P2P_CH2	P2P CH2																	Channel 2 P2P value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4A	P2P_CH3	P2P CH3																	Channel 3 P2P value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4B	P2P_CH4	P2P CH4																	Channel 4 P2P value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4C	PEAK_CH1	PEAK CH1																	Channel 1 Peak value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4D	PEAK_CH2	PEAK CH2																	Channel 2 Peak value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4E	PEAK_CH3	PEAK CH3																	Channel 3 Peak value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
4F	PEAK_CH4	PEAK CH4																	Channel 4 Peak value.
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
50	GPIO_CTRL	POL																	GPIO polarity
		SEL																	GPIO output source selection 00=GPIO clock 01=FLL lock 10=1 10=0
		DIR																	GPIO direction 1=output 0=input
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
51	MISC_CTRL	SPI3_EN																	Mode pin = 0 1 disable SPI3 0 enable SPI3 Mode pin = 1 I2C mode regardless
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**

52	I2C_CTRL	TO_DIS																	I2C time out function 1 = Disable 0 = Enable
		TIMEOUT																	
		Default	**0**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0xEFFF**
58	I2C_DEVICE_ID	I2C_DEVID																	I2C device ID address
		SI_REV																	Silicon Revision is F1
		Default	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**X**	**Read Only**
5A	RST	SW_RST																	Software reset without reset of register contents.
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
60	VMID_CTRL	TEST																	
		VMIDEN																	VMID 0 = Disable 1 = Enable
		VMIDSEL																	Vmid tie-off selection options 00 = open (default) 01 = 50kΩ resistors 10 = 250kΩ resistors 11 = 5kΩ resistors
		BIAS_ADJ																	Master bias current power reduction options 00 = normal operation (default) 01 = 10% reduced bias current from default 10 = 17% reduced bias current from default 11 = 10% increased bias current from default
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
61	MUTE	MUTE CH4																	MIC4 PGA mute enable 0 = Mute Disable 1 = Mute Enable
		MUTE CH3																	MIC3 PGA mute enable 0 = Mute Disable 1 = Mute Enable
		MUTE CH2																	MIC2 PGA mute enable 0 = Mute Disable 1 = Mute Enable
		MUTE CH1																	MIC1 PGA mute enable 0 = Mute Disable 1 = Mute Enable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
64	ANALOG_ADC1	resetR																	Reset integrators in ADC CH4...1 1 = Reset 0 = Normal operation
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
65	ANALOG_ADC2	adc_up																	Channel 4 to 1 PGA bias current increase for driving the ADC at high sample rates
		bias1																	Change bias currents in ADC 00 = Nominal
		bias0																	01 = Double 10 = Half 11 = Quarter of nominal value
		Vrefsel1																	Change Vref in ADC: 00 = Use analog supply
		Vrefsel0																	01, 10, 11 use internal value derived from Vmid, value changes in 0.5dB steps
																			Reserved
																			Reserved
		lfsrresetn																	0 = Reset the LFSR for the DEM algorithm 1 = Default
		monadd																	Should remain zero.
		mon1st																	
		mon2nd																	
		mon3rd																	
		mon4th																	
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0x0020**
66	ANALOG_PWR	PON_CH4																	1 = Power on signal ADC CH1 to CH4
		PON_CH3																	
		PON_CH2																	
		PON_CH1																	
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
67	MIC_BIAS	PU_BUF																	Micbias were driven by two stages output buffers; MICBIAS 2nd stage output buffers

																			Bit 1 = MICBIAS2 Bit 0 = MICBIAS1 1 = Power on 0 = Power off
		PU_PRE																	MICBIAS power on 1st stage output buffers (pre-amplifier) 1 = Enable 0 = Disable
		FAST																	MICBIAS fast charge filter 1 = Enable 0 = Disable
		DISCH																	MICBIAS discharge filter 1 = Enable 0 = Disable
		LVL_LOW																	MICBIAS Set output level 1.8V 1 = Enable 0 = Disable
		LVL																	MICBIAS Set output level 000 = 2.1V 001 = 2.2V 010 = 2.3V 011 = 2.4V 100 = 2.5V 101 = 2.6V 110 = 2.7V 111 = 2.8V
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0x0004**
68	REFERENCE	STG2_SEL																	Enable PGA class A mode of operation (instead of class AB) 1 = Enable 0 = Class AB
		PDVMDFST																	Power Down Fast VREF Ramp up 1 = Disable 0 = Enable
		BIASEN																	Enable Global Analog Bias enable /Bias/power management 1 = Enable 0 = Disable
		DISCHRG																	Charge inputs selected by FEPGA2: ACDC_CTRL[7:0] to VREF 1 = Enable 0 = Disable
		BYPASS_IBCTR																	Bypass PGA current control 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
69	FEPGA1	CM_LCK																	Common mode Threshold lock adjust
		IB_LOOP																	PGA Current Trim
		IBCTR_CODE																	PGA Current Trim
		MODE_CH2																	Channel 2 PGA mode selection; MODE_CH2[0] = Anti-aliasing filter adjust when Fs<=16KHz MODE_CH2[1] = Disconnects MICP & MICN from FEPGA MODE_CH2[2] = No function MODE_CH2[3] = Shorts the inputs to ground with 12kOhm differentially terminated 1 = Enable 0 = Disable
		MODE_CH1																	Channel 1 PGA mode selection; MODE_CH1[0] = Anti-aliasing filter adjust when Fs<=16KHz MODE_CH1[1] = Disconnects MICP & MICN from FEPGA MODE_CH1[2] = No function MODE_CH1[3] = Shorts the inputs to ground with 12kOhm differentially terminated 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
6A	FEPGA2	ACDC_CTRL																	DC state control for Input pins. Action takes effect when DISCHRG=1 ACDC_CTRL[0] charges MIC1P to VREF ACDC_CTRL[1] charges MIC1N to VREF ACDC_CTRL[2] charges MIC2P to VREF ACDC_CTRL[3] charges MIC2N to VREF ACDC_CTRL[4] charges MIC3P to VREF ACDC_CTRL[5] charges MIC3N to VREF ACDC_CTRL[6] charges MIC4P to VREF ACDC_CTRL[7] charges MIC4N to VREF

																			1 = Enable 0 = Disable
		MODE_CH4																	Channel 4 PGA mode selection; MODE_CH1[0] = Anti-aliasing filter adjust when Fs<=16KHz MODE_CH1[1] = Disconnects MICP & MICN from FEPGA MODE_CH1[2] = No function MODE_CH1[3] = Shorts the inputs to ground with 12kOhm differentially terminated 1 = Enable 0 = Disable
		MODE_CH3																	Channel 3 PGA mode selection; MODE_CH1[0] = Anti-aliasing filter adjust when Fs<=16KHz MODE_CH1[1] = Disconnects MICP & MICN from FEPGA MODE_CH1[2] = No function MODE_CH1[3] = Shorts the inputs to ground with 12kOhm differentially terminated 1 = Enable 0 = Disable
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**
6B	FEPGA3	GAIN_CH2																	Channel 2 PGA Gain. Increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = +35dB 100101 = +36dB
		GAIN_CH1																	Channel 1 PGA Gain. Increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = +35dB 100101 = +36dB
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0x0101**
6C	FEPGA4	GAIN_CH4																	Channel 4 PGA Gain. Increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = +35dB 100101 = +36dB
		GAIN_CH3																	Channel 3 PGA Gain. Increments in 1dB steps 000000 = -1dB 000001 = 0dB ▼ 100100 = +35dB 100101 = +36dB
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0x0101**
6D	PWR	PUP																	Power Up Channel 4 to 1 PGA
		Default	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0x0000**

8 Typical Application Diagram

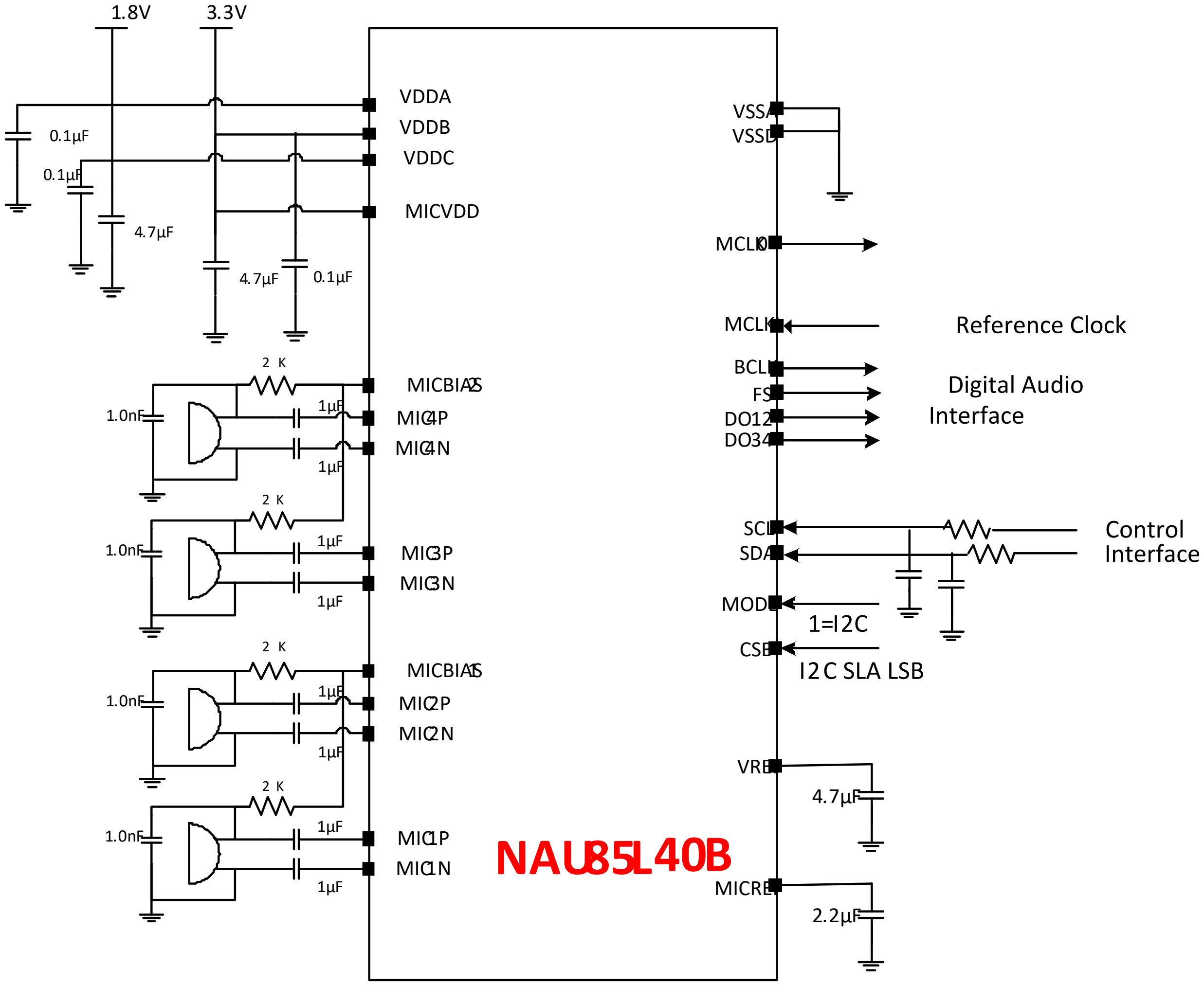


Figure 28: Typical Single-ended use Application Diagram

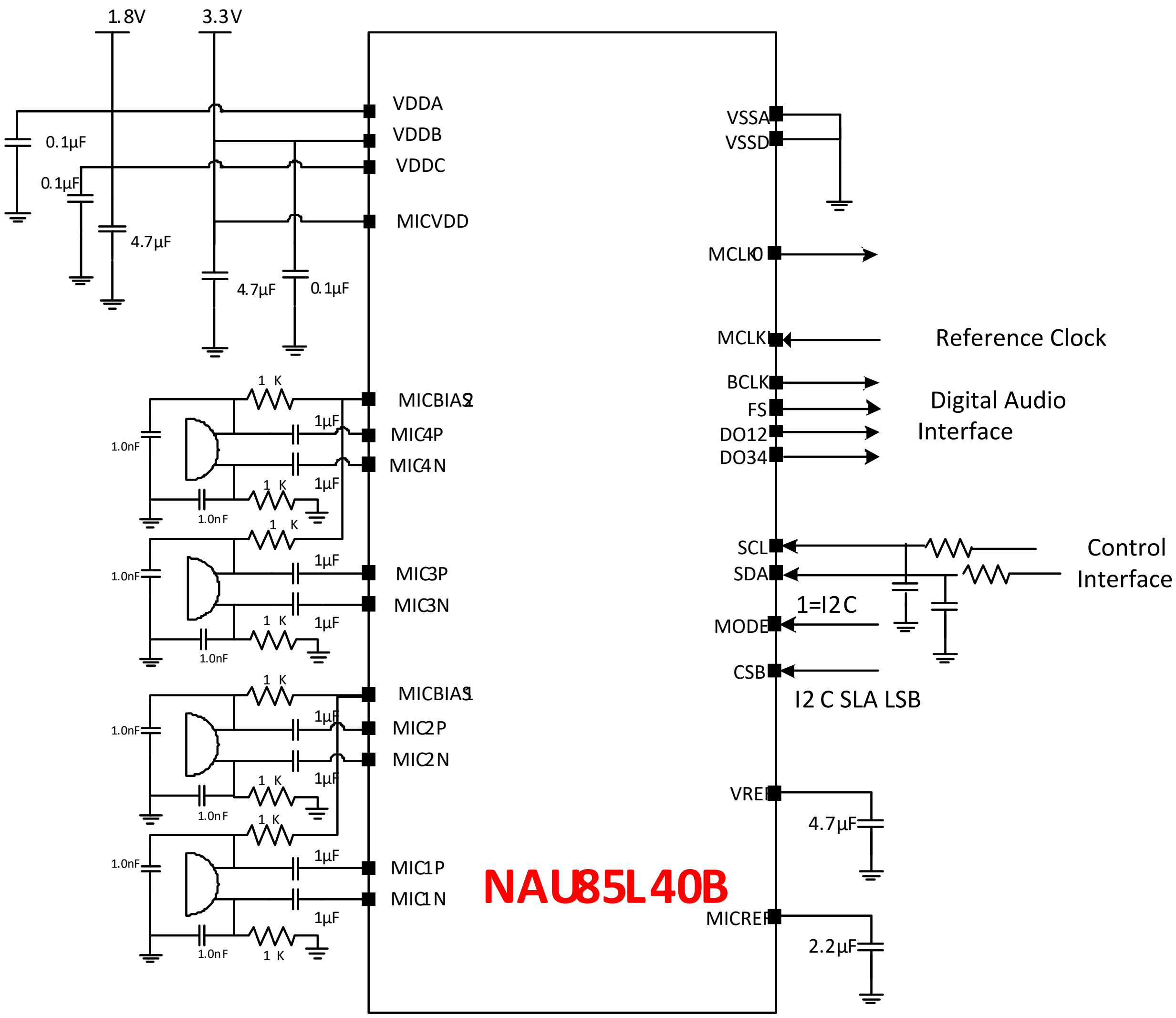
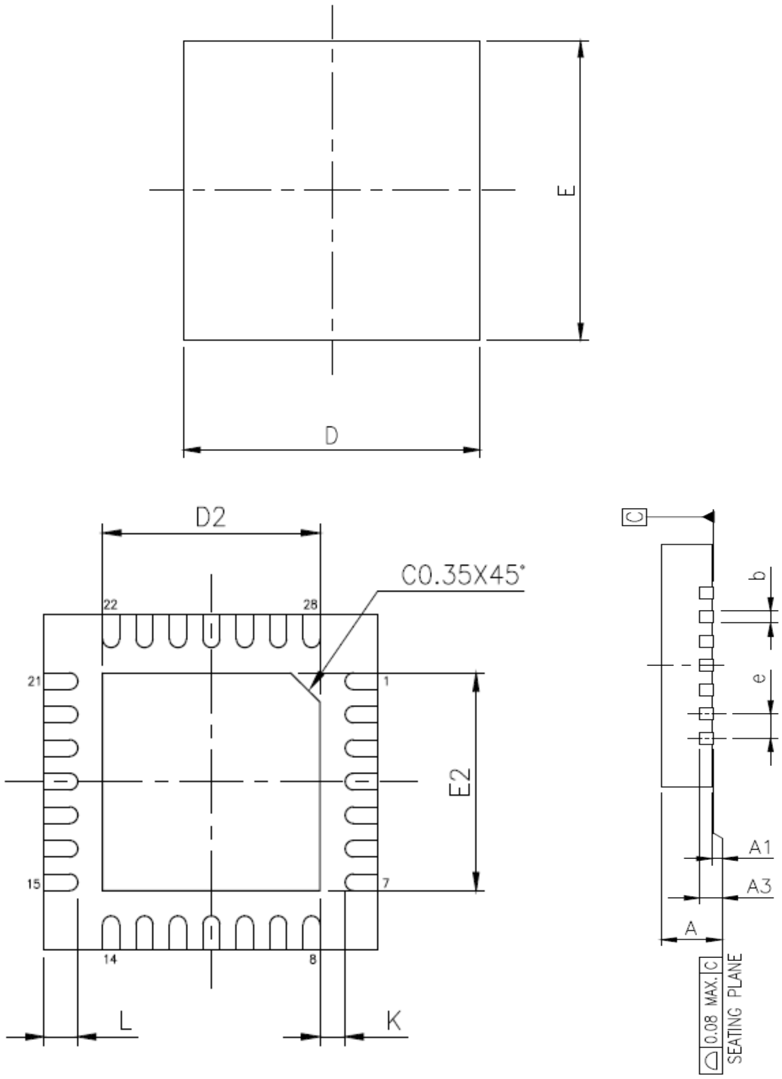


Figure 29: Typical Application Schematic for Differential Microphone Connection

Note: SCL and SDA can add a low pass filter as shown above to reduce glitch. The corner frequency is 8Mhz to 33Mhz for the low pass filter.

9 Package Information

QFN 28L 4X4 mm^2,Thickness:0.8 mm(Max), Pitch:0.40 mm EP SIZE 2.6X2.6 mm



PKG CODE	QFN 28L		
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.15	0.20	0.25
D	4.00 BSC		
E	4.00 BSC		
e	0.40 BSC		
K	0.20	—	—
D2	2.55	2.60	2.65
E2	2.55	2.60	2.65
L	0.30	0.40	0.50

10 ORDERING INFORMATION

Part Number	Dimension	Package	Package Material
NAU85L40YGB	4x4 mm	QFN-28	Green

NAU88L40_ _B

Package Material:

G = Green Package (Halogen-free, RoHS-compliant) & TSCA-compliant

Package Type:

Y = QFN-28

11 REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0	Nov 05,2014	Update AC/DC parameters
1.1	Aug 6, 2015	VHI, Update REG0X11, 12
1.1.1	Sep 9, 2015	Figure 1 description change, Reg10, 69,6A description
1.1.2	Oct 1, 2015	Add PRO Reset application note
1.1.3	Oct 9, 2015	Add VDDB restriction
1.1.4	Oct 14 2015	Revise package information
1.1.5	Oct 21, 2015	Figure.7 change noise gate from -19dB to -39dB
1.1.6	Dec 1, 2015	Register 23, 24 change default setting 0x1010
1.1.7	Jan 22, 2016	Figure 11, SYSCLK_SRC Update shutdown current Reg0x12[9:0] & Reg0x13[9:0]
1.1.8	Apr 26, 2016	Resistor values added Reg0x20 description added Update Fig.7
1.1.9	Jun 6, 2016	Table 7, Figure 10 Corrected Reg0x6, Reg0x11[13:12] Fig.9 changed Reg0x12&13 Time slot description Add Note Fig 11, FLL equation 1 &example change
1.2	Feb 16, 2017	Sec 3.1 description error Add description for Reg0x2[15] Add 6.7 audio Interface timing diagram
1.3	Apr 4, 2017	Change to revision B, updated THD and SNR values
1.4	Jul 31, 2017	Update 0x3A [14] register description
1.5	Aug 25, 2017	Add fs=96KHz, SMPL_RATE 0x3A[7:5]
1.6	Jul 30, 2018	Register 58 SI_rev added F1 as revision number Register 51[15] description correction Add low pass filter in Fig 28 and Fig 29
1.7	Jan 17, 2020	Add FLL application note

1.8	Dec 18, 2020	Add GPIO description
1.9	Jan 28, 2021	Add Audio format timing parameters
2.0	Mar 10, 2021	Add FS_{ADC} limit
2.1	Mar 18, 2021	Change FS_{ADC} limit
2.2	Mar 30, 2021	Change FS_{ADC} description
2.3	Aug 4, 2022	Section 6.7 updated diagram and timing data Reg11[4] DO12_OUT ADC output description Reg20[11] ALC_NG_ADJ Reg61[11:10] and Reg61[8] MIC_BIAS description
2.4	Feb 1, 2023	Update Halogen-free, RoHS-compliant and TSCA-compliant description

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