NuMicro® Family

Arm® Cortex®-M4-based Microcontroller

M463/M467 Series
Datasheet

For additional information or questions, please contact: Nuvoton Technology Corporation.

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1 GENERAL DESCRIPTION

The NuMicro M463/M467 series is a 32-bit microcontroller based on Arm Cortex-M4F core, with DSP instruction set and single-precision floating-point unit (FPU), targeted for IoT, Industrial, and consumer applications. The M463/M467 series runs up to 200 MHz, and features 1.7 V to 3.6 V wide operating voltage, -40 °C to 85 °C /105°C wide operating temperature, a variety of packages choice, and excellent high immunity characteristics by ESD HBM 2 KV and EFT 4.4 KV.

As the new smart function added on home appliances, the M463/M467 series provides up to 1024 KB dual-bank of Flash memory for code storage and 512 KB SRAM for run time operation. The dual bank design of 1024 KB Flash memory supports the Firmware update through the Over-The-Air (FOTA) process. Additionally, in response to the code security requirements, the M463/M467 series supports Execute-Only Memory (XOM) function to protect confidential program code information from stealing in the run-time. In order to reduce the data access overhead of CPU core to peripherals, up to 32 channels of peripheral direct memory access (PDMA) is provided.

The M463/M467 series supports plenty of peripherals, including Ethernet 10/100 MAC, hardware crypto engine, key store, true random number generator (TRNG), programmable audio PLL, HyperBus interface, 4 sets of CAN FD, USB HS OTG, USB FS OTG, up to 24 channels of 16-bit PWM, 10 sets of UART, 4 sets of SPI/I^{2}S, 2 sets of Quad-SPI, 5 sets of I^{2}C, 1 set of USCI, 1 set of PSIO, 4 sets of EQEI and a real-time clock (RTC).

The M463/M467 series also provides rich analog peripherals including 4 sets of analog comparators, up to 28 channels of 12-bit SAR ADC, and 2 channels of 12-bit DAC.

For the development, Nuvoton provides the NuMaker-M467HJ, NuMaker-M463KG evaluation board, and Nuvoton Nu-Link debugger. The 3rd Party IDE such as Keil MDK, IAR EWARM, Eclippse IDE with GNU GCC compilers are also supported.

Product Line	Core (MHz)	Ethernet	Crypto + TRNG	CAN FD	USB OTG	HBI	EBI	UART	I^{2}C	QSPI/SPI	PWM	ADC	DAC	ACMP	EQEI
M463 Series	200	-	√	2	HS x1	-	√	8+1	5	SPI x4 QSPI x2	24	16	-	2	2
M467 Series	200	√	√	4	HS x1 FS x1	√	√	10+3	5	SPI x4 QSPI x2	24	28	2	4	4

This series supports five package choices which are designed for home appliance PCB demands.

- QFN48 w/ EPAD: 5 mm x 5 mm, Load pitch: 0.35 mm
- LQFP48: Body Size 7 mm x 7 mm, Load Pitch 0.5 mm
- LQFP64: Body Size 7 mm x 7 mm, Load Pitch 0.4 mm
- LQFP128: Body Size 14 mm x 14 mm, Load Pitch 0.4 mm
- LQFP144: Body Size 20 mm x 20 mm, Load Pitch 0.5 mm
- LQFP176: Body Size 24 mm x 24 mm, Load Pitch 0.5 mm

The NuMicro M463/M467 series is suitable for a wide range of applications such as:

- IoT Gateway
- Industrial Control
- Telecom
- Data Center

2 FEATURES

2.1 M463/M467 Series Features

Core and System	
ARM Cortex-M4	• Arm Cortex-M4 processor, running up to 200 MHz • Built-in Memory Protection Unit (MPU) • Built-in Nested Vectored Interrupt Controller (NVIC) • Hardware IEEE 754 compliant Floating-point Unit (FPU) • DSP extension with hardware divider and single-cycle 32-bit hardware multiplier • 24-bit system tick timer • Programmble and maskable interrupt • Low Power Sleep mode by WFI and WFE instructions
Brown-out Detector (BOD)	• Eight-level BOD with brown-out interrupt and reset option
Low Voltage Reset (LVR)	• LVR with 1.5V threshold voltage level
Security	• 96-bit Unique ID (UID) • 128-bit Unique Customer ID (UCID)
Memories	
Boot Loader	• Factory pre-loaded mask ROM for secure boot procedure and ISP procedure • Uses SHA-256 and ECDSA-P256 to validate data in APROM and LDROM • NuMicro ISP Programming Tool for firmware upgrade via UART, CAN FD, SPI, I^2C and high speed USB device
Flash	• Up to 1024 Kbytes on-chip Application ROM (APROM) • Dual bank 1024 Kbytes APROM for Over-The-Air (OTA) upgrade • Four eXecute-Only-Memory (XOM) regions for code protection • Embedded with 4 Kbytes cache, with performance at zero wait cycle in continuous address read access • 8 Kbytes on-chip Flash for user-defined loader (LDROM) • 3 Kbytes One Time Programmable (OTP) ROM for data security • All on-chip Flash support 4 Kbytes page erase • Fast Flash programming verification with CRC32 • On-chip Flash programming with In-Chip Programming (ICP), In-System Programming (ISP) and In-Application Programming (IAP) capabilities • Configurable boot up sources including boot loader, user-defined

	loader (LDROM) or Application ROM (APROM) • Data Flash with configurable memory size • 2-wired ICP Flash updating through SWD interface • 32-bit/64-bit and multi-word Flash programming function
SRAM	• Up to 512 Kbytes on-chip SRAM includes: 128 Kbytes SRAM located in bank 0 with programmable size of SPD retention The first 64 Kbytes supports hardware parity check; Exception (NMI) generated upon a parity check error 128 Kbytes SRAM located in bank 1 with SPD retention 256 Kbytes SRAM located in bank 2 that can be used as cache for external SPI Flash memory • Supports byte-, half-word- and word-access • PDMA operation
Cyclic Redundancy Calculation (CRC)	• Supports 8-bits, 16-bits and 32-bits configurable polynomials, CRC-CCITT, CRC-8, CRC-16 and CRC-32 polynomials included • Programmable initial value • Supports order reverse setting and one's complement setting for input data and CRC checksum • Supports 8-bit, 16-bit, and 32-bit data width • Supports using PDMA to write data to perform CRC operation
Peripheral DMA (PDMA)	• Up to 32 independent and configurable channels for automatic data transfer between memories and peripherals • Basic and Scatter-Gather transfer modes • Each channel supports circular buffer management using Scatter-Gather Transfer mode • Stride function for rectangle image data movement • Supports Fixed-priority and Round-robin priority modes • Single and burst transfer types • Byte-, half-word- and word tranfer unit with count up to 65536 • Incremental or fixed source and destination address
Clocks	
External Clock Source	• 4~24 MHz High-speed eXternal crystal oscillator (HXT) for precise timing operation • 32.7688 kHz Low-speed eXternal crystal oscillator (LXT) for RTC function and low-power system operation • Supports clock failure detection for external crystal oscillators and exception generation (NMI)
Internal Clock Source	• 48 MHz High-speed Internal RC oscillator (HIRC48) for crystal-less USB

	• 12 MHz High-speed Internal RC oscillator (HIRC) can optionally be used as a system clock • 10 kHz Low-speed Internal RC oscillator (LIRC) for watchdog timer and wakeup operation • Up to 400 MHz on-chip PLL, sourced from HIRC or HXT, allowing CPU operation up to the maximim CPU frequency without the need for a high-frequency crystal • Programmable Audio PLL (PLLFN), sourced from HIRC or HXT
Real-Time Clock (RTC)	• Real-Time Clock with a separate power domain and independent V_{BAT} pin • Supports 80 bytes of battery-powered backup registers, which can be cleared by tamper pins • Supports 6 static and dynamic tamper pins • Able to wake up CPU from any reduced power mode • Supports frequency compensation of RTC clock source • Supports Alarm registers (second, minute, hour, day, month, year) • Supports RTC Time Tick and Alarm Match interrupt • Automatic leap year recognition • Supports 1 Hz clock output for calibration
Timers	
32-bit Timer	**TIMER** • Four sets of 32-bit timers with 24-bit up counter and one 8-bit pre-scale counter from independent clock source • One-shot, Periodic, Toggle-output and Continuous Counting operation modes • Supports event counting function to count the event from external pins • Supports external capture pin for interval measurement and resetting 24-bit up counter • Supports chip wake-up function, if a timer interrupt signal is generated **PWM** • Eight 16-bit PWM counters with 12-bit clock prescale • Supports 12-bit deadband (dead time) • Up, down or up-down PWM counter type • Supports brake function • Supports mask function and tri-state output for each PWM channel
Enhanced PWM (EPWM)	• Twelve 16-bit counters with 12-bit clock prescale for twelve 200 MHz PWM output channels • Up to 12 independent input capture channels with 16-bit resolution counter

	• Supports dead time with maximum divided 12-bit prescale • Up, down or up-down PWM counter type • Supports complementary mode for 3 complementary paired PWM output channels • Synchronous function for phase control • Counter synchronous start function • Brake function with auto recovery mechanism • Mask function and tri-state output for each PWM channel • Trigger EADC or DAC to start conversion immediately • Trigger EADC to start conversion after a short delay • Supports External Pin Trigger Function
Basic PWM (BPWM)	• Two 16-bit counters with 12-bit clock prescale for twelve 200 MHz PWM output channels • Up to 6 independent input capture channels with 16-bit resolution counter • Up, down or up-down PWM counter type • Counter synchronous start function • Complementary mode for 3 complementary paired PWM output channels • Mask function and tri-state output for each PWM channel • Able to trigger EADC to start conversion
Watchdog	• 18-bit free running up counter for WDT time-out interval • Supports multiple clock sources from LIRC (default selection), HCLK/2048 and LXT with 8 selectable time-out period • Able to wake up system from Power-down or Idle mode • Time-out event to trigger interrupt or reset system • Supports four WDT reset delay periods, including 1026, 130, 18 or 3 WDT_CLK reset delay period • Configured to force WDT enabled on chip power-on or reset
Window Watchdog	• Clock sourced from HCLK/2048 or LIRC; the window set by 6-bit counter with 11-bit prescale • Suspended in Idle/Power-down mode
Analog Interfaces	
Enhanced Analog-to-Digital Converter (EADC)	• Up to three sets of 12-bit, 19-ch 5 MSPS SAR EADC with up to 16 single-ended input channels or 8 differential input pairs; 10-bit accuracy is guaranteed • Three internal channels for V_{BAT}, band-gap VBG input and Temperature sensor input • Supports external V_{REF} pin or internal reference voltage • Supports Power-down mode

	• Supports calibration capability • Conversion can be triggered by software, external pin, Timer 0~3 overflow pulse or EPWM/BPWM • Configurable EADC sampling time • Up to 19 sample modules • Double data buffers for sample module 0~3 • PDMA operation • Supports Averageing mode and Oversampling mode, where Oversampling mode provides up to 16-bit precision • Supports early interrupt with delay counter feature
Digital-to-Analog Converter (DAC)	• Up to two sets of 12-bit, 1 MSPS voltage type DAC with 8-bit mode and 8μs rail-to-rail settle time • Maximum output voltage AV_{DD} -0.2V at buffer mode • Conversion can be triggered by software, Timer0~3, EPWM, external pin • Supports group mode for synchronized data update of two DACs • PDMA operation
Analog Comparator (ACMP)	• Up to four rail-to-rail Analog Comparators • Supports four multiplexed I/O pins at positive input • Supports I/O pins, band-gap, DAC, and 16-level Voltage divider from AV_{DD} or V_{REF} at negative input • Supports four programmable power modes for power saving • Supports wake up from Power-down by interrput • Supports triggers for brake events and cycle-by-cycle control for PWM • Supports window compare mode and window latch mode • Supports programmable hysteresis window: 0mV, 20mV and 40mV • Supports offset calibration
Communication Interfaces	
Low-power UART	• Low-power UARTs with up to 10 MHz baud rate • Auto-Baud Rate measurement and baud rate compensation function • Supports low power UART (LPUART): baud rate clock from LXT (32.768 kHz) with 9600 bps in Power-down mode even system clock is stopped • 16-byte FIFOs with programmable level trigger • Auto flow control (nCTS and nRTS) • Supports IrDA (SIR) function • Supports LIN function on UART0 and UART1 • Supports RS-485 9-bit mode and direction control

	• Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function in idle mode • Supports hardware or software enables to program nRTS pin to control RS-485 transmission direction • 8-bit receiver FIFO time-out detection function • Supports break error, frame error, parity error and receive/transmit FIFO overflow detection function • Supports PDMA operation • Supports Single-wire function mode • Supports TX and RX swap function mode
Smart Card Interface	Up to three sets of Smart Card interfaces • ISO-7816-3 compliant with ISO-7816-3 T=0, T=1 • Supports full duplex UART function • 4-byte FIFOs with programmable level trigger • Programmable guard time selection (11 ETU ~ 266 ETU) • One 24-bit and two 8 bit time-out counters for Answer to Request (ATR) and waiting times processing • Auto inverse convention function • Stop clock level and clock stop (clock keep) function • Transmitter and receiver error retry function • Supports hardware activation, deactivation and warm reset sequence process • Supports hardware auto deactivation sequence after card removal
I^2C	• Up to five sets of I^2C devices with Master/Slave mode • Supports Standard mode (100 kbps), Fast mode (400 kbps), Fast mode plus (1 Mbps) and High speed mode (Up to 3.4Mbps) • Supports 10 bits mode • Programmable clocks allowing for versatile rate control • Supports multiple address recognition (four slave address with mask option) • Supports SMBus and PMBus • Supports multi-address power-down wake-up function • PDMA operation • Supports pin swap function • Supports setup/hold time programmable • Supports two level buffer mode
SPI Master (SPI Flash)	• Supports SPI master mode • One slave/device select line for external SPI Flash component • Maximum 32 Mbytes external SPI Flash memory with standard (1-bit), dual (2-bit) and quad (4-bit) transfer mode • 16 Kbytes cache memory for enhancing program execution

	performance • 64-bit key length for code protection • DMA mode for code transfer between SPI Flash memory and SRAM • SPI Master function with 8-, 16-, 24-, and 32-bit length of transaction and burst mode operation, which can transmit/receive data up to four successive transactions in one transfer • Supports Double Transfer Rate (DTR) mode • Supports eXcute-In-Place (XIP)
Quad SPI	• Up to two sets of Quad SPI with Master/Slave mode • Master mode up to 100 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 50 MHz (V_{DD} = 2.7V ~ 3.6V) • Supports Dual and Quad I/O Transfer mode • Supports one data channel half-duplex transfer • Supports double data rate mode (Master TX DIR Mode Only) • Supports receive-only mode • Configurable bit length of a transfer word from 8 to 32-bit • Provides separate 8-level depth transmit and receive FIFO buffers • Supports MSB first or LSB first transfer sequence • Supports the byte reorder function • Supports Byte or Word Suspend mode • Supports 3-wired, no slave select signal, bi-direction interface • PDMA operation
SPI/I²S	• Up to four sets of SPI/I²S controllers with Master/Slave mode • Provides separate 4-level of 32-bit (or 8-level of 16-bit) transmit and receive FIFO buffers **SPI** • Master mode up to 100 MHz (V_{DD} = 2.7V ~ 3.6V) • Slave mode up to 50 MHz (V_{DD} = 2.7V ~ 3.6V) • Configurable bit length of a transfer word from 4 to 32-bit • MSB first or LSB first transfer sequence • Byte reorder function • Supports Byte or Word Suspend mode • Supports one data channel half-duplex transfer • Supports receive-only mode **I²S** • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit audio data sizes • Supports PCM mode A, PCM mode B, I²S and MSB justified data format • PDMA operation

I²S	• Up to two sets of I²S interfaces with Master/Slave mode • Supports mono and stereo audio data with 8-, 16-, 24- and 32-bit word sizes • Two 16-level FIFO data buffers, one for transmitting and the other for receiving • Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format • Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format • PCM protocol supports TDM multi-channel transmission in one audio sample; the number of data channel can be set as 2, 4, 6 or 8 • PDMA operation
Universal Serial Control Interface (USCI)	• Configured as UART, SPI or I²C function • Supports single byte TX and RX buffer mode **UART** • Supports one transmit buffer and two receive buffers for data payload • Supports hardware auto flow control function and programmable flow control trigger level • 9-bit Data Transfer • Baud rate detection by built-in capture event of baud rate generator • Supports wake-up function • PDMA operation **SPI** • Supports Master or Slave mode operation • Supports one transmit buffer and two receive buffer for data payload • Configurable bit length of a transfer word from 4 to 16-bit • Supports MSB first or LSB first transfer sequence • Supports Word Suspend function • Supports 3-wire, no slave select signal, bi-direction interface • Supports wake-up function: input slave select transition • Supports one data channel half-duplex transfer • PDMA operation **I²C** • Supports master and slave device capability • Supports one transmit buffer and two receive buffer for data payload • Communication in standard mode (100 kbps), fast mode (up to 400 kbps), and Fast mode plus (1 Mbps) • Supports 10-bit mode

	• Supports 10-bit bus time out capability • Supports bus monitor mode • Supports power-down wake-up by data toggle or address match • Supports multiple address recognition • Supports device address flag • Programmable setup/hold time
Controller Area Network with Feasibility Data Rate (CAN FD)	• Up to four sets of CAN FD controllers • Compliant with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015 • Compliant with CAN FD version 1.0 with up to 64 data bytes supported • Supports CAN Error logging, AUTOSAR and SAE J1938 • Built-in 1.5K word (32-bit) Message SRAM for each CAN FD controller
Secure Digital Host Controller (SDHC)	• Compliant with SD Memory Card Specification Version 2.0 • Supports 50 MHz to achieve 200 Mbps at 3.3V operation • Supports dedicated DMA master with Scatter-Gather function to accelerate the data transfer between system memory and SD/SDHC/SDIO card
External Bus Interface (EBI)	• Supports up to three memory banks with individual adjustment of timing parameter • Supports dedicated external chip select pin with polarity control and up to 1 Mbytes addressing space for each bank • 8-/16-bit data width • Supports byte write in 16-bit data width mode • Configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R) • Supports Address/Data multiplexed mode • Supports address bus and data bus separate mode • Supports LCD interface i80 mode • PDMA operation
Programmable Serial I/O (PSIO)	• Supports up to 8 PSIO pins • Supports 6 clock sources with clock divider • Supports 4 slot controllers for timing sequence control • Supports 8 check points to connect with slots in each pin • Supports 8 check point actions in each check point • Supports four I/O modes, input, output, open-drain, and quasi • Supports switch I/O mode in different check points • Supports four kinds of Interrupt trigger conditions • PDMA operation

GPIO	• Supports four I/O modes: Quasi bi-direction, Push-Pull output, Open-Drain output and Input only with high impendence mode • Selectable TTL/Schmitt trigger input • Configured as interrupt source with edge/level trigger setting • Supports independent pull-up/pull-down control • Supports high driver and high sink current I/O • Supports software selectable slew rate control • Supports 5V-tolerance function except analog I/O • Configurable I/O mode of all pins after reset default to Quasi-bidirection mode or input mode
KeyPad Interface (KPI)	• Matrix keypad interface with up to 6x8 array • Programmable de-bounce time • Generates interrupt and update press/release status of all keys once key press or release detected
Control Interfaces	
Enhanced Quadrature Encoder Interface (EQEI)	• Two EQEI phase inputs (EQEI_A, EQEI_B) and one Index input (EQEI_INDEX) • Supports 2/4 times free-counting mode and 2/4 compare-counting mode • Supports encoder pulse width measurement mode with ECAP • Supports swap function for input signals (EQEI_A, EQEI_B) • Supports for detecting the occurrence of phase error • Supports one times index signal reset function
Enhanced Capture (ECAP)	• Up to four sets of Enhanced input Capture units • Supports three input channels with independent capture counter hold register • 24-bit Input Capture up-counting timer/counter supports captured events reset and/or reload capture counter • Supports rising edge, falling edge and both edge detector options with noise filter in front of input ports • Supports compare-match function
Advanced Connectivity	
USB 2.0 Full Speed with on-chip transceiver	**USB 2.0 Full Speed OTG (On-The-Go)** • On-chip USB 2.0 full speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 2.0 Full Speed Host Controller**

	• Compliant with USB Revision 1.1 Specification • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Supports Control, Bulk, Interrupt, Isochronous and Split transfers • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Supports port power control and port overcurrent detection • Built-in DMA **USB 2.0 Full Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports suspend function when no bus activity exists for 3 ms • 25 configurable endpoints for configurable Isochronous, Bulk, Interrupt and Control transfer types • 1.5 Kbytes configurable RAM for endpoint buffer • Remote wake-up capability • Start of Frame (SOF) locked clock pulse generation for crystal-less feature • USB 2.0 link power management • Supports double buffer function
USB 2.0 High Speed with on-chip transceiver	**USB 2.0 High Speed OTG (On-The-Go)** • On-chip USB 2.0 high speed OTG transceiver • Compliant with USB OTG Supplement 2.0 • Configurable as host-only, device-only, ID-dependent or OTG device **USB 2.0 High Speed Host Controller** • Compliant with USB Revision 2.0 Specification • Compatible with EHCI (Enhanced Host Controller Interface) Revision 1.0 • Compatible with OHCI (Open Host Controller Interface) Revision 1.0 • Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices • Integrated a port routing logic to route full/low speed device to OHCI controller • Supports an integrated Root Hub • Built-in DMA **USB 2.0 High Speed Device Controller** • Compliant with USB Revision 2.0 Specification • Supports 12 configurable endpoints; each can be Isochronous, Bulk or Interrupt and either IN or OUT direction

	• Maximum packet size up to 1024 bytes • Three different operation modes of an in-endpoint: Auto Validation mode, Manual Validation mode and Fly mode • Suspend, resume and remote wake-up capability • Built-in DMA • Supports Battery Charging 1.2 (BC1.2) • Supports Link Power Management (LPM)
Ethernet MAC	• Compliant with IEEE Std 802.3-2008 for Ethernet MAC • Compliant with IEEE Std 1588-2008 for precision networked clock synchronization. • Compliant with RMII specification version 1.2 from RMII consortium • Full-duplex operation IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion Forwarding of received Pause frames to the user application • Half-duplex operation CSMA/CD Protocol support Flow control using backpressure support Frame bursting and frame extension in 1000 Mbps half-duplex operation Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size • IEEE 802.1Q VLAN tag detection for reception frames • Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1) • Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2) • CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control • Serial management interface (MDC/MDIO) master mode for PHY device configuration and management • Supports Magic Packet recognition to wake system up from Power-down mode
HyperBus Interface (HBI)	• Supports HyperRAM 2.0 with HyperRAM 1.0 • Up to 90 MHz HyperBus clock Rate • Maximum 1440 Mbits/s data rate • Configurable reset timing control • Configurable chip select timing control for HyperRAM Hybrid Sleep or DPD mode

Digital Camera Interface	
Camera Capture Interface (CCAP)	• Supports CCIR601, CCIR656 and 4-bit interfaces for CMOS sensor • Up to 320x240 (QVGA) resolution • Color format for data input supports YUV4:2:2 and RGB565 • Color format for data output supports YUV4:2:2, RGB565, RGB555 and Y-only • Supports 1-bit Y(luminance) output with 8-bit threshold setting for 2-level image thresholding • Supports the CROP function to crop input image to the required size for digital application • Supports image scaling-down
Cryptography Accelerator	
Elliptic Curve Cryptography (ECC)	• Hardware ECC accelerator • Supports 163-bit ~ 571-bit key length • Supports both prime field GF(p) and binary field GF(2m) • Supports NIST P-192, P-224, P-256, P-384 and P-521 curve sizes • Supports NIST B-163, B-233, B-283, B-409 and B-571 curve sizes • Supports NIST K-163, K-233, K-283, K-409 and K-571 curve sizes • Supports point multiplication, addition and doubling operations in GF(p) and GF(2m) • Supports modulus division, multiplication, addition and subtraction operations in GF(p) • Supports Curve25519 • Improved side-channel attack protection • Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
Rivest–Shamir–Adleman Cryptography (RSA)	• Supports both encryption and decryption with up to 4096 bits • CRT decryption with up to 4096 bits • Improved side-channel attack protection ability
Advanced Encryption Standard (AES)	• Hardware AES accelerator • Supports 128-bit, 192-bit and 256-bit key length and key expander, and is compliant with FIPS 197 • Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 block cipher modes • Compliant with NIST SP800-38A and addendum • Supports CCM mode, GCM mode and GMAC function • Improved side-channel attack protection ability
Secure Hash Algorithm	• Hardware SHA accelerator

(SHA)	• Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and and SHA-512/t • Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256 • Compliant with FIPS 180/180-2
keyed-Hash Message Authentication Code (HMAC)	• Hardware HMAC accelerator • Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and HMAC-SHA-512 • Supports HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512 • Compliant with FIPS 180/180-2
Pseudo Random Number Generator (PRNG)	• Hardware PRNG accelerator • Supports take seed from TRNG
True Random Number Generator (TRNG)	• 800 random bits per second
Key store	• Supports programming interface for key management • Supports multiple key size from 128 bits to 4096 bits • Supports 32 SRAM keys, 32 Flash keys and 8 OTP keys at most • Supports crypto engine access key in key store directly • Supports ECDH operation with ECC and PRNG engine • Supports to store middle data for RSA CRT and SCAP mode • Supports revoke operation for each key • Supports erase key in SRAM/Flash and revoke key in OTP while tamper detected • Supports auto verify function • Supports lock function for OTP keys • Supports data remanence prevention at SRAM

3 PARTS INFORMATION

3.1 Package Type

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

3.1.1 M463/M467 Series

Part No.	QFN48 (5x5mm)	LQFP48 (7x7mm)	LQFP64 (7x7mm)	LQFP128 (14x14mm)	LQFP144 (20x20mm)	LQFP176 (24x24mm)
M463	M463YGCAE	M463LGCAE	M463SGCAE	M463KGCAE		
M467			M467SJHAN	M467KJHAN	M467JJHAN	M467HJHAN

3.2 M463/M467 Series Naming Rule

M4	60	H	J	H	A	E
Core	Series	Package	Flash Size	SRAM Size	Revision	Temperature
Cortex-M4F	63: CAN FD/ USB HS 67: Ethernet/ Crypto	Y: QFN48 (5x5 mm) L: LQFP48 (7x7 mm) S: LQFP64 (7x7 mm) K: LQFP128 (14x14 mm) J: LQFP144 (20x20 mm) H: LQFP176 (24x24 mm)	J: 1024 Kbytes G: 256 Kbytes	H: 512 Kbytes C: 128 Kbytes	A	N:-40˚C ~ 85˚C E:-40˚C ~ 105˚C

3.3 M463/M467 Series Selection Guide

3.3.1 M463 Series

PART NUMBER		M463			
		KGCAE	SGCAE	LGCAE	YGCAE
System Frequency (MHz)		200			
Flash (KB)		256			
SRAM (KB)		128			
LDROM (KB)		8			
XOM (regions)		4			
PDMA		16-ch			
I/O		100	44	33	33
RTC (V_{BAT})		√			
32-bit Timer		4			
16-bit EPWM		12			
16-bit BPWM		12			
Connectivity	UART	8			
	QSPI	2			
	SPI/I^2S	4			
	I^2C	5			
	CAN FD	2			
	PSIO	1			
	USCI	1			
	SD Host	1			
	ISO-7816-3	1			
USB High Speed OTG with PHY		√			
LCD Parallel Data Bus (External Bus Interface)		√			
EQEI		2			
ECAP		2			
KPI		6x8			
12-bit ADC		16	16	12	12
Analog Comparator		2			
Crypto		AES-256			
TRNG		√			
Operating Temperature		-40˚C ~ 105˚C			
Package		LQFP 128 (14x14mm)	LQFP 64 (7x7mm)	LQFP 48 (7x7mm)	QFN 48 (5x5mm)

3.3.2 M467 Series

PART NUMBER		M467			
		HJHAN	JJHAN	KJHAN	SJHAN
System Frequency (MHz)		200			
Flash (KB)		1024			
SRAM (KB)		512			
LDROM (KB)		8			
XOM (regions)		4			
PDMA		2 set, each with 16-ch			
I/O		146	114	100	44
RTC (V_{BAT})		√			
32-bit Timer		4			
16-bit EPWM		12			
16-bit BPWM		12			
Connectivity	UART	10			9
	QSPI	2			
	SPI/I²S	4			
	SPI Master	1			
	I²S	2			
	I²C	5			
	CAN FD	4			
	PSIO	1			
	USCI	1			
	SD Host	2			
	ISO-7816-3	3			
USB High Speed OTG with PHY		√			
USB Full Speed OTG with PHY		√			
LCD Parallel Data Bus (External Bus Interface)		√			
HyperBus Interface		√			-
EQEI		4			
ECAP		4			
KPI		6x8			
12-bit ADC		28			20
12-bit DAC		2			
Analog Comparator		4			
Crypto		AES-256, ECC-571, SHA-512, HMAC-512, RSA-4096, SM2			

TRNG	√			
Ethernet 10/100 Mac	√			
Camera Capture Interface	√			
Operating Temperature	-40˚C ~ 85˚C			
Package	LQFP 176 (24x24mm)	LQFP 144 (20x20mm)	LQFP 128 (14x14mm)	LQFP 64 (7x7mm)

3.4 M463/M467 Series Features Comparison Table

Section	Sub-section	M463	M467
System Manager	Figure 6.2-11 SRAM Memory Organization for 512 Kbyte Device	-	●
	Figure 6.2-12 SRAM Memory Organization for 128 Kbyte Device	●	-
FMC	Dual Bank Architecture	-	●
	Physical and Virtual Address Concept	-	●
	APROM Reboot Address Operation Model Selection	-	●
Cryptographic Accelerator	Cryptographic Accelerator (CRYPTO)	-	●
	Cryptographic Accelerator for M463 Series (CRYPTO_M463)	●	-
RTC	Spare Registers and Tamper Detector for M463 Series	●	-
	Spare Registers and Tamper Detector for M467 Series	-	●

4 PIN CONFIGURATION

4.1 Pin Configuration

Users can find pin configuration information in the M463/M467 series Multi-function Pin diagram sections or by using NuTool - PinConfigure. The NuTool - PinConfigure contains all NuMicro Family chip series with all part number, and helps users configure GPIO multi-function correctly and handily.

4.1.1 M463 Series Pin Diagram

4.1.1.1 M463 Series QFN48-Pin Diagram

Corresponding Part Number: M463YGCAE

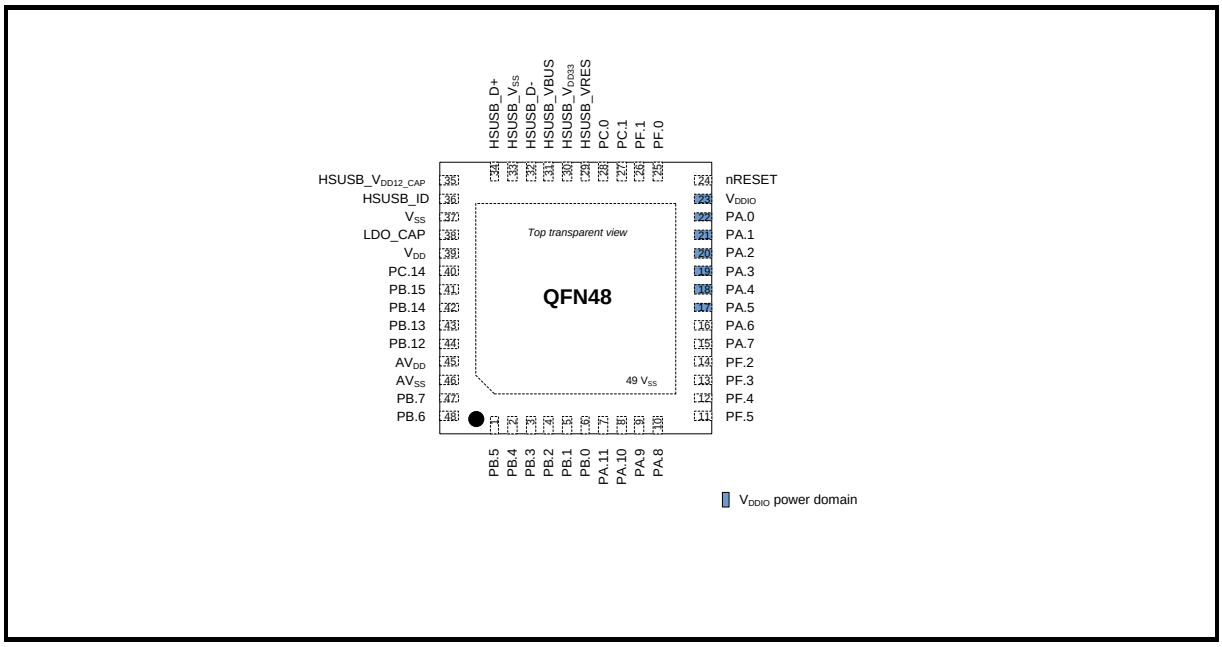


Figure 4.1-1 M463 Series QFN48-Pin Diagram

4.1.1.2 M463 Series LQFP48-Pin Diagram

Corresponding Part Number: M463LGCAE

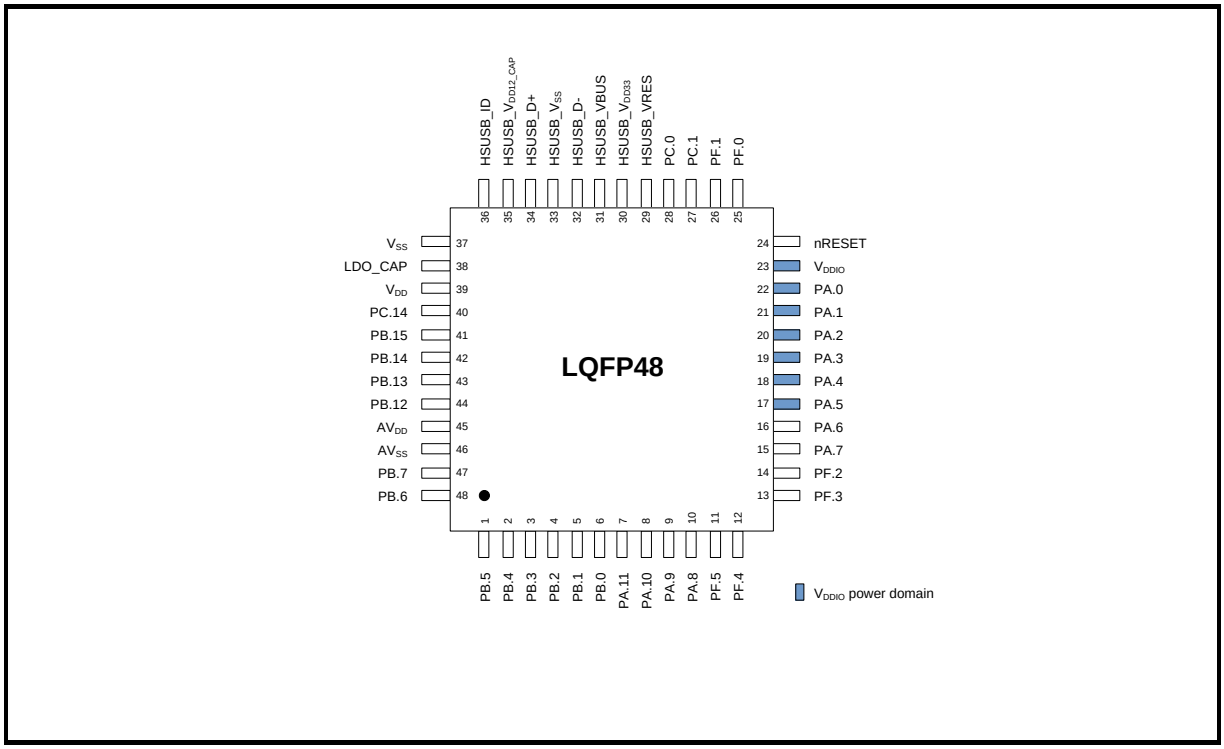


Figure 4.1-2 M463 Series LQFP48-Pin Diagram

4.1.1.3 M463 Series LQFP64-Pin Diagram

Corresponding Part Number: M463SGCAE

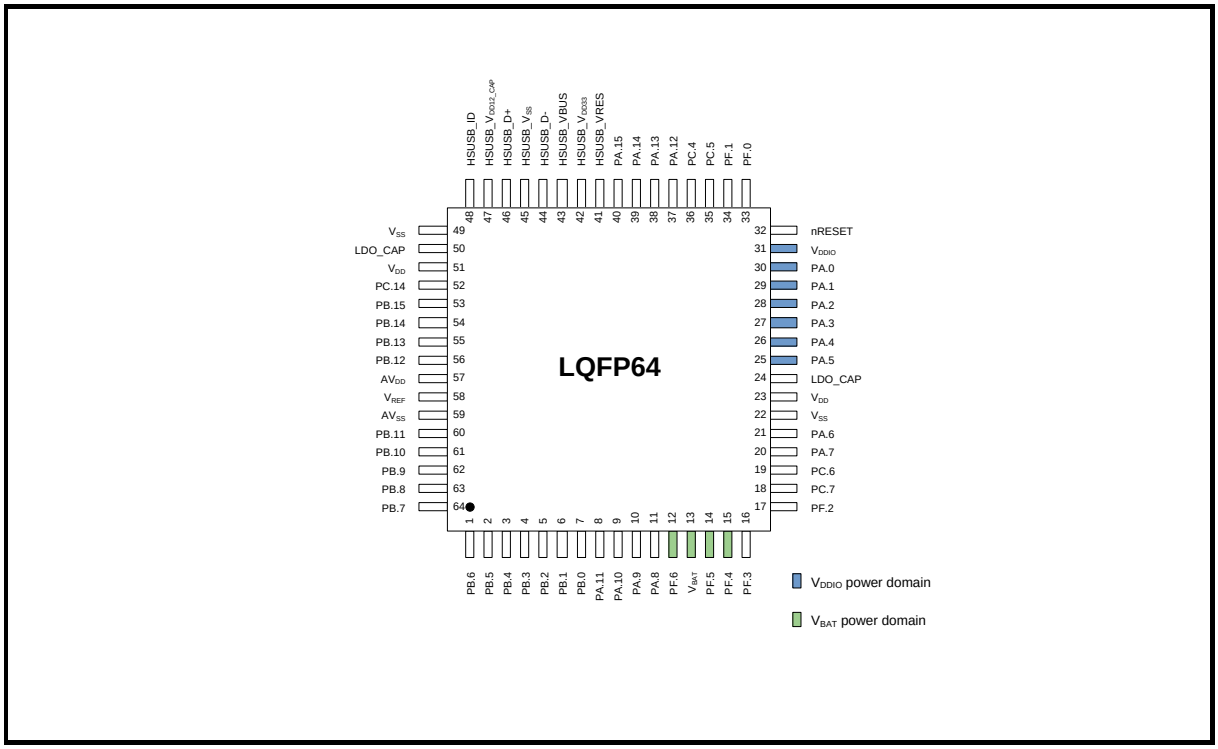


Figure 4.1-3 M463 Series LQFP64-Pin Diagram

4.1.1.4 M463 Series LQFP128-Pin Diagram

Corresponding Part Number: M463KGCAE

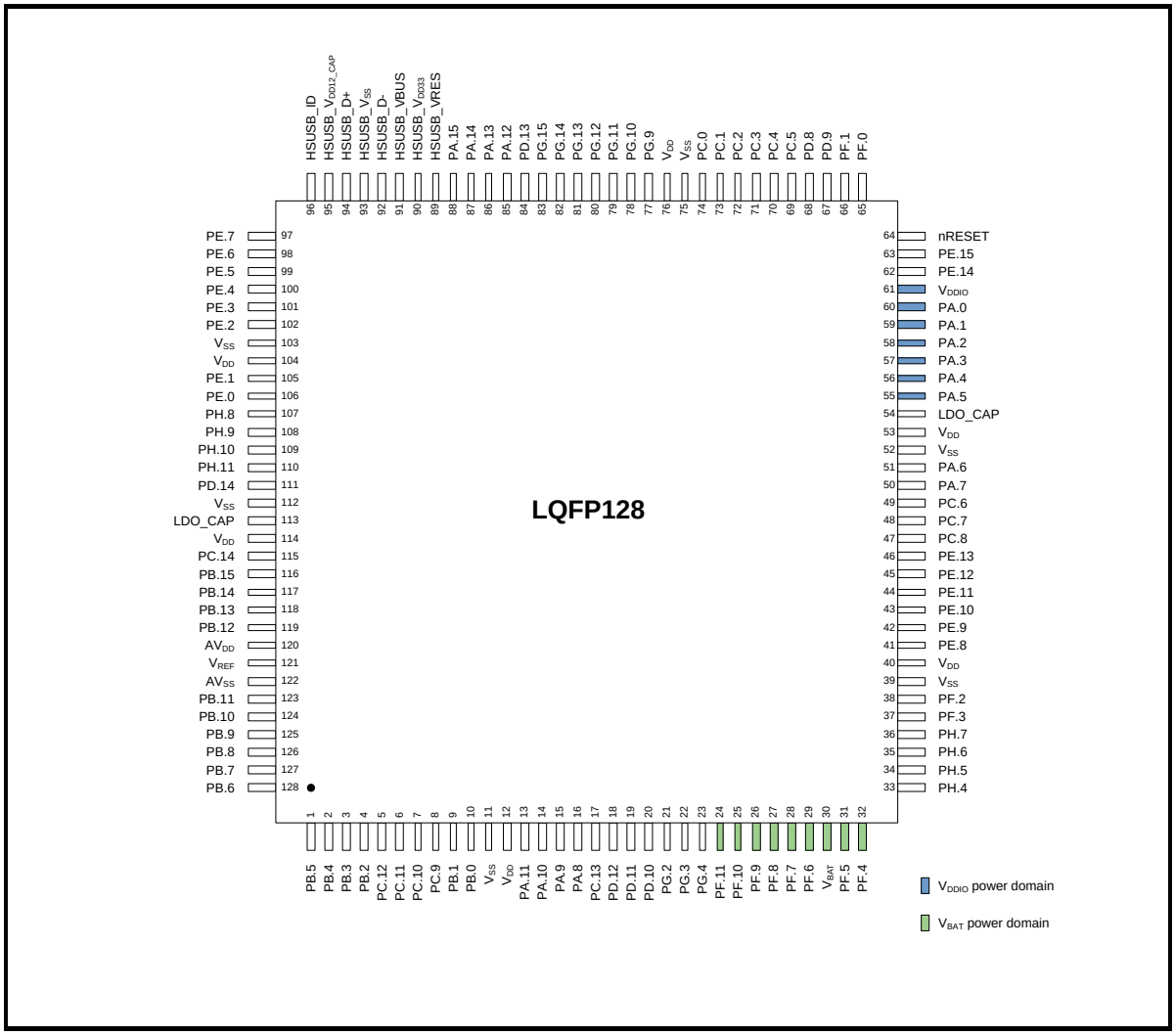


Figure 4.1-4 M463 Series LQFP128-Pin Diagram

4.1.2 M467 Series Pin Diagram

4.1.2.1 M467 Series LQFP64-Pin Diagram

Corresponding Part Number: M467SJHAN

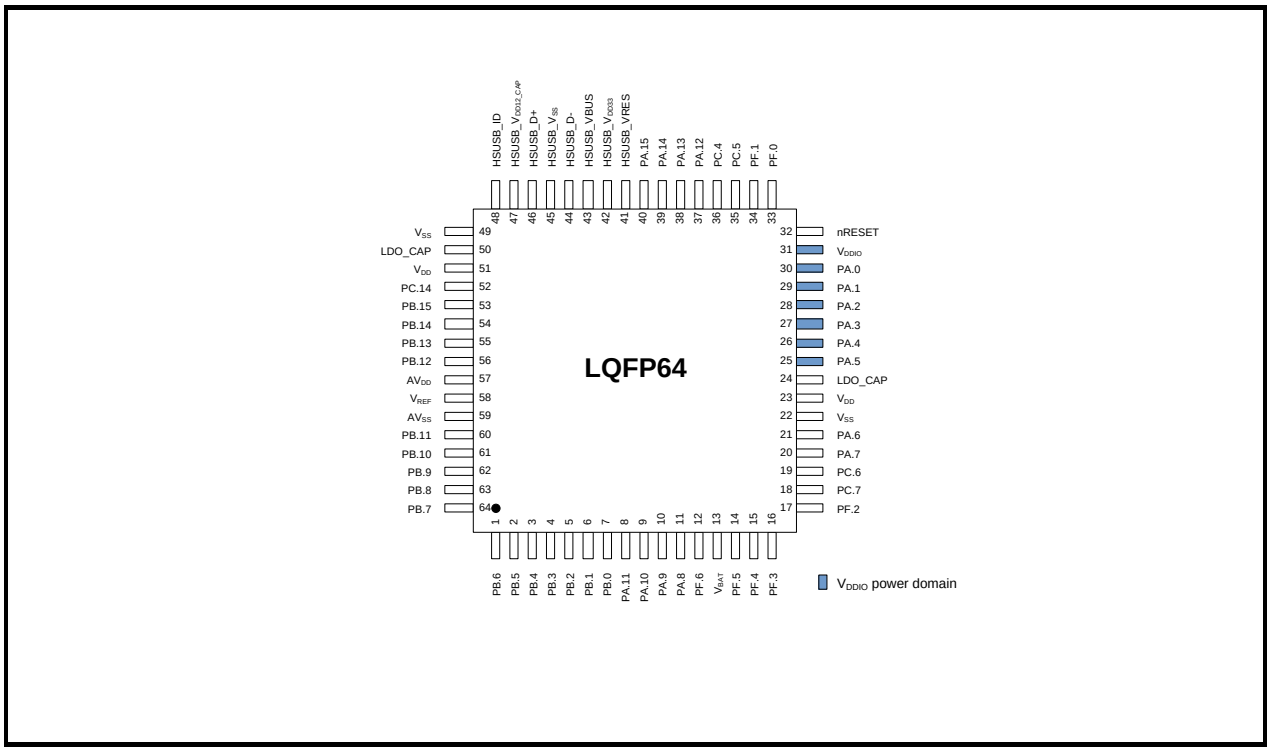


Figure 4.1-5 M467 Series LQFP64-Pin Diagram

4.1.2.2 M467 Series LQFP128-Pin Diagram

Corresponding Part Number: M467KJHAN

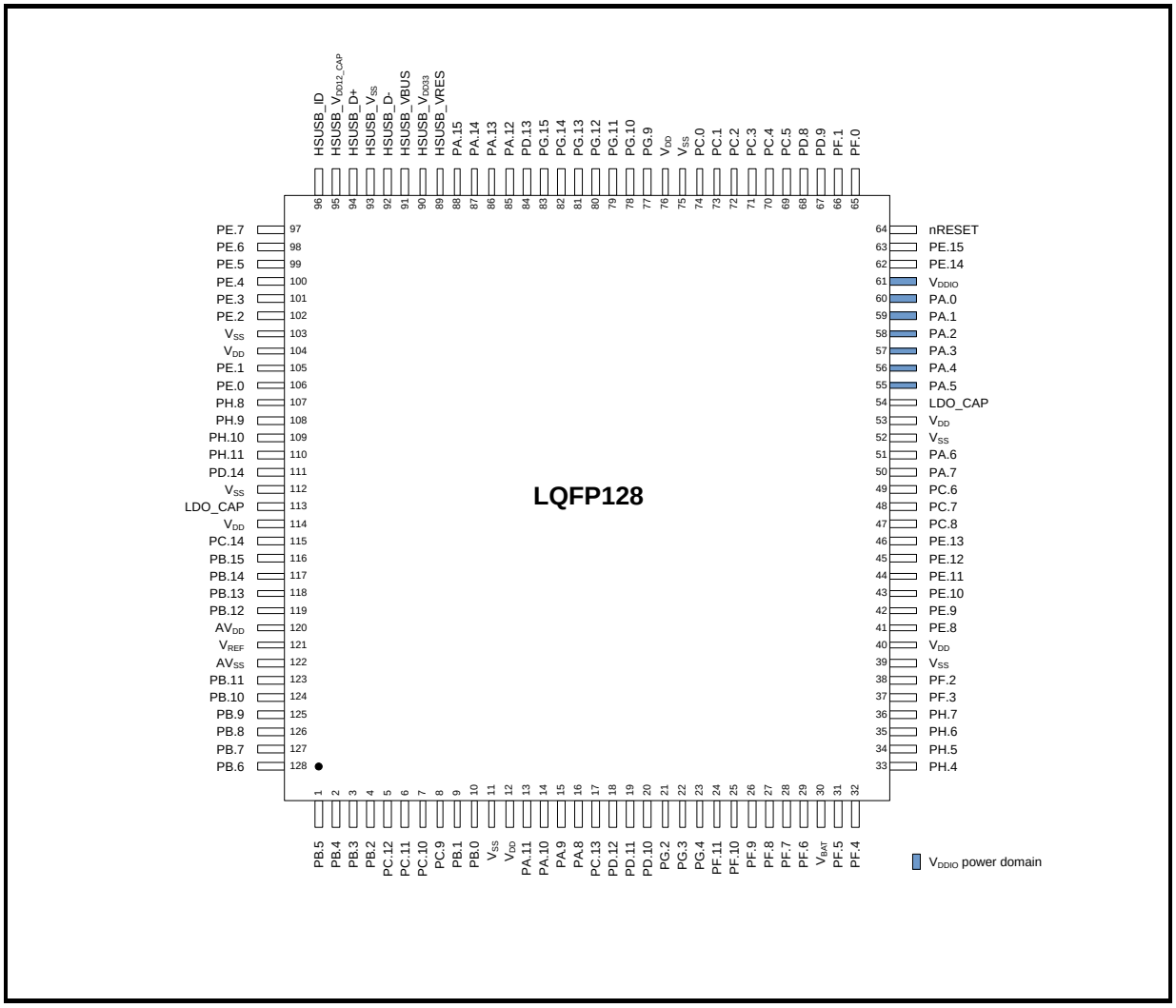


Figure 4.1-6 M467 Series LQFP128-Pin Diagram

4.1.2.3 M467 Series LQFP144-Pin Diagram

Corresponding Part Number: M467JJHAN

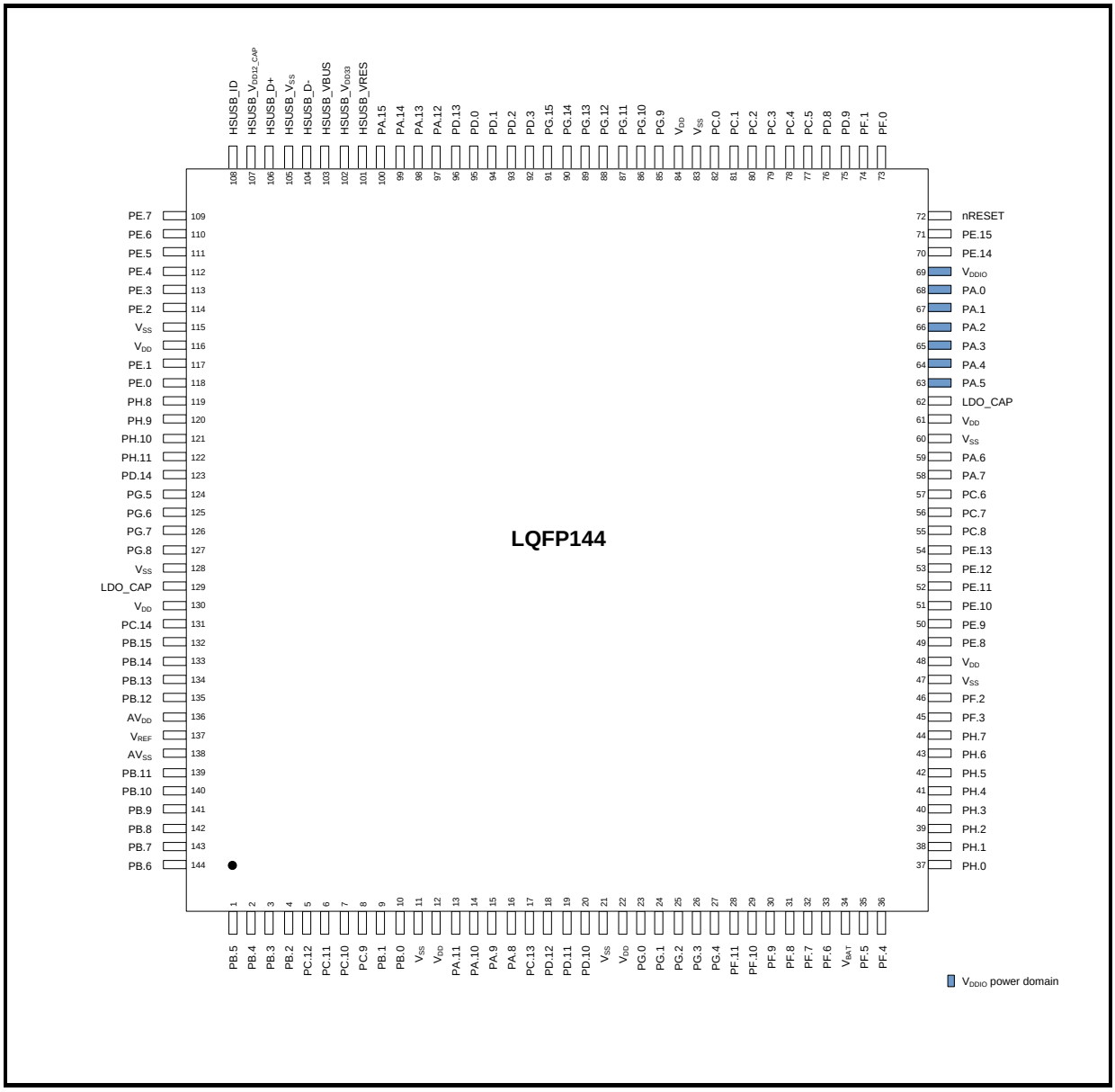


Figure 4.1-7 M467 Series LQFP144-Pin Diagram

4.1.2.4 M467 Series LQFP176-Pin Diagram

Corresponding Part Number: M467HJHAN

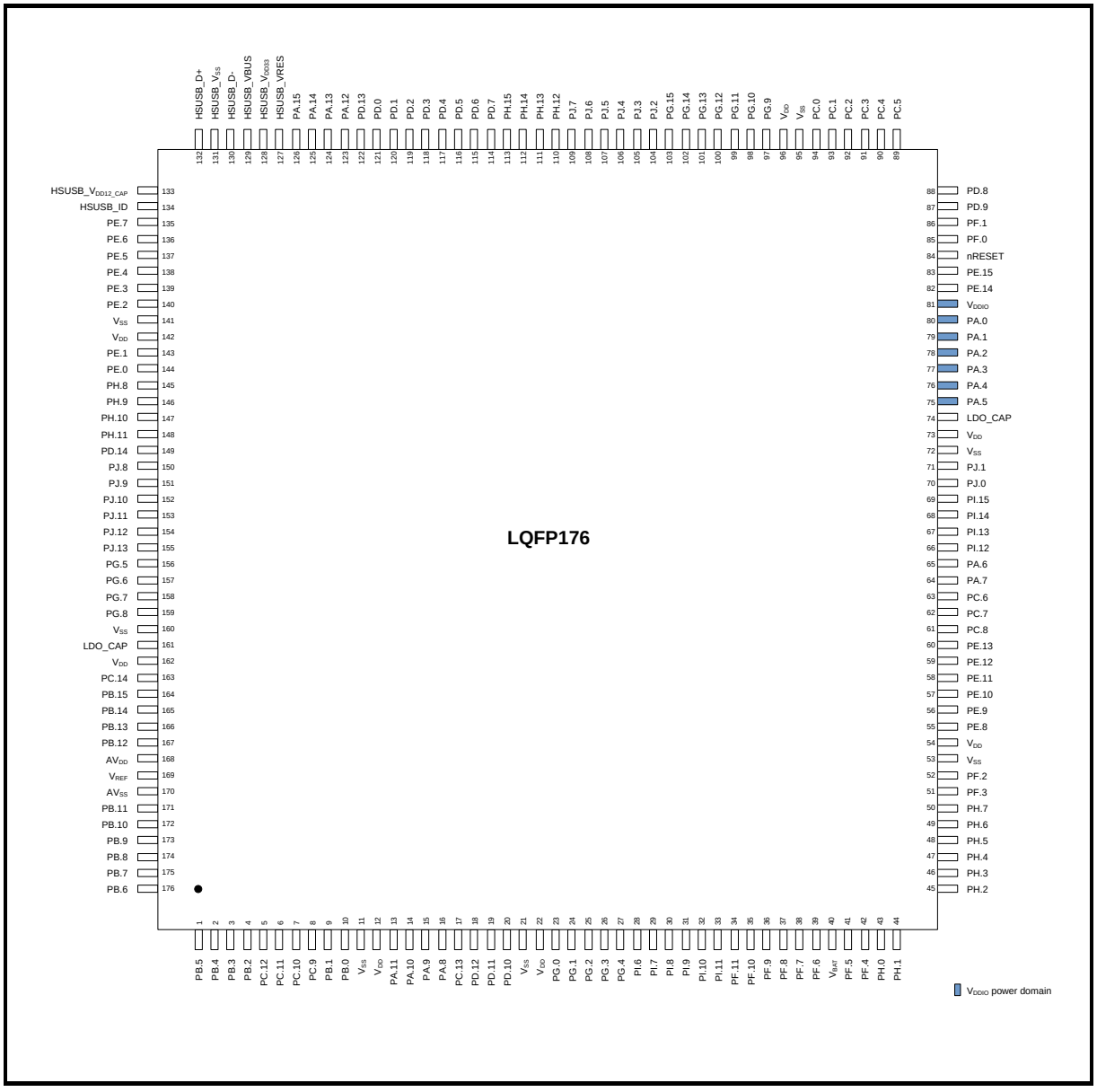


Figure 4.1-8 M467 Series LQFP176-Pin Diagram

4.1.3 M463 Series Multi-function Pin Diagram

4.1.3.1 M463 Series QFN48-Pin Multi-function Pin Diagram

Corresponding Part Number: M463YGCAE

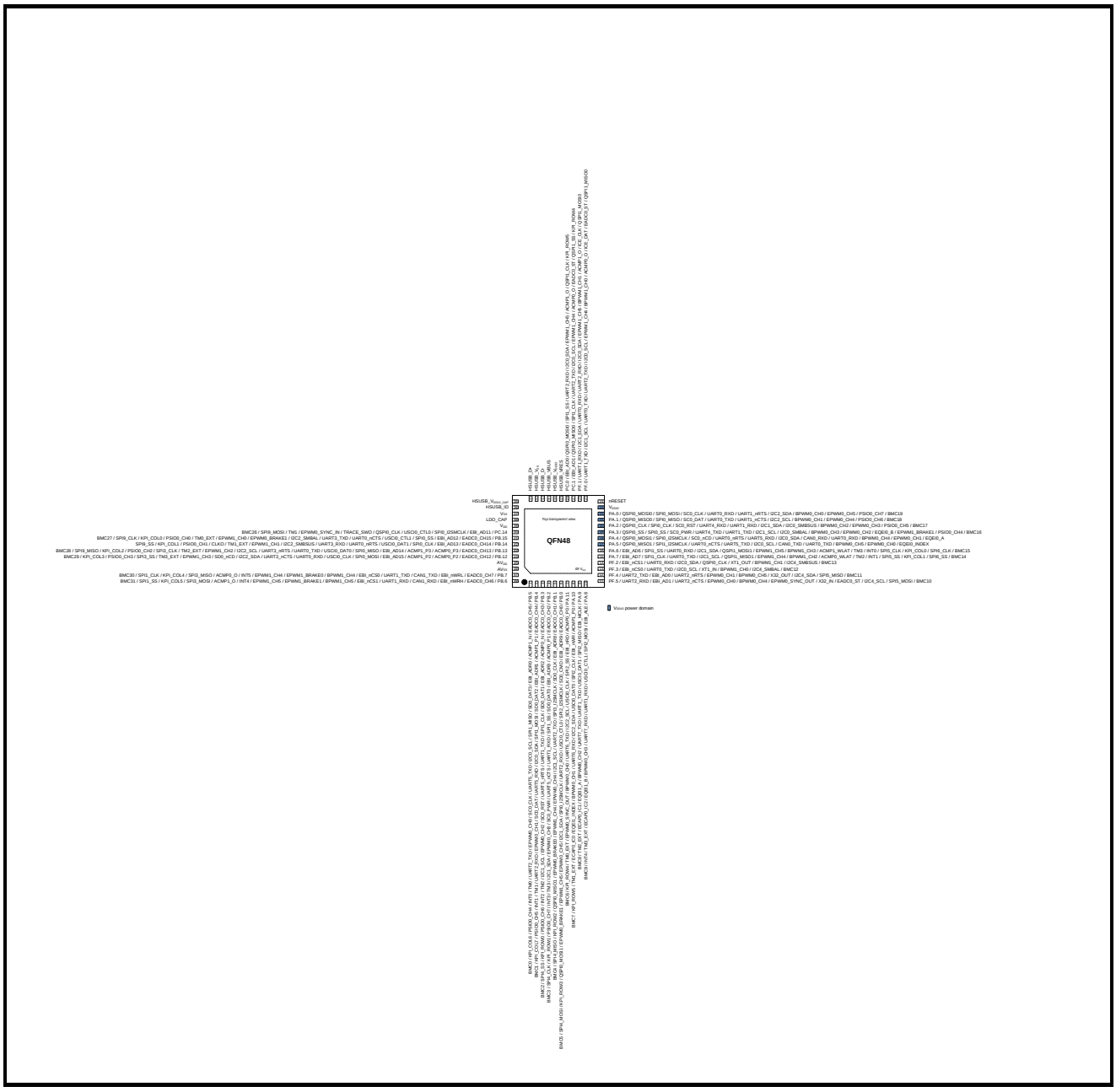


Figure 4.1-9 M463 Series QFN48-Pin Multi-function Pin Diagram

Pin	Type	M463YGCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS

Pin	Type	M463YGCAE Pin Function
		/ SC0_RST / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1 / KPI_ROW2
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / KPI_ROW3
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / KPI_ROW4
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / KPI_ROW5
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / I2C4_SDA
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0 / I2C4_SMBAL
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
17	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART5_TXD / I2C0_SCL / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / PSIO0_CH5
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / PSIO0_CH6
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / PSIO0_CH7
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / QSPI1_MISO0
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / QSPI1_MOSI0
27	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ACMP0_O /

Pin	Type	M463YGCAE Pin Function
		EADC0_ST / QSPI1_SS / KPI_ROW4
28	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ACMP1_O / QSPI1_CLK / KPI_ROW5
29	A	HSUSB_VRES
30	P	HSUSB_VDD33
31	I/O	HSUSB_VBUS
32	A	HSUSB_D-
33	P	HSUSB_VSS
34	A	HSUSB_D+
35	A	HSUSB_VDD12_CAP
36	I	HSUSB_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PSIO0_CH0 / KPI_COL0
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / TM1_EXT / CLKO / PSIO0_CH1 / KPI_COL1
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / PSIO0_CH2 / KPI_COL2
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / PSIO0_CH3 / KPI_COL3
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O / KPI_COL4 / SPI1_CLK
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / KPI_COL5 / SPI1_SS
49	P	V_{SS}

Table 4.1-1 M463YGCAE Multi-function Pin Table

4.1.3.2 M463 Series LQFP48-Pin Multi-function Pin Diagram

Corresponding Part Number: M463LGCAE

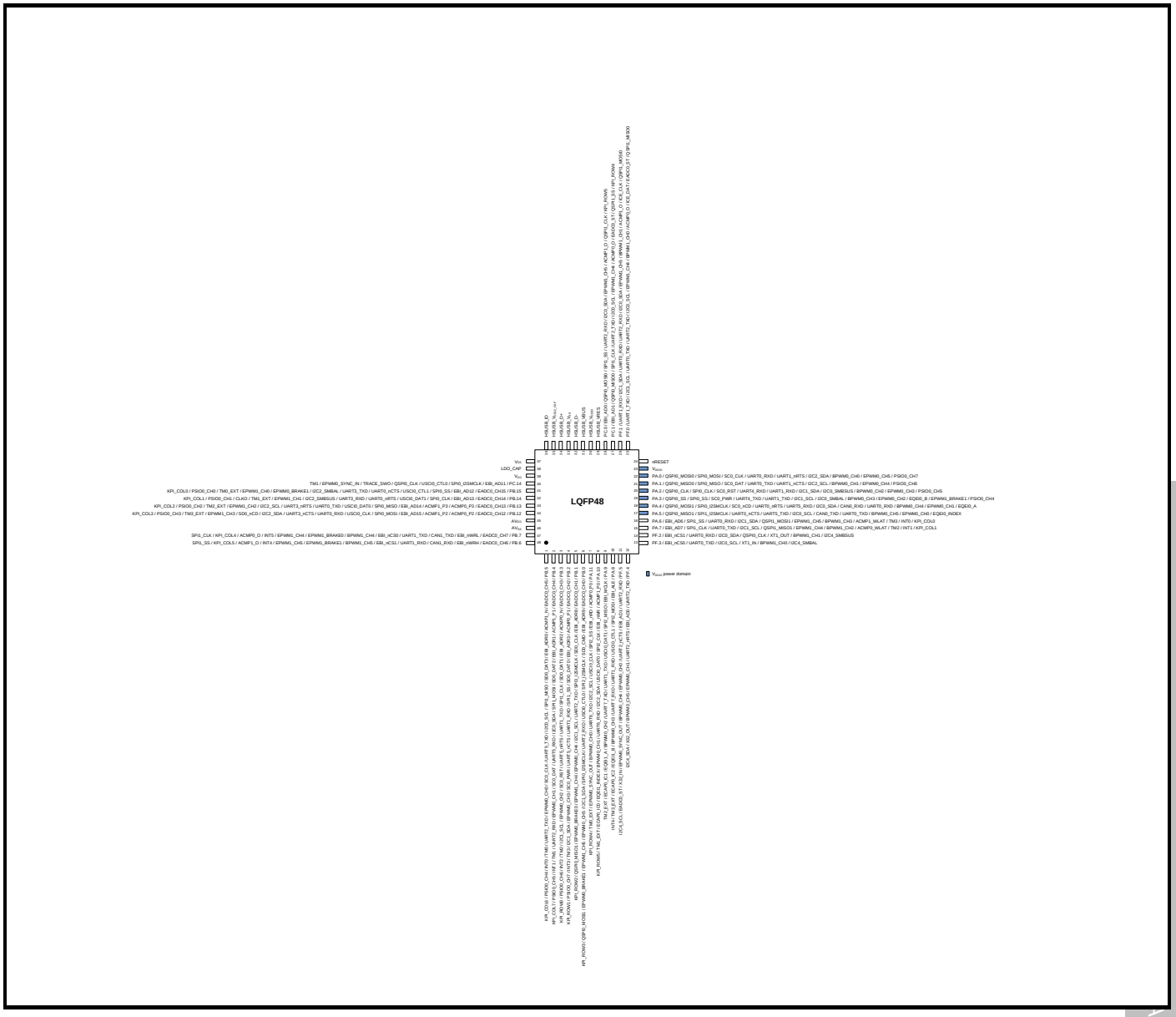


Figure 4.1-10 M463 Series LQFP48-Pin Multi-function Pin Diagram

Pin	Type	M463LGCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1

Pin	Type	M463LGCAE Pin Function
5	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1 / KPI_ROW2
6	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / KPI_ROW3
7	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / KPI_ROW4
8	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / KPI_ROW5
9	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT
10	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4
11	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL
12	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / I2C4_SDA
13	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0 / I2C4_SMBAL
14	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS
15	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
16	I/O	PA.6 / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
17	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
18	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
19	I/O	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
20	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / PSIO0_CH5
21	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / PSIO0_CH6
22	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / PSIO0_CH7
23	P	V_{DDIO}
24	I	nRESET
25	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / QSPI1_MISO0
26	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / QSPI1_MOSI0
27	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ACMP0_O / EADC0_ST / QSPI1_SS / KPI_ROW4
28	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ACMP1_O / QSPI1_CLK / KPI_ROW5

Pin	Type	M463LGCAE Pin Function
29	A	HSUSB_VRES
30	P	HSUSB_VDD33
31	I/O	HSUSB_VBUS
32	A	HSUSB_D-
33	P	HSUSB_VSS
34	A	HSUSB_D+
35	A	HSUSB_VDD12_CAP
36	I	HSUSB_ID
37	P	V_{SS}
38	A	LDO_CAP
39	P	V_{DD}
40	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1
41	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PSIO0_CH0 / KPI_COL0
42	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / TM1_EXT / CLKO / PSIO0_CH1 / KPI_COL1
43	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / PSIO0_CH2 / KPI_COL2
44	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / PSIO0_CH3 / KPI_COL3
45	P	AV_{DD}
46	P	AV_{SS}
47	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CAN1_TXD / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O / KPI_COL4 / SPI1_CLK
48	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / CAN1_RXD / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / KPI_COL5 / SPI1_SS

Table 4.1-2 M463LGCAE Multi-function Pin Table

4.1.3.3 M463 Series LQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M463SGCAE

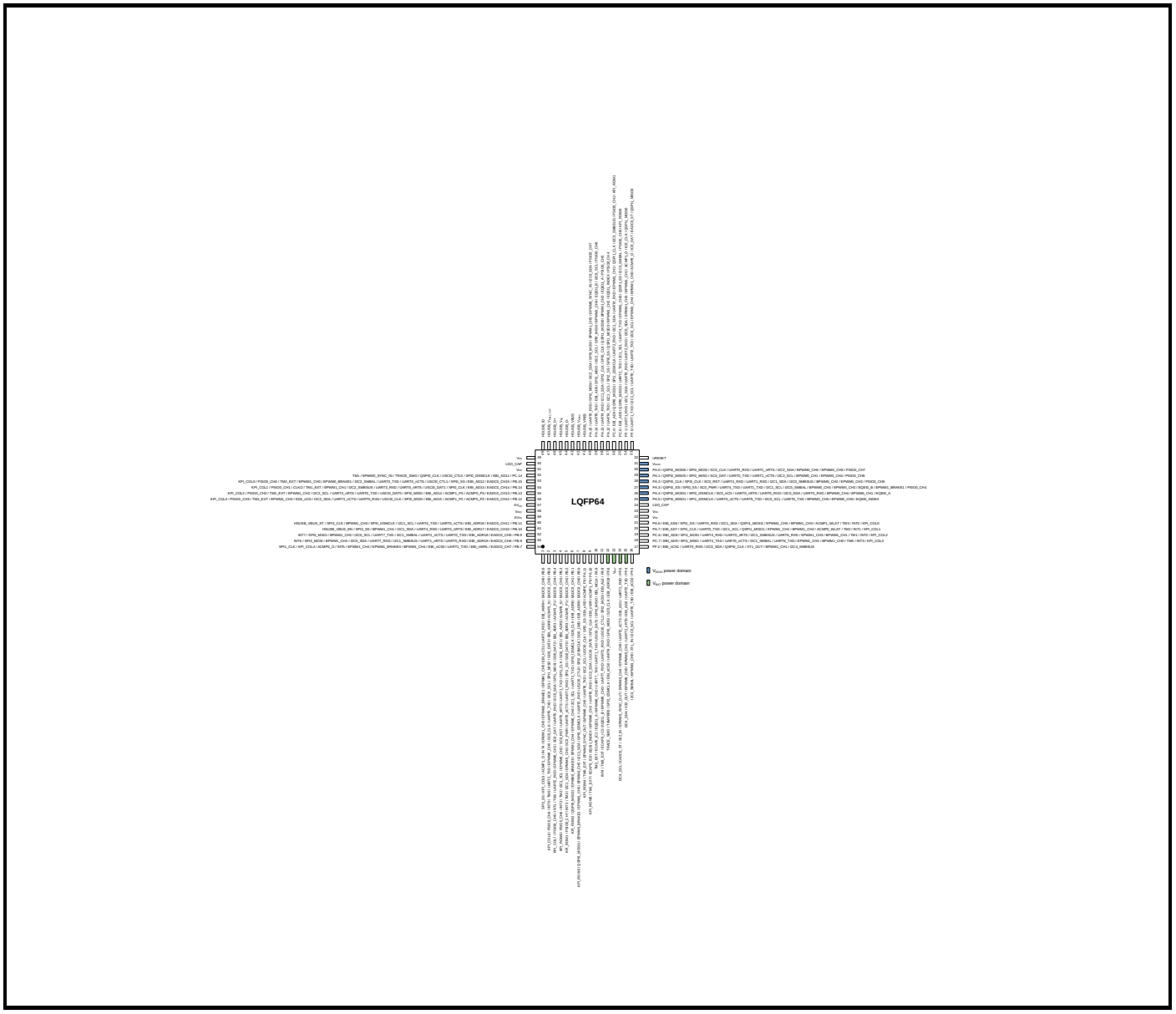


Figure 4.1-11 M463 Series LQFP64-Pin Multi-function Pin Diagram

Pin	Type	M463SGCAE Pin Function
1	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / KPI_COL5 / SPI1_SS
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
4	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0

Pin	Type	M463SGCAE Pin Function
5	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
6	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1 / KPI_ROW2
7	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / KPI_ROW3
8	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / KPI_ROW4
9	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / KPI_ROW5
10	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT
11	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / SC0_CLK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / SPI3_I2SMCLK / TAMPER0 / TRACE_SWO
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL
15	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / I2C4_SDA
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0 / I2C4_SMBAL
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS
18	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / UART6_TXD / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / KPI_COL3
19	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / KPI_COL2
20	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
21	I/O	PA.6 / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP
25	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART5_TXD / I2C0_SCL / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
26	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
27	I/O	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
28	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / PSIO0_CH5
29	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / PSIO0_CH6

Pin	Type	M463SGCAE Pin Function
30	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / PSIO0_CH7
31	P	V_{DDIO}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / QSPI1_MISO0
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / QSPI1_MOSI0
35	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / UART4_TXD / EPWM1_CH0 / QSPI1_SS / I2C3_SMBAL / PSIO0_CH0 / KPI_ROW0
36	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / UART4_RXD / EPWM1_CH1 / QSPI1_CLK / I2C3_SMBSUS / PSIO0_CH1 / KPI_ROW1
37	I/O	PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / SPI0_SS / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / PSIO0_CH4
38	I/O	PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / SPI0_CLK / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / PSIO0_CH5
39	I/O	PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / BPWM1_CH4 / EQEI1_B / I2C0_SCL / PSIO0_CH6
40	I/O	PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / BPWM1_CH5 / EPWM0_SYNC_IN / I2C0_SDA / PSIO0_CH7
41	A	HSUSB_VRES
42	P	HSUSB_VDD33
43	I/O	HSUSB_VBUS
44	A	HSUSB_D-
45	P	HSUSB_VSS
46	A	HSUSB_D+
47	A	HSUSB_VDD12_CAP
48	I	HSUSB_ID
49	P	V_{SS}
50	A	LDO_CAP
51	P	V_{DD}
52	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1
53	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PSIO0_CH0 / KPI_COL0
54	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / TM1_EXT / CLKO / PSIO0_CH1 / KPI_COL1
55	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / PSIO0_CH2 / KPI_COL2
56	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / PSIO0_CH3 / KPI_COL3
57	P	AV_{DD}

Pin	Type	M463SGCAE Pin Function
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / HSUSB_VBUS_ST
61	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / UART0_nRTS / UART4_RXD / I2C1_SDA / BPWM1_CH1 / SPI3_SS / HSUSB_VBUS_EN
62	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7
63	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6
64	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O / KPI_COL4 / SPI1_CLK

Table 4.1-3 M463SGCAE Multi-function Pin Table

4.1.3.4 M463 Series LQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M463KGCAE

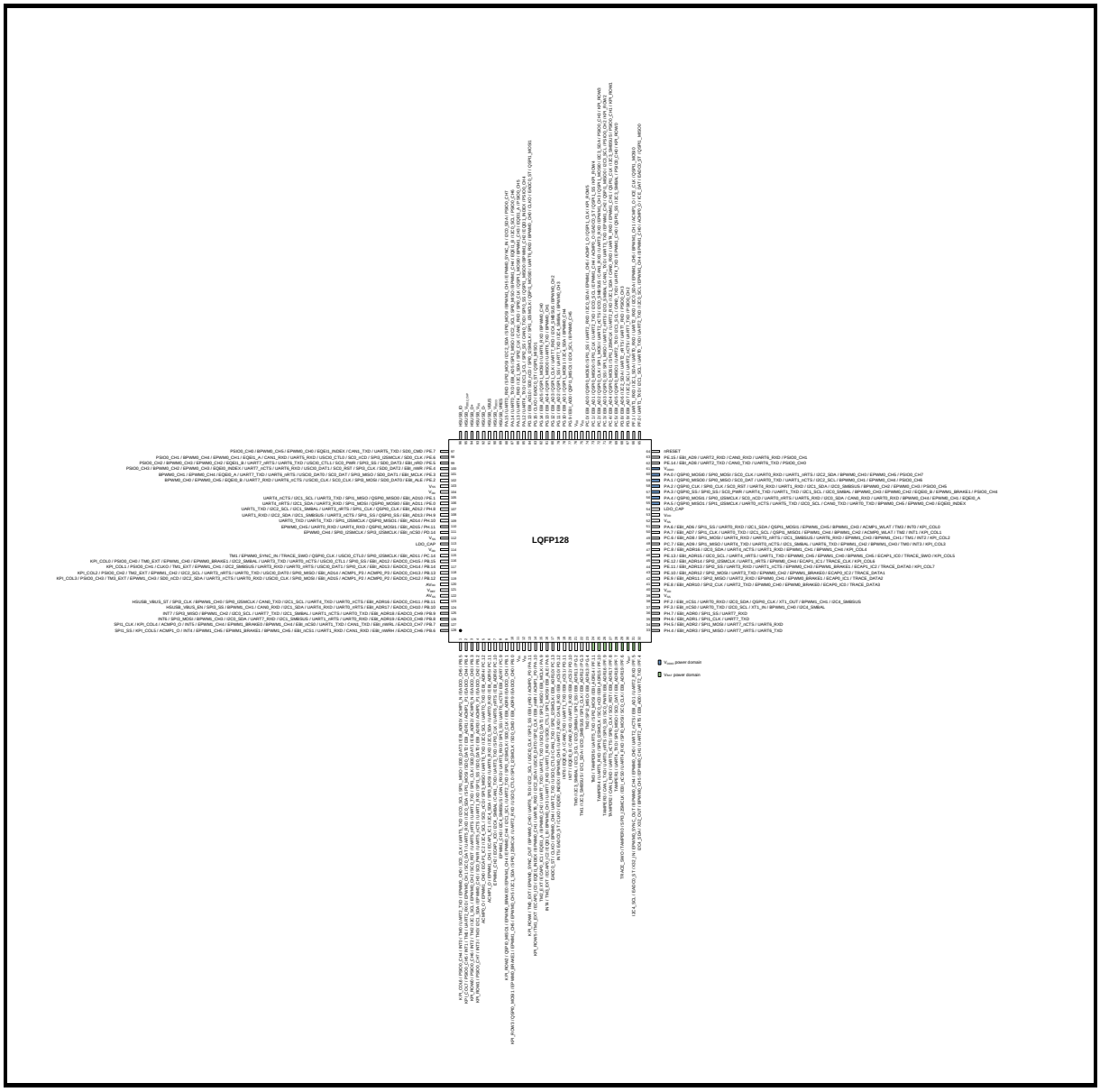


Figure 4.1-12 M463 Series LQFP128-Pin Multi-function Pin Diagram

Pin	Type	M463KGCAE Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0
4	I/O	PB.2 / EADC0_CH2 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1

Pin	Type	M463KGCAE Pin Function
5	I/O	PC.12 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / I2C4_SCL / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / I2C4_SDA / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CAN1_TXD / I2C4_SMBAL / ECAP1_IC0 / EPWM1_CH2
8	I/O	PC.9 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CAN1_RXD / I2C4_SMBSUS / EPWM1_CH3
9	I/O	PB.1 / EADC0_CH1 / EBI_ADR8 / SD0_CLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / QSPI0_MISO1 / KPI_ROW2
10	I/O	PB.0 / EADC0_CH0 / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / QSPI0_MOSI1 / KPI_ROW3
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / ACMP0_P0 / EBI_nRD / SPI2_SS / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / TM0_EXT / KPI_ROW4
14	I/O	PA.10 / ACMP1_P0 / EBI_nWR / SPI2_CLK / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / TM1_EXT / KPI_ROW5
15	I/O	PA.9 / EBI_MCLK / SPI2_MISO / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / TM2_EXT
16	I/O	PA.8 / EBI_ALE / SPI2_MOSI / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / TM3_EXT / INT4
17	I/O	PC.13 / EBI_ADR10 / SPI2_I2SMCLK / CAN1_TXD / USCI0_CTL0 / UART2_TXD / BPWM0_CH4 / CLKO / EADC0_ST
18	I/O	PD.12 / EBI_nCS0 / CAN1_RXD / UART2_RXD / BPWM0_CH5 / EQEI0_INDEX / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EBI_nCS1 / UART1_TXD / CAN0_TXD / EQEI0_A / INT6
20	I/O	PD.10 / EBI_nCS2 / UART1_RXD / CAN0_RXD / EQEI0_B / INT7
21	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / I2C3_SMBAL / TM0
22	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / I2C3_SMBSUS / TM1
23	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / TM2
24	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / TAMPER5 / TM3
25	I/O	PF.10 / EBI_ADR15 / SC0_nCD / SPI0_I2SMCLK / UART5_RXD / TAMPER4
26	I/O	PF.9 / EBI_ADR16 / SC0_PWR / SPI0_SS / UART5_nRTS / CAN1_TXD / TAMPER3
27	I/O	PF.8 / EBI_ADR17 / SC0_RST / SPI0_CLK / UART5_nCTS / CAN1_RXD / TAMPER2
28	I/O	PF.7 / EBI_ADR18 / SC0_DAT / SPI0_MISO / UART4_TXD / TAMPER1
29	I/O	PF.6 / EBI_ADR19 / SC0_CLK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / SPI3_I2SMCLK / TAMPER0 / TRACE_SWO
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL
32	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT /

Pin	Type	M463KGCAE Pin Function
		I2C4_SDA
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0 / I2C4_SMBAL
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / SPI2_CLK / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / TRACE_DATA3
42	I/O	PE.9 / EBI_ADR11 / SPI2_MISO / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / TRACE_DATA2
43	I/O	PE.10 / EBI_ADR12 / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / TRACE_DATA1
44	I/O	PE.11 / EBI_ADR13 / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / KPI_COL7
45	I/O	PE.12 / EBI_ADR14 / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / KPI_COL6
46	I/O	PE.13 / EBI_ADR15 / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5
47	I/O	PC.8 / EBI_ADR16 / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / KPI_COL4
48	I/O	PC.7 / EBI_AD9 / SPI1_MISO / UART4_TXD / UART0_nCTS / I2C1_SMBAL / UART6_TXD / EPWM1_CH2 / BPWM1_CH0 / TM0 / INT3 / KPI_COL3
49	I/O	PC.6 / EBI_AD8 / SPI1_MOSI / UART4_RXD / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / EPWM1_CH3 / BPWM1_CH1 / TM1 / INT2 / KPI_COL2
50	I/O	PA.7 / EBI_AD7 / SPI1_CLK / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
51	I/O	PA.6 / EBI_AD6 / SPI1_SS / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
52	P	V_{SS}
53	P	V_{DD}
54	A	LDO_CAP
55	I/O	PA.5 / QSPI0_MISO1 / SPI1_I2SMCLK / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
56	I/O	PA.4 / QSPI0_MOSI1 / SPI0_I2SMCLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
57	I/O	PA.3 / QSPI0_SS / SPI0_SS / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
58	I/O	PA.2 / QSPI0_CLK / SPI0_CLK / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / PSIO0_CH5

Pin	Type	M463KGCAE Pin Function
59	I/O	PA.1 / QSPI0_MISO0 / SPI0_MISO / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / BPWM0_CH1 / EPWM0_CH4 / PSIO0_CH6
60	I/O	PA.0 / QSPI0_MOSI0 / SPI0_MOSI / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / BPWM0_CH0 / EPWM0_CH5 / PSIO0_CH7
61	P	V_{DDIO}
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CAN0_TXD / UART6_TXD / PSIO0_CH0
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CAN0_RXD / UART6_RXD / PSIO0_CH1
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / UART2_TXD / I2C0_SCL / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST / QSPI1_MISO0
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / UART2_RXD / I2C0_SDA / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / QSPI1_MOSI0
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD / PSIO0_CH2
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD / PSIO0_CH3
69	I/O	PC.5 / EBI_AD5 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / QSPI1_SS / I2C3_SMBAL / PSIO0_CH0 / KPI_ROW0
70	I/O	PC.4 / EBI_AD4 / QSPI0_MOSI1 / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / QSPI1_CLK / I2C3_SMBSUS / PSIO0_CH1 / KPI_ROW1
71	I/O	PC.3 / EBI_AD3 / QSPI0_SS / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CAN1_TXD / UART3_TXD / EPWM1_CH2 / QSPI1_MISO0 / I2C3_SCL / PSIO0_CH2 / KPI_ROW2
72	I/O	PC.2 / EBI_AD2 / QSPI0_CLK / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD / EPWM1_CH3 / QSPI1_MOSI0 / I2C3_SDA / PSIO0_CH3 / KPI_ROW3
73	I/O	PC.1 / EBI_AD1 / QSPI0_MISO0 / SPI1_CLK / UART2_TXD / I2C0_SCL / EPWM1_CH4 / ACMP0_O / EADC0_ST / QSPI1_SS / KPI_ROW4
74	I/O	PC.0 / EBI_AD0 / QSPI0_MOSI0 / SPI1_SS / UART2_RXD / I2C0_SDA / EPWM1_CH5 / ACMP1_O / QSPI1_CLK / KPI_ROW5
75	P	V_{SS}
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / QSPI1_MISO1 / I2C4_SCL / BPWM0_CH5
78	I/O	PG.10 / EBI_AD1 / QSPI1_MOSI1 / I2C4_SDA / BPWM0_CH4
79	I/O	PG.11 / EBI_AD2 / QSPI1_SS / UART7_TXD / I2C4_SMBAL / BPWM0_CH3
80	I/O	PG.12 / EBI_AD3 / QSPI1_CLK / UART7_RXD / I2C4_SMBSUS / BPWM0_CH2
81	I/O	PG.13 / EBI_AD4 / QSPI1_MISO0 / UART6_TXD / BPWM0_CH1
82	I/O	PG.14 / EBI_AD5 / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0
83	I/O	PG.15 / CLKO / EADC0_ST / QSPI1_MISO1
84	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0 / CLKO / EADC0_ST / QSPI1_MOSI1
85	I/O	PA.12 / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SPI0_SS / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / PSIO0_CH4
86	I/O	PA.13 / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SPI0_CLK / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / PSIO0_CH5
87	I/O	PA.14 / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SPI0_MISO / BPWM1_CH4 / EQEI1_B /

Pin	Type	M463KGCAE Pin Function
		I2C0_SCL / PSIO0_CH6
88	I/O	PA.15 / UART0_RXD / SPI2_MOSI / I2C2_SDA / SPI0_MOSI / BPWM1_CH5 / EPWM0_SYNC_IN / I2C0_SDA / PSIO0_CH7
89	A	HSUSB_VRES
90	P	HSUSB_VDD33
91	I/O	HSUSB_VBUS
92	A	HSUSB_D-
93	P	HSUSB_VSS
94	A	HSUSB_D+
95	A	HSUSB_VDD12_CAP
96	I	HSUSB_ID
97	I/O	PE.7 / SD0_CMD / UART5_TXD / CAN1_TXD / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / PSIO0_CH0
98	I/O	PE.6 / SD0_CLK / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CAN1_RXD / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / PSIO0_CH1
99	I/O	PE.5 / EBI_nRD / SD0_DAT3 / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / PSIO0_CH2
100	I/O	PE.4 / EBI_nWR / SD0_DAT2 / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / PSIO0_CH3
101	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / EQEI0_A / EPWM0_CH4 / BPWM0_CH1
102	I/O	PE.2 / EBI_ALE / SD0_DAT0 / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / EQEI0_B / EPWM0_CH5 / BPWM0_CH0
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS
106	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS
107	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD
108	I/O	PH.9 / EBI_AD13 / QSPI0_SS / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD
109	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / SPI1_I2SMCLK / UART4_TXD / UART0_TXD
110	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5
111	I/O	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SPI0_I2SMCLK / EPWM0_CH4
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EBI_AD11 / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / TM1
116	I/O	PB.15 / EADC0_CH15 / EBI_AD12 / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / EPWM0_BRAKE1 / EPWM1_CH0 / TM0_EXT / PSIO0_CH0 / KPI_COL0

Pin	Type	M463KGCAE Pin Function
117	I/O	PB.14 / EADC0_CH14 / EBI_AD13 / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / EPWM1_CH1 / TM1_EXT / CLKO / PSIO0_CH1 / KPI_COL1
118	I/O	PB.13 / EADC0_CH13 / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / EPWM1_CH2 / TM2_EXT / PSIO0_CH2 / KPI_COL2
119	I/O	PB.12 / EADC0_CH12 / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / EPWM1_CH3 / TM3_EXT / PSIO0_CH3 / KPI_COL3
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / HSUSB_VBUS_ST
124	I/O	PB.10 / EADC0_CH10 / EBI_ADR17 / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS / HSUSB_VBUS_EN
125	I/O	PB.9 / EADC0_CH9 / EBI_ADR18 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / INT7
126	I/O	PB.8 / EADC0_CH8 / EBI_ADR19 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / INT6
127	I/O	PB.7 / EADC0_CH7 / EBI_nWRL / CAN1_TXD / UART1_TXD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / ACMP0_O / KPI_COL4 / SPI1_CLK
128	I/O	PB.6 / EADC0_CH6 / EBI_nWRH / CAN1_RXD / UART1_RXD / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / ACMP1_O / KPI_COL5 / SPI1_SS

Table 4.1-4 M463KGCAE Multi-function Pin Table

4.1.4 M467 Series Multi-function Pin Diagram

4.1.4.1 M467 Series LQFP64-Pin Multi-function Pin Diagram

Corresponding Part Number: M467SJHAN

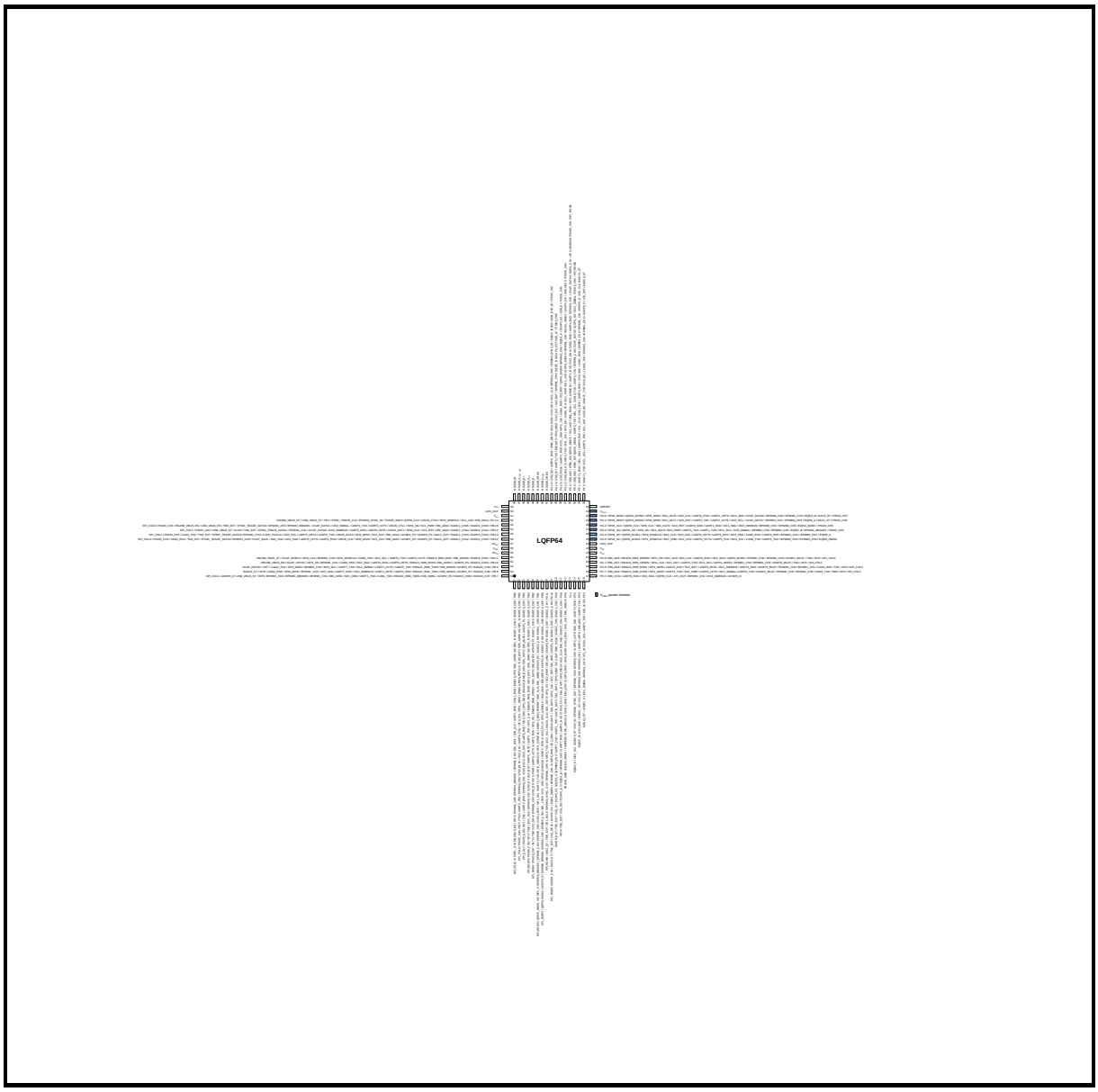


Figure 4.1-13 M467 Series LQFP64-Pin Multi-function Pin Diagram

Pin	Type	M467SJHAN Pin Function
1	I/O	PB.6 / EADC0_CH6 / EADC2_CH14 / ACMP2_N / EBI_nWRH / EMAC0_PPS / CAN1_RXD / UART1_RXD / SD1_CLK / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / KPI_COL5
2	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
3	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 /

Pin	Type	M467SJHAN Pin Function
		PSIO0_CH5 / KPI_COL7
4	I/O	PB.3 / EADC0_CH3 / EADC1_CH11 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0
5	I/O	PB.2 / EADC0_CH2 / EADC1_CH10 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
6	I/O	PB.1 / EADC0_CH1 / EADC1_CH9 / EADC2_CH9 / ACMP3_P0 / EBI_ADR8 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / KPI_ROW2
7	I/O	PB.0 / EADC0_CH0 / EADC1_CH8 / EADC2_CH8 / ACMP3_N / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / KPI_ROW3
8	I/O	PA.11 / EADC1_CH7 / EADC2_CH7 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4
9	I/O	PA.10 / EADC1_CH6 / EADC2_CH6 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5
10	I/O	PA.9 / EADC1_CH5 / EADC2_CH5 / EBI_MCLK / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
11	I/O	PA.8 / EADC1_CH4 / EADC2_CH4 / EBI_ALE / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
12	I/O	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / CAN2_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
13	P	V_{BAT}
14	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL / EQEI2_A
15	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EADC1_ST / I2C4_SDA / EQEI2_B
16	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / XT1_IN / BPWM1_CH0 / I2C4_SMBAL / ACMP2_O / EADC2_ST
17	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS / ACMP3_O
18	I/O	PC.7 / EBI_AD9 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / CAN3_TXD / TM0 / INT3 / KPI_COL3
19	I/O	PC.6 / EBI_AD8 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / CAN3_RXD / TM1 / INT2 / KPI_COL2
20	I/O	PA.7 / EBI_AD7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
21	I/O	PA.6 / EBI_AD6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
22	P	V_{SS}
23	P	V_{DD}
24	A	LDO_CAP

Pin	Type	M467SJHAN Pin Function
25	I/O	PA.5 / SPIM_D2 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
26	I/O	PA.4 / SPIM_D3 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
27	I/O	PA.3 / SPIM_SS / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
28	I/O	PA.2 / SPIM_CLK / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / PSIO0_CH5
29	I/O	PA.1 / SPIM_MISO / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / PSIO0_CH6
30	I/O	PA.0 / SPIM_MOSI / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7
31	P	V_{DDIO}
32	I	nRESET
33	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
34	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / EADC1_ST
35	I/O	PC.5 / EBI_AD5 / SPIM_D2 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / QSPI1_SS / I2C3_SMBAL / PSIO0_CH0 / KPI_ROW0
36	I/O	PC.4 / EBI_AD4 / SPIM_D3 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / QSPI1_CLK / I2C3_SMBSUS / PSIO0_CH1 / KPI_ROW1
37	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / ECAP3_IC0 / USB_VBUS / PSIO0_CH4
38	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / ECAP3_IC1 / USB_D- / PSIO0_CH5
39	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / ECAP3_IC2 / USB_D+ / PSIO0_CH6
40	I/O	PA.15 / I2S0_DO / UART0_RXD / SPIM_MOSI / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7
41	A	HSUSB_VRES
42	P	HSUSB_VDD33
43	I/O	HSUSB_VBUS
44	A	HSUSB_D-
45	P	HSUSB_VSS
46	A	HSUSB_D+
47	A	HSUSB_VDD12_CAP
48	I	HSUSB_ID
49	P	V_{SS}
50	A	LDO_CAP

Pin	Type	M467SJHAN Pin Function
51	P	V_{DD}
52	I/O	PC.14 / EBI_AD11 / SC1_nCD / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / ETMC_TRACE_CLK / TM1 / USB_VBUS_ST / HSUSB_VBUS_ST
53	I/O	PB.15 / EADC0_CH15 / EADC1_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 / ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0
54	I/O	PB.14 / EADC0_CH14 / EADC1_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1
55	I/O	PB.13 / EADC0_CH13 / EADC1_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / CAN3_TXD / PSIO0_CH2 / KPI_COL2
56	I/O	PB.12 / EADC0_CH12 / EADC1_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / CAN3_RXD / PSIO0_CH3 / KPI_COL3
57	P	AV_{DD}
58	A	V_{REF}
59	P	AV_{SS}
60	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST
61	I/O	PB.10 / EADC0_CH10 / ACMP2_P3 / EBI_ADR17 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN
62	I/O	PB.9 / EADC0_CH9 / ACMP2_P2 / EBI_ADR18 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / CAN2_TXD / INT7 / CCAP_HSYNC
63	I/O	PB.8 / EADC0_CH8 / ACMP2_P1 / EBI_ADR19 / EMAC0_RMII_TXD1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / CAN2_RXD / INT6 / EADC2_ST
64	I/O	PB.7 / EADC0_CH7 / EADC2_CH15 / ACMP2_P0 / EBI_nWRL / EMAC0_RMII_TXEN / CAN1_TXD / UART1_TXD / SD1_CMD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / KPI_COL4

Table 4.1-5 M467SJHAN Multi-function Pin Table

4.1.4.2 M467 Series LQFP128-Pin Multi-function Pin Diagram

Corresponding Part Number: M467KJHAN

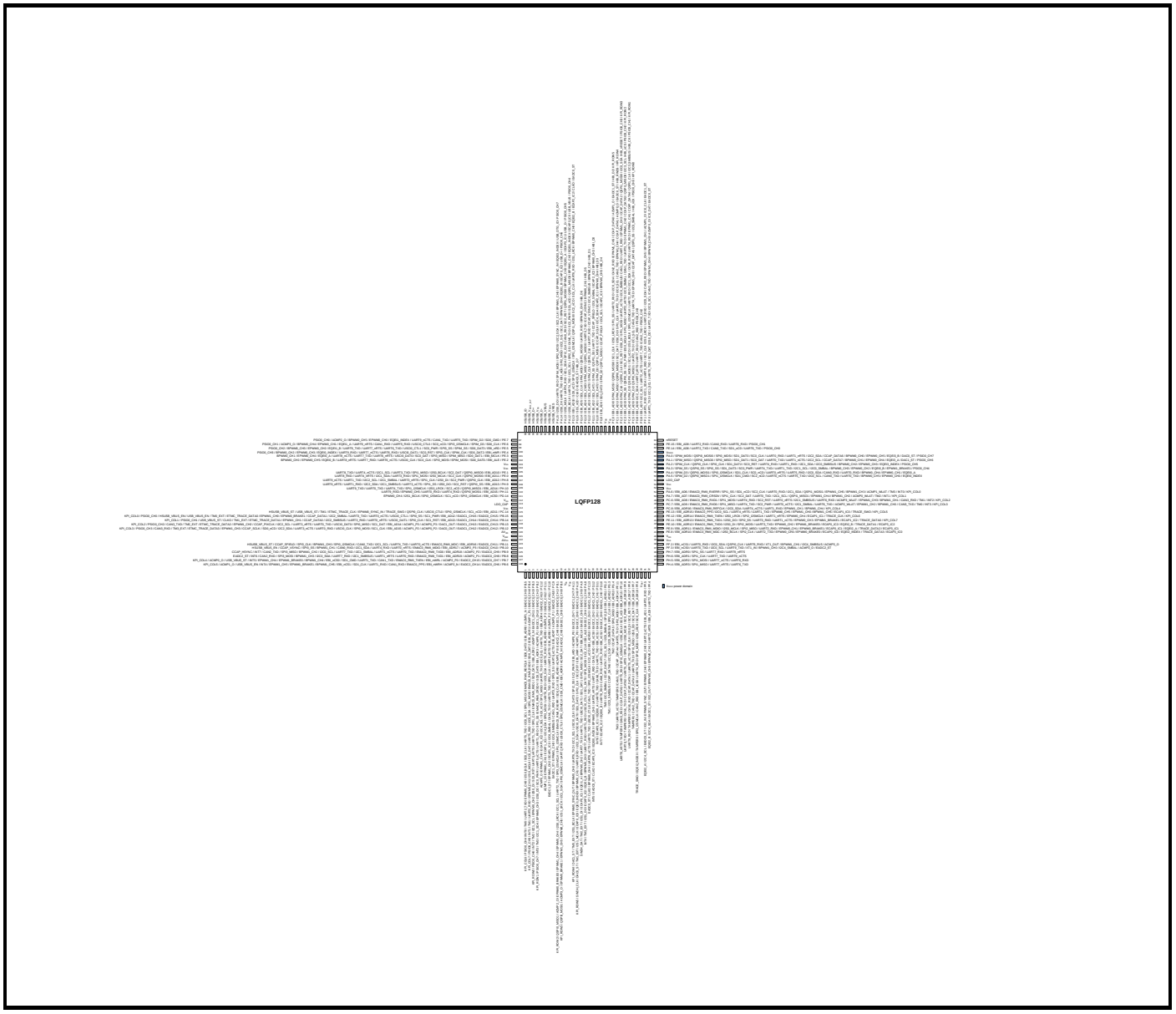


Figure 4.1-14 M467 Series LQFP128-Pin Multi-function Pin Diagram

Pin	Type	M467KJHAN Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / EADC1_CH11 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0

Pin	Type	M467KJHAN Pin Function
4	I/O	PB.2 / EADC0_CH2 / EADC1_CH10 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
5	I/O	PC.12 / EADC2_CH13 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / I2C4_SCL / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EADC2_CH12 / ACMP3_P3 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / I2C4_SDA / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EADC2_CH11 / ACMP3_P2 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CAN1_TXD / I2C4_SMBAL / ECAP1_IC0 / EPWM1_CH2 / EADC1_ST
8	I/O	PC.9 / EADC2_CH10 / ACMP3_P1 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CAN1_RXD / I2C4_SMBSUS / EPWM1_CH3 / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / EADC1_CH9 / EADC2_CH9 / ACMP3_P0 / EBI_ADR8 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / KPI_ROW2
10	I/O	PB.0 / EADC0_CH0 / EADC1_CH8 / EADC2_CH8 / ACMP3_N / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / KPI_ROW3
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC1_CH7 / EADC2_CH7 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4
14	I/O	PA.10 / EADC1_CH6 / EADC2_CH6 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5
15	I/O	PA.9 / EADC1_CH5 / EADC2_CH5 / EBI_MCLK / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
16	I/O	PA.8 / EADC1_CH4 / EADC2_CH4 / EBI_ALE / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
17	I/O	PC.13 / EADC1_CH3 / EADC2_CH3 / EBI_ADR10 / SC2_nCD / SPI2_I2SMCLK / CAN1_TXD / USCI0_CTL0 / UART2_TXD / UART8_nCTS / BPWM0_CH4 / CLKO / EADC0_ST
18	I/O	PD.12 / EADC1_CH2 / EADC2_CH2 / EBI_nCS0 / CAN1_RXD / UART2_RXD / UART8_nRTS / BPWM0_CH5 / EQEI0_INDEX / ECAP3_IC0 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EADC1_CH1 / EADC2_CH1 / EBI_nCS1 / UART1_TXD / CAN0_TXD / UART8_TXD / EQEI0_A / ECAP3_IC1 / INT6
20	I/O	PD.10 / EADC1_CH0 / EADC2_CH0 / EBI_nCS2 / UART1_RXD / CAN0_RXD / UART8_RXD / EQEI0_B / ECAP3_IC2 / INT7
21	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / CCAP_DATA7 / I2C3_SMBAL / TM0
22	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / CCAP_DATA6 / I2C3_SMBSUS / TM1
23	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / CCAP_DATA5 / TM2
24	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / CCAP_DATA4 / CAN3_TXD / TAMPER5 / UART9_nCTS / TM3
25	I/O	PF.10 / EBI_ADR15 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / CCAP_DATA3 / CAN3_RXD / TAMPER4 / UART9_nRTS
26	I/O	PF.9 / EBI_ADR16 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / CCAP_DATA2 / CAN1_TXD / TAMPER3 / UART9_TXD

Pin	Type	M467KJHAN Pin Function
27	I/O	PF.8 / EBI_ADR17 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / CCAP_DATA1 / CAN1_RXD / TAMPER2 / UART9_RXD
28	I/O	PF.7 / EBI_ADR18 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / CCAP_DATA0 / CAN2_TXD / TAMPER1
29	I/O	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / CAN2_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
30	P	V_{BAT}
31	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL / EQEI2_A
32	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EADC1_ST / I2C4_SDA / EQEI2_B
33	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
34	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD
35	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD / UART9_nCTS
36	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD / UART9_nRTS
37	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / XT1_IN / BPWM1_CH0 / I2C4_SMBAL / ACMP2_O / EADC2_ST
38	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS / ACMP3_O
39	P	V_{SS}
40	P	V_{DD}
41	I/O	PE.8 / EBI_ADR10 / EMAC0_RMII_MDC / I2S0_BCLK / SPI2_CLK / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / EQEI2_INDEX / TRACE_DATA3 / ECAP3_IC0
42	I/O	PE.9 / EBI_ADR11 / EMAC0_RMII_MDIO / I2S0_MCLK / SPI2_MISO / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / EQEI2_A / TRACE_DATA2 / ECAP3_IC1
43	I/O	PE.10 / EBI_ADR12 / EMAC0_RMII_TXD0 / I2S0_DI / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / EQEI2_B / TRACE_DATA1 / ECAP3_IC2
44	I/O	PE.11 / EBI_ADR13 / EMAC0_RMII_TXD1 / I2S0_DO / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / KPI_COL7
45	I/O	PE.12 / EBI_ADR14 / EMAC0_RMII_TXEN / I2S0_LRCK / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / KPI_COL6
46	I/O	PE.13 / EBI_ADR15 / EMAC0_PPS / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5
47	I/O	PC.8 / EBI_ADR16 / EMAC0_RMII_REFCLK / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / KPI_COL4
48	I/O	PC.7 / EBI_AD9 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / CAN3_TXD / TM0 / INT3 / KPI_COL3
49	I/O	PC.6 / EBI_AD8 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / CAN3_RXD / TM1 / INT2 / KPI_COL2
50	I/O	PA.7 / EBI_AD7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
51	I/O	PA.6 / EBI_AD6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0

Pin	Type	M467KJHAN Pin Function
52	P	V_{SS}
53	P	V_{DD}
54	A	LDO_CAP
55	I/O	PA.5 / SPIM_D2 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
56	I/O	PA.4 / SPIM_D3 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
57	I/O	PA.3 / SPIM_SS / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
58	I/O	PA.2 / SPIM_CLK / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / PSIO0_CH5
59	I/O	PA.1 / SPIM_MISO / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / PSIO0_CH6
60	I/O	PA.0 / SPIM_MOSI / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7
61	P	V_{DDIO}
62	I/O	PE.14 / EBI_AD8 / UART2_TXD / CAN0_TXD / SD1_nCD / UART6_TXD / PSIO0_CH0
63	I/O	PE.15 / EBI_AD9 / UART2_RXD / CAN0_RXD / UART6_RXD / PSIO0_CH1
64	I	nRESET
65	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
66	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / EADC1_ST
67	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD / CAN2_TXD / PSIO0_CH2
68	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD / CAN2_RXD / PSIO0_CH3
69	I/O	PC.5 / EBI_AD5 / SPIM_D2 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / QSPI1_SS / I2C3_SMBAL / HBI_nCK / PSIO0_CH0 / KPI_ROW0
70	I/O	PC.4 / EBI_AD4 / SPIM_D3 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / QSPI1_CLK / I2C3_SMBSUS / HBI_CK / PSIO0_CH1 / KPI_ROW1
71	I/O	PC.3 / EBI_AD3 / SPIM_SS / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CAN1_TXD / UART3_TXD / EPWM1_CH2 / CCAP_DATA3 / QSPI1_MISO0 / I2C3_SCL / HBI_nCS / PSIO0_CH2 / KPI_ROW2
72	I/O	PC.2 / EBI_AD2 / SPIM_CLK / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD / EPWM1_CH3 / CCAP_DATA2 / QSPI1_MOSI0 / I2C3_SDA / HBI_nRESET / PSIO0_CH3 / KPI_ROW3
73	I/O	PC.1 / EBI_AD1 / SPIM_MISO / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / HBI_RWDS / KPI_ROW4
74	I/O	PC.0 / EBI_AD0 / SPIM_MOSI / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / EADC1_ST / HBI_D2 / KPI_ROW5
75	P	V_{SS}

Pin	Type	M467KJHAN Pin Function
76	P	V_{DD}
77	I/O	PG.9 / EBI_AD0 / SD1_DAT3 / SPIM_D2 / QSPI1_MISO1 / CCAP_PIXCLK / I2C4_SCL / ECAP2_IC0 / BPWM0_CH5 / HBI_D4
78	I/O	PG.10 / EBI_AD1 / SD1_DAT2 / SPIM_D3 / QSPI1_MOSI1 / CCAP_SCLK / I2C4_SDA / ECAP2_IC1 / BPWM0_CH4 / HBI_D3
79	I/O	PG.11 / EBI_AD2 / SD1_DAT1 / SPIM_SS / QSPI1_SS / UART7_TXD / CCAP_SFIELD / I2C4_SMBAL / ECAP2_IC2 / BPWM0_CH3 / HBI_D0
80	I/O	PG.12 / EBI_AD3 / SD1_DAT0 / SPIM_CLK / QSPI1_CLK / UART7_RXD / CCAP_VSYNC / I2C4_SMBSUS / BPWM0_CH2 / HBI_D1
81	I/O	PG.13 / EBI_AD4 / SD1_CMD / SPIM_MISO / QSPI1_MISO0 / UART6_TXD / CCAP_HSYNC / BPWM0_CH1 / HBI_D5
82	I/O	PG.14 / EBI_AD5 / SD1_CLK / SPIM_MOSI / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0 / HBI_D6
83	I/O	PG.15 / SD1_nCD / CLKO / EADC0_ST / HBI_D7
84	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / SC2_nCD / SD1_CLK / UART6_RXD / I2S1_LRCK / BPWM0_CH0 / EQEI2_B / ECAP2_IC2 / CLKO / EADC0_ST
85	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / ECAP3_IC0 / USB_VBUS / PSIO0_CH4
86	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / ECAP3_IC1 / USB_D- / PSIO0_CH5
87	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / ECAP3_IC2 / USB_D+ / PSIO0_CH6
88	I/O	PA.15 / I2S0_DO / UART0_RXD / SPIM_MOSI / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7
89	A	HSUSB_VRES
90	P	HSUSB_VDD33
91	I/O	HSUSB_VBUS
92	A	HSUSB_D-
93	P	HSUSB_VSS
94	A	HSUSB_D+
95	A	HSUSB_VDD12_CAP
96	I	HSUSB_ID
97	I/O	PE.7 / SD0_CMD / SPIM_D2 / UART5_TXD / CAN1_TXD / UART9_nCTS / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / ACMP2_O / PSIO0_CH0
98	I/O	PE.6 / SD0_CLK / SPIM_D3 / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CAN1_RXD / UART9_nRTS / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / ACMP3_O / PSIO0_CH1
99	I/O	PE.5 / EBI_nRD / SD0_DAT3 / SPIM_SS / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / UART9_TXD / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / PSIO0_CH2
100	I/O	PE.4 / EBI_nWR / SD0_DAT2 / SPIM_CLK / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / UART9_RXD / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / PSIO0_CH3
101	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / SPIM_MISO / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / UART8_nCTS / EQEI0_A / EPWM0_CH4 / BPWM0_CH1
102	I/O	PE.2 / EBI_ALE / SD0_DAT0 / SPIM_MOSI / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / UART8_nRTS / EQEI0_B / EPWM0_CH5 / BPWM0_CH0

Pin	Type	M467KJHAN Pin Function
103	P	V_{SS}
104	P	V_{DD}
105	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD
106	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD
107	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / UART9_nCTS
108	I/O	PH.9 / EBI_AD13 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / UART9_nRTS
109	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / UART9_TXD
110	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / UART9_RXD
111	I/O	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SC1_nCD / SPI0_I2SMCLK / I2S1_BCLK / EPWM0_CH4
112	P	V_{SS}
113	A	LDO_CAP
114	P	V_{DD}
115	I/O	PC.14 / EBI_AD11 / SC1_nCD / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / ETMC_TRACE_CLK / TM1 / USB_VBUS_ST / HSUSB_VBUS_ST
116	I/O	PB.15 / EADC0_CH15 / EADC1_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 / ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0
117	I/O	PB.14 / EADC0_CH14 / EADC1_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1
118	I/O	PB.13 / EADC0_CH13 / EADC1_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / CAN3_TXD / PSIO0_CH2 / KPI_COL2
119	I/O	PB.12 / EADC0_CH12 / EADC1_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / CAN3_RXD / PSIO0_CH3 / KPI_COL3
120	P	AV_{DD}
121	A	V_{REF}
122	P	AV_{SS}
123	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST
124	I/O	PB.10 / EADC0_CH10 / ACMP2_P3 / EBI_ADR17 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN
125	I/O	PB.9 / EADC0_CH9 / ACMP2_P2 / EBI_ADR18 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / CAN2_TXD / INT7 / CCAP_HSYNC
126	I/O	PB.8 / EADC0_CH8 / ACMP2_P1 / EBI_ADR19 / EMAC0_RMII_TXD1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / CAN2_RXD / INT6 / EADC2_ST

Pin	Type	M467KJHAN Pin Function
127	I/O	PB.7 / EADC0_CH7 / EADC2_CH15 / ACMP2_P0 / EBI_nWRL / EMAC0_RMII_TXEN / CAN1_TXD / UART1_TXD / SD1_CMD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / KPI_COL4
128	I/O	PB.6 / EADC0_CH6 / EADC2_CH14 / ACMP2_N / EBI_nWRH / EMAC0_PPS / CAN1_RXD / UART1_RXD / SD1_CLK / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / KPI_COL5

Table 4.1-6 M467KJHAN Multi-function Pin Table

4.1.4.3 M467 Series LQFP144-Pin Multi-function Pin Diagram

Corresponding Part Number: M467JJHAN

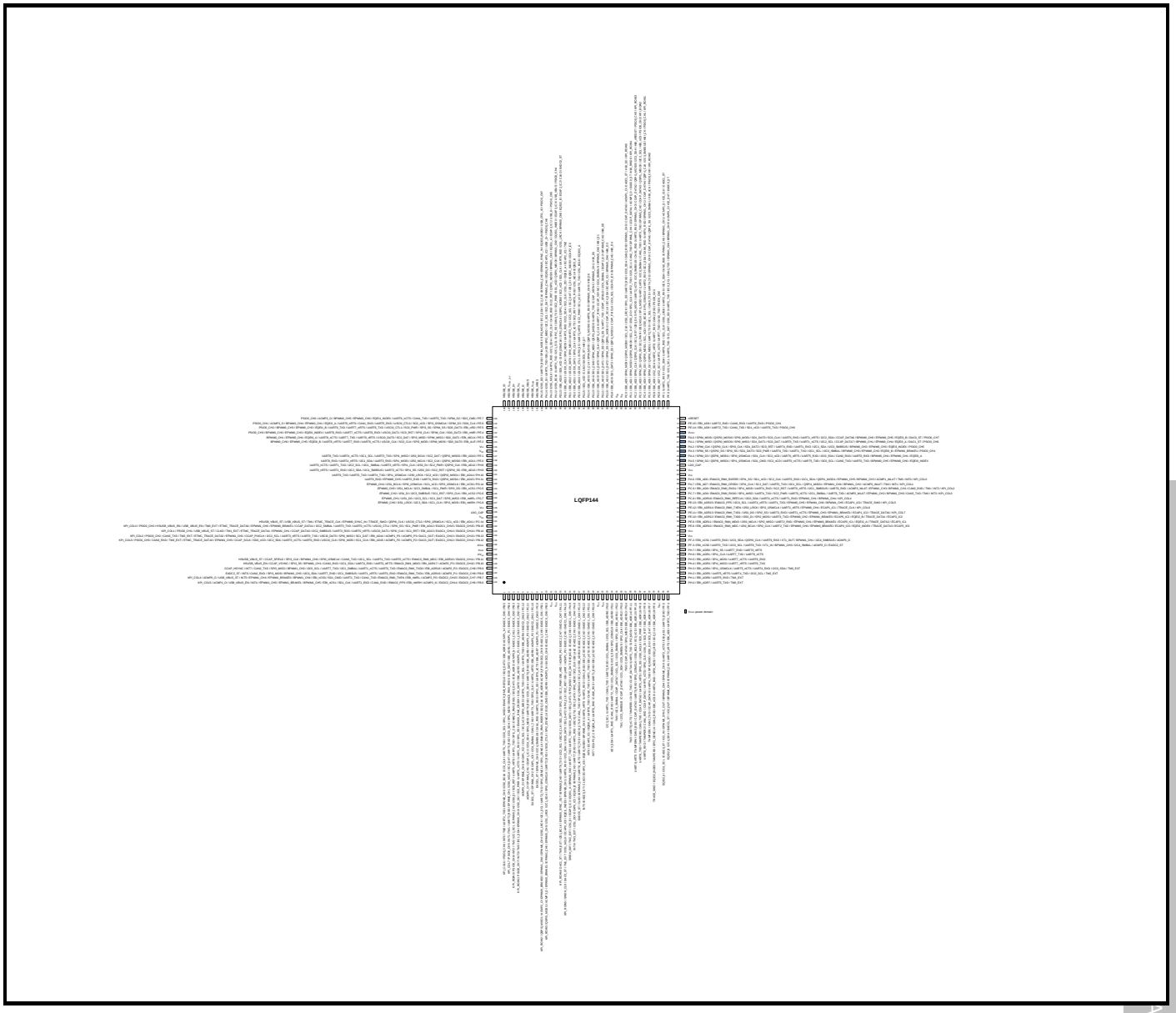


Figure 4.1-15 M467 Series LQFP144-Pin Multi-function Pin Diagram

Pin	Type	M467JJHAN Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / EADC1_CH11 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0

Pin	Type	M467JJHAN Pin Function
4	I/O	PB.2 / EADC0_CH2 / EADC1_CH10 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
5	I/O	PC.12 / EADC2_CH13 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / I2C4_SCL / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EADC2_CH12 / ACMP3_P3 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / I2C4_SDA / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EADC2_CH11 / ACMP3_P2 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CAN1_TXD / I2C4_SMBAL / ECAP1_IC0 / EPWM1_CH2 / EADC1_ST
8	I/O	PC.9 / EADC2_CH10 / ACMP3_P1 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CAN1_RXD / I2C4_SMBSUS / EPWM1_CH3 / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / EADC1_CH9 / EADC2_CH9 / ACMP3_P0 / EBI_ADR8 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / KPI_ROW2
10	I/O	PB.0 / EADC0_CH0 / EADC1_CH8 / EADC2_CH8 / ACMP3_N / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / KPI_ROW3
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC1_CH7 / EADC2_CH7 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4
14	I/O	PA.10 / EADC1_CH6 / EADC2_CH6 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5
15	I/O	PA.9 / EADC1_CH5 / EADC2_CH5 / EBI_MCLK / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
16	I/O	PA.8 / EADC1_CH4 / EADC2_CH4 / EBI_ALE / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
17	I/O	PC.13 / EADC1_CH3 / EADC2_CH3 / EBI_ADR10 / SC2_nCD / SPI2_I2SMCLK / CAN1_TXD / USCI0_CTL0 / UART2_TXD / UART8_nCTS / BPWM0_CH4 / CLKO / EADC0_ST
18	I/O	PD.12 / EADC1_CH2 / EADC2_CH2 / EBI_nCS0 / CAN1_RXD / UART2_RXD / UART8_nRTS / BPWM0_CH5 / EQEI0_INDEX / ECAP3_IC0 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EADC1_CH1 / EADC2_CH1 / EBI_nCS1 / UART1_TXD / CAN0_TXD / UART8_TXD / EQEI0_A / ECAP3_IC1 / INT6
20	I/O	PD.10 / EADC1_CH0 / EADC2_CH0 / EBI_nCS2 / UART1_RXD / CAN0_RXD / UART8_RXD / EQEI0_B / ECAP3_IC2 / INT7
21	P	V_{SS}
22	P	V_{DD}
23	I/O	PG.0 / EBI_ADR8 / I2C0_SCL / I2C1_SMBAL / UART2_RXD / CAN1_TXD / UART1_TXD / I2C3_SCL
24	I/O	PG.1 / EBI_ADR9 / SPI2_I2SMCLK / I2C0_SDA / I2C1_SMBSUS / UART2_TXD / CAN1_RXD / UART1_RXD / I2C3_SDA
25	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / CCAP_DATA7 / I2C3_SMBAL / TM0
26	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / CCAP_DATA6 / I2C3_SMBSUS / TM1
27	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / CCAP_DATA5 / TM2

Pin	Type	M467JJHAN Pin Function
28	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / CCAP_DATA4 / CAN3_TXD / TAMPER5 / UART9_nCTS / TM3
29	I/O	PF.10 / EBI_ADR15 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / CCAP_DATA3 / CAN3_RXD / TAMPER4 / UART9_nRTS
30	I/O	PF.9 / EBI_ADR16 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / CCAP_DATA2 / CAN1_TXD / TAMPER3 / UART9_TXD
31	I/O	PF.8 / EBI_ADR17 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / CCAP_DATA1 / CAN1_RXD / TAMPER2 / UART9_RXD
32	I/O	PF.7 / EBI_ADR18 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / CCAP_DATA0 / CAN2_TXD / TAMPER1
33	I/O	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / CAN2_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
34	P	V_{BAT}
35	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL / EQEI2_A
36	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EADC1_ST / I2C4_SDA / EQEI2_B
37	I/O	PH.0 / EBI_ADR7 / UART5_TXD / TM0_EXT
38	I/O	PH.1 / EBI_ADR6 / UART5_RXD / TM1_EXT
39	I/O	PH.2 / EBI_ADR5 / UART5_nRTS / UART4_TXD / I2C0_SCL / TM2_EXT
40	I/O	PH.3 / EBI_ADR4 / SPI1_I2SMCLK / UART5_nCTS / UART4_RXD / I2C0_SDA / TM3_EXT
41	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
42	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD
43	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD / UART9_nCTS
44	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD / UART9_nRTS
45	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / XT1_IN / BPWM1_CH0 / I2C4_SMBAL / ACMP2_O / EADC2_ST
46	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS / ACMP3_O
47	P	V_{SS}
48	P	V_{DD}
49	I/O	PE.8 / EBI_ADR10 / EMAC0_RMII_MDC / I2S0_BCLK / SPI2_CLK / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / EQEI2_INDEX / TRACE_DATA3 / ECAP3_IC0
50	I/O	PE.9 / EBI_ADR11 / EMAC0_RMII_MDIO / I2S0_MCLK / SPI2_MISO / UART2_RXD / EPWM0_CH1 / EPWM0_BRAKE1 / ECAP0_IC1 / EQEI2_A / TRACE_DATA2 / ECAP3_IC1
51	I/O	PE.10 / EBI_ADR12 / EMAC0_RMII_TXD0 / I2S0_DI / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / EQEI2_B / TRACE_DATA1 / ECAP3_IC2
52	I/O	PE.11 / EBI_ADR13 / EMAC0_RMII_TXD1 / I2S0_DO / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / KPI_COL7
53	I/O	PE.12 / EBI_ADR14 / EMAC0_RMII_TXEN / I2S0_LRCK / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / KPI_COL6
54	I/O	PE.13 / EBI_ADR15 / EMAC0_PPS / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5

Pin	Type	M467JJHAN Pin Function
55	I/O	PC.8 / EBI_ADR16 / EMAC0_RMII_REFCLK / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / KPI_COL4
56	I/O	PC.7 / EBI_AD9 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / CAN3_TXD / TM0 / INT3 / KPI_COL3
57	I/O	PC.6 / EBI_AD8 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / CAN3_RXD / TM1 / INT2 / KPI_COL2
58	I/O	PA.7 / EBI_AD7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
59	I/O	PA.6 / EBI_AD6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
60	P	V_{SS}
61	P	V_{DD}
62	A	LDO_CAP
63	I/O	PA.5 / SPIM_D2 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
64	I/O	PA.4 / SPIM_D3 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
65	I/O	PA.3 / SPIM_SS / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
66	I/O	PA.2 / SPIM_CLK / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / PSIO0_CH5
67	I/O	PA.1 / SPIM_MISO / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / PSIO0_CH6
68	I/O	PA.0 / SPIM_MOSI / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7
69	P	V_{DDIO}
70	I/O	PE.14 / EBI_AD8 / UART2_TXD / CAN0_TXD / SD1_nCD / UART6_TXD / PSIO0_CH0
71	I/O	PE.15 / EBI_AD9 / UART2_RXD / CAN0_RXD / UART6_RXD / PSIO0_CH1
72	I	nRESET
73	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
74	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / EADC1_ST
75	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD / CAN2_TXD / PSIO0_CH2
76	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD / CAN2_RXD / PSIO0_CH3
77	I/O	PC.5 / EBI_AD5 / SPIM_D2 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / QSPI1_SS / I2C3_SMBAL / HBI_nCK / PSIO0_CH0 / KPI_ROW0
78	I/O	PC.4 / EBI_AD4 / SPIM_D3 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / QSPI1_CLK / I2C3_SMBSUS / HBI_CK / PSIO0_CH1 / KPI_ROW1
79	I/O	PC.3 / EBI_AD3 / SPIM_SS / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS /

Pin	Type	M467JJHAN Pin Function
		I2C0_SMBAL / CAN1_TXD / UART3_TXD / EPWM1_CH2 / CCAP_DATA3 / QSPI1_MISO0 / I2C3_SCL / HBI_nCS / PSIO0_CH2 / KPI_ROW2
80	I/O	PC.2 / EBI_AD2 / SPIM_CLK / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD / EPWM1_CH3 / CCAP_DATA2 / QSPI1_MOSI0 / I2C3_SDA / HBI_nRESET / PSIO0_CH3 / KPI_ROW3
81	I/O	PC.1 / EBI_AD1 / SPIM_MISO / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / HBI_RWDS / KPI_ROW4
82	I/O	PC.0 / EBI_AD0 / SPIM_MOSI / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / EADC1_ST / HBI_D2 / KPI_ROW5
83	P	V_{SS}
84	P	V_{DD}
85	I/O	PG.9 / EBI_AD0 / SD1_DAT3 / SPIM_D2 / QSPI1_MISO1 / CCAP_PIXCLK / I2C4_SCL / ECAP2_IC0 / BPWM0_CH5 / HBI_D4
86	I/O	PG.10 / EBI_AD1 / SD1_DAT2 / SPIM_D3 / QSPI1_MOSI1 / CCAP_SCLK / I2C4_SDA / ECAP2_IC1 / BPWM0_CH4 / HBI_D3
87	I/O	PG.11 / EBI_AD2 / SD1_DAT1 / SPIM_SS / QSPI1_SS / UART7_TXD / CCAP_SFIELD / I2C4_SMBAL / ECAP2_IC2 / BPWM0_CH3 / HBI_D0
88	I/O	PG.12 / EBI_AD3 / SD1_DAT0 / SPIM_CLK / QSPI1_CLK / UART7_RXD / CCAP_VSYNC / I2C4_SMBSUS / BPWM0_CH2 / HBI_D1
89	I/O	PG.13 / EBI_AD4 / SD1_CMD / SPIM_MISO / QSPI1_MISO0 / UART6_TXD / CCAP_HSYNC / BPWM0_CH1 / HBI_D5
90	I/O	PG.14 / EBI_AD5 / SD1_CLK / SPIM_MOSI / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0 / HBI_D6
91	I/O	PG.15 / SD1_nCD / CLKO / EADC0_ST / HBI_D7
92	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / SC2_PWR / SC1_nCD / UART0_TXD / I2S1_BCLK / EQEI3_A
93	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / SC2_RST / UART0_RXD / I2S1_MCLK / EQEI3_B
94	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL / SC2_DAT / I2S1_DI / EQEI2_INDEX / ECAP2_IC0
95	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / SC2_CLK / I2S1_DO / EQEI2_A / ECAP2_IC1 / TM2
96	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / SC2_nCD / SD1_CLK / UART6_RXD / I2S1_LRCK / BPWM0_CH0 / EQEI2_B / ECAP2_IC2 / CLKO / EADC0_ST
97	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / ECAP3_IC0 / USB_VBUS / PSIO0_CH4
98	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / ECAP3_IC1 / USB_D- / PSIO0_CH5
99	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / ECAP3_IC2 / USB_D+ / PSIO0_CH6
100	I/O	PA.15 / I2S0_DO / UART0_RXD / SPIM_MOSI / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7
101	A	HSUSB_VRES
102	P	HSUSB_VDD33
103	I/O	HSUSB_VBUS

Pin	Type	M467JJHAN Pin Function
104	A	HSUSB_D-
105	P	HSUSB_VSS
106	A	HSUSB_D+
107	A	HSUSB_VDD12_CAP
108	I	HSUSB_ID
109	I/O	PE.7 / SD0_CMD / SPIM_D2 / UART5_TXD / CAN1_TXD / UART9_nCTS / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / ACMP2_O / PSIO0_CH0
110	I/O	PE.6 / SD0_CLK / SPIM_D3 / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CAN1_RXD / UART9_nRTS / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / ACMP3_O / PSIO0_CH1
111	I/O	PE.5 / EBI_nRD / SD0_DAT3 / SPIM_SS / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / UART9_TXD / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / PSIO0_CH2
112	I/O	PE.4 / EBI_nWR / SD0_DAT2 / SPIM_CLK / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / UART9_RXD / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / PSIO0_CH3
113	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / SPIM_MISO / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / UART8_nCTS / EQEI0_A / EPWM0_CH4 / BPWM0_CH1
114	I/O	PE.2 / EBI_ALE / SD0_DAT0 / SPIM_MOSI / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / UART8_nRTS / EQEI0_B / EPWM0_CH5 / BPWM0_CH0
115	P	V_{SS}
116	P	V_{DD}
117	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD
118	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD
119	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / UART9_nCTS
120	I/O	PH.9 / EBI_AD13 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / UART9_nRTS
121	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / UART9_TXD
122	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / UART9_RXD
123	I/O	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SC1_nCD / SPI0_I2SMCLK / I2S1_BCLK / EPWM0_CH4
124	I/O	PG.5 / EBI_nCS1 / SPI3_SS / SC1_PWR / I2C3_SMBAL / I2S1_MCLK / EPWM0_CH3
125	I/O	PG.6 / EBI_nCS2 / SPI3_CLK / SC1_RST / I2C3_SMBSUS / I2S1_DI / EPWM0_CH2
126	I/O	PG.7 / EBI_nWRL / SPI3_MISO / SC1_DAT / I2C3_SCL / I2S1_DO / EPWM0_CH1
127	I/O	PG.8 / EBI_nWRH / SPI3_MOSI / SC1_CLK / I2C3_SDA / I2S1_LRCK / EPWM0_CH0
128	P	V_{SS}
129	A	LDO_CAP
130	P	V_{DD}
131	I/O	PC.14 / EBI_AD11 / SC1_nCD / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / ETMC_TRACE_CLK / TM1 / USB_VBUS_ST / HSUSB_VBUS_ST
132	I/O	PB.15 / EADC0_CH15 / EADC1_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 /

Pin	Type	M467JJHAN Pin Function
		ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0
133	I/O	PB.14 / EADC0_CH14 / EADC1_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1
134	I/O	PB.13 / EADC0_CH13 / EADC1_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / CAN3_TXD / PSIO0_CH2 / KPI_COL2
135	I/O	PB.12 / EADC0_CH12 / EADC1_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / CAN3_RXD / PSIO0_CH3 / KPI_COL3
136	P	AV_{DD}
137	A	V_{REF}
138	P	AV_{SS}
139	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST
140	I/O	PB.10 / EADC0_CH10 / ACMP2_P3 / EBI_ADR17 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN
141	I/O	PB.9 / EADC0_CH9 / ACMP2_P2 / EBI_ADR18 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / CAN2_TXD / INT7 / CCAP_HSYNC
142	I/O	PB.8 / EADC0_CH8 / ACMP2_P1 / EBI_ADR19 / EMAC0_RMII_TXD1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / CAN2_RXD / INT6 / EADC2_ST
143	I/O	PB.7 / EADC0_CH7 / EADC2_CH15 / ACMP2_P0 / EBI_nWRL / EMAC0_RMII_TXEN / CAN1_TXD / UART1_TXD / SD1_CMD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / KPI_COL4
144	I/O	PB.6 / EADC0_CH6 / EADC2_CH14 / ACMP2_N / EBI_nWRH / EMAC0_PPS / CAN1_RXD / UART1_RXD / SD1_CLK / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / KPI_COL5

Table 4.1-7 M467JJHAN Multi-function Pin Table

4.1.4.4 M467 Series LQFP176-Pin Multi-function Pin Diagram

Corresponding Part Number: M467HJHAN

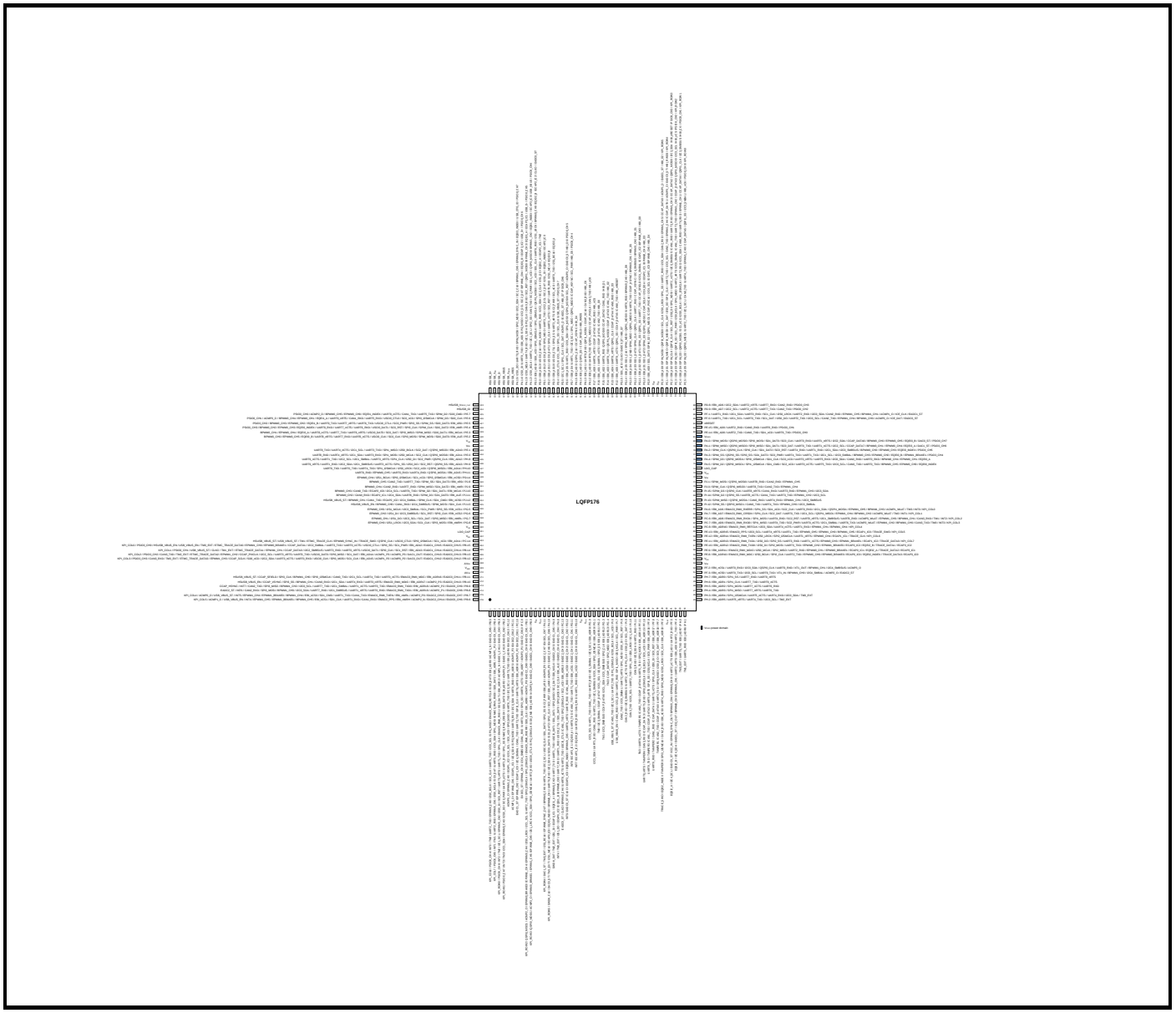


Figure 4.1-16 M467 Series LQFP176-Pin Multi-function Pin Diagram

Pin	Type	M467HJHAN Pin Function
1	I/O	PB.5 / EADC0_CH5 / ACMP1_N / EBI_ADR0 / SD0_DAT3 / EMAC0_RMII_REFCLK / SPI1_MISO / I2C0_SCL / UART5_TXD / SC0_CLK / I2S0_BCLK / EPWM0_CH0 / UART2_TXD / TM0 / INT0 / PSIO0_CH4 / KPI_COL6
2	I/O	PB.4 / EADC0_CH4 / ACMP1_P1 / EBI_ADR1 / SD0_DAT2 / EMAC0_RMII_RXD0 / SPI1_MOSI / I2C0_SDA / UART5_RXD / SC0_DAT / I2S0_MCLK / EPWM0_CH1 / UART2_RXD / TM1 / INT1 / PSIO0_CH5 / KPI_COL7
3	I/O	PB.3 / EADC0_CH3 / EADC1_CH11 / ACMP0_N / EBI_ADR2 / SD0_DAT1 / EMAC0_RMII_RXD1 / SPI1_CLK / UART1_TXD / UART5_nRTS / SC0_RST / I2S0_DI / EPWM0_CH2 / I2C1_SCL / TM2 / INT2 / PSIO0_CH6 / KPI_ROW0

Pin	Type	M467HJHAN Pin Function
4	I/O	PB.2 / EADC0_CH2 / EADC1_CH10 / ACMP0_P1 / EBI_ADR3 / SD0_DAT0 / EMAC0_RMII_CRSDV / SPI1_SS / UART1_RXD / UART5_nCTS / SC0_PWR / I2S0_DO / EPWM0_CH3 / I2C1_SDA / TM3 / INT3 / PSIO0_CH7 / KPI_ROW1
5	I/O	PC.12 / EADC2_CH13 / EBI_ADR4 / UART0_TXD / I2C0_SCL / UART6_TXD / SPI3_MISO / SC0_nCD / I2C4_SCL / ECAP1_IC2 / EPWM1_CH0 / ACMP0_O
6	I/O	PC.11 / EADC2_CH12 / ACMP3_P3 / EBI_ADR5 / UART0_RXD / I2C0_SDA / UART6_RXD / SPI3_MOSI / I2C4_SDA / ECAP1_IC1 / EPWM1_CH1 / ACMP1_O
7	I/O	PC.10 / EADC2_CH11 / ACMP3_P2 / EBI_ADR6 / UART6_nRTS / SPI3_CLK / UART3_TXD / CAN1_TXD / I2C4_SMBAL / ECAP1_IC0 / EPWM1_CH2 / EADC1_ST
8	I/O	PC.9 / EADC2_CH10 / ACMP3_P1 / EBI_ADR7 / UART6_nCTS / SPI3_SS / UART3_RXD / CAN1_RXD / I2C4_SMBSUS / EPWM1_CH3 / EADC1_ST
9	I/O	PB.1 / EADC0_CH1 / EADC1_CH9 / EADC2_CH9 / ACMP3_P0 / EBI_ADR8 / SD0_CLK / EMAC0_RMII_RXERR / SPI1_I2SMCLK / SPI3_I2SMCLK / UART2_TXD / I2C1_SCL / I2S0_LRCK / EPWM0_CH4 / EPWM1_CH4 / EPWM0_BRAKE0 / ACMP2_O / QSPI0_MISO1 / KPI_ROW2
10	I/O	PB.0 / EADC0_CH0 / EADC1_CH8 / EADC2_CH8 / ACMP3_N / EBI_ADR9 / SD0_CMD / SPI2_I2SMCLK / USCI0_CTL0 / UART2_RXD / SPI0_I2SMCLK / I2C1_SDA / I2S1_LRCK / EPWM0_CH5 / EPWM1_CH5 / EPWM0_BRAKE1 / ACMP3_O / QSPI0_MOSI1 / KPI_ROW3
11	P	V_{SS}
12	P	V_{DD}
13	I/O	PA.11 / EADC1_CH7 / EADC2_CH7 / ACMP0_P0 / EBI_nRD / SC2_PWR / SPI2_SS / SD1_DAT3 / USCI0_CLK / I2C2_SCL / UART6_TXD / BPWM0_CH0 / EPWM0_SYNC_OUT / I2S1_BCLK / TM0_EXT / DAC1_ST / KPI_ROW4
14	I/O	PA.10 / EADC1_CH6 / EADC2_CH6 / ACMP1_P0 / EBI_nWR / SC2_RST / SPI2_CLK / SD1_DAT2 / USCI0_DAT0 / I2C2_SDA / UART6_RXD / BPWM0_CH1 / EQEI1_INDEX / ECAP0_IC0 / I2S1_MCLK / TM1_EXT / DAC0_ST / SWDH_CLK / KPI_ROW5
15	I/O	PA.9 / EADC1_CH5 / EADC2_CH5 / EBI_MCLK / SC2_DAT / SPI2_MISO / SD1_DAT1 / USCI0_DAT1 / UART1_TXD / UART7_TXD / BPWM0_CH2 / EQEI1_A / ECAP0_IC1 / I2S1_DI / TM2_EXT / SWDH_DAT
16	I/O	PA.8 / EADC1_CH4 / EADC2_CH4 / EBI_ALE / SC2_CLK / SPI2_MOSI / SD1_DAT0 / USCI0_CTL1 / UART1_RXD / UART7_RXD / BPWM0_CH3 / EQEI1_B / ECAP0_IC2 / I2S1_DO / TM3_EXT / INT4
17	I/O	PC.13 / EADC1_CH3 / EADC2_CH3 / EBI_ADR10 / SC2_nCD / SPI2_I2SMCLK / CAN1_TXD / USCI0_CTL0 / UART2_TXD / UART8_nCTS / BPWM0_CH4 / CLKO / EADC0_ST
18	I/O	PD.12 / EADC1_CH2 / EADC2_CH2 / EBI_nCS0 / CAN1_RXD / UART2_RXD / UART8_nRTS / BPWM0_CH5 / EQEI0_INDEX / ECAP3_IC0 / CLKO / EADC0_ST / INT5
19	I/O	PD.11 / EADC1_CH1 / EADC2_CH1 / EBI_nCS1 / UART1_TXD / CAN0_TXD / UART8_TXD / EQEI0_A / ECAP3_IC1 / INT6
20	I/O	PD.10 / EADC1_CH0 / EADC2_CH0 / EBI_nCS2 / UART1_RXD / CAN0_RXD / UART8_RXD / EQEI0_B / ECAP3_IC2 / INT7
21	P	V_{SS}
22	P	V_{DD}
23	I/O	PG.0 / EBI_ADR8 / I2C0_SCL / I2C1_SMBAL / UART2_RXD / CAN1_TXD / UART1_TXD / I2C3_SCL
24	I/O	PG.1 / EBI_ADR9 / SPI2_I2SMCLK / I2C0_SDA / I2C1_SMBSUS / UART2_TXD / CAN1_RXD / UART1_RXD / I2C3_SDA
25	I/O	PG.2 / EBI_ADR11 / SPI2_SS / I2C0_SMBAL / I2C1_SCL / CCAP_DATA7 / I2C3_SMBAL / TM0
26	I/O	PG.3 / EBI_ADR12 / SPI2_CLK / I2C0_SMBSUS / I2C1_SDA / CCAP_DATA6 / I2C3_SMBSUS / TM1
27	I/O	PG.4 / EBI_ADR13 / SPI2_MISO / CCAP_DATA5 / TM2

Pin	Type	M467HJHAN Pin Function
28	I/O	PI.6 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_TXD / I2C1_SCL / CAN3_TXD / USB_VBUS_ST
29	I/O	PI.7 / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_RXD / I2C1_SDA / CAN3_RXD / USB_VBUS_EN
30	I/O	PI.8 / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nRTS / I2C0_SMBAL / CAN2_TXD
31	I/O	PI.9 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_nCTS / I2C0_SMBSUS / CAN2_RXD
32	I/O	PI.10 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_TXD / I2C0_SCL / CAN3_TXD
33	I/O	PI.11 / UART2_RXD / I2C0_SDA / CAN3_RXD
34	I/O	PF.11 / EBI_ADR14 / SPI2_MOSI / UART5_TXD / CCAP_DATA4 / CAN3_TXD / TAMPER5 / UART9_nCTS / TM3
35	I/O	PF.10 / EBI_ADR15 / SC0_nCD / I2S0_BCLK / SPI0_I2SMCLK / UART5_RXD / CCAP_DATA3 / CAN3_RXD / TAMPER4 / UART9_nRTS
36	I/O	PF.9 / EBI_ADR16 / SC0_PWR / I2S0_MCLK / SPI0_SS / UART5_nRTS / CCAP_DATA2 / CAN1_TXD / TAMPER3 / UART9_TXD
37	I/O	PF.8 / EBI_ADR17 / SC0_RST / I2S0_DI / SPI0_CLK / UART5_nCTS / CCAP_DATA1 / CAN1_RXD / TAMPER2 / UART9_RXD
38	I/O	PF.7 / EBI_ADR18 / SC0_DAT / I2S0_DO / SPI0_MISO / UART4_TXD / CCAP_DATA0 / CAN2_TXD / TAMPER1
39	I/O	PF.6 / EBI_ADR19 / SC0_CLK / I2S0_LRCK / SPI0_MOSI / UART4_RXD / EBI_nCS0 / CAN2_RXD / SPI3_I2SMCLK / TAMPER0 / EQEI2_INDEX / TRACE_SWO
40	P	V_{BAT}
41	I/O	PF.5 / UART2_RXD / EBI_AD1 / UART2_nCTS / EPWM0_CH0 / BPWM0_CH4 / EPWM0_SYNC_OUT / X32_IN / EADC0_ST / I2C4_SCL / EQEI2_A
42	I/O	PF.4 / UART2_TXD / EBI_AD0 / UART2_nRTS / EPWM0_CH1 / BPWM0_CH5 / X32_OUT / EADC1_ST / I2C4_SDA / EQEI2_B
43	I/O	PH.0 / EBI_ADR7 / UART5_TXD / TM0_EXT
44	I/O	PH.1 / EBI_ADR6 / UART5_RXD / TM1_EXT
45	I/O	PH.2 / EBI_ADR5 / UART5_nRTS / UART4_TXD / I2C0_SCL / TM2_EXT
46	I/O	PH.3 / EBI_ADR4 / SPI1_I2SMCLK / UART5_nCTS / UART4_RXD / I2C0_SDA / TM3_EXT
47	I/O	PH.4 / EBI_ADR3 / SPI1_MISO / UART7_nRTS / UART6_TXD
48	I/O	PH.5 / EBI_ADR2 / SPI1_MOSI / UART7_nCTS / UART6_RXD
49	I/O	PH.6 / EBI_ADR1 / SPI1_CLK / UART7_TXD / UART9_nCTS
50	I/O	PH.7 / EBI_ADR0 / SPI1_SS / UART7_RXD / UART9_nRTS
51	I/O	PF.3 / EBI_nCS0 / UART0_TXD / I2C0_SCL / UART9_TXD / XT1_IN / BPWM1_CH0 / I2C4_SMBAL / ACMP2_O / EADC2_ST
52	I/O	PF.2 / EBI_nCS1 / UART0_RXD / I2C0_SDA / QSPI0_CLK / UART9_RXD / XT1_OUT / BPWM1_CH1 / I2C4_SMBSUS / ACMP3_O
53	P	V_{SS}
54	P	V_{DD}
55	I/O	PE.8 / EBI_ADR10 / EMAC0_RMII_MDC / I2S0_BCLK / SPI2_CLK / UART2_TXD / EPWM0_CH0 / EPWM0_BRAKE0 / ECAP0_IC0 / EQEI2_INDEX / TRACE_DATA3 / ECAP3_IC0
56	I/O	PE.9 / EBI_ADR11 / EMAC0_RMII_MDIO / I2S0_MCLK / SPI2_MISO / UART2_RXD / EPWM0_CH1 /

Pin	Type	M467HJHAN Pin Function
		EPWM0_BRAKE1 / ECAP0_IC1 / EQEI2_A / TRACE_DATA2 / ECAP3_IC1
57	I/O	PE.10 / EBI_ADR12 / EMAC0_RMII_TXD0 / I2S0_DI / SPI2_MOSI / UART3_TXD / EPWM0_CH2 / EPWM1_BRAKE0 / ECAP0_IC2 / EQEI2_B / TRACE_DATA1 / ECAP3_IC2
58	I/O	PE.11 / EBI_ADR13 / EMAC0_RMII_TXD1 / I2S0_DO / SPI2_SS / UART3_RXD / UART1_nCTS / EPWM0_CH3 / EPWM1_BRAKE1 / ECAP1_IC2 / TRACE_DATA0 / KPI_COL7
59	I/O	PE.12 / EBI_ADR14 / EMAC0_RMII_TXEN / I2S0_LRCK / SPI2_I2SMCLK / UART1_nRTS / EPWM0_CH4 / ECAP1_IC1 / TRACE_CLK / KPI_COL6
60	I/O	PE.13 / EBI_ADR15 / EMAC0_PPS / I2C0_SCL / UART4_nRTS / UART1_TXD / EPWM0_CH5 / EPWM1_CH0 / BPWM1_CH5 / ECAP1_IC0 / TRACE_SWO / KPI_COL5
61	I/O	PC.8 / EBI_ADR16 / EMAC0_RMII_REFCLK / I2C0_SDA / UART4_nCTS / UART1_RXD / EPWM1_CH1 / BPWM1_CH4 / KPI_COL4
62	I/O	PC.7 / EBI_AD9 / EMAC0_RMII_RXD0 / SPI1_MISO / UART4_TXD / SC2_PWR / UART0_nCTS / I2C1_SMBAL / UART6_TXD / ACMP2_WLAT / EPWM1_CH2 / BPWM1_CH0 / CAN3_TXD / TM0 / INT3 / KPI_COL3
63	I/O	PC.6 / EBI_AD8 / EMAC0_RMII_RXD1 / SPI1_MOSI / UART4_RXD / SC2_RST / UART0_nRTS / I2C1_SMBSUS / UART6_RXD / ACMP3_WLAT / EPWM1_CH3 / BPWM1_CH1 / CAN3_RXD / TM1 / INT2 / KPI_COL2
64	I/O	PA.7 / EBI_AD7 / EMAC0_RMII_CRSDV / SPI1_CLK / SC2_DAT / UART0_TXD / I2C1_SCL / QSPI1_MISO1 / EPWM1_CH4 / BPWM1_CH2 / ACMP0_WLAT / TM2 / INT1 / KPI_COL1
65	I/O	PA.6 / EBI_AD6 / EMAC0_RMII_RXERR / SPI1_SS / SD1_nCD / SC2_CLK / UART0_RXD / I2C1_SDA / QSPI1_MOSI1 / EPWM1_CH5 / BPWM1_CH3 / ACMP1_WLAT / TM3 / INT0 / KPI_COL0
66	I/O	PI.12 / SPIM_SS / QSPI0_MISO1 / CAN0_TXD / UART4_TXD / EPWM1_CH0 / I2C3_SMBAL
67	I/O	PI.13 / SPIM_MISO / QSPI0_MOSI1 / CAN0_RXD / UART4_RXD / EPWM1_CH1 / I2C3_SMBSUS
68	I/O	PI.14 / SPIM_D2 / QSPI0_SS / UART8_nCTS / CAN1_TXD / UART3_TXD / EPWM1_CH2 / I2C3_SCL
69	I/O	PI.15 / SPIM_D3 / QSPI0_CLK / UART8_nRTS / CAN1_RXD / UART3_RXD / EPWM1_CH3 / I2C3_SDA
70	I/O	PJ.0 / SPIM_CLK / QSPI0_MISO0 / UART8_TXD / CAN2_TXD / EPWM1_CH4
71	I/O	PJ.1 / SPIM_MOSI / QSPI0_MOSI0 / UART8_RXD / CAN2_RXD / EPWM1_CH5
72	P	V_{SS}
73	P	V_{DD}
74	A	LDO_CAP
75	I/O	PA.5 / SPIM_D2 / QSPI0_MISO1 / SPI1_I2SMCLK / SD1_CMD / SC2_nCD / UART0_nCTS / UART5_TXD / I2C0_SCL / CAN0_TXD / UART0_TXD / BPWM0_CH5 / EPWM0_CH0 / EQEI0_INDEX
76	I/O	PA.4 / SPIM_D3 / QSPI0_MOSI1 / SPI0_I2SMCLK / SD1_CLK / SC0_nCD / UART0_nRTS / UART5_RXD / I2C0_SDA / CAN0_RXD / UART0_RXD / BPWM0_CH4 / EPWM0_CH1 / EQEI0_A
77	I/O	PA.3 / SPIM_SS / QSPI0_SS / SPI0_SS / SD1_DAT3 / SC0_PWR / UART4_TXD / UART1_TXD / I2C1_SCL / I2C0_SMBAL / BPWM0_CH3 / EPWM0_CH2 / EQEI0_B / EPWM1_BRAKE1 / PSIO0_CH4
78	I/O	PA.2 / SPIM_CLK / QSPI0_CLK / SPI0_CLK / SD1_DAT2 / SC0_RST / UART4_RXD / UART1_RXD / I2C1_SDA / I2C0_SMBSUS / BPWM0_CH2 / EPWM0_CH3 / EQEI3_INDEX / PSIO0_CH5
79	I/O	PA.1 / SPIM_MISO / QSPI0_MISO0 / SPI0_MISO / SD1_DAT1 / SC0_DAT / UART0_TXD / UART1_nCTS / I2C2_SCL / CCAP_DATA7 / BPWM0_CH1 / EPWM0_CH4 / EQEI3_A / DAC1_ST / PSIO0_CH6
80	I/O	PA.0 / SPIM_MOSI / QSPI0_MOSI0 / SPI0_MOSI / SD1_DAT0 / SC0_CLK / UART0_RXD / UART1_nRTS / I2C2_SDA / CCAP_DATA6 / BPWM0_CH0 / EPWM0_CH5 / EQEI3_B / DAC0_ST / PSIO0_CH7

Pin	Type	M467HJHAN Pin Function
81	P	V_{DDIO}
82	I/O	PE.14 / EBI_AD8 / UART2_TXD / CAN0_TXD / SD1_nCD / UART6_TXD / PSIO0_CH0
83	I/O	PE.15 / EBI_AD9 / UART2_RXD / CAN0_RXD / UART6_RXD / PSIO0_CH1
84	I	nRESET
85	I/O	PF.0 / UART1_TXD / I2C1_SCL / UART0_TXD / SC1_DAT / I2S0_DO / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / BPWM1_CH0 / ACMP0_O / ICE_DAT / EADC0_ST
86	I/O	PF.1 / UART1_RXD / I2C1_SDA / UART0_RXD / SC1_CLK / I2S0_LRCK / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / BPWM1_CH1 / ACMP1_O / ICE_CLK / EADC1_ST
87	I/O	PD.9 / EBI_AD7 / I2C2_SCL / UART2_nCTS / UART7_TXD / CAN2_TXD / PSIO0_CH2
88	I/O	PD.8 / EBI_AD6 / I2C2_SDA / UART2_nRTS / UART7_RXD / CAN2_RXD / PSIO0_CH3
89	I/O	PC.5 / EBI_AD5 / SPIM_D2 / QSPI0_MISO1 / UART2_TXD / I2C1_SCL / CAN0_TXD / UART4_TXD / EPWM1_CH0 / CCAP_DATA5 / QSPI1_SS / I2C3_SMBAL / HBI_nCK / PSIO0_CH0 / KPI_ROW0
90	I/O	PC.4 / EBI_AD4 / SPIM_D3 / QSPI0_MOSI1 / SC1_nCD / I2S0_BCLK / SPI1_I2SMCLK / UART2_RXD / I2C1_SDA / CAN0_RXD / UART4_RXD / EPWM1_CH1 / CCAP_DATA4 / QSPI1_CLK / I2C3_SMBSUS / HBI_CK / PSIO0_CH1 / KPI_ROW1
91	I/O	PC.3 / EBI_AD3 / SPIM_SS / QSPI0_SS / SC1_PWR / I2S0_MCLK / SPI1_MISO / UART2_nRTS / I2C0_SMBAL / CAN1_TXD / UART3_TXD / EPWM1_CH2 / CCAP_DATA3 / QSPI1_MISO0 / I2C3_SCL / HBI_nCS / PSIO0_CH2 / KPI_ROW2
92	I/O	PC.2 / EBI_AD2 / SPIM_CLK / QSPI0_CLK / SC1_RST / I2S0_DI / SPI1_MOSI / UART2_nCTS / I2C0_SMBSUS / CAN1_RXD / UART3_RXD / EPWM1_CH3 / CCAP_DATA2 / QSPI1_MOSI0 / I2C3_SDA / HBI_nRESET / PSIO0_CH3 / KPI_ROW3
93	I/O	PC.1 / EBI_AD1 / SPIM_MISO / QSPI0_MISO0 / SC1_DAT / I2S0_DO / SPI1_CLK / UART2_TXD / I2C0_SCL / CAN2_TXD / EPWM1_CH4 / CCAP_DATA1 / ACMP0_O / EADC0_ST / HBI_RWDS / KPI_ROW4
94	I/O	PC.0 / EBI_AD0 / SPIM_MOSI / QSPI0_MOSI0 / SC1_CLK / I2S0_LRCK / SPI1_SS / UART2_RXD / I2C0_SDA / CAN2_RXD / EPWM1_CH5 / CCAP_DATA0 / ACMP1_O / EADC1_ST / HBI_D2 / KPI_ROW5
95	P	V_{SS}
96	P	V_{DD}
97	I/O	PG.9 / EBI_AD0 / SD1_DAT3 / SPIM_D2 / QSPI1_MISO1 / CCAP_PIXCLK / I2C4_SCL / ECAP2_IC0 / BPWM0_CH5 / HBI_D4
98	I/O	PG.10 / EBI_AD1 / SD1_DAT2 / SPIM_D3 / QSPI1_MOSI1 / CCAP_SCLK / I2C4_SDA / ECAP2_IC1 / BPWM0_CH4 / HBI_D3
99	I/O	PG.11 / EBI_AD2 / SD1_DAT1 / SPIM_SS / QSPI1_SS / UART7_TXD / CCAP_SFIELD / I2C4_SMBAL / ECAP2_IC2 / BPWM0_CH3 / HBI_D0
100	I/O	PG.12 / EBI_AD3 / SD1_DAT0 / SPIM_CLK / QSPI1_CLK / UART7_RXD / CCAP_VSYNC / I2C4_SMBSUS / BPWM0_CH2 / HBI_D1
101	I/O	PG.13 / EBI_AD4 / SD1_CMD / SPIM_MISO / QSPI1_MISO0 / UART6_TXD / CCAP_HSYNC / BPWM0_CH1 / HBI_D5
102	I/O	PG.14 / EBI_AD5 / SD1_CLK / SPIM_MOSI / QSPI1_MOSI0 / UART6_RXD / BPWM0_CH0 / HBI_D6
103	I/O	PG.15 / SD1_nCD / CLKO / EADC0_ST / HBI_D7
104	I/O	PJ.2 / EBI_AD5 / UART8_nCTS / QSPI1_SS / CCAP_DATA5 / CAN0_TXD / HBI_nRESET
105	I/O	PJ.3 / EBI_AD4 / UART8_nRTS / QSPI1_CLK / CCAP_DATA4 / CAN0_RXD / HBI_D3
106	I/O	PJ.4 / EBI_AD3 / UART8_TXD / QSPI1_MISO0 / CCAP_DATA3 / CAN1_TXD / HBI_D2

Pin	Type	M467HJHAN Pin Function
107	I/O	PJ.5 / EBI_AD2 / UART8_RXD / QSPI1_MOSI0 / CCAP_DATA2 / CAN1_RXD / HBI_D1
108	I/O	PJ.6 / EBI_AD1 / UART9_nCTS / CCAP_DATA1 / CAN2_TXD / HBI_D0
109	I/O	PJ.7 / EBI_AD0 / UART9_nRTS / CCAP_DATA0 / CAN2_RXD / HBI_nCS
110	I/O	PH.12 / EBI_AD0 / UART9_TXD / QSPI1_MISO1 / CCAP_PIXCLK / CAN3_TXD / HBI_nCK
111	I/O	PH.13 / EBI_AD1 / UART9_RXD / QSPI1_MOSI1 / CCAP_SCLK / CAN3_RXD / HBI_CK
112	I/O	PH.14 / EBI_AD2 / QSPI1_SS / CCAP_SFIELD / HBI_RWDS
113	I/O	PH.15 / EBI_AD3 / QSPI1_CLK / CCAP_VSYNC / HBI_D4
114	I/O	PD.7 / EBI_AD4 / UART1_TXD / I2C0_SCL / SPI1_MISO / QSPI1_MISO0 / CCAP_HSYNC / SC1_PWR / HBI_D5 / PSIO0_CH4
115	I/O	PD.6 / EBI_AD5 / UART1_RXD / I2C0_SDA / SPI1_MOSI / QSPI1_MOSI0 / SC1_RST / ACMP0_O / EADC0_ST / HBI_D6 / PSIO0_CH5
116	I/O	PD.5 / I2C1_SCL / SPI1_CLK / SC1_DAT / ACMP1_O / EADC1_ST / HBI_D7 / PSIO0_CH6
117	I/O	PD.4 / USCI0_CTL0 / I2C1_SDA / SPI1_SS / SC1_CLK / USB_VBUS_ST / PSIO0_CH7
118	I/O	PD.3 / EBI_AD10 / USCI0_CTL1 / SPI0_SS / UART3_nRTS / SC2_PWR / SC1_nCD / UART0_TXD / I2S1_BCLK / EQEI3_A
119	I/O	PD.2 / EBI_AD11 / USCI0_DAT1 / SPI0_CLK / UART3_nCTS / SC2_RST / UART0_RXD / I2S1_MCLK / EQEI3_B
120	I/O	PD.1 / EBI_AD12 / USCI0_DAT0 / SPI0_MISO / UART3_TXD / I2C2_SCL / SC2_DAT / I2S1_DI / EQEI2_INDEX / ECAP2_IC0
121	I/O	PD.0 / EBI_AD13 / USCI0_CLK / SPI0_MOSI / UART3_RXD / I2C2_SDA / SC2_CLK / I2S1_DO / EQEI2_A / ECAP2_IC1 / TM2
122	I/O	PD.13 / EBI_AD10 / SD0_nCD / SPI0_I2SMCLK / SPI1_I2SMCLK / QSPI1_MOSI0 / SC2_nCD / SD1_CLK / UART6_RXD / I2S1_LRCK / BPWM0_CH0 / EQEI2_B / ECAP2_IC2 / CLKO / EADC0_ST
123	I/O	PA.12 / I2S0_BCLK / UART4_TXD / I2C1_SCL / SPI2_SS / CAN0_TXD / SC2_PWR / SD1_nCD / QSPI1_MISO0 / BPWM1_CH2 / EQEI1_INDEX / ECAP3_IC0 / USB_VBUS / PSIO0_CH4
124	I/O	PA.13 / I2S0_MCLK / UART4_RXD / I2C1_SDA / SPI2_CLK / CAN0_RXD / SC2_RST / QSPI1_MOSI0 / BPWM1_CH3 / EQEI1_A / ECAP3_IC1 / USB_D- / PSIO0_CH5
125	I/O	PA.14 / I2S0_DI / UART0_TXD / EBI_AD5 / SPI2_MISO / I2C2_SCL / SC2_DAT / BPWM1_CH4 / EQEI1_B / ECAP3_IC2 / USB_D+ / PSIO0_CH6
126	I/O	PA.15 / I2S0_DO / UART0_RXD / SPIM_MOSI / SPI2_MOSI / I2C2_SDA / SC2_CLK / BPWM1_CH5 / EPWM0_SYNC_IN / EQEI3_INDEX / USB_OTG_ID / PSIO0_CH7
127	A	HSUSB_VRES
128	P	HSUSB_VDD33
129	I/O	HSUSB_VBUS
130	A	HSUSB_D-
131	P	HSUSB_VSS
132	A	HSUSB_D+
133	A	HSUSB_VDD12_CAP
134	I	HSUSB_ID
135	I/O	PE.7 / SD0_CMD / SPIM_D2 / UART5_TXD / CAN1_TXD / UART9_nCTS / EQEI1_INDEX / EPWM0_CH0 / BPWM0_CH5 / ACMP2_O / PSIO0_CH0

Pin	Type	M467HJHAN Pin Function
136	I/O	PE.6 / SD0_CLK / SPIM_D3 / SPI3_I2SMCLK / SC0_nCD / USCI0_CTL0 / UART5_RXD / CAN1_RXD / UART9_nRTS / EQEI1_A / EPWM0_CH1 / BPWM0_CH4 / ACMP3_O / PSIO0_CH1
137	I/O	PE.5 / EBI_nRD / SD0_DAT3 / SPIM_SS / SPI3_SS / SC0_PWR / USCI0_CTL1 / UART6_TXD / UART7_nRTS / UART9_TXD / EQEI1_B / EPWM0_CH2 / BPWM0_CH3 / PSIO0_CH2
138	I/O	PE.4 / EBI_nWR / SD0_DAT2 / SPIM_CLK / SPI3_CLK / SC0_RST / USCI0_DAT1 / UART6_RXD / UART7_nCTS / UART9_RXD / EQEI0_INDEX / EPWM0_CH3 / BPWM0_CH2 / PSIO0_CH3
139	I/O	PE.3 / EBI_MCLK / SD0_DAT1 / SPIM_MISO / SPI3_MISO / SC0_DAT / USCI0_DAT0 / UART6_nRTS / UART7_TXD / UART8_nCTS / EQEI0_A / EPWM0_CH4 / BPWM0_CH1
140	I/O	PE.2 / EBI_ALE / SD0_DAT0 / SPIM_MOSI / SPI3_MOSI / SC0_CLK / USCI0_CLK / UART6_nCTS / UART7_RXD / UART8_nRTS / EQEI0_B / EPWM0_CH5 / BPWM0_CH0
141	P	V_{SS}
142	P	V_{DD}
143	I/O	PE.1 / EBI_AD10 / QSPI0_MISO0 / SC2_DAT / I2S0_BCLK / SPI1_MISO / UART3_TXD / I2C1_SCL / UART4_nCTS / UART8_TXD
144	I/O	PE.0 / EBI_AD11 / QSPI0_MOSI0 / SC2_CLK / I2S0_MCLK / SPI1_MOSI / UART3_RXD / I2C1_SDA / UART4_nRTS / UART8_RXD
145	I/O	PH.8 / EBI_AD12 / QSPI0_CLK / SC2_PWR / I2S0_DI / SPI1_CLK / UART3_nRTS / I2C1_SMBAL / I2C2_SCL / UART1_TXD / UART9_nCTS
146	I/O	PH.9 / EBI_AD13 / QSPI0_SS / SC2_RST / I2S0_DO / SPI1_SS / UART3_nCTS / I2C1_SMBSUS / I2C2_SDA / UART1_RXD / UART9_nRTS
147	I/O	PH.10 / EBI_AD14 / QSPI0_MISO1 / SC2_nCD / I2S0_LRCK / SPI1_I2SMCLK / UART4_TXD / UART0_TXD / UART9_TXD
148	I/O	PH.11 / EBI_AD15 / QSPI0_MOSI1 / UART4_RXD / UART0_RXD / EPWM0_CH5 / UART9_RXD
149	I/O	PD.14 / EBI_nCS0 / SPI3_I2SMCLK / SC1_nCD / SPI0_I2SMCLK / I2S1_BCLK / EPWM0_CH4
150	I/O	PJ.8 / EBI_nRD / SD1_DAT3 / SPIM_SS / UART7_TXD / CAN2_TXD / BPWM0_CH5
151	I/O	PJ.9 / EBI_nWR / SD1_DAT2 / SPIM_MISO / UART7_RXD / CAN2_RXD / BPWM0_CH4
152	I/O	PJ.10 / EBI_MCLK / SD1_DAT1 / SPIM_D2 / UART6_TXD / I2C4_SCL / ECAP2_IC0 / CAN0_TXD / BPWM0_CH3
153	I/O	PJ.11 / EBI_ALE / SD1_DAT0 / SPIM_D3 / UART6_RXD / I2C4_SDA / ECAP2_IC1 / CAN0_RXD / BPWM0_CH2
154	I/O	PJ.12 / EBI_nCS0 / SD1_CMD / SPIM_CLK / I2C4_SMBAL / ECAP2_IC2 / CAN1_TXD / BPWM0_CH1 / HSUSB_VBUS_ST
155	I/O	PJ.13 / SD1_CLK / SPIM_MOSI / I2C4_SMBSUS / CAN1_RXD / BPWM0_CH0 / HSUSB_VBUS_EN
156	I/O	PG.5 / EBI_nCS1 / SPI3_SS / SC1_PWR / I2C3_SMBAL / I2S1_MCLK / EPWM0_CH3
157	I/O	PG.6 / EBI_nCS2 / SPI3_CLK / SC1_RST / I2C3_SMBSUS / I2S1_DI / EPWM0_CH2
158	I/O	PG.7 / EBI_nWRL / SPI3_MISO / SC1_DAT / I2C3_SCL / I2S1_DO / EPWM0_CH1
159	I/O	PG.8 / EBI_nWRH / SPI3_MOSI / SC1_CLK / I2C3_SDA / I2S1_LRCK / EPWM0_CH0
160	P	V_{SS}
161	A	LDO_CAP
162	P	V_{DD}
163	I/O	PC.14 / EBI_AD11 / SC1_nCD / SPI0_I2SMCLK / USCI0_CTL0 / QSPI0_CLK / TRACE_SWO / EPWM0_SYNC_IN / ETMC_TRACE_CLK / TM1 / USB_VBUS_ST / HSUSB_VBUS_ST

Pin	Type	M467HJHAN Pin Function
164	I/O	PB.15 / EADC0_CH15 / EADC1_CH15 / EBI_AD12 / SC1_PWR / SPI0_SS / USCI0_CTL1 / UART0_nCTS / UART3_TXD / I2C2_SMBAL / CCAP_DATA1 / EPWM0_BRAKE1 / EPWM1_CH0 / ETMC_TRACE_DATA0 / TM0_EXT / USB_VBUS_EN / HSUSB_VBUS_EN / PSIO0_CH0 / KPI_COL0
165	I/O	PB.14 / EADC0_CH14 / EADC1_CH14 / EBI_AD13 / SC1_RST / SPI0_CLK / USCI0_DAT1 / UART0_nRTS / UART3_RXD / I2C2_SMBSUS / CCAP_DATA0 / EPWM1_CH1 / ETMC_TRACE_DATA1 / TM1_EXT / CLKO / USB_VBUS_ST / PSIO0_CH1 / KPI_COL1
166	I/O	PB.13 / EADC0_CH13 / EADC1_CH13 / DAC1_OUT / ACMP0_P3 / ACMP1_P3 / EBI_AD14 / SC1_DAT / SPI0_MISO / USCI0_DAT0 / UART0_TXD / UART3_nRTS / I2C2_SCL / CCAP_PIXCLK / EPWM1_CH2 / ETMC_TRACE_DATA2 / TM2_EXT / CAN3_TXD / PSIO0_CH2 / KPI_COL2
167	I/O	PB.12 / EADC0_CH12 / EADC1_CH12 / DAC0_OUT / ACMP0_P2 / ACMP1_P2 / EBI_AD15 / SC1_CLK / SPI0_MOSI / USCI0_CLK / UART0_RXD / UART3_nCTS / I2C2_SDA / SD0_nCD / CCAP_SCLK / EPWM1_CH3 / ETMC_TRACE_DATA3 / TM3_EXT / CAN3_RXD / PSIO0_CH3 / KPI_COL3
168	P	AV_{DD}
169	A	V_{REF}
170	P	AV_{SS}
171	I/O	PB.11 / EADC0_CH11 / EBI_ADR16 / EMAC0_RMII_MDC / UART0_nCTS / UART4_TXD / I2C1_SCL / CAN0_TXD / SPI0_I2SMCLK / BPWM1_CH0 / SPI3_CLK / CCAP_SFIELD / HSUSB_VBUS_ST
172	I/O	PB.10 / EADC0_CH10 / ACMP2_P3 / EBI_ADR17 / EMAC0_RMII_MDIO / UART0_nRTS / UART4_RXD / I2C1_SDA / CAN0_RXD / BPWM1_CH1 / SPI3_SS / CCAP_VSYNC / HSUSB_VBUS_EN
173	I/O	PB.9 / EADC0_CH9 / ACMP2_P2 / EBI_ADR18 / EMAC0_RMII_TXD0 / UART0_TXD / UART1_nCTS / I2C1_SMBAL / UART7_TXD / I2C0_SCL / BPWM1_CH2 / SPI3_MISO / CAN2_TXD / INT7 / CCAP_HSYNC
174	I/O	PB.8 / EADC0_CH8 / ACMP2_P1 / EBI_ADR19 / EMAC0_RMII_TXD1 / UART0_RXD / UART1_nRTS / I2C1_SMBSUS / UART7_RXD / I2C0_SDA / BPWM1_CH3 / SPI3_MOSI / CAN2_RXD / INT6 / EADC2_ST
175	I/O	PB.7 / EADC0_CH7 / EADC2_CH15 / ACMP2_P0 / EBI_nWRL / EMAC0_RMII_TXEN / CAN1_TXD / UART1_TXD / SD1_CMD / EBI_nCS0 / BPWM1_CH4 / EPWM1_BRAKE0 / EPWM1_CH4 / INT5 / USB_VBUS_ST / ACMP0_O / KPI_COL4
176	I/O	PB.6 / EADC0_CH6 / EADC2_CH14 / ACMP2_N / EBI_nWRH / EMAC0_PPS / CAN1_RXD / UART1_RXD / SD1_CLK / EBI_nCS1 / BPWM1_CH5 / EPWM1_BRAKE1 / EPWM1_CH5 / INT4 / USB_VBUS_EN / ACMP1_O / KPI_COL5

Table 4.1-8 M467HJHAN Multi-function Pin Table

4.2 Pin Mapping Table

4.2.1 M463 Series Mapping Table

The following is the pin mapping table of M463 series

	M463 Series			
Pin Name	M463YG	M463LG	M463SG	M463KG
PB.5	1	1	2	1
PB.4	2	2	3	2
PB.3	3	3	4	3
PB.2	4	4	5	4
PC.12				5
PC.11				6
PC.10				7
PC.9				8
PB.1	5	5	6	9
PB.0	6	6	7	10
V_{SS}				11
V_{DD}				12
PA.11	7	7	8	13
PA.10	8	8	9	14
PA.9	9	9	10	15
PA.8	10	10	11	16
PC.13				17
PD.12				18
PD.11				19
PD.10				20
V_{SS}				
V_{DD}				
PG.2				21
PG.3				22
PG.4				23
PF.11				24
PF.10				25
PF.9				26
PF.8				27

PF.7				28
PF.6			12	29
V_{BAT}			13	30
PF.5	11	11	14	31
PF.4	12	12	15	32
PH.4				33
PH.5				34
PH.6				35
PH.7				36
PF.3	13	13	16	37
PF.2	14	14	17	38
V_{SS}				39
V_{DD}				40
PE.8				41
PE.9				42
PE.10				43
PE.11				44
PE.12				45
PE.13				46
PC.8				47
PC.7			18	48
PC.6			19	49
PA.7	15	15	20	50
PA.6	16	16	21	51
V_{SS}			22	52
V_{DD}			23	53
LDO_CAP			24	54
PA.5	17	17	25	55
PA.4	18	18	26	56
PA.3	19	19	27	57
PA.2	20	20	28	58
PA.1	21	21	29	59
PA.0	22	22	30	60
V_{DDIO}	23	23	31	61
PE.14				62

PE.15				63
nRESET	24	24	32	64
PF.0	25	25	33	65
PF.1	26	26	34	66
PD.9				67
PD.8				68
PC.5			35	69
PC.4			36	70
PC.3				71
PC.2				72
PC.1	27	27		73
PC.0	28	28		74
V_{SS}				75
V_{DD}				76
PG.9				77
PG.10				78
PG.11				79
PG.12				80
PG.13				81
PG.14				82
PG.15				83
PD.13				84
PA.12			37	85
PA.13			38	86
PA.14			39	87
PA.15			40	88
HSUSB_V_{RES}	29	29	41	89
HSUSB_VDD_{33}	30	30	42	90
HSUSB_VBUS	31	31	43	91
HSUSB_D-	32	32	44	92
HSUSB_VSS	33	33	45	93
HSUSB_D+	34	34	46	94
HSUSB_VDD_{12}_CAP	35	35	47	95
HSUSB_ID	36	36	48	96

PE.7				97
PE.6				98
PE.5				99
PE.4				100
PE.3				101
PE.2				102
V_{SS}	37	37	49	103
V_{DD}				104
PE.1				105
PE.0				106
PH.8				107
PH.9				108
PH.10				109
PH.11				110
PD.14				111
V_{SS}				112
LDO_CAP	38	38	50	113
V_{DD}	39	39	51	114
PC.14	40	40	52	115
PB.15	41	41	53	116
PB.14	42	42	54	117
PB.13	43	43	55	118
PB.12	44	44	56	119
AV_{DD}	45	45	57	120
V_{REF}			58	121
AV_{SS}	46	46	59	122
PB.11			60	123
PB.10			61	124
PB.9			62	125
PB.8			63	126
PB.7	47	47	64	127
PB.6	48	48	1	128
V_{SS}	49			

4.2.2 M467 Series Mapping Table

The following is the pin mapping table of M467 series.

	M467 Series			
Pin Name	M467SJ	M467KJ	M467JJ	M467HJ
PB.5	2	1	1	1
PB.4	3	2	2	2
PB.3	4	3	3	3
PB.2	5	4	4	4
PC.12		5	5	5
PC.11		6	6	6
PC.10		7	7	7
PC.9		8	8	8
PB.1	6	9	9	9
PB.0	7	10	10	10
V_{SS}		11	11	11
V_{DD}		12	12	12
PA.11	8	13	13	13
PA.10	9	14	14	14
PA.9	10	15	15	15
PA.8	11	16	16	16
PC.13		17	17	17
PD.12		18	18	18
PD.11		19	19	19
PD.10		20	20	20
V_{SS}			21	21
V_{DD}			22	22
PG.0			23	23
PG.1			24	24
PG.2		21	25	25
PG.3		22	26	26
PG.4		23	27	27
PI.6				28
PI.7				29
PI.8				30
PI.9				31

PI.10				32
PI.11				33
PF.11		24	28	34
PF.10		25	29	35
PF.9		26	30	36
PF.8		27	31	37
PF.7		28	32	38
PF.6	12	29	33	39
V_{BAT}	13	30	34	40
PF.5	14	31	35	41
PF.4	15	32	36	42
PH.0			37	43
PH.1			38	44
PH.2			39	45
PH.3			40	46
PH.4		33	41	47
PH.5		34	42	48
PH.6		35	43	49
PH.7		36	44	50
PF.3	16	37	45	51
PF.2	17	38	46	52
V_{SS}		39	47	53
V_{DD}		40	48	54
PE.8		41	49	55
PE.9		42	50	56
PE.10		43	51	57
PE.11		44	52	58
PE.12		45	53	59
PE.13		46	54	60
PC.8		47	55	61
PC.7	18	48	56	62
PC.6	19	49	57	63
PA.7	20	50	58	64
PA.6	21	51	59	65
PI.12				66

PI.13				67
PI.14				68
PI.15				69
PJ.0				70
PJ.1				71
V_{SS}	22	52	60	72
V_{DD}	23	53	61	73
LDO_CAP	24	54	62	74
PA.5	25	55	63	75
PA.4	26	56	64	76
PA.3	27	57	65	77
PA.2	28	58	66	78
PA.1	29	59	67	79
PA.0	30	60	68	80
V_{DDIO}	31	61	69	81
PE.14		62	70	82
PE.15		63	71	83
nRESET	32	64	72	84
PF.0	33	65	73	85
PF.1	34	66	74	86
PD.9		67	75	87
PD.8		68	76	88
PC.5	35	69	77	89
PC.4	36	70	78	90
PC.3		71	79	91
PC.2		72	80	92
PC.1		73	81	93
PC.0		74	82	94
V_{SS}		75	83	95
V_{DD}		76	84	96
PG.9		77	85	97
PG.10		78	86	98
PG.11		79	87	99
PG.12		80	88	100
PG.13		81	89	101

PG.14		82	90	102
PG.15		83	91	103
HBI_PWR				
PJ.2				104
PJ.3				105
PJ.4				106
PJ.5				107
PJ.6				108
PJ.7				109
PH.12				110
PH.13				111
PH.14				112
PH.15				113
PD.7				114
PD.6				115
PD.5				116
HBI_PWR				
PD.4				117
PD.3			92	118
PD.2			93	119
PD.1			94	120
PD.0			95	121
PD.13		84	96	122
PA.12	37	85	97	123
PA.13	38	86	98	124
PA.14	39	87	99	125
PA.15	40	88	100	126
HSUSB_V_{RES}	41	89	101	127
HSUSB_VDD_{33}	42	90	102	128
HSUSB_VBUS	43	91	103	129
HSUSB_D-	44	92	104	130
HSUSB_VSS	45	93	105	131
HSUSB_D+	46	94	106	132
HSUSB_VDD_{12_CAP}	47	95	107	133
HSUSB_ID	48	96	108	134

PE.7		97	109	135
PE.6		98	110	136
PE.5		99	111	137
PE.4		100	112	138
PE.3		101	113	139
PE.2		102	114	140
V_{SS}	49	103	115	141
V_{DD}		104	116	142
PE.1		105	117	143
PE.0		106	118	144
PH.8		107	119	145
PH.9		108	120	146
PH.10		109	121	147
PH.11		110	122	148
PD.14		111	123	149
PJ.8				150
PJ.9				151
PJ.10				152
PJ.11				153
PJ.12				154
PJ.13				155
PG.5			124	156
PG.6			125	157
PG.7			126	158
PG.8			127	159
V_{SS}		112	128	160
LDO_CAP	50	113	129	161
V_{DD}	51	114	130	162
PC.14	52	115	131	163
PB.15	53	116	132	164
PB.14	54	117	133	165
PB.13	55	118	134	166
PB.12	56	119	135	167
AV_{DD}	57	120	136	168
V_{REF}	58	121	137	169

AV_{SS}	59	122	138	170
PB.11	60	123	139	171
PB.10	61	124	140	172
PB.9	62	125	141	173
PB.8	63	126	142	174
PB.7	64	127	143	175
PB.6	1	128	144	176

4.3 Pin Functional Description

4.3.1 M463/M467 Series Summary Function Pin Description

Group	Pin Name	Type	Description
ACMP0	ACMP0_N	A	Analog comparator 0 negative input pin.
	ACMP0_O	O	Analog comparator 0 output pin.
	ACMP0_P0	A	Analog comparator 0 positive input 0 pin.
	ACMP0_P1	A	Analog comparator 0 positive input 1 pin.
	ACMP0_P2	A	Analog comparator 0 positive input 2 pin.
	ACMP0_P3	A	Analog comparator 0 positive input 3 pin.
	ACMP0_WLAT	I	Analog comparator 0 window latch input pin
ACMP1	ACMP1_N	A	Analog comparator 1 negative input pin.
	ACMP1_O	O	Analog comparator 1 output pin.
	ACMP1_P0	A	Analog comparator 1 positive input 0 pin.
	ACMP1_P1	A	Analog comparator 1 positive input 1 pin.
	ACMP1_P2	A	Analog comparator 1 positive input 2 pin.
	ACMP1_P3	A	Analog comparator 1 positive input 3 pin.
	ACMP1_WLAT	I	Analog comparator 1 window latch input pin
ACMP2	ACMP2_N	A	Analog comparator 2 negative input pin.
	ACMP2_O	O	Analog comparator 2 output pin.
	ACMP2_P0	A	Analog comparator 2 positive input 0 pin.
	ACMP2_P1	A	Analog comparator 2 positive input 1 pin.
	ACMP2_P2	A	Analog comparator 2 positive input 2 pin.
	ACMP2_P3	A	Analog comparator 2 positive input 3 pin.
	ACMP2_WLAT	I	Analog comparator 2 window latch input pin
ACMP3	ACMP3_N	A	Analog comparator 3 negative input pin.
	ACMP3_O	O	Analog comparator 3 output pin.
	ACMP3_P0	A	Analog comparator 3 positive input 0 pin.
	ACMP3_P1	A	Analog comparator 3 positive input 1 pin.
	ACMP3_P2	A	Analog comparator 3 positive input 2 pin.
	ACMP3_P3	A	Analog comparator 3 positive input 3 pin.
	ACMP3_WLAT	I	Analog comparator 3 window latch input pin
BPWM0	BPWM0_CH0	I/O	BPWM0 channel 0 output/capture input.
	BPWM0_CH1	I/O	BPWM0 channel 1 output/capture input.
	BPWM0_CH2	I/O	BPWM0 channel 2 output/capture input.
	BPWM0_CH3	I/O	BPWM0 channel 3 output/capture input.

Group	Pin Name	Type	Description
	BPWM0_CH4	I/O	BPWM0 channel 4 output/capture input.
	BPWM0_CH5	I/O	BPWM0 channel 5 output/capture input.
BPWM1	BPWM1_CH0	I/O	BPWM1 channel 0 output/capture input.
	BPWM1_CH1	I/O	BPWM1 channel 1 output/capture input.
	BPWM1_CH2	I/O	BPWM1 channel 2 output/capture input.
	BPWM1_CH3	I/O	BPWM1 channel 3 output/capture input.
	BPWM1_CH4	I/O	BPWM1 channel 4 output/capture input.
	BPWM1_CH5	I/O	BPWM1 channel 5 output/capture input.
CAN0	CAN0_RXD	I	CAN0 bus receiver input.
	CAN0_TXD	O	CAN0 bus transmitter output.
CAN1	CAN1_RXD	I	CAN1 bus receiver input.
	CAN1_TXD	O	CAN1 bus transmitter output.
CAN2	CAN2_RXD	I	CAN2 bus receiver input.
	CAN2_TXD	O	CAN2 bus transmitter output.
CAN3	CAN3_RXD	I	CAN3 bus receiver input.
	CAN3_TXD	O	CAN3 bus transmitter output.
CCAP	CCAP_DATA0	I	Camera capture data input bus bit 0.
	CCAP_DATA1	I	Camera capture data input bus bit 1.
	CCAP_DATA2	I	Camera capture data input bus bit 2.
	CCAP_DATA3	I	Camera capture data input bus bit 3.
	CCAP_DATA4	I	Camera capture data input bus bit 4.
	CCAP_DATA5	I	Camera capture data input bus bit 5.
	CCAP_DATA6	I	Camera capture data input bus bit 6.
	CCAP_DATA7	I	Camera capture data input bus bit 7.
	CCAP_HSYNC	I	Camera capture interface hsync input pin.
	CCAP_PIXCLK	I	Camera capture interface pix clock input pin.
	CCAP_SCLK	O	Camera capture interface sensor clock pin.
	CCAP_SFIELD	I	Camera capture interface SFIELD input pin.
	CCAP_VSYNC	I	Camera capture interface vsync input pin.
CLKO	CLKO	O	Clock Out
DAC0	DAC0_OUT	A	DAC0 channel analog output.
	DAC0_ST	I	DAC0 external trigger input.
DAC1	DAC1_OUT	A	DAC1 channel analog output.
	DAC1_ST	I	DAC1 external trigger input.

Group	Pin Name	Type	Description
EADC0	EADC0_CH0	A	EADC0 channel 0 analog input.
	EADC0_CH1	A	EADC0 channel 1 analog input.
	EADC0_CH2	A	EADC0 channel 2 analog input.
	EADC0_CH3	A	EADC0 channel 3 analog input.
	EADC0_CH4	A	EADC0 channel 4 analog input.
	EADC0_CH5	A	EADC0 channel 5 analog input.
	EADC0_CH6	A	EADC0 channel 6 analog input.
	EADC0_CH7	A	EADC0 channel 7 analog input.
	EADC0_CH8	A	EADC0 channel 8 analog input.
	EADC0_CH9	A	EADC0 channel 9 analog input.
	EADC0_CH10	A	EADC0 channel 10 analog input.
	EADC0_CH11	A	EADC0 channel 11 analog input.
	EADC0_CH12	A	EADC0 channel 12 analog input.
	EADC0_CH13	A	EADC0 channel 13 analog input.
	EADC0_CH14	A	EADC0 channel 14 analog input.
	EADC0_CH15	A	EADC0 channel 15 analog input.
	EADC0_ST	I	EADC0 external trigger input.
EADC1	EADC1_CH0	A	EADC1 channel 0 analog input.
	EADC1_CH1	A	EADC1 channel 1 analog input.
	EADC1_CH2	A	EADC1 channel 2 analog input.
	EADC1_CH3	A	EADC1 channel 3 analog input.
	EADC1_CH4	A	EADC1 channel 4 analog input.
	EADC1_CH5	A	EADC1 channel 5 analog input.
	EADC1_CH6	A	EADC1 channel 6 analog input.
	EADC1_CH7	A	EADC1 channel 7 analog input.
	EADC1_CH8	A	EADC1 channel 8 analog input.
	EADC1_CH9	A	EADC1 channel 9 analog input.
	EADC1_CH10	A	EADC1 channel 10 analog input.
	EADC1_CH11	A	EADC1 channel 11 analog input.
	EADC1_CH12	A	EADC1 channel 12 analog input.
	EADC1_CH13	A	EADC1 channel 13 analog input.
	EADC1_CH14	A	EADC1 channel 14 analog input.
	EADC1_CH15	A	EADC1 channel 15 analog input.
	EADC1_ST	I	EADC1 external trigger input.

Group	Pin Name	Type	Description
EADC2	EADC2_CH0	A	EADC2 channel 0 analog input.
	EADC2_CH1	A	EADC2 channel 1 analog input.
	EADC2_CH2	A	EADC2 channel 2 analog input.
	EADC2_CH3	A	EADC2 channel 3 analog input.
	EADC2_CH4	A	EADC2 channel 4 analog input.
	EADC2_CH5	A	EADC2 channel 5 analog input.
	EADC2_CH6	A	EADC2 channel 6 analog input.
	EADC2_CH7	A	EADC2 channel 7 analog input.
	EADC2_CH8	A	EADC2 channel 8 analog input.
	EADC2_CH9	A	EADC2 channel 9 analog input.
	EADC2_CH10	A	EADC2 channel 10 analog input.
	EADC2_CH11	A	EADC2 channel 11 analog input.
	EADC2_CH12	A	EADC2 channel 12 analog input.
	EADC2_CH13	A	EADC2 channel 13 analog input.
	EADC2_CH14	A	EADC2 channel 14 analog input.
	EADC2_CH15	A	EADC2 channel 15 analog input.
	EADC2_ST	I	EADC2 external trigger input.
EBI	EBI_AD0	I/O	EBI address/data bus bit 0.
	EBI_AD1	I/O	EBI address/data bus bit 1.
	EBI_AD2	I/O	EBI address/data bus bit 2.
	EBI_AD3	I/O	EBI address/data bus bit 3.
	EBI_AD4	I/O	EBI address/data bus bit 4.
	EBI_AD5	I/O	EBI address/data bus bit 5.
	EBI_AD6	I/O	EBI address/data bus bit 6.
	EBI_AD7	I/O	EBI address/data bus bit 7.
	EBI_AD8	I/O	EBI address/data bus bit 8.
	EBI_AD9	I/O	EBI address/data bus bit 9.
	EBI_AD10	I/O	EBI address/data bus bit 10.
	EBI_AD11	I/O	EBI address/data bus bit 11.
	EBI_AD12	I/O	EBI address/data bus bit 12.
	EBI_AD13	I/O	EBI address/data bus bit 13.
	EBI_AD14	I/O	EBI address/data bus bit 14.
	EBI_AD15	I/O	EBI address/data bus bit 15.
	EBI_ADR0	O	EBI address bus bit 0.

Group	Pin Name	Type	Description
	EBI_ADR1	O	EBI address bus bit 1.
	EBI_ADR2	O	EBI address bus bit 2.
	EBI_ADR3	O	EBI address bus bit 3.
	EBI_ADR4	O	EBI address bus bit 4.
	EBI_ADR5	O	EBI address bus bit 5.
	EBI_ADR6	O	EBI address bus bit 6.
	EBI_ADR7	O	EBI address bus bit 7.
	EBI_ADR8	O	EBI address bus bit 8.
	EBI_ADR9	O	EBI address bus bit 9.
	EBI_ADR10	O	EBI address bus bit 10.
	EBI_ADR11	O	EBI address bus bit 11.
	EBI_ADR12	O	EBI address bus bit 12.
	EBI_ADR13	O	EBI address bus bit 13.
	EBI_ADR14	O	EBI address bus bit 14.
	EBI_ADR15	O	EBI address bus bit 15.
	EBI_ADR16	O	EBI address bus bit 16.
	EBI_ADR17	O	EBI address bus bit 17.
	EBI_ADR18	O	EBI address bus bit 18.
	EBI_ADR19	O	EBI address bus bit 19.
	EBI_ALE	O	EBI address latch enable output pin.
	EBI_MCLK	O	EBI external clock output pin.
	EBI_nCS0	O	EBI chip select 0 output pin.
	EBI_nCS1	O	EBI chip select 1 output pin.
	EBI_nCS2	O	EBI chip select 2 output pin.
	EBI_nRD	O	EBI read enable output pin.
	EBI_nWR	O	EBI write enable output pin.
	EBI_nWRH	O	EBI high byte write enable output pin
	EBI_nWRL	O	EBI low byte write enable output pin.
ECAP0	ECAP0_IC0	I	Enhanced capture unit 0 input 0 pin.
	ECAP0_IC1	I	Enhanced capture unit 0 input 1 pin.
	ECAP0_IC2	I	Enhanced capture unit 0 input 2 pin.
ECAP1	ECAP1_IC0	I	Enhanced capture unit 1 input 0 pin.
	ECAP1_IC1	I	Enhanced capture unit 1 input 1 pin.
	ECAP1_IC2	I	Enhanced capture unit 1 input 2 pin.

Group	Pin Name	Type	Description
ECAP2	ECAP2_IC0	I	Enhanced capture unit 2 input 0 pin.
	ECAP2_IC1	I	Enhanced capture unit 2 input 1 pin.
	ECAP2_IC2	I	Enhanced capture unit 2 input 2 pin.
ECAP3	ECAP3_IC0	I	Enhanced capture unit 3 input 0 pin.
	ECAP3_IC1	I	Enhanced capture unit 3 input 1 pin.
	ECAP3_IC2	I	Enhanced capture unit 3 input 2 pin.
EMAC0	EMAC0_PPS	O	EMAC0 Pulse Per Second output pin.
	EMAC0_RMII_CRSDV	I	EMAC0 RMII Carrier Sense/Receive Data input pin.
	EMAC0_RMII_MDC	O	EMAC0 RMII PHY Management Clock output pin.
	EMAC0_RMII_MDIO	I/O	EMAC0 RMII PHY Management Data pin.
	EMAC0_RMII_REFCLK	I	EMAC0 RMII reference clock input pin.
	EMAC0_RMII_RXD0	I	EMAC0 RMII Receive Data bus bit 0.
	EMAC0_RMII_RXD1	I	EMAC0 RMII Receive Data bus bit 1.
	EMAC0_RMII_RXERR	I	EMAC0 RMII Receive Data Error input pin.
	EMAC0_RMII_TXD0	O	EMAC0 RMII Transmit Data bus bit 0.
	EMAC0_RMII_TXD1	O	EMAC0 RMII Transmit Data bus bit 1.
	EMAC0_RMII_TXEN	O	EMAC0 RMII Transmit Enable output pin.
EPWM0	EPWM0_BRAKE0	I	EPWM0 Brake 0 input pin.
	EPWM0_BRAKE1	I	EPWM0 Brake 1 input pin.
	EPWM0_CH0	I/O	EPWM0 channel 0 output/capture input.
	EPWM0_CH1	I/O	EPWM0 channel 1 output/capture input.
	EPWM0_CH2	I/O	EPWM0 channel 2 output/capture input.
	EPWM0_CH3	I/O	EPWM0 channel 3 output/capture input.
	EPWM0_CH4	I/O	EPWM0 channel 4 output/capture input.
	EPWM0_CH5	I/O	EPWM0 channel 5 output/capture input.
	EPWM0_SYNC_IN	I	EPWM0 counter synchronous trigger input pin.
	EPWM0_SYNC_OUT	O	EPWM0 counter synchronous trigger output pin.
EPWM1	EPWM1_BRAKE0	I	EPWM1 Brake 0 input pin.
	EPWM1_BRAKE1	I	EPWM1 Brake 1 input pin.
	EPWM1_CH0	I/O	EPWM1 channel 0 output/capture input.
	EPWM1_CH1	I/O	EPWM1 channel 1 output/capture input.
	EPWM1_CH2	I/O	EPWM1 channel 2 output/capture input.
	EPWM1_CH3	I/O	EPWM1 channel 3 output/capture input.
	EPWM1_CH4	I/O	EPWM1 channel 4 output/capture input.

Group	Pin Name	Type	Description
	EPWM1_CH5	I/O	EPWM1 channel 5 output/capture input.
EQEI0	EQEI0_A	I	EQEI0 phase A input
	EQEI0_B	I	EQEI0 phase B input
	EQEI0_INDEX	I	EQEI0 index input
EQEI1	EQEI1_A	I	EQEI1 phase A input
	EQEI1_B	I	EQEI1 phase B input
	EQEI1_INDEX	I	EQEI1 index input
EQEI2	EQEI2_A	I	EQEI2 phase A input
	EQEI2_B	I	EQEI2 phase B input
	EQEI2_INDEX	I	EQEI2 index input
EQEI3	EQEI3_A	I	EQEI3 phase A input
	EQEI3_B	I	EQEI3 phase B input
	EQEI3_INDEX	I	EQEI3 index input
ETMC	ETMC_TRACE_CLK	I	ETM receiver Trace Clock input pin
	ETMC_TRACE_DATA0	I	ETM receiver Trace Data 0 input pin
	ETMC_TRACE_DATA1	I	ETM receiver Trace Data 1 input pin
	ETMC_TRACE_DATA2	I	ETM receiver Trace Data 2 input pin
	ETMC_TRACE_DATA3	I	ETM receiver Trace Data 3 input pin
HBI	HBI_CK	O	HyperBus clock pin.
	HBI_D0	I/O	HyperBus data 0 pin.
	HBI_D1	I/O	HyperBus data 1 pin.
	HBI_D2	I/O	HyperBus data 2 pin.
	HBI_D3	I/O	HyperBus data 3 pin.
	HBI_D4	I/O	HyperBus data 4 pin.
	HBI_D5	I/O	HyperBus data 5 pin.
	HBI_D6	I/O	HyperBus data 6 pin.
	HBI_D7	I/O	HyperBus data 7 pin.
	HBI_PWR		
	HBI_RWDS	I/O	HyperBus read-write data strobe pin.
	HBI_nCK	O	HyperBus reverse clock pin.
	HBI_nCS	O	HyperBus chip select pin.
	HBI_nRESET	O	HyperBus reset pin.

Group	Pin Name	Type	Description
HSUSB	HSUSB_VBUS_EN	O	HSUSB external V_{BUS} regulator enable pin.
	HSUSB_VBUS_ST	I	HSUSB external V_{BUS} regulator status pin.
I2C0	I2C0_SCL	I/O	I2C0 clock pin.
	I2C0_SDA	I/O	I2C0 data input/output pin.
	I2C0_SMBAL	O	I2C0 SMBus SMBALTER pin
	I2C0_SMBSUS	O	I2C0 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C1	I2C1_SCL	I/O	I2C1 clock pin.
	I2C1_SDA	I/O	I2C1 data input/output pin.
	I2C1_SMBAL	O	I2C1 SMBus SMBALTER pin
	I2C1_SMBSUS	O	I2C1 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C2	I2C2_SCL	I/O	I2C2 clock pin.
	I2C2_SDA	I/O	I2C2 data input/output pin.
	I2C2_SMBAL	O	I2C2 SMBus SMBALTER pin
	I2C2_SMBSUS	O	I2C2 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C3	I2C3_SCL	I/O	I2C3 clock pin.
	I2C3_SDA	I/O	I2C3 data input/output pin.
	I2C3_SMBAL	O	I2C3 SMBus SMBALTER pin
	I2C3_SMBSUS	O	I2C3 SMBus SMBSUS pin (PMBus CONTROL pin)
I2C4	I2C4_SCL	I/O	I2C4 clock pin.
	I2C4_SDA	I/O	I2C4 data input/output pin.
	I2C4_SMBAL	O	I2C4 SMBus SMBALTER pin
	I2C4_SMBSUS	O	I2C4 SMBus SMBSUS pin (PMBus CONTROL pin)
I2S0	I2S0_BCLK	O	I2S0 bit clock output pin.
	I2S0_DI	I	I2S0 data input pin.
	I2S0_DO	O	I2S0 data output pin.
	I2S0_LRCK	O	I2S0 left right channel clock output pin.
	I2S0_MCLK	O	I2S0 master clock output pin.
I2S1	I2S1_BCLK	O	I2S1 bit clock output pin.
	I2S1_DI	I	I2S1 data input pin.
	I2S1_DO	O	I2S1 data output pin.
	I2S1_LRCK	O	I2S1 left right channel clock output pin.
	I2S1_MCLK	O	I2S1 master clock output pin.
ICE	ICE_CLK	I	Serial wired debugger clock pin. **Note:** It is recommended to use 100 kΩ pull-up resistor on ICE_CLK pin.
	ICE_DAT	I/O	Serial wired debugger data pin.

Group	Pin Name	Type	Description
			Note: It is recommended to use 100 kΩ pull-up resistor on ICE_DAT pin.
INT0	INT0	I	External interrupt 0 input pin.
INT1	INT1	I	External interrupt 1 input pin.
INT2	INT2	I	External interrupt 2 input pin.
INT3	INT3	I	External interrupt 3 input pin.
INT4	INT4	I	External interrupt 4 input pin.
INT5	INT5	I	External interrupt 5 input pin.
INT6	INT6	I	External interrupt 6 input pin.
INT7	INT7	I	External interrupt 7 input pin.
KPI	KPI_COL0	I	Keypad Interface Column 0 input pin.
	KPI_COL1	I	Keypad Interface Column 1 input pin.
	KPI_COL2	I	Keypad Interface Column 2 input pin.
	KPI_COL3	I	Keypad Interface Column 3 input pin.
	KPI_COL4	I	Keypad Interface Column 4 input pin.
	KPI_COL5	I	Keypad Interface Column 5 input pin.
	KPI_COL6	I	Keypad Interface Column 6 input pin.
	KPI_COL7	I	Keypad Interface Column 7 input pin.
	KPI_ROW0	O	Keypad Interface Row 0 output pin.
	KPI_ROW1	O	Keypad Interface Row 1 output pin.
	KPI_ROW2	O	Keypad Interface Row 2 output pin.
	KPI_ROW3	O	Keypad Interface Row 3 output pin.
	KPI_ROW4	O	Keypad Interface Row 4 output pin.
	KPI_ROW5	O	Keypad Interface Row 5 output pin.
PSIO0	PSIO0_CH0	I/O	PSIO 0 channel 0 input/output pin.
	PSIO0_CH1	I/O	PSIO 0 channel 1 input/output pin.
	PSIO0_CH2	I/O	PSIO 0 channel 2 input/output pin.
	PSIO0_CH3	I/O	PSIO 0 channel 3 input/output pin.
	PSIO0_CH4	I/O	PSIO 0 channel 4 input/output pin.
	PSIO0_CH5	I/O	PSIO 0 channel 5 input/output pin.
	PSIO0_CH6	I/O	PSIO 0 channel 6 input/output pin.
	PSIO0_CH7	I/O	PSIO 0 channel 7 input/output pin.
QSPI0	QSPI0_CLK	I/O	Quad SPI0 serial clock pin.
	QSPI0_MISO0	I/O	Quad SPI0 MISO0 (Master In, Slave Out) pin.
	QSPI0_MISO1	I/O	Quad SPI0 MISO1 (Master In, Slave Out) pin.
	QSPI0_MOSI0	I/O	Quad SPI0 MOSI0 (Master Out, Slave In) pin.

Group	Pin Name	Type	Description
	QSPI0_MOSI1	I/O	Quad SPI0 MOSI1 (Master Out, Slave In) pin.
	QSPI0_SS	I/O	Quad SPI0 slave select pin.
QSPI1	QSPI1_CLK	I/O	Quad SPI1 serial clock pin.
	QSPI1_MISO0	I/O	Quad SPI1 MISO0 (Master In, Slave Out) pin.
	QSPI1_MISO1	I/O	Quad SPI1 MISO1 (Master In, Slave Out) pin.
	QSPI1_MOSI0	I/O	Quad SPI1 MOSI0 (Master Out, Slave In) pin.
	QSPI1_MOSI1	I/O	Quad SPI1 MOSI1 (Master Out, Slave In) pin.
	QSPI1_SS	I/O	Quad SPI1 slave select pin.
SC0	SC0_CLK	O	Smart Card 0 clock pin.
	SC0_DAT	I/O	Smart Card 0 data pin.
	SC0_PWR	O	Smart Card 0 power pin.
	SC0_RST	O	Smart Card 0 reset pin.
	SC0_nCD	I	Smart Card 0 card detect pin.
SC1	SC1_CLK	O	Smart Card 1 clock pin.
	SC1_DAT	I/O	Smart Card 1 data pin.
	SC1_PWR	O	Smart Card 1 power pin.
	SC1_RST	O	Smart Card 1 reset pin.
	SC1_nCD	I	Smart Card 1 card detect pin.
SC2	SC2_CLK	O	Smart Card 2 clock pin.
	SC2_DAT	I/O	Smart Card 2 data pin.
	SC2_PWR	O	Smart Card 2 power pin.
	SC2_RST	O	Smart Card 2 reset pin.
	SC2_nCD	I	Smart Card 2 card detect pin.
SD0	SD0_CLK	O	SD/SDIO0 clock output pin
	SD0_CMD	I/O	SD/SDIO0 command/response pin
	SD0_DAT0	I/O	SD/SDIO0 data line bit 0.
	SD0_DAT1	I/O	SD/SDIO0 data line bit 1.
	SD0_DAT2	I/O	SD/SDIO0 data line bit 2.
	SD0_DAT3	I/O	SD/SDIO0 data line bit 3.
	SD0_nCD	I	SD/SDIO0 card detect input pin
SD1	SD1_CLK	O	SD/SDIO1 clock output pin
	SD1_CMD	I/O	SD/SDIO1 command/response pin
	SD1_DAT0	I/O	SD/SDIO1 data line bit 0.
	SD1_DAT1	I/O	SD/SDIO1 data line bit 1.

Group	Pin Name	Type	Description
	SD1_DAT2	I/O	SD/SDIO1 data line bit 2.
	SD1_DAT3	I/O	SD/SDIO1 data line bit 3.
	SD1_nCD	I	SD/SDIO1 card detect input pin
SPI0	SPI0_CLK	I/O	SPI0 serial clock pin.
	SPI0_I2SMCLK	I/O	SPI0 I^2S master clock output pin
	SPI0_MISO	I/O	SPI0 MISO (Master In, Slave Out) pin.
	SPI0_MOSI	I/O	SPI0 MOSI (Master Out, Slave In) pin.
	SPI0_SS	I/O	SPI0 slave select pin.
SPI1	SPI1_CLK	I/O	SPI1 serial clock pin.
	SPI1_I2SMCLK	I/O	SPI1 I^2S master clock output pin
	SPI1_MISO	I/O	SPI1 MISO (Master In, Slave Out) pin.
	SPI1_MOSI	I/O	SPI1 MOSI (Master Out, Slave In) pin.
	SPI1_SS	I/O	SPI1 slave select pin.
SPI2	SPI2_CLK	I/O	SPI2 serial clock pin.
	SPI2_I2SMCLK	I/O	SPI2 I^2S master clock output pin
	SPI2_MISO	I/O	SPI2 MISO (Master In, Slave Out) pin.
	SPI2_MOSI	I/O	SPI2 MOSI (Master Out, Slave In) pin.
	SPI2_SS	I/O	SPI2 slave select pin.
SPI3	SPI3_CLK	I/O	SPI3 serial clock pin.
	SPI3_I2SMCLK	I/O	SPI3 I^2S master clock output pin
	SPI3_MISO	I/O	SPI3 MISO (Master In, Slave Out) pin.
	SPI3_MOSI	I/O	SPI3 MOSI (Master Out, Slave In) pin.
	SPI3_SS	I/O	SPI3 slave select pin.
SPI4	SPI4_CLK	I/O	SPI4 serial clock pin.
	SPI4_MISO	I/O	SPI4 MISO (Master In, Slave Out) pin.
	SPI4_MOSI	I/O	SPI4 MOSI (Master Out, Slave In) pin.
	SPI4_SS	I/O	SPI4 slave select pin.
SPI5	SPI5_CLK	I/O	SPI5 serial clock pin.
	SPI5_MISO	I/O	SPI5 MISO (Master In, Slave Out) pin.
	SPI5_MOSI	I/O	SPI5 MOSI (Master Out, Slave In) pin.
	SPI5_SS	I/O	SPI5 slave select pin.
SPI6	SPI6_CLK	I/O	SPI6 serial clock pin.
	SPI6_MISO	I/O	SPI6 MISO (Master In, Slave Out) pin.
	SPI6_MOSI	I/O	SPI6 MOSI (Master Out, Slave In) pin.

Group	Pin Name	Type	Description
	SPI6_SS	I/O	SPI6 slave select pin.
SPI7	SPI7_CLK	I/O	SPI7 serial clock pin.
	SPI7_MISO	I/O	SPI7 MISO (Master In, Slave Out) pin.
	SPI7_MOSI	I/O	SPI7 MOSI (Master Out, Slave In) pin.
	SPI7_SS	I/O	SPI7 slave select pin.
SPI8	SPI8_CLK	I/O	SPI8 serial clock pin.
	SPI8_MISO	I/O	SPI8 MISO (Master In, Slave Out) pin.
	SPI8_MOSI	I/O	SPI8 MOSI (Master Out, Slave In) pin.
	SPI8_SS	I/O	SPI8 slave select pin.
SPI9	SPI9_CLK	I/O	SPI9 serial clock pin.
	SPI9_MISO	I/O	SPI9 MISO (Master In, Slave Out) pin.
	SPI9_MOSI	I/O	SPI9 MOSI (Master Out, Slave In) pin.
	SPI9_SS	I/O	SPI9 slave select pin.
SPI10	SPI10_CLK	I/O	SPI10 serial clock pin.
	SPI10_MISO	I/O	SPI10 MISOO (Master In, Slave Out) pin.
	SPI10_MOSI	I/O	SPI10 MOSII (Master Out, Slave In) pin.
	SPI10_SS	I/O	SPI10 slave select S pin.
SPIM	SPIM_CLK	I/O	SPIM serial clock pin.
	SPIM_D2	I/O	SPIM data 2 pin for Quad Mode I/O.
	SPIM_D3	I/O	SPIM data 3 pin for Quad Mode I/O.
	SPIM_MISO	I/O	SPIM MISO (Master In, Slave Out) pin.
	SPIM_MOSI	I/O	SPIM MOSI (Master Out, Slave In) pin.
	SPIM_SS	I/O	SPIM slave select pin.
SWDH	SWDH_CLK	O	Serial Wire Debug Host Clock output
	SWDH_DAT	I/O	Serial Wire Debug Host Data input/output pin
TAMPER0	TAMPER0	I/O	TAMPER detector loop pin 0.
TAMPER1	TAMPER1	I/O	TAMPER detector loop pin 1.
TAMPER2	TAMPER2	I/O	TAMPER detector loop pin 2.
TAMPER3	TAMPER3	I/O	TAMPER detector loop pin 3.
TAMPER4	TAMPER4	I/O	TAMPER detector loop pin 4.
TAMPER5	TAMPER5	I/O	TAMPER detector loop pin 5.
TM0	TM0	I/O	Timer0 event counter input/toggle output pin.
	TM0_EXT	I/O	Timer0 external capture input/toggle output pin.
TM1	TM1	I/O	Timer1 event counter input/toggle output pin.

Group	Pin Name	Type	Description
	TM1_EXT	I/O	Timer1 external capture input/toggle output pin.
TM2	TM2	I/O	Timer2 event counter input/toggle output pin.
	TM2_EXT	I/O	Timer2 external capture input/toggle output pin.
TM3	TM3	I/O	Timer3 event counter input/toggle output pin.
	TM3_EXT	I/O	Timer3 external capture input/toggle output pin.
TRACE	TRACE_CLK	O	ETM Trace Clock output pin
	TRACE_DATA0	O	ETM Trace Data 0 output pin
	TRACE_DATA1	O	ETM Trace Data 1 output pin
	TRACE_DATA2	O	ETM Trace Data 2 output pin
	TRACE_DATA3	O	ETM Trace Data 3 output pin
	TRACE_SWO	O	Trace Single Wire output pin.
UART0	UART0_RXD	I	UART0 data receiver input pin.
	UART0_TXD	O	UART0 data transmitter output pin.
	UART0_nCTS	I	UART0 clear to Send input pin.
	UART0_nRTS	O	UART0 request to Send output pin.
UART1	UART1_RXD	I	UART1 data receiver input pin.
	UART1_TXD	O	UART1 data transmitter output pin.
	UART1_nCTS	I	UART1 clear to Send input pin.
	UART1_nRTS	O	UART1 request to Send output pin.
UART2	UART2_RXD	I	UART2 data receiver input pin.
	UART2_TXD	O	UART2 data transmitter output pin.
	UART2_nCTS	I	UART2 clear to Send input pin.
	UART2_nRTS	O	UART2 request to Send output pin.
UART3	UART3_RXD	I	UART3 data receiver input pin.
	UART3_TXD	O	UART3 data transmitter output pin.
	UART3_nCTS	I	UART3 clear to Send input pin.
	UART3_nRTS	O	UART3 request to Send output pin.
UART4	UART4_RXD	I	UART4 data receiver input pin.
	UART4_TXD	O	UART4 data transmitter output pin.
	UART4_nCTS	I	UART4 clear to Send input pin.
	UART4_nRTS	O	UART4 request to Send output pin.
UART5	UART5_RXD	I	UART5 data receiver input pin.
	UART5_TXD	O	UART5 data transmitter output pin.
	UART5_nCTS	I	UART5 clear to Send input pin.

Group	Pin Name	Type	Description
	UART5_nRTS	O	UART5 request to Send output pin.
UART6	UART6_RXD	I	UART6 data receiver input pin.
	UART6_TXD	O	UART6 data transmitter output pin.
	UART6_nCTS	I	UART6 clear to Send input pin.
	UART6_nRTS	O	UART6 request to Send output pin.
UART7	UART7_RXD	I	UART7 data receiver input pin.
	UART7_TXD	O	UART7 data transmitter output pin.
	UART7_nCTS	I	UART7 clear to Send input pin.
	UART7_nRTS	O	UART7 request to Send output pin.
UART8	UART8_RXD	I	UART8 data receiver input pin.
	UART8_TXD	O	UART8 data transmitter output pin.
	UART8_nCTS	I	UART8 clear to Send input pin.
	UART8_nRTS	O	UART8 request to Send output pin.
UART9	UART9_RXD	I	UART9 data receiver input pin.
	UART9_TXD	O	UART9 data transmitter output pin.
	UART9_nCTS	I	UART9 clear to Send input pin.
	UART9_nRTS	O	UART9 request to Send output pin.
USB	USB_D+	A	USB differential signal D+.
	USB_D-	A	USB differential signal D-.
	USB_OTG_ID	I	USB_ identification.
	USB_VBUS	I/O	Power supply from USB host or HUB.
	USB_VBUS_EN	O	USB external V_{BUS} regulator enable pin.
	USB_VBUS_ST	I	USB external V_{BUS} regulator status pin.
	HSUSB_D+	A	HSUSB differential signal D+.
	HSUSB_D-	A	HSUSB differential signal D-.
	HSUSB_ID	I	HSUSB identification.
	HSUSB_VBUS	I/O	HSUSB Power supply from USB host or HUB.
	HSUSB_VDD12_CAP	A	HSUSB Internal power regulator output 1.2V decoupling pin. **Note:** This pin needs to be connected with a 1uF capacitor.
	HSUSB_VDD33	P	Power supply for HSUSB VDD33
	HSUSB_VRES	A	HSUSB module reference resister
	HSUSB_VSS	P	Ground pin for HSUSB.
USCI0	USCI0_CLK	I/O	USCI0 clock pin.
	USCI0_CTL0	I/O	USCI0 control 0 pin.
	USCI0_CTL1	I/O	USCI0 control 1 pin.

Group	Pin Name	Type	Description
	USCI0_DAT0	I/O	USCI0 data 0 pin.
	USCI0_DAT1	I/O	USCI0 data 1 pin.
X32	X32_IN	I	External 32.768 kHz crystal input pin.
	X32_OUT	O	External 32.768 kHz crystal output pin.
XT1	XT1_IN	I	External 4~24 MHz (high speed) crystal input pin.
	XT1_OUT	O	External 4~24 MHz (high speed) crystal output pin.
Power	AV_{DD}	P	Power supply for internal analog circuit.
	AV_{SS}	P	Ground pin for analog circuit.
	HBI_PWR	P	Power supply for internal HyperRAM.
	LDO_CAP	A	LDO output pin. **Note:** This pin needs to be connected with a capacitor whose value can be found in General operating conditions table in Datasheet.
	V_{BAT}	P	Power supply by batteries for RTC.
	V_{DD}	P	Power supply for I/O ports and LDO source for internal PLL and digital circuit.
	V_{DDIO}	P	Power supply for PA.0~PA.5.
	V_{REF}	A	ADC reference voltage input. **Note:** This pin needs to be connected with a 1uF capacitor.
	V_{SS}	P	Ground pin for digital circuit.
	nRESET	I	External reset input: active LOW, with an internal pull-up. Set this pin low reset to initial state. **Note:** It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

5 BLOCK DIAGRAM

5.1 M463/M467 Series Block Diagram

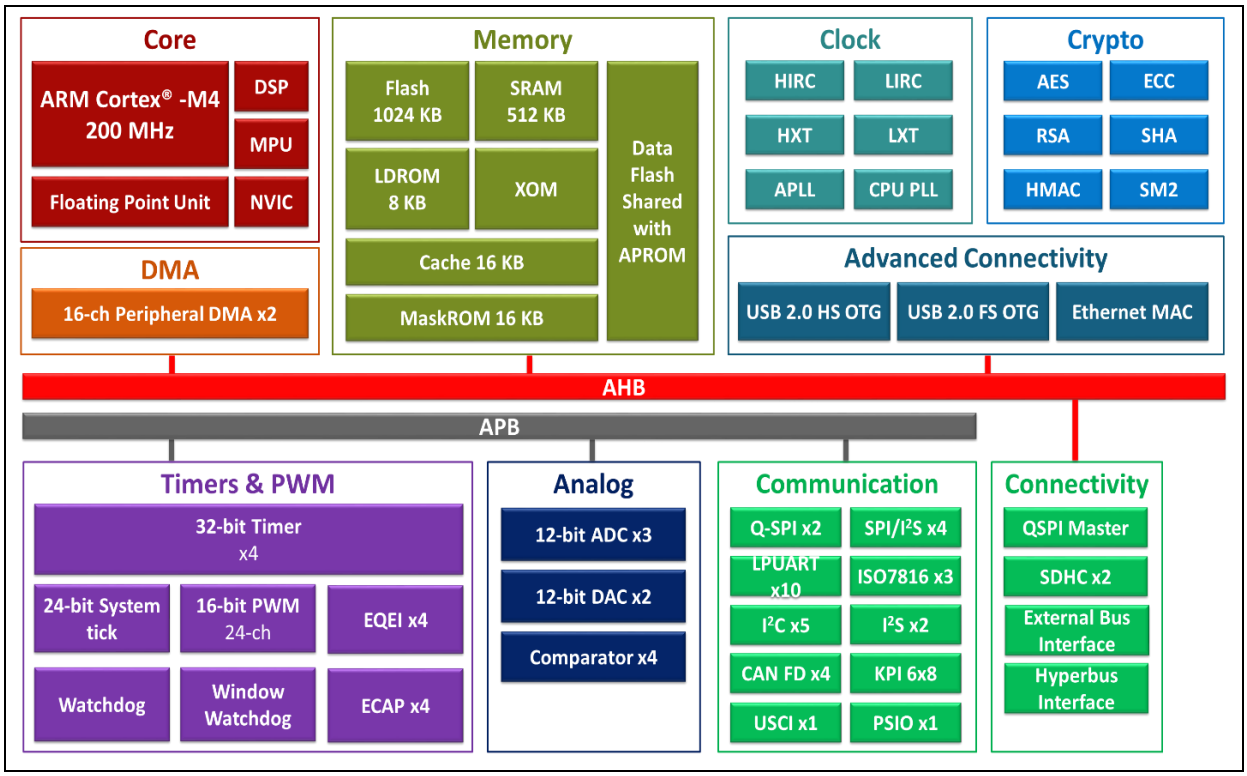


Figure 5.1-1 M463/M467 Series Block Diagram

6 FUNCTIONAL DESCRIPTION

6.1 ARM Cortex-M4 Core

The Cortex-M4 processor, a configurable, multistage, 32-bit RISC processor, has three AMBA AHB-Lite interfaces for best parallel performance and includes an NVIC component. The processor with optional hardware debug functionality can execute Thumb code and is compatible with other Cortex-M profile processors. The profile supports two modes -Thread mode and Handler mode. Handler mode is entered as a result of an exception. An exception return can only be issued in Handler mode. Thread mode is entered on Reset, and can be entered as a result of an exception return. The Cortex-M4F is a processor with the same capability as the Cortex-M4 processor and includes floating point arithmetic functionality. The NuMicro M463/M467 series is embedded with Cortex-M4F processor. Throughout this document, the name Cortex-M4 refers to both Cortex-M4 and Cortex-M4F processors.

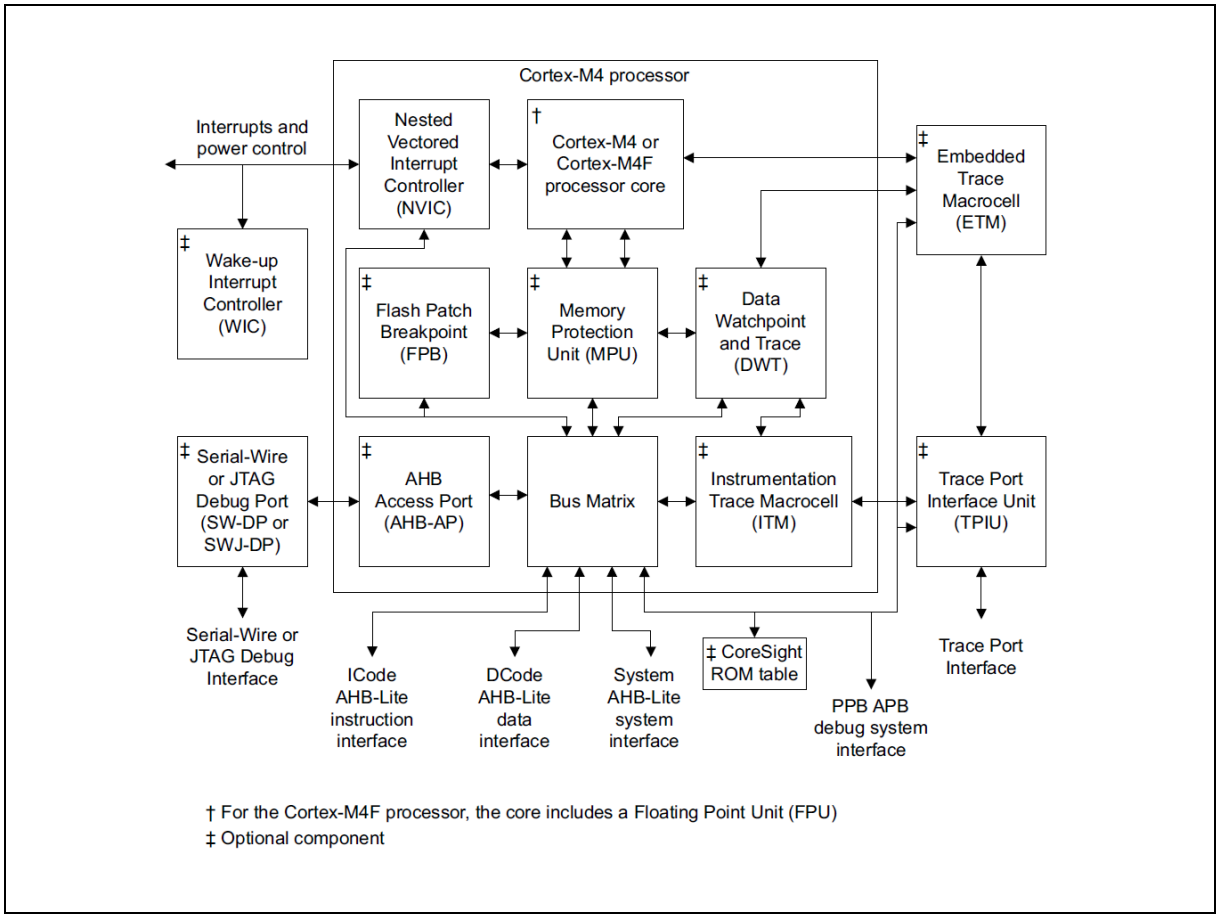


Figure 6.1-1 Cortex-M4 Block Diagram

Cortex-M4 processor features:

- A low gate count processor core, with low latency interrupt processing that has:
  - A subset of the Thumb instruction set, defined in the *ARMv7-M Architecture Reference Manual*
  - Banked Stack Pointer (SP)
  - Hardware integer divide instructions, SDIV and UDIV
  - Handler and Thread modes
  - Thumb and Debug states

- Support for interruptible-continued instructions LDM, STM, PUSH, and POP for low interrupt latency
- Automatic processor state saving and restoration for low latency *Interrupt Service Routine (ISR)* entry and exit
- Support for ARMv6 big-endian byte-invariant or little-endian accesses
- Support for ARMv6 unaligned accesses

- Floating Point Unit (FPU) in the Cortex-M4F processor providing:
  - 32-bit instructions for single-precision (C float) data-processing operations
  - Combined Multiply and Accumulate instructions for increased precision (Fused MAC)
  - Hardware support for conversion, addition, subtraction, multiplication with optional accumulate, division, and square-root
  - Hardware support for denormals and all IEEE rounding modes
  - 32 dedicated 32-bit single precision registers, also addressable as 16 double-word registers
  - Decoupled three stage pipeline
- Nested Vectored Interrupt Controller (NVIC) closely integrated with the processor core to achieve low latency interrupt processing. Features include:
  - External interrupts. Configurable from 1 to 240
  - Bits of priority, configurable from 3 to 8
  - Dynamic reprioritization of interrupts
  - Priority grouping which enables selection of preempting interrupt levels and nonpreempting interrupt levels
  - Support for tril-chaining and late arrival of interrupts, which enables back-to-back interrupt processing without the overhead of state saving and restoration between interrupts.
  - Processor state automatically saved on interrupt entry, and restored on interrupt exit with on instruction overhead
  - Support for Wake-up Interrupt Controller (WIC) with Ultra-low Power Sleep mode
- Memory Protection Unit (MPU). An optional MPU for memory protection, including:
  - Eight memory regions
  - Sub Region Disable (SRD), enabling efficient use of memory regions
  - The ability to enable a background region that implements the default memory map attributes
- Low-cost debug solution that features:
  - Debug access to all memory and registers in the system, including access to memory mapped devices, access to internal core registers when the core is halted, and access to debug control registers even while SYSRESETn is asserted.
  - Serial Wire Debug Port(SW-DP) or Serial Wire JTAG Debug Port (SWJ-DP) debug access
  - Optional Flash Patch and Breakpoint (FPB) unit for implementing breakpoints and code patches
  - Optional Data Watchpoint and Trace (DWT) unit for implementing watchpoints, data

tracing, and system profiling

- Optional Instrumentation Trace Macrocell (ITM) for support of printf() style debugging
- Optional Trace Port Interface Unit (TPIU) for bridging to a Trace Port Analyzer (TPA), including Single Wire Output (SWO) mode
- Optional Embedded Trace Macrocell (ETM) for instruction trace.

- Bus interfaces:
  - Three Advanced High-performance Bus-Lite (AHB-Lite) interfaces: ICode, Dcode, and System bus interfaces
  - Private Peripheral Bus (PPB) based on Advanced Peripheral Bus (APB) interface
  - Bit-band support that includes atomic bit-band write and read operations.
  - Memory access alignment
  - Write buffer for buffering of write data
  - Exclusive access transfers for multiprocessor systems

6.2 System Manager

6.2.1 Overview

System management includes the following sections:

- System Reset
- System Power Distribution
- SRAM Memory Organization
- System Timer (SysTick)
- Nested Vectored Interrupt Controller (NVIC)
- System Control register

6.2.2 System Reset

The system reset can be issued by one of the events listed below. These reset event flags can be read from SYS_RSTSTS register to determine the reset source. Hardware reset sources are from peripheral signals. Software reset can trigger reset through setting control registers.

- Hardware Reset Sources
  - Power-on Reset
  - Low level on the nRESET pin
  - Watchdog Time-out Reset and Window Watchdog Reset (WDT/WWDT Reset)
  - Low Voltage Reset (LVR)
  - Brown-out Detector Reset (BOD Reset)
  - CPU Lockup Reset
- Software Reset Sources
  - CHIP Reset will reset whole chip by writing 1 to CHIPRST (SYS_IPRST0[0])
  - MCU Reset to reboot but keeping the booting setting from APROM or LDROM by writing 1 to SYSRESETREQ (AIRCR[2])
  - CPU Reset for Cortex-M4 core only by writing 1 to CPURST (SYS_IPRST0[1])

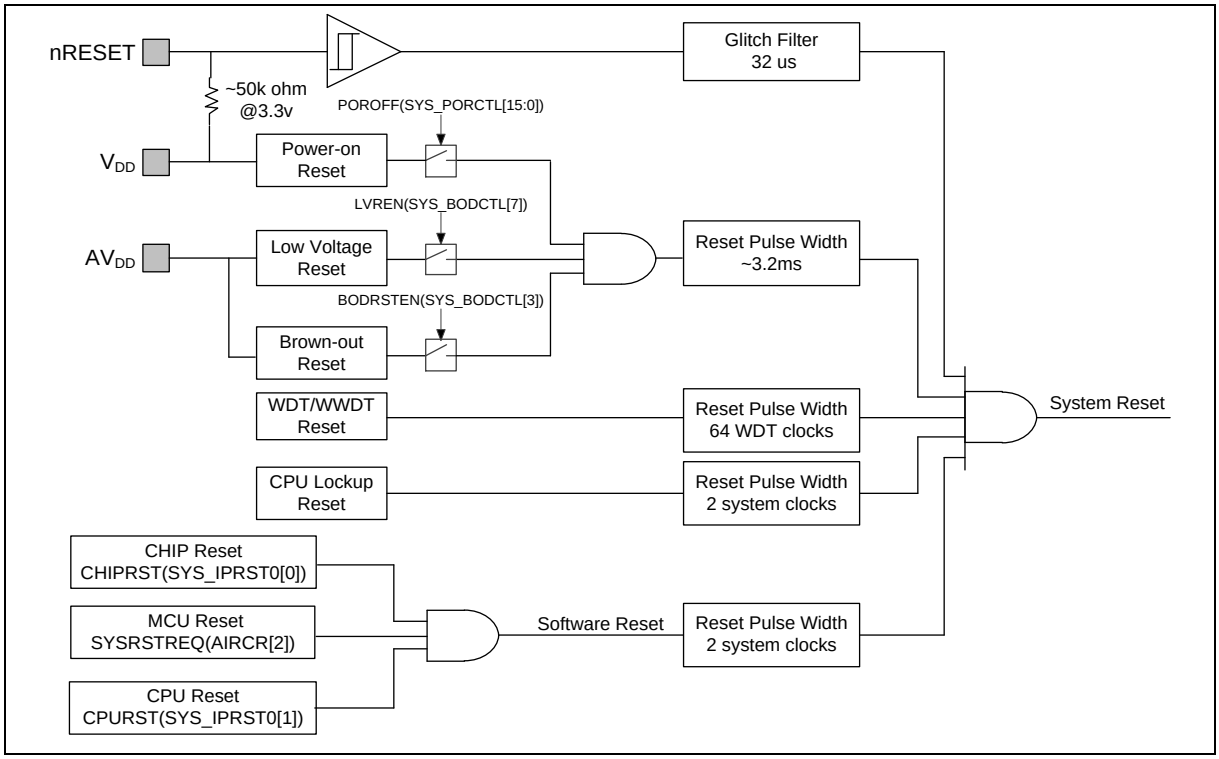


Figure 6.2-1 System Reset Sources

The Mask ROM which is built-in secure boot and ROM ISP function is the initial boot source after chip is powered on or cold reset. User can refer to Mask ROM application note for the detailed features and functions. System cold reset events include nRESET pin, WDT/WWDT, LVR, BOD, CHIP reset and wake-up from Deep Power-down mode (DPD). Other reset events include MCU, CPU, Lockup reset and wake-up from Standby Power-down mode (SPD) are defined as warm reset events.

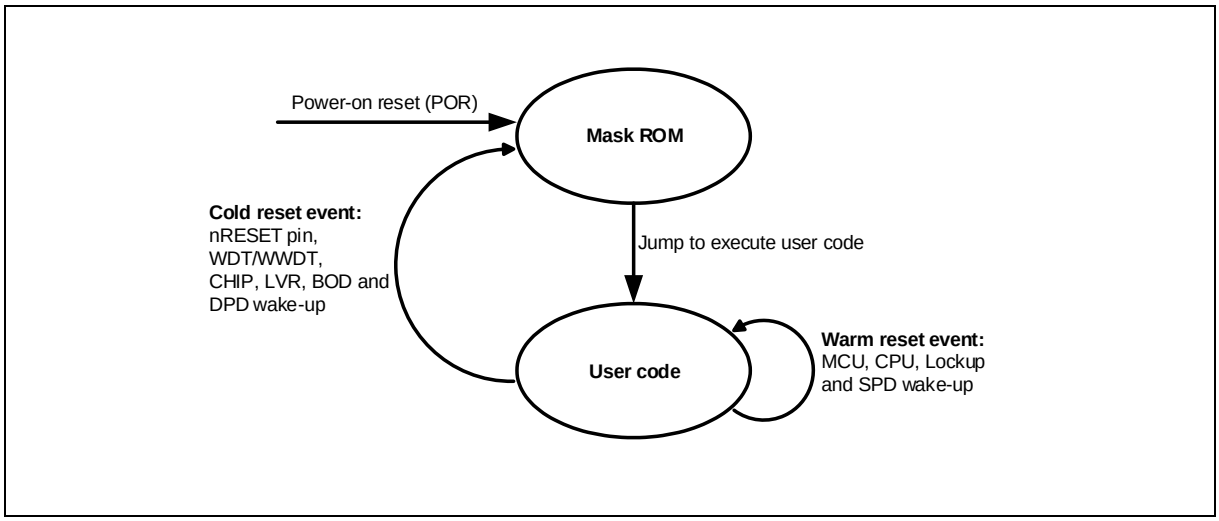


Figure 6.2-2 Reset Event State Machine

There are a total of 9 reset sources in the NuMicro family. In general, CPU reset is used to reset Cortex-M4 only; the other reset sources will reset Cortex-M4 and all peripherals. However, there are small differences between each reset source and they are listed in Table 6.2-1.

Reset Sources Register	POR	NRESET	WDT	LVR	BOD	Lockup	CHIP	MCU	CPU
SYS_RSTSTS	Bit 0 = 1	Bit 1 = 1	Bit 2 = 1	Bit 3 = 1	Bit 4 = 1	Bit 8 = 1	Bit 0 = 1	Bit 5 = 1	Bit 7 = 1
CHIPRST (SYS_IPRST0[0])	0x0	-	-	-	-	-	-	-	-
BODEN (SYS_BODCTL[0])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-
BODVL (SYS_BODCTL[2:1])									
BODRSTEN (SYS_BODCTL[3])									
HXTEN (CLK_PWRCTL[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTEN (CLK_PWRCTL[1])	0x0	-	-	-	-	-	-	-	-
WDTCKEN (CLK_APBCLK0[0])	0x1	-	0x1	-	-	-	0x1	-	-
HCLKSEL (CLK_CLKSEL0[2:0])	0x2 PLL	0x2 PLL	0x2 PLL	0x2 PLL	0x2 PLL	0x7 HIRC	0x2 PLL	0x7 HIRC	-
CLK_PCLKDIV	0x11	0x11	0x11	0x11	0x11	0x0	0x11	0x0	-
CLK_PLLCTL	0x8421E	0x8421E	0x8421E	0x8421E	0x8421E	0x5842B	0x8421E	0x5842B	-
WDTSEL (CLK_CLKSEL1[1:0])	0x3	0x3	-	-	-	-	-	-	-
HXTSTB (CLK_STATUS[0])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
LXTSTB (CLK_STATUS[1])	0x0	-	-	-	-	-	-	-	-
PLLSTB (CLK_STATUS[2])	0x1	0x1	0x1	0x1	0x1	0x0	0x1	0x0	-
HIRCSTB (CLK_STATUS[4])	0x1	0x1	0x1	0x1	0x1	0x1	0x1	0x1	-
CLKSFAIL (CLK_STATUS[7])	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0	-
PDMSEL (CLK_PMUCTL[2:0])	0x0	-	-	-	-	-	-	-	-
RSTEN (WDT_CTL[1])	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	Reload from CONFIG0	-	Reload from CONFIG0	-	-
WDTEN (WDT_CTL[7])									
WDT_CTL except bit 1 and bit 7.	0x0800	0x0800	0x0800	0x0800	0x0800	-	0x0800	-	-

WDT_ALTCTL	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_RLDCNT	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CTL	0x3F0800	0x3F0800	0x3F0800	0x3F0800	0x3F0800	-	0x3F0800	-	-
WWDT_STATUS	0x0000	0x0000	0x0000	0x0000	0x0000	-	0x0000	-	-
WWDT_CNT	0x3F	0x3F	0x3F	0x3F	0x3F	-	0x3F	-	-
FMC_DFBA	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	Reload from CONFIG1	-	Reload from CONFIG1	-	-
VECMAP (FMC_ISPSTS[23:9])	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	Reload base on CONFIG0	-	Reload base on CONFIG0	-	-
FMC_CYCCTL	0x8	0x8	0x8	0x8	0x8	0x1	0x8	0x1	-
Debug lock active	Reload base on CONFIG2	Reload base on CONFIG2	Reload base on CONFIG2	Reload base on CONFIG2	Reload base on CONFIG2	-	Reload base on CONFIG2	-	-
Other Peripheral Registers	Reset Value								-
FMC Registers	Reset Value								
Note: '-' means that the value of register keeps original setting.									

Table 6.2-1 Reset Value of Registers

6.2.2.1 nRESET Reset

The nRESET reset means to generate a reset signal by pulling low nRESET pin, which is an asynchronous reset input pin and can be used to reset system at any time. When the nRESET voltage is lower than 0.2 V_{DD} and the state keeps longer than 32 us (glitch filter), chip will be reset. The nRESET reset will control the chip in reset state until the nRESET voltage rises above 0.7 V_{DD} and the state keeps longer than 32 us (glitch filter). The PINRF(SYS_RSTSTS[1]) will be set to 1 if the previous reset source is nRESET reset. Figure 6.2-4 shows the nRESET reset waveform. Note that the nRESET de-glitch time is typically 300ns in SPDx and DPDx mode.

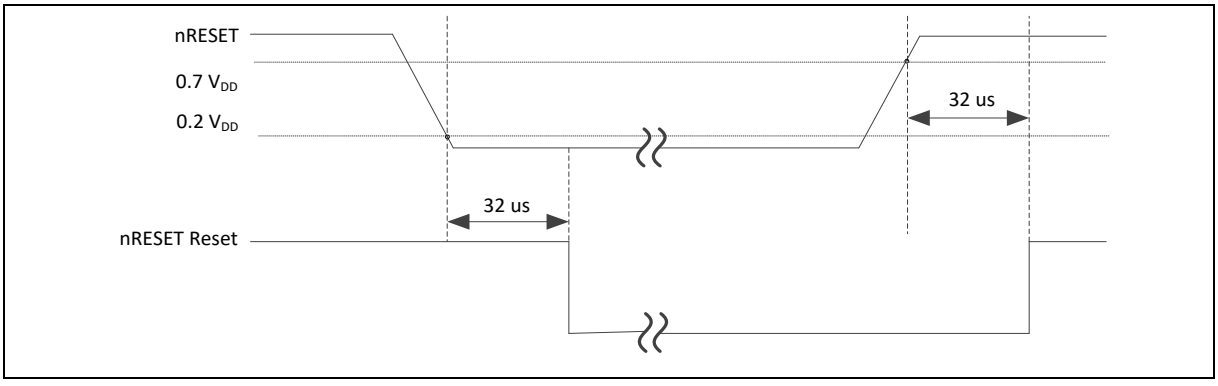


Figure 6.2-3 nRESET Reset Waveform(Except SPDx and DPDx mode)

6.2.2.2 Power-on Reset (POR)

The Power-on reset (POR) is used to generate a stable system reset signal and forces the system to be reset when power-on to avoid unexpected behavior of MCU. When applying the power to MCU, the

POR module will detect the rising voltage and generate reset signal to system until the voltage is ready for MCU operation. At POR reset, the PORF(SYS_RSTSTS[0]) will be set to 1 to indicate there is a POR reset event. The PORF(SYS_RSTSTS[0]) bit can be cleared by writing 1 to it. Figure 6.2-5Figure 6.2-4 shows the power-on reset waveform.

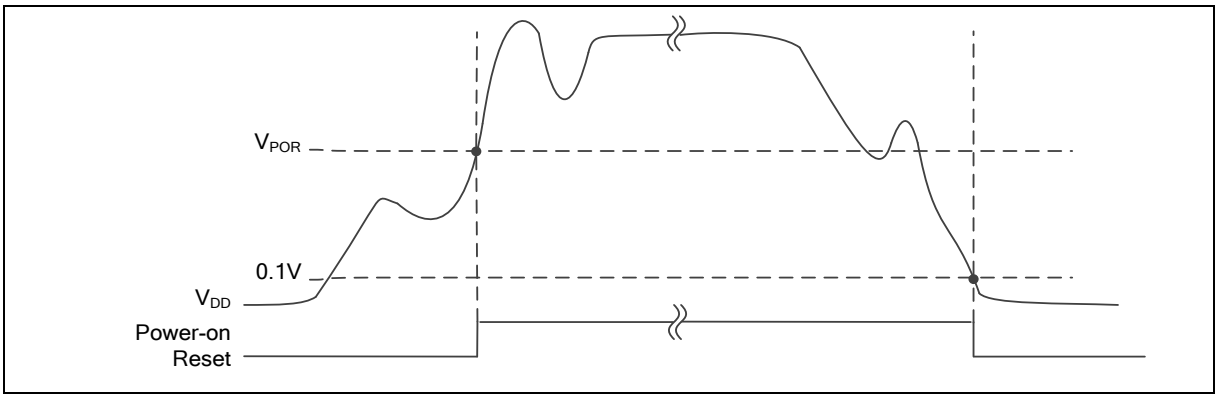


Figure 6.2-4 Power-on Reset (POR) Waveform

6.2.2.3 Low Voltage Reset (LVR)

If the Low Voltage Reset function is enabled by setting the Low Voltage Reset Enable Bit LVREN (SYS_BODCTL[7]) to 1, after 100us~200us delay, LVR detection circuit will be stable and the LVR function will be active. Then LVR function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]), chip will be reset. The LVR reset will control the chip in reset state until the AV_{DD} voltage rises above V_{LVR} and the state keeps longer than De-glitch time set by LVRDGSEL (SYS_BODCTL[14:12]). The default setting of Low Voltage Reset is enabled without De-glitch function. Figure 6.2-6 shows the Low Voltage Reset waveform.

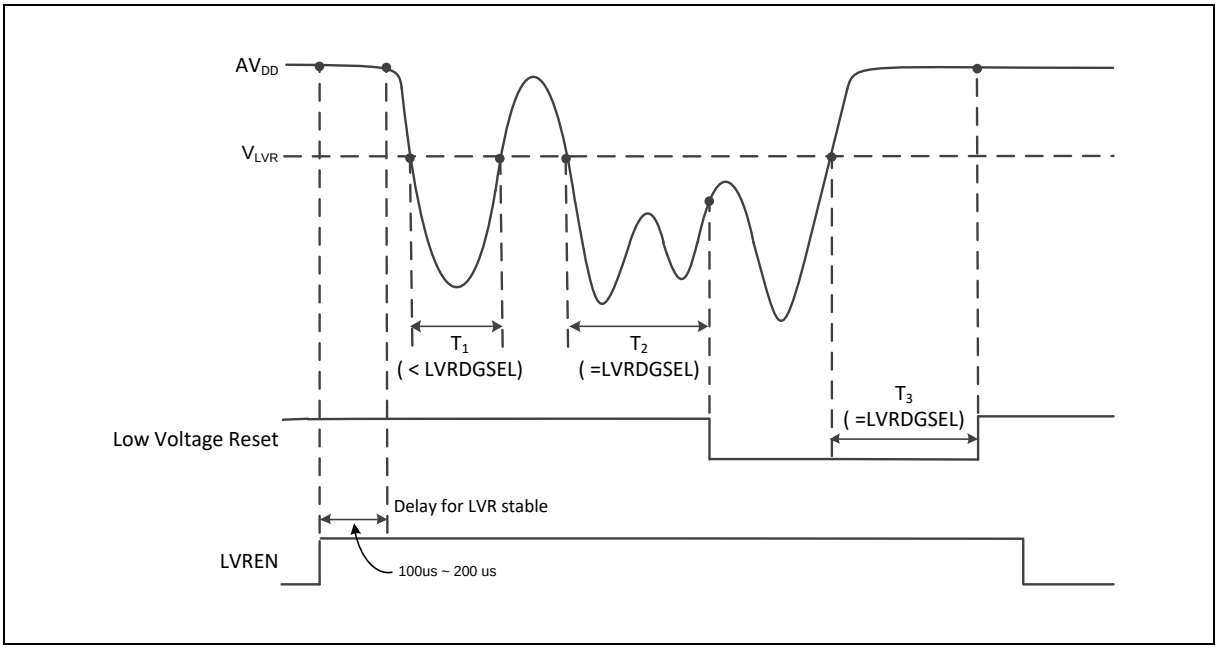


Figure 6.2-5 Low Voltage Reset (LVR) Waveform

6.2.2.4 Brown-out Detector Reset (BOD Reset)

If the Brown-out Detector (BOD) function is enabled by setting the Brown-out Detector Enable Bit BODEN (SYS_BODCTL[0]), Brown-out Detector function will detect AV_{DD} during system operation. When the AV_{DD} voltage is lower than V_{BOD} which is decided by BODEN and BODVL (SYS_BODCTL[18:16]) and the state keeps longer than De-glitch time set by BODDGSEL (SYS_BODCTL[10:8]), chip will be reset. The BOD reset will control the chip in reset state until the AV_{DD} voltage rises above V_{BOD} and the state keeps longer than De-glitch time set by BODDGSEL. The default value of BODEN, BODVL and BODRSTEN (SYS_BODCTL[3]) is set by Flash controller user configuration register CBODEN (CONFIG0 [19]), CBOV (CONFIG0 [23:21]) and CBORST(CONFIG0[20]) respectively. User can determine the initial BOD setting by setting the CONFIG0 register. Figure 6.2-7 shows the Brown-out Detector waveform.

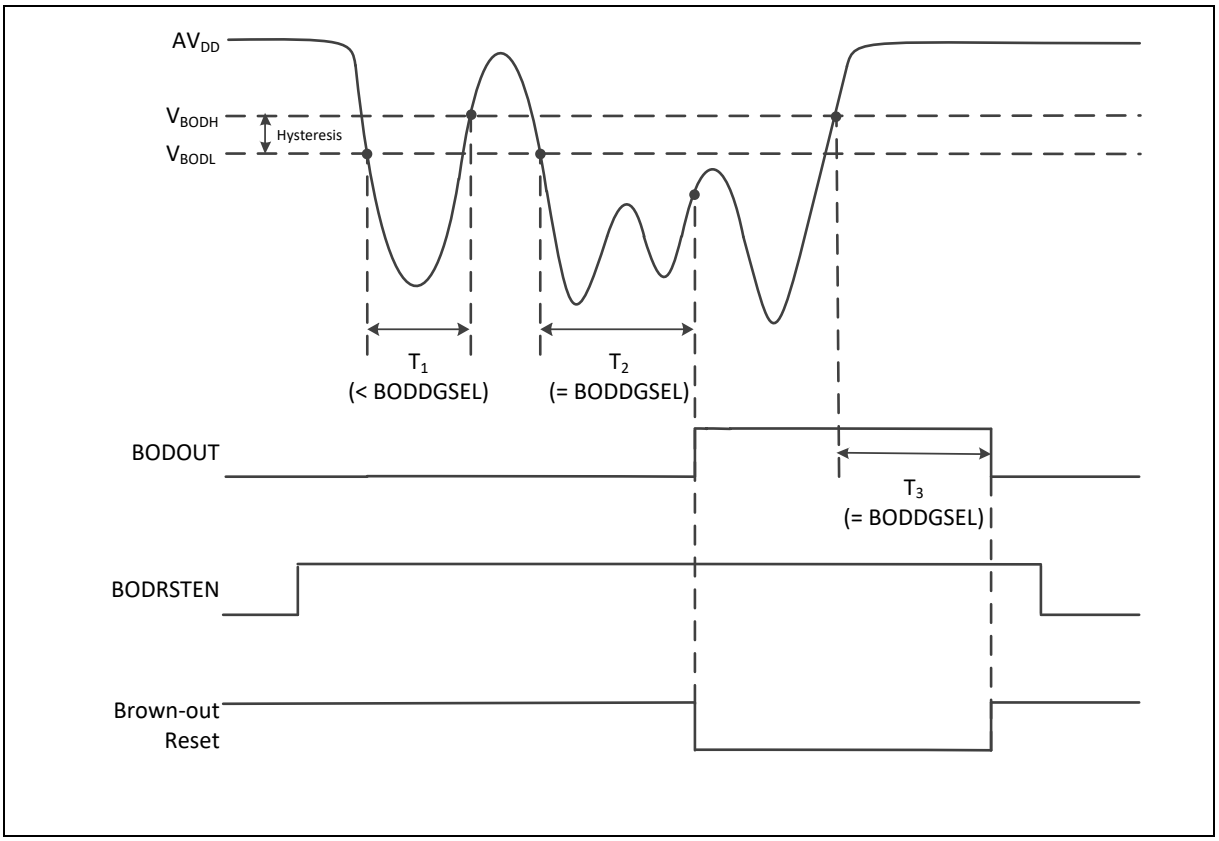


Figure 6.2-6 Brown-out Detector (BOD) Waveform

6.2.2.5 Watchdog Timer Reset (WDT)

In most industrial applications, system reliability is very important. To automatically recover the MCU from failure status is one way to improve system reliability. The watchdog timer(WDT) is widely used to check if the system works fine. If the MCU is crashed or out of control, it may cause the watchdog time-out. User may decide to enable system reset during watchdog time-out to recover the system and take action for the system crash/out-of-control after reset.

Software can check if the reset is caused by watchdog time-out to indicate the previous reset is a watchdog reset and handle the failure of MCU after watchdog time-out reset by checking WDTRF(SYS_RSTSTS[2]).

6.2.2.6 CPU Lockup Reset

CPU enters lockup status after CPU produces hardfault at hardfault handler and chip gives immediate indication of seriously errant kernel software. This is the result of the CPU being locked because of an unrecoverable exception following the activation of the processor's built in system state protection

hardware. When chip enters debug mode, the CPU lockup reset will be ignored.

6.2.2.7 CPU Reset, CHIP Reset and MCU Reset

The CPU Reset means only Cortex-M4 core is reset and all other peripherals remain the same status after CPU reset. User can set the CPURST(SYS_IPRST0[1]) to 1 to assert the CPU Reset signal.

The CHIP Reset is same with Power-on Reset. The CPU and all peripherals are reset and BS(FMC_ISPCTL[1]) bit is automatically reloaded from CONFIG0 setting. User can set the CHIPRST(SYS_IPRST0[1]) to 1 to assert the CHIP Reset signal.

The MCU Reset is similar with CHIP Reset. The difference is that BS(FMC_ISPCTL[1]) will not be reloaded from CONFIG0 setting and keep its original software setting for booting from APROM or LDROM. User can set the SYSRESETREQ(AIRCR[2]) to 1 to assert the MCU Reset.

6.2.3 System Power Distribution

In this chip, power distribution is divided into five segments:

- Analog power from AV_{DD} and AV_{SS} provides the power for analog components operation.
- Digital power from V_{DD} and V_{SS} supplies the power to the internal regulator which provides power levels(PL0/PL1) for digital operation and I/O pins.
- I/O power from V_{DDIO} supplies the power for PA.0 ~ PA.5
- USB 2.0 transceiver power from HSUSB_VDD33 offers the power for operating the USB transceiver.
- RTC power from V_{BAT} provides the power for RTC, backup registers and PF.4 ~ PF.11.

The outputs of internal voltage regulator, LDO_CAP, require an external capacitor which should be located close to the corresponding pin. Analog power (AV_{DD}) should be the same voltage level of the digital power (V_{DD}). Figure 6.2-8 shows the NuMicro M463/M467 series power distribution.

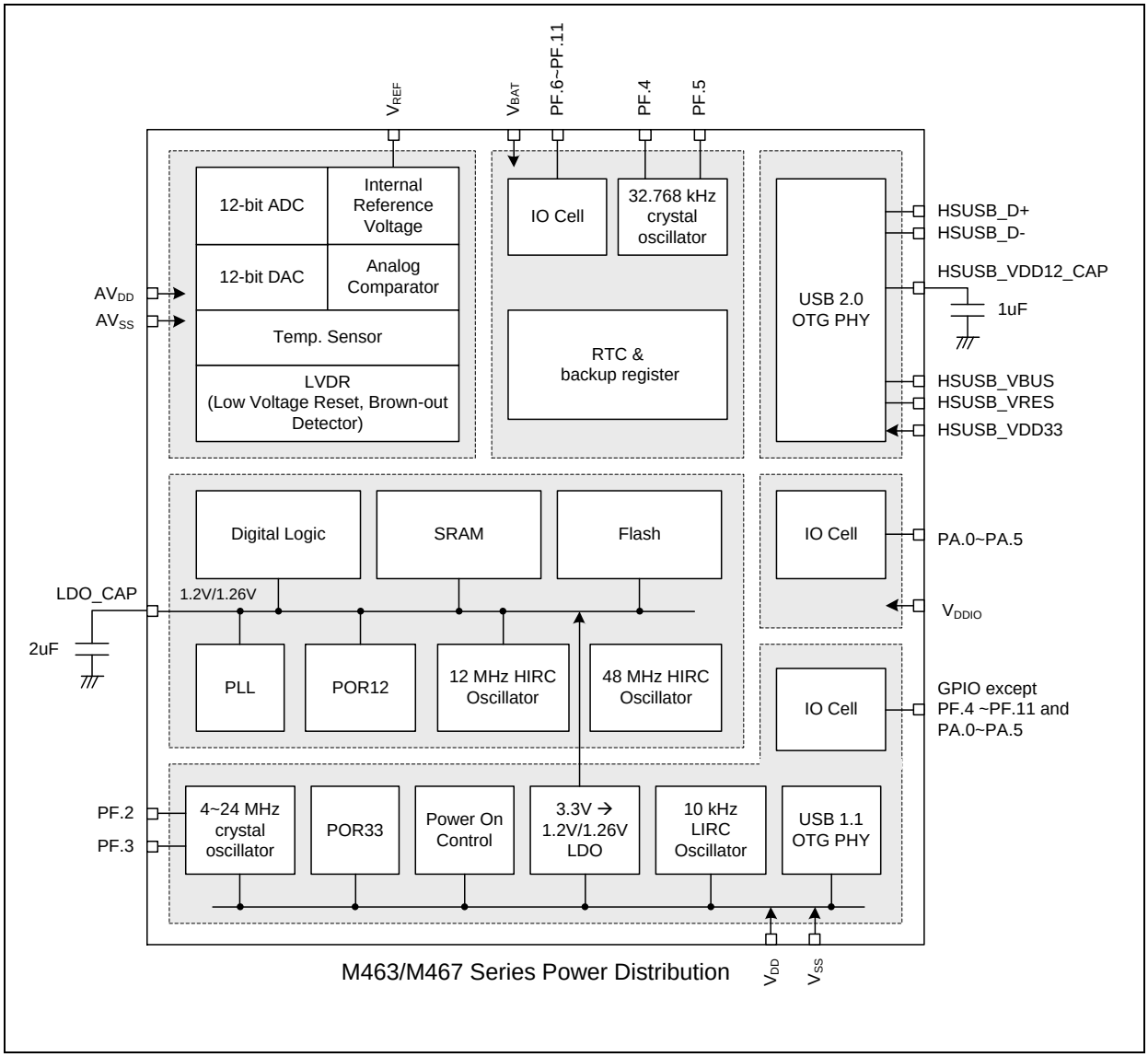


Figure 6.2-7 NuMicro M463/M467 Series Power Distribution Diagram

Note:

1. When VBAT power source first power-on, the power-on reset will happened and reset all VBAT domain circuit. The I/O in VBAT domain (PF.4 ~ PF.11) will become floating state and make additional leakage in VBAT domain. User should power on VDD first to reset chip and set I/O control to make these I/Os becomes a static state to prevent additional leakage.

6.2.4 Power Modes and Wake-up Sources

The NuMicro M463/M467 series has power manager unit to support several operating modes for saving power. Table 6.2-2 lists all power mode at NuMicro M463/M467 series.

Mode	CPU Operating and HCLK Maximum Speed (MHz)	APB and PCLK Maximum Speed (MHz)	LDO_CAP (V)	Clock Disable
Normal mode Power Level 1 (PL1)	180	90	1.20	All clocks are disabled by control register.

Turbo mode Power Level 0 (PL0)	200	100	1.26	All clocks are disabled by control register.
Idle mode	CPU enters Sleep mode	CPU enter Sleep mode	1.20/1.26	Only CPU clock is disabled.
Fast Wakeup Power-down mode (FWPD)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Normal Power-down mode (NPD)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	1.20/1.26	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Low leakage Power-down mode (LLPD)	CPU enters Deep Sleep mode	CPU enters Deep Sleep mode	0.9	Most clocks are disabled except LIRC/LXT, and only RTC/WDT/Timer/UART peripheral clocks still enable if their clock sources are selected as LIRC/LXT.
Standby Power-down mode (SPD)	Power off	Power off	Floating	Only LIRC still enable for wake-up timer usage. Only LXT still enabled for RTC function usage.
Deep Power-down mode (DPD)	Power off	Power off	Floating	Only LIRC still enabled for wake-up timer usage. Only LXT still enabled for RTC function usage.

Table 6.2-2 Power Mode Table

Note:

1. User must turn on LIRC before entering SPD mode.

There are different power mode entry setting for each power mode, with different entry setting and leaving condition. Table 6.2-3 shows the entry setting for each power mode. When chip power-on, chip is running at normal mode. User can enter each mode by setting SLEEPDEEP (SCR[2]), PDEN (CLK_PWRCTL[7]) and PDMSEL (CLK_PMUCTL[2:0]) and execute WFI instruction.

Register/Instruction Mode	SLEEPDEEP (SCR[2])	PDEN (CLK_PWRCTL[7])	PDMSEL (CLK_PMUCTL[2:0])	CPU Run WFI Instruction
Normal mode	0	0	0	NO
Idle mode	0	0	0	YES
Fast Wakeup Power-down mode	1	1	2	YES
Normal Power-down mode	1	1	0	YES
Low leakage Power-down mode	1	1	1	YES
Standby Power-down mode	1	1	4	YES
Deep Power-down mode	1	1	6	YES

Table 6.2-3 Power Mode Difference Table

There are several wake-up sources in Idle mode and Power-down mode.Table 6.2-4 lists the available clocks for each power mode.

Power Mode	Normal Mode	Idle Mode	Power-Down Mode
Definition	CPU is in active state	CPU is in sleep state	CPU is in sleep state and all

			clocks stop except LXT and LIRC. SRAM content retain.
Entry Condition	Chip is in normal mode after system reset released	CPU executes WFI instruction.	CPU sets sleep mode enable and power down enable and executes WFI instruction.
Wake-up Sources	N/A	All interrupts	RTC, WDT, I²C, Timer, UART, BOD, GPIO, INT, SDH, USCI, USBD, USBH, OTG, ACMP, EMAC, HSUSBD, HSUSBH and HSOTG.
Available Clocks	All	All except CPU clock	LXT and LIRC
After Wake-up	N/A	CPU back to normal mode	CPU back to normal mode

Table 6.2-4 Power Mode Definition Table

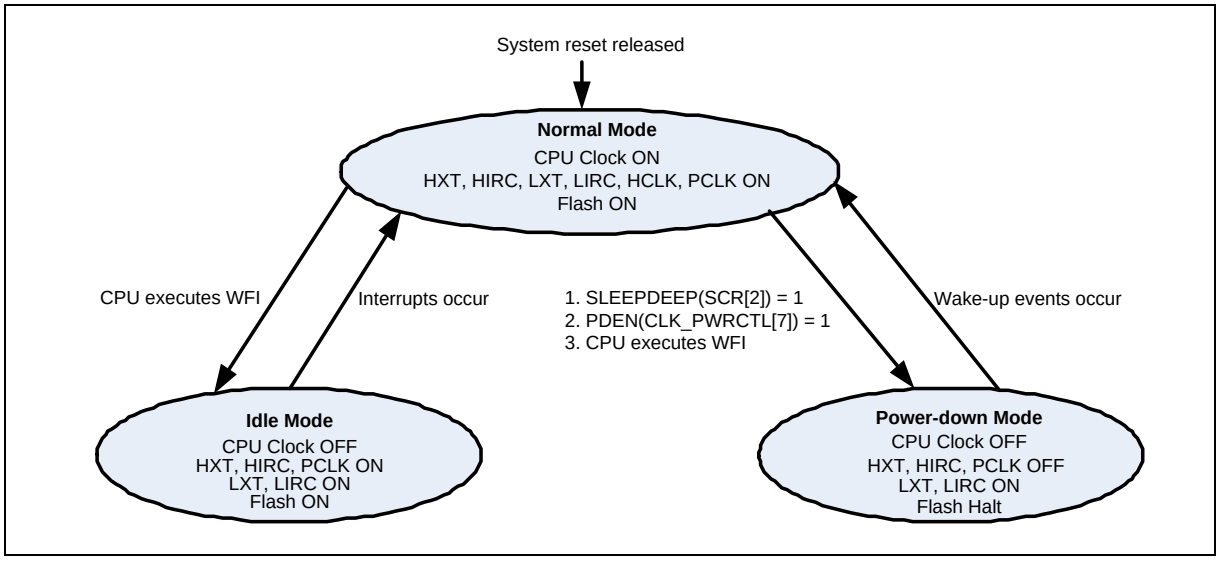


Figure 6.2-8 Power Mode State Machine

	Idle Mode	NPD, LLPD, FWPD	SPD	DPD
HXT	ON	Halt	Halt	Halt
HIRC	ON	Halt	Halt	Halt
LXT	ON	ON/OFF[1]	ON/OFF[1]	ON/OFF[1]
LIRC	ON	ON/OFF[2]	ON/OFF[2]	ON/OFF[2,8]
PLL	ON	Halt	Halt	Halt
HCLK/PCLK	ON	Halt	Halt	Halt
CPU	Halt	Halt	Halt	Halt
SRAM retention	ON	ON	ON/OFF[7]	Halt
FLASH	ON	Halt	Halt	Halt
TIMER	ON	ON/OFF[3]	Halt	Halt
WDT	ON	ON/OFF[4]	Halt	Halt
RTC	ON	ON/OFF[5]	ON/OFF[9]	ON/OFF[9]
UART	ON	ON/OFF[6]	Halt	Halt
Others	ON	Halt	Halt	Halt

Table 6.2-5 Clocks in Power Modes

Note:

1. LXT ON or OFF depends on software setting in normal mode.
2. LIRC ON or OFF depends on software setting in normal mode.
3. If TIMER clock source is selected as LIRC/LXT and LIRC/LXT is on.
4. If WDT clock source is selected as LIRC/LXT and LIRC/LXT is on.
5. If RTC clock source is selected as LIRC/LXT and LIRC/LXT is on.
6. If UART clock source is selected as LXT and LXT is on.
7. SRAM retention size depends on software setting in normal mode.
8. If timer wake-up function is disabled, LIRC will be disabled automatically when chip enters DPD mode for power saving.
9. If RTC clock source is selected as LXT and LXT is on.

Wake-up sources in Normal Power-down mode (NPD):

RTC, WDT, I²C, Timer, UART, USCI, BOD, GPIO, INT, SDH, USBD, USBH, OTG, ACMP, EMAC, HSUSBD, HSUSBH and HSOTG.

After chip enters power down, the following wake-up sources can wake chip up to normal mode. Table 6.2-6Table 6.2-6 lists the condition about how to enter Power-down mode again for each peripheral.

User needs to wait this condition before setting PDEN(CLK_PWRCTL[7]) and execute WFI to enter Power-down mode.

Wake-Up	Wake-Up Condition	Power-Down Mode	Re-Entering Power-Down Mode Condition

Source		NPD/ FWPD/ LLPD	SPD	DPD	
BOD	Brown-Out Detector Reset / Interrupt	V	-	-	After software writes 1 to clear BODIF (SYS_BODCTL[4]).
	Brown-Out Detector Reset	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear BODWK (CLK_PMUSTS[13]) when SPD mode is entered.
LVR	LVR Reset	V	-	-	After software writes 1 to clear LVRF (SYS_RSTSTS[3])
		-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear LVRWK (CLK_PMUSTS[12]) when SPD mode is entered.
POR	POR Reset	V	V	V	After software writes 1 to clear PORF (SYS_RSTSTS[0]).
RST pin	RST pin Reset	V	-	-	After software writes 1 to clear PINRF (SYS_RSTSTS[1]).
		-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RSTWK (CLK_PMUSTS[15]) when SPD or DPD mode is entered.
INT	External Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO	GPIO Interrupt	V	-	-	After software write 1 to clear the Px_INTSRC[n] bit.
GPIO(PA~PD) Wake-up pin	rising or falling edge event, 62-pin	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear GPxWK (CLK_PMUSTS[11:8]) when SPD mode is entered.
GPIO(PC.0/PB.0/PB.2/PB.12/PF.6) Wake-up pin	rising or falling edge event, 5-pin	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear PINWKx (CLK_PMUSTS[6:3] and CLK_PMUSTS[0]) when DPD mode is entered.
VBUS(PA.12)	rising or falling edge event	-	-	V	After software writes 1 (CLK_PMUSTS[31]) to clear VBUSWK (CLK_PMUSTS[7]) when DPD mode is entered.
TIMER	Timer Interrupt	V	-	-	After software writes 1 to clear TWKF (TIMERx_INTSTS[1]) and TIF (TIMERx_INTSTS[0]).
Wakeup timer	Wakeup by wake-up timer time-out	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear TMRWK (CLK_PMUSTS[1]) when SPD or DPD mode is entered.
WDT	WDT Interrupt	V	-	-	After software writes 1 to clear WKF (WDT_CTL[5]) (Write Protect).
RTC	Alarm Interrupt	V	-	-	After software writes 1 to clear ALMIF (RTC_INTSTS[0]).
	Time Tick Interrupt	V	-	-	After software writes 1 to clear TICKIF (RTC_INTSTS[1]).
	Wakeup by RTC alarm	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.
	Wakeup by RTC tick time	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.

	Wakeup by tamper event	-	V	V	After software writes 1 (CLK_PMUSTS[31]) to clear RTCWK (CLK_PMUSTS[2]) when DPD or SPD mode is entered.
UART	nCTS wake-up	V	-	-	After software writes 1 to clear CTSWKF (UARTx_WKSTS[0]).
	RX Data wake-up	V	-	-	After software writes 1 to clear DATWKF (UARTx_WKSTS[1]).
	Received FIFO Threshold Wake-up	V	-	-	After software writes 1 to clear RFRTWKF (UARTx_WKSTS[2]).
	RS-485 AAD Mode Wake-up	V	-	-	After software writes 1 to clear RS485WKF (UARTx_WKSTS[3]).
	Received FIFO Threshold Time-out Wake-up	V	-	-	After software writes 1 to clear TOUTWKF (UARTx_WKSTS[4]).
USCI UART	CTS Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
	Data Toggle	V	-	-	After software writes 1 to clear WKF (UUART_WKSTS[0]).
USCI I^2C	Data toggle	V	-	-	After software writes 1 to clear WKF (UI2C_WKSTS[0]).
	Address match	V	-	-	After software writes 1 to clear WKAKDONE (UI2C_PROTSTS[16], then writes 1 to clear WKF (UI2C_WKSTS[0]).
USCI SPI	SS Toggle	V	-	-	After software writes 1 to clear WKF (USPI_WKSTS[0]).
I^2C	Address match wake-up	V	-	-	After software writes 1 to clear WKAKDONE (I2C_WKSTS[1]). Then software writes 1 to clear WKIF(I2C_WKSTS[0]).
SDH	Card detection	V	-	-	Clear CDIF (SDH_INTSTS[8]) after SDH wake-up.
USBD	1.Remote Wake-up 2.Plug in wake-up	V	-	-	After software writes 1 to clear BUSIF (USBD_INTSTS[0]).
USBH	1.Connection detected 2.Disconnect detected 3.Remote-wakeup	V	-	-	1.After write 1 to clear RHSC (HcInterruptStatus[7]). 2.After write 1 to clear RHSC (HcInterruptStatus[7]). 3.After write 1 to clear RHSC (HcInterruptStatus[7]). and port suspended.
OTG	ID pin state be change	V	-	-	After software writes 1 to set WKEN(OTG_CTL[5]).
ACMP	Comparator Power-Down Wake-Up Interrupt	V	-	-	After software writes 1 to clear WKIF0 (ACMP_STATUS[8]), WKIF1 (ACMP_STATUS[9]), WKIF2 (ACMP_STATUS2[8]) and WKIF3 (ACMP_STATUS2[9]).
	ACMPO status change	-	V	-	After software writes 1 (CLK_PMUSTS[31]) to clear ACMPWKx (CLK_PMUSTS[19:16]) when SPD mode is entered.
EMAC	Magic Packet Detection	V	-	-	After software read to clear MGKPRCVD(PMT_Control_Status[5]), Magic Packet Received.
HSUSBD	1.V_{BUS} plug in/out 2.USB Resume/Reset	V	-	-	1. After software writes 1 to clear HSUSBD_BUSINTSTS[8](V_{BUS}) 2. After software writes 1 to clear HSUSBD_BUSINTSTS[2](Resume) or

					HSUSBD_BUSINTSTS[1](Reset)
HSUSBH	1. Remote-wakeup (while port in suspend state) 2. Connector plug-in detect 3. Connector plug-out detect (while port in suspend state) 4. Overcurrent detect	V	-	-	After software writes 1 to clear PCD (HSUSBH_USTSR[2])
HSOTG	ID pin state be change	V	-	-	After software writes 1 to set WKEN(HSOTG_CTL[5]).

Table 6.2-6 Re-Entering Power-down Mode Condition

6.2.5 Power Modes and Power Level Transition

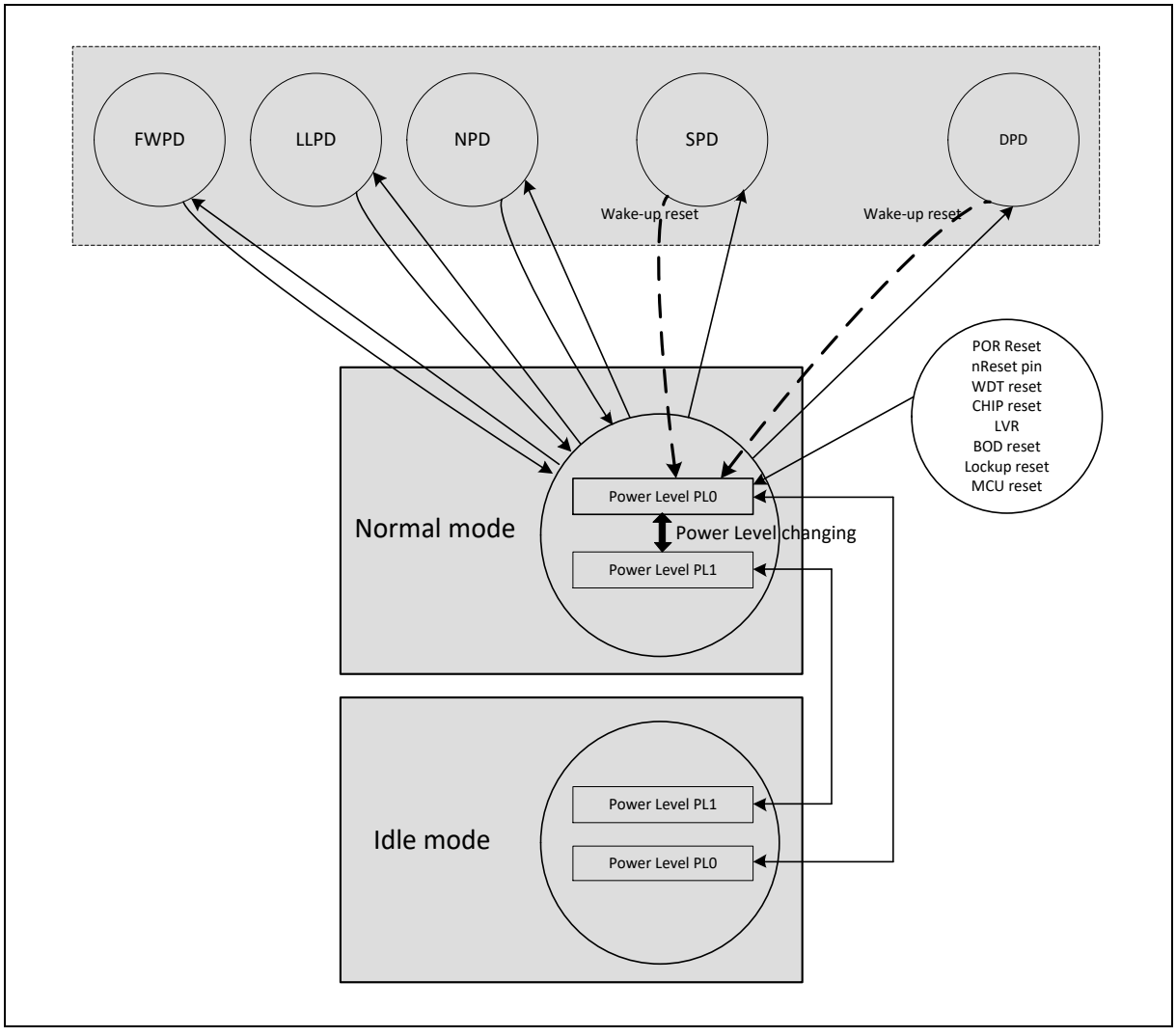


Figure 6.2-9 NuMicro M463/M467 Series Power Distribution Diagram

6.2.6 System Memory Map

The NuMicro M463/M467 series provides 4G-byte addressing space. The memory locations assigned to each on-chip controllers are shown in Table 6.2-7. The detailed register definition, memory space, and programming will be described in the following sections for each on-chip peripheral. The NuMicro M463/M467 series only supports little-endian data format.

Address Space	Token	Controllers
Flash and SRAM Memory Space		
0x0000_0000 – 0x000F_FFFF	FLASH_BA	FLASH APROM Memory Space (1024 Kbytes)
0x0010_0000 – 0x020F_FFFF	SPIM_BA	SPIM Memory Space (32 Mbytes) with FLASH 1024 Kbytes
0x0A00_0000 – 0x0BFF_FFFF	HRAM_BA	HyperRAM Memory Executable Space (32 Mbytes)
0x0F10_0000 – 0x0F10_1FFF	FLASH_BA	FLASH LDROM Memory Space (8 Kbytes)
0x1000_0000 – 0x1007_FFFF	SRAM_BA	SRAM Memory Space Remapping (512 Kbytes)
0x2000_0000 – 0x2007_FFFF	SRAM_BA	SRAM Memory Space (512 Kbytes)
0x6000_0000 – 0x602F_FFFF	EXTMEM_BA	External Memory Space (3 Mbytes)
0x8000_0000 – 0x81FF_FFFF	EXTHRAM_BA	External HyperRAM Memory Space (32 Mbytes)
Peripheral Controllers Space (0x4000_0000 – 0x400F_FFFF)		
0x4000_0000 – 0x4000_01FF	SYS_BA	System Control Registers
0x4000_0200 – 0x4000_02FF	CLK_BA	Clock Control Registers
0x4000_0300 – 0x4000_03FF	NMI_BA	NMI Control Registers
0x4000_4000 – 0x4000_4FFF	GPIO_BA	GPIO Control Registers
0x4000_7000 – 0x4000_7FFF	SPIM_BA	SPIM Control Registers
0x4000_8000 – 0x4000_8FFF	PDMA0_BA	Peripheral DMA0 Control Registers
0x4000_9000 – 0x4000_9FFF	USBH_BA	USB Host Control Registers
0x4000_C000 – 0x4000_CFFF	FMC_BA	Flash Memory Control Registers
0x4000_D000 – 0x4000_DFFF	SDH0_BA	SDHOST0 Control Registers
0x4000_E000 – 0x4000_EFFF	SDH1_BA	SDHOST1 Control Registers
0x4001_0000 – 0x4001_0FFF	EBI_BA	External Bus Interface Control Registers
0x4001_2000 – 0x4001_1FFF	EMAC0_BA	EMAC0 Control Registers
0x4001_8000 – 0x4001_8FFF	PDMA1_BA	Peripheral DMA1 Control Registers
0x4001_9000 – 0x4001_9FFF	HSUSBD_BA	HSUSBD Control Registers
0x4001_A000 – 0x4001_AFFF	HSUSBH _BA	HSUSBH Host Control Registers
0x4002_0000 – 0x4002_1FFF	CANFD0_BA	CANFD0 Control Registers
0x4002_4000 – 0x4002_5FFF	CANFD1_BA	CANFD1 Control Registers
0x4002_8000 – 0x4002_9FFF	CANFD2_BA	CANFD2 Control Registers
0x4002_C000 – 0x4002_DFFF	CANFD3_BA	CANFD3 Control Registers
0x4003_0000 – 0x4003_0FFF	CCAP_BA	CCAP Control Registers
0x4003_1000 – 0x4003_1FFF	CRC_BA	CRC Generator Registers

0x4003_2000 – 0x4003_4FFF	CRYPTO_BA	Cryptographic Accelerator Registers
0x4003_5000 – 0x4003_5FFF	KS_BA	Key Store Control Registers
APB Controllers Space (0x4000_0000 ~ 0x400F_FFFF)		
0x4004_0000 – 0x4004_00FF	WDT_BA	Watchdog Timer Control Registers
0x4004_0100 – 0x4004_0FFF	WWDT_BA	Window Watchdog Timer Control Registers
0x4004_1000 – 0x4004_1FFF	RTC_BA	Real Time Clock (RTC) Control Register
0x4004_3000 – 0x4004_3FFF	EADC0_BA	Enhanced Analog-Digital-Converter 0 (EADC0) Control Registers
0x4004_5000 – 0x4004_5FFF	ACMP01_BA	Analog Comparator 0/1 Control Registers
0x4004_7000 – 0x4004_7FFF	DAC_BA	DAC Control Registers
0x4004_8000 – 0x4004_8FFF	I2S0_BA	I2S0 Interface Control Registers
0x4004_9000 – 0x4004_9FFF	I2S1_BA	I2S1 Interface Control Registers
0x4004_B000 – 0x4004_BFFF	EADC1_BA	Enhanced Analog-Digital-Converter 1 (EADC1) Control Registers
0x4004_D000 – 0x4004_DFFF	OTG_BA	OTG Control Registers
0x4004_F000 – 0x4004_FFFF	HSOTG_BA	HSOTG Control Registers
0x4005_0000 – 0x4005_0FFF	TMR01_BA	Timer0/Timer1 Control Registers
0x4005_1000 – 0x4005_1FFF	TMR23_BA	Timer2/Timer3 Control Registers
0x4005_8000 – 0x4005_8FFF	EPWM0_BA	EPWM0 Control Registers
0x4005_9000 – 0x4005_9FFF	EPWM1_BA	EPWM1 Control Registers
0x4005_A000 – 0x4005_AFFF	BPWM0_BA	BPWM0 Control Registers
0x4005_B000 – 0x4005_BFFF	BPWM1_BA	BPWM1 Control Registers
0x4006_0000 – 0x4006_0FFF	QSPI0_BA	QSPI0 Control Registers
0x4006_1000 – 0x4006_1FFF	SPI0_BA	SPI0 Control Registers
0x4006_2000 – 0x4006_2FFF	SPI1_BA	SPI1 Control Registers
0x4006_3000 – 0x4006_3FFF	SPI2_BA	SPI2 Control Registers
0x4006_4000 – 0x4006_4FFF	SPI3_BA	SPI3 Control Registers
0x4006_5000 – 0x4006_5FFF	SPI4_BA	SPI4 Control Registers
0x4006_6000 – 0x4006_6FFF	SPI5_BA	SPI5 Control Registers
0x4006_7000 – 0x4006_7FFF	SPI6_BA	SPI6 Control Registers
0x4006_8000 – 0x4006_8FFF	SPI7_BA	SPI7 Control Registers
0x4006_9000 – 0x4006_9FFF	QSPI1_BA	QSPI1 Control Registers
0x4006_B000 – 0x4006_BFFF	SPI8_BA	SPI8 Control Registers
0x4006_C000 – 0x4006_CFFF	SPI9_BA	SPI9 Control Registers
0x4006_D000 – 0x4006_DFFF	SPI10_BA	SPI10 Control Registers
0x4007_0000 – 0x4007_0FFF	UART0_BA	UART0 Control Registers
0x4007_1000 – 0x4007_1FFF	UART1_BA	UART1 Control Registers

0x4007_2000 – 0x4007_2FFF	UART2_BA	UART2 Control Registers
0x4007_3000 – 0x4007_3FFF	UART3_BA	UART3 Control Registers
0x4007_4000 – 0x4007_4FFF	UART4_BA	UART4 Control Registers
0x4007_5000 – 0x4007_5FFF	UART5_BA	UART5 Control Registers
0x4007_6000 – 0x4007_6FFF	UART6_BA	UART6 Control Registers
0x4007_7000 – 0x4007_7FFF	UART7_BA	UART7 Control Registers
0x4007_8000 – 0x4007_8FFF	UART8_BA	UART8 Control Registers
0x4007_9000 – 0x4007_9FFF	UART9_BA	UART9 Control Registers
0x4008_0000 – 0x4008_0FFF	I2C0_BA	I2C0 Control Registers
0x4008_1000 – 0x4008_1FFF	I2C1_BA	I2C1 Control Registers
0x4008_2000 – 0x4008_2FFF	I2C2_BA	I2C2 Control Registers
0x4008_3000 – 0x4008_3FFF	I2C3_BA	I2C3 Control Registers
0x4008_4000 – 0x4008_4FFF	I2C4_BA	I2C4 Control Registers
0x4009_0000 – 0x4009_0FFF	SC0_BA	Smartcard Host 0 Control Registers
0x4009_1000 – 0x4009_1FFF	SC1_BA	Smartcard Host 1 Control Registers
0x4009_2000 – 0x4009_2FFF	SC2_BA	Smartcard Host 2 Control Registers
0x4009_7000 – 0x4009_7FFF	EADC2_BA	Enhanced Analog-Digital-Converter 2(EADC2) Control Registers
0x400B_0000 – 0x400B_0FFF	EQEI0_BA	EQEI0 Control Registers
0x400B_1000 – 0x400B_1FFF	EQEI1_BA	EQEI1 Control Registers
0x400B_2000 – 0x400B_2FFF	EQEI2_BA	EQEI2 Control Registers
0x400B_3000 – 0x400B_3FFF	EQEI3_BA	EQEI3 Control Registers
0x400B_4000 – 0x400B_4FFF	ECAP0_BA	ECAP0 Control Registers
0x400B_5000 – 0x400B_5FFF	ECAP1_BA	ECAP1 Control Registers
0x400B_6000 – 0x400B_6FFF	ECAP2_BA	ECAP2 Control Registers
0x400B_7000 – 0x400B_7FFF	ECAP3_BA	ECAP3 Control Registers
0x400B_9000 – 0x400B_9FFF	TRNG_BA	TRNG Control Registers
0x400C_0000 – 0x400C_0FFF	USBD_BA	USB Device Control Register
0x400C_2000 – 0x400C_2FFF	KPI_BA	Key Pad Control Register
0x400C_3000 – 0x400C_3FFF	PSIO_BA	PSIO Device Control Register
0x400C_9000 – 0x400C_9FFF	ACMP23_BA	Analog Comparator 2/3 Control Registers
0x400C_E000 – 0x400C_EFFF	HBI_BA	HBI Control Registers
0x400D_0000 – 0x400D_0FFF	USCI0_BA	USCI0 Control Registers
System Controllers Space (0xE000_E000 ~ 0xE000_EFFF)		
0xE000_E010 – 0xE000_E0FF	SCS_BA	System Timer Control Registers
0xE000_E100 – 0xE000_ECFF	SCS_BA	External Interrupt Controller Control Registers

0xE000_ED00 – 0xE000_ED8F	SCS_BA	System Control Registers

Table 6.2-7 Address Space Assignments for On-Chip Controllers

6.2.7 SRAM Memory Organization

The M463/M467 series supports embedded SRAM with total up to 512 Kbytes size and the SRAM organization is separated to three banks: SRAM bank0, SRAM bank1 and SRAM bank2. The first bank has 128 Kbytes address space, the second bank has 128 Kbyte address space and the third bank has 256 Kbyte address space. These three banks address space can be accessed simultaneously. The SRAM bank0 first 64 Kbyte supports parity error check at 512 Kbytes device and all 32 Kbytes at 128 Kbytes device to make sure chip operating more stable.

- Supports total up to 512 Kbytes SRAM
- Supports byte / half word / word write
- Supports parity error check function for SRAM bank0 first 64 Kbytes at 512 Kbytes device
- Supports parity error check function for SRAM bank0 all 32 Kbytes at 128 Kbytes device
- Supports oversize response error
- Supports remap address to 0x1000_0000

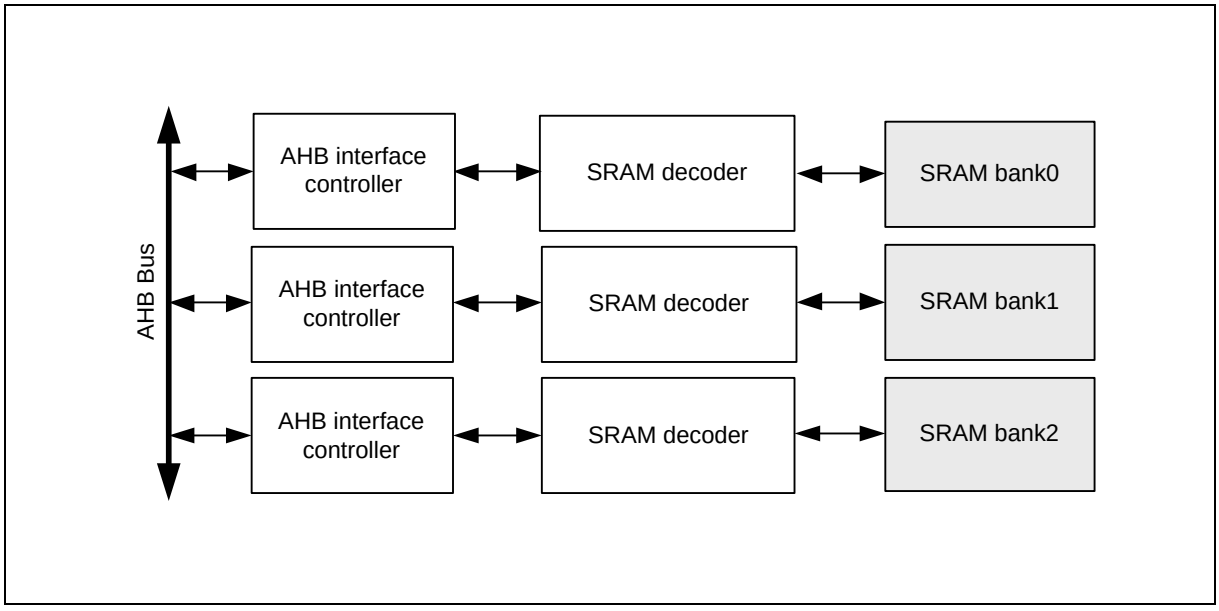


Figure 6.2-10 SRAM Block Diagram

Figure 6.2-11 shows the SRAM organization of M463/M467 series. There are three SRAM banks in M463/M467 series. The bank0 is addressed to 128 Kbytes, bank1 is addressed to 128 Kbytes and the bank2 is addressed to 256 Kbytes. The bank0 address space is from 0x2000_0000 to 0x2001_FFFF. The bank1 address space is from 0x2002_0000 to 0x2003_FFFF. The bank2 address space is from 0x2004_0000 to 0x2007_FFFF. The address between 0x2008_0000 to 0x3FFF_FFFF is illegal memory space and chip will enter hardfault if CPU accesses these illegal memory addresses.

The address of each bank is remapping from 0x2000_0000 to 0x1000_0000. CPU can access SRAM bank0 through 0x2000_0000 to 0x2001_FFFF or 0x1000_0000 to 0x1001_FFFF, and access SRAM bank1 through 0x2002_0000 to 0x2003_FFFF or 0x1002_0000 to 0x1003_FFFF and access SRAM bank2 through 0x2004_0000 to 0x2007_FFFF or 0x1004_0000 to 0x1007_FFFF.

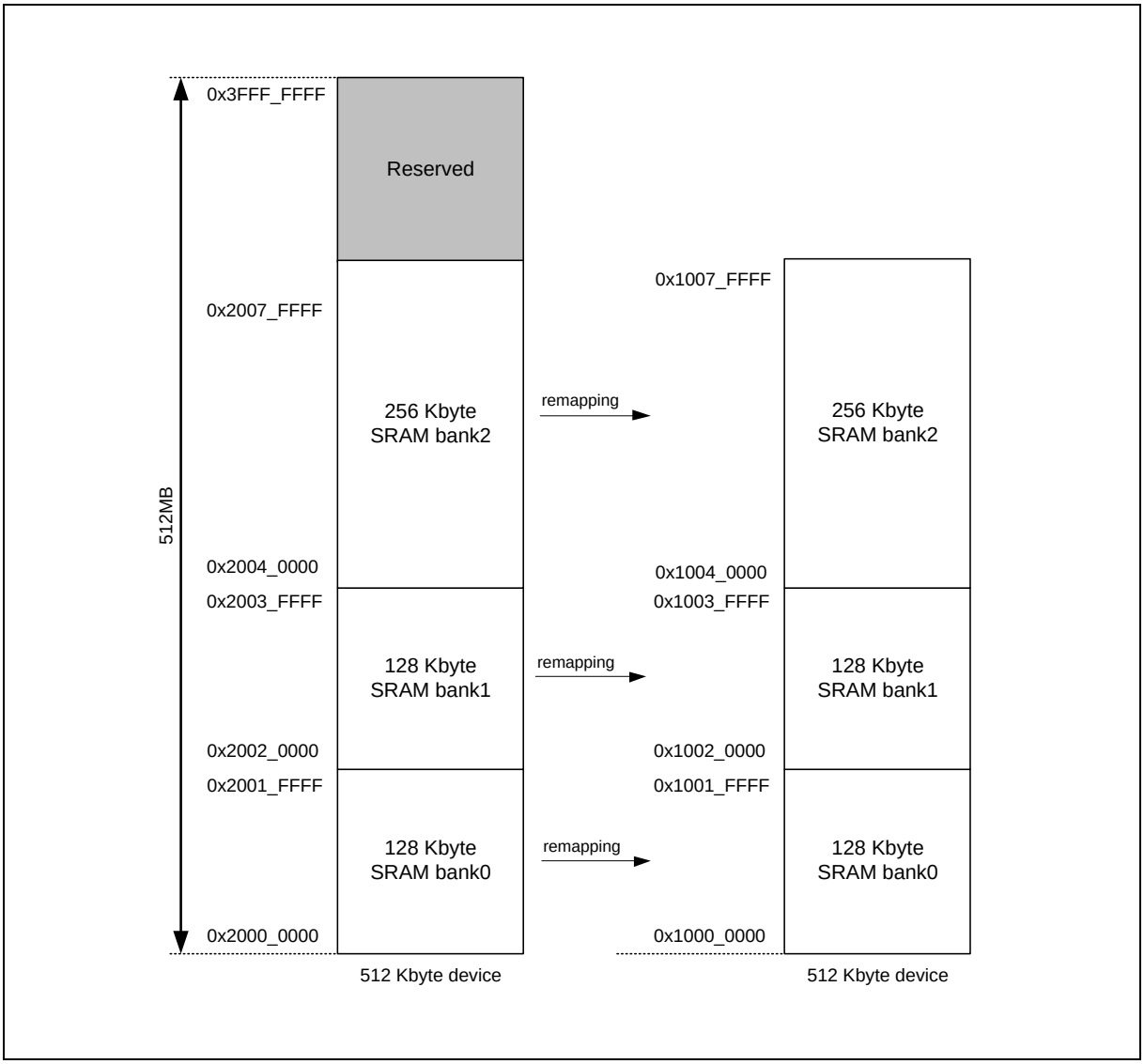


Figure 6.2-11 SRAM Memory Organization for 512 Kbyte Device

For 512 Kbytes device, SRAM bank0 first 64 Kbytes has byte parity error check function. When CPU is accessing the first 64 Kbytes of SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

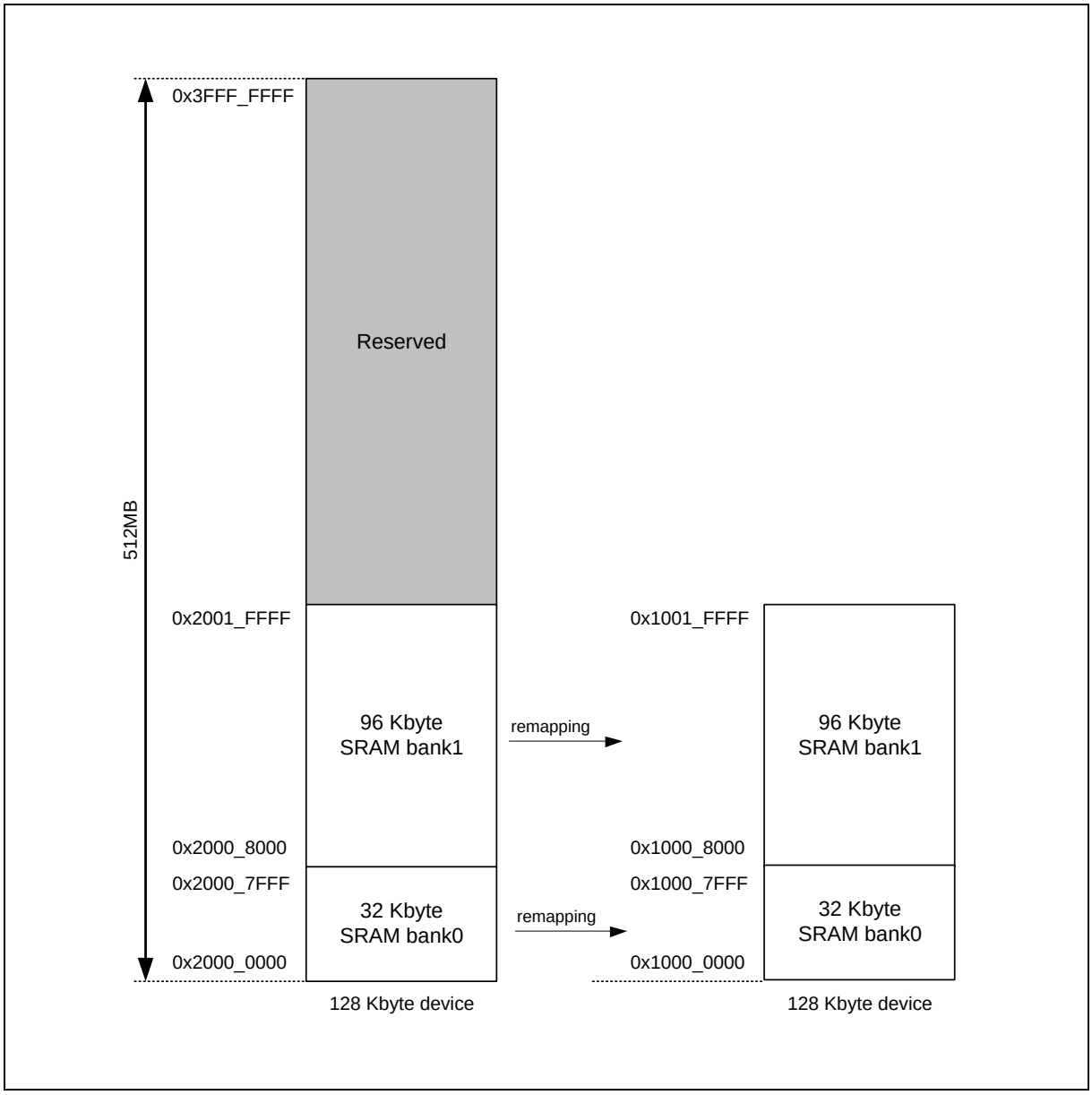


Figure 6.2-12 SRAM Memory Organization for 128 Kbyte Device

For 128 Kbytes device, SRAM bank0 all 32 Kbytes has byte parity error check function. When CPU is accessing 32 Kbytes of SRAM bank0, the parity error checking mechanism is dynamic operating. As parity error occurred, the PERRIF (SYS_SRAM_STATUS[0]) will be asserted to 1 and the SYS_SRAM_ERRADDR register will recode the address with parity error. Chip will enter interrupt when SRAM parity error occurred if PERRIEN (SYS_SRAM_INTCTL[0]) is set to 1. When SRAM parity error occurred, chip will stop detecting SRAM parity error until user writes 1 to clear the PERRIF(SYS_SRAM_STATUS[0]) bit.

6.2.8 Bus Matrix

The M463/M467 series supports Bus Matrix to manage the access arbitration between masters. The access arbitration can be selected by INTACTEN (SYS_AHBMCTL[0]) to use round-robin algorithm or set Cortex-M4 CPU as the highest bus priority.

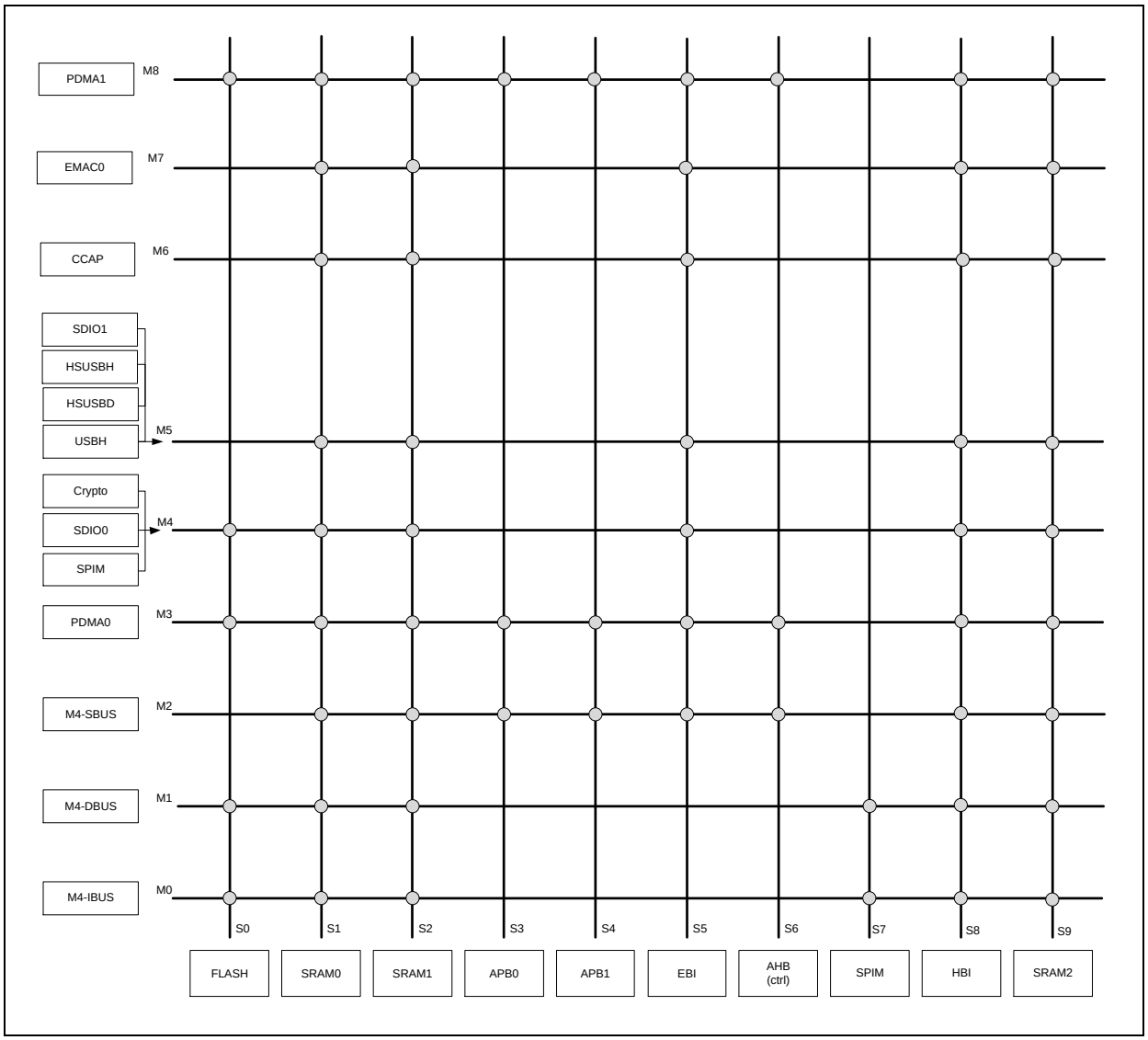


Figure 6.2-13 NuMicro M463/M467 Series Bus Matrix Diagram

6.2.9 HIRC Auto Trim

This chip supports auto-trim function: the HIRC trim (12 MHz RC oscillator) and HIRC48M trim (48 MHz RC oscillator), according to the accurate LXT (32.768 kHz crystal oscillator) or internal USB synchronous mode, automatically gets accurate HIRC output frequency, 0.25 % deviation within all temperature ranges.

For instance, the system needs an accurate 12 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_IRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_IRCTCTL[1:0] trim frequency selection) to “01”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_IRCTISTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

In HIRC48M case, the system needs an accurate 48 MHz clock. In such case, if neither using use PLL as the system clock source nor soldering 32.768 kHz crystal in system, user has to set REFCKSEL (SYS_HIRCTCTL[10] reference clock selection) to “1”, set FREQSEL (SYS_HIRCTCTL[1:0] trim frequency selection) to “10”, and the auto-trim function will be enabled. Interrupt status bit FREQLOCK (SYS_HIRCTSTS[8] HIRC frequency lock status) “1” indicates the HIRC output frequency is accurate within 0.25% deviation.

6.2.10 Register Lock Control

Some of the system control registers need to be protected to avoid inadvertent write and disturb the chip operation. These system control registers are protected after the power-on reset till user to disable register protection. For user to program these protected registers, a register protection disable sequence needs to be followed by a special programming. The register protection disable sequence is writing the data “59h”, “16h” “88h” to the register SYS_REGLCTL address at 0x4000_0100 continuously. Any different data value, different sequence or any other write to other address during these three data writing will abort the whole sequence.

SYS_IPRST0	**Address 0x4000_0008**
SYS_BODCTL	address 0x4000_0018
SYS_PORCTL	address 0x4000_0024
SYS_VREFCTL	address 0x4000_0028
SYS_USBPHY	address 0x4000_002C
SYS_SRAM_BISTCTL	address 0x4000_00D0
SYS_PORDISAN	address 0x4000_01EC
SYS_PLCTL	address 0x4000_01F8
CLK_PWRCTL	address 0x4000_0200
CLK_APBCLK0	address 0x4000_0208
CLK_CLKSEL0	address 0x4000_0210
CLK_CLKSEL1	address 0x4000_0214
CLK_PLLCTL	address 0x4000_0240
CLK_PLLFNCTL0	address 0x4000_0248
CLK_PLLFNCTL1	address 0x4000_024C
CLK_CLKDSTS	address 0x4000_0274
CLK_PMUCTL	address 0x4000_0290
NMIEN	address 0x4000_0300
AHBMCTL	address 0x4000_0400
FMC_ISPCTL	address 0x4000_C000
FMC_ISPTRG	address 0x4000_C010
FMC_ISPSTS	address 0x4000_C040
FMC_CYCCTL	address 0x4000_C04C
WDT_CTL	address 0x4004_0000
WDT_ALTCTL	address 0x4004_0004

TIMER0_CTL	address 0x4005_0000
TIMER1_CTL	address 0x4005_0100
TIMER2_CTL	address 0x4005_1000
TIMER3_CTL	address 0x4005_1100
TIMER0_PWMCTL	address 0x4005_0040
TIMER1_PWMCTL	address 0x4005_0140
TIMER2_PWMCTL	address 0x4005_1040
TIMER3_PWMCTL	address 0x4005_1140
TIMER0_PWMDTCTL	address 0x4005_0058
TIMER1_PWMDTCTL	address 0x4005_0158
TIMER2_PWMDTCTL	address 0x4005_1058
TIMER3_PWMDTCTL	address 0x4005_1158
TIMER0_PWMBRKCTL	address 0x4005_0070
TIMER1_PWMBRKCTL	address 0x4005_0170
TIMER2_PWMBRKCTL	address 0x4005_1070
TIMER3_PWMBRKCTL	address 0x4005_1170
TIMER0_PWMSWBRK	address 0x4005_007C
TIMER1_PWMSWBRK	address 0x4005_017C
TIMER2_PWMSWBRK	address 0x4005_107C
TIMER3_PWMSWBRK	address 0x4005_117C
TIMER0_PWMINTEN1	address 0x4005_0084
TIMER1_PWMINTEN1	address 0x4005_0184
TIMER2_PWMINTEN1	address 0x4005_1084
TIMER3_PWMINTEN1	address 0x4005_1184
TIMER0_PWMINTSTS1	address 0x4005_008C
TIMER1_PWMINTSTS1	address 0x4005_018C
TIMER2_PWMINTSTS1	address 0x4005_108C
TIMER3_PWMINTSTS1	address 0x4005_118C
EPWM_CTL0	address 0x4005_8000/0x4005_9000
EPWM_CTL1	address 0x4005_8000/0x4005_9000
EPWM_DTCTL0_1	address 0x4005_8070/0x4005_9070
EPWM_DTCTL2_3	address 0x4005_8074/0x4005_9074
EPWM_DTCTL4_5	address 0x4005_8078/0x4005_9078
EPWM_BRKCTL0_1	address 0x4005_80C8/0x4005_90C8
EPWM_BRKCTL2_3	address 0x4005_80CC/0x4005_90CC

EPWM_BRKCTL4_5	address 0x4005_80D0/0x4005_90D0
EPWM_SWBRK	address 0x4005_80DC/0x4005_90DC
EPWM_INTEN1	address 0x4005_80E4/0x4005_90E4
EPWM_INTSTS1	address 0x4005_80EC/0x4005_90EC
BPWM_CTL0	address 0x4005_A000/0x4005_B000

6.2.11 System Timer (SysTick)

The Cortex-M4 includes an integrated system timer, SysTick, which provides a simple, 24-bit clear-on-write, decrementing, wrap-on-zero counter with a flexible control mechanism. The counter can be used as a Real Time Operating System (RTOS) tick timer or as a simple counter.

When system timer is enabled, it will count down from the value in the SysTick Current Value Register (SYST_VAL) to zero, and reload (wrap) to the value in the SysTick Reload Value Register (SYST_LOAD) on the next clock cycle, and then decrement on subsequent clocks. When the counter transitions to zero, the COUNTFLAG status bit is set. The COUNTFLAG bit clears on reads.

The SYST_VAL value is UNKNOWN on reset. Software should write to the register to clear it to zero before enabling the feature. This ensures the timer will count from the SYST_LOAD value rather than an arbitrary value when it is enabled.

If the SYST_LOAD is zero, the timer will be maintained with a current value of zero after it is reloaded with this value. This mechanism can be used to disable the feature independently from the timer enable bit.

For more detailed information, please refer to the "*Arm Cortex-M4 Technical Reference Manual*" and "*Arm v7-M Architecture Reference Manual*".

6.2.12 Nested Vectored Interrupt Controller (NVIC)

The NVIC and the processor core interface are closely coupled to enable low latency interrupt processing and efficient processing of late arriving interrupts. The NVIC maintains knowledge of the stacked, or nested, interrupts to enable tail-chaining of interrupts. You can only fully access the NVIC from privileged mode, but you can cause interrupts to enter a pending state in user mode if you enable the Configuration and Control Register. Any other user mode access causes a bus fault. You can access all NVIC registers using byte, halfword, and word accesses unless otherwise stated. NVIC registers are located within the SCS (System Control Space). All NVIC registers and system debug registers are little-endian regardless of the endianness state of the processor.

The NVIC supports:

- An implementation-defined number of interrupts, in the range 1-240 interrupts.
- A programmable priority level of 0-15 for each interrupt; a higher level corresponds to a lower priority, so level 0 is the highest interrupt priority.
- Level and pulse detection of interrupt signals.
- Dynamic reprioritization of interrupts.
- Grouping of priority values into group priority and subpriority fields.
- Interrupt tail-chaining.
- An external Non Maskable Interrupt (NMI)
- WIC with Ultra-low Power Sleep mode support

The processor automatically stacks its state on exception entry and unstacks this state on exception exit, with no instruction overhead. This provides low latency exception handling.

6.2.12.1 Exception Model and System Interrupt Map

Table 6.2-9 lists the exception model supported by M463/M467 series. Software can set 16 levels of priority on some of these exceptions as well as on all interrupts. The highest user-configurable priority is denoted as “0x00” and the lowest priority is denoted as “0xF0” (The 4-LSB always 0). The default priority of all the user-configurable interrupts is “0x00”. Note that priority “0” is treated as the fourth priority on the system, after three system exceptions “Reset”, “NMI” and “Hard Fault”.

When any interrupts is accepted, the processor will automatically fetch the starting address of the interrupt service routine (ISR) from a vector table in memory. On system reset, the vector table is fixed at address 0x00000000. Privileged software can write to the VTOR to relocate the vector table start address to a different memory location, in the range 0x00000080 to 0x3FFFFF80,

The vector table contains the initialization value for the stack pointer on reset, and the entry point addresses for all exception handlers. The vector number on previous page defines the order of entries in the vector table associated with exception handler entry as illustrated in previous section.

Exception Type	Vector Number	Vector Address	Priority
Reset	1	0x00000004	-3
NMI	2	0x00000008	-2
Hard Fault	3	0x0000000C	-1
Memory Manager Fault	4	0x00000010	Configurable
Bus Fault	5	0x00000014	Configurable
Usage Fault	6	0x00000018	Configurable
Reserved	7 ~ 10		Reserved

SVCall	11	0x0000002C	Configurable
Debug Monitor	12	0x00000030	Configurable
Reserved	13		Reserved
PendSV	14	0x00000038	Configurable
SysTick	15	0x0000003C	Configurable
Interrupt (IRQ0 ~ IRQ127)	16 ~ 143	0x00000000 + (Vector Number)*4	Configurable

Table 6.2-8 Exception Model

Vector Number	Interrupt Number (Bit In Interrupt Registers)	Interrupt Name	Interrupt Description
0 ~ 15	-	-	System exceptions
16	0	BODOUT	Brown-out low voltage detected interrupt
17	1	IRC_INT	IRC TRIM interrupt
18	2	PWRWU_INT	Clock controller interrupt for chip wake-up from power-down state
19	3	SRAM_PERR	SRAM parity check error interrupt
20	4	CLKFAIL	Clock fail detected interrupt
21	5	FMC_ISP_INT	FMC ISP interrupt
22	6	RTC_INT	Real time clock interrupt
23	7	TAMPER_INT	Backup register tamper interrupt
24	8	WDT_INT	Watchdog Timer interrupt
25	9	WWDT_INT	Window Watchdog Timer interrupt
26	10	EINT0	External interrupt from INT0 pin
27	11	EINT1	External interrupt from INT1 pin
28	12	EINT2	External interrupt from INT2 pin
29	13	EINT3	External interrupt from INT3 pin
30	14	EINT4	External interrupt from INT4 pin
31	15	EINT5	External interrupt from INT5 pin
32	16	GPA_INT	External interrupt from PA[15:0] pin
33	17	GPB_INT	External interrupt from PB[15:0] pin
34	18	GPC_INT	External interrupt from PC[15:0] pin
35	19	GPD_INT	External interrupt from PD[15:0] pin
36	20	GPE_INT	External interrupt from PE[15:0] pin
37	21	GPF_INT	External interrupt from PF[15:0] pin
38	22	QSPI0_INT	QSPI0 interrupt

39	23	SPI0_INT	SPI0 interrupt
40	24	BRAKE0_INT	EPWM0 brake interrupt
41	25	EPWM0_P0_INT	EPWM0 pair 0 interrupt
42	26	EPWM0_P1_INT	EPWM0 pair 1 interrupt
43	27	EPWM0_P2_INT	EPWM0 pair 2 interrupt
44	28	BRAKE1_INT	EPWM1 brake interrupt
45	29	EPWM1_P0_INT	EPWM1 pair 0 interrupt
46	30	EPWM1_P1_INT	EPWM1 pair 1 interrupt
47	31	EPWM1_P2_INT	EPWM1 pair 2 interrupt
48	32	TMR0_INT	Timer 0 interrupt
49	33	TMR1_INT	Timer 1 interrupt
50	34	TMR2_INT	Timer 2 interrupt
51	35	TMR3_INT	Timer 3 interrupt
52	36	UART0_INT	UART0 interrupt
53	37	UART1_INT	UART1 interrupt
54	38	I2C0_INT	I2C0 interrupt
55	39	I2C1_INT	I2C1 interrupt
56	40	PDMA0_INT	PDMA0 interrupt
57	41	DAC_INT	DAC interrupt
58	42	EADC0_INT0	EADC0 interrupt source 0
59	43	EADC0_INT1	EADC0 interrupt source 1
60	44	ACMP01_INT	ACMP0 and ACMP1 interrupt
61	45	ACMP23_INT	ACMP2 and ACMP3 interrupt
62	46	EADC0_INT2	EADC0 interrupt source 2
63	47	EADC0_INT3	EADC0 interrupt source 3
64	48	UART2_INT	UART2 interrupt
65	49	UART3_INT	UART3 interrupt
66	50	QSPI1_INT	QSPI1 interrupt
67	51	SPI1_INT	SPI1 interrupt
68	52	SPI2_INT	SPI2 interrupt
69	53	USBD_INT	USB device interrupt
70	54	USBH_INT	USB host interrupt
71	55	USBOTG_INT	USB OTG interrupt
73	57	SPI5_INT	SPI5 interrupt
74	58	SC0_INT	Smart card host 0 interrupt

75	59	SC1_INT	Smart card host 1 interrupt
76	60	SC2_INT	Smart card host 2 interrupt
77	61	GPJ_INT	External interrupt from PJ[15:0] pin
78	62	SPI3_INT	SPI3 interrupt
79	63	SPI4_INT	SPI4 interrupt
80	64	SDHOST0_INT	SD host 0 interrupt
81	65	HSUSBD_INT	HSUSBD interrupt
82	66	EMAC0_INT	Ethernet MAC 0 interrupt
83	67	Reserved	Reserved
84	68	I2S0_INT	I2S0 interrupt
85	69	I2S1_INT	I2S1 interrupt
86	70	SPI6_INT	SPI6 interrupt
87	71	CRYPTO	Crypto interrupt
88	72	GPG_INT	External interrupt from PG[15:0] pin
89	73	EINT6	External interrupt from INT6 pin
90	74	UART4_INT	UART4 interrupt
91	75	UART5_INT	UART5 interrupt
92	76	USCI0_INT	USCI0 interrupt
93	77	SPI7_INT	SPI7 interrupt
94	78	BPWM0_INT	BPWM0 interrupt
95	79	BPWM1_INT	BPWM1 interrupt
96	80	SPIM_INT	SPI Master interrupt
97	81	CCAP_INT	CCAP interrupt
98	82	I2C2_INT	I2C2 interrupt
99	83	I2C3_INT	I2C3 interrupt
100	84	EQEI0_INT	EQEI0 interrupt
101	85	EQEI1_INT	EQEI1 interrupt
102	86	ECAP0_INT	ECAP0 interrupt
103	87	ECAP1_INT	ECAP1 interrupt
105	88	GPH_INT	External interrupt from PH[15:0] pin
105	89	EINT7	External interrupt from INT7 pin
106	90	SDHOST1_INT	SD host 1 interrupt
107	91	PSIO_INT	PSIO interrupt
108	92	HSUSBH_INT	HSUSBH interrupt
109	93	HSOTG_INT	HSOTG interrupt

110	94	ECAP2_INT	ECAP2 interrupt
111	95	ECAP3_INT	ECAP3 interrupt
112	96	KPI_INT	KPI interrupt
113	97	HBI_INT	HyperBus interface interrupt
114	98	PDMA1_INT	PDMA1 interrupt
115	99	UART8_INT	UART8 interrupt
116	100	UART9_INT	UART9 interrupt
117	101	TRNG_INT	TRNG interrupt
118	102	UART6_INT	UART6 interrupt
119	103	UART7_INT	UART7 interrupt
120	104	EADC1_INT0	EADC1 interrupt source 0
121	105	EADC1_INT1	EADC1 interrupt source 1
122	106	EADC1_INT2	EADC1 interrupt source 2
123	107	EADC1_INT3	EADC1 interrupt source 3
124	108	SPI8_INT	SPI8 interrupt
125	109	KS_INT	Key store interrupt
126	110	GPI_INT	External interrupt from PI[15:0] pin
127	111	SPI9_INT	SPI9 interrupt
128	112	CANFD0_INT0	CANFD0 interrupt source 0
129	113	CANFD0_INT1	CANFD0 interrupt source 1
130	114	CANFD1_INT0	CANFD1 interrupt source 0
131	115	CANFD1_INT1	CANFD1 interrupt source 1
132	116	EQEI2_INT	EQEI2 interrupt
133	117	EQEI3_INT	EQEI3 interrupt
134	118	I2C4_INT	I2C4 interrupt
135	119	SPI10_INT	SPI10 interrupt
136	120	CANFD2_INT0	CANFD2 interrupt source 0
137	121	CANFD2_INT1	CANFD2 interrupt source 1
138	122	CANFD3_INT0	CANFD3 interrupt source 0
139	123	CANFD3_INT1	CANFD3 interrupt source 1
140	124	EADC2_INT0	EADC2 interrupt source 0
141	125	EADC2_INT1	EADC2 interrupt source 1
142	126	EADC2_INT2	EADC2 interrupt source 2
143	127	EADC2_INT3	EADC2 interrupt source 3

Table 6.2-9 Interrupt Number Table

6.2.12.2 Operation Description

NVIC interrupts can be enabled and disabled by writing to their corresponding Interrupt Set-Enable or Interrupt Clear-Enable register bit-field. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current enabled state of the corresponding interrupts. When an interrupt is disabled, interrupt assertion will cause the interrupt to become Pending, however, the interrupt will not activate. If an interrupt is Active when it is disabled, it remains in its Active state until cleared by reset or an exception return. Clearing the enable bit prevents new activations of the associated interrupt.

NVIC interrupts can be pended/un-pended using a complementary pair of registers to those used to enable/disable the interrupts, named the Set-Pending Register and Clear-Pending Register respectively. The registers use a write-1-to-enable and write-1-to-clear policy, both registers reading back the current pended state of the corresponding interrupts. The Clear-Pending Register has no effect on the execution status of an Active interrupt.

NVIC interrupts are prioritized by updating an 8-bit field within a 32-bit register (each register supporting four interrupts).

The general registers associated with the NVIC are all accessible from a block of memory in the System Control Space and will be described in next section.

6.2.12.3 NVIC Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NVIC Base Address: **NVIC_BA = 0xE000_E100**				
NVIC_ISER0	NVIC_BA+0x00	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000
NVIC_ISER1	NVIC_BA+0x04	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000
NVIC_ISER2	NVIC_BA+0x08	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000
NVIC_ISER3	NVIC_BA+0x0C	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000
NVIC_ICER0	NVIC_BA+0x80	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000
NVIC_ICER1	NVIC_BA+0x84	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000
NVIC_ICER2	NVIC_BA+0x88	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000
NVIC_ICER3	NVIC_BA+0x8C	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000
NVIC_ISPR2	NVIC_BA+0x108	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000
NVIC_ISPR3	NVIC_BA+0x10C	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000
NVIC_ICPR2	NVIC_BA+0x188	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000
NVIC_ICPR3	NVIC_BA+0x18C	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000
NVIC_IABR2	NVIC_BA+0x208	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000
NVIC_IABR3	NVIC_BA+0x20C	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000
NVIC_IPRn **n=0,1..31**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ127 Priority Control Register	0x0000_0000
STIR	NVIC_BA+0xE00	W	Software Trigger Interrupt Registers	0x0000_0000

IRQ0 ~ IRQ127 Set-enable Control Register (NVIC_ISER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER0	NVIC_BA+0x00	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Set-enable Control Register (NVIC_ISER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER1	NVIC_BA+0x04	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Set-enable Control Register (NVIC_ISER2)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER2	NVIC_BA+0x08	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Set-enable Control Register (NVIC_ISER3)

Register	Offset	R/W	Description	Reset Value
NVIC_ISER3	NVIC_BA+0x0C	R/W	IRQ0 ~ IRQ127 Set-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETENA							

Bits	Description	
[31:0]	**SETENA**	**Interrupt Set Enable Bit** The NVIC_ISER0-NVIC_ISER3 registers enable interrupts, and show which interrupts are enabled Write Operation: 0 = No effect. 1 = Interrupt Enabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Clear-enable Control Register (NVIC_ICER0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER0	NVIC_BA+0x80	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Clear-enable Control Register (NVIC_ICER1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER1	NVIC_BA+0x84	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Clear-enable Control Register (NVIC_ICER2)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER2	NVIC_BA+0x88	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Clear-enable Control Register (NVIC_ICER3)

Register	Offset	R/W	Description	Reset Value
NVIC_ICER3	NVIC_BA+0x8C	R/W	IRQ0 ~ IRQ127 Clear-enable Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALENA							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALENA							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALENA							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALENA							

Bits	Description	
[31:0]	**CALENA**	**Interrupt Clear Enable Bit** The NVIC_ICER0-NVIC_ICER3 registers disable interrupts, and show which interrupts are enabled. Write Operation: 0 = No effect. 1 = Interrupt Disabled. Read Operation: 0 = Interrupt Disabled. 1 = Interrupt Enabled.

IRQ0 ~ IRQ127 Set-pending Control Register (NVIC_ISPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR0	NVIC_BA+0x100	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Set-pending Control Register (NVIC_ISPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR1	NVIC_BA+0x104	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Set-pending Control Register (NVIC_ISPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR2	NVIC_BA+0x108	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Set-pending Control Register (NVIC_ISPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_ISPR3	NVIC_BA+0x10C	R/W	IRQ0 ~ IRQ127 Set-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
SETPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
SETPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
SETPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
SETPEND							

Bits	Description	
[31:0]	**SETPEND**	**Interrupt Set-pending** The NVIC_ISPR0-NVIC_ISPR3 registers force interrupts into the pending state, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Changes interrupt state to pending. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Clear-pending Control Register (NVIC_ICPR0)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR0	NVIC_BA+0x180	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Clear-pending Control Register (NVIC_ICPR1)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR1	NVIC_BA+0x184	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Clear-pending Control Register (NVIC_ICPR2)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR2	NVIC_BA+0x188	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Clear-pending Control Register (NVIC_ICPR3)

Register	Offset	R/W	Description	Reset Value
NVIC_ICPR3	NVIC_BA+0x18C	R/W	IRQ0 ~ IRQ127 Clear-pending Control Register	0x0000_0000

31	30	29	28	27	26	25	24
CALPEND							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
CALPEND							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
CALPEND							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
CALPEND							

Bits	Description	
[31:0]	**CALPEND**	**Interrupt Clear-pending** The NVIC_ICPR0-NVIC_ICPR3 registers remove the pending state from interrupts, and show which interrupts are pending. Write Operation: 0 = No effect. 1 = Removes pending state an interrupt. Read Operation: 0 = Interrupt is not pending. 1 = Interrupt is pending.

IRQ0 ~ IRQ127 Active Bit Register (NVIC_IABR0)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR0	NVIC_BA+0x200	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ127 Active Bit Register (NVIC_IABR1)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR1	NVIC_BA+0x204	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ127 Active Bit Register (NVIC_IABR2)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR2	NVIC_BA+0x208	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ127 Active Bit Register (NVIC_IABR3)

Register	Offset	R/W	Description	Reset Value
NVIC_IABR3	NVIC_BA+0x20C	R/W	IRQ0 ~ IRQ127 Active Bit Register	0x0000_0000

31	30	29	28	27	26	25	24
ACTIVE							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
ACTIVE							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
ACTIVE							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
ACTIVE							

Bits	Description	
[31:0]	**ACTIVE**	**Interrupt Active Flags** The NVIC_IABR0-NVIC_IABR3 registers indicate which interrupts are active. 0 = Interrupt not active. 1 = Interrupt active.

IRQ0 ~ IRQ127 Interrupt Priority Register (NVIC_IPRn)

Register	Offset	R/W	Description	Reset Value
NVIC_IPRn **n=0,1..31**	NVIC_BA+0x300 +0x4*n	R/W	IRQ0 ~ IRQ127 Priority Control Register	0x0000_0000

31	30	29	28	27	26	25	24
PRI_4n_3				Reserved			
23	22	21	20	19	18	17	16
PRI_4n_2				Reserved			
15	14	13	12	11	10	9	8
PRI_4n_1				Reserved			
7	6	5	4	3	2	1	0
PRI_4n_0				Reserved			

Bits	Description	
[31:28]	**PRI_4n_3**	**Priority of IRQ_4n+3** “0” denotes the highest priority and “15” denotes the lowest priority
[27:24]	**Reserved**	Reserved.
[23:20]	**PRI_4n_2**	**Priority of IRQ_4n+2** “0” denotes the highest priority and “15” denotes the lowest priority
[19:16]	**Reserved**	Reserved.
[15:12]	**PRI_4n_1**	**Priority of IRQ_4n+1** “0” denotes the highest priority and “15” denotes the lowest priority
[11:8]	**Reserved**	Reserved.
[7:4]	**PRI_4n_0**	**Priority of IRQ_4n+0** “0” denotes the highest priority and “15” denotes the lowest priority
[3:0]	**Reserved**	Reserved.

Software Trigger Interrupt Register (STIR)

Register	Offset	R/W	Description	Reset Value
STIR	NVIC_BA+0xE00	W	Software Trigger Interrupt Registers	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Reserved							**INTID**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INTID							

Bits	Description	
[31:9]	**Reserved**	Reserved.
[8:0]	**INTID**	**Interrupt ID (Write Only)** Write to the STIR To Generate An Interrupt from Software When the USERSETMPEND bit in the CCR is set to 1, unprivileged software can access the STIR. Number of valid Interrupt ID refers Table 6.2-10. For example, a value of 0x03 specifies interrupt IRQ3.

6.2.12.4 NMI Control Registers

R: read only, **W:** write only, **R/W:** both read and write

Register	Offset	R/W	Description	Reset Value
NMI Base Address: **NMI_BA = 0x4000_0300**				
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

NMI Source Interrupt Enable Register (NMIEN)

Register	Offset	R/W	Description	Reset Value
NMIEN	NMI_BA+0x00	R/W	NMI Source Interrupt Enable Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	**22**	**21**	**20**	**19**	**18**	**17**	**16**
Reserved							
15	**14**	**13**	**12**	**11**	**10**	**9**	**8**
UART1INT	**UART0INT**	**EINT5**	**EINT4**	**EINT3**	**EINT2**	**EINT1**	**EINT0**
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
TAMPERINT	**RTCINT**	**Reserved**	**CLKFAIL**	**SRAMPERR**	**PWRWUINT**	**IRCINT**	**BODOUT**

Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1INT**	**UART1 NMI Source Enable (Write Protect)** 0 = UART1 NMI source Disabled. 1 = UART1 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[14]	**UART0INT**	**UART0 NMI Source Enable (Write Protect)** 0 = UART0 NMI source Disabled. 1 = UART0 NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[13]	**EINT5**	**External Interrupt from INT5 Pins NMI Source Enable (Write Protect)** 0 = External interrupt from INT5 pins NMI source Disabled. 1 = External interrupt from INT5 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[12]	**EINT4**	**External Interrupt from INT4 Pins NMI Source Enable (Write Protect)** 0 = External interrupt from INT4 pins NMI source Disabled. 1 = External interrupt from INT4 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[11]	**EINT3**	**External Interrupt from INT3 Pins NMI Source Enable (Write Protect)** 0 = External interrupt from INT3 pins NMI source Disabled. 1 = External interrupt from INT3 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[10]	**EINT2**	**External Interrupt from INT2 Pins NMI Source Enable (Write Protect)** 0 = External interrupt from INT2 pins NMI source Disabled. 1 = External interrupt from INT2 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[9]	**EINT1**	**External Interrupt from INT1 Pins NMI Source Enable (Write Protect)**

		0 = External interrupt from INT1 pins NMI source Disabled. 1 = External interrupt from INT1 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[8]	**EINT0**	**External Interrupt from INT0 Pins NMI Source Enable (Write Protect)** 0 = External interrupt from INT0 pins NMI source Disabled. 1 = External interrupt from INT0 pins NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[7]	**TAMPERINT**	**TAMPER NMI Source Enable (Write Protect)** 0 = Backup register tamper detected interrupt.NMI source Disabled. 1 = Backup register tamper detected interrupt.NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[6]	**RTCINT**	**RTC NMI Source Enable (Write Protect)** 0 = RTC NMI source Disabled. 1 = RTC NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected NMI Source Enable (Write Protect)** 0 = Clock fail detected interrupt NMI source Disabled. 1 = Clock fail detected interrupt NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[3]	**SRAMPERR**	**SRAM Parity Check Error NMI Source Enable (Write Protect)** 0 = SRAM parity check error NMI source Disabled. 1 = SRAM parity check error NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[2]	**PWRWUINT**	**Power-down Mode Wake-up NMI Source Enable (Write Protect)** 0 = Power-down mode wake-up NMI source Disabled. 1 = Power-down mode wake-up NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[1]	**IRCINT**	**IRC TRIM NMI Source Enable (Write Protect)** 0 = IRC TRIM NMI source Disabled. 1 = IRC TRIM NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.
[0]	**BODOUT**	**BOD NMI Source Enable (Write Protect)** 0 = BOD NMI source Disabled. 1 = BOD NMI source Enabled. **Note:** This bit is write protected. Refer to the SYS_REGLCTL register.

NMI Source Interrupt Status Register (NMISTS)

Register	Offset	R/W	Description	Reset Value
NMISTS	NMI_BA+0x04	R	NMI Source Interrupt Status Register	0x0000_0000

31	30	29	28	27	26	25	24
Reserved							
23	22	21	20	19	18	17	16
Reserved							
15	14	13	12	11	10	9	8
UART1INT	UART0INT	EINT5	EINT4	EINT3	EINT2	EINT1	EINT0
7	6	5	4	3	2	1	0
TAMPERINT	RTCINT	Reserved	CLKFAIL	SRAMPERR	PWRWUINT	IRCINT	BODOUT

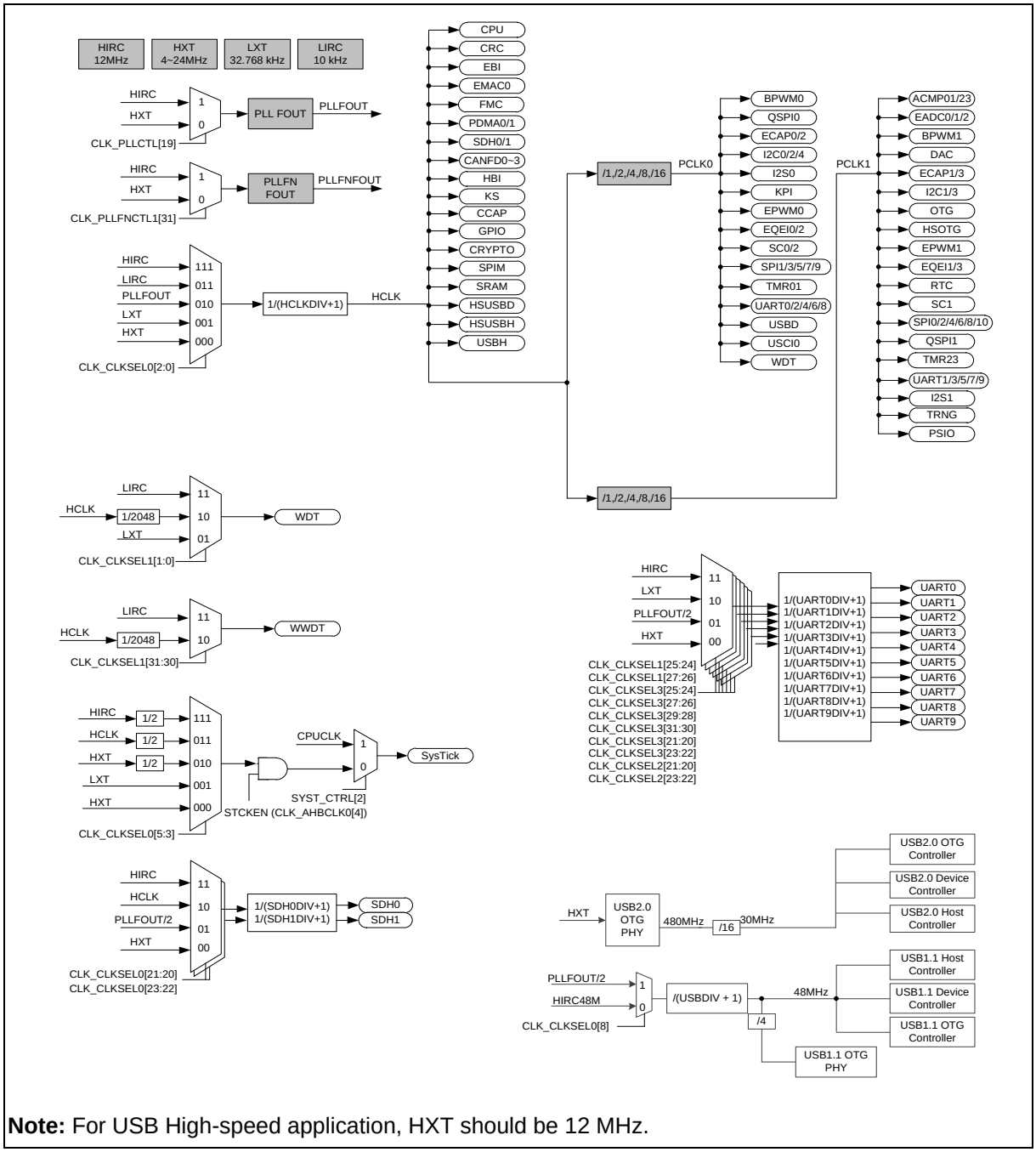
Bits	Description	
[31:16]	**Reserved**	Reserved.
[15]	**UART1_INT**	**UART1 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[14]	**UART0_INT**	**UART0 Interrupt Flag (Read Only)** 0 = UART1 interrupt is deasserted. 1 = UART1 interrupt is asserted.
[13]	**EINT5**	**External Interrupt from INT5 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from INT5 interrupt is deasserted. 1 = External Interrupt from INT5 interrupt is asserted.
[12]	**EINT4**	**External Interrupt from INT4 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from INT4 interrupt is deasserted. 1 = External Interrupt from INT4 interrupt is asserted.
[11]	**EINT3**	**External Interrupt from INT3 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from PD.0 interrupt is deasserted. 1 = External Interrupt from PD.0 interrupt is asserted.
[10]	**EINT2**	**External Interrupt from INT2 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from INT2 interrupt is deasserted. 1 = External Interrupt from INT2 interrupt is asserted.
[9]	**EINT1**	**External Interrupt from INT1 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from INT1 interrupt is deasserted. 1 = External Interrupt from INT1 interrupt is asserted.
[8]	**EINT0**	**External Interrupt from INT0 Pins Interrupt Flag (Read Only)** 0 = External Interrupt from INT0 interrupt is deasserted. 1 = External Interrupt from INT0 interrupt is asserted.
[7]	**TAMPERINT**	**TAMPER Interrupt Flag (Read Only)**

		0 = Backup register tamper detected interrupt is deasserted. 1 = Backup register tamper detected interrupt is asserted.
[6]	**RTCINT**	**RTC Interrupt Flag (Read Only)** 0 = RTC interrupt is deasserted. 1 = RTC interrupt is asserted.
[5]	**Reserved**	Reserved.
[4]	**CLKFAIL**	**Clock Fail Detected Interrupt Flag (Read Only)** 0 = Clock fail detected interrupt is deasserted. 1 = Clock fail detected interrupt is asserted.
[3]	**SRAMPERR**	**SRAM Parity Check Error Interrupt Flag (Read Only)** 0 = SRAM parity check error interrupt is deasserted. 1 = SRAM parity check error interrupt is asserted.
[2]	**PWRWUINT**	**Power-down Mode Wake-up Interrupt Flag (Read Only)** 0 = Power-down mode wake-up interrupt is deasserted. 1 = Power-down mode wake-up interrupt is asserted.
[1]	**IRCINT**	**IRC TRIM Interrupt Flag (Read Only)** 0 = IRC TRIM interrupt is deasserted. 1 = IRC TRIM interrupt is asserted.
[0]	**BODOUT**	**BOD Interrupt Flag (Read Only)** 0 = BOD interrupt is deasserted. 1 = BOD interrupt is asserted.

6.3 Clock Controller

6.3.1 Overview

The clock controller generates clocks for the whole chip, including system clocks and all peripheral clocks. The clock controller also implements the power control function with the individually clock ON/OFF control, clock source selection and a clock divider. The chip will not enter Power-down mode until CPU sets the Power-down enable bit PDEN(CLK_PWRCTL[7]) and Cortex-M4 core executes the WFI instruction. After that, chip enters Power-down mode and wait for wake-up interrupt source triggered to leave Power-down mode. In Power-down mode, the clock controller turns off the 4~24 MHz external high speed crystal (HXT), 12 MHz internal high speed RC oscillator (HIRC) and PLL to reduce the overall system power consumption. Figure 6.3-1 shows the clock generator and the overview of the clock source control.



Note: For USB High-speed application, HXT should be 12 MHz.

Figure 6.3-1 Clock Generator Global View Diagram (1/3)

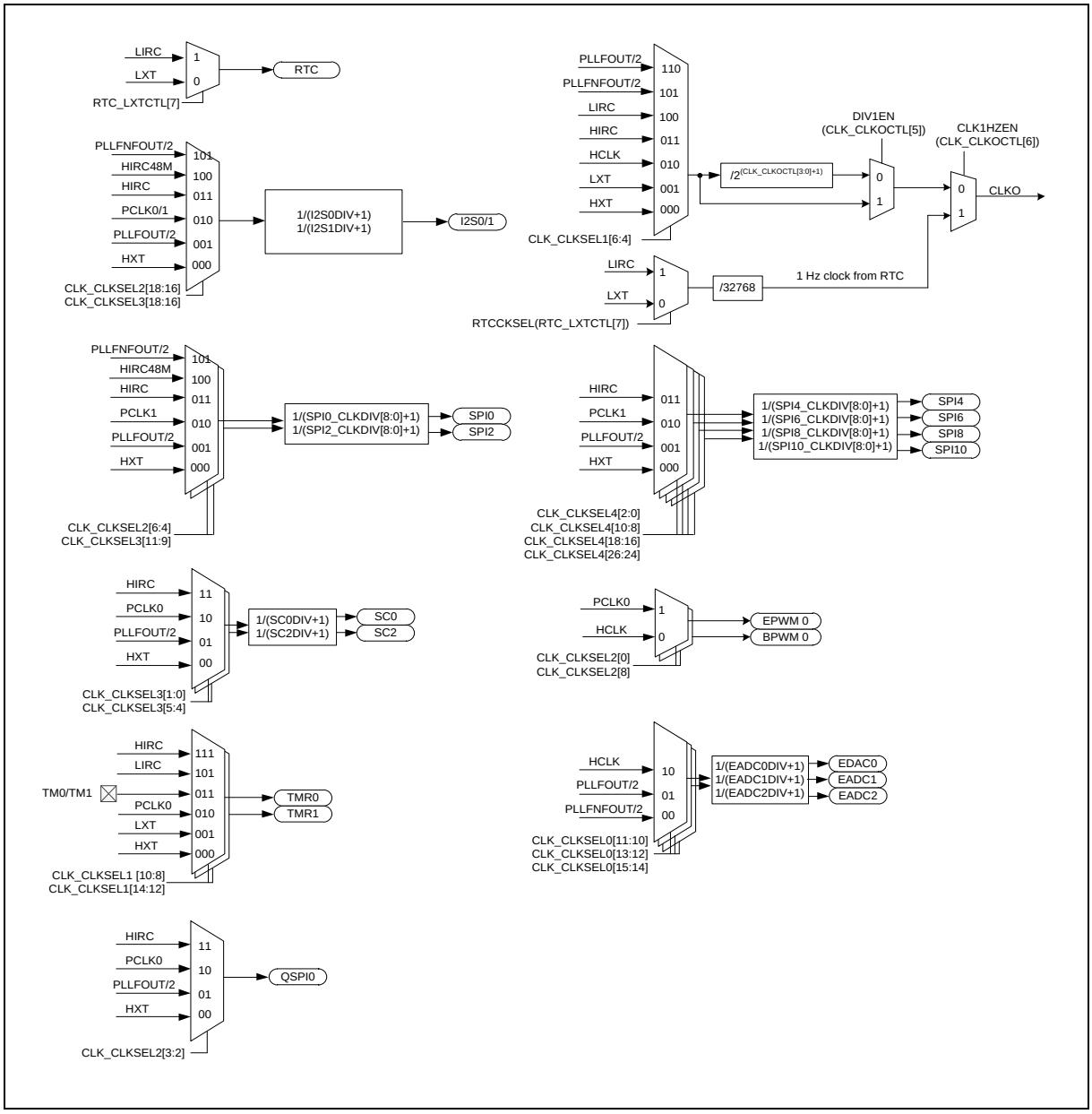


Figure 6.3-2 Clock Generator Global View Diagram (2/3)

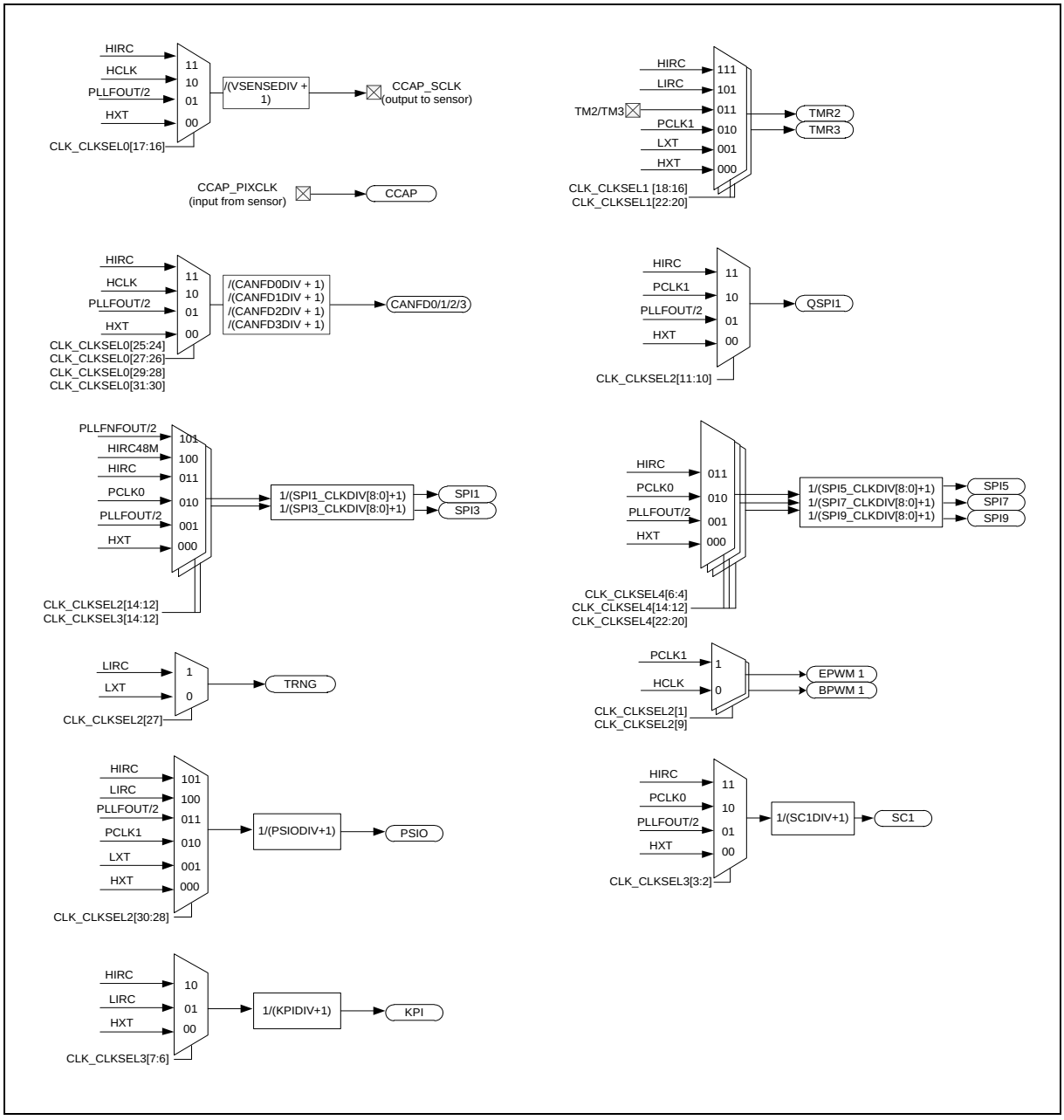


Figure 6.3-3 Clock Generator Global View Diagram (3/3)

6.3.2 Clock Generator

The clock generator consists of 7 clock sources, which are listed below:

- 32.768 kHz external low speed crystal oscillator (LXT)
- 4~24 MHz external high speed crystal oscillator (HXT)
- Programmable PLL output clock frequency (PLLFOUT), PLL source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)
- Programmable Audio PLL (PLLFN) output clock frequency (PLLFNFOUT), PLLFN source can be selected from external 4~24 MHz external high speed crystal (HXT) or 12 MHz internal high speed oscillator (HIRC)

- 12 MHz internal high speed RC oscillator (HIRC)
- 10 kHz internal low speed RC oscillator (LIRC)
- 48 MHz internal high speed RC oscillator (HIRC48M)

Each of these clock sources has certain stable time to wait for clock operating at stable frequency. When clock source is enabled, a stable counter start counting and correlated clock stable index is set to 1 after stable counter value reach a define value as shown in Table 6.3-1.

System and peripheral can use the clock as its operating clock only when correlate clock stable index is set to 1. The clock stable index as shown in Table 6.3-2 will auto clear when user disables the clock source.

Besides, the clock stable index of HXT, HIRC, HIRC48M, PLL and PLLFN will auto clear when chip enter power-down and clock stable counter will re-counting after chip wake-up if correlate clock is enabled.

Clock Source	Clock Stable Count Value	Clock Stable Time
HXT	4096 HXT clocks	341.33us for 12 MHz
LXT	16384 LXT clocks	500ms for 32.768 kHz
PLL	1200 PLL source clocks (CLK_PLLCTL[23]=0) 2400 PLL source clocks (CLK_PLLCTL[23]=1)	100us for 12 MHz 200us for 12 MHz
LIRC	1 LIRC clock	100us for 10 kHz
HIRC	64 HIRC clocks (CLK_PWRCTL[17:16]=0x0) 24 HIRC clocks (CLK_PWRCTL[17:16]=0x1)	5.33us for 12 MHz 2us for 12 MHz
HIRC48M	256 HIRC48M clocks	5.33us for 48 MHz
PLLFN	1200 PLL source clocks (CLK_PLLFNCTL1[28]=0) 2400 PLL source clocks (CLK_PLLFNCTL1[28]=1)	100us for 12 MHz 200us for 12 MHz

Table 6.3-1 Clock Stable Count Value Table

Clock Source	Clock Source Enable Bit	Correlated Clock Stable Index
HXT	HXTEN(CLK_PWRCTL[0])	HXTSTB(CLK_STATUS[0])
LXT	LXTEN(CLK_PWRCTL[1])	LXTSTB(CLK_STATUS[1])
PLL	PD(CLK_PLLCTL[16])	PLLSTB(CLK_STATUS[2])
LIRC	LIRCEN(CLK_PWRCTL[3])	LIRCSTB(CLK_STATUS[3])
HIRC	HIRCEN(CLK_PWRCTL[4])	HIRCSTB(CLK_STATUS[4])
HIRC48M	HIRC48MEN(CLK_PWRCTL[18])	HIRC48MSTB(CLK_STATUS[6])
PLLFN	PD(CLK_PLLFNCTL1[28])	PLLFNSTB(CLK_STATUS[10])

Table 6.3-2 Each Clock Source Enable Bit and Corresponding Stable Flag Table

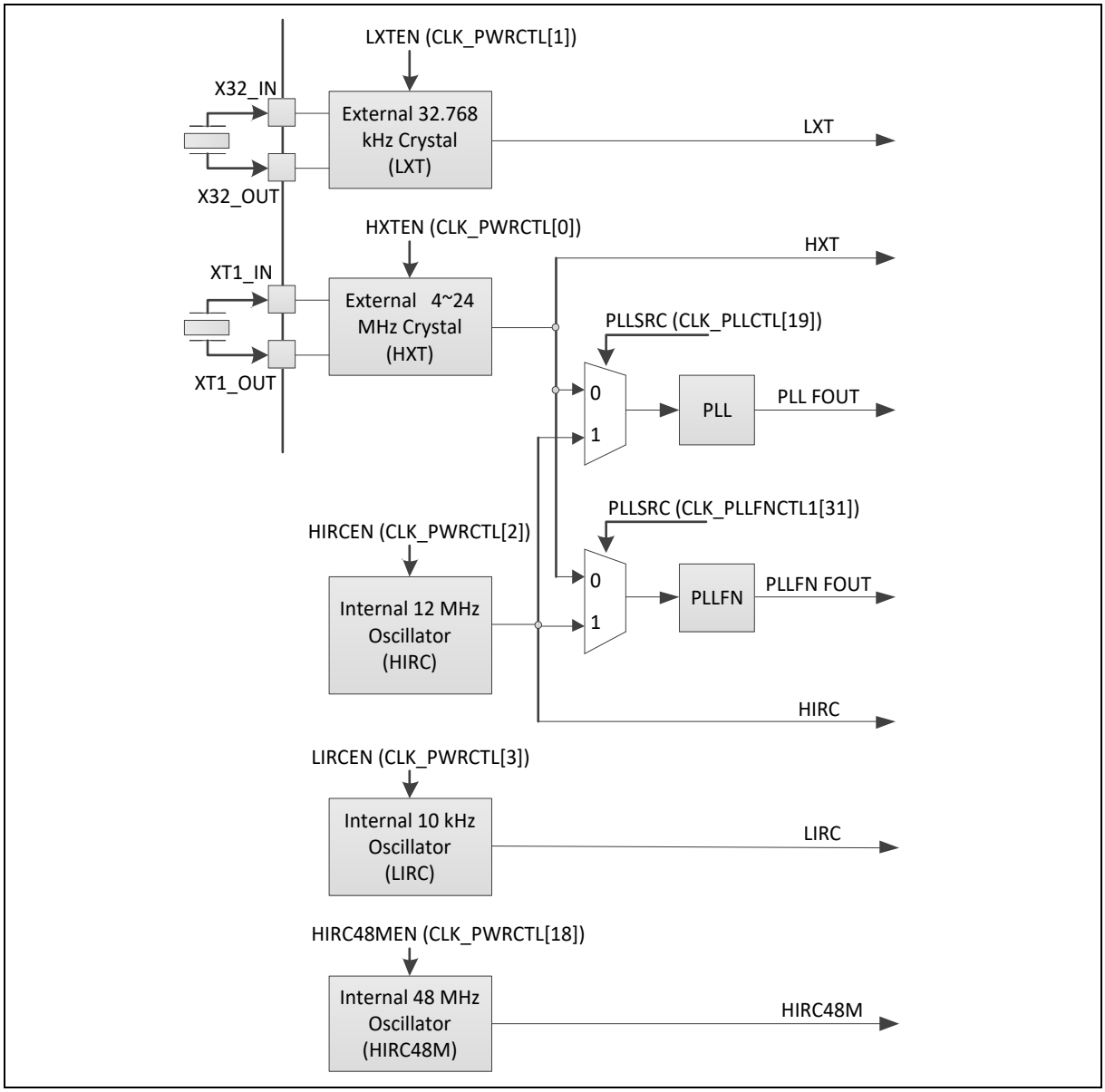


Figure 6.3-4 Clock Generator Block Diagram

6.3.3 System Clock and SysTick Clock

The system clock has 5 clock sources, which were generated from clock generator block. The clock source switch depends on the register HCLKSEL (CLK_CLKSEL0[2:0]). The block diagram is shown in Figure 6.3-5.

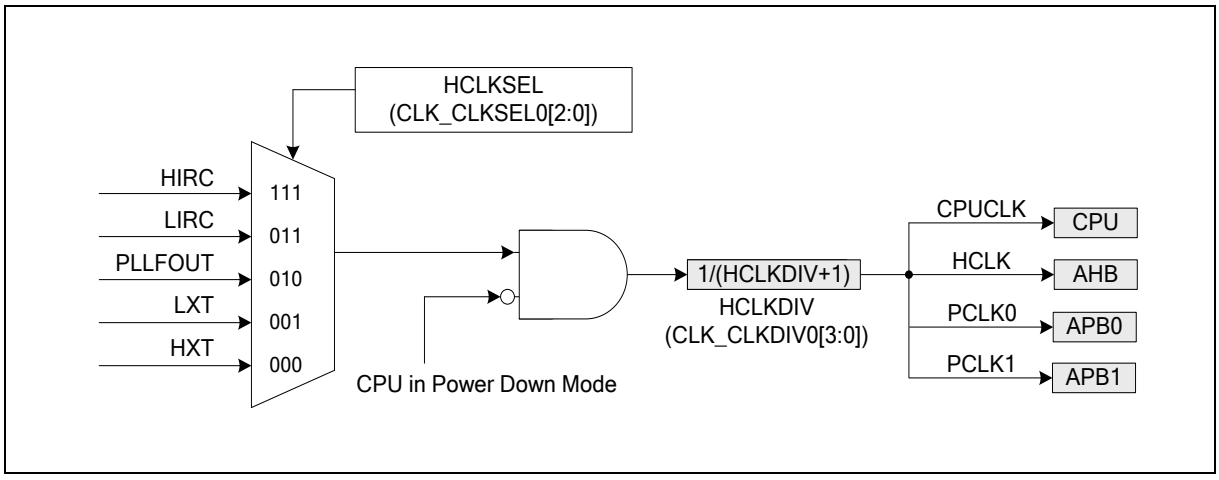


Figure 6.3-5 System Clock Block Diagrams

There are two clock fail detectors to observe HXT and LXT clock source and they have individual enable and interrupt control. When HXT detector is enabled, the HIRC clock is enabled automatically. When LXT detector is enabled, the LIRC clock is enabled automatically.

When HXT clock detector is enabled, the system clock will auto switch to HIRC if HXT clock stop being detected on the following condition: system clock source comes from HXT or system clock source comes from PLL with HXT as the input of PLL. If HXT clock stop condition is detected, the HXTFIF (CLK_CLKDSTS[0]) is set to 1 and chip will enter interrupt if HXTFIE (CLK_CLKDCTL[5]) is set to 1. User can try to recover HXT by disable HXT and enable HXT again to check if the clock stable bit is set to 1 or not. If HXT clock stable bit is set to 1, it means HXT is recover to oscillate after re-enable action and user can switch system clock to HXT again.

Figure 6.3-6 shows that the HXT clock stops detection and system clock switches to HIRC procedure.

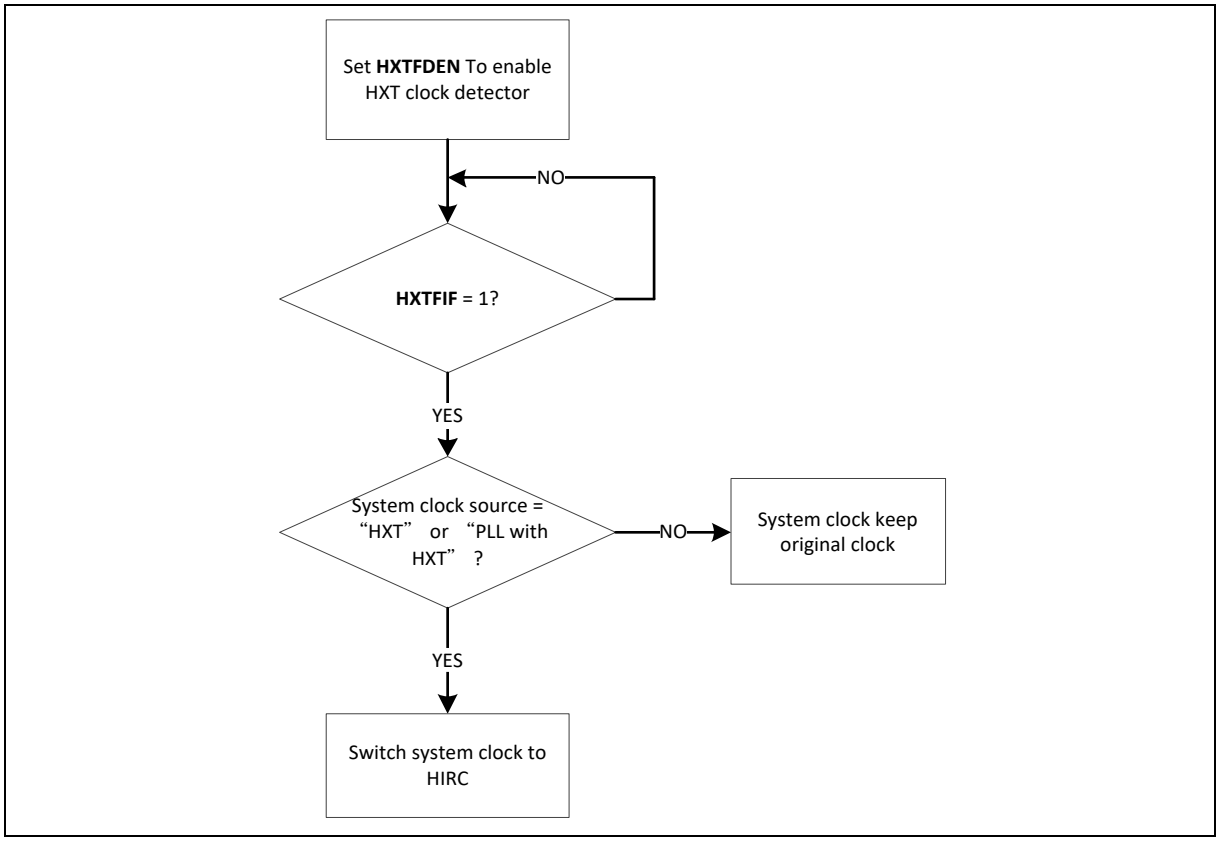


Figure 6.3-6 HXT Stop Protect Procedure

The clock source of SysTick in Cortex-M4 core can use CPU clock or external clock (SYST_CTRL[2]). If using external clock, the SysTick clock (STCLK) has 5 clock sources. The clock source switch depends on the setting of the register STCLKSEL (CLK_CLKSEL0[5:3]). The block diagram is shown in Figure 6.3-7.

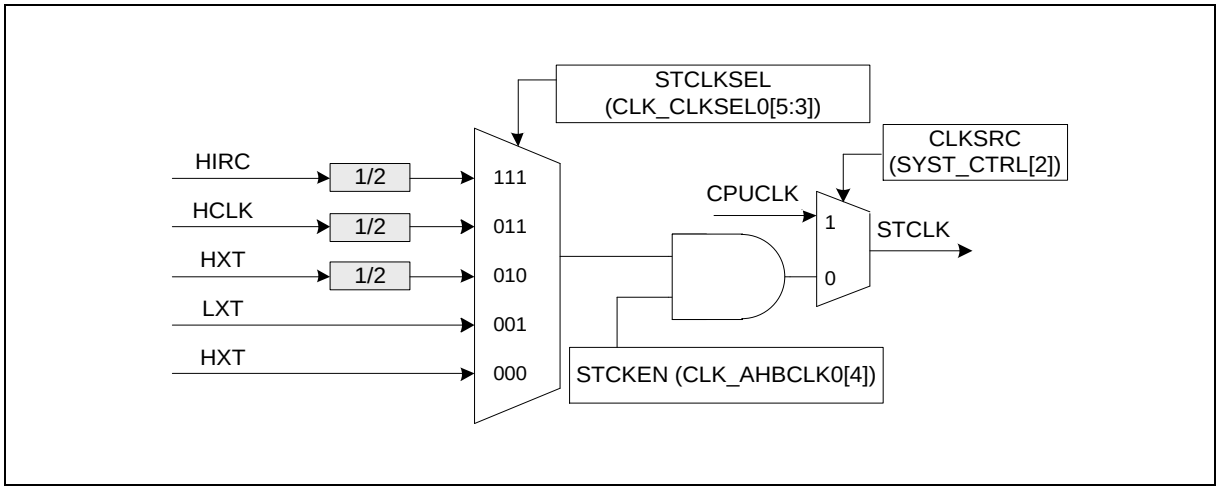


Figure 6.3-7 SysTick Clock Control Block Diagram

6.3.4 Peripherals Clock

Each peripheral clock has its own clock source selection. Refer to the CLK_CLKSEL0, CLK_CLKSEL1, CLK_CLKSEL2, CLK_CLKSEL3 and CLK_CLKSEL4 register.

6.3.5 Power-down Mode Clock

When entering Power-down mode, system clocks, some clock sources and some peripheral clocks are disabled. Some clock sources and peripherals clock are still active in Power-down mode.

The clocks, which still keep active, are listed below:

- Clock Generator
  - 10 kHz internal low speed RC oscillator (LIRC) clock
  - 32.768 kHz external low speed crystal oscillator (LXT) clock
- Peripherals Clock (When the modules adopt LXT or LIRC as clock source)

6.3.6 Clock Output

This device is equipped with a power-of-2 frequency divider that is composed of 16 chained divide-by-2 shift registers. One of the 16 shift register outputs selected by a sixteen to one multiplexer is reflected to CLKO function pin. Therefore, there are 16 options of power-of-2 divided clocks with the frequency from $F_{in}/2^1$ to $F_{in}/2^{16}$ where F_{in} is input clock frequency to the clock divider.

The output formula is $\mathbf{F_{out} = F_{in}/2^{(N+1)}}$, where F_{in} is the input clock frequency, F_{out} is the clock divider output frequency and N is the 4-bit value in FREQSEL (CLK_CLKOCTL[3:0]).

When writing 1 to CLKOEN (CLK_CLKOCTL[4]), the chained counter starts to count. When writing 0 to CLKOEN (CLK_CLKOCTL[4]), the chained counter continuously runs till divided clock reaches low state and stays in low state.

When entering Power-down mode, clock output does not output clock even if the CKO clock source is LXT.

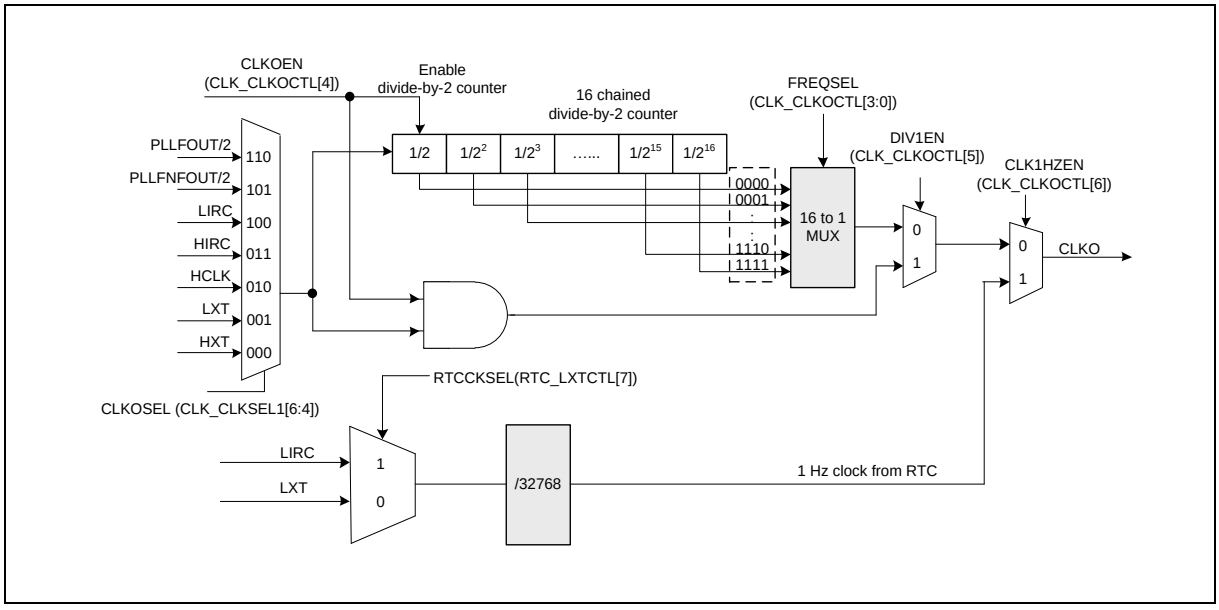


Figure 6.3-8 Clock Output Block Diagram

6.3.7 USB Clock Source

The clock sources of USB 1.1 and 2.0 systems are generated from USB2.0 PHY clock or programmable PLL output. The generated clocks are shown in Figure 6.3-9.

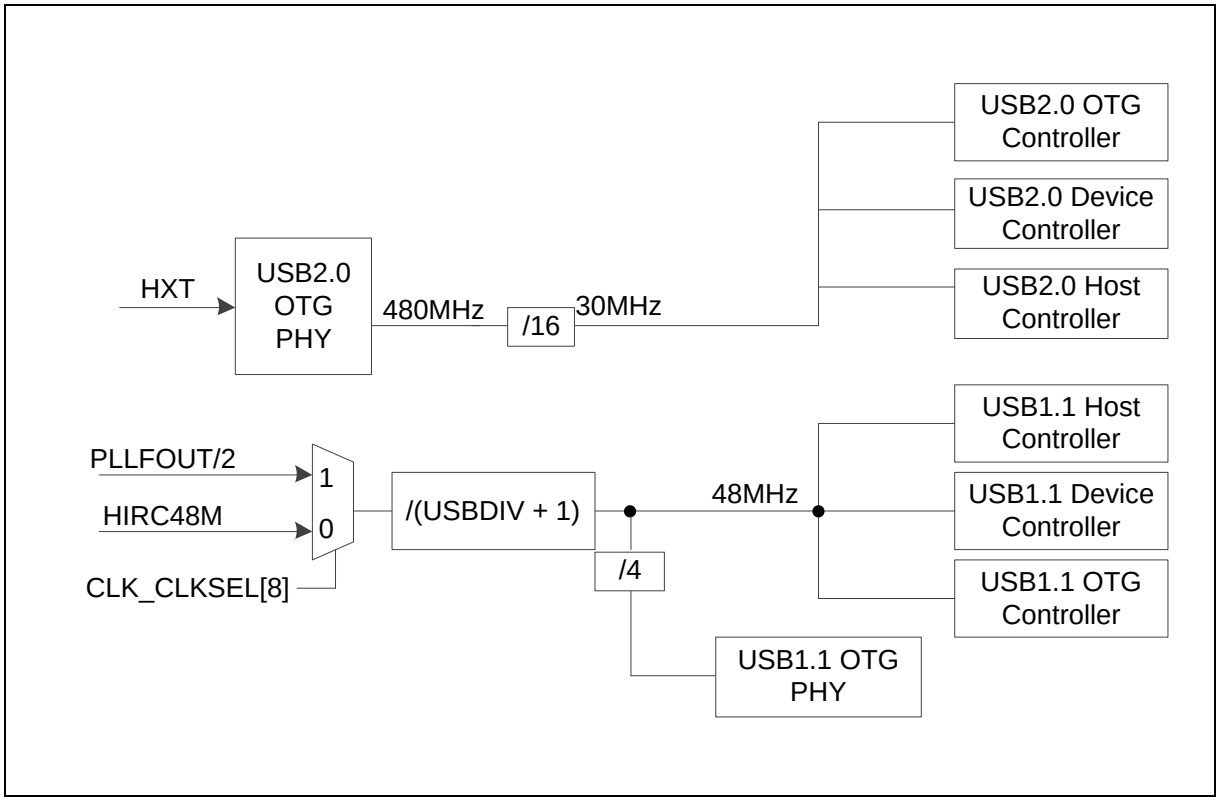


Figure 6.3-9 USB Clock Source

6.4 True Random Number Generator (TRNG)

6.4.1 Overview

The purpose of True Random Number Generator (TRNG) is to generate the randomness by extracting from physical phenomena.

6.4.2 Features

- 800 random bits per second
- Provides the true random number seed for PRNG

6.5 Flash Memory Controller (FMC)

6.5.1 Overview

The FMC is equipped with 256/512/1024 Kbytes on-chip embedded Flash for application and configurable Data Flash to store some application dependent data. Thus, the total size of application rom (APROM) is 256/512/1024 Kbytes. A User Configuration block provides for system initiation. A 8 Kbytes loader ROM (LDROM) is used for In-System-Programming (ISP) function. A 3 Kbytes one-time-program ROM (OTP) is used for recording one-time-program data. A 16/24 Kbytes Boot Loader consists of native ISP functions and secure boot function. A 4 Kbytes cache with zero wait cycle is used to improve Flash access performance. This chip also supports In-Application-Programming (IAP) function. User switches the code executing without chip reset after the embedded Flash is updated.

6.5.2 Features

- Supports dual-bank Flash macro for safe firmware upgrade
- Supports 256/512/1024 Kbytes application ROM (APROM)
- Supports 8 Kbytes loader ROM (LDROM)
- Supports 4 XOM (eXecution Only Memory) regions to conceal user program in APROM.
- Supports Data Flash with configurable memory size
- Supports 16 bytes User Configuration block to control system initiation
- Supports 3 Kbytes one-time-program ROM (OTP)
- Supports 4 Kbytes page erase for all embedded Flash
- Supports bank erase for APROM, except for XOM regions
- Supports Boot Loader with native In-System-Programming (ISP) functions
- Supports Secure Boot function for code integrity and authenticity
- Supports Security Key protection function for APROM, LDROM and User Configuration block.
- Supports 32-bit/64-bit and multi-word Flash programming function
- Supports fast Flash programming verification function
- Supports CRC32 checksum calculation function
- Supports Flash all one verification function
- Supports In-System-Programming (ISP) / In-Application-Programming (IAP) to update embedded Flash memory
- Supports cache memory to improve Flash access performance and reduce power consumption

6.6 External Bus Interface (EBI)

6.6.1 Overview

This chip is equipped with an external bus interface (EBI) for external device use. To save the connections between an external device and a chip, EBI is operating at address bus and data bus multiplex mode. The EBI supports three chip selects that can connect three external devices with different timing setting requirements.

6.6.2 Features

- Supports up to three memory banks
- Supports dedicated external chip select pin with polarity control for each bank
- Supports accessible space up to 1 Mbytes for each bank, actually external addressable space is dependent on package pin out
- Supports 8-/16-bit data width
- Supports byte write in 16-bit data width mode
- Supports address bus and data bus multiplex mode
- Supports address bus and data bus separate mode
- Supports Timing parameters individual adjustment for each memory block
- Supports LCD interface i80 mode
- Supports PDMA mode
- Supports variable external bus base clock (MCLK) which based on HCLK
- Supports configurable idle cycle for different access condition: Idle of Write command finish (W2X) and Idle of Read-to-Read (R2R)

6.7 HyperBus Interface Controller (HBI)

6.7.1 Overview

HyperBus is a low signal count, Double Data Rate (DDR) interface, which achieves high speed read and write throughout. The DDR protocol transfers two data bytes per clock cycle on the DQ input/output signals. A read or write transaction on HyperBus consists of a series of 16-bit wide, one clock cycle data transfer at the HyperRAM memory.

There is one APB and one AHB interfaces in this controller. The APB interface is used to configure the setting registers and short word access. The AHB interface is used to direct access HyperRAM up to 32 Mbytes.

6.7.2 Features

- HyperRAM 2.0
  - HyperRAM 1.0 supported
- Supports 32 Mbytes address memory space access
- Up to 90Mhz HyperBus clock rate
  - Maximum 1440M Bits/s data rate
- Configurable reset timing control
- Configurable chip select timing control for HyperRAM exit from HS (Hybrid Sleep) or DPD (deep power down) mode

6.8 General Purpose I/O (GPIO)

6.8.1 Overview

This chip has up to 146 General Purpose I/O pins to be shared with other function pins depending on the chip configuration. These 146 pins are arranged in 10 ports named as PA, PB, PC, PD, PE, PF, PG, PH, PI and PJ. PA, PB, PE, PG and PH has 16 pins on port. PC, PD has 15 pins on port. PF has 12 pins on port. PI has 10 pins on port. PJ has 14 pins on port. Each of the 146 pins is independent and has the corresponding register bits to control the pin mode function and data.

The I/O type of each of I/O pins can be configured by software individually as Input, Push-pull output, Open-drain output or Quasi-bidirectional mode. After the chip is reset, the I/O mode of all pins are depending on CIOINI (CONFIG0[10]). Please refer to the Datasheet for detailed pin operation voltage information about V_{DD}, V_{DDIO} and V_{BAT} electrical characteristics.

6.8.2 Features

- Four I/O modes:
  - Quasi-bidirectional mode
  - Push-Pull Output mode
  - Open-Drain Output mode
  - Input only with high impendence mode
- TTL/Schmitt trigger input selectable
- I/O pin can be configured as interrupt source with edge/level setting
- Supports High Drive and High Slew Rate I/O mode
- Configurable default I/O mode of all pins after reset by CIOINI (CONFIG0[10]) setting
  - CIOINI = 0, all GPIO pins in Quasi-bidirectional mode after chip reset
  - CIOINI = 1, all GPIO pins in input mode after chip reset
- Supports independent pull-up and pull-down control
- Enabling the pin interrupt function will also enable the wake-up function
- Supports EINT0~7 edge detect and trigger function

6.9 PDMA Controller (PDMA)

6.9.1 Overview

The peripheral direct memory access (PDMA) controller is used to provide high-speed data transfer. The PDMA controller can transfer data from one address to another without CPU intervention. This has the benefit of reducing the workload of CPU and keeps CPU resources free for other applications. There are two PDMA controller PDMA0 and PDMA1. PDMA controller has a total of 16 channels and each channel can perform transfer between memory and peripherals or between memory and memory.

6.9.2 Features

- Supports 16 independently configurable channels
- Supports selectable 2 level of priority (fixed priority or round-robin priority)
- Supports 2 PDMA controller PDMA0 and PDMA1
- Supports transfer data width of 8, 16, and 32 bits
- Supports source and destination address increment size can be byte, half-word, word or no increment
- Supports software and USB, UART, USCI, SPI, QSPI, ACMP, PSIO, EINT, EPWM, I^2C0, I^2C1, I^2S, Timer, ADC, and DAC request
- Supports Scatter-gather mode to perform sophisticated transfer through the use of the descriptor link list table
- Supports single and burst transfer type
- Supports time-out function on all channels
- Supports stride function from channel 0 to channel 5
- Supports enhanced stride function on channel 0 and channel1

6.10 Timer Controller (TMR)

6.10.1 Overview

The timer controller includes four 32-bit timers, Timer0 ~ Timer3, allowing user to easily implement a timer control for applications. The timer can perform functions, such as frequency measurement, delay timing, clock generation, and event counting by external input pins, and interval measurement by external capture pins.

The timer controller also provides four PWM generators. Each PWM generator supports two PWM output channels in independent mode and complementary mode. The output state of PWM output pin can be control by pin mask, polarity and break control, and dead-time generator.

6.10.2 Features

6.10.2.1 Timer Function Features

- Four sets of 32-bit timers, each timer having one 24-bit up counter and one 8-bit prescale counter
- Independent clock source for each timer
- Provides one-shot, periodic, toggle-output and continuous counting operation modes
- 24-bit up counter value is readable through CNT (TIMERx_CNT[23:0])
- Supports event counting function
- Supports 3-bit capture input noise filter
- 24-bit capture value is readable through CAPDAT (TIMERx_CAP[23:0])
- Supports external capture pin event for interval measurement
- Supports external capture pin event to reset 24-bit up counter
- Supports chip wake-up from Idle/Power-down mode if a timer interrupt signal is generated
- Support Timer0 ~ Timer3 time-out interrupt signal or capture interrupt signal to trigger EPWM, BPWM, EADC, DAC and PDMA function
- Supports internal capture triggered while internal ACMP output signal transition
- Supports internal clock (HIRC, LIRC) and external clock (HXT, LXT) for capture event
- Supports Inter-Timer trigger mode
- Supports event counting source from ACMP or internal USB SOF signal

6.10.2.2 PWM Function Features

- Supports maximum clock frequency up to maximum PCLK
- Supports independent mode for PWM generator with two output channels
- Supports complementary mode for PWM generator with paired PWM output channel
  - 12-bit dead-time insertion with 12-bit prescale
- Supports 12-bit prescale from 1 to 4096
- Supports 16-bit PWM counter
  - Up, down and up-down count operation type
  - One-shot or auto-reload counter operation mode
- Supports mask function and tri-state enable for each PWM output pin

- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, Brown-out detection, SRAM parity error and CPU lockup)
  - Brake pin noise filter control for brake source
  - Edge detect brake source to control brake state until brake status cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:
  - PWM zero point, period point, up-count compared or down-count compared point events
  - Brake condition happened
- Supports PWM output accumulator event to trigger PDMA transfer
- Supports PWM output accumulator event to stop PWM counting
- Supports trigger EADC on the following events:
  - PWM zero point, period, zero or period point, up-count compared or down-count compared point events
- Supports External Pin event to trigger PWM counter action

6.11 Basic PWM Generator and Capture Timer (BPWM)

6.11.1 Overview

The chip provides two BPWM generators — BPWM0 and BPWM1. Each BPWM supports 6 channels of BPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit BPWM counter with 16-bit comparator. The BPWM counter supports up, down and up-down counter types, all 6 channels share one counter. BPWM uses the comparator compared with counter to generate events. These events are used to generate BPWM pulse, interrupt and trigger signal for EADC0/1/2 to start conversion. For BPWM output control unit, it supports polarity output, independent pin mask and tri-state output enable.

The BPWM generator also supports input capture function to latch BPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened.

6.11.2 Features

6.11.2.1 BPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency.
- Supports up to two BPWM modules; each module provides 6 output channels
- Supports independent mode for BPWM output/Capture input channel
- Supports 12-bit prescalar from 1 to 4096
- Supports 16-bit resolution BPWM counter; each module provides 1 BPWM counter
  - Up, down and up/down counter operation type
- Supports mask function and tri-state enable for each BPWM pin
- Supports interrupt in the following events:
  - BPWM counter matches 0, period value or compared value
- Supports trigger EADC0/1/2 in the following events:
  - BPWM counter matches 0, period value or compared value

6.11.2.2 Capture Function Features

- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option

6.12 EPWM Generator and Capture Timer (EPWM)

6.12.1 Overview

The chip provides two EPWM generators — EPWM0 and EPWM1. Each EPWM supports 6 channels of EPWM output or input capture. There is a 12-bit prescaler to support flexible clock to the 16-bit EPWM counter with 16-bit comparator. The EPWM counter supports up, down and up-down counter types. EPWM uses comparator compared with counter to generate events. These events use to generate EPWM pulse, interrupt and trigger signal for EADC/DAC to start conversion.

The EPWM generator supports two standard EPWM output modes: Independent mode and Complementary mode, they have difference architecture. There are two output functions based on standard output modes: Group function and Synchronous function. Group function can be enabled under Independent mode or complementary mode. Synchronous function only enabled under complementary mode. Complementary mode has two comparators to generate various EPWM pulse with 12-bit dead-time generator and another free trigger comparator to generate trigger signal for EADC. For EPWM output control unit, it supports polarity output, independent pin mask and brake functions.

The EPWM generator also supports input capture function. It supports latch EPWM counter value to corresponding register when input channel has a rising transition, falling transition or both transition is happened. Capture function also support PDMA to transfer captured data to memory.

6.12.2 Features

6.12.2.1 EPWM Function Features

- Supports maximum clock frequency up to maximum PLL frequency
- Supports up to two EPWM modules, each module provides 6 output channels
- Supports independent mode for EPWM output/Capture input channel
- Supports complementary mode for 3 complementary paired EPWM output channel
  - Dead-time insertion independent control with 12-bit resolution
  - Synchronous function for phase control
  - Two compared values during one period
- Supports 12-bit prescaler from 1 to 4096
- Supports 16-bit resolution EPWM counter
  - Up, down and up/down counter operation type
- Supports one-shot or auto-reload counter operation mode
- Supports group function
- Supports synchronous function
- Supports mask function and tri-state enable for each EPWM pin
- Supports brake function
  - Brake source from pin, analog comparator and system safety events (clock failed, SRAM parity error, Brown-out detection and CPU lockup).
  - Noise filter for brake source from pin
  - Leading edge blanking (LEB) function for brake source from analog comparator
  - Edge detect brake source to control brake state until brake interrupt cleared
  - Level detect brake source to auto recover function after brake condition removed
- Supports interrupt on the following events:

- EPWM counter matches 0, period value or compared value
- Brake condition happened

- Supports trigger EADC/DAC on the following events:
  - EPWM counter matches 0, period value or compared value
  - EPWM counter matches free trigger comparator compared value (only for EADC)
  - Supports EPWM trigger EADC event prescaler feature
- Supports PDMA transfer for Interrupt Flag Accumulator Function
- Supports EPWM output accumulator stop counter mode
- Supports Fault Detect function
- Supports External Pin Trigger Function

6.12.2.2 Capture Function Features

- Supports 3-bit capture input noise filter
- Supports up to 12 capture input channels with 16-bit resolution
- Supports rising or falling capture condition
- Supports input rising/falling capture interrupt
- Supports rising/falling capture with counter reload option
- Supports PDMA transfer function for EPWM all channels

6.13 Enhanced Quadrature Encoder Interface (EQEI)

6.13.1 Overview

There are four EQEI controllers in this device. The Enhanced Quadrature Encoder Interface (EQEI) decodes speed of rotation and motion sensor information. It can be used in any application that uses a quadrature encoder for feedback.

6.13.2 Features

6.13.2.1 Enhanced Quadrature Encoder Interface (EQEI) Features

- Up to four EQEI controllers, EQEI0, EQEI1, EQEI2 and EQEI3.
- Two EQEI phase inputs, QEA and QEB; One Index input.
- A 32-bit up/down Quadrature Encoder Pulse Counter (EQEI_CNT)
- A 32-bit software-latch Quadrature Encoder Pulse Counter Hold Register (EQEI_CNTHOLD)
- A 32-bit Quadrature Encoder Pulse Counter Index Latch Register (EQEI_CNTLATCH)
- A 32-bit Quadrature Encoder Pulse Counter Compare Register (EQEI_CNTCMP) with a Pre-set Maximum Count Register (EQEI_CNTMAX)
- A 32-bit up count Unit Timer Pulse Counter (EQEI_UTCNT)
- A 32-bit Unit Timer Pulse Counter Compare Register (EQEI_UTCMP)
- One EQEI control register (EQEI_CTL) and one EQEI Status Register (EQEI_STATUS)
- Four Quadrature encoder pulse counter operation modes:
  - Supports X4 free-counting mode
  - Supports X2 free-counting mode
  - Supports X4 compare-counting mode
  - Supports X2 compare-counting mode
- Two Quadrature encoder phase counter operation modes:
  - Supports X1 1-phase 2 input compare-counting mode
  - Supports X2 1-phase 2 input compare-counting mode
- Two Quadrature encoder directional counter operation modes:
  - Supports X1 1-phase 1 input compare-counting mode
  - Supports X2 1-phase 1 input compare-counting mode
- Supports swap function for input signals QEA and QEB
- Supports for detecting the occurrence of phase error from input signals QEA and QEB
- Supports one times index signal reset function for Quadrature encoder pulse counter
- Encoder Pulse Width measurement mode
- Input frequency of QEA/QEB/IDX without noise filter must lower than PCLK/4
- Input frequency of QEA/QEB/IDX with noise filter must lower than Noise Filter Clock/8

6.14 Watchdog Timer (WDT)

6.14.1 Overview

The Watchdog Timer (WDT) is used to perform a system reset when system runs into an unknown state. This prevents system from hanging for an infinite period of time. Besides, this Watchdog Timer supports the function to wake up system from Idle/Power-down mode.

6.14.2 Features

- 20-bit free running up counter for WDT time-out interval
- Selectable time-out interval (2^4 ~ 2^{20}) and the time-out interval is 1.6 ms ~ 104.8576 s if WDT_CLK = 10 kHz
- System kept in reset state for a period of (1 / WDT_CLK) * 63
- Supports selectable WDT reset delay period, including 1026, 130, 18 or 3 WDT_CLK reset delay period
- Supports to force WDT enabled after chip powered on or reset by setting CWDTEN[2:0] in Config0 register
- Supports WDT time-out wake-up function only if WDT clock source is selected as LIRC 10 kHz or LXT

6.15 Window Watchdog Timer (WWDT)

6.15.1 Overview

The Window Watchdog Timer (WWDT) is used to perform a system reset within a specified window period to prevent software running to uncontrollable status by any unpredictable condition.

6.15.2 Features

- 6-bit down counter value (CNTDAT, WWDT_CNT[5:0]) and 6-bit compare value (CMPDAT, WWDT_CTL[21:16]) to make the WWDT time-out window period flexible
- Supports 4-bit value (PSCSEL, WWDT_CTL[11:8]) to programmable maximum 11-bit prescale counter period of WWDT counter
- WWDT counter suspends in Idle/Power-down mode

6.16 Real Time Clock (RTC)

6.16.1 Overview

The Real Time Clock (RTC) controller provides the real time and calendar message. The RTC offers programmable time tick and alarm match interrupts. The data format of time and calendar messages are expressed in BCD format. A digital frequency compensation feature is available to compensate external crystal oscillator frequency accuracy.

6.16.2 Features

- Supports external power pin V_{BAT}.
- Supports real time counter in RTC_TIME (hour, minute, second) and calendar counter in RTC_CAL (year, month, day) for RTC time and calendar check.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) settings in RTC_TALM and RTC_CALM.
- Supports alarm time (hour, minute, second) and calendar (year, month, day) mask enable in RTC_TAMSK and RTC_CAMSK.
- Selectable 12-hour or 24-hour time scale in RTC_CLKFMT register.
- Optional support 1/128 second HZCNT in RTC_TIME and RTC_TALM.
- Supports Leap Year indication in RTC_LEAPYEAR register.
- Supports Day of the Week counter in RTC_WEEKDAY register.
- Frequency of RTC clock source compensate by RTC_FREQADJ register.
- All time and calendar message expressed in BCD format.
- Supports periodic RTC Time Tick interrupt with 8 period interval options 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2 and 1 second.
- Supports RTC Time Tick and Alarm Match interrupt.
- Supports 1 Hz clock output.
- Supports chip wake-up from Idle or Power-down mode while a RTC interrupt signal is generated.
- Supports Daylight Saving Time software control in RTC_DSTCTL.
- Supports up to 3 pairs dynamic loop tamper pin or 6 individual tamper pins.
- Supports up to 80 bytes spare registers and tamper pins detection to clear the content of these spare registers.
- Supports Flash mass erase operate will also clear the spare registers content.

6.17 Camera Capture Interface Controller (CCAP)

6.17.1 Overview

The camera capture interface controller (CCAP) is designed to capture image data from a sensor. After capturing or fetching image data, it processes the image data. Then, the embedded DMA controller will move the data from the internal FIFO to system memory with AHB bus.

6.17.2 Features

- CCIR601 & CCIR656 interfaces supported for connection to CMOS image sensor
- 4-bit and 8-bit camera data width for CCIR656 interface
- YUV422 and RGB565 color format supported for data-in from CMOS sensor
- YUV422, RGB565, RGB555 and Y-only color supported for packet data output.
- Single interrupt source to interrupt controller from maskable interrupt source: Address Match, Bus Master Transfer Error, Video Frame End
- Embedded DMA controller supported to transfer data from internal FIFO to system memory through AHB bus
- CROP function supported to crop input image to the required size for digital application.
- Frame rate scaling-down supported
- Image scaling-down supported
- Bit luma output with 8-bit threshold setting supported.

6.18 Enhanced Input Capture Timer (ECAP)

6.18.1 Overview

The chip provides up to four units of Input Capture Timer/Counter whose capture function can detect the digital edge-changed signal at channel inputs. Each unit has three input capture channels. The timer/counter is equipped with up counting, reload and compare-match capabilities.

6.18.2 Features

- Up to four Input Capture Timer/Counter units, CAP0, CAP1, CAP2 and CAP3.
- Each unit has 3 input channels.
- Each unit has its own interrupt vector.
- Each input channel has its own capture counter hold register.
- 24-bit Input Capture up-counting timer/counter.
- With noise filter in front end of input ports.
- Edge detector with three options:
  - Rising edge detection
  - Falling edge detection
  - Both edge detection
- Captured events reset and/or reload capture counter.
- Supports compare-match function.

6.19 USCI - Universal Serial Control Interface Controller (USCI)

6.19.1 Overview

The Universal Serial Control Interface (USCI) is a flexible interface module covering several serial communication protocols. The user can configure this controller as UART, SPI, or I^2C functional protocol.

6.19.2 Features

The controller can be individually configured to match the application needs. The following protocols are supported:

- UART
- SPI
- I^2C

6.20 USCI – UART Mode

6.20.1 Overview

The asynchronous serial channel UART covers the reception and the transmission of asynchronous data frames. It performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data transmitted from the controller. The receiver and transmitter are independent, and the transmission and reception can be started separately.

The UART controller also provides auto flow control. There are three conditions to wake up the system.

6.20.2 Features

- Supports one transmit buffer and two receive buffer for data payload
- Supports hardware auto flow control function
- Supports programmable baud-rate generator
- Support 9-bit Data Transfer (Support 9-bit RS-485)
- Baud rate detection possible by built-in capture event of baud rate generator
- Supports PDMA transfer
- Supports Wake-up function (Incoming Data and nCTS Wakeup Only)

6.21 USCI - SPI Mode

6.21.1 Overview

The SPI protocol of USCI controller applies to synchronous serial data communication and allows full duplex transfer. It supports both master and Slave operation mode with the 4-wire bi-direction interface. SPI mode of USCI controller performs a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. The SPI mode is selected by FUNMODE (USPI_CTL[2:0]) = 0x1

This SPI protocol can operate as Master or Slave mode by setting the SLAVE (USPI_PROTCTL[0]) to communicate with the off-chip SPI Slave or master device. The application block diagrams in Master and Slave mode are shown below.

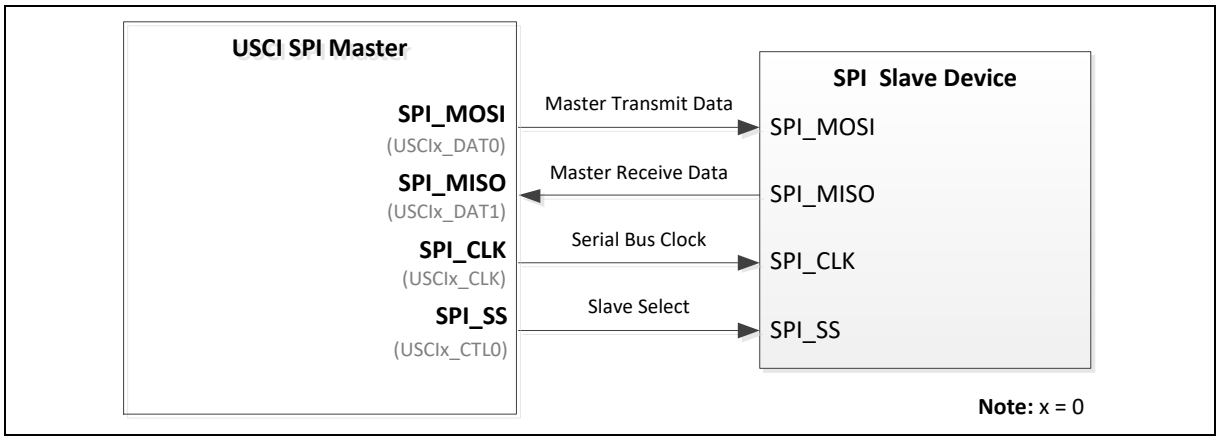


Figure 6.21-1 SPI Master Mode Application Block Diagram

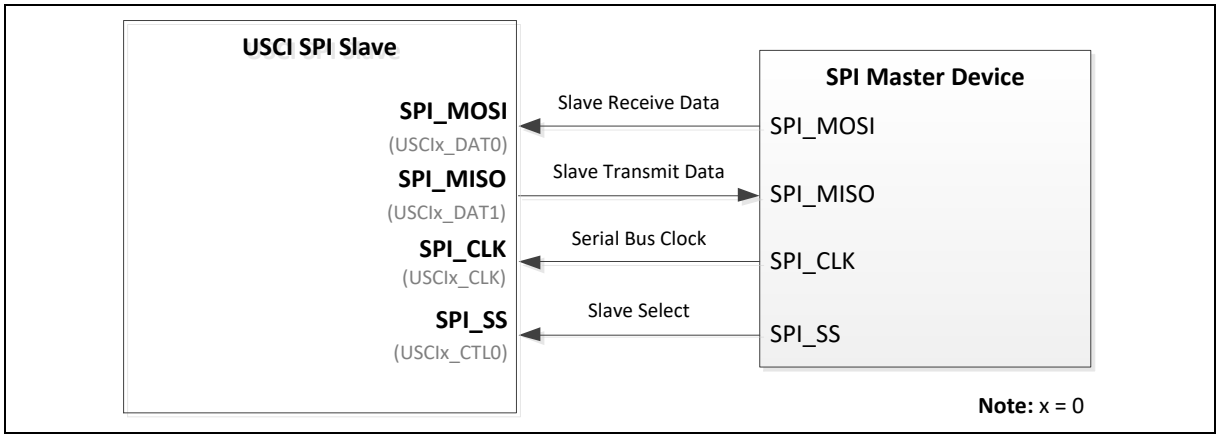


Figure 6.21-2 SPI Slave Mode Application Block Diagram

6.21.2 Features

- Supports Master or Slave mode operation (the maximum frequency -- Master = f_{PCLK} / 2, Slave < f_{PCLK} / 5)
- Configurable bit length of a transfer word from 4 to 16-bit
- Supports one transmit buffer and two receive buffers for data payload
- Supports MSB first or LSB first transfer sequence

- Supports Word Suspend function
- Supports PDMA transfer
- Supports 3-wire, no slave select signal, bi-direction interface
- Supports wake-up function by slave select signal in Slave mode
- Supports one data channel half-duplex transfer

6.22 USCI - I²C Mode

6.22.1 Overview

On I²C bus, data is transferred between a Master and a Slave. Data bits transfer on the SCL and SDA lines are synchronously on a byte-by-byte basis. Each data byte is 8-bit. There is one SCL clock pulse for each data bit with the MSB being transmitted first, and an acknowledge bit follows each transferred byte. Each bit is sampled during the high period of SCL; therefore, the SDA line may be changed only during the low period of SCL and must be held stable during the high period of SCL. A transition on the SDA line while SCL is high is interpreted as a command (START or STOP). Please refer to Figure 6.22-1 for more detailed I²C BUS Timing.

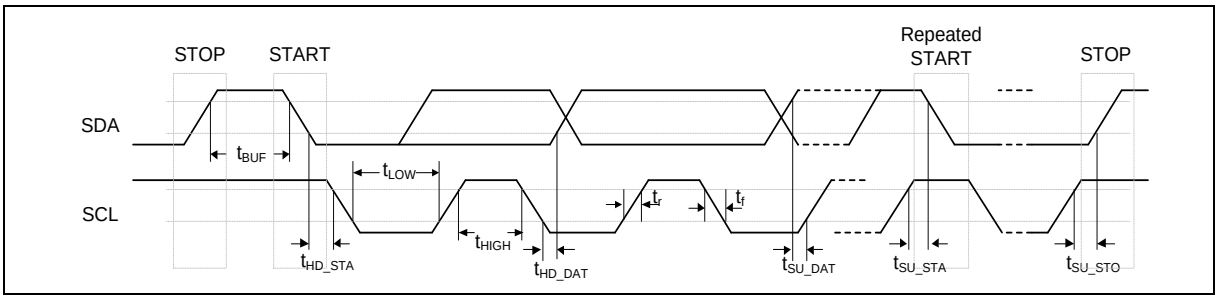


Figure 6.22-1 I²C Bus Timing

The device's on-chip I²C provides the serial interface that meets the I²C bus standard mode specification. The I²C port handles byte transfers autonomously. The I²C mode is selected by FUNMODE (UI2C_CTL [2:0]) = 100B. When enable this port, the USCI interfaces to the I²C bus via two pins: SDA and SCL. When I/O pins are used as I²C ports, user must set the pins function to I²C in advance.

Note: Pull-up resistor is needed for I²C operation because the SDA and SCL are set to open-drain pins when USCI is selected to I²C operation mode.

6.22.2 Features

- Full master and slave device capability
- Supports of 7-bit addressing, as well as 10-bit addressing
- Communication in standard mode (100 kbit/s) or in fast mode (up to 400 kbit/s)
- Supports multi-master bus
- Supports one transmit buffer and two receive buffer for data payload
- Supports 10-bit bus time-out capability
- Supports bus monitor mode.
- Supports Power down wake-up by START signal or address match
- Supports setup/hold time programmable
- Supports multiple address recognition (two slave address with mask option)

6.23 UART Interface Controller (UART)

6.23.1 Overview

The chip provides ten channels of Universal Asynchronous Receiver/Transmitters (UART). The UART controller performs serial-to-parallel conversion on data received from the peripheral and parallel-to-serial conversion on data transmitted from the CPU. Each UART controller channel supports ten types of interrupts. The UART controller supports flow control function. The UART controller also supports IrDA SIR, LIN, RS-485 and Single-wire function modes and auto-baud rate measuring function.

6.23.2 Features

- Full-duplex asynchronous communications
- Separates receive and transmit 16/16 bytes entry FIFO for data payloads
- Supports hardware auto-flow control
- Programmable receiver buffer trigger level
- Supports programmable baud rate generator for each channel individually
- Supports nCTS, incoming data, Received Data FIFO reached threshold and RS-485 Address Match (AAD mode) wake-up function
- Supports 8-bit receiver buffer time-out detection function
- Programmable transmitting data delay time between the last stop and the next START bit by setting DLY (UART_TOUT [15:8])
- Supports Auto-Baud Rate measurement and baud rate compensation function
  - 9600 bps for UART_CLK is selected LXT.
- Supports break error, frame error, parity error and receive/transmit buffer overflow detection function
- Fully programmable serial-interface characteristics
  - Programmable number of data bit, 5-, 6-, 7-, 8- bit character
  - Programmable PARITY bit, even, odd, no parity or stick PARITY bit generation and detection
  - Programmable STOP bit, 1, 1.5, or 2 STOP bit generation
- Supports IrDA SIR function mode
  - 3/16 bit duration for normal mode
- Supports LIN function mode (Only UART0/UART1 with LIN function)
  - LIN master/slave mode
  - Programmable break generation function for transmitter
  - Break detection function for receiver
- Supports RS-485 function mode
  - RS-485 9-bit mode
  - Hardware or software enables to program nRTS pin to control RS-485 transmission direction
- Supports PDMA transfer function
- Supports Single-wire function mode.

UART Feature	UART0/ UART1	UART2 ~ UART9	USCI-UART
FIFO	16 Bytes	16 Bytes	TX: 1byte RX: 2byte
Auto Flow Control (CTS/RTS)	√	√	√
IrDA	√	√	-
LIN	√	-	-
RS-485 Function Mode	√	√	√
nCTS Wake-up	√	√	√
Incoming Data Wake-up	√	√	√
Received Data FIFO reached threshold Wake-up	√	√	-
RS-485 Address Match (AAD mode) Wake-up	√	√	-
Received Data FIFO reached threshold Time-out Wake-up	√	√	-
Baud Rate Compensation	√	√	-
Auto-Baud Rate Measurement	√	√	√
STOP bit Length	1, 1.5, 2 bit	1, 1.5, 2 bit	1, 2 bit
Word Length	5, 6, 7, 8 bits	5, 6, 7, 8 bits	6~13 bits
Even / Odd Parity	√	√	√
Stick Bit	√	√	-

Table 6.23-1 M463/M467 Series UART Features

6.24 Ethernet MAC Controller (EMAC)

6.24.1 Overview

The EMAC enables a host to transmit and receive data over Ethernet in compliance with the IEEE 802.3-2008 standard.

In addition to the default interfaces defined in the IEEE 802.3 specifications, the EMAC supports several industry standard interfaces to the PHY. The EMAC is compliant with the following standards:

- IEEE 802.3-2008 for Ethernet MAC
- IEEE 1588-2008 standard for precision networked clock synchronization
- AMBA 2.0 for AHB master/slave port
- RMII specification version 1.2 from RMII consortium

6.24.2 Features

- 10 and 100 Mbps data transfer rates with the following PHY interfaces:
  - RMII interface to communicate with an external Fast Ethernet PHY
- Full-duplex operation:
  - IEEE 802.3x flow control automatic transmission of zero-quanta Pause frame on flow control input de-assertion
  - Forwarding of received Pause frames to the user application
- Half-duplex operation:
  - CSMA/CD Protocol support
  - Flow control using backpressure support
- Preamble and start of frame data (SFD) insertion in Transmit path
- Preamble and SFD deletion in the Receive path
- Automatic CRC and pad generation controllable on a per-frame basis
- Automatic Pad and CRC Stripping options for receive frames
- Programmable frame length to support Standard or Jumbo Ethernet frames with up to 16 Kbytes of size
- Programmable Interframe Gap (IFG) (40-96 bit times in steps of 8)
- Option to transmit frames with reduced preamble size
- Separate 32-bit status for transmit and receive packets
- IEEE 802.1Q VLAN tag detection for reception frames
- Separate transmission, reception, and control interfaces to the application
- Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
- Enhanced Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
- Support Ethernet frame timestamping as described in IEEE 1588-2002 and IEEE 1588-2008.

  The 64-bit timestamps are given in the transmit or receive status of each frame

- MDIO master interface for PHY device configuration and management
- Standard IEEE 802.3az-2010 for Energy Efficient Ethernet
- Flexibility to control the Pulse-Per-Second (PPS) output signal (ptp_pps_o)
- CRC replacement, Source Address field insertion or replacement, and VLAN insertion, replacement, and deletion in transmitted frames with per-frame control
- Programmable watchdog timeout limit in the receive path

6.25 Smart Card Host Interface (SC)

6.25.1 Overview

The Smart Card Interface controller (SC controller) is based on ISO/IEC 7816-3 standard and fully compliant with PC/SC Specifications. It also provides status of card insertion/removal. It can also be set as UART mode to communicate with other device.

6.25.2 Features

- ISO 7816-3 T = 0, T = 1 compliant
- EMV2000 compliant
- Three ISO 7816-3 ports
- Separates receive/transmit 4 bytes' entry FIFO for data payloads
- Programmable transmission clock frequency
- Programmable receiver buffer trigger level
- Programmable guard time selection (11 ETU ~ 267 ETU)
- One 24-bit timer and two 8-bit timers for Answer to Request (ATR) and waiting times processing
- Supports auto direct / inverse convention function
- Supports transmitter and receiver error retry and error number limiting function
- Supports hardware activation sequence process, and the time between PWR on and CLK start is configurable
- Supports hardware warm reset sequence process
- Supports hardware deactivation sequence process
- Supports hardware auto deactivation sequence when detected the card removal
- Supports UART mode
  - Full duplex, asynchronous communications
  - Separates receiving / transmitting 4 bytes' entry FIFO for data payloads
  - Supports programmable baud rate generator
  - Supports programmable receiver buffer trigger level
  - Programmable transmitting data delay time between the last stop bit leaving the TX-FIFO and the de-assertion by setting EGT (SCn_EGT[7:0])
  - Programmable even, odd or no parity bit generation and detection
  - Programmable stop bit, 1- or 2- stop bit generation

6.26 I²S Controller (I²S)

6.26.1 Overview

The I²S controller consists of I²S protocol to interface with external audio CODEC. Two 16-level depth FIFO for reading path and writing path respectively are capable of handling 8/16/24/32 bits audio data sizes. A PDMA controller handles the data movement between FIFO and memory.

6.26.2 Features

- Supports Master mode and Slave mode
- Capable of handling 8, 16, 24 and 32 bits data sizes in each audio channel
- Supports monaural and stereo audio data
- Supports I²S protocols: Philips standard, MSB-justified, and LSB-justified data format
- Supports PCM protocols: PCM standard, MSB-justified, and LSB-justified data format
- PCM protocol supports TDM multi-channel transmission in one audio sample, and the number of data channel can be set as 2, 4, 6, or 8
- Provides two 16-level FIFO data buffers, one for transmitting and the other for receiving
- Generates interrupt requests when buffer levels cross a programmable boundary
- Supports two PDMA requests, one for transmitting and the other for receiving

6.27 Serial Peripheral Interface (SPI)

6.27.1 Overview

The Serial Peripheral Interface (SPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains up to four sets of SPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device. Each SPI controller can be configured as a master or a slave device and supports the PDMA function to access the data buffer. Each SPI controller also supports I^2S mode to connect external audio CODEC.

6.27.2 Features

- SPI Mode
  - Up to four sets of SPI controllers
  - Supports Master or Slave mode operation
  - Master mode up to 100 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7~3.6V)
  - Configurable bit length of a transaction word from 4 to 32-bit
  - Provides separate 4-level depth transmit and receive FIFO buffers
  - Supports MSB first or LSB first transfer sequence
  - Supports Byte Reorder function
  - Supports Byte or Word Suspend mode
  - Supports PDMA transfer
  - Supports 3-Wire, no slave selection signal, bi-direction interface
  - Supports one data channel half-duplex transfer
  - Supports receive-only mode
- I^2S Mode
  - Supports Master or Slave
  - Capable of handling 8-, 16-, 24- and 32-bit word sizes
  - Each provides two 4-level FIFO data buffers, one for transmitting and the other for receiving
  - Supports monaural and stereo audio data
  - Supports PCM mode A, PCM mode B, I^2S and MSB justified data format
  - Supports two PDMA requests, one for transmitting and the other for receiving

6.28 Quad Serial Peripheral Interface (QSPI)

6.28.1 Overview

The Quad Serial Peripheral Interface (QSPI) applies to synchronous serial data communication and allows full duplex transfer. Devices communicate in Master/Slave mode with the 4-wire bi-direction interface. The chip contains two QSPI controllers performing a serial-to-parallel conversion on data received from a peripheral device, and a parallel-to-serial conversion on data transmitted to a peripheral device.

The QSPI controller supports 2-bit Transfer mode to perform full-duplex 2-bit data transfer and also supports Dual and Quad I/O Transfer mode and the controller supports the PDMA function to access the data buffer.

6.28.2 Features

- Supports Master or Slave mode operation
- Master mode up to 100 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Slave mode up to 50 MHz (when chip works at V_{DD} = 2.7V~3.6V)
- Supports 2-bit Transfer mode
- Supports Dual and Quad I/O Transfer mode
- Configurable bit length of a transaction word from 8 to 32-bit
- Provides separate 8-level depth transmit and receive FIFO buffers
- Supports MSB first or LSB first transfer sequence
- Supports Byte Reorder function
- Supports Byte or Word Suspend mode
- Supports PDMA transfer
- Supports 3-Wire, no slave selection signal, bi-direction interface
- Supports one data channel half-duplex transfer
- Supports Transmit Double Transfer Rate Mode (TX DTR mode)
- Supports receive-only mode

6.29 SPI Synchronous Serial Interface Controller (SPI Master Mode)

6.29.1 Overview

The SPI Synchronous serial Interface Controller for SPI master mode performs a serial-to-parallel conversion on data received from the peripheral, and a parallel-to-serial conversion on data received from MCU. This SPI controller can drive one external peripheral (External SPI Flash) and it is seen as the SPI master mode. It can generate an interrupt signal when data transfer is finished and can be cleared by writing 1 to the interrupt flag. The active level of device/slave select signal can be chosen to low active or high active, which depends on the peripheral. Writing a divisor into the SPIM_CTL1 register can program the frequency of serial clock output to the peripheral.

In SPI Flash controller, normal I/O mode contains four 32-bit transmit/receive buffers, and can provide 1 to 4 burst mode operation. The number of bits in each transaction can be 8, 16, 24, or 32; data can be transmitted/received up to four successive transactions in one transfer.

By DMA write mode, user can move data from SRAM to external SPI Flash component. In DMA read mode, user can move data from external SPI Flash component to SRAM. In direct memory mapping mode (DMM mode), this SPI Flash controller will translate the AHB bus commands into SPI Flash operations without MCU setting related SPI Flash command. Therefore users can access external SPI Flash as a ROM module.

In direct memory mapping mode with cache off mode, it will pre-fetch 4-word Flash data after a direct memory mapping access. When using direct memory mapping mode with cache on mode, it will use 16 Kbytes cache memory to reduce the number of accessing external SPI Flash component and the performance of SPI Flash access can be improved. To improve the read operation of SPI Flash without increasing the serial clock frequency, this SPI Flash controller supports DTR (Double Transfer Rate) read command codes that support Standard/Dual/Quad SPI modes. The one byte command code is still latched into the device on the rising edge of the serial clock similar to all other SPI commands. Once a DTR instruction code is accepted by the device, the address input and data output will be latched on both rising and falling edges of the serial clock.

For data protection, this SPI Flash controller supports cipher encryption and decryption circuits to protect data which user places into external SPI Flash when DMA read/write mode and direct memory mapping mode are used.

6.29.2 Features

- Supports maximum 32 Mbytes SPI Flash size
- Supports SPI master mode
- Supports Direct Memory Mapping Mode and Normal I/O Mode
- Supports 8/16/24/32 bits transaction for Normal I/O mode
- Provides burst mode operation in Normal I/O mode, which can transmit/receive data up to four successive transactions in one transfer
- Supports DMA mode read/write
- Supports standard (1-bit), dual (2-bit), and quad (4-bit) I/O transfer mode
- Supports Double Transfer Rate (DTR) mode
- Supports 16 Kbytes cache memory
- Supports Cipher encryption/decryption
- One slave/device select line for external SPI Flash component

6.30 I²C Serial Interface Controller (I²C)

6.30.1 Overview

I²C is a two-wire, bi-directional serial bus that provides a simple and efficient method of data exchange between devices. The I²C standard is a true multi-master bus including collision detection and arbitration that prevents data corruption if two or more masters attempt to control the bus simultaneously.

There are five sets of I²C controllers which support Power-down wake-up function.

6.30.2 Features

The I²C bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus. The main features of the I²C bus include:

- Supports up to five I²C ports
- Master/Slave mode
- Bidirectional data transfer between masters and slaves
- Multi-master bus (no central master)
- Supports Standard mode (100 kbps), Fast mode (400 kbps) and Fast mode plus (1 Mbps)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization used as a handshake mechanism to suspend and resume serial transfer
- Built-in 14-bit time-out counter requesting the I²C interrupt if the I²C bus hangs up and timer-out counter overflow
- Programmable clocks allow for versatile rate control
- Supports 7-bit addressing and 10-bit addressing mode
- Supports multiple address recognition (four slave address with mask option)
- Supports Power-down wake-up function
- Supports PDMA with one buffer capability (Only I²C0/1 with PDMA function)
- Supports two-level buffer function
- Supports setup/hold time programmable
- Supports Bus Management (SM/PM compatible) function compatible with the SMBUS specification rev 2.0 (http://smbus.org/specs/) and PMBUS specification rev 1.2 (http://pmbus.org/)

6.31 Secure Digital Host Controller (SDH)

6.31.1 Overview

The Secure Digital Host Controller (SD Host) has DMAC unit and SD unit. The DMAC unit provides a DMA (Direct Memory Access) function for SD to exchange data between system memory and shared buffer (128 bytes), and the SD unit controls the interface of SD/SDHC. The SDHOST controller can support SD/SDHC and cooperated with DMAC to provide a fast data transfer between system memory and cards.

6.31.2 Features

- AMBA AHB master/slave interface compatible, for data transfer and register read/write.
- Supports single DMA channel.
- Supports hardware Scatter-Gather function.
- Using single 128 Bytes shared buffer for data exchange between system memory and cards.
- Synchronous design for DMA with single clock domain, AHB bus clock (HCLK).
- Interface with DMAC for register read/write and data transfer.
- Supports SD/SDHC card.
- Completely asynchronous design for Secure Digital with two clock domains, HCLK and Engine clock, note that frequency of HCLK should be higher than the frequency of peripheral clock.

6.32 Programmable Serial I/O (PSIO)

6.32.1 Overview

Programmable Serial I/O (PSIO) provides a simple way to implement simple serial signal processing, e.g. UART and IR. The PSIO can control when the pin will output high or low and how long the pin need to output high or low. It also provides the easy way to sample the pin state.

6.32.2 Features

- Supports up to 8 PSIO pins, from PSIO pin0 to PSIO pin7
- Supports 6 clock sources, they are HXT, LXT, HIRC, LIRC, PLL/2, PCLK1
- Supports one clock divider, which can be divided from 1 to 255
- Supports slot controller for timing sequence control
  - Supports 4 slot controllers, 8 slots in each slot controller
  - Supports counting from 1 PSIO clock to 15 PSIO clocks in each slot
  - Supports 3 slot repeat modes:
    - Normal repeat mode
    - Normal repeat mode with infinity loops
    - Whole repeat mode
  - Supports 4 slot trigger conditions:
    - Triggered by software
    - Triggered by falling edge
    - Triggered by rising edge
    - Triggered by rising edge or falling edge
- Supports PSIO PIN for pin state control
  - Supports 8 check points to connect with slots in each pin
  - Supports 8 check point actions in each check point.
  - Supports 7 kinds of check point action to setting
    - Output high
    - Output low
    - Output data
    - Output toggle
    - Input data
    - Input status
    - Input status update
  - Supports 4 I/O modes, input, output, open-drain, and quasi
  - Supports switch I/O mode in different check points
- Supports 4 kinds of Interrupt trigger conditions
  - Two sets of configurable slot interrupt controllers
  - Mismatch interrupt when PSIO is enabled with PDMA

- Transfer Error interrupt
- Slot controller counting done interrupt

- Supports PDMA function

6.33 USB 1.1 Device Controller (USBD)

6.33.1 Overview

There is one set of USB 2.0 full-speed device controller and transceiver in this device. It is compliant with USB 2.0 full-speed device specification and supports Control/Bulk/Interrupt/Isochronous transfer types.

In this device controller, there are two main interfaces: the APB bus and USB bus which comes from the USB PHY transceiver. For the APB bus, the CPU can program control registers through it. There are 1.5K byte sizes internal SRAM as data buffer in this controller. For IN or OUT transfer, it is necessary to write data to SRAM or read data from SRAM through the APB interface or SI.E. User needs to set the effective starting address of SRAM for each endpoint buffer through buffer segmentation register (USBD_BUFSEG0~24).

There are 25 endpoints in this controller. Each of the endpoint can be configured as IN or OUT endpoint. All the operations including Control, Bulk, Interrupt and Isochronous transfer are implemented in this block. The block of “Endpoint Control” is also used to manage the data sequential synchronization, endpoint states, current start address, transaction status, and data buffer status for each endpoint.

There are five different interrupt events in this controller. They are the no-event-wake-up, device plug-in or plug-out event, USB events, such as IN ACK, OUT ACK, and BUS events, such as suspend and resume and SOF event, receive Start of Frame(SOF) packet in every 1ms event. Any event will cause an interrupt, and users just need to check the related event flags in interrupt event status register (USBD_INTSTS) to acknowledge what kind of interrupt occurring, and then check the related USB Endpoint Status Register (USBD_EPSTS0~3) to acknowledge what kind of event occurring in this endpoint.

A software-disconnect function is also supported for this USB controller. It is used to simulate the disconnection of this device from the host. If user enables SE0 bit (USBD_SE0), the USB controller will force the output of USB_D+ and USB_D- to level low and its function is disabled. After disabling the SE0 bit, host will enumerate the USB device again.

For more information on the Universal Serial Bus, please refer to *Universal Serial Bus Specification Revision 1.1.*

6.33.2 Features

- Compliant with USB 2.0 Full-Speed specification
- Provides 1 interrupt vector with 5 different interrupt events (NEVWK, VBDET, USB, BUS and SOF)
- Supports Control/Bulk/Interrupt/Isochronous transfer type
- Supports suspend function when no bus activity existing for 3ms
- Supports 25 endpoints for configurable Control/Bulk/Interrupt/Isochronous transfer types and maximum 1.5 Kbyte buffer size
- Provides remote wake-up capability
- Supports double buffer function

6.34 High Speed USB 2.0 Device Controller (HSUSBD)

6.34.1 Overview

The USB device controller interfaces the AHB bus and the UTMI bus. The USB controller contains both the AHB master interface and AHB slave interface. CPU programs the USB controller registers through the AHB slave interface. For IN or OUT transfer, the USB device controller needs to write data to memory or read data from memory through the AHB master interface. The USB device controller is compliant with USB 2.0 specification and it contains 12 configurable endpoints in addition to control endpoint. These endpoints could be configured to BULK, INTERRUPT or ISO. The USB device controller has a built-in DMA to relieve the load of CPU.

6.34.2 Features

- USB Specification revision 2.0 compliant
- Supports 12 configurable endpoints in addition to Control Endpoint
- Each of the endpoints can be Isochronous, Bulk or Interrupt and either IN or OUT direction
- Three different operation modes of an in-endpoint – Auto Validation mode, Manual Validation mode, Fly mode
- Supports DMA operation
- Supports Endpoint Maximum Packet Size up to 1024 bytes
- Supports V_{BUS} / Resume wakeup from system power-down mode
- Supports Link Power Management (LPM) feature
- Supports Battery Charging 1.2 (BC1.2) feature

6.35 USB 2.0 Host Controller (USBH)

6.35.1 Overview

This chip is equipped with a USB 2.0 HS/FS Host Controller (USBH) that supports Enhanced Host Controller Interface (EHCI) and Open Host Controller Interface (OpenHCI, OHCI) Specification, a register-level description of a host controller, to manage the devices and data transfer of Universal Serial Bus (USB).

The USBH supports an integrated Root Hub with a USB port, a DMA for real-time data transfer between system memory and USB bus, port power control and port overcurrent detection.

The USBH is responsible for detecting the connect and disconnect of USB devices, managing data transfer, collecting status and activity of USB bus, providing power control and detecting overcurrent of attached USB devices.

6.35.2 Features

- Compliant with Universal Serial Bus (USB) Specification Revision 2.0.
- Supports Enhanced Host Controller Interface (EHCI) Specification Revision 1.0
- Supports Open Host Controller Interface (OpenHCI) Specification Revision 1.0.
- Supports high-speed (480Mbps), full-speed (12Mbps) and low-speed (1.5Mbps) USB devices.
- Supports Control, Bulk, Interrupt, Isochronous and Split transfers.
- Supports an integrated Root Hub.
- Supports a port routing logic to route full/low speed device to OHCI controller.
- Supports two USB host port shared with USB device (OTG function).
- Supports port power control and port overcurrent detection.
- Supports DMA for real-time data transfer.

6.36 USB On-The-Go (OTG)

6.36.1 Overview

The OTG controller interfaces to USB PHY and USB controllers which consist of an USB 1.1 host controller and an USB 2.0 FS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 2.0 Specification”.

An USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in USBROLE (SYS_USBPHY[1:0]). In Host-only mode, the USB frame acts as USB host. The USB frame can support both full-speed and low-speed transfer. In Device-only mode, the USB frame acts as USB device. USB device support full-speed transfer. In ID dependent mode, the USB frame can be USB Host or USB device depending on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. The USB frame only supports full-speed transfer when OTG device acts as a peripheral

6.36.2 Features

- Built-in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The role of USB frame is only dependent on USB_ID pin state --as USB Host (USB_ID pin is at low) or USB Device (USB_ID pin is at high). Both HNP and SRP protocols are not supported.
  - OTG device: depends on USB_ID pin state to be A-device (USB_ID pin is low) or B-device (USB_ID pin is high). HNP and SRP protocols are supported.

6.37 High Speed USB On-The-Go (HSOTG)

6.37.1 Overview

The HSOTG controller interfaces to USB PHY and USB controllers which consist of a USB 2.0 host controller and a USB 2.0 HS device controller. The OTG controller supports HNP and SRP protocols defined in the “On-The-Go and Embedded Host Supplement to the USB 2.0 Revision 1.3 Specification”.

USB frame, including USB host, USB device, and OTG controller, can be configured as Host-only, Device-only, ID dependent or OTG device mode defined in HSUSBROLE (SYS_USBPHY[17:16]). In Host-only mode, USB frame acts as USB host. USB frame can support high-speed, full-speed and low-speed transfer. In Device-only mode, USB frame acts as USB device. USB frame supports high-speed and full-speed transfer. In ID dependent mode, USB frame can be USB Host or USB device depends on USB_ID pin state. In OTG device mode, the role of USB frame depends on the definition of OTG specification. USB frame supports high-speed and full-speed transfer when OTG device acts as a peripheral.

6.37.2 Features

- Built in USB PHY
- Configurable to operate as:
  - Host-only
  - Device-only
  - ID dependent: The USB frame can act as USB Host (USB_ID pin is at low) or USB Device (USB_ID pin is at high) only depending on USB_ID pin state. HNP or SRP protocol is not supported.

- OTG device: It can be A-device (USB_ID pin state is at low) or B-device (USB_ID pin state is at high) depending on USB_ID pin state. HNP and SRP protocols are supported.

6.38 Controller Area Network with Feasibility Data Rate (CAN FD)

6.38.1 Overview

The CAN FD controller performs communication according to ISO 11898-1:2015 and need be connected to additional transceiver hardware for the physical layer.

The CAN FD controller consists of one CAN Core, Memory access control and arbiter, Tx Handler, Rx Handler, a shared Message RAM memory and a 32-bit AHB interface for control and configuration registers.

The message storage is intended to be a single-ported Message RAM outside of the CAN Core module. It is connected to the CAN Core via the memory control interface. The Message RAM implements filters, receive FIFOs, transmit event FIFOs and transmit FIFOs.

All functions concerning the handling of messages are implemented by the Rx Handler and the Tx Handler. The Rx Handler manages message acceptance filtering, the transfer of received messages from the CAN Core to the Message RAM as well as providing received message status information. The Tx Handler is responsible for the transfer of transmit messages from the Message RAM to the CAN Core as well as providing transmitted status information.

The controller's clock domain concept allows the separation among CAN Core clock and the AHB clock.

6.38.2 Features

- Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015
- CAN FD with up to 64 data bytes supported
- CAN Error Logging
- AUTOSAR support
- SAE J1939 support
- Improved acceptance filtering
- Two configurable Receive FIFOs
- Separate signaling on reception of High Priority Messages
- Configurable Transmit FIFO, Transmit Queue, Transmit Event FIFO
- Direct Message RAM access for CPU
- Programmable loop-back test mode
- Maskable module interrupts
- Two clock domains (CAN Core clock and AHB clock)
- Power-down support

6.39 CRC Controller (CRC)

6.39.1 Overview

The Cyclic Redundancy Check (CRC) generator can perform CRC calculation with 8-bits, 16-bits and 32-bits configurable polynomials.

6.39.2 Features

- Supports 8-bits, 16-bits and 32-bits configurable polynomials
- Programmable seed value
- Supports programmable order reverse setting for input data and CRC checksum
- Supports programmable 1's complement setting for input data and CRC checksum
- Supports 8/16/32-bit of data width
  - 8-bit write mode: 1-AHB clock cycle operation
  - 16-bit write mode: 2-AHB clock cycle operation
  - 32-bit write mode: 4-AHB clock cycle operation
- Supports using PDMA to write data to perform CRC operation

6.40 Cryptographic Accelerator (CRYPTO)

6.40.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES, SHA/HMAC, RSA, and ECC algorithms.

The PRNG core supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation. (283~571 bits are only generated for key store).

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2, CBC-CS3, CCM and GCM mode.

The SHA accelerator is an implementation fully compliant with the SHA-160, SHA-224, SHA-256, SHA-384, SHA-512, SHA-512/t, SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256. The SHA accelerator supports HMAC (Keyed-Hash Message Authentication Code) algorithms including HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, HMAC-SHA-512, HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512.

The ECC accelerator is an implementation fully compliant with elliptic curve cryptography by using polynomial basis in binary field and prime filed.

The RSA accelerator is an implementation fully compliant with RSA cryptography, CRT decryption algorithm and side-channel attack countermeasures algorithm.

The Crypto can get key from key store and/or put the key to key store determined by the function of each accelerator.

6.40.2 Features

- PRNG
  - Supports 128, 163, 192, 224, 233, 255, 256, 283, 384, 409, 512, 521 and 571 bits random number generation (283~571 bits are only generated for key store).
  - Can take the true random number seed from TRNG
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports CCM mode, GCM mode and GMAC function
  - Supports key expander for key expansion in FIPS NIST 197
  - Supports one technique to improve side-channel attack protection ability
- SHA
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports SHA-160, SHA-224, SHA-256, SHA-384, SHA-512 and SHA-512/t
  - Supports SHA3-224, SHA3-256, SHA3-384, SHA3-512, SHAKE128 and SHAKE256
- HMAC
  - Supports FIPS NIST 180, 180-2, 180-4
  - Supports HMAC-SHA-160, HMAC-SHA-224, HMAC-SHA-256, HMAC-SHA-384, and

HMAC-SHA-512

- Supports HMAC-SHA3-224, HMAC-SHA3-256, HMAC-SHA3-384, and HMAC-SHA3-512

- ECC
  - Supports both prime field GF(p) and binary filed GF(2^m)
  - Supports NIST P-192, P-224, P-256, P-384, and P-521
  - Supports NIST B-163, B-233, B-283, B-409, and B-571
  - Supports NIST K-163, K-233, K-283, K-409, and K-571
  - Supports Curve25519
  - Supports Public Key Cryptographic Algorithm SM2 Based on Elliptic Curves
  - Supports point multiplication, addition and doubling operations in GF(p) and GF(2^m)
  - Supports modulus division, multiplication, addition and subtraction operations in GF(p)
  - Supports four techniques to improve side-channel attack protection ability
- RSA
  - Supports both encryption and decryption with 1024, 2048, 3072 and 4096 bits
  - Supports CRT decryption with 2048, 3072 and 4096 bits
  - Supports three techniques to improve side-channel attack protection ability

6.41 Cryptographic Accelerator for M463 Series (CRYPTO_M463)

6.41.1 Overview

The Crypto (Cryptographic Accelerator) includes a secure pseudo random number generator (PRNG) core and supports AES algorithm.

The PRNG core supports 128, 192 and 256 bits random number generation.

The AES accelerator is an implementation fully compliant with the AES (Advance Encryption Standard) encryption and decryption algorithm. The AES accelerator supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 mode.

The Crypto can get key from key store and/or put the key to key store determined by the function of each accelerator.

6.41.2 Features

- PRNG
  - Supports 128, 192, and 256 bits random number generation.
  - Can take the true random number seed from TRNG
- AES
  - Supports FIPS NIST 197
  - Supports SP800-38A and addendum
  - Supports 128, 192, and 256 bits key
  - Supports both encryption and decryption
  - Supports ECB, CBC, CFB, OFB, CTR, CBC-CS1, CBC-CS2 and CBC-CS3 modes
  - Supports key expander for key expansion in FIPS NIST 197

6.42 Key Store (KS)

6.42.1 Overview

The Key Store (KS) is the key management device and has a 4 Kbytes SRAM, 4 Kbytes Flash and OTP for key storage. The Key Store is capable of providing a crypto engine to access or storing the key while encryption, decryption and generation. The Key Store supports revoke key operation if the key is unused. The Key Store is able to protect the key by data remanence prevention for SRAM.

6.42.2 Features

- Supports programming interface for key management
- Supports key size required for Cryptographic engine from 128-bit to 4096-bit
- Supports 32 SRAM keys by 4 Kbytes SRAM
- Supports 32 Flash keys by 4 Kbytes Flash
- Supports 8 OTP keys, maximum key size is 256-bit
- Supports crypto engine access or store key in key store directly
- Supports to store AES/HMAC/ECC/RSA/CPU key
- Supports to store RSA middle data for CRT and SCAP mode
- Supports ECDH operation with ECC and PRNG engine
- Supports revoke operation
- Supports erase key in SRAM/Flash and revoke key in OTP while tamper event detected
- Supports data remanence prevention at SRAM
- Supports auto verify function
- Supports lock function for OTP keys

6.43 Keypad Interface (KPI)

6.43.1 Overview

The Keypad Interface (**KPI**) is an APB slave with configurable minimum 2-row up to 6-row scan output and minimum 1-column up to 8-column scan input. Any keys in the array pressed or released are de-bounced and generate an interrupt.

The KPI supports release multiple keys and press multiple keys scan interrupt. The interrupt is generated whenever it detects any key in the keypad pressing or releasing. User can know the interrupt source by querying KPI_STATUS register.

6.43.2 Features

- Matrix keypad interface (maximum 6x8 array, and minimum 2x1array)
- Programmable de-bounce time
- Generates interrupt and updates all the keys(maximum 48 keys, minimum 2 keys) information (press/release) every time the user pressing or releasing

6.44 Enhanced 12-bit Analog-to-Digital Converter (EADC)

6.44.1 Overview

The chip contains three 12-bit successive approximation analog-to-digital converters (SAR EADC converter) with 16 external input channels and 3 internal channels. The EADC converter can be started by software trigger, EPWM0/1 triggers, BPWM0/1 triggers, timer0~3 overflow pulse triggers, ADINT0 interrupt EOC (End of conversion) and ADINT1 interrupt EOC pulse trigger and external pin (EADC0_ST, EADC1_ST, EADC2_ST for EADC0~2 respectively) input signal.

6.44.2 Features

- Analog input voltage range: 0~ V_{REF} (Max to 3.6V)
- Reference voltage from V_{REF} pin
- 12-bit resolution and 10-bit accuracy is guaranteed
- Up to 16 single-end analog external input channels or 8 pair differential analog input channels
- Up to 3 internal channels, they are band-gap voltage (V_{BG}), temperature sensor (V_{TEMP}) , and Battery power divided by 4 (V_{BAT}/4)
- Four EADC interrupts (ADINT0~3) with individual interrupt vector addresses for EADC
- Maximum EADC clock frequency is 95 MHz for EADC
- Up to 5 MSPS conversion rate for EADC
- Supports calibration function and calibration interrupt
- Supports internal reference voltage V_{REF}: 1.6V, 2V, 2.5V and 3V.
- Supports power-down mode
- Up to 19 sample modules
  - Sample modules0~15 is configurable for EADC converter channel (EADC_CH0~15) and trigger source for each EADC
  - Sample module 16~18 is fixed for channel 16, 17, 18 input sources as band-gap voltage, temperature sensor, and Battery power divided by 4 (V_{BAT}/4)
  - Double buffer for sample control logic module 0~3
  - Configurable sampling time for each sample module
  - Conversion results are held in 19 data registers with valid and overrun indicators.
- Averaging (2^n times, n=0~8) to support up to 12-bit result and over-sampling, or called Accumulation, (2^n times, n=0~8) to support up to 16-bit result
- Supports conversion results left-alignment
- Any EADC conversion of each EADC can be started by:
  - Write 1 to SWTRGn (EADC_SWTRG[n], n = 0~18)
  - External pin EADC0_ST, EADC1_ST, EADC2_ST for EADC0~2 respectively
  - Timer0~3 overflow pulse triggers
  - ADINT0 and ADINT1 interrupt EOC (End of conversion) pulse triggers
  - EPWM/BPWM triggers
  - ADINT0 and ADINT1 interrupt SOC (Start of conversion) pulse trigger with delay counter

- Supports PDMA transfer
- Conversion Result Monitor by Compare Mode
- Supports triple ADC simultaneous mode

6.45 Digital to Analog Converter (DAC)

6.45.1 Overview

The DAC module is a 12-bit, voltage output digital-to-analog converter. It can be configured to 12- or 8-bit output mode and can be used in conjunction with the PDMA controller. The DAC integrates a voltage output buffer that can be used to reduce output impendence and drive external loads directly without having to add an external operational amplifier.

6.45.2 Features

- Analog output voltage range: 0~AV_{DD}.
- Supports 12- or 8-bit output mode.
- Rail to rail settle time 8us.
- Supports up to two 12-bit 1 MSPS voltage type DAC.
- Reference voltage from internal reference voltage (INT_VREF), V_{REF} pin.
- DAC maximum conversion updating rate 1 MSPS.
- Supports voltage output buffer mode and bypass voltage output buffer mode.
- Supports software and hardware trigger, including Timer0~3, EPWM0, EPWM1, and external trigger pin to start DAC conversion.
- Supports PDMA mode.
- Supports group mode of synchronized update capability for two DACs.

6.46 Analog Comparator Controller (ACMP)

6.46.1 Overview

The chip provides four comparators. The comparator output is logic 1 when positive input is greater than negative input; otherwise, the output is 0. Each comparator can be configured to generate an interrupt when the comparator output value changes.

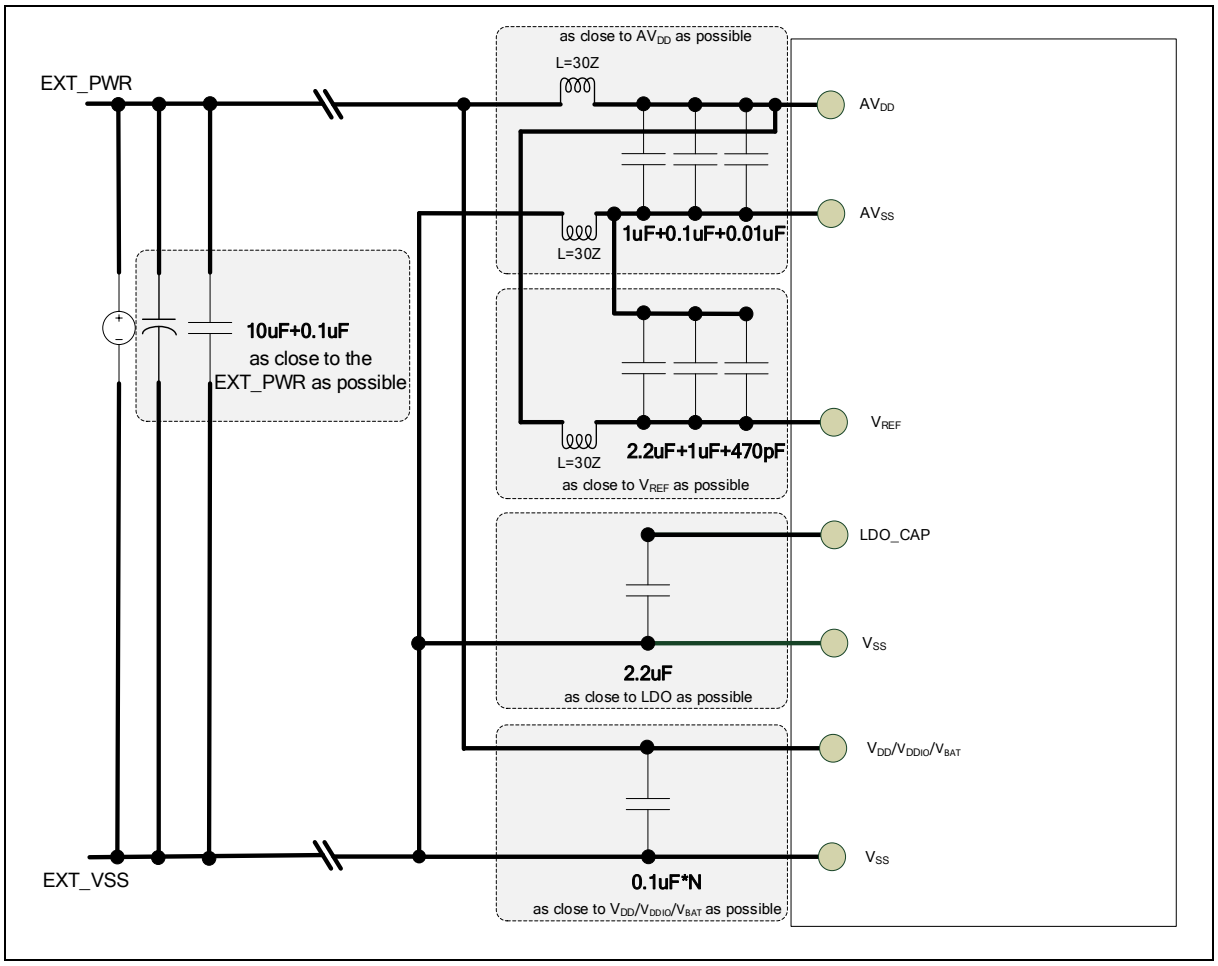
6.46.2 Features

- Analog input voltage range: 0 ~ AV_{DD} (voltage of AV_{DD} pin)
- Up to four rail-to-rail analog comparators
- Supports hysteresis function
  - Supports programmable hysteresis window: 0mV,-, 20mV,-, 40mV,
- Supports wake-up function
- Selectable input sources of positive input and negative input
- ACMP0 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP0_P0, ACMP0_P1, ACMP0_P2, or ACMP0_P3
  - 4 negative sources:
    - ACMP0_N
    - Supports Comparator Reference Voltage (CRV0)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP1 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP1_P0, ACMP1_P1, ACMP1_P2, or ACMP1_P3
  - 4 negative sources:
    - ACMP1_N
    - Supports Comparator Reference Voltage (CRV1)
    - Internal band-gap voltage (VBG)
    - DAC0 output (DAC0_OUT)
- ACMP2 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP2_P0, ACMP2_P1, ACMP2_P2, or ACMP2_P3
  - 4 negative sources:
    - ACMP2_N
    - Supports Comparator Reference Voltage (CRV2)
    - Internal band-gap voltage (VBG)
    - DAC1 output (DAC1_OUT)

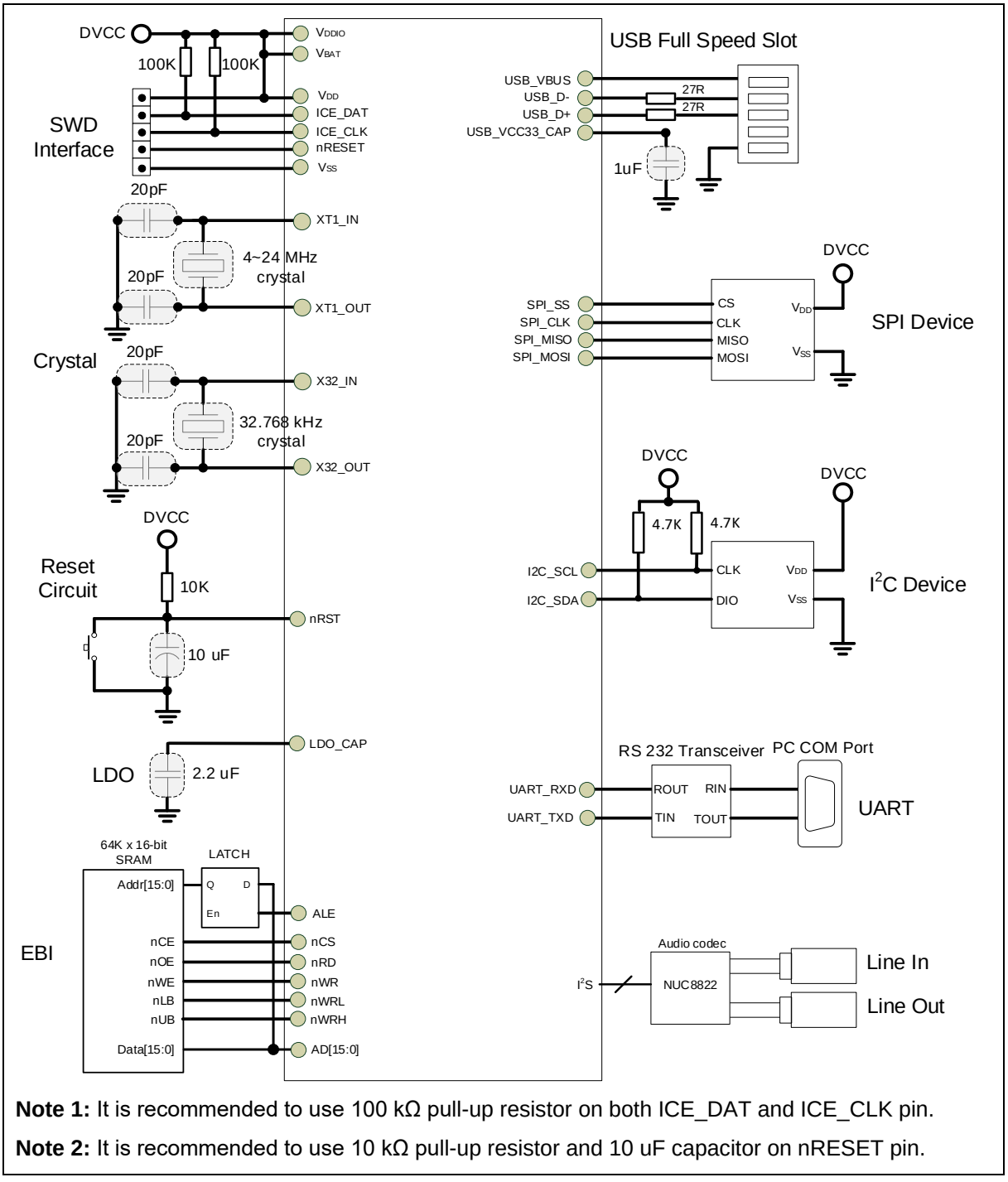
- ACMP3 supports:
  - 4 multiplexed I/O pins at positive sources:
    - ACMP3_P0, ACMP3_P1, ACMP3_P2, or ACMP3_P3
  - 4 negative sources:
    - ACMP3_N
    - Supports Comparator Reference Voltage (CRV3)
    - Internal band-gap voltage (VBG)
    - DAC1 output (DAC1_OUT)
- Shares one ACMP interrupt vector for two comparators
- Interrupts generated when compare results change (Interrupt event condition is programmable)
- Supports triggers for break events and cycle-by-cycle control for EPWM
- Supports window compare mode and window latch mode
- Supports offset calibration

7 APPLICATION CIRCUIT

7.1 Power Supply Scheme



7.2 Peripheral Application Scheme



Note 1: It is recommended to use 100 kΩ pull-up resistor on both ICE_DAT and ICE_CLK pin.

Note 2: It is recommended to use 10 kΩ pull-up resistor and 10 uF capacitor on nRESET pin.

8 ELECTRICAL CHARACTERISTICS FOR M463 SERIES

8.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

8.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
V_{DDIO}-V_{SS}[*1]	V_{DDIO} Power Supply	-0.3	4.0	V
V_{BAT}-V_{SS}[*1]	V_{BAT} Power Supply	-0.3	4.0	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input Voltage on 5V-tolerance GPIO	-	5.5	V
	Input Voltage on RTC domain (PF.6 ~ PF.11)		V_{DD}	V
	Input Voltage on any other pin[*2]		V_{DD}	V

Notes:

1. All main power (V_{DD}, V_{DDIO}, V_{BAT}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 9.1-2 Current Characteristics for the values of the maximum allowed injected current

Table 8.1-1 Voltage Characteristics

8.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	-	100	
I_{BAT}	Maximum Current into V_{BAT}	-	100	
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 8.1-2 Current Characteristics

8.1.3 Thermal Characteristics

The average junction temperature can be calculated by using the following equation:

$T_J = T_A + (P_D \times \theta_{JA})$

- T_A = ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_D = sum of internal and I/O power dissipation

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	105	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 48-pin QFN(5x5 mm)	-	37.8	-	℃/Watt
	Thermal resistance junction-ambient 48-pin LQFP(7x7 mm)	-	60	-	℃/Watt
	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	53.55	-	℃/Wat
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	50.09	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 8.1-3 Thermal Characteristics

8.1.4 EMC Characteristics

8.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

8.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

8.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-2000	-	+2000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-500	-	500	
LU[*3]	Pin current for latch-up[*3]	-400	-	400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 8.1-4 EMC Characteristics

8.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
48-pin QFN(5x5 mm) [*1]	MSL 3
48-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin LQFP(7x7 mm) [*1]	MSL 3
64-pin QFN(8x8 mm) [*1]	MSL 3
100-pin LQFP(14x14 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3
144-pin LQFP(20x20 mm) [*1]	MSL 3
176-pin LQFP(24x24 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 8.1-5 Package Moisture Sensitivity(MSL)

8.1.6 Soldering Profile

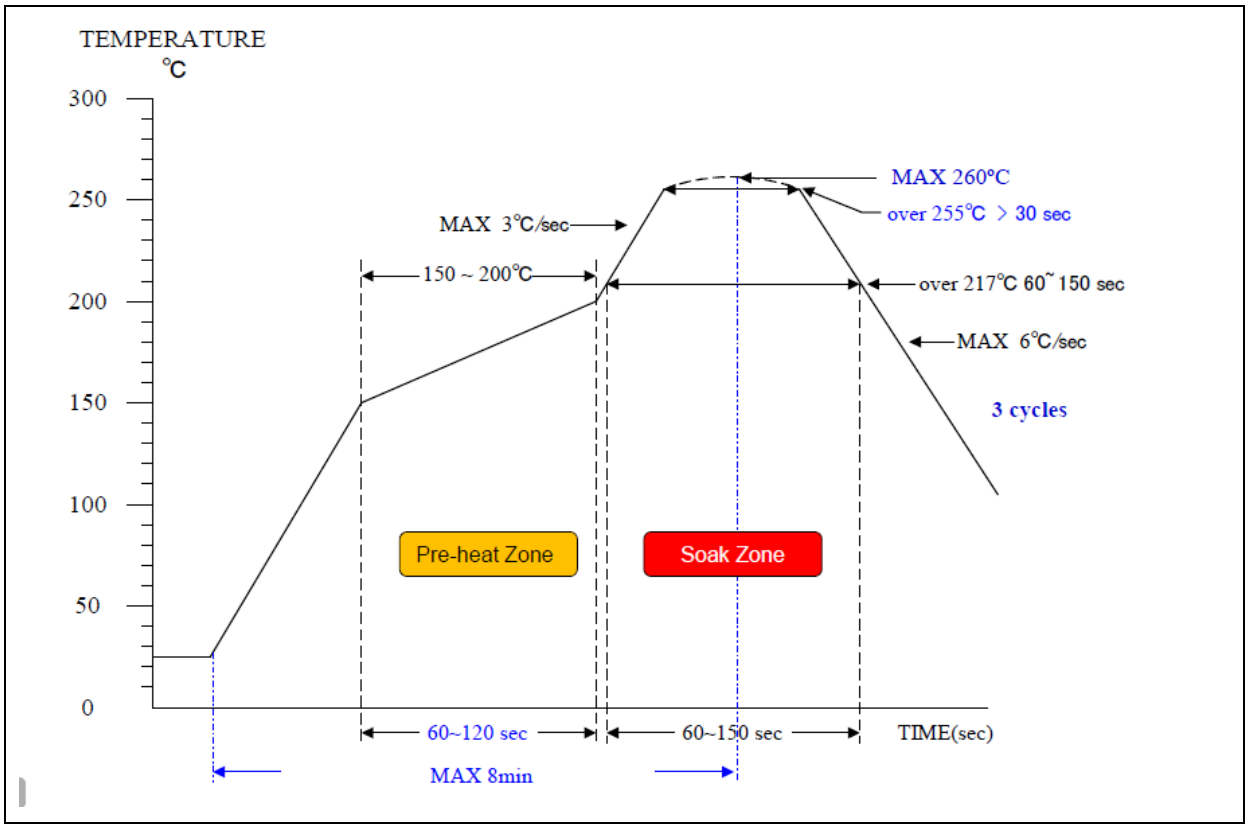


Figure 8.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1. Determined according to J-STD-020C	

Table 8.1-6 Soldering Profile

8.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.7 ~ 3.6V, T_A = 25°C, HCLK = 200 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	200	MHz	Turbo run mode with PL0 (PLSEL = 00)
V_{DD}	Operation voltage	1.7	-	3.6	V	
V_{DDIO}	V_{DDIO} Operation voltage	1.7	-	3.6		
V_{BAT}	V_{BAT} Operation voltage	1.7	-	3.6		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.7	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.26	-		
V_{BG}	Band-gap voltage	1.173	1.210	1.246	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	20	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	2.2			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	150	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.64	-	µC	V_{DD} = 1.2 V, T_A = 105 °C

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 2.2 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 8.2-1 General Operating Conditions

8.3 DC Electrical Characteristics

8.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.7 ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_RUN}	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable PLL	200 MHz	26.88	27.01	29.40	31.16	mA
		192 MHz	26.56	26.66	29.11	30.93	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT clock	180 MHz	23.66	23.76	25.95	27.58	
		160 MHz	21.62	21.68	23.81	25.43	
		144 MHz	19.10	19.18	21.16	22.73	
		120 MHz	16.08	16.12	17.98	19.50	
		96 MHz	13.71	13.76	15.65	17.14	
		84 MHz	12.10	12.18	13.95	15.42	
		72 MHz	10.51	10.55	12.26	13.71	
		60 MHz	8.89	8.94	10.55	12.03	
		50 MHz	7.56	7.59	9.17	10.61	
		24 MHz	3.84	3.89	5.36	6.73	
		12 MHz	1.78	1.79	3.17	4.51	
		6 MHz	1.09	1.10	2.45	3.77	
		4 MHz	0.87	0.88	2.20	3.53	
		2 MHz	0.63	0.64	1.97	3.29	
		1 MHz	0.51	0.52	1.84	3.18	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable LIRC or LXT clock.	32.768 kHz	0.25	0.26	1.56	2.91	
		10 kHz	0.24	0.25	1.55	2.90	

	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable PLL	200 MHz	86.54	86.71	90.48	92.99	
		192 MHz	83.85	84.08	87.83	90.41	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT clock	180 MHz	74.81	75.04	78.31	80.55	
		160 MHz	66.70	66.90	69.92	72.07	
		144 MHz	60.21	60.35	63.26	65.31	
		120 MHz	50.42	50.56	53.22	55.10	
		96 MHz	41.31	41.42	43.97	45.76	
		84 MHz	36.29	36.41	38.82	40.52	
		72 MHz	31.30	31.37	33.59	35.26	
		60 MHz	26.28	26.36	28.42	30.02	
		50 MHz	22.09	22.14	24.10	25.66	
		24 MHz	11.14	11.20	12.75	14.15	
		12 MHz	5.58	5.60	7.06	8.47	
		6 MHz	3.25	3.26	4.67	6.06	
		4 MHz	2.48	2.49	3.87	5.27	
		2 MHz	1.70	1.71	3.09	4.45	
		1 MHz	1.30	1.31	2.70	4.05	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable	32.768 kHz	0.46	0.47	1.81	3.16	
		10 kHz	0.45	0.46	1.79	3.14	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]			Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C)	T_A = 105 °C)	
I_{DD_IDLE}	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable PLL	200 MHz	7.19	7.23	8.95	10.55	mA
		192 MHz	7.62	7.68	9.51	11.14	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT clock	180 MHz	6.88	6.93	8.54	9.99	
		160 MHz	6.35	6.39	7.97	9.41	
		144 MHz	5.69	5.74	7.26	8.68	
		120 MHz	4.87	4.91	6.40	7.81	
		96 MHz	4.76	4.80	6.37	7.79	
		84 MHz	4.27	4.31	5.84	7.25	
		72 MHz	3.77	3.81	5.32	6.70	
		60 MHz	3.29	3.33	4.77	6.17	
		50 MHz	2.89	2.93	4.35	5.74	
		24 MHz	1.61	1.66	3.07	4.43	
		12 MHz	0.69	0.69	2.01	3.34	
		6 MHz	0.54	0.55	1.87	3.20	
		4 MHz	0.49	0.50	1.81	3.15	
		2 MHz	0.44	0.45	1.76	3.10	
		1 MHz	0.42	0.43	1.74	3.07	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable LIRC or LXT clock.	32.768 kHz	0.24	0.25	1.56	2.90	
		10 kHz	0.24	0.25	1.56	2.89	
	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable	200 MHz	65.24	65.37	68.52	70.75	
		192 MHz	63.41	63.56	66.74	69.03	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT clock	180 MHz	56.71	56.84	59.57	61.56	
		160 MHz	50.58	50.69	53.27	55.17	
		144 MHz	45.66	45.75	48.21	50.05	
		120 MHz	38.27	38.36	40.60	42.34	
		96 MHz	31.55	31.64	33.83	35.52	
		84 MHz	27.73	27.82	29.90	31.54	
		72 MHz	23.95	24.01	25.98	27.55	
		60 MHz	20.14	20.20	22.04	23.59	

		50 MHz	16.97	17.02	18.78	20.32	
		24 MHz	8.71	8.76	10.26	11.67	
		12 MHz	4.33	4.34	5.79	7.16	
		6 MHz	2.62	2.63	4.01	5.39	
		4 MHz	2.04	2.05	3.43	4.79	
		2 MHz	1.45	1.46	2.85	4.20	
		1 MHz	1.17	1.17	2.55	3.89	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable	32.768 kHz	0.46	0.47	1.81	3.15	
		10 kHz	0.45	0.46	1.79	3.13	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 8.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 10 kHz	Typ[*2]	Max[*3][*4]			Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_DPD}	Deep Power-down mode, all peripherals disable (LVR disabled)	-	-	0.14	0.24	1.05	2.03	µA
	Deep Power-down mode, RTC enable and run (LVR disabled)	V	-	1.06	1.24	2.23	3.29	
	Deep Power-down mode, RTC enable and run (LVR disabled)	-	V	0.48	0.61	1.47	2.46	
I_{DD_SPD}	Standby Power-down mode, all peripherals disable (No RAM retention)	-	-	0.90	1.07	2.66	4.66	
	Standby Power-down mode, all peripherals disable (16KB RAM retention)	-	-	3.32	3.60	35.50	72.80	uA
	Standby Power-down mode, all peripherals disable (32KB RAM retention)	-	-	5.60	6.06	66.26	136.52	
	Standby Power-down mode, all peripherals disable (64KB RAM retention)	-	-	9.73	10.72	123.91	255.07	
	Standby Power-down mode, all peripherals disable (128KB RAM retention)	-	-	17.94	19.81	236.20	484.76	
	Standby Power-down mode, all peripherals disable (256KB RAM retention)	-	-	17.93	19.78	236.27	485.01	
	Standby Power-down mode, RTC enable and run (No RAM retention)	V	-	1.82	2.07	3.82	5.91	

	Standby Power-down mode, RTC enable and run (No RAM retention)	-	V	1.23	1.44	3.08	5.10	uA
I_{DD_LLPD}	Low leakage Power-down mode, all peripherals disable	-	-	0.08	0.09	0.77	1.48	mA
	Low leakage Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	0.08	0.09	0.77	1.49	
	Low leakage Power-down mode, WDT /Timer use LIRC, RTC use LIRC	-	V	0.08	0.09	0.77	1.49	
	Ultra Low leakage Power-down mode, WDT/Timer use LIRC, UART /RTC use LXT	V	V	0.08	0.09	0.77	1.49	
I_{DD_PD} (PL0)	Power-down mode, all peripherals disable	-	-	0.21	0.22	1.64	3.11	mA
	Power-down mode, all peripherals disable (LVR disabled)			0.20	0.22	1.65	3.12	
	Power-down mode, RTC enable and run	V		0.21	0.22	1.65	3.12	

	Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	0.21	0.22	1.65	3.13	
	Power-down mode, WDT/Timer use LIRC, RTC use LIRC	-	V	0.21	0.22	1.66	3.13	
	Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT	V	V	0.21	0.22	1.65	3.14	
I_{DD_PD} (PL1)	Power-down mode, all peripherals disable			0.17	0.19	1.44	2.76	mA
	Power-down mode, all peripherals disable (LVR disabled)			0.17	0.19	1.44	2.77	
	Power-down mode, RTC enable and run			0.18	0.19	1.45	2.77	
	Power-down mode, WDT/Timer/UART/RTC enable and run			0.18	0.19	1.45	2.78	
	Power-down mode, WDT/Timer use LIRC, RTC use LIRC			0.18	0.19	1.45	2.78	
	Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT			0.18	0.19	1.45	2.78	
I_{DD_FWPD} (PL0)	Fast wake up Power-down mode, all peripherals disable	-	-	0.27	0.28	1.68	3.08	mA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	0.27	0.29	1.69	3.11	

	Fast wake up Power-down mode, WDT/Timer use LIRC, RTC use LIRC	-	V	0.27	0.28	1.69	3.12	
	Fast wake up Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT	V	V	0.27	0.28	1.70	3.14	
I_{DD_FWPD1} (PL1)	Fast wake up Power-down mode, all peripherals disable			0.24	0.25	1.49	2.79	mA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run			0.24	0.25	1.50	2.80	
	Fast wake up Power-down mode, WDT/Timer use LIRC, RTC use LIRC			0.24	0.25	1.50	2.81	
	Fast wake up Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT			0.24	0.25	1.50	2.82	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L7 gain level. → AE should list test condition.
2. $V_{DD} = AV_{DD} = V_{BAT} =$ 3.3V, LVR enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, DAC, ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 8.3-3 Chip Current Consumption in Power-Down Mode

8.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{BAT} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 200 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA0	7344	uA
ISP	~0	
EBI	605	
ST	267	
EMAC0	653	
SDH0	4890	
CRC	331	
CCAP	655	
SEN	655	
HSUSBD[*3]	3049	
HBI	348	
CRPT	2174	
KS	1001	
SPIM	653	
FMCIDLE	1738	
USBH[*3]	8873	
SDH1	1172	
TRACE	~0	
GPA	169	
GPB	139	
GPC	140	
GPD	117	
GPE	159	
GPF	138	
GPG	146	
GPH	138	
WDT	615	
RTC	454	

TMR0	687	
TMR1	697	
TMR2	695	
TMR3	677	
CLKO	756	
ACMP01[*2]	622	
I2C0	397	
I2C1	428	
I2C2	398	
I2C3	425	
QSPI0	1600	
SPI0	1429	
SPI1	1441	
SPI2	1453	
UART0	1299	
UART1	1306	
UART2	1248	
UART3	1268	
UART4	1258	
UART5	1261	
UART6	1250	
UART7	1267	
OTG[*3]	856	
USBD[*3]	830	
EADC0[*1]	3043	
I2S0	886	
HSOTG	1007	
SC0	1006	
I2C4	398	
QSPI1	1559	
SPI3	1467	
SPI4	1361	
USCI0	490	
PSIO	2029	
DAC[*4]	371	

ECAP2	347	
ECAP3	370	
EPWM0	776	
EPWM1	766	
BPWM0	460	
BPWM1	479	
EQEI2C	346	
EQEI3C	370	
EQEI0	457	
EQEI1	481	
TRNG	666	
ECAP0	490	
ECAP1	514	
I2S1	903	
EADC1[*1]	853	
KPI	1051	
EADC2[*1]	489	
ACMP23[*2]	401	
UART8	530	
UART9	529	
CANFD0	4475	
CANFD1	4499	
CANFD2	680	
CANFD3	682	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 8.3-4 Peripheral Current Consumption

8.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 8.3-5 is measured on a wakeup phase with a 12 MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	10	-	cycles
t_{WU_DPD}[*1][*2] [*3]	Wakeup from Deep Power-down mode	11.428	-	mS
t_{WU_SPD}[*1][*2]	Wakeup from Standby Power-down mode	176.003	-	µS
t_{WU_LLPD}[*1][*2]	Wakeup from Low leakage Power-down mode	51.035	-	
t_{WU_NPD}[*1][*2]	Wakeup from Normal Power-down mode	10.102	-	
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	7.357	-	
t_{ET_IDLE}	Enter to IDLE mode	17	-	cycles
t_{ET_DPD}	Enter to Deep Power-down mode	59.042	-	µS
t_{ET_SPD}	Enter to Standby Power-down mode	55.042	-	
t_{ET_LLPD}	Enter to Low leakage Power-down mode	1.305	-	
t_{ET_NPD}	Enter to Normal Power-down mode	1.388	-	
t_{ET_FWPD}	Enter to fast wake up Power-down mode	1.383	-	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. CONFIG3[12:8] =0x1F with MKROM-ISP function. CONFIG3[12:8] =0x2 without MKROM-ISP function.

Table 8.3-5 Low-Power Mode Wakeup Timings

8.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 8.3-6 I/O Current Injection Characteristics

8.3.5 I/O DC Characteristics

8.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min[*2]	Typ[*1]	Max[*2]	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-			V_{DD} = 3.0 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.7 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 3.6 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1.0	-	V_{DD}		V_{DD} = 1.7V
V_{HY}	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*3]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 3.3 V, Open-drain or input only mode on any other 3.3V tolerance pins
R_{PU}	Pull up resistor	43	51	60	kΩ	VDD=3.6V
R_{PD}	Pull down resistor	43	51	60	kΩ	VDD=3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design result, not tested in production.
3. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 8.3-7 I/O Input Characteristics

8.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	6.66	7.74	9.50	μA	V_{DD} = 3.0V V_{IN}=(V_{DD}-0.4) V
		6.64	7.71	9.46	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		6.53	7.56	9.25	μA	V_{DD} = 1.7 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	13.52	17.51	23.16	mA	V_{DD} = 3.0V V_{IN}=(V_{DD}-0.4) V
		12.33	15.92	21.57	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		7.12	9.85	13.20	mA	V_{DD} = 1.7 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	-12.97	-16.65	-24.45	mA	V_{DD} = 3.0V V_{IN}= 0.4 V
		-11.96	-15.71	-23.40	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		-6.83	-9.55	-15.03	mA	V_{DD} = 1.7 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	4.64	4.73	4.82	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 8.3-8 I/O Output Characteristics

8.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	41	54	60	kΩ	VDD=3.6V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	µS	Normal run and Idle mode
		-	32	-		Fast wake up Power-down mode
		-	32	-		Power-down mode
		-	32	-		Low leakage Power-down mode
		-	0	-		Standby Power-down mode
		-	0	-		Deep Power-down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 8.3-9 nRESET Input Characteristics

8.4 AC Electrical Characteristics

8.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

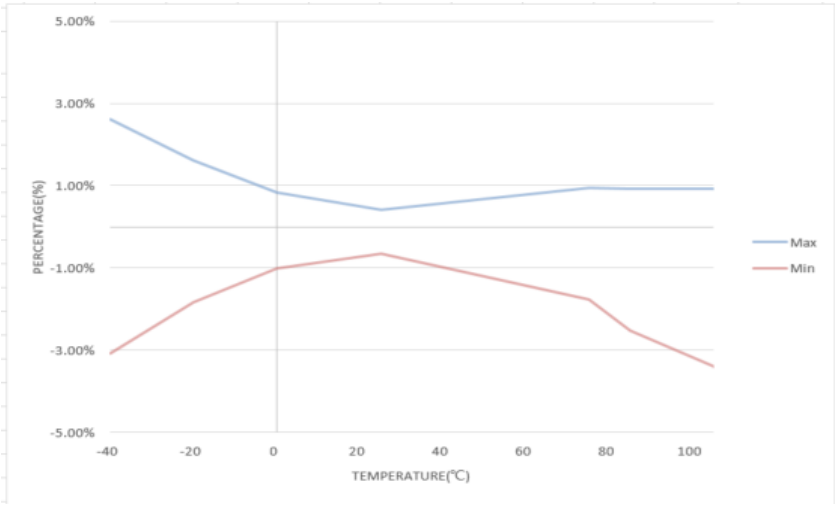
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-4	-	+4	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7~3.6V
I_{HRC}[*1]	Operating current	-	100	230	μA	
T_S[*2]	Stable time	-	-	5	μS	T_A = -40°C ~ +105 °C, V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-1.

Figure 8.4-1 HIRC48 vs. Temperature

8.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

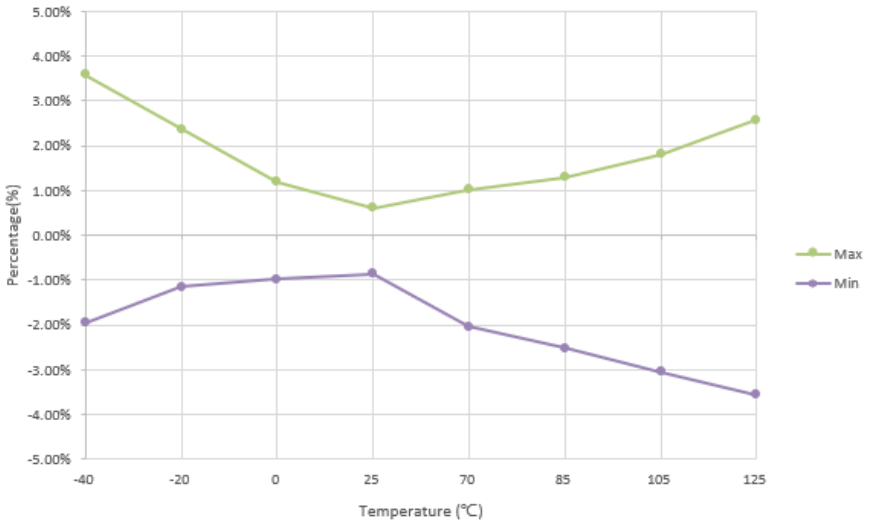
The 12 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
f_{HRC}	Oscillator frequnecy	11.88	12	12.12	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-3	-	+3	%	T_A = -40°C ~ +85 °C, V_{DD} = 1.7~3.6V
		-4	-	+4	%	T_A = -40°C ~ +105 °C, V_{DD} = 1.7~3.6V
I_{HRC}[*1]	Operating current	-	70		μA	
T_S[*2]	Stable time	-	-	20	μS	T_A = -40°C ~ +105 °C, V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 8.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-2.

Figure 8.4-2 HIRC vs. Temperature

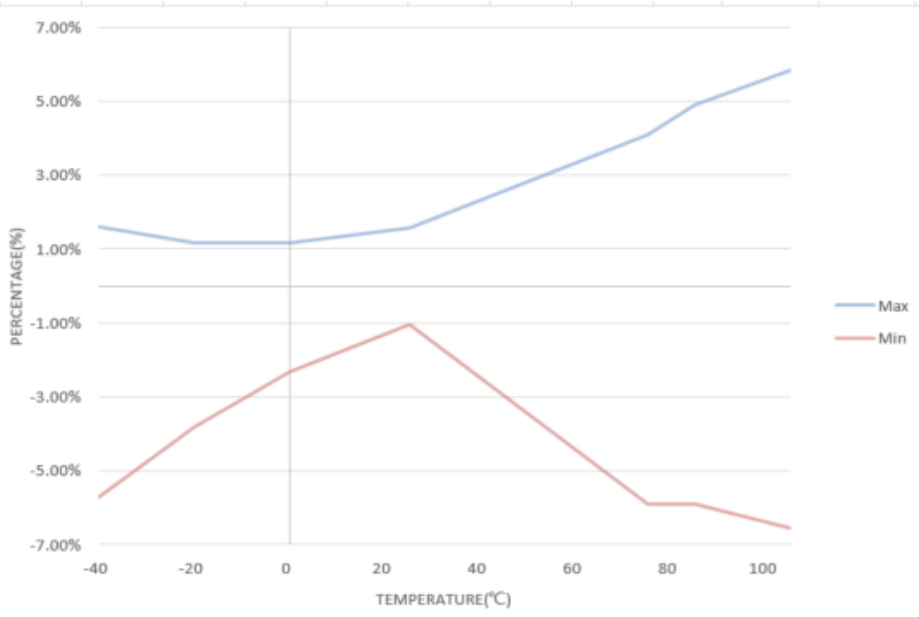
8.4.3 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	10	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~105°C V_{DD} = 1.7~3.6V
I_{LRC}	Operating current	-	0.5	0.7	µA	V_{DD} = 3.3V
T_S	Stable time	-	-	500 [*3]	µS	T_A=-40~105°C V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. The 10 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 8.4-3 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 8.4-3.

Figure 8.4-3 LIRC vs. Temperature

8.4.4 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
R_f	Internal feedback resister	-	1	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	200	250	300	µA	4 MHz, Gain = L0, C_L = 12.5 pF
		350	400	450		12 MHz, Gain = L1, C_L = 12.5 pF
		450	500	550		16 Mhz, Gain = L2, C_L = 12.5 pF
		600	640	700		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time	1300	1800	2000	µS	4 MHz, Gain = L0, C_L = 12.5 pF
		458	479	600		12 MHz, Gain = L1, C_L = 12.5 pF
		340	400	500		16 Mhz, Gain = L2, C_L = 12.5 pF
		230	250	400		24 MHz, Gain = L3, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	$0.3V_{DD}$	$0.5V_{DD}$	$0.7V_{DD}$	V	

Notes:
1. Guaranteed by design, not tested in production.

Table 8.4-4 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	30		Crystal @12 MHz, C_L = 12.5 pF, Gain = L1
		-	-	30		Crystal @16 MHz, C_L = 12.5 pF, Gain = L2
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L3

Notes:

1. Guaranteed by design, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

$$S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$$

R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

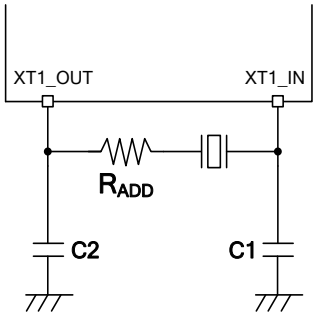


Table 8.4-5 External 4~24 MHz High Speed Crystal Characteristics

8.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

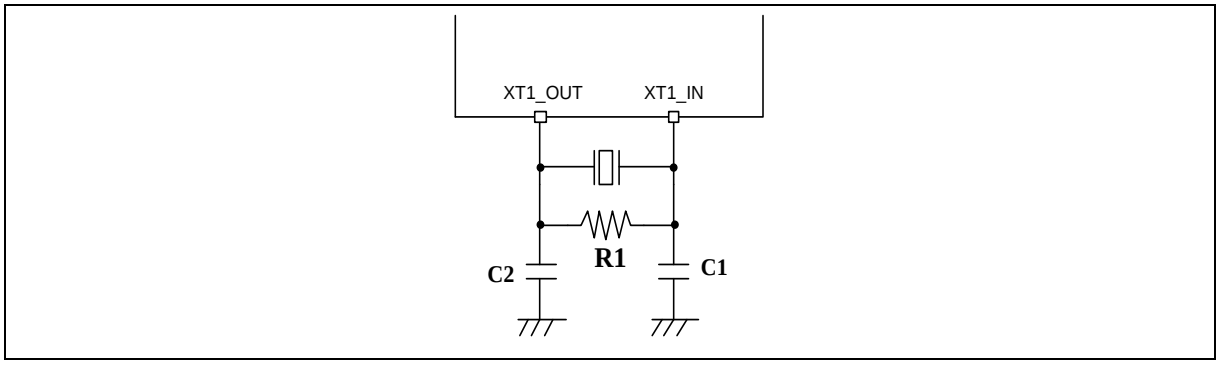
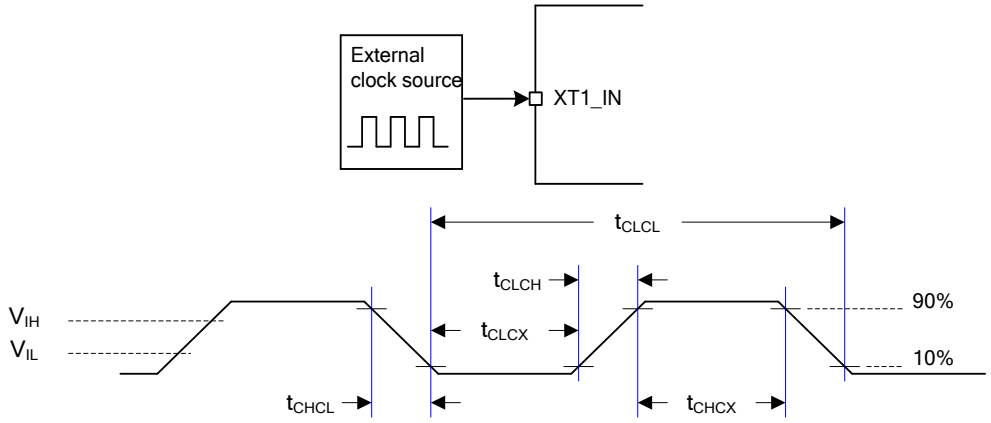


Figure 8.4-6 Typical Crystal Application Circuit

8.4.5 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	XT1_IN should be set as Schmitter Trigger
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by design, not tested in production.

Table 8.4-7 External 4~24 MHz High Speed Clock Input Signal

8.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BAT}	Operation voltage	1.62	-	3.6	V	
T_{LXT}	Temperature range	-40	-	105	°C	
R_f	Internal feedback resistor	-	8	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	130	270	750	nA	ESR=35 kΩ, C_L =12 pF, Gain= L1
		160	350	850		ESR=35 kΩ, C_L= 12 pF, Gain= L2
		195	390	960		ESR=35 kΩ, C_L= 20 pF, Gain= L3
		230	450	1060		ESR=35 kΩ, C_L= 20 pF, Gain= L4
		300	560	1300		ESR=70 kΩ, C_L= 20 pF, Gain= L5
		370	680	1500		ESR=70 kΩ, C_L= 20 pF, Gain= L6
		500	920	1950		ESR=70 kΩ, C_L= 20 pF, Gain= L7
Ts_{LXT}	Stable time	1	-	2	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.35	0.5	-	V	

Notes:

1. Guaranteed by design, not tested in production.

Table 8.4-8 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 8.4-9 External 32.768 kHz Low Speed Crystal Characteristics

8.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

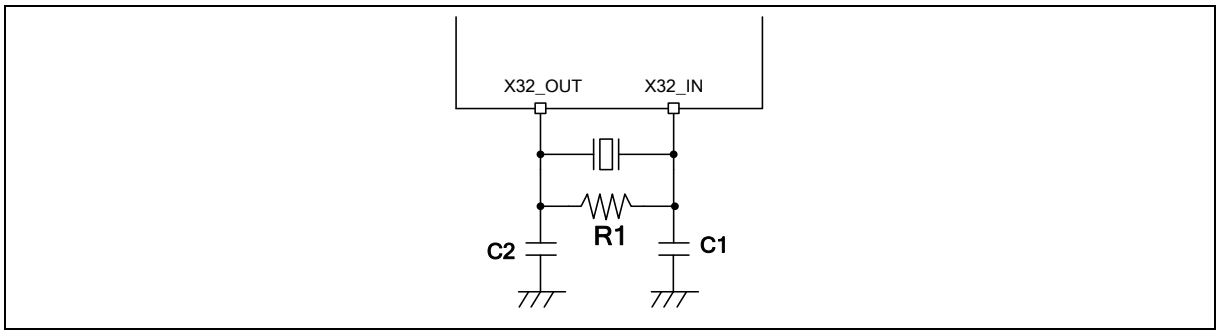
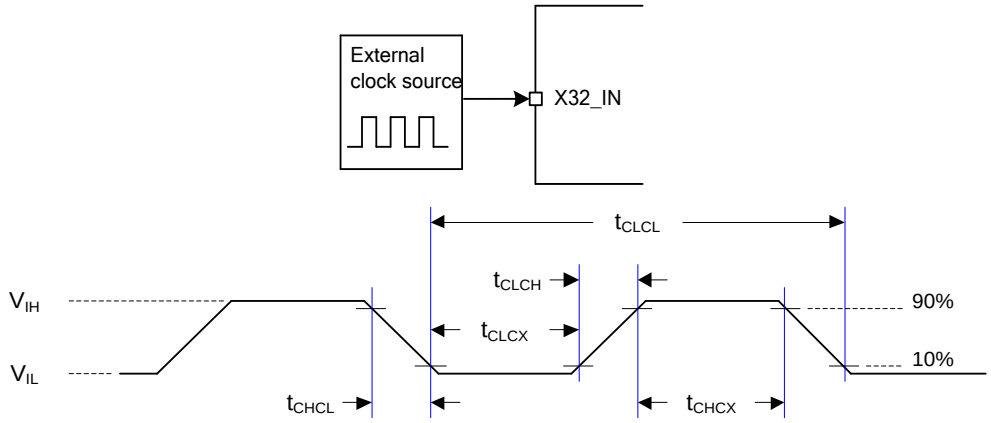


Figure 8.4-10 Typical 32.768 kHz Crystal Application Circuit

8.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	X32_IN should be set as Schmitter Trigger
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1. Guaranteed by design, not tested in production

Table 8.4-11 External 32.768 kHz Low Speed Clock Input Signal

8.4.8 Fractional PLL Characteristics

Symbols	Parameter	Min.	Typ.	Max.	Units	Test Condition
IV_{DD}	Operating current@500MHz		2.0	2.6	mA	Does not contain clock filter current
CLK_IN	Input Clock Frequency	1		24	MHz	
Fref	Input Reference Frequency(Fref=CLK_IN/M)	1		8	MHz	
OUT_PLL	Output Frequency (OUT_PLL=Fvco/R)	25		500	MHz	
Fvco[*1]	VCO Output Frequency Fvco = CLK_IN*(2*N/M) N range : 12~255	200		500	MHz	
Jitter[*2] (peak-peak)	200MHz		250		ps	
	500MHz		250		ps	
Lock time	Form PLL_EN to OUT_PLL with clock time			200	us	
TJ	Operating junction temperature	-40	25	125	˚C	

Notes:
1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

8.4.9 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	500	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}[*1]	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	100	µS	
Jitter[*2]	Cycle-to-cycle Jitter	-	250	-	pS	
I_{DD}	Power consumption	2.7	3.25	3.3	mA	VDD=3.6V @ f_{PLL_VCO} = 500 MHz

Notes:
1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production

Table 8.4-12 PLL Characteristics

8.4.10 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	3.27	4.93	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		2.2	3.08		C_L = 10 pF, V_{DD} >= 3.0 V
		3.52	5.48		C_L = 30 pF, V_{DD} >= 2.7 V
		2.37	3.46		C_L = 10 pF, V_{DD} >= 2.7 V
		7.03	10.01		C_L = 30 pF, V_{DD} >= 1.7 V
		4.83	6.52		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	2.58	3.63		C_L = 30 pF, V_{DD} >= 3.0 V
		1.40	1.85		C_L = 10 pF, V_{DD} >= 3.0 V
		2.78	3.98		C_L = 30 pF, V_{DD} >= 2.7 V
		1.54	2.05		C_L = 10 pF, V_{DD} >= 2.7 V
		4.59	6.91		C_L = 30 pF, V_{DD} >= 1.7 V
		2.99	3.63		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (Fast Slew Rate)	2.60	3.61		C_L = 30 pF, V_{DD} >= 3.0 V
		1.40	1.81		C_L = 10 pF, V_{DD} >= 3.0 V
		2.82	3.95		C_L = 30 pF, V_{DD} >= 2.7 V
		1.48	2.01		C_L = 10 pF, V_{DD} >= 2.7 V
		4.72	6.86		C_L = 30 pF, V_{DD} >= 1.7 V
		2.72	3.57		C_L = 10 pF, V_{DD} >= 1.7 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	3.43	5.21	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		2.38	3.46		C_L = 10 pF, V_{DD} >= 3.0 V
		3.69	5.75		C_L = 30 pF, V_{DD} >= 2.7 V
		2.61	3.84		C_L = 10 pF, V_{DD} >= 2.7 V
		6.71	10.08		C_L = 30 pF, V_{DD} >= 1.7 V

		4.88	6.81		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	2.27	3.12	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		1.26	1.57		C_L = 10 pF, V_{DD} >= 3.0 V
		2.46	3.45		C_L = 30 pF, V_{DD} >= 2.7 V
		1.39	1.76		C_L = 10 pF, V_{DD} >= 2.7 V
		4.13	6.15		C_L = 30 pF, V_{DD} >= 1.7 V
		2.34	3.24		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (Fast Slew Rate)	2.31	3.11	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		1.28	1.56		C_L = 10 pF, V_{DD} >= 3.0 V
		2.50	3.45		C_L = 30 pF, V_{DD} >= 2.7 V
		1.37	1.76		C_L = 10 pF, V_{DD} >= 2.7 V
		4.11	6.15		C_L = 30 pF, V_{DD} >= 1.7 V
		2.28	3.23		C_L = 10 pF, V_{DD} >= 1.7 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	99.50	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		145.56	-		C_L = 10 pF, V_{DD} >= 3.0 V
		92.46	-		C_L = 30 pF, V_{DD} >= 2.7 V
		133.87	-		C_L = 10 pF, V_{DD} >= 2.7 V
		48.52	-		C_L = 30 pF, V_{DD} >= 1.7 V
		68.66	-		C_L = 10 pF, V_{DD} >= 1.7 V
	I/O maximum frequency (High Slew Rate)	137.46	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		250.63	-		C_L = 10 pF, V_{DD} >= 3.0 V
		127.23	-		C_L = 30 pF, V_{DD} >= 2.7 V
		227.53	-		C_L = 10 pF, V_{DD} >= 2.7 V
		76.45	-		C_L = 30 pF, V_{DD} >= 1.7 V
		125.08	-		C_L = 10 pF, V_{DD} >= 1.7 V

	I/O maximum frequency (Fast Slew Rate)	135.78	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		248.76	-		C_L = 10 pF, V_{DD} >= 3.0 V
		125.31	-		C_L = 30 pF, V_{DD} >= 2.7 V
		233.92	-		C_L = 10 pF, V_{DD} >= 2.7 V
		75.50	-		C_L = 30 pF, V_{DD} >= 1.7 V
		133.33	-		C_L = 10 pF, V_{DD} >= 1.7 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Notes:

1. Guaranteed by design result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 8.4-13 I/O AC Characteristics

8.5 Analog Characteristics

8.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.7	-	3.6	V	
V_{LDO}	Output voltage	0.9	1.26	1.32	V	
T_A	Temperature	-40	-	105	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.
3. V_{LDO} is only used to supply internal power.

8.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	35	45	µA	V_{DD}=AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	0.3	0.6		V_{DD}=AV_{DD} = 3.6V
I_{BOD}[*1]	BOD operating current	-	30	40		V_{DD}=AV_{DD} = 3.6V, Normal mode
		-	1	-		V_{DD}=AV_{DD} = 3.6V, Low Power mode
V_{POR}	POR reset voltage (Rising edge)	1.4	1.49	1.57	V	
	POR reset voltage (Falling edge)	1.38	1.46	1.54		
V_{LVR}	LVR reset voltage (Rising edge)	1.45	1.5	1.6		
	LVR reset voltage (Falling cedge)	1.4	1.5	1.55		
V_{BOD}	BOD brown-out detect voltage (Rising edge)	1.60	1.70	1.80		BODVL = 0
		1.80	1.90	2.00		BODVL = 1
		2.00	2.10	2.20		BODVL = 2
		2.20	2.30	2.40		BODVL = 3
		2.40	2.50	2.60		BODVL = 4
		2.60	2.70	2.80		BODVL = 5
		2.80	2.90	3.00		BODVL = 6
		3.00	3.10	3.20		BODVL = 7
	BOD brown-out detect voltage (Falling edge)	1.50	1.60	1.70		BODVL = 0
		1.70	1.80	1.90		BODVL = 1
		1.90	2.00	2.10		BODVL = 2
		2.10	2.20	2.30		BODVL = 3
		2.30	2.40	2.50		BODVL = 4
		2.50	2.60	2.70		BODVL = 5
		2.70	2.80	2.90		BODVL = 6
		2.90	3.00	3.10		BODVL = 7
T_{LVR_SU}[*2]	LVR startup time	-	-	256	µS	Normal mode
		-	-	512		Low Power mode
T_{LVR_RE}[*1]	LVR respond time	-	1	2		Normal mode
		-	20	100		Low Power mode
T_{BOD_SU}[*2]	BOD startup time	-	1000	-		-
T_{BOD_RE}[*1]	BOD respond time	-	10	-		Normal mode
		-	20000	-		Low Power mode
R_{VDDR}[*1]	VDD rise time rate	-	10	-	µS/V	POR Enabled

R_{VDDF}[*1]	VDD fall time rate	-	10	-		POR Enabled
		-	0.66-	-		LVR Enabled
		-	133	-		LVRLP Enabled
		-	66.67	-		BOD 1.6V Enabled, Normal mode
		-	28.57	-		BOD 1.8V Enabled, Normal mode
		-	18.18	-		BOD 2.0V Enabled, Normal mode
		-	13.33	-		BOD 2.2V Enabled, Normal mode
		-	10.53	-		BOD 2.4V Enabled, Normal mode
		-	8.70	-		BOD 2.6V Enabled, Normal mode
		-	7.41	-		BOD 2.8V Enabled, Normal mode
		-	6.45	-		BOD 3.0V Enabled, Normal mode
		-	133333.3	-		BOD 1.6V Enabled, Low Power mode
		-	57142.86	-		BOD 1.8V Enabled, Low Power mode
		-	36363.64	-		BOD 2.0V Enabled, Low Power mode
		-	26666.67	-		BOD 2.2V Enabled, Low Power mode
		-	21052.63	-		BOD 2.4V Enabled, Low Power mode
		-	17391.3	-		BOD 2.6V Enabled, Low Power mode
		-	14814.81	-		BOD 2.8V Enabled, Low Power mode
		-	12903.23	-		BOD 3.0V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 8.5-1 Reset and Power Control Unit

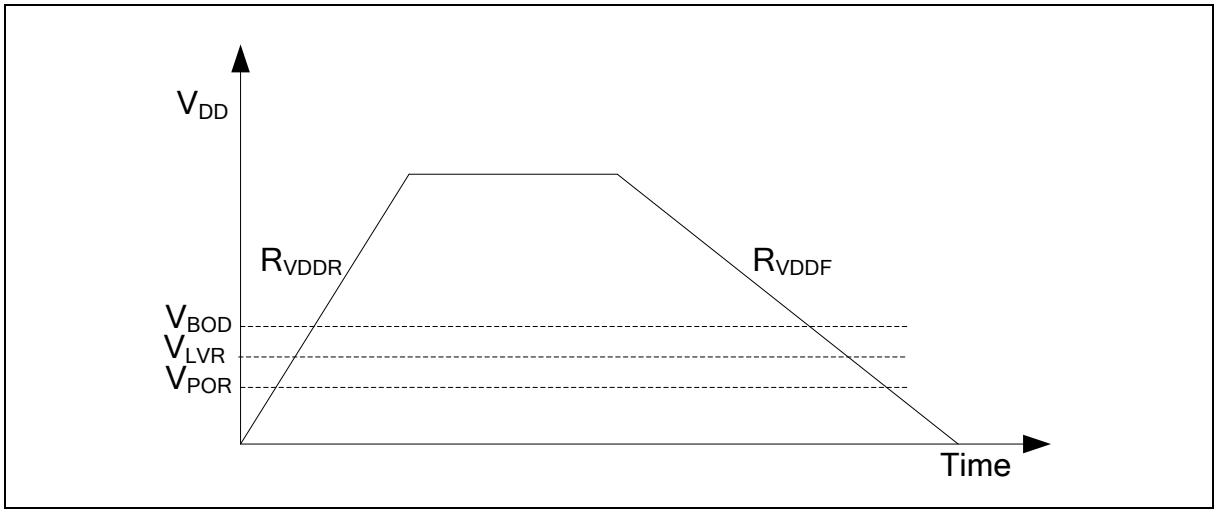


Figure 8.5-1 Power Ramp Up/Down Condition

8.5.3 12-bit SAR Analog To Digital Converter (ADC)

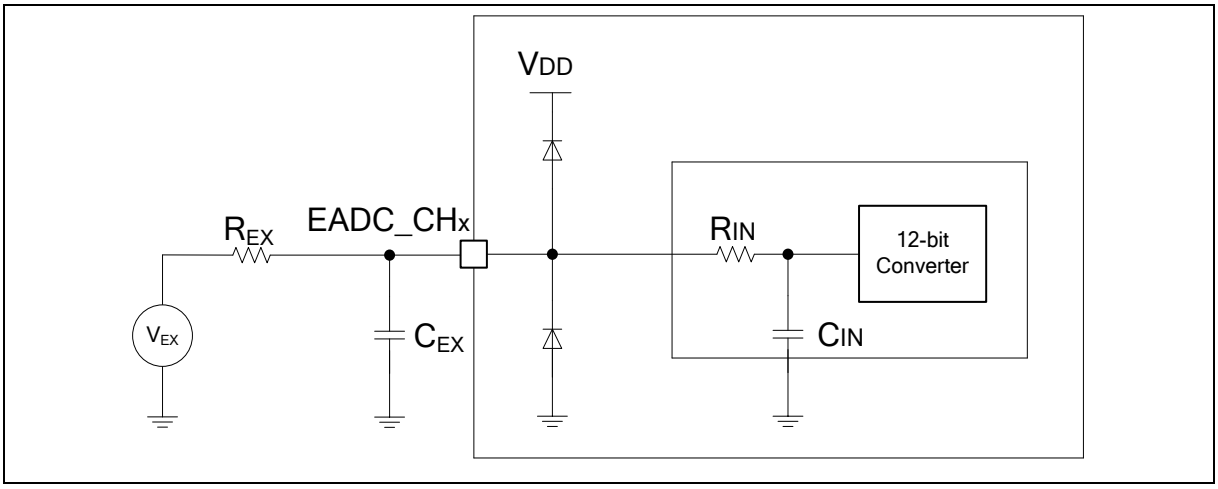
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	105	℃	
AV_{DD}	Analog operating voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	330	-	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 90 MHz $T_{CONV} = 20 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	12	-	60	MHz	1.7V ≦ V_{REF} ≦ 3.6V
		12	-	90	MHz	2.5V ≦ V_{REF} ≦ 3.6V
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	20	-	275	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 19 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	0.6	-	3	MSPS	1.7V ≦ V_{REF} ≦ 3.6V $F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(EADC_SCTLx[31:24]) = 0
		0.6	-	4.5	MSPS	2.5V ≦ V_{REF} ≦ 3.6V $F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(EADC_SCTLx[31:24]) = 0
T_{EN}	Enable to ready time	5	-	-	$1/F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-4	-	+3	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-5	-	+6	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	10.0	-	bits	F_{ADC} = 90 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	60.2	-	dB	
SNR[*1]	Signal-to-noise ratio	-	60.2	-		
THD[*1]	Total harmonic distortion	-	-74	-		

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}[*1]	Internal Capacitance	-	2.9	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	500	Ω	
R_{EX}[*1]	External input impedance	-	-	23	kΩ	F_{ADC} = 90 MHz T_{SMP} = 275/F_{ADC} T_A = 25 °C

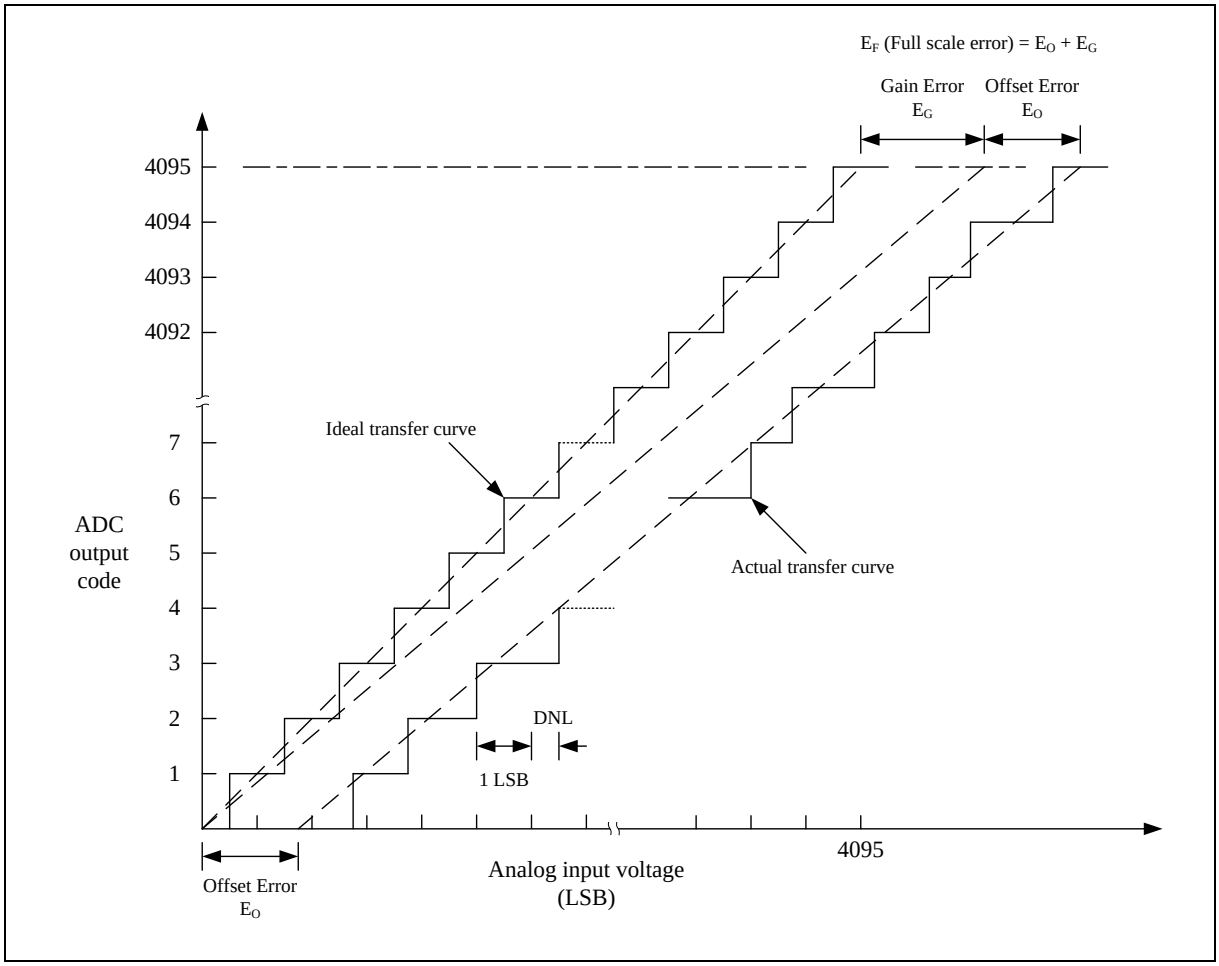
Notes:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

8.5.4 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	-
N_R	Resolution		12		bit	-
V_{REF}	Reference supply voltage	1.5	-	3.6	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error	-2	-	2	LSB	12-bit mode
INL[*2]	Integral non-linearity error	-4	-	4	LSB	12-bit mode
OE[*2]	Offset Error	-8	-	8	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
GE[*2]	Gain Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
AE[*2]	Absolute Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
V_O[*1]	Output Voltage	0.2		AVDD-0.2	V	DACOUT buffer ON
		1 LSB		VREF – 1 LSB		DACOUT buffer OFF
R_{LOAD}[*2] [*3]	Resistive load	7.5	-	-	kΩ	DACOUT buffer ON
R_O[*2]	Output impedance	-	9.8	-	kΩ	DACOUT buffer OFF
C_{LOAD}[*2] [*4]	Capacitive load	-	-	20	pF	DACOUT buffer OFF
I_{DAC_AVDD}[*2]	DAC operating current on AV_{DD} supply	-	132	-	μA	AV_{DD} = 3.6V, no load, lowest code (0x000)
		-	338	-		AV_{DD} = 3.6V, no load, middle code (0x800)
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	130	140	μA	V_{REF} =3.6V, no load, middle code (0x800)
T_B[*2]	Settling Time	-	5	6	μs	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB,

						C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5kΩ
F_S	Update Rate	-	-	1	M_{SPS}	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5kΩ
T_{WAKEUP}	Wake-up Time	-	5	10	µs	Wakeup time from OFF state. Input code between lowest and highest possible codes. DAC clock source = 1MHz
PSRR[*1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

8.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	V_{DD} = AV_{DD}
T_A	Temperature	-40	-	105	℃	
I_{ACMP}[*2]	ACMP operating current	-	70	-	μA	MODESEL = 11
		-	35	-		MODESEL = 10
		-	2	-		MODESEL = 01
		-	1	-		MODESEL = 00
V_{CM}[*2]	Input common mode voltage range	0.1	1/2 AV_{DD}	AV_{DD} -0.1		
V_{DI}[*2]	Differential input voltage sensitivity	20	-	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	±5	±10	mV	MODESEL =10~11 Hysteresis disable (HYSSEL = 00)
		-	±10	±20	mV	MODESEL =00~01 Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	60		HYSSEL = 100
A_v[*1]	DC voltage Gain	51	70	-	dB	
T_d[*2]	Propagation delay	-	30	60	nS	MODESEL = 11
		-	100	150		MODESEL = 10
		-	0.8	2	μS	MODESEL = 01
		-	1.5	3.5		MODESEL = 00
T_{Setup}[*2]	Setup time	-	-	1	μS	MODESEL = 11
		-	-	1		MODESEL = 10
		-	-	20		MODESEL = 01
		-	-	20		MODESEL = 00
A_{CRV}[*2]	CRV output voltage	-1.6	-	1.6	%	AVDD x (1/6+CRVCTL/24)
T_{SETUP_CRV}[*2]	Setup time	-	-	0.6	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	50	μA	

Notes:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production

Table 8.5-2 ACMP Characteristics

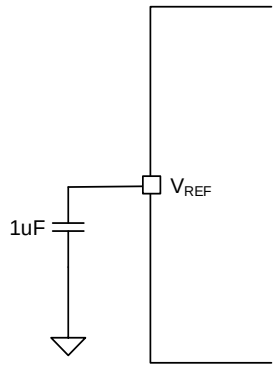
8.5.6 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	1.584	1.6	1.616	V	AV_{DD} >= 2.0 V
		1.980	2.0	2.020		AV_{DD} >= 2.2 V
		2.475	2.5	2.525		AV_{DD} >= 2.7 V
		2.970	3.0	3.030		AV_{DD} >= 3.2 V
T_S[*1]	Stable time	-	-	2	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	-	48	uS	C_L =0.1 uF, V_{REF} initial=0, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	70	-	uA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 8.5-2 Typical Connection with Internal Voltage Reference

8.5.7 Temperature Sensor

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	653	674	694	mV	T_A = 25°C
T_C[*1]	Temperature Coefficient	-1.91	-1.82	-1.73	mV/°C	
T_S[*2]	Stable time	-	-	1	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	3	-	-	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	25	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

8.6 Communications Characteristics

8.6.1 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.3	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

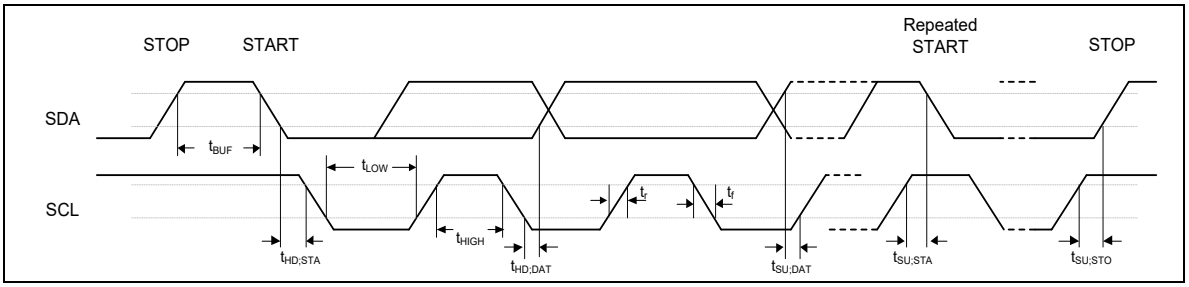


Figure 8.6-1 I²C Timing Diagram

8.6.2 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	3.0 V ≤ VD ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	2	nS	3.0 V ≤ VDD ≤ 3.6V, C_L = 30 pF

Note:

1. Guaranteed by design, not tested in production.

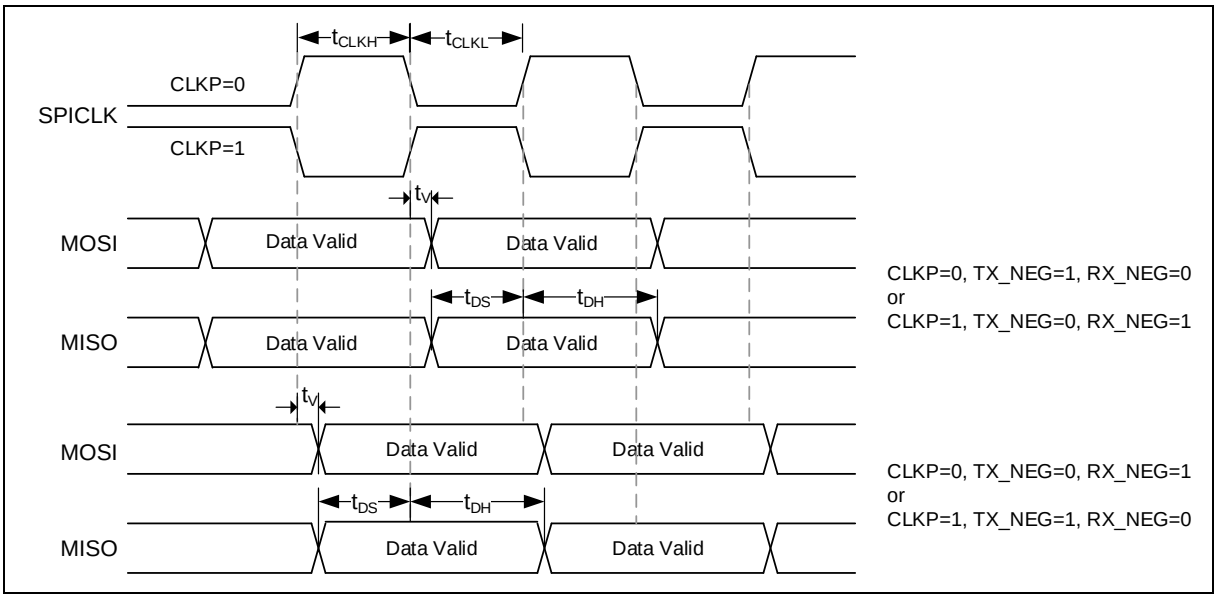


Figure 8.6-2 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	20	MHz	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	6	-	-	nS	
t_V	Data output valid time	-	-	13	nS	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

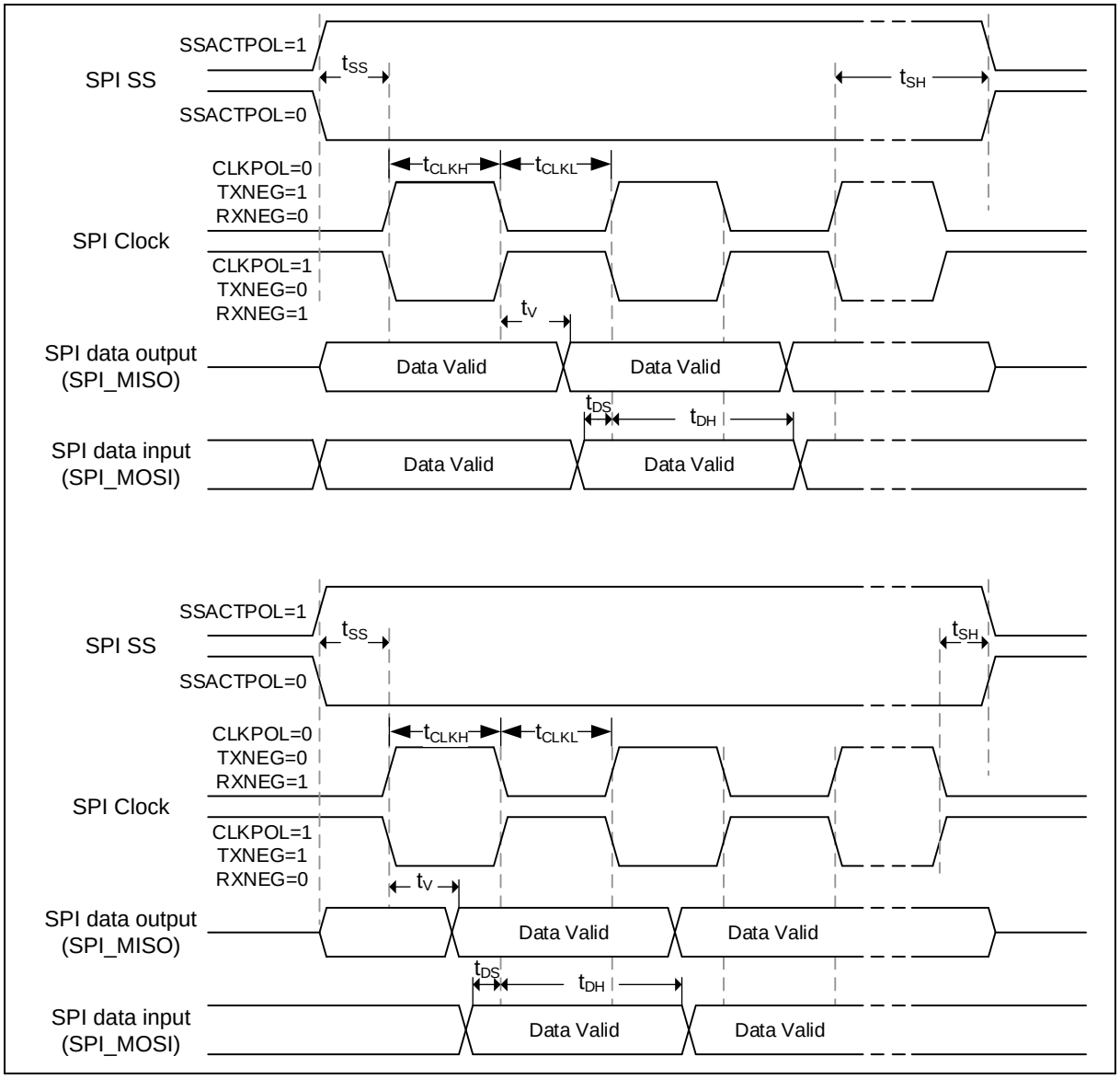


Figure 8.6-3 SPI Slave Mode Timing Diagram

8.6.3 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	16		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

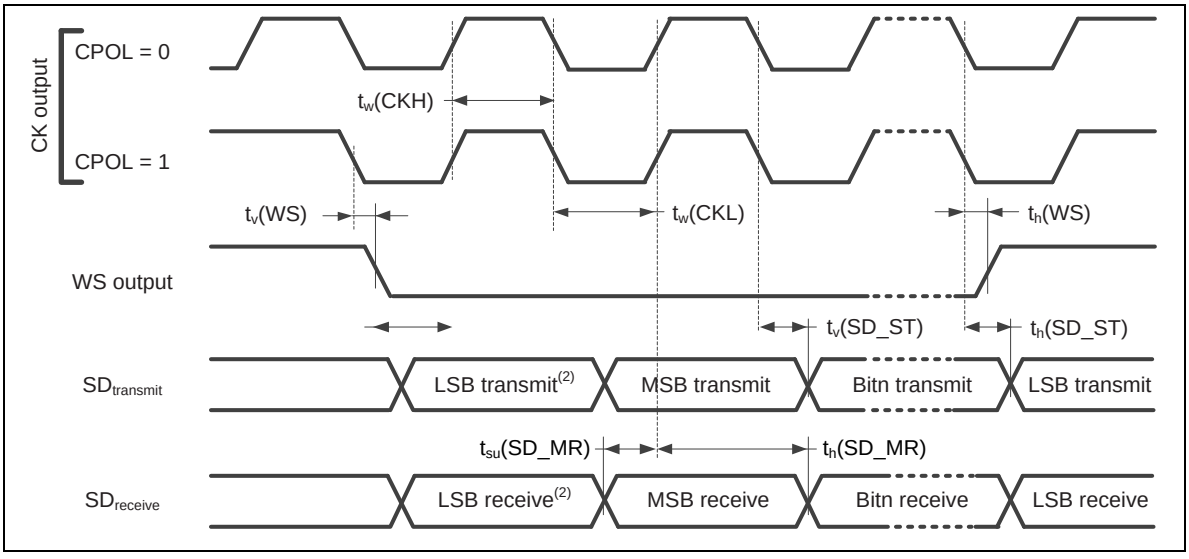


Figure 8.6-4 I²S Master Mode Timing Diagram

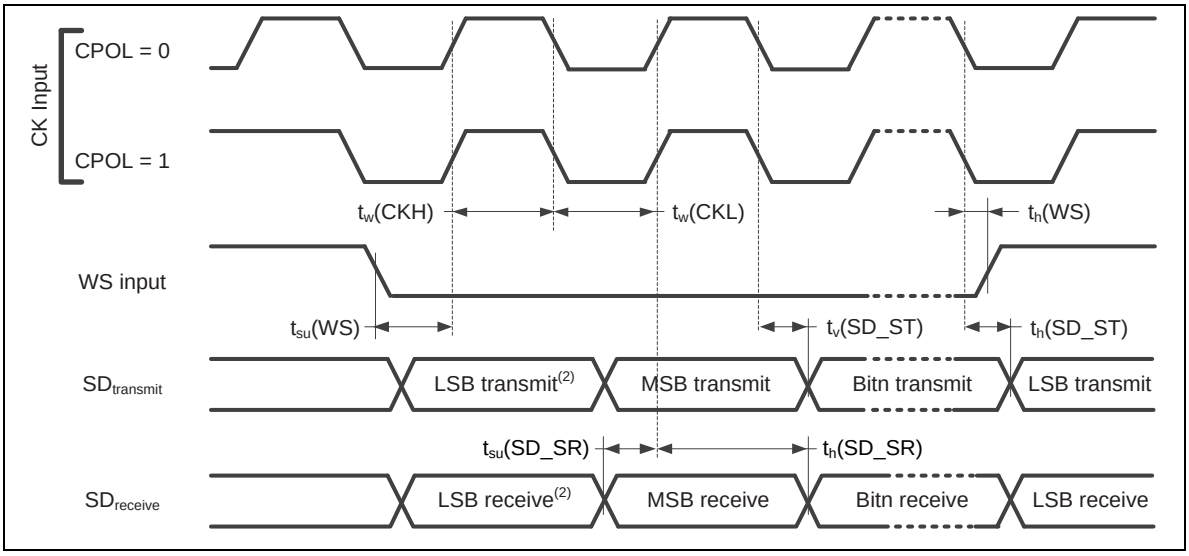


Figure 8.6-5 I²S Slave Mode Timing Diagram

8.6.4 USCI - I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

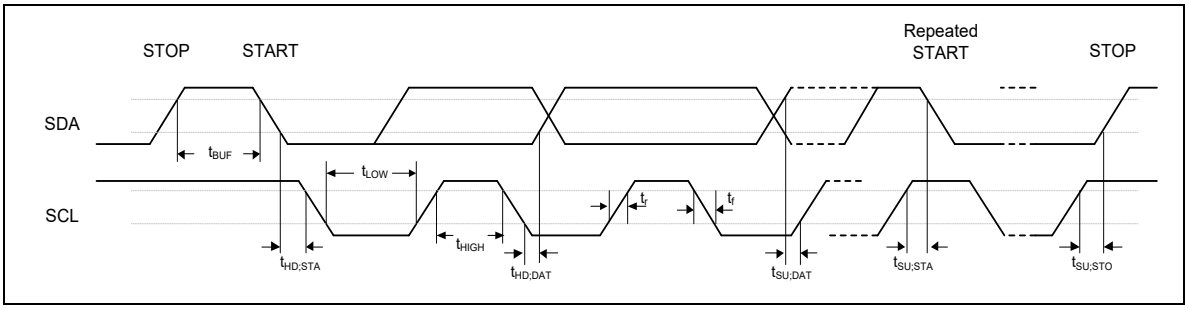


Figure 8.6-6 I²C Timing Diagram

8.6.5 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI MASTER MODE (V_{DD} = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns
SPI MASTER MODE (V_{DD} = 1.8~2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	-	1	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

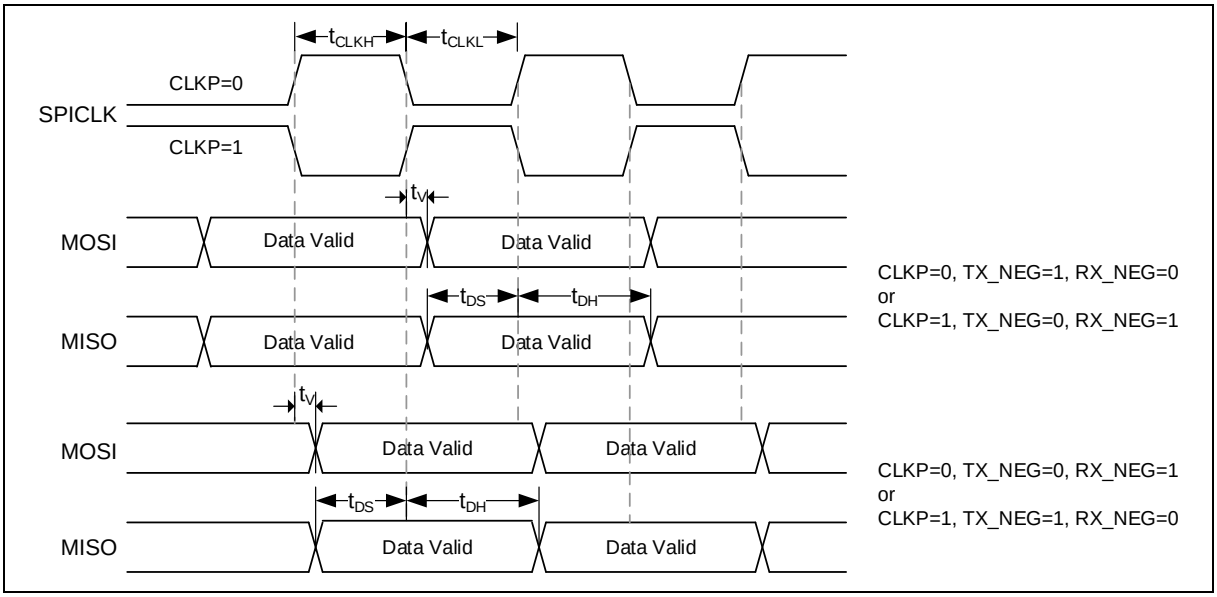


Figure 8.6-7 SPI Master Mode Timing Diagram

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI SLAVE MODE (V_{DD} = 3.0~3.6V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-		T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		8	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
SPI SLAVE MODE (V_{DD} = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		10	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

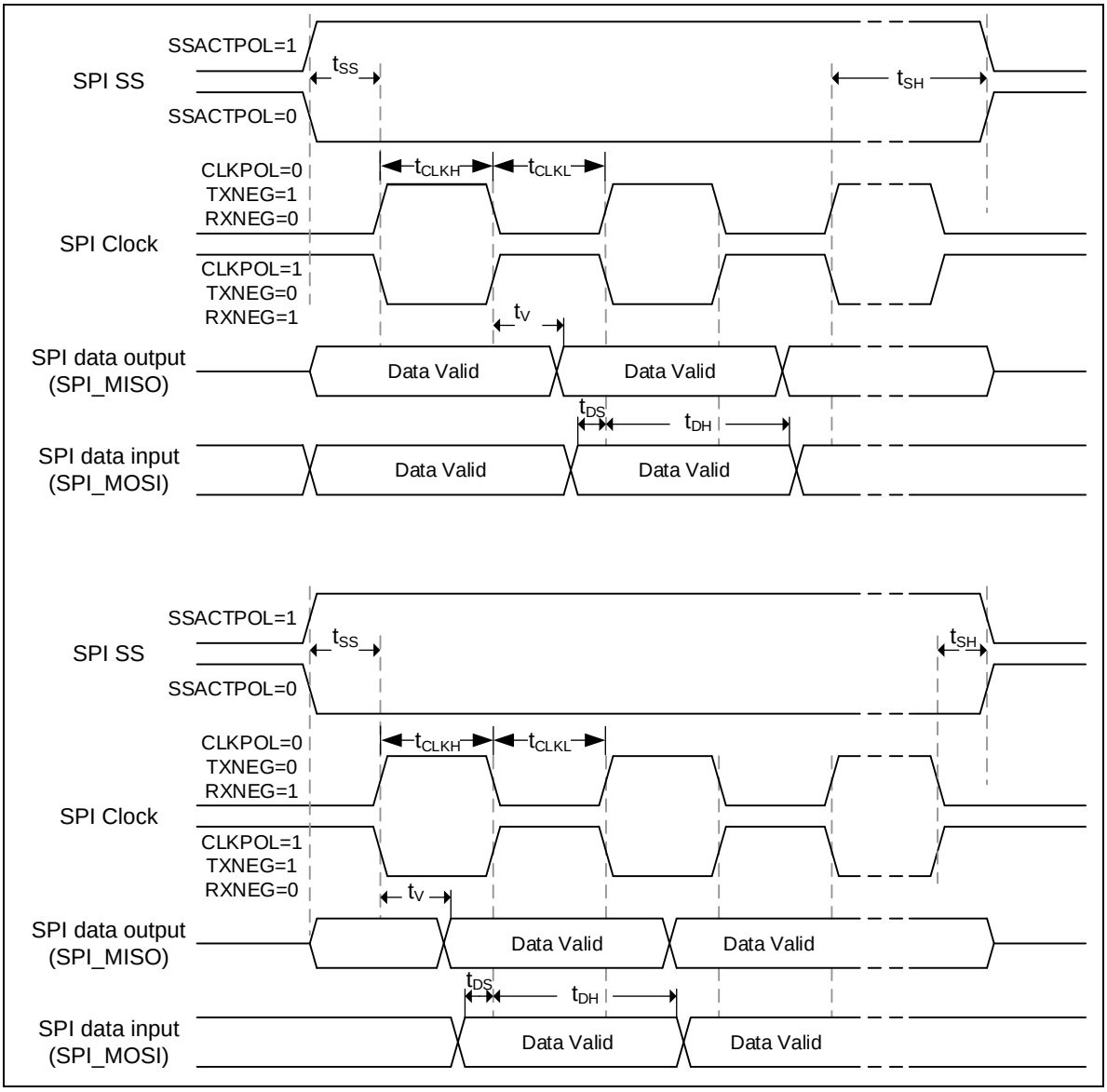


Figure 8.6-8 SPI Slave Mode Timing Diagram

8.6.6 USB Characteristics

8.6.6.1 USB High-Speed Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	High Speed Driver Rise Time	500	-		ps	CL=5pF
T_{FF}	High Speed Driver Fall Time	500	-		ps	CL=5pF
T_{FRFF}	Rise and Fall Time Matching	90		111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

8.6.7 SDIO Characteristics

8.6.7.1 SDIO Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Note:

1. Guaranteed by characterization result, not tested in production.

Table 8.6-1 SDIO Default Mode Timing

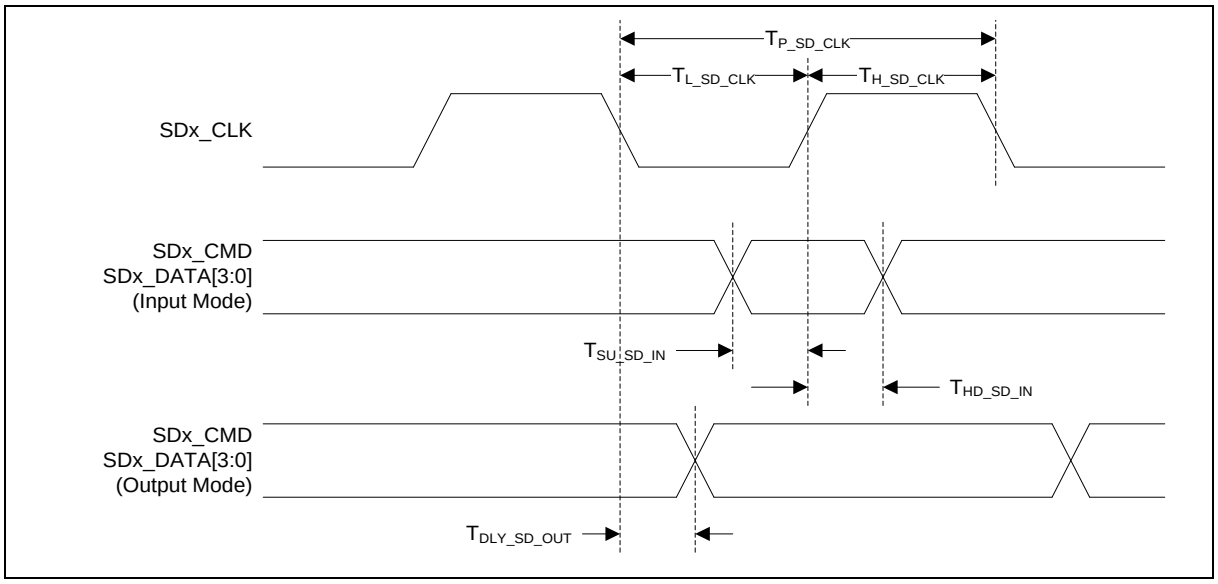


Figure 8.6-9 SDIO Default Mode

8.6.7.2 SDIO Dynamic characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Note:
1. Guaranteed by characterization result, not tested in production.

Table 8.6-2 SDIO Dynamic Characteristics

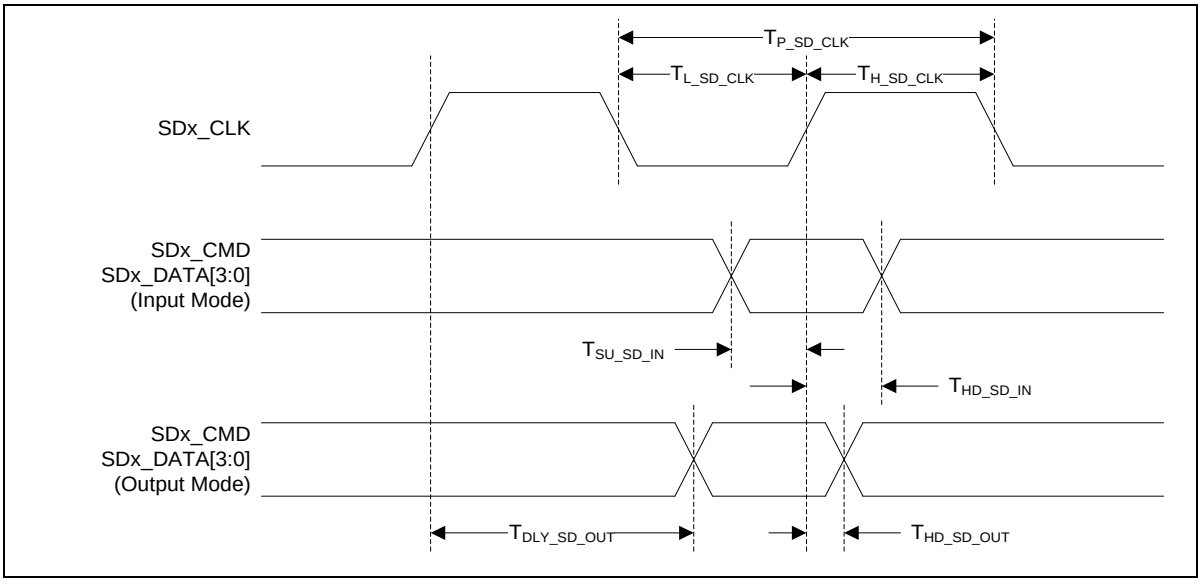


Figure 8.6-10 SDIO High-Speed Mode

8.6.8 CAN FD Characteristics

Symbol	Parameter	Min	Max [*1]	Unit	Test Conditions
t_{CAN_TXD}	TXD output delay (Normal Slew Rate)	-	8.5	nS	2.7 V ≤ VDD ≤ 3.6V , C_L = 30 pF
t_{CAN_RXD}	RXD input delay	-	7.2	nS	2.7 V ≤ VDD ≤ 3.6V
Note: Guaranteed by design, not tested in production.					

8.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.08	1.2	1.32	V	T_A = 25℃
T_{ERASE}	Page erase time	80	89.26	160	ms	
T_{PROG}	Program time	8	45.4	-	μs	
I_{DD1}	Read current	-	3.21	4.12	mA	
I_{DD2}	Program current	-	4	5	mA	
I_{DD3}	Erase current	-	4	5	mA	
N_{ENDUR}	Cycling Endurance	10,000	-	-	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	10	-	-	year	20 kcycle[2] , T_J = 85℃
		100	-	-	year	20 kcycle[2] , T_J = 25℃

Notes:

1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
3. Guaranteed by design.

Table 8.7-1 Flash DC Electrical Characteristics

9 ELECTRICAL CHARACTERISTICS FOR M467 SERIES

9.1 Absolute Maximum Ratings

Stresses above the absolute maximum ratings may cause permanent damage to the device. The limiting values are stress ratings only and cannot be used to functional operation of the device. Exposure to the absolute maximum ratings may affect device reliability and proper operation is not guaranteed.

9.1.1 Voltage Characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}[*1]	DC power supply	-0.3	4.0	V
V_{DDIO}-V_{SS}[*1]	V_{DDIO} Power Supply	-0.3	4.0	V
V_{BAT}-V_{SS}[*1]	V_{BAT} Power Supply	-0.3	4.0	V
ΔV_{DD}	Variations between different V_{DD} power pins	-	50	mV
$\|V_{DD} - AV_{DD}\|$	Allowed voltage difference for V_{DD} and AV_{DD}	-	50	mV
ΔV_{SS}	Variations between different ground pins	-	50	mV
$\|V_{SS} - AV_{SS}\|$	Allowed voltage difference for V_{SS} and AV_{SS}	-	50	mV
V_{IN}	Input Voltage on 5V-tolerance GPIO	-	5.5	V
	Input Voltage on RTC domain (PF.6 ~ PF.11)		V_{DD}	V
	Input Voltage on any other pin[*2]		V_{DD}	V

Notes:

1. All main power (V_{DD}, V_{DDIO}, V_{BAT}, AV_{DD}) and ground (V_{SS}, AV_{SS}) pins must be connected to the external power supply.
2. Refer to Table 9.1-2 Current Characteristics for the values of the maximum allowed injected current

Table 9.1-1 Voltage Characteristics

9.1.2 Current Characteristics

Symbol	Description	Min	Max	Unit
ΣI_{DD}[*1]	Maximum current into V_{DD}	-	200	mA
I_{DDIO}	Maximum Current into V_{DDIO}	-	100	
I_{BAT}	Maximum Current into V_{BAT}	-	100	
ΣI_{SS}	Maximum current out of V_{SS}	-	100	
I_{IO}	Maximum current sunk by a I/O Pin	-	20	
	Maximum current sourced by a I/O Pin	-	20	
	Maximum current sunk by total I/O Pins[*2]	-	100	
	Maximum current sourced by total I/O Pins[*2]	-	100	
$I_{INJ(PIN)}$ [*3]	Maximum injected current by a I/O Pin	-	±5	
$\Sigma I_{INJ(PIN)}$ [*3]	Maximum injected current by total I/O Pins	-	±25	

Note:

1. Maximum allowable current is a function of device maximum power dissipation.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins.
3. A positive injection is caused by $V_{IN}>AV_{DD}$ and a negative injection is caused by $V_{IN}<V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. It is recommended to connect an overvoltage protection diode between the analog input pin and the voltage supply pin.

Table 9.1-2 Current Characteristics

9.1.3 Thermal Characteristics

The maximum junction temperature T_{Jmax} in ℃, can be cacultated by the following equation:

$T_{Jmax} = T_{Amax} + (P_{Dmax} \times \theta_{JA})$, where,

- T_{Amax} = maximum ambient temperature (℃)
- θ_{JA} = thermal resistance junction-ambient (℃/Watt)
- P_{Dmax} = max power consumption of the chip, it's a multiply of max supply Vmax and max working current Imax (P_{Dmax} = Vmax x Imax)

Symbol	Description	Min	Typ	Max	Unit
T_A	Operating ambient temperature	-40	-	85	℃
T_J	Operating junction temperature	-40	-	125	
T_{ST}	Storage temperature	-65	-	150	
θ_{JA}[*1]	Thermal resistance junction-ambient 64-pin LQFP(7x7 mm)	-	53.55	-	℃/Watt
	Thermal resistance junction-ambient 128-pin LQFP(14x14 mm)	-	50.09	-	℃/Watt
	Thermal resistance junction-ambient 144-pin LQFP(20x20 mm)	-	40.91	-	℃/Watt
	Thermal resistance junction-ambient 176-pin LQFP(24x24 mm)	-	39.13	-	℃/Watt

Note:

1. Determined according to JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions

Table 9.1-3 Thermal Characteristics

9.1.4 EMC Characteristics

9.1.4.1 Electrostatic discharge (ESD)

For the Nuvoton MCU products, there are ESD protection circuits which built into chips to avoid any damage that can be caused by typical levels of ESD.

9.1.4.2 Static latchup

Two complementary static tests are required on six parts to assess the latchup

performance:

- A supply overvoltage is applied to each power supply pin
- A current injection is applied to each input, output and configurable I/O pin

9.1.4.3 Electrical fast transients (EFT)

In some application circuit compoment will produce fast and narrow high-frequency trasnients bursts of narrow high-frequency transients on the power distribution system..

- Inductive loads:
  - Relays, switch contactors
  - Heavy-duty motors when de-energized etc.

The fast transient immunity requirements for electronic products are defined in IEC 61000-4-4 by International ElectrotechnicalCommission (IEC).

Symbol	Description	Min	Typ	Max	Unit
V_{HBM}[*1]	Electrostatic discharge,human body mode	-2000	-	+2000	V
V_{CDM}[*2]	Electrostatic discharge,charge device model	-500	-	500	
LU[*3]	Pin current for latch-up[*3]	-400	-	400	mA
V_{EFT}[*4] [*5]	Fast transient voltage burst	-4.4	-	+4.4	kV

Notes:

1. Determined according to ANSI/ESDA/JEDEC JS-001 Standard, Electrostatic Discharge Sensitivity Testing – Human Body Model (HBM) – Component Level
2. Determined according to ANSI/ESDA/JEDEC JS-002 standard for Electrostatic Discharge Sensitivity (ESD) Testing – Charged Device Model (CDM) – Component Level.
3. Determined according to JEDEC EIA/JESD78 standard.
4. Determinded according to IEC 61000-4-4 Electrical fast transient/burst immunity test.
5. The performace cretia class is 4A.

Table 9.1-4 EMC Characteristics

9.1.5 Package Moisture Sensitivity(MSL)

The MSL rating of an IC determines its floor life before the board mounting once its dry bag has been opened. All Nuvoton surface mount chips have a moisture level classification. The information is also displayed on the bag packing.

Pacakge	MSL
64-pin LQFP(7x7 mm) [*1]	MSL 3
128-pin LQFP(14x14 mm) [*1]	MSL 3
144-pin LQFP(20x20 mm) [*1]	MSL 3
176-pin LQFP(24x24 mm) [*1]	MSL 3
Note: 1. Determined according to IPC/JEDEC J-STD-020	

Table 9.1-5 Package Moisture Sensitivity(MSL)

9.1.6 Soldering Profile

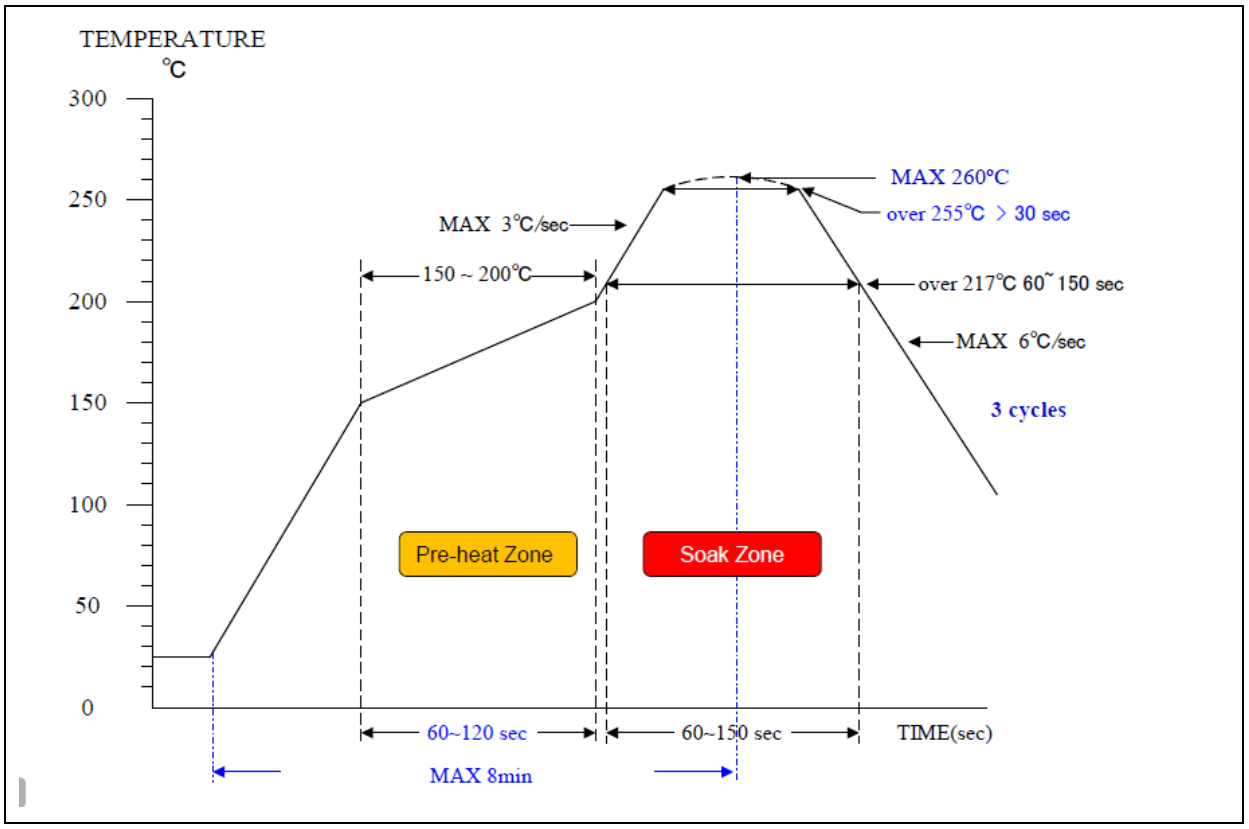


Figure 9.1-1 Soldering Profile from J-STD-020C

Porfile Feature	Pb Free Package
Average ramp-up rate (217℃ to peak)	3℃/sec. max
Preheat temperature 150℃ ~200℃	60 sec. to 120 sec.
Temperature maintained above 217℃	60 sec. to 150 sec.
Time with 5℃ of actual peak temperature	> 30 sec.
Peak temperature range	260℃
Ramp-down rate	6℃/sec ax.
Time 25℃ to peak temperature	8 min. max
Note: 1.Determined according to J-STD-020C	

Table 9.1-6 Soldering Profile

9.2 General Operating Conditions

(V_{DD}-V_{SS} = 1.7 ~ 3.6V, T_A = 25°C, HCLK = 200 MHz unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	85	℃	
f_{HCLK}	Internal AHB clock frequency	-	-	200	MHz	Turbo run mode with PL0 (PLSEL = 00)
V_{DD}	Operation voltage	1.7	-	3.6	V	
V_{DDIO}	V_{DDIO} Operation voltage	1.7	-	3.6		
V_{BAT}	V_{BAT} Operation voltage	1.7	-	3.6		
AV_{DD}[*1]	Analog operation voltage	V_{DD}				
V_{REF}	Analog reference voltage	1.7	-	AV_{DD}		
V_{LDO}	LDO output voltage	-	1.26	-		
V_{BG}	Band-gap voltage	1.173	1.210	1.246	V	
T_{VBG_ADC}[*3]	ADC sampling time when reading the band-gap voltage	20	-	-	µS	
C_{LDO}[*2]	LDO output capacitor on each pin	2.2			µF	
R_{ESR}[*3]	ESR of C_{LDO} output capacitor	-	-	0.5	Ω	
I_{RUSH}[*3]	InRush current on voltage regulator power-on (POR or wakeup from Standby)	-	-	150	mA	
E_{RUSH}[*3]	InRush energy on voltage regulator power-on (POR or wakeup from Standby)	-	2.64	-	µC	V_{DD} = 1.2 V, T_A = 85 °C

Note:

1. It is recommended to power V_{DD} and AV_{DD} from the same source. A maximum difference of 0.3 V between V_{DD} and AV_{DD} can be tolerated during power-on and power-off operation .
2. To ensure stability, an external 2.2 µF output capacitor, C_{LDO} must be connected between the LDO_CAP pin and the closest GND pin of the device. Solid tantalum and multilayer ceramic capacitors are suitable as output capacitor. Additional 100 nF bypass capacitor between LDO_CAP pin and the closest GND pin of the device helps decrease output noise and improves the load transient response.
3. Guaranteed by design, not tested in production

Table 9.2-1 General Operating Conditions

9.3 DC Electrical Characteristics

9.3.1 Supply Current Characteristics

The current consumption is a combination of internal and external parameters and factors such as operating frequencies, device software configuration, I/O pin loading, I/O pin switching rate, program location in memory and so on. The current consumption is measured as described in below condition and table to inform test characterization result.

- All GPIO pins are in push pull mode and output high.
- The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 1.7 ~ 3.6 V unless otherwise specified.
- $V_{DD} = AV_{DD} = V_{DDIO} = V_{BAT}$
- When the peripherals are enabled HCLK is the system clock, $f_{PCLK0, 1} = f_{HCLK}/2$.
- Program run CoreMark® code in Flash.

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]		Unit
			T_A = 25 °C	T_A = 25 °C)	T_A = 85 °C)	
I_{DD_RUN}	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable PLL	200 MHz	34.92	35.98	51.25	mA
		192 MHz	34.26	35.53	50.76	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT clock	180 MHz	30.51	31.53	44.61	
		160 MHz	28.01	28.98	42.06	
		144 MHz	24.78	25.79	38.80	
		120 MHz	20.92	21.93	34.91	
		96 MHz	17.79	18.85	31.89	
		84 MHz	15.76	16.78	29.76	
		72 MHz	13.75	14.77	27.74	
		60 MHz	11.74	12.78	25.70	
		50 MHz	10.03	11.09	23.98	
		24 MHz	5.43	6.52	19.42	
		12 MHz	2.92	3.94	16.72	
		6 MHz	2.01	3.03	15.80	
		4 MHz	1.69	2.74	15.50	
		2 MHz	1.38	2.44	15.20	
		1 MHz	1.24	2.28	15.04	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable LIRC or LXT clock.	32.768 kHz	0.94	1.98	14.74	
		10 kHz	0.93	1.98	14.74	

	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable PLL	200 MHz	153.75	155.39	168.82	
		192 MHz	148.63	150.24	163.88	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT clock	180 MHz	132.89	134.02	145.42	
		160 MHz	118.88	119.84	131.53	
		144 MHz	107.60	108.56	120.54	
		120 MHz	90.59	91.47	103.68	
		96 MHz	74.09	74.89	87.51	
		84 MHz	65.29	66.07	78.72	
		72 MHz	56.52	57.27	70.03	
		60 MHz	47.68	48.41	61.25	
		50 MHz	40.29	41.00	53.93	
		24 MHz	19.98	20.95	34.07	
		12 MHz	10.49	11.44	24.28	
		6 MHz	6.15	7.13	19.97	
		4 MHz	4.71	5.72	18.54	
		2 MHz	3.26	4.28	17.11	
		1 MHz	2.56	3.56	16.38	
	Normal run mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable	32.768 kHz	1.29	2.35	15.17	
		10 kHz	1.27	2.33	15.14	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 9.3-1 Current Consumption in Normal Run Mode

Symbol	Conditions	F_{HCLK}	Typ [*1]	Max[*1][*2]		Unit
			T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_IDLE}	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals disable PLL	200 MHz	8.46	9.69	24.65	mA
		192 MHz	8.90	10.17	25.23	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable HIRC, PLL, HXT clock	180 MHz	7.97	9.00	21.97	
		160 MHz	7.40	8.43	21.37	
		144 MHz	6.68	7.71	20.64	
		120 MHz	5.84	6.85	19.75	
		96 MHz	5.71	6.74	19.71	
		84 MHz	5.19	6.23	19.16	
		72 MHz	4.66	5.72	18.62	
		60 MHz	4.14	5.20	18.09	
		50 MHz	3.71	4.76	17.63	
		24 MHz	2.40	3.48	16.36	
		12 MHz	1.38	2.43	15.22	
		6 MHz	1.23	2.28	15.06	
		4 MHz	1.17	2.22	15.00	
		2 MHz	1.12	2.17	14.95	
		1 MHz	1.09	2.14	14.93	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals disable LIRC or LXT clock.	32.768 kHz	0.93	1.96	14.75	
		10 kHz	0.93	1.96	14.73	
	Turbo run mode with PL0 (PLSEL = 00), executed from Flash, all peripherals enable	200 MHz	126.58	127.77	141.61	
		192 MHz	122.50	123.68	137.87	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable HIRC, PLL, HXT clock	180 MHz	109.52	110.36	122.19	
		160 MHz	97.95	98.70	110.81	
		144 MHz	88.62	89.43	101.59	
		120 MHz	74.62	75.32	87.79	
		96 MHz	61.22	61.87	74.62	
		84 MHz	54.00	54.69	67.49	
		72 MHz	46.76	47.43	60.32	
		60 MHz	39.48	40.15	53.10	

		50 MHz	33.43	34.09	47.09	
		24 MHz	16.68	17.66	30.77	
		12 MHz	8.77	9.74	22.60	
		6 MHz	5.27	6.25	19.10	
		4 MHz	4.09	5.11	17.96	
		2 MHz	2.93	3.95	16.78	
		1 MHz	2.35	3.38	16.20	
	Idle mode with PL1 (PLSEL = 01), executed from Flash, all peripherals enable	32.768 kHz	1.28	2.34	15.16	
		10 kHz	1.26	2.31	15.13	

Notes:

1. When analog peripheral blocks such as USB, DAC, ADC, ACMP, PLL, HIRC, LIRC, HXT and LXT are ON, an additional power consumption should be considered.
2. Based on characterization, not tested in production unless otherwise specified.

Table 9.3-2 Current Consumption in Idle Mode

Symbol	Test Conditions	LXT[*1] 32.768 kHz	LIRC 10 kHz	Typ[*2]	Max[*3][*4]		Unit
				T_A = 25 °C	T_A = 25 °C	T_A = 85 °C	
I_{DD_DPD}	Deep Power-down mode, all peripherals disable (LVR disabled)	-	-	0.2	0.8	2.2	µA
	Deep Power-down mode, RTC enable and run (LVR disabled)	V	-	1.1	1.9	3.5	
	Deep Power-down mode, RTC enable and run (LVR disabled)	-	V	0.5	1.2	2.7	
I_{DD_SPD}	Standby Power-down mode, all peripherals disable (No RAM retention)	-	-	1.2	1.7	8.2	uA
	Standby Power-down mode, all peripherals disable (16KB RAM retention)	-	-	6.9	15.0	136.0	
	Standby Power-down mode, all peripherals disable (32KB RAM retention)	-	-	12.7	28.0	259.2	
	Standby Power-down mode, all peripherals disable (64KB RAM retention)	-	-	24.2	54.2	504.9	
	Standby Power-down mode, all peripherals disable (128KB RAM retention)	-	-	46.6	106.2	978.7	
	Standby Power-down mode, all peripherals disable (256KB RAM retention)	-	-	90.2	206.9	1893.5	
	Standby Power-down mode, RTC enable and run (No RAM retention)	V	-	2.2	2.7	9.5	

	Standby Power-down mode, RTC enable and run (No RAM retention)	-	V	1.6	2.1	8.6	uA
I_{DD_LLPD}	Low leakage Power-down mode, all peripherals disable	-	-	0.34	0.77	6.93	mA
	Low leakage Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	0.35	0.77	6.93	
	Low leakage Power-down mode, WDT /Timer use LIRC, RTC use LIRC	-	V	0.35	0.77	6.93	
	Ultra Low leakage Power-down mode, WDT/Timer use LIRC, UART /RTC use LXT	V	V	0.35	0.77	6.95	
I_{DD_PD} (PL0)	Power-down mode, all peripherals disable	-	-	1.01	2.27	16.77	mA
	Power-down mode, all peripherals disable (LVR disabled)			1.01	2.27	16.79	
	Power-down mode, RTC enable and run	V		1.01	2.27	16.82	

	Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	1.01	2.27	16.83	
	Power-down mode, WDT/Timer use LIRC, RTC use LIRC	-	V	1.00	2.27	16.84	
	Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT	V	V	1.01	2.26	16.86	
I_{DD_PD} (PL1)	Power-down mode, all peripherals disable			0.85	1.88	14.48	mA
	Power-down mode, all peripherals disable (LVR disabled)			0.85	1.88	14.49	
	Power-down mode, RTC enable and run			0.85	1.88	14.48	
	Power-down mode, WDT/Timer/UART/RTC enable and run			0.86	1.88	14.50	
	Power-down mode, WDT/Timer use LIRC, RTC use LIRC			0.85	1.88	14.50	
	Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT			0.86	1.88	14.52	
I_{DD_FWPD} (PL0)	Fast wake up Power-down mode, all peripherals disable	-	-	1.03	2.22	16.41	mA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run	V	-	1.05	2.29	16.54	

	Fast wake up Power-down mode, WDT/Timer use LIRC, RTC use LIRC	-	V	1.07	2.32	16.59	
	Fast wake up Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT	V	V	1.08	2.33	16.65	
I_{DD_FWPD1} (PL1)	Fast wake up Power-down mode, all peripherals disable			0.92	1.95	14.34	mA
	Fast wake up Power-down mode, WDT/Timer/UART/RTC enable and run			0.93	1.95	14.39	
	Fast wake up Power-down mode, WDT/Timer use LIRC, RTC use LIRC			0.93	1.95	14.42	
	Fast wake up Power-down mode, WDT/Timer use LIRC, UART/RTC use LXT			0.93	1.95	14.44	

Notes:

1. Crystal used: AURUM XF66RU000032C0 with a C_L of 20 pF for L7 gain level. → AE should list test condition.
2. $V_{DD} = AV_{DD} = V_{BAT} =$ 3.3V, LVR enabled, POR disabled and BOD disabled.
3. Based on characterization, not tested in production unless otherwise specified.
4. When analog peripheral blocks such as USB, DAC, ADC and ACMP are ON, an additional power consumption should be considered.
5. Based on characterization, tested in production.

Table 9.3-3 Chip Current Consumption in Power-Down Mode

9.3.2 On-Chip Peripheral Current Consumption

- The typical values for T_A= 25 °C and V_{DD} = AV_{DD} = V_{BAT} = 3.3 V unless otherwise specified.
- All GPIO pins are set as output high of push pull mode without multi-function.
- HCLK is the system clock, f_{HCLK} = 200 MHz, $f_{PCLK0, 1}$ = f_{HCLK}/2.
- The result value is calculated by measuring the difference of current consumption between all peripherals clocked off and only one peripheral clocked on

Peripheral	I_{DD}[*1]	Unit
PDMA0	9494	uA
ISP	~0	
EBI	867	
ST	268	
EMAC0	10180	
SDH0	6220	
CRC	378	
CCAP	6458	
SEN	2328	
HSUSBD[*3]	5130	
HBI	1414	
CRPT	5854	
KS	2411	
SPIM	14156	
FMCIDLE	1970	
USBH[*3]	11089	
SDH1	6098	
PDMA1	7934	
TRACE	~0	
GPA	155	
GPB	145	
GPC	137	
GPD	140	
GPE	145	
GPF	130	
GPG	145	
GPH	152	
WDT	630	

RTC	407	
TMR0	689	
TMR1	669	
TMR2	670	
TMR3	692	
CLKO	607	
ACMP01[*2]	573	
I2C0	397	
I2C1	372	
I2C2	403	
I2C3	367	
QSPI0	1412	
SPI0	1285	
SPI1	1369	
SPI2	1223	
UART0	1132	
UART1	1099	
UART2	1091	
UART3	1070	
UART4	1087	
UART5	1057	
UART6	1087	
UART7	1076	
OTG[*3]	1472	
USBD[*3]	1711	
EADC0[*1]	3085	
I2S0	1420	
HSOTG	1399	
SC0	896	
SC1	789	
SC2	833	
I2C4	405	
QSPI1	1322	
SPI3	1331	
USCI0	479	

PSIO	1912	
DAC[*4]	426	
ECAP2	498	
ECAP3	470	
EPWM0	810	
EPWM1	756	
BPWM0	475	
BPWM1	457	
EQEI2C	462	
EQEI3C	446	
EQEI0	460	
EQEI1	439	
TRNG	745	
ECAP0	491	
ECAP1	471	
I2S1	1345	
EADC1[*1]	2927	
KPI	1034	
EADC2[*1]	2882	
ACMP23[*2]	585	
UART8	360	
UART9	363	
CANFD0	4591	
CANFD1	4546	
CANFD2	4583	
CANFD3	4539	
GPI	128	
GPJ	143	

Notes:

1. Guaranteed by characterization results, not tested in production.
2. When the ADC is turned on, add an additional power consumption per ADC for the analog part.
3. When the ACMP is turned on, add an additional power consumption per ACMP for the analog part.
4. When the USB is turned on, add an additional power consumption per USB for the analog part.
5. When the DAC is turned on, add an additional power consumption per DAC for the analog part.

Table 9.3-4 Peripheral Current Consumption

9.3.3 Wakeup Time from Low-Power Modes

The wakeup times given in Table 9.3-5 is measured on a wakeup phase with a 12MHz HIRC oscillator.

Symbol	Parameter	Typ	Max	Unit
t_{WU_IDLE}	Wakeup from IDLE mode	10	-	cycles
t_{WU_DPD}[*1][*2] [*3]	Wakeup from Deep Power-down mode	11.428	-	mS
t_{WU_SPD}[*1][*2]	Wakeup from Standby Power-down mode	176.003	-	µS
t_{WU_LLPD}[*1][*2]	Wakeup from Low leakage Power-down mode	51.035	-	
t_{WU_NPD}[*1][*2]	Wakeup from Normal Power-down mode	10.102	-	
t_{WU_FWPD}[*1][*2]	Wakeup from fast wake up Power-down mode	7.357	-	
t_{ET_IDLE}	Enter to IDLE mode	17	-	cycles
t_{ET_DPD}	Enter to Deep Power-down mode	59.042	-	µS
t_{ET_SPD}	Enter to Standby Power-down mode	55.042	-	
t_{ET_LLPD}	Enter to Low leakage Power-down mode	1.305	-	
t_{ET_NPD}	Enter to Normal Power-down mode	1.388	-	
t_{ET_FWPD}	Enter to fast wake up Power-down mode	1.383	-	

Notes:

1. Based on test during characterization, not tested in production.
2. The wakeup times are measured from the wakeup event to the point in which the application code reads the first instruction.
3. CONFIG3[12:8] =0x1F with MKROM-ISP function. CONFIG3[12:8] =0x2 without MKROM-ISP function.

Table 9.3-5 Low-Power Mode Wakeup Timings

9.3.4 I/O Current Injection Characteristics

In general, I/O current injection due to external voltages below V_{SS} or above V_{DD} should be avoided during normal product operation. However, the analog compoenent of the MCU is most likely to be affected by the injection current , but it is not easily clarified when abnormal injection accidentally happens. It is recommended to add a Schottky diode (pin to ground or pin to V_{DD}) to pins that include analog function which may potentially injection currents.

Symbol	Parameter	Negative injection	Positive injection	Unit	Test Condition
$I_{INJ(PIN)}$	Injected current by a I/O Pin	-0	0	mA	Injected current on nReset pins
		-0	0		Injected current on PF2~PF5, PA10, PA11 and PB0~PB15 for analog input function
		-5	+5		Injected current on any other I/O except analog input pin

Table 9.3-6 I/O Current Injection Characteristics

9.3.5 I/O DC Characteristics

9.3.5.1 PIN Input Characteristics

Symbol	Parameter	Min[*2]	Typ[*1]	Max[*2]	Unit	Test Conditions
V_{IL}	Input low voltage (Schmitt trigger)	0	-	0.3*V_{DD}	V	
	Input low voltage (TTL trigger)	0	-			V_{DD} = 3.0 V
		0	-	0.7		V_{DD} = 2.7 V
		0	-	0.5		V_{DD} = 1.7 V
V_{IH}	Input high voltage (Schmitt trigger)	0.7*V_{DD}	-	V_{DD}	V	
	Input high voltage (TTL trigger)	2	-	V_{DD}		V_{DD} = 3.6 V
		1.5	-	V_{DD}		V_{DD} = 3.3 V
		1.0	-	V_{DD}		V_{DD} = 1.7V
V_{HY}	Hysteresis voltage of schmitt input	-	0.2*V_{DD}	-	V	
I_{LK}[*3]	Input leakage current	-1	-	1	µA	V_{SS} < V_{IN} < V_{DD}, Open-drain or input only mode
		-1	-	1		V_{DD} < V_{IN} < 3.3 V, Open-drain or input only mode on any other 3.3V tolerance pins
R_{PU}	Pull up resistor	43	51	60	kΩ	VDD=3.6V
R_{PD}	Pull down resistor	43	51	60	kΩ	VDD=3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design result, not tested in production.
3. Leakage could be higher than the maximum value, if abnormal injection happens.

Table 9.3-7 I/O Input Characteristics

9.3.5.2 I/O Output Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{SR}[*1] [*2]	Source current for quasi-bidirectional mode and high level	6.66	7.74	9.50	μA	V_{DD} = 3.0V V_{IN}=(V_{DD}-0.4) V
		6.64	7.71	9.46	μA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		6.53	7.56	9.25	μA	V_{DD} = 1.7 V V_{IN}=(V_{DD}-0.4) V
	Source current for push-pull mode and high level	13.52	17.51	23.16	mA	V_{DD} = 3.0V V_{IN}=(V_{DD}-0.4) V
		12.33	15.92	21.57	mA	V_{DD} = 2.7 V V_{IN}=(V_{DD}-0.4) V
		7.12	9.85	13.20	mA	V_{DD} = 1.7 V V_{IN}=(V_{DD}-0.4) V
I_{SK}[*1] [*2]	Sinkcurrent for push-pull mode and low level	-12.97	-16.65	-24.45	mA	V_{DD} = 3.0V V_{IN}= 0.4 V
		-11.96	-15.71	-23.40	mA	V_{DD} = 2.7 V V_{IN}= 0.4 V
		-6.83	-9.55	-15.03	mA	V_{DD} = 1.7 V V_{IN}= 0.4 V
C_{IO}[*1]	I/O pin capacitance	4.64	4.73	4.82	pF	

Notes:

1. Guaranteed by characterization result, not tested in production.
2. The I_{SR} and I_{SK} must always respect the abslute maximum current and the sum of I/O, CPU and peripheral must not exceed ΣI_{DD} and ΣI_{SS}.

Table 9.3-8 I/O Output Characteristics

9.3.5.3 nRESET Input Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{ILR}	Negative going threshold, nRESET	-	-	$0.3*V_{DD}$	V	
V_{IHR}	Positive going threshold, nRESET	$0.7*V_{DD}$	-	-	V	
R_{RST}[*1]	Internal nRESET pull up resistor	41	54	60	kΩ	VDD=3.6V
t_{FR}[*1]	nRESET input filtered pulse time	-	32	-	µS	Normal run and Idle mode
		-	32	-		Fast wake up Power-down mode
		-	32	-		Power-down mode
		-	32	-		Low leakage Power-down mode
		-	0	-		Standby Power-down mode
		-	0	-		Deep Power-down mode

Notes:

1. Guaranteed by characterization result, not tested in production.
2. It is recommended to add a 10 kΩ and 10uF capacitor at nRESET pin to keep reset signal stable.

Table 9.3-9 nRESET Input Characteristics

9.4 AC Electrical Characteristics

9.4.1 48 MHz Internal High Speed RC Oscillator (HIRC)

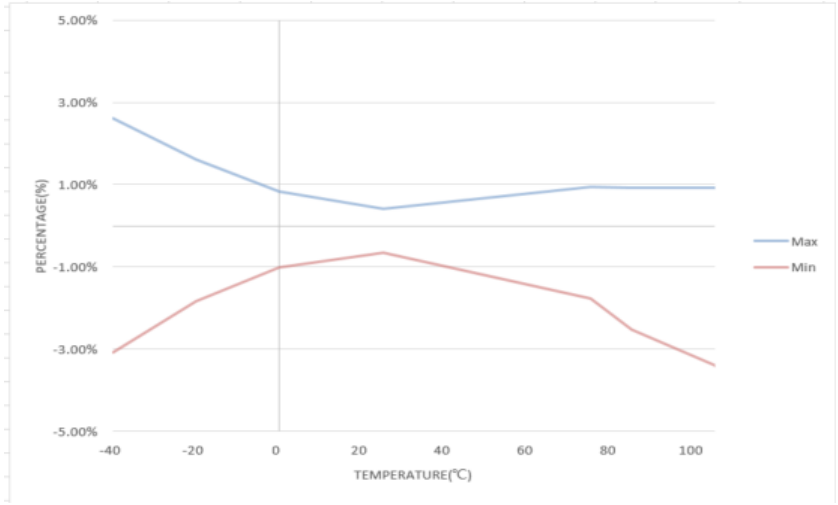
The 48 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
f_{HRC}	Oscillator frequnecy	47.52	48	48.48	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-4	-	+4	%	T_A = -40°C ~ +85 °C, V_{DD} = 1.7~3.6V
I_{HRC}[*1]	Operating current	-	100	230	µA	
T_S[*2]	Stable time	-	-	5	µS	T_A = -40°C ~ +85 °C, V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 9.4-1 48 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 9.4-1.

Figure 9.4-1 HIRC48 vs. Temperature

9.4.2 12 MHz Internal High Speed RC Oscillator (HIRC)

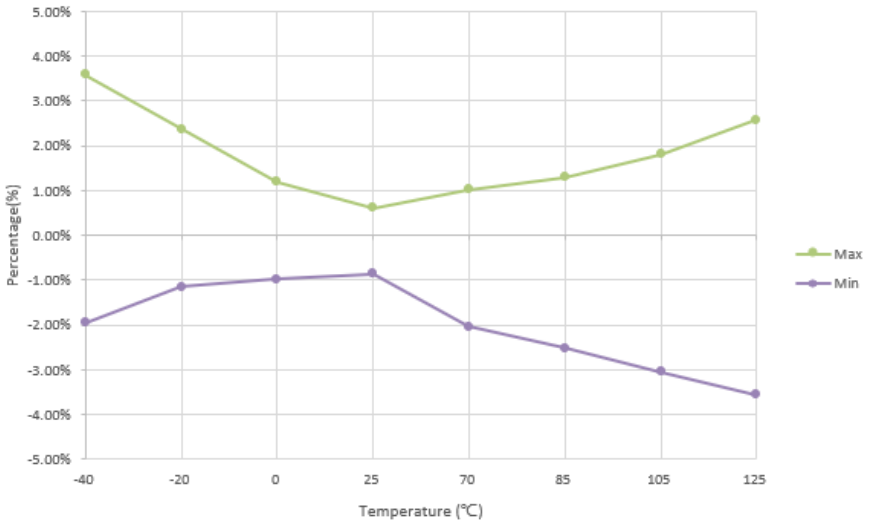
The 12 MHz RC oscillator is calibrated in production.

Symbol.	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
f_{HRC}	Oscillator frequnecy	11.88	12	12.12	MHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-1	-	1	%	T_A = 25 °C, V_{DD} = 3.3V
		-3	-	+3	%	T_A = -40°C ~ +8`5 °C, V_{DD} = 1.7~3.6V
		-4	-	+4	%	T_A = -40°C ~ +85 °C, V_{DD} = 1.7~3.6V
I_{HRC}[*1]	Operating current	-	70		μA	
T_S[*2]	Stable time	-	-	20	μS	T_A = -40°C ~ +85 °C, V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization result, not tested in production.
2. Guaranteed by design.

Table 9.4-2 12 MHz Internal High Speed RC Oscillator(HIRC) Characteristics



Notes:

2. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 9.4-2.

Figure 9.4-2 HIRC vs. Temperature

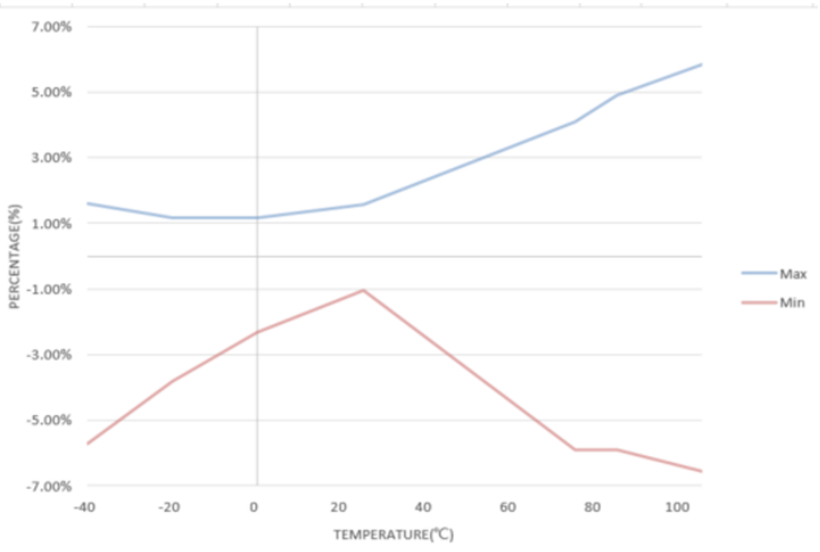
9.4.3 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
F_{LRC} [*2]	Oscillator frequnecy	-	10	-	kHz	T_A = 25 °C, V_{DD} = 3.3V
	Frequency drift over temperarure and volatge	-2	-	2	%	T_A = 25 °C, V_{DD} = 3.3V
		-15	-	15	%	T_A=-40~85°C V_{DD} = 1.7~3.6V
I_{LRC}	Operating current	-	0.5	0.7	µA	V_{DD} = 3.3V
T_S	Stable time	-	-	500 [*3]	µS	T_A=-40~85°C V_{DD} = 1.7~3.6V

Notes:

1. Guaranteed by characterization, not tested in production.
2. The 10 kHz low speed RC oscillator can be calibrated by user.
3. Guaranteed by design.

Table 9.4-3 10 kHz Internal Low Speed RC Oscillator(LIRC) Characteristics



Notes:

1. The graph is a statistical result using a limited number of samples. For the actual characteristic range, please refer to Table 9.4-3.

Figure 9.4-3 LIRC vs. Temperature

9.4.4 External 4~24 MHz High Speed Crystal/Ceramic Resonator (HXT) Characteristics

The high-speed external (HXT) clock can be supplied with a 4 to 24 MHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the XT1_IN and XT1_Out pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
V_{DD}	Operating voltage	1.7	-	3.6	V	
R_f	Internal feedback resister	-	1	-	MΩ	
f_{HXT}	Oscillator frequency	4	-	24	MHz	
I_{HXT}	Current consumption	200	250	300	µA	4 MHz, Gain = L0, C_L = 12.5 pF
		350	400	450		12 MHz, Gain = L1, C_L = 12.5 pF
		450	500	550		16 Mhz, Gain = L2, C_L = 12.5 pF
		600	640	700		24 MHz, Gain = L3, C_L = 12.5 pF
T_S	Stable time	1300	1800	2000	µS	4 MHz, Gain = L0, C_L = 12.5 pF
		458	479	600		12 MHz, Gain = L1, C_L = 12.5 pF
		340	400	500		16 Mhz, Gain = L2, C_L = 12.5 pF
		230	250	400		24 MHz, Gain = L3, C_L = 12.5 pF
Du_{HXT}	Duty cycle	40	-	60	%	
Vpp	Peak-to-peak amplitude	$0.3V_{DD}$	$0.5V_{DD}$	$0.7V_{DD}$	V	

Notes:
1. Guaranteed by design, not tested in production.

Table 9.4-4 External 4~24 MHz High Speed Crystal (HXT) Oscillator

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
Rs	Equivalent series resisotr(ESR)	-	-	120	Ω	Crystal @4 MHz, C_L = 12.5 pF, Gain = L0
		-	-	30		Crystal @12 MHz, C_L = 12.5 pF, Gain = L1
		-	-	30		Crystal @16 MHz, C_L = 12.5 pF, Gain = L2
		-	-	25		Crystal @24 MHz, C_L = 12.5 pF, Gain = L3

Notes:

1. Guaranteed by design, not tested in production.
2. Safety factor (S_f) must be higher than 5 for HXT to determine the oscillator safe operation during the application life. If Safety factor isn't enough, the HXT gain need be changed to higher driving level.

   $S_f = \frac{-R}{Crystal\ ESR} = \frac{R_{ADD} + R_S}{R_S}$

   R_{ADD}: The value of smallest series resistance preventing the oscillator from starting up successfully. This resistance is only used to measure Safety factor (S_f) of crystal in engineer stage, not for mass produciton.

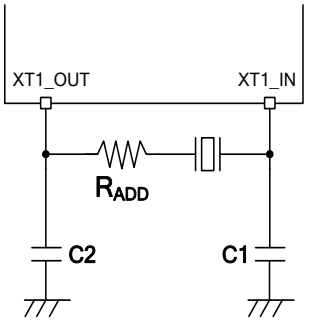


Table 9.4-5 External 4~24 MHz High Speed Crystal Characteristics

9.4.4.1 Typical Crystal Application Circuits

For C1 and C2, it is recommended to use high-quality external ceramic capacitors in 10 pF ~ 20 pF range, designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. The crystal manufacturer typically specifies a load capacitance which is the series combination of C1 and C2. PCB and MCU pin capacitance must be included (8 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C1 and C2.

CRYSTAL	C1	C2	R1
4 MHz ~ 24 MHz	10 ~ 20 pF	10 ~ 20 pF	without

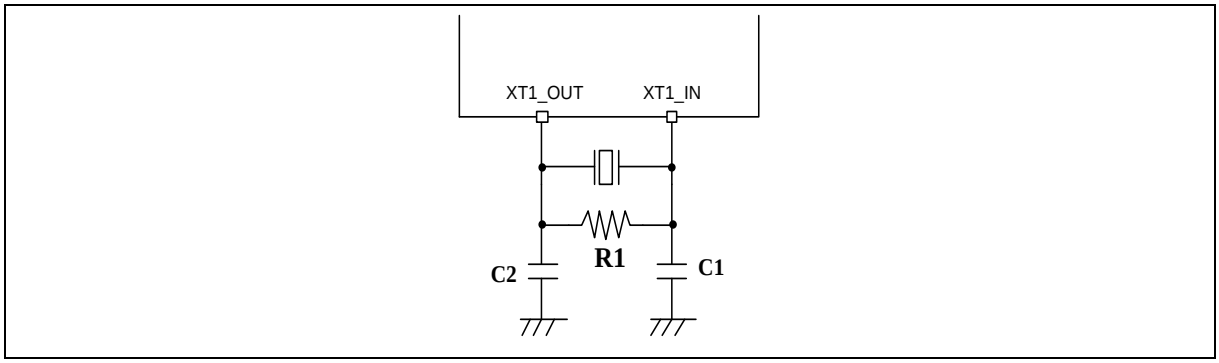
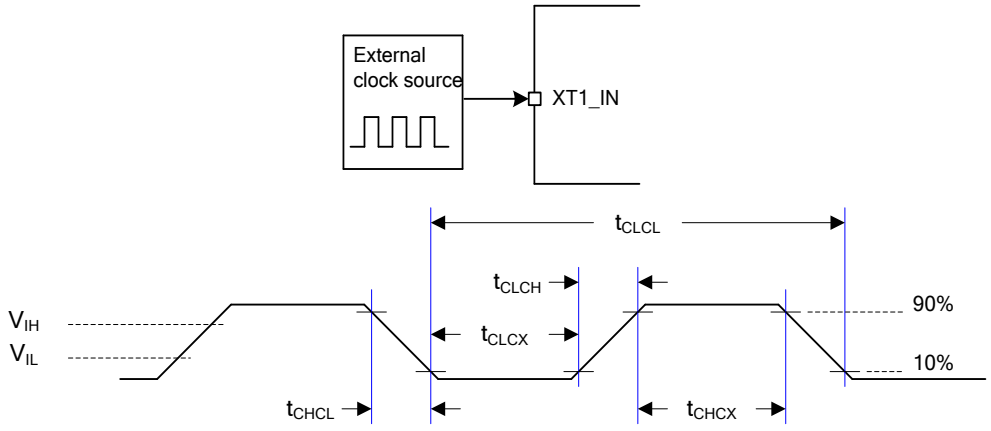


Figure 9.4-4 Typical Crystal Application Circuit

9.4.5 External 4~24 MHz High Speed Clock Input Signal Characteristics

For clock input mode the HXT oscillator is switched off and XT1_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{HXT_ext}	External user clock source frequency	1	-	24	MHz	
t_{CHCX}	Clock high time	8	-	-	nS	
t_{CLCX}	Clock low time	8	-	-	nS	
t_{CLCH}	Clock rise time	-	-	10	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	10	nS	High (90%) to low level (10%) fall time
Du_{E_HXT}	Duty cycle	40	-	60	%	
V_{IH}	Input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	XT1_IN should be set as Schmitter Trigger
V_{IL}	Input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1.Guaranteed by design, not tested in production.

Table 9.4-6 External 4~24 MHz High Speed Clock Input Signal

9.4.6 External 32.768 kHz Low Speed Crystal/Ceramic Resonator (LXT) Characteristics

The low-speed external (LXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this secion are based on characterization results obtained with typical external components. In the application, the external components have to be placed as close as possible to the X32_OUT and X32_IN pins and must not be connected to any other devices in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
V_{BAT}	Operation voltage	1.62	-	3.6	V	
T_{LXT}	Temperature range	-40	-	85	°C	
R_f	Internal feedback resistor	-	8	-	MΩ	
F_{LXT}	Oscillator frequency		32.768		kHz	
I_{LXT}	Current consumption	130	270	750	nA	ESR=35 kΩ, C_L =12 pF, Gain= L1
		160	350	850		ESR=35 kΩ, C_L= 12 pF, Gain= L2
		195	390	960		ESR=35 kΩ, C_L= 20 pF, Gain= L3
		230	450	1060		ESR=35 kΩ, C_L= 20 pF, Gain= L4
		300	560	1300		ESR=70 kΩ, C_L= 20 pF, Gain= L5
		370	680	1500		ESR=70 kΩ, C_L= 20 pF, Gain= L6
		500	920	1950		ESR=70 kΩ, C_L= 20 pF, Gain= L7
Ts_{LXT}	Stable time	1	-	2	S	
Du_{LXT}	Duty cycle	30	-	70	%	
V_{pp}	Peak-to-peak amplitude	0.35	0.5	-	V	

Notes:

1. Guaranteed by design, not tested in production.

Table 9.4-7 External 32.768 kHz Low Speed Crystal (LXT) Oscillator

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Rs	Equivalnet Series Resisotr(ESR)	-	35	70	kΩ	Crystal @32.768 kHz

Table 9.4-8 External 32.768 kHz Low Speed Crystal Characteristics

9.4.6.1 Typical Crystal Application Circuits

CRYSTAL	C1	C2	R1
32.768 kHz, ESR < 70 KΩ	5 ~ 20 pF	5 ~ 20 pF	without

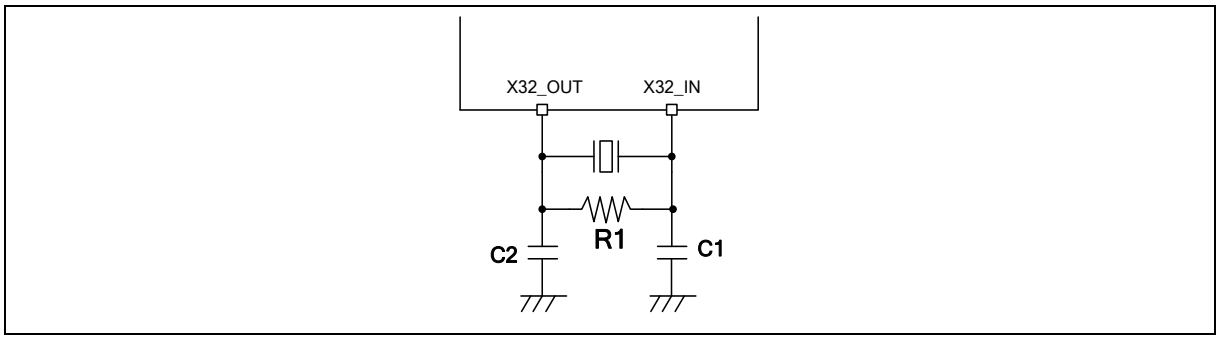
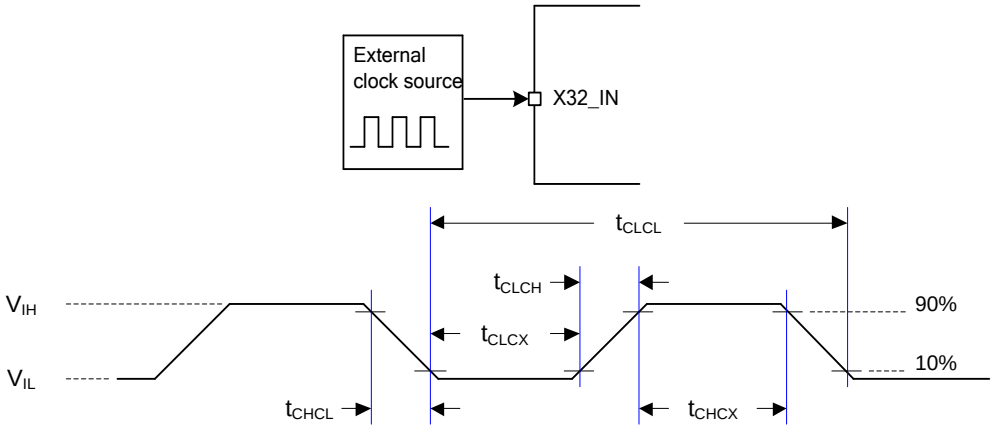


Figure 9.4-5 Typical 32.768 kHz Crystal Application Circuit

9.4.7 External 32.768 kHz Low Speed Clock Input Signal Characteristics

For clock input mode the LXT oscillator is switched off and X32_IN is a standard input pin to receive external clock. The external clock signal has to respect the below Table. The characteristics result from tests performed using a wavefrom generator.

Symbol	Parameter	Min [*1]	Typ	Max [*1]	Unit	Test Conditions
f_{LXT_ext}	External clock source frequency	-	32.768	-	kHz	
t_{CHCX}	Clock high time	450	-	-	nS	
t_{CLCX}	Clock low time	450	-	-	nS	
t_{CLCH}	Clock rise time	-	-	50	nS	Low (10%) to high level (90%) rise time
t_{CHCL}	Clock fall time	-	-	50	nS	High (90%) to low level (10%) fall time
Du_{E_LXT}	Duty cycle	30	-	70	%	
Xin_VIH	LXT input pin input high voltage	$0.7*V_{DD}$	-	V_{DD}	V	X32_IN should be set as Schmitter Trigger
Xin_VIL	LXT input pin input low voltage	V_{SS}	-	$0.3*V_{DD}$	V	



Notes:

1.Guaranteed by design, not tested in production

Table 9.4-9 External 32.768 kHz Low Speed Clock Input Signal

9.4.8 Fractional PLL Characteristics

Symbols	Parameter	Min.	Typ.	Max.	Units	Test Condition
IV_{DD}	Operating current@500MHz		2.0	2.6	mA	Does not contain clock filter current
CLK_IN	Input Clock Frequency	1		24	MHz	
Fref	Input Reference Frequency(Fref=CLK_IN/M)	1		8	MHz	
OUT_PLL	Output Frequency (OUT_PLL=Fvco/R)	25		500	MHz	
Fvco[*1]	VCO Output Frequency Fvco = CLK_IN*(2*N/M) N range : 12~255	200		500	MHz	
Jitter[*2] (peak-peak)	200MHz		250		ps	
	500MHz		250		ps	
Lock time	Form PLL_EN to OUT_PLL with clock time			200	us	
TJ	Operating junction temperature	-40	25	125	˚C	

Notes:

1.Guaranteed by characterization, not tested in production

2.Guaranteed by design, not tested in production

9.4.9 PLL Characteristics

Symbol	Parameter	Min[*1]	Typ	Max[*1]	Unit	Test Conditions
f_{PLL_in}	PLL input clock	4	-	24	MHz	
f_{PLL_OUT}	PLL multiplier output clock	50	-	500	MHz	
f_{PLL_REF}	PLL reference clock	4	-	8	MHz	
f_{PLL_VCO}[*1]	PLL voltage controlled oscillator	200	-	500	MHz	
T_L	PLL locking time	-	-	100	µS	
Jitter[*2]	Cycle-to-cycle Jitter	-	250	-	pS	
I_{DD}	Power consumption	2.7	3.25	3.3	mA	VDD=3.6V @ f_{PLL_VCO} = 500 MHz

Notes:

1.Guaranteed by characterization, not tested in production

2.Guaranteed by design, not tested in production

Table 9.4-10 PLL Characteristics

9.4.10 I/O AC Characteristics

Symbol	Parameter	Typ.	Max[*1].	Unit	Test Conditions[*2]
$t_{f(IO)out}$	Output high (90%) to low level (10%) fall time (Normal Slew Rate)	3.27	4.93	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		2.2	3.08		C_L = 10 pF, V_{DD} >= 3.0 V
		3.52	5.48		C_L = 30 pF, V_{DD} >= 2.7 V
		2.37	3.46		C_L = 10 pF, V_{DD} >= 2.7 V
		7.03	10.01		C_L = 30 pF, V_{DD} >= 1.7 V
		4.83	6.52		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (High Slew Rate)	2.58	3.63		C_L = 30 pF, V_{DD} >= 3.0 V
		1.40	1.85		C_L = 10 pF, V_{DD} >= 3.0 V
		2.78	3.98		C_L = 30 pF, V_{DD} >= 2.7 V
		1.54	2.05		C_L = 10 pF, V_{DD} >= 2.7 V
		4.59	6.91		C_L = 30 pF, V_{DD} >= 1.7 V
		2.99	3.63		C_L = 10 pF, V_{DD} >= 1.7 V
	Output high (90%) to low level (10%) fall time (Fast Slew Rate)	2.60	3.61		C_L = 30 pF, V_{DD} >= 3.0 V
		1.40	1.81		C_L = 10 pF, V_{DD} >= 3.0 V
		2.82	3.95		C_L = 30 pF, V_{DD} >= 2.7 V
		1.48	2.01		C_L = 10 pF, V_{DD} >= 2.7 V
		4.72	6.86		C_L = 30 pF, V_{DD} >= 1.7 V
		2.72	3.57		C_L = 10 pF, V_{DD} >= 1.7 V
$t_{r(IO)out}$	Output low (10%) to high level (90%) rise time (Normal Slew Rate)	3.43	5.21	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		2.38	3.46		C_L = 10 pF, V_{DD} >= 3.0 V
		3.69	5.75		C_L = 30 pF, V_{DD} >= 2.7 V
		2.61	3.84		C_L = 10 pF, V_{DD} >= 2.7 V
		6.71	10.08		C_L = 30 pF, V_{DD} >= 1.7 V

		4.88	6.81		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (High Slew Rate)	2.27	3.12	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		1.26	1.57		C_L = 10 pF, V_{DD} >= 3.0 V
		2.46	3.45		C_L = 30 pF, V_{DD} >= 2.7 V
		1.39	1.76		C_L = 10 pF, V_{DD} >= 2.7 V
		4.13	6.15		C_L = 30 pF, V_{DD} >= 1.7 V
		2.34	3.24		C_L = 10 pF, V_{DD} >= 1.7 V
	Output low (10%) to high level (90%) rise time (Fast Slew Rate)	2.31	3.11	nS	C_L = 30 pF, V_{DD} >= 3.0 V
		1.28	1.56		C_L = 10 pF, V_{DD} >= 3.0 V
		2.50	3.45		C_L = 30 pF, V_{DD} >= 2.7 V
		1.37	1.76		C_L = 10 pF, V_{DD} >= 2.7 V
		4.11	6.15		C_L = 30 pF, V_{DD} >= 1.7 V
		2.28	3.23		C_L = 10 pF, V_{DD} >= 1.7 V
$f_{max(IO)out}$[*3]	I/O maximum frequency (Normal Slew Rate)	99.50	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		145.56	-		C_L = 10 pF, V_{DD} >= 3.0 V
		92.46	-		C_L = 30 pF, V_{DD} >= 2.7 V
		133.87	-		C_L = 10 pF, V_{DD} >= 2.7 V
		48.52	-		C_L = 30 pF, V_{DD} >= 1.7 V
		68.66	-		C_L = 10 pF, V_{DD} >= 1.7 V
	I/O maximum frequency (High Slew Rate)	137.46	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		250.63	-		C_L = 10 pF, V_{DD} >= 3.0 V
		127.23	-		C_L = 30 pF, V_{DD} >= 2.7 V
		227.53	-		C_L = 10 pF, V_{DD} >= 2.7 V
		76.45	-		C_L = 30 pF, V_{DD} >= 1.7 V
		125.08	-		C_L = 10 pF, V_{DD} >= 1.7 V

	I/O maximum frequency (Fast Slew Rate)	135.78	-	MHz	C_L = 30 pF, V_{DD} >= 3.0 V
		248.76	-		C_L = 10 pF, V_{DD} >= 3.0 V
		125.31	-		C_L = 30 pF, V_{DD} >= 2.7 V
		233.92	-		C_L = 10 pF, V_{DD} >= 2.7 V
		75.50	-		C_L = 30 pF, V_{DD} >= 1.7 V
		133.33	-		C_L = 10 pF, V_{DD} >= 1.7 V
I_{DIO}[*4]	I/O dynamic current consumption	2.77	-	mA	C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		1.19	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 24 MHz
		0.69	-		C_L = 30 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz
		0.3	-		C_L = 10 pF, V_{DD} = 3.3 V, $f_{(IO)out}$ = 6 MHz

Notes:

1. Guaranteed by design result, not tested in production.
2. C_L is a external capacitive load to simulate PCB and device loading.
3. The maximum frequency is defined by $f_{max} = \frac{2}{3 \times (t_f + t_r)}$.
4. The I/O dynamic current consumption is defined by $I_{DIO} = V_{DD} \times f_{IO} \times (C_{IO} + C_L)$

Table 9.4-11 I/O AC Characteristics

9.5 Analog Characteristics

9.5.1 LDO

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{DD}	Power supply	1.7	-	3.6	V	
V_{LDO}	Output voltage	0.9	1.26	1.32	V	
T_A	Temperature	-40	-	85	℃	

Notes:

1. It is recommended a 0.1μF bypass capacitor is connected between VDD and the closest VSS pin of the device.
2. For ensuring power stability, a 2.2μF capacitor must be connected between LDO_CAP pin and the closest VSS pin of the device.
3. V_{LDO} is only used to supply internal power.

9.5.2 Reset and Power Control Block Characteristics

The parameters in below table are derived from tests performed under ambient temperature.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
I_{POR}[*1]	POR operating current	-	35	45	µA	V_{DD}=AV_{DD} = 3.6V
I_{LVR}[*1]	LVR operating current	-	0.3	0.6		V_{DD}=AV_{DD} = 3.6V
I_{BOD}[*1]	BOD operating current	-	30	40		V_{DD}=AV_{DD} = 3.6V, Normal mode
		-	1	-		V_{DD}=AV_{DD} = 3.6V, Low Power mode
V_{POR}	POR reset voltage (Rising edge)	1.4	1.49	1.57	V	
	POR reset voltage (Falling edge)	1.38	1.46	1.54		
V_{LVR}	LVR reset voltage (Rising edge)	1.45	1.5	1.6		
	LVR reset voltage (Falling cedge)	1.4	1.5	1.55		
V_{BOD}	BOD brown-out detect voltage (Rising edge)	1.60	1.70	1.80		BODVL = 0
		1.80	1.90	2.00		BODVL = 1
		2.00	2.10	2.20		BODVL = 2
		2.20	2.30	2.40		BODVL = 3
		2.40	2.50	2.60		BODVL = 4
		2.60	2.70	2.80		BODVL = 5
		2.80	2.90	3.00		BODVL = 6
		3.00	3.10	3.20		BODVL = 7
	BOD brown-out detect voltage (Falling edge)	1.50	1.60	1.70		BODVL = 0
		1.70	1.80	1.90		BODVL = 1
		1.90	2.00	2.10		BODVL = 2
		2.10	2.20	2.30		BODVL = 3
		2.30	2.40	2.50		BODVL = 4
		2.50	2.60	2.70		BODVL = 5
		2.70	2.80	2.90		BODVL = 6
		2.90	3.00	3.10		BODVL = 7
T_{LVR_SU}[*2]	LVR startup time	-	-	256	µS	Normal mode
		-	-	512		Low Power mode
T_{LVR_RE}[*1]	LVR respond time	-	1	2		Normal mode
		-	20	100		Low Power mode
T_{BOD_SU}[*2]	BOD startup time	-	1000	-		-
T_{BOD_RE}[*1]	BOD respond time	-	10	-		Normal mode
		-	20000	-		Low Power mode
R_{VDDR}[*1]	VDD rise time rate	-	10	-	µS/V	POR Enabled

R_{VDDF}[*1]	VDD fall time rate	-	10	-		POR Enabled
		-	0.66-	-		LVR Enabled
		-	133	-		LVRLP Enabled
		-	66.67	-		BOD 1.6V Enabled, Normal mode
		-	28.57	-		BOD 1.8V Enabled, Normal mode
		-	18.18	-		BOD 2.0V Enabled, Normal mode
		-	13.33	-		BOD 2.2V Enabled, Normal mode
		-	10.53	-		BOD 2.4V Enabled, Normal mode
		-	8.70	-		BOD 2.6V Enabled, Normal mode
		-	7.41	-		BOD 2.8V Enabled, Normal mode
		-	6.45	-		BOD 3.0V Enabled, Normal mode
		-	133333.3	-		BOD 1.6V Enabled, Low Power mode
		-	57142.86	-		BOD 1.8V Enabled, Low Power mode
		-	36363.64	-		BOD 2.0V Enabled, Low Power mode
		-	26666.67	-		BOD 2.2V Enabled, Low Power mode
		-	21052.63	-		BOD 2.4V Enabled, Low Power mode
		-	17391.3	-		BOD 2.6V Enabled, Low Power mode
		-	14814.81	-		BOD 2.8V Enabled, Low Power mode
		-	12903.23	-		BOD 3.0V Enabled, Low Power mode

Notes:

1. Guaranteed by characterization, not tested in production.
2. Design for specified applcaiton.

Table 9.5-1 Reset and Power Control Unit

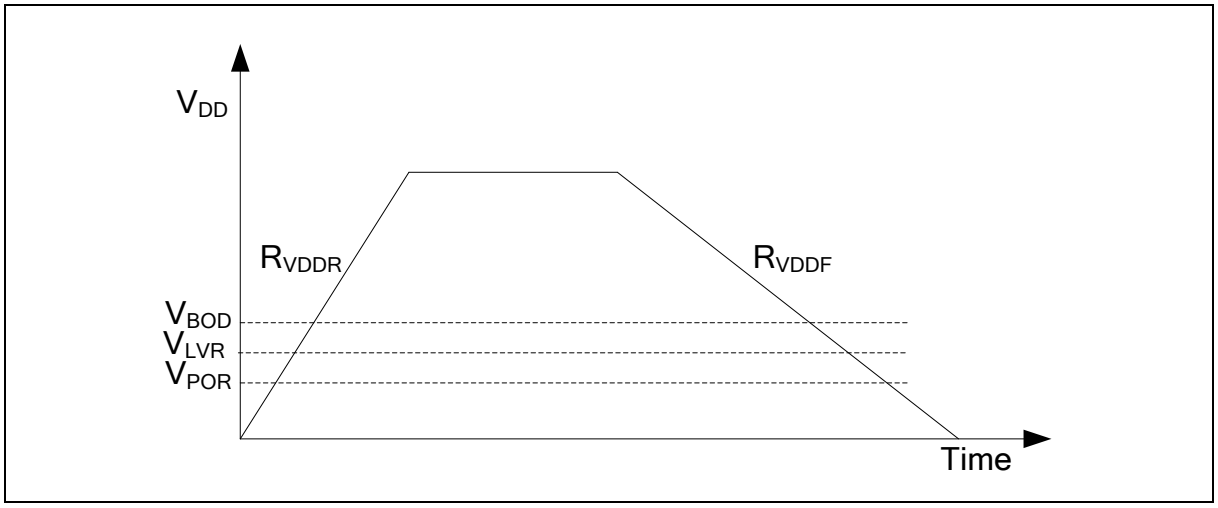


Figure 9.5-1 Power Ramp Up/Down Condition

9.5.3 12-bit SAR Analog To Digital Converter (ADC)

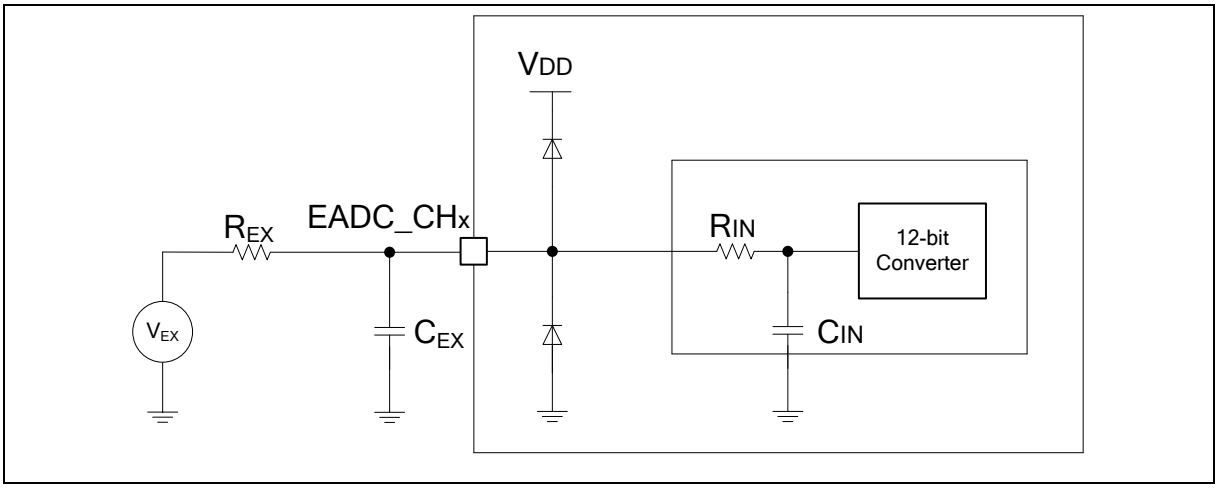
Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
T_A	Temperature	-40	-	85	℃	
AV_{DD}	Analog operating voltage	1.7	-	3.6	V	$V_{DD} = AV_{DD}$
V_{REF}	Reference voltage	1.7	-	AV_{DD}	V	
V_{IN}	ADC channel input voltage	0	-	V_{REF}	V	
I_{ADC}[*1]	ADC Operating current (AV_{DD} + V_{REF} current)	-	330	-	μA	$AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V F_{ADC} = 90 MHz $T_{CONV} = 20 * T_{ADC}$
N_R	Resolution	12			Bit	
F_{ADC}[*1] $1/T_{ADC}$	ADC Clock frequency	12	-	60	MHz	1.7V ≦ V_{REF} ≦ 3.6V
		12	-	90	MHz	2.5V ≦ V_{REF} ≦ 3.6V
T_{SMP}	Sampling Time	1	-	256	$1/F_{ADC}$	T_{SMP} = (EXTSMPT(EADC_SCTLx[31:24]) + 1) * T_{ADC}
T_{CONV}	Conversion time	20	-	275	$1/F_{ADC}$	$T_{CONV} = T_{SMP} + 19 * T_{ADC}$
F_{SPS}[*1]	Sampling Rate	0.6	-	3	MSPS	1.7V ≦ V_{REF} ≦ 3.6V $F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(EADC_SCTLx[31:24]) = 0
		0.6	-	4.5	MSPS	2.5V ≦ V_{REF} ≦ 3.6V $F_{SPS} = F_{ADC} / T_{CONV}$ EXTSMPT(EADC_SCTLx[31:24]) = 0
T_{EN}	Enable to ready time	5	-	-	$1/F_{ADC}$	
INL[*1]	Integral Non-Linearity Error	-4	-	+3	LSB	$V_{REF} = AV_{DD}$
DNL[*1]	Differential Non-Linearity Error	-1	-	+2	LSB	$V_{REF} = AV_{DD}$
E_G[*1]	Gain error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_O[*1]$_T$	Offset error	-4	-	+4	LSB	$V_{REF} = AV_{DD}$
E_A[*1]	Absolute Error	-5	-	+6	LSB	$V_{REF} = AV_{DD}$
ENOB[*1]	Effective number of bits	-	10.0	-	bits	F_{ADC} = 90 MHz $AV_{DD} = V_{DD} = V_{REF}$ = 3.3 V Input Frequency = 20 kHz T_A = 25 °C
SINAD[*1]	Signal-to-noise and distortion ratio	-	60.2	-	dB	
SNR[*1]	Signal-to-noise ratio	-	60.2	-		
THD[*1]	Total harmonic distortion	-	-74	-		

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
C_{IN}[*1]	Internal Capacitance	-	2.9	-	pF	
R_{IN}[*1]	Internal Switch Resistance	-	-	500	Ω	
R_{EX}[*1]	External input impedance	-	-	23	kΩ	F_{ADC} = 90 MHz T_{SMP} = 275/F_{ADC} T_A = 25 °C

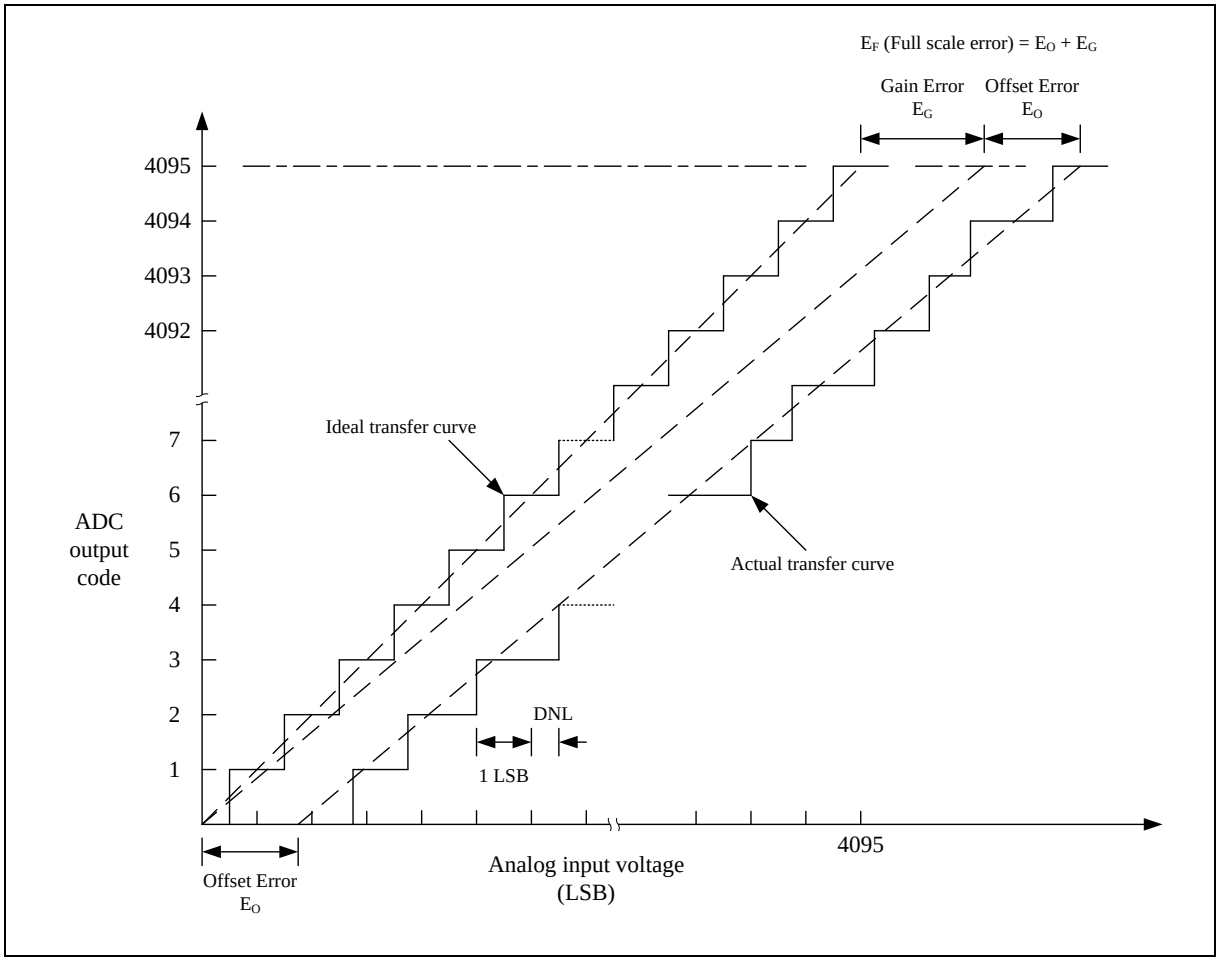
Notes:

1. Guaranteed by characterization result, not tested in production.
2. R_{EX} max formula is used to determine the maximum external impedance allowed for 1/4 LSB error. N = 12 (based on 12-bit resoluton) and k is the number of sampling clocks (T_{SMP}). C_{EX} represents the capacitance of PCB and pad and is combined with R_{EX} into a low-pass filter. Once the R_{EX} and C_{EX} values are too large, it is possible to filter the real signal and reduce the ADC accuracy.

$$R_{EX} < \frac{k}{f_{ADC} \times (C_{IN} + C_{EX}) \times \ln(2^{N+2})} - R_{IN}$$



Note: Injection current is a important topic of ADC accuracy. Injecting current on any analog input pins should be avoided to protect the conversion being performed on another analog input. It is recommended to add Schottky diodes (pin to ground and pin to power) to analog pins which may potentially inject currents.



Note: The INL is the peak difference between the transition point of the steps of the calibrated transfer curve and the ideal transfer curve. A calibrated transfer curve means it has calibrated the offset and gain error from the actual transfer curve.

9.5.4 Digital to Analog Converter (DAC)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	-
N_R	Resolution		12		bit	-
V_{REF}	Reference supply voltage	1.5	-	3.6	V	$V_{REF} \le AV_{DD}$
DNL[*2]	Differential non-linearity error	-2	-	2	LSB	12-bit mode
INL[*2]	Integral non-linearity error	-4	-	4	LSB	12-bit mode
OE[*2]	Offset Error	-8	-	8	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
GE[*2]	Gain Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
AE[*2]	Absolute Error	-10	-	10	LSB	12-bit mode DACOUT buffer ON
		-4	-	4	LSB	12-bit mode DACOUT buffer OFF
V_O[*1]	Output Voltage	0.2		AVDD-0.2	V	DACOUT buffer ON
		1 LSB		VREF – 1 LSB		DACOUT buffer OFF
R_{LOAD}[*2] [*3]	Resistive load	7.5	-	-	kΩ	DACOUT buffer ON
R_O[*2]	Output impedance	-	9.8	-	kΩ	DACOUT buffer OFF
C_{LOAD}[*2] [*4]	Capacitive load	-	-	20	pF	DACOUT buffer OFF
I_{DAC_AVDD}[*2]	DAC operating current on AV_{DD} supply	-	132	-	μA	AV_{DD} = 3.6V, no load, lowest code (0x000)
		-	338	-		AV_{DD} = 3.6V, no load, middle code (0x800)
I_{DAC_VREF}[*2]	DAC operating current on V_{REF} supply	-	130	140	μA	V_{REF} =3.6V, no load, middle code (0x800)
T_B[*2]	Settling Time	-	5	6	μs	Full scale: for a 12-bit input code transition between the lowest and the highest input codes when DAC_OUT reaches final value +/-1 LSB,

						C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5kΩ
F_S	Update Rate	-	-	1	M_{SPS}	Max. frequency for a correct DAC_OUT change from core i to i+1LSB, C_{LOAD} ≤ 50pF, R_{LOAD} ≥ 5kΩ
T_{WAKEUP}	Wake-up Time	-	5	10	µs	Wakeup time from OFF state. Input code between lowest and highest possible codes. DAC clock source = 1MHz
PSRR[*1]	Power Supply Rejection Ratio	-	-60	-40	dB	No R_{LOAD}, C_{LOAD} = 50pF

Note:

1. Guaranteed by design, not tested in production
2. Guaranteed by characteristic, not tested in production.
3. Resistive load between DACOUT and AV_{SS}.
4. Capacitive load at DACOUT pin.

9.5.5 Analog Comparator Controller (ACMP)

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
AV_{DD}	Analog supply voltage	1.8	-	3.6	V	V_{DD} = AV_{DD}
T_A	Temperature	-40	-	85	℃	
I_{ACMP}[*2]	ACMP operating current	-	70	-	μA	MODESEL = 11
		-	35	-		MODESEL = 10
		-	2	-		MODESEL = 01
		-	1	-		MODESEL = 00
V_{CM}[*2]	Input common mode voltage range	0.1	1/2 AV_{DD}	AV_{DD} -0.1		
V_{DI}[*2]	Differential input voltage sensitivity	20	-	-	mV	Hysteresis disable (HYSSEL = 00)
V_{offset}[*2]	Input offset voltage	-	±5	±10	mV	MODESEL =10~11 Hysteresis disable (HYSSEL = 00)
		-	±10	±20	mV	MODESEL =00~01 Hysteresis disable (HYSSEL = 00)
V_{hys}[*2]	Hysteresis window	-	0	-	mV	HYSSEL = 000
		10	20	40		HYSSEL = 010
		20	40	60		HYSSEL = 100
A_v[*1]	DC voltage Gain	51	70	-	dB	
T_d[*2]	Propagation delay	-	30	60	nS	MODESEL = 11
		-	100	150		MODESEL = 10
		-	0.8	2	μS	MODESEL = 01
		-	1.5	3.5		MODESEL = 00
T_{Setup}[*2]	Setup time	-	-	1	μS	MODESEL = 11
		-	-	1		MODESEL = 10
		-	-	20		MODESEL = 01
		-	-	20		MODESEL = 00
A_{CRV}[*2]	CRV output voltage	-1.6	-	1.6	%	AVDD x (1/6+CRVCTL/24)
T_{SETUP_CRV}[*2]	Setup time	-	-	0.6	μS	CRV output voltage settle to ±5%
I_{DD_CRV}[*2]	Operating current	-	30	50	μA	

Notes:

1.Guaranteed by design, not tested in production

2.Guaranteed by characteristic, not tested in production

Table 9.5-2 ACMP Characteristics

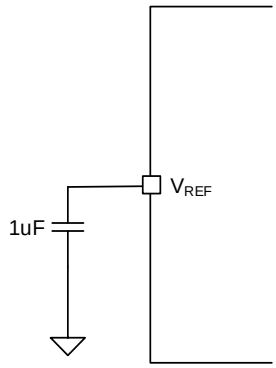
9.5.6 Internal Voltage Reference

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{REF_INT}	Internal reference voltage	1.584	1.6	1.616	V	AV_{DD} >= 2.0 V
		1.980	2.0	2.020		AV_{DD} >= 2.2 V
		2.475	2.5	2.525		AV_{DD} >= 2.7 V
		2.970	3.0	3.030		AV_{DD} >= 3.2 V
T_S[*1]	Stable time	-	-	2	mS	C_L =4.7 uF, V_{REF} initial=0, Preload is enabled.
		-	-	48	uS	C_L =0.1 uF, V_{REF} initial=0, Preload is enabled.
I_{VREF_INT}[*1]	V_{REF_INT} operating current	-	70	-	uA	

Note:

1. Guaranteed by characterization, not tested in production



Note: V_{REF_INT} is only supported while package includes V_{REF} pin with external capacitor.

Figure 9.5-2 Typical Connection with Internal Voltage Reference

9.5.7 Temperature Sensor

The maximum values are obtained for V_{DD} = 3.6 V and maximum ambient temperature (T_A), and the typical values for T_A= 25 °C and V_{DD} = 3.3 V unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{TEMP_OS}[*1]	Temperature sensor offset voltage	653	674	694	mV	T_A = 25°C
T_C[*1]	Temperature Coefficient	-1.91	-1.82	-1.73	mV/°C	
T_S[*2]	Stable time	-	-	1	µS	
T_{TEMP_ADC}[*1]	ADC sampling time when reading the temperature	3	-	-	µS	
I_{TEMP}[*1]	Temperature sensor operating current	-	16	25	µA	

Note:

1. Guaranteed by characterization, not tested in production
2. Guaranteed by design, not tested in production
3. V_{TEMP} (mV) = T_C (mV/°C) x Temperature (°C) + V_{TEMP_OS} (mV)

9.6 Communications Characteristics

9.6.1 I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.3	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

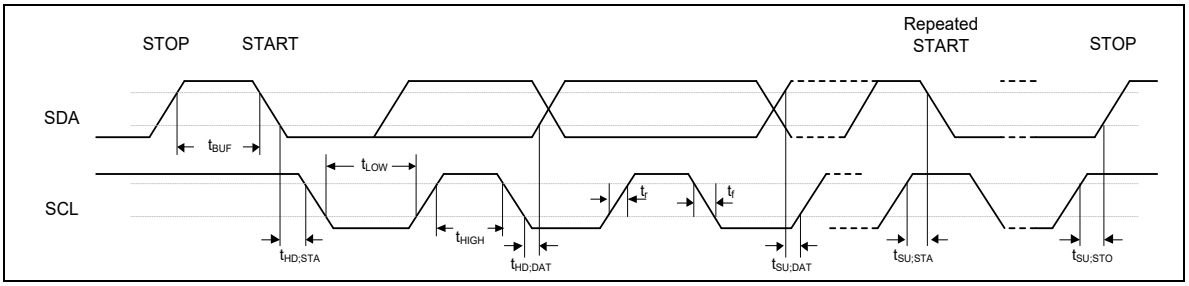


Figure 9.6-1 I²C Timing Diagram

9.6.2 SPI Dynamic Characteristics

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} $1/ T_{SPICLK}$	SPI clock frequency	-	-	100	MHz	3.0 V ≤ VD ≤ 3.6 V, C_L = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	4	-	-	nS	
t_V	Data output valid time	-	-	2	nS	3.0 V ≤ VDD ≤ 3.6V, C_L = 30 pF

Note:

2. Guaranteed by design, not tested in production.

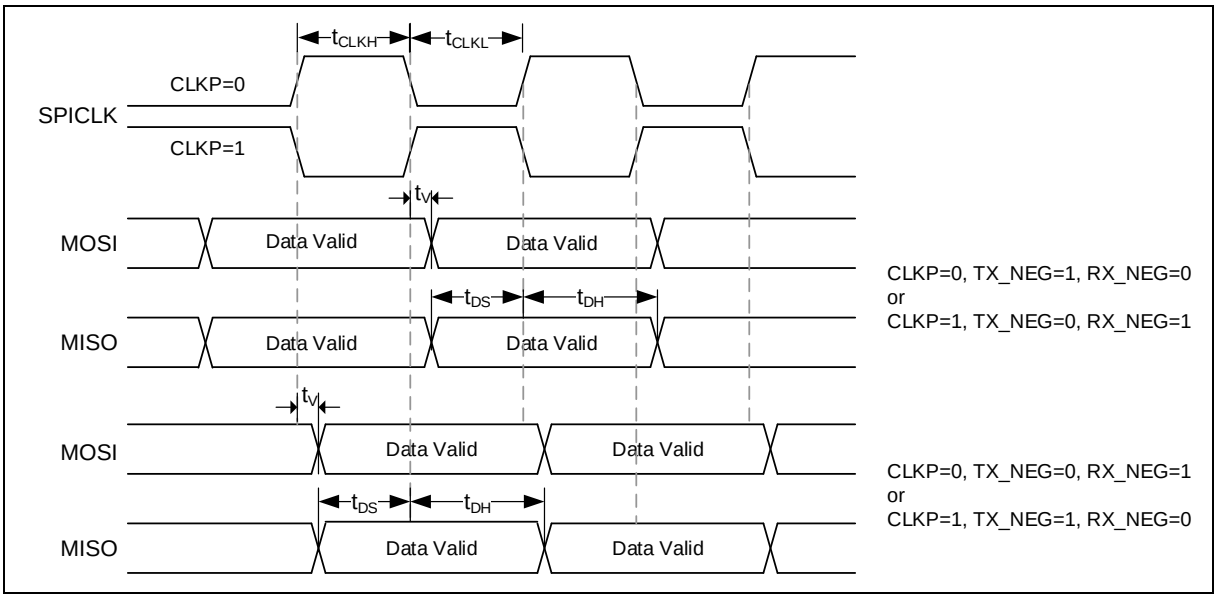


Figure 9.6-2 SPI Master Mode Timing Diagram

Symbol	Parameter	Specificaitons[*1]				Test Conditions
		Min	Typ	Max	Unit	
F_{SPICLK} 1/ T_{SPICLK}	SPI clock frequency	-	-	20	MHz	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF
t_{CLKH}	Clock output High time	T_{SPICLK} / 2			nS	
t_{CLKL}	Clock output Low time	T_{SPICLK} / 2			nS	
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	nS	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	nS	
t_{DS}	Data input setup time	0	-	-	nS	
t_{DH}	Data input hold time	6	-	-	nS	
t_V	Data output valid time	-	-	13	nS	3.0 V ≤ VDD ≤ 3.6 V, CL = 30 pF

Note:

1. Guaranteed by design, not tested in production.

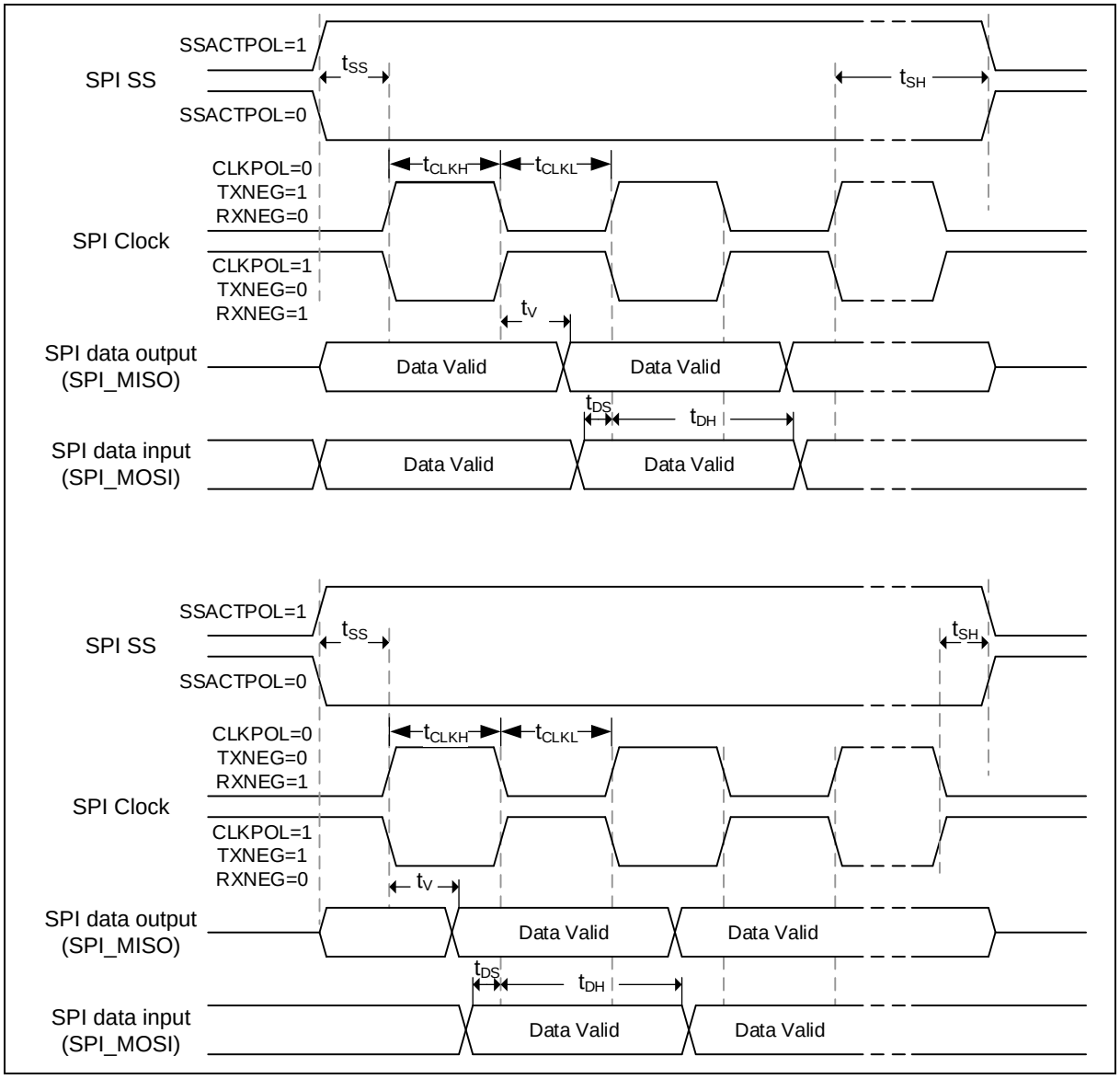


Figure 9.6-3 SPI Slave Mode Timing Diagram

9.6.3 I²S Dynamic Characteristics

Symbol	Parameter	Min	Max	Unit	Test Conditions
$t_{w(CKH)}$	I²S clock high time	40	-	ns	Master f_{PCLK} = MHz, data: 24 bits, audio frequency = 256 kHz
$t_{w(CKL)}$	I²S clock low time	40	-		
$t_{v(WS)}$	WS valid time	4	16		Master mode
$t_{h(WS)}$	WS hold time	1	-		Master mode
$t_{su(WS)}$	WS setup time	24	-		Slave mode
$t_{h(WS)}$	WS hold time	0	-		Slave mode
$DuCy_{(SCK)}$	I²S slave input clock duty cycle	30	70	%	Slave mode
$t_{su(SD\_MR)}$	Data input setup time	10	-	ns	Master receiver
$t_{su(SD\_SR)}$		7	-		Slave receiver
$t_{h(SD\_MR)}$	Data input hold time	7	-		Master receiver
$t_{h(SD\_SR)}$		4	-		Slave receiver
$t_{v(SD\_ST)}$	Data output valid time	-	10		Slave transmitter (after enable edge)
$t_{h(SD\_ST)}$	Data output hold time	4	-		Slave transmitter (after enable edge)
$t_{v(SD\_MT)}$	Data output valid time	-	4		Master transmitter (after enable edge)
$t_{h(SD\_MT)}$	Data output hold time	0	-		Master transmitter (after enable edge)

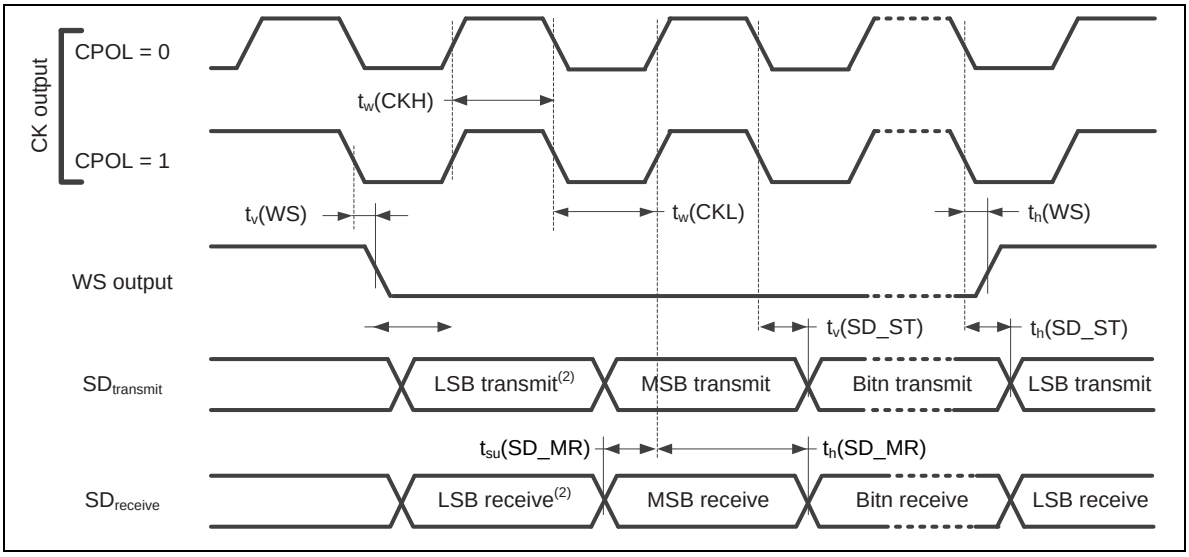


Figure 9.6-4 I²S Master Mode Timing Diagram

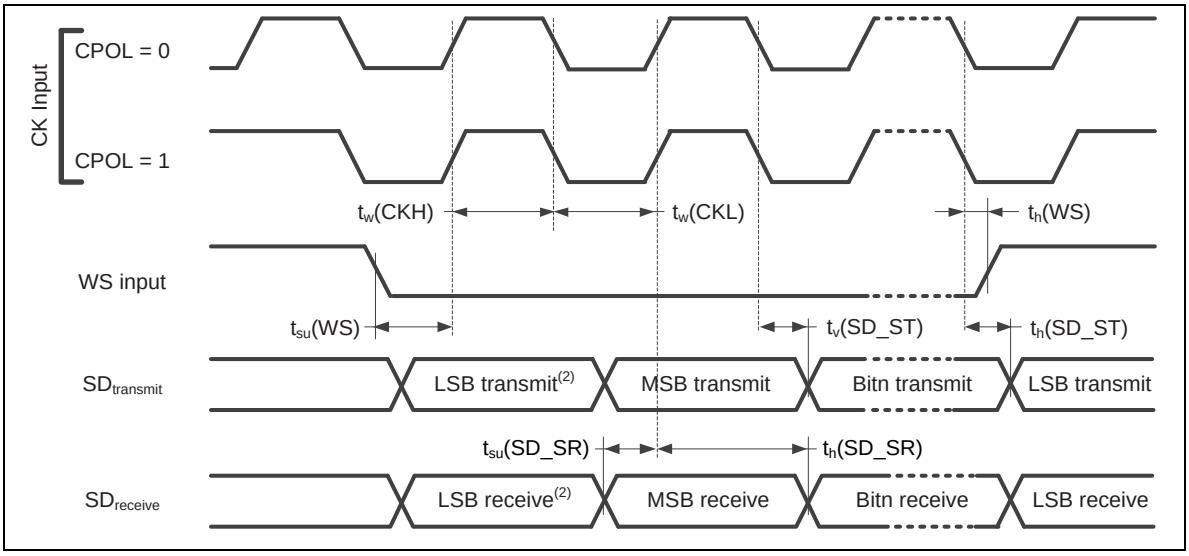


Figure 9.6-5 I²S Slave Mode Timing Diagram

9.6.4 USCI - I²C Dynamic Characteristics

Symbol	Parameter	Standard Mode[1][2]		Fast Mode[1][2]		Unit
		Min.	Max.	Min.	Max.	
t_{LOW}	SCL low period	4.7	-	1.2	-	uS
t_{HIGH}	SCL high period	4	-	0.6	-	uS
$t_{SU;\ STA}$	Repeated START condition setup time	4.7	-	1.2	-	uS
$t_{HD;\ STA}$	START condition hold time	4	-	0.6	-	uS
$t_{SU;\ STO}$	STOP condition setup time	4	-	0.6	-	uS
t_{BUF}	Bus free time	4.7[3]	-	1.2[3]	-	uS
$t_{SU;DAT}$	Data setup time	250	-	100	-	nS
$t_{HD;DAT}$	Data hold time	0[4]	3.45[5]	0[4]	0.8[5]	uS
t_r	SCL/SDA rise time	-	1000	20+0.1C_b	300	nS
t_f	SCL/SDA fall time	-	300	-	300	nS
C_b	Capacitive load for each bus line	-	400	-	400	pF

Note:

1. Guaranteed by characteristic, not tested in production
2. HCLK must be higher than 2 MHz to achieve the maximum standard mode I²C frequency. It must be higher than 8 MHz to achieve the maximum fast mode I²C frequency.
3. I²C controller must be retriggered immediately at slave mode after receiving STOP condition.
4. The device must internally provide a hold time of at least 300 ns for the SDA signal in order to bridge the undefined region of the falling edge of SCL.
5. The maximum hold time of the Start condition has only to be met if the interface does not stretch the low period of SCL signal.

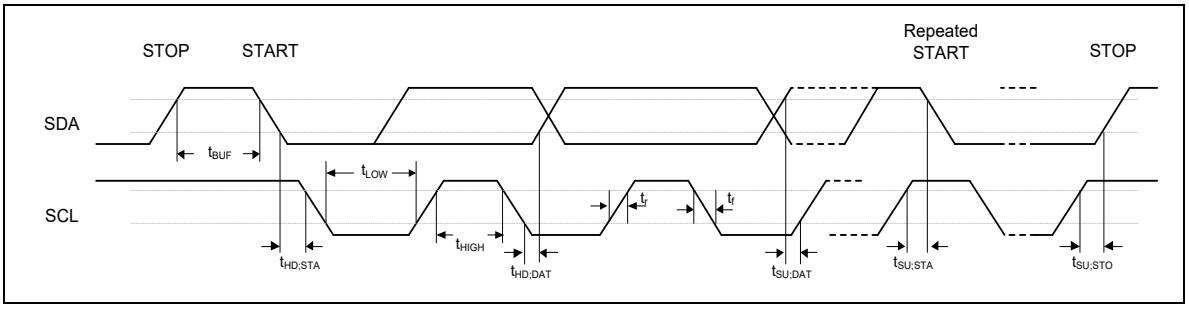


Figure 9.6-6 I²C Timing Diagram

9.6.5 USCI - SPI Dynamic Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI MASTER MODE (V_{DD} = 3.0~3.6 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	0	1	ns
SPI MASTER MODE (V_{DD} = 1.8~2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]			T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]			T_{SPICLK} / 2	ns
t_{DS}	Data setup time	0	-	-	ns
t_{DH}	Data hold time	2	-	-	ns
t_V	Data output valid time	-	-	1	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

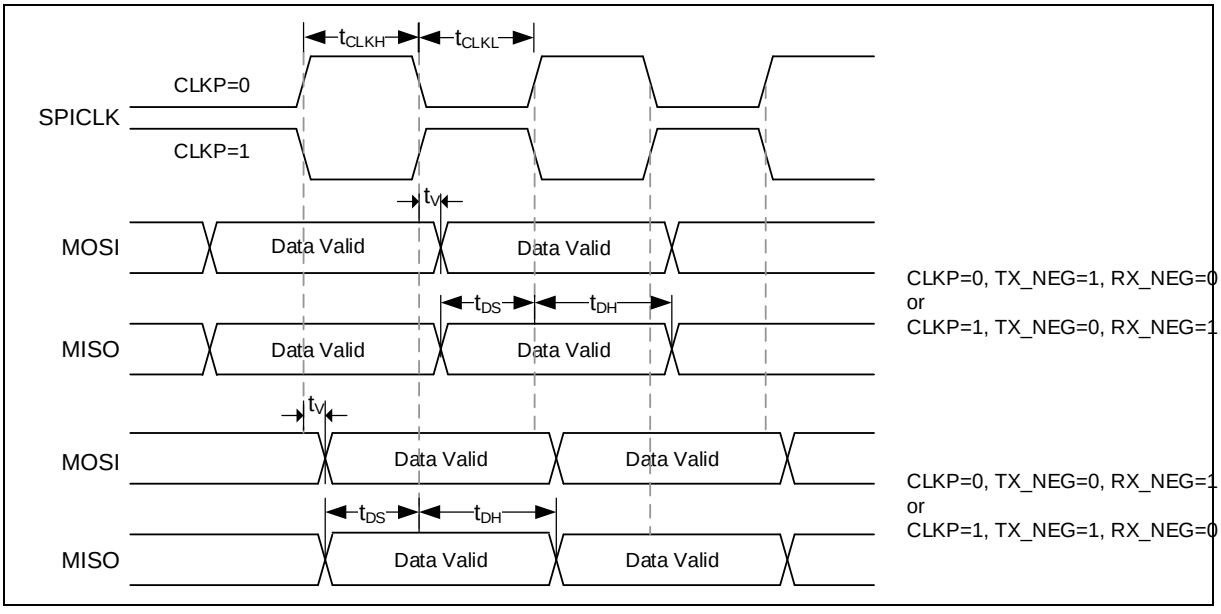


Figure 9.6-7 SPI Master Mode Timing Diagram

Symbol	Parameter	Min.	Typ.	Max.	Unit
SPI SLAVE MODE (V_{DD} = 3.0~3.6V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-		T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 2ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		8	ns
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
SPI SLAVE MODE (V_{DD} = 1.8 V ~ 2.0 V, 30 PF LOADING CAPACITOR)					
t_{CLKH}	Clock output High time [*1]	-	-	T_{SPICLK} / 2	ns
t_{CLKL}	Clock output Low time [*1]	-	-	T_{SPICLK} / 2	ns
t_{SS}	Slave select setup time	1 T_{SPICLK} + 3ns	-	-	ns
t_{SH}	Slave select hold time	1 T_{SPICLK}	-	-	ns
t_{DS}	Data input setup time	0	-	-	ns
t_{DH}	Data input hold time	2	-	-	ns
t_V	Data output valid time	-		10	ns

Note:

1. The minimum clock period for SPICLK is 10.4 ns (96 MHz).

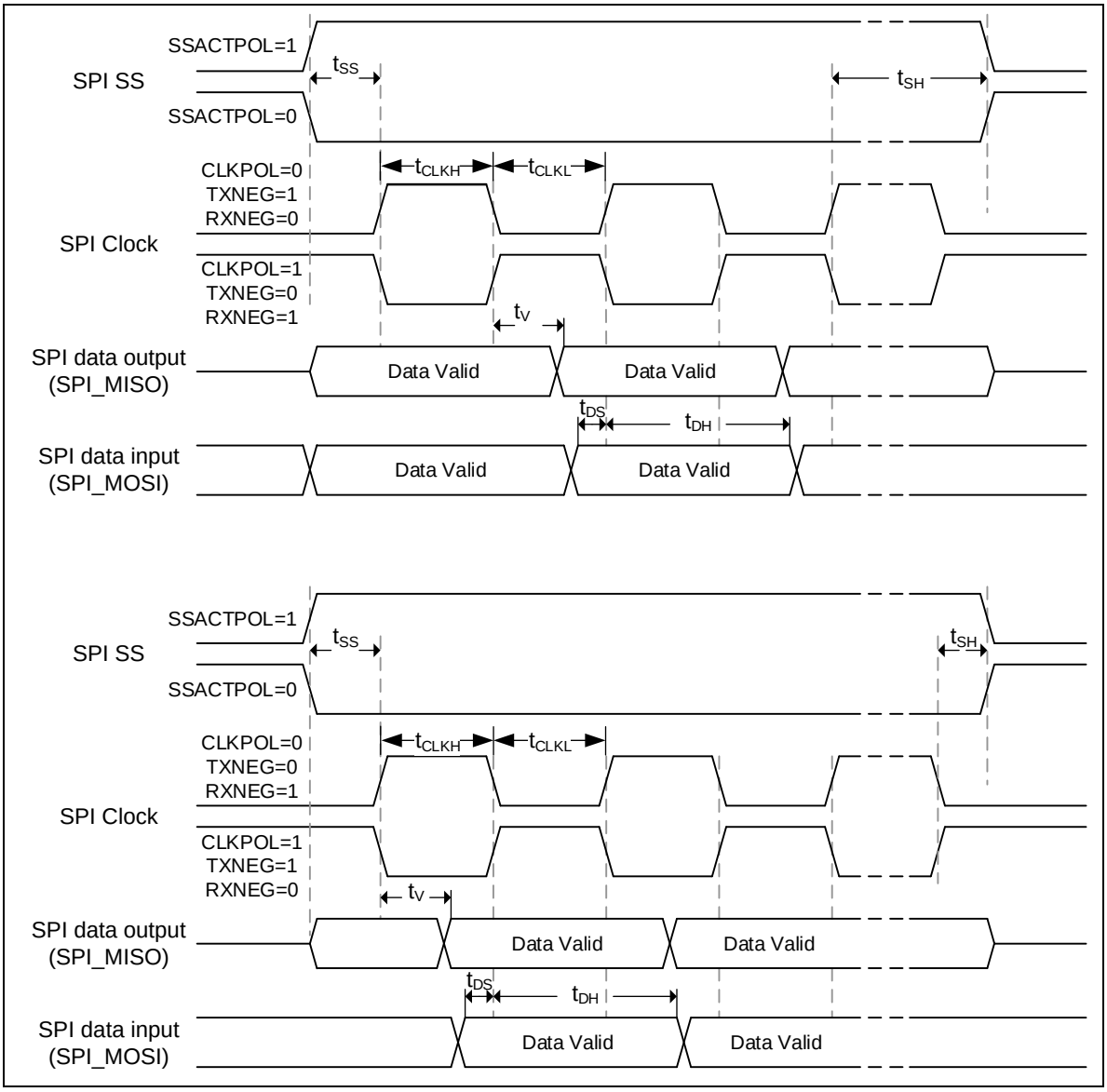


Figure 9.6-8 SPI Slave Mode Timing Diagram

9.6.6 USB Characteristics

9.6.6.1 USB High-Speed Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_{FR}	High Speed Driver Rise Time	500	-		ps	CL=5pF
T_{FF}	High Speed Driver Fall Time	500	-		ps	CL=5pF
T_{FRFF}	Rise and Fall Time Matching	90		111.11	%	$T_{FRFF}=T_{FR}/T_{FF}$

9.6.7 Ethernet Characteristics

9.6.7.1 RMII Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_REFCLK}$	RMII_REFCLK Period	-	20.0 +/- 50 ppm	-	ns	-
$T_{H\_RMII\_REFCLK}$	RMII_REFCLK High Time	8.0	10.0	12.0	ns	-
$T_{L\_RMII\_REFCLK}$	RMII_REFCLK Low Time	8.0	10.0	12.0	ns	-
$T_{DLY\_RMII\_TX}$	RMII_REFCLK Rising to Valid RMII_TXEN, RMII_TXDATA0 and RMII_TXDATA1 Delay	-	-	10	ns	-
$T_{SU\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Setup Time to RMII_REFCLK Rising	5	-	-	ns	-
$T_{HD\_RMII\_RX}$	RMII_CRSDV, RMII_RXDATA0 and RMII_RXDATA1 Hold Time from RMII_REFCLK Rising	2	-	-	ns	-

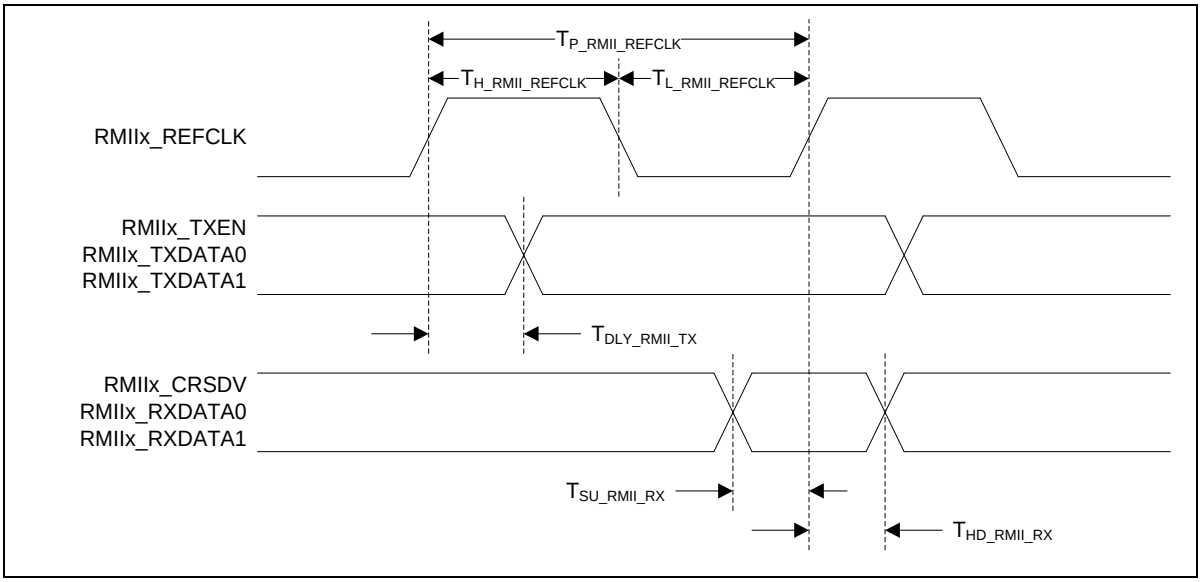


Figure 9.6-9 RMII Interface Timing Diagram

9.6.7.2 Ethernet PHY Management Interface Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_RMII\_MDC}$	RMII_MDC Period	400	-	-	ns	-
$T_{H\_RMII\_MDC}$	RMII_MDC High Time	200	-	-	ns	-
$T_{L\_RMII\_MDC}$	RMII_MDC Low Time	200	-	-	ns	-
$T_{DLY\_RMII\_MDIOWR}$	RMII_MDC Falling to Valid RMII_MDIO Delay	-	-	10	ns	-
$T_{SU\_RMII\_MDIORD}$	RMII_MDIO Setup Time to RMII_MDC Rising	10	-	-	ns	-
$T_{HD\_RMII\_MDIORD}$	RMII_MDIO Hold Time from RMII_MDC Rising	10	-	-	ns	-

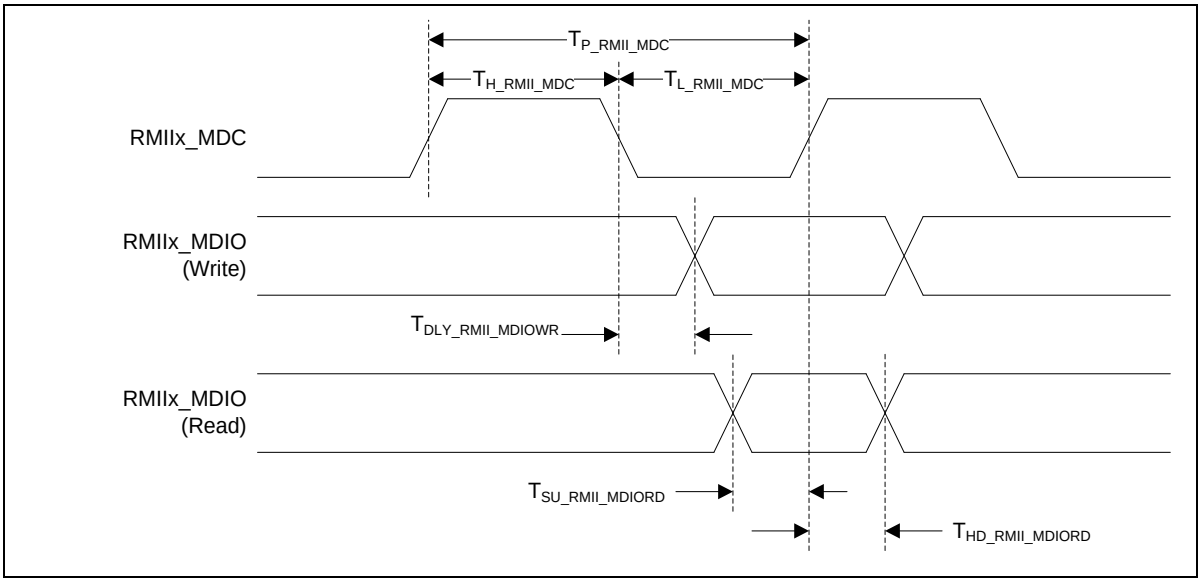


Figure 9.6-10 Ethernet PHY Management Interface Timing Diagram

9.6.8 SDIO Characteristics

9.6.8.1 SDIO Default Mode Timing

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period (Data Transfer Mode)	40	-	-	ns	-
$T_{P\_SD\_CLK\_ID}$	SD_CLK Period (Identification Mode)	2,500	-	-	ns	
$T_{H\_SD\_CLK}$	SD_CLK High Time	-	20	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	-	20	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	5	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	5	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-

Note:

1. Guaranteed by characterization result, not tested in production.

Table 9.6-1 SDIO Default Mode Timing

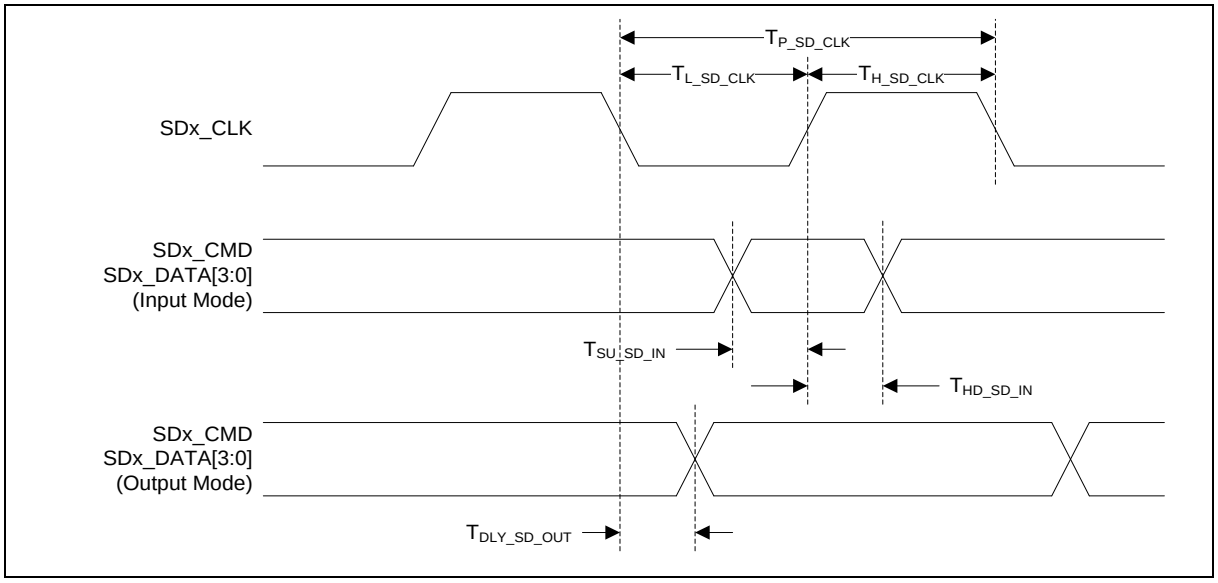


Figure 9.6-11 SDIO Default Mode

9.6.8.2 SDIO Dynamic characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_SD\_CLK}$	SD_CLK Period	20	-	-	ns	-
$T_{H\_SD\_CLK}$	SD_CLK High Time	7	-	-	ns	-
$T_{L\_SD\_CLK}$	SD_CLK Low Time	7	-	-	ns	-
$T_{SU\_SD\_IN}$	SD_DATA Setup Time to SD_CLK Rising	6	-	-	ns	-
$T_{HD\_SD\_IN}$	SD_DATA Hold Time from SD_CLK Rising	2	-	-	ns	-
$T_{DLY\_SD\_OUT}$	SD_CLK Falling to Valid SD_DATA Delay	-	-	14	ns	-
$T_{HD\_SD\_OUT}$	SD_DATA Hold Time from SD_CLK Rising	2.5	-	-	ns	-

Note:

1. Guaranteed by characterization result, not tested in production.

Table 9.6-2 SDIO Dynamic Characteristics

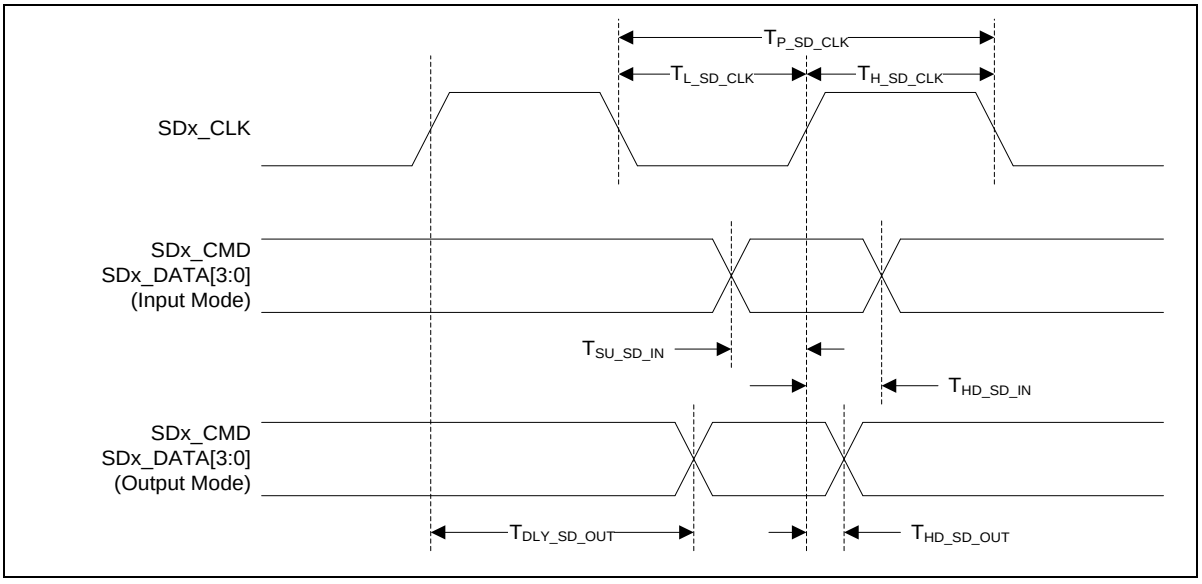


Figure 9.6-12 SDIO High-speed Mode

9.6.9 Camera Capture Interface (CCAP) Characteristics

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
$T_{P\_CCAP\_PCLK}$	CCAP_PCLK Period	20	-	-	ns	
$T_{H\_CCAP\_PCLK}$	CCAP_PCLK High Time	-	10.0	-	ns	
$T_{L\_CCAP\_PCLK}$	CCAP_PCLK Low Time	-	10.0	-	ns	
$T_{SU\_CCAP\_IN}$	CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Setup Time to CCAP_PCLK Rising	4	-	-	ns	
$T_{HD\_CCAP\_IN}$	CCAP_HSYNC, CCAP_VSYNC, CCAP_FIELD and CCAP_DATA Hold Time from CCAP_PCLK Rising	1	-	-	ns	

Note:

1.Guaranteed by design.

Table 9.6-3 Camera Capture Interface Timing

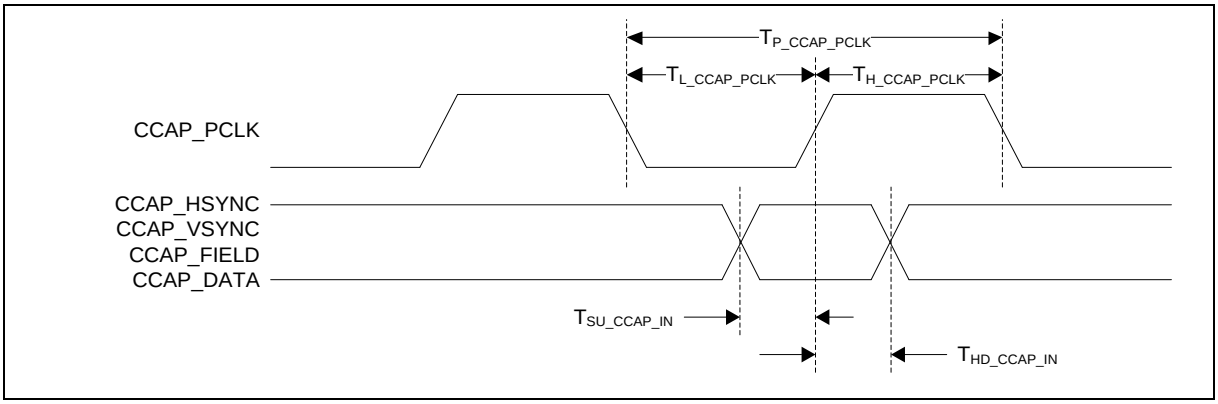


Figure 9.6-13 Camera Capture Interface Timing Diagram

9.6.10 CAN FD Characteristics

Symbol	Parameter	Min	Max [*1]	Unit	Test Conditions
t_{CAN_TXD}	TXD output delay (Normal Slew Rate)	-	8.5	nS	2.7 V ≤ VDD ≤ 3.6V , C_L = 30 pF
t_{CAN_RXD}	RXD input delay	-	7.2	nS	2.7 V ≤ VDD ≤ 3.6V
Note: Guaranteed by design, not tested in production.					

9.7 Flash DC Electrical Characteristics

The devices are shipped to customers with the Flash memory erased.

Symbol	Parameter	Min[3]	Typ	Max	Unit	Test Condition
V_{FLA}[1]	Supply voltage	1.08	1.2	1.32	V	T_A = 25℃
T_{ERASE}	Page erase time	80	89.26	160	ms	
T_{PROG}	Program time	8	45.4	-	μs	
I_{DD1}	Read current	-	3.21	4.12	mA	
I_{DD2}	Program current	-	4	5	mA	
I_{DD3}	Erase current	-	4	5	mA	
N_{ENDUR}	Cycling Endurance	10,000	-	-	cycles[2]	T_J = -40℃~125℃
T_{RET}	Data retention	10	-	-	year	20 kcycle[2] , T_J = 85℃
		100	-	-	year	20 kcycle[2] , T_J = 25℃

Notes:

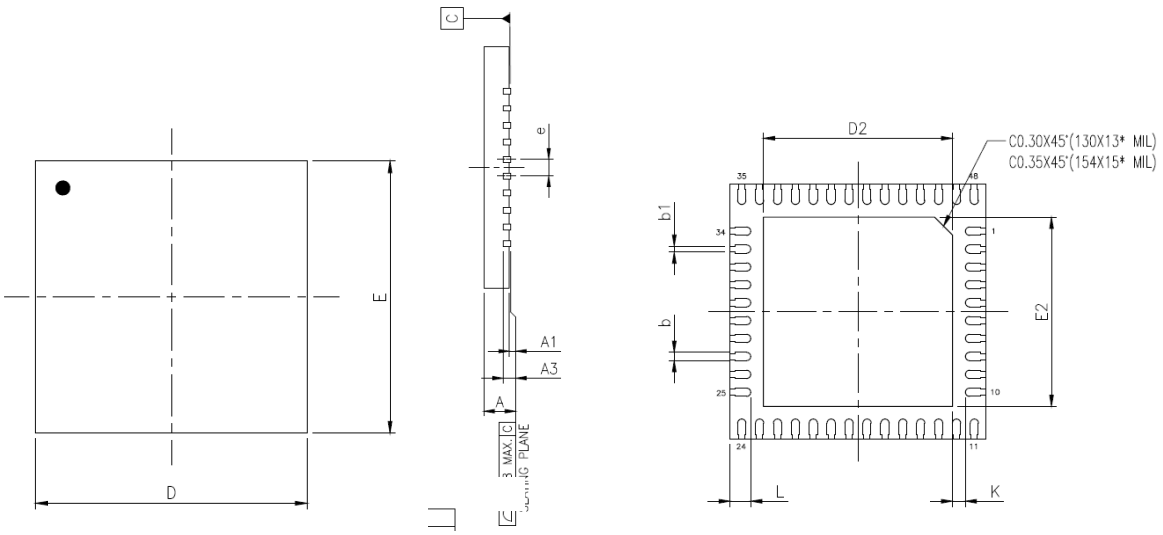
1. V_{FLA} is source from chip internal LDO output voltage.
2. Number of program/erase cycles. The flash data can only be programmed once at the same address after flash erase.
3. Guaranteed by design.

Table 9.7-1 Flash DC Electrical Characteristics

10 PACKAGE DIMENSIONS

Package is Halogen-free, RoHS-compliant and TSCA-compliant.

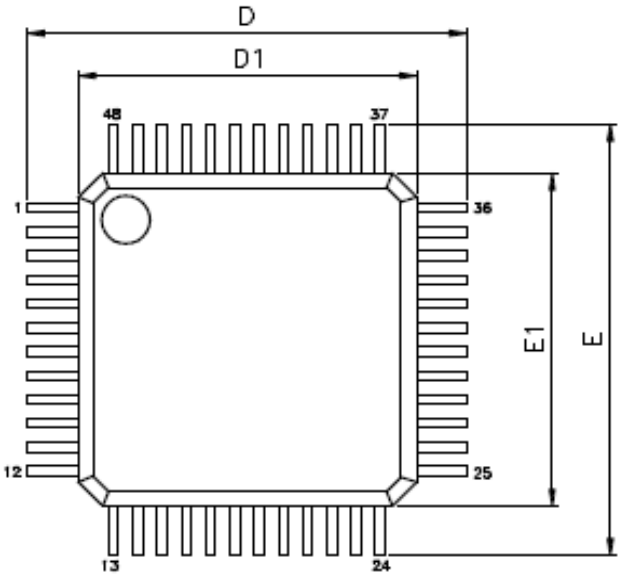
10.1 QFN48L 5x5mm, Thickness 0.80mm, Lead_Pitch 0.35mm, Lead_Length 0.40mm, EP Size 3.70x3.70mm

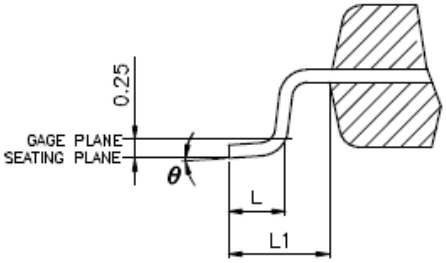


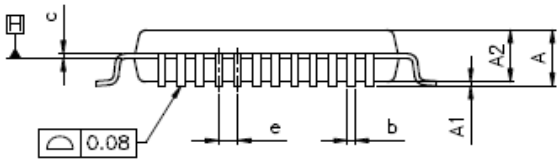
SYMBOLS	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.13	0.18	0.23
b1	0.07	0.12	0.17
D		5.00 BSC	
E		5.00 BSC	
e		0.35 BSC	
K	0.20	—	—

PAD SIZE	D2			E2			L		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
130X13* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45
154X15* MIL	3.65	3.70	3.75	3.65	3.70	3.75	0.35	0.40	0.45

10.2 LQFP48L 7x7mm, Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm



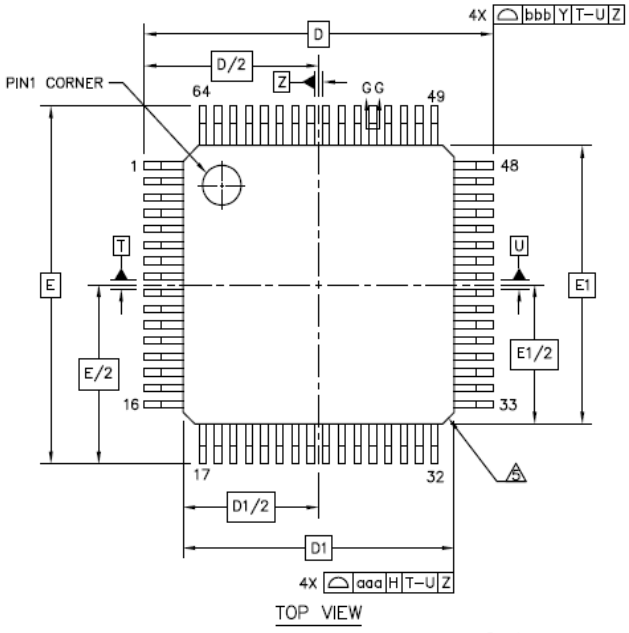


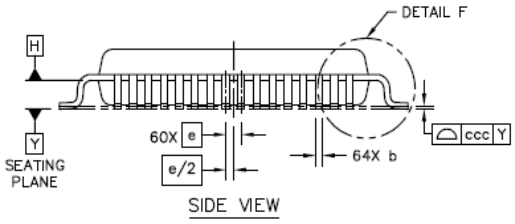


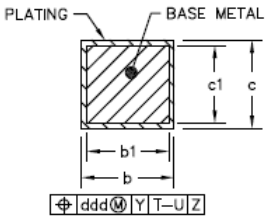
VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

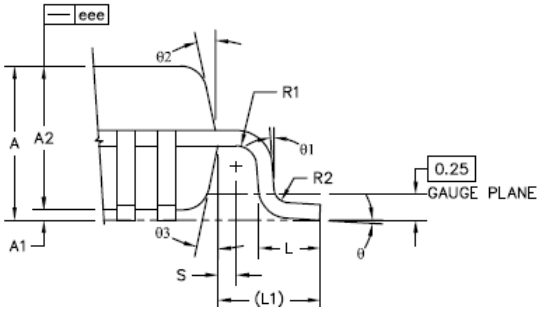
SYMBOLS	MIN.	NOM.	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
S	0.20	--	--
θ	0°	3.5°	7°
θ1	0°	--	--
θ2	11°	12°	13°
θ3	11°	12°	13°

10.3 LQFP64L 7x7mm, Thickness 1.40mm, Lead_Pitch 0.40mm, Lead_Length 1.00mm



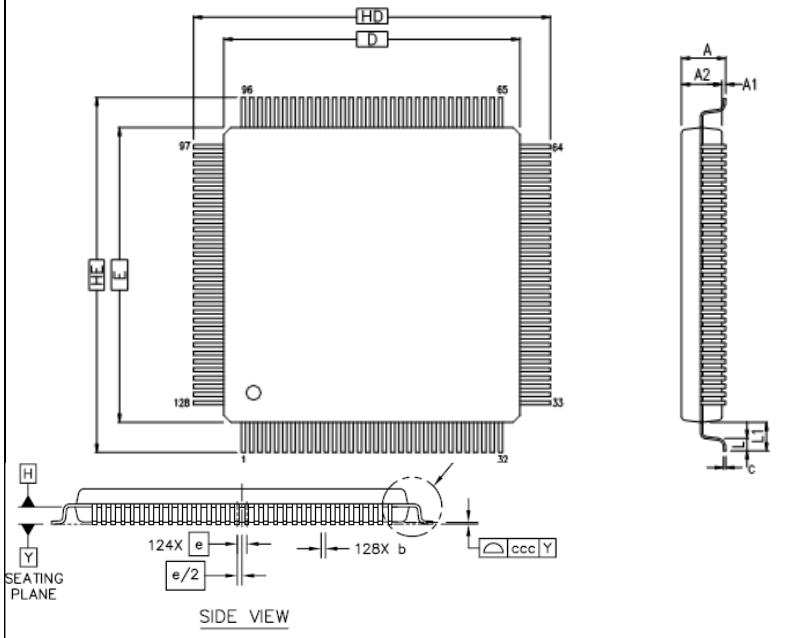






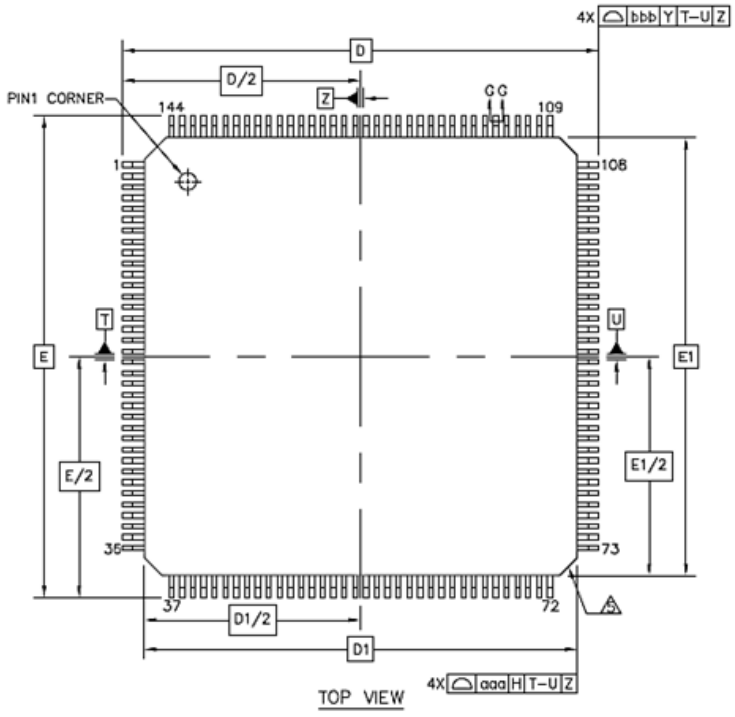
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

10.4 LQFP128L 14x14mm, Thickness 1.40mm, Lead_Pitch 0.40mm, Lead_Length 1.00mm

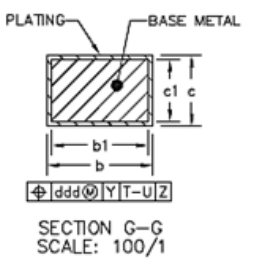


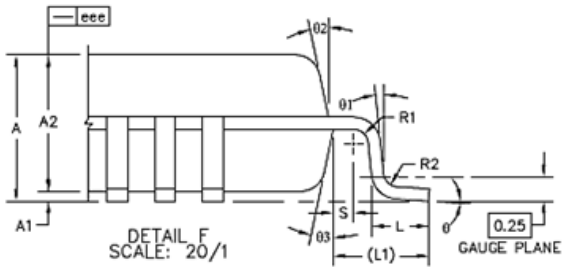
SYMBOL	MIN	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
HD	15.85	16.00	16.15
D	13.85	14.00	14.15
HE	15.85	16.00	16.15
E	13.85	14.00	14.15
b	0.13	0.16	0.23
e	-	0.40	-
θ°	0	3.5	7
c	0.09	-	0.20
L	0.45	0.60	0.75
L1	-	1.00	-
Y	-	-	0.10

10.5 LQFP144L 20x20mm, Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm

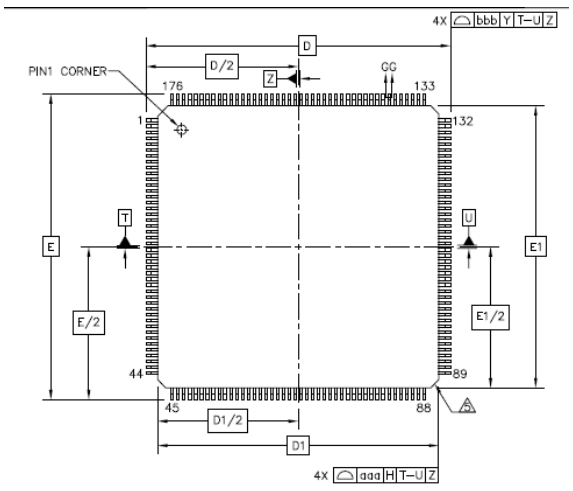


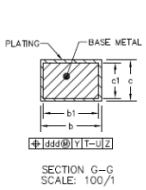
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	22 BSC		
	Y	E	22 BSC		
	X	D1	20 BSC		
	Y	E1	20 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.08		
MOLD FLATNESS		eee	0.05		

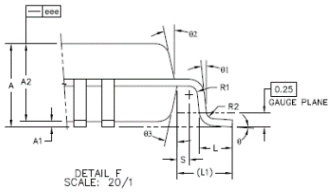




10.6 LQFP176L 24x24mm, Thickness 1.40mm, Lead_Pitch 0.50mm, Lead_Length 1.00mm







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.17	0.22	0.27
LEAD WIDTH		b1	0.17	0.2	0.23
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	26 BSC		
	Y	E	26 BSC		
	X	D1	24 BSC		
	Y	E1	24 BSC		
LEAD PITCH		e	0.5 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2 REF.		
PACKAGE EDGE TOLERANCE		aaa	0.1		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

11 ABBREVIATIONS

11.1 Abbreviations

Acronym	Description
ACMP	Analog Comparator Controller
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
APB	Advanced Peripheral Bus
AHB	Advanced High-Performance Bus
BOD	Brown-out Detection
CAN	Controller Area Network
CCAP	Camera Capture Interface
DAP	Debug Access Port
DES	Data Encryption Standard
EADC	Enhanced Analog-to-Digital Converter
EBI	External Bus Interface
EMAC	Ethernet MAC Controller
EPWM	Enhanced Pulse Width Modulation
FIFO	First In, First Out
FMC	Flash Memory Controller
FPU	Floating-point Unit
GPIO	General-Purpose Input/Output
HCLK	The Clock of Advanced High-Performance Bus
HIRC	12 MHz Internal High Speed RC Oscillator
HXT	4~24 MHz External High Speed Crystal Oscillator
IAP	In Application Programming
ICP	In Circuit Programming
ISP	In System Programming
LDO	Low Dropout Regulator
LIN	Local Interconnect Network
LIRC	10 kHz internal low speed RC oscillator (LIRC)
MPU	Memory Protection Unit
NVIC	Nested Vectored Interrupt Controller
PCLK	The Clock of Advanced Peripheral Bus
PDMA	Peripheral Direct Memory Access
PLL	Phase-Locked Loop

PWM	Pulse Width Modulation
EQEI	Enhanced Quadrature Encoder Interface
SD	Secure Digital
SPI	Serial Peripheral Interface
SPS	Samples per Second
TDES	Triple Data Encryption Standard
TK	Touch Key
TMR	Timer Controller
UART	Universal Asynchronous Receiver/Transmitter
UCID	Unique Customer ID
USB	Universal Serial Bus
WDT	Watchdog Timer
WWDT	Window Watchdog Timer

Table 11.1-1 List of Abbreviations

12 REVISION HISTORY

Date	Revision	Description
2022.12.26	1.00	• Initial version.

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.