Battery Monitoring IC
For Industry

KA49503A
Product Brief

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■ IMPORTANT NOTICE

Regarding the specifications of this product, it is considered that you have agreed to the quality level and disclaimer described below.

Support for industry standards and quality standards

Functional safety standards for automobiles ISO26262	**No**
AECQ-100	**No**
Market failure rate	**50Fit**

Disclaimer

1. When the application system is designed using this IC, please design the system at your own risk. Please read, consider, and apply appropriate usage notes and description in this standard.

2. When designing your application system, please take into the consideration of break down and failure mode occurrence and possibility in semiconductor products. Measures on the systems such as, but not limited to, redundant design, mitigating the spread of fire, or preventing glitch, are recommended in order to prevent physical injury, fire, social damages, etc. in using the Nuvoton Technology Japan Corporation (hereinafter referred to as NTCJ) products.

3. When using this IC, for each actual application systems, verify the systems and the all functionality of this IC as intended in application systems and the safety including the long-term reliability at your own risk

4. Please use this IC in compliance with all applicable laws, regulations and safety-related requirements that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. NTCJ shall not be held responsible for any damage incurred as a result of this IC being used not in compliance with the applicable laws, regulations and safety-related requirements.

5. This IC does not have any security functions using cryptographic algorithms, such as authentication, encryption, tampering detection.

6. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular industry standard (e.g., ISO 9001, IATF 16949, ISO 26262, etc.), this IC is neither designed nor intended for use in such environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular industry standard.

7. Using IC that have been indicated as compliant with industry functional safety standards does not warrant that the application meets the requirements of industry functional safety standards. NTCJ shall not be held responsible for the application compliance with requirements of the particular industry functional safety standard.

8. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular quality standard (e.g., AECQ-100, etc.), this IC is neither designed nor intended for use in such the environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular quality standard.

9. In case of damages, costs, losses, and/or liabilities incurred by NTCJ arising from customer's non-compliance with above from 1 to 8, customer will indemnify NTCJ against every damages, costs, losses and responsibility.

Battery Monitoring IC for Industry

Features

KA49503A is a battery monitoring IC with protection function. With high resolution ADC built-in, KA49503A is capable to measure battery cell voltage and current level accurately.

Through SPI serial interface, microcontroller unit (MCU) is able to read the status and measured result by KA49503A. The ALARM pins alert the MCU with the abnormal condition such as over voltage (OV), under voltage (UV), over current (OC) and short circuit (SC).

KA49503A can support an application with up to 16 batteries cells in series or a maximum voltage of 85V, it is suitable for application with high input voltage such as E-bike, UPS etc.

- Maximum support 16 battery cells in series
- 10mV measurement accuracy with 14 bits voltage ADC for cell voltage, and 5 channels analog input measurement
- Built-in 16 bits low speed current measurement ADC (Coulomb Counter) and high speed current measurement ADC
- Low–side shunt sense resistor for current measurement and monitoring
- 2 interrupt pins ADIRQ1, ADIRQ2 for voltage measurement and current measurement
- Operation mode - Active, Standby and Shutdown Mode
- SPI serial communication interface up to 1MHz clock with CRC code correction and watchdog timer
- Built-in ALARM pins for overvoltage, undervoltage, overcurrent and short circuit detection and protection feature
- Built-in cell balancing MOSFET, with support of external cell balance MOSFET operation
- 6 channels General GPIO and 2 channels high voltage output
- High-side Charge (CHG) & Discharge (DIS) N-ch FET driver with built-in charge pump and FETOFF control pin
- 50mA 5V LDO
- Package : LQFP 80L (14x14x1.4mm^3, Lead Pitch 0.65mm)

Application

Pedelec, e-Bike, UPS, Server Backup System, Power Tool, Energy Storage Systems etc

Note: This IC may not be able to fulfill the functional safety requirements when Automotive grade Laws or Regulations are applied to Electric Bicycles. In this case, please consider using our Automotive Grade ICs.

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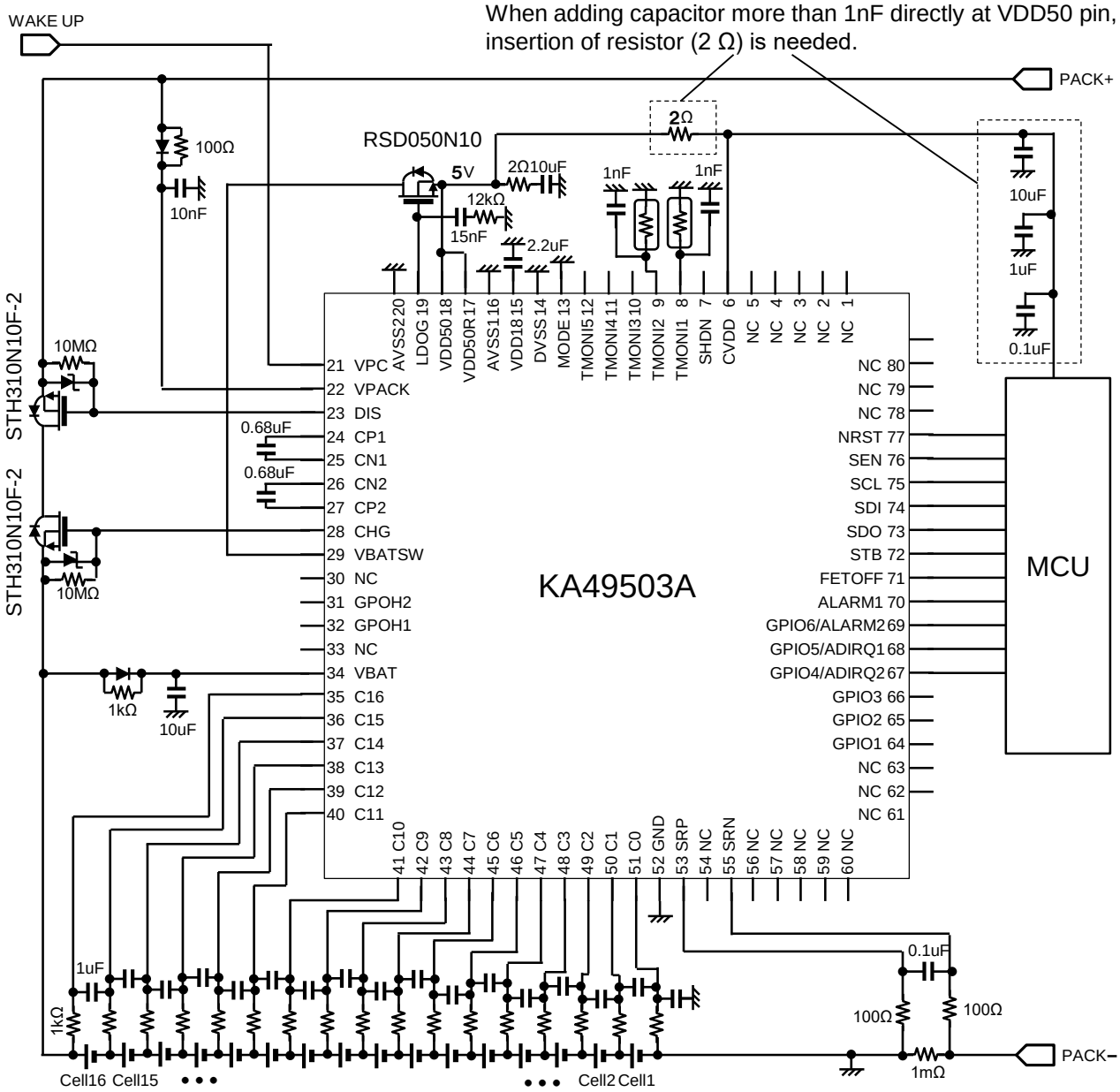
Chapter 1 Overview

1.1 Recommended Circuit

When connecting a circuit to VDD50, please be careful about below.

- Adding capacitor more than 1nF to VDD50 pin directly is prohibited.
- When needing capacitor more than 1nF, please use through 2Ω resistor.
  Please design as the total capacitor is from 6uF to 16uF.



Note: The recommended circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. Customer is fully responsible for the incorporation of the above illustrated application circuit in the production.

1.2 Electrical Characteristics

1.2.1 ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Notes
Supply voltage	V_{VBAT}	-0.3 ~ 99	V	*1
	V_{CVDD}	-0.3 ~ 6.5	V	*1
Operating junction temperature	T_j	-40 ~ 125	°C	*2
Storage temperature	T_{stg}	-55 ~ 125	°C	*2
Input Voltage Range	C16	-0.3 ~ VBAT+1.2	V	*3
	Cn (n=1~15)	-0.3 ~ VBAT+0.3	V	*3
	C0	-0.3 ~ 6.5	V	
	SEN, SCL, SDI, FETOFF STB, GPIOn (n=1~6)	-0.3 ~ V_{CVDD}+0.3	V	*4
	TMONIn (n=1~5),	-0.3 ~ V_{VDD50}+0.3	V	*4
	SRP.SRN	-0.5 ~ 2.0	V	
	VPC	-0.3 ~ 99	V	
	SHDN	-0.3 ~ 6.5	V	
Output Voltage Range	ALARM1,SDO,NRST	-0.3 ~ V_{CVDD}+0.3	V	
	VDD50	-0.3 ~ 6.5	V	
	GPOHn (n=1~2)	-0.3 ~ 99	V	
Output Current Range	ALARM1,SDO,NRST	-6.0 ~ +6.0	mA	*5
	GPIOn (n=1~6)	(-12.0 ~ +12.0)		*6
Allowable Voltage Between Pins	C_n - C_{n-1} (n=1~16)	-0.3 ~ 11	V	

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
Do not apply external currents and voltages to any pin not specifically mentioned.

*1 : The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2 : Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25 °C

*3 : (VBAT+0.3) & (VBAT+1.2) shall not over 99V.

*4 : (VCVDD + 0.3), (VVDD50 + 0.3) must not exceed 6.5V.

*5: + Polarity is the direction that flows from the pin to the outside, - polarity is the direction that flows from the outside to the pin.

*6: This is the rated current at the I / O output drivability setting 2mA. The value of () is the rated current when increasing the I / O output drivability by register settings.

1.2.2 POWER DISSIPATION RATING

Package	θj-a	θj-c	P_D（Ta=25℃）	P_D（Ta=105℃）
LQFP 80L (14x14x1.4mm^3, Lead Pitch 0.65mm)	55.5 °C/W	7.2 °C/W	1.80 W	0.36 W

Note) For the actual usage, please refer to the P_D-T_a characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

1.2.3 RECOMMENDED OPERATING CONDITIONS

Parameter	Pin Name	Min.	Typ.	Max.	Unit	Notes
Supply voltage range	V_{VBAT}	12.5	59.2	85	V	
	V_{CVDD}	3.0	5.0	5.5	V	
Input Voltage Range	C_n - C_{n-1} (n=1～16)	0	—	5.0	V	
	SEN, SCL, SDI	0	—	V_{CVDD}	V	
	TMONIn (n=1～5)	0	—	5.0	V	
	GPIOn (n=1～6)	0	—	V_{CVDD}	V	
	SRP,SRN	-0.18	—	0.18	V	
	VPC	0	—	85	V	
	SHDN	0	—	V_{VDD50}	V	
Operating Ambient Temperature	Ta_{opr}	–40	25	105	℃	

1.2.4 ELECTRICAL CHARACTERISTICS

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SUPPLY CURRENT							
VBAT Active Mode	I_{BAT1}		—	3.1	3.9	mA	
VBAT Standby Mode	I_{BAT2}	5VLDO:Low Power, Coulomb Counter:off FDRV:Intermittent Communication:off	—	0.15	0.30	mA	
VBAT Shutdown Mode	I_{BAT3}		0	—	1	μA	
5VLDO							
VDD50 Output Voltage	V_{VDD}		4.75	5.0	5.25	V	
VDD50 Drive Current	I_{VDD1}	Normal mode	0	—	50	mA	
VDD50 Drive Current	I_{VDD2}	Low Power mode	0	—	5	mA	
CELL BALANCING CONTROL OUTPUT (CBn)							
Output Impedance	Z_{CB}	⊿Cn = 3.0V ~ 5.0V	—	12.5	20	Ω	

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CELL VOLTAGE MONITOR							
Input Voltage Range	ΔCn	C_n - C_{n-1} (n=1～16)	0	—	5	V	
Voltage Resolution	V_{RES}	14bits	-—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_VC1}	ΔCn = 2.0V ～ 4.3 V	–10	—	10	mV	
Voltage Accuracy2	V_{ACC_VC2}	ΔCn = 2.0V ～ 4.3 V Ta = –30℃ ～ 65℃	–10	—	10	mV	*2
Conversion Time	t_{conv}	time/cell	—	50	—	μs	*1
Cell Measurement Input Current	I_{IN}	Active mode	–5	—	5	μA	
Input Leakage Current	I_{LK}	Shutdown mode	–1	—	1	μA	
OVER / UNDER VOLTAGE DETECTOR (OV / UV)							
OV detection threshold step	V_{ACC_OV}	2.0～4.5V@6bit	—	50	—	mV	*1
UV detection threshold step	V_{ACC_UV}	0.5～3.0V@6bit	—	50	—	mV	*1
VPACK CELL VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0	—	85	V	
Voltage Resolution	V_{RES}	14bits	—	6.1	—	mV	*1
Voltage Accuracy1	V_{ACC_VPACK1}	V_{VPACK} = 12.5V ～ 72V	–1	—	1	V	
Voltage Accuracy2	V_{ACC_VPACK2}	V_{VPACK} = 12.5V ～ 72V T_a = –30℃ ～ 65℃	–1	—	1	V	*2

*1 : It is a design center value.
*2 It is design value. The inspection is not done.

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TMONI1-5 VOLTAGE MONITOR							
Input Voltage Range	V_{IN}		0	—	5	V	
Voltage Resolution	V_{RES}	14bits	—	0.3	—	mV	*1
Voltage Accuracy1	V_{ACC_TMONI1}	VIN = 0.4V～4.7V Not use Pull-up Resistance	–10	—	10	mV	
Voltage Accuracy2	V_{ACC_TMONI2}	VIN = 0.4V～4.7V Not use Pull-up Resistance T_a = –30℃ ～ 65℃	–10	—	10	mV	*3
Input Pull-up Resistance	R_{PU}		7	10	13	kΩ	
Input Pull-up Resistance Temperature coefficient	RT_{PU}	T_a = –30℃ ～ 65℃	–1.0	—	1.0	%	*3
THERMAL SHUTDOWN							
Shutdown Threshold	T_{SD2}	Tj	150	175	200	°C	*2 *3

*1 : It is a design center value.
*2 : When thermal shutdown occurs, all circuitry is shutdown.
Following wake up (to active mode) sequence in order to restart.
*3 : It is design value. The inspection is not done.

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LOW SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN}		-180	—	180	mV	
Voltage Resolution	V_{RES}	16bits	—	5.493	—	μV	*1
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*2
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-25	—	25	μV	*2
HIGH SPEED CURRENT MONITOR (SRP,SRN)							
Input Voltage Range	V_{IN}		-180	—	180	mV	
Voltage Resolution	V_{RES}	15bits	—	10.99	—	μV	*1
Voltage Accuracy1	V_{ACC_IMONI}	VIN = 100mV	-1000	—	1000	μV	
Voltage Accuracy2	V_{ACC_IMONI}	VIN = 10mV	-150	—	150	μV	*2
Voltage Accuracy3	V_{ACC_IMONI}	VIN = 1mV	-50	—	50	μV	*2
CURRENT PROTECTION (SRP,SRN)							
Over Current in Charge Detection Accuracy1	V_{CP_OCC}	Detection Threshold 10mV	-5	—	5	mV	*2
Over Current in Charge Detection Accuracy2	V_{CP_OCC}	Detection Threshold from 20mV to 100mV	–10	—	10	mV	*2
Over Current in Charge Detection Accuracy3	V_{CP_OCC}	Detection Threshold from 100mV to 200mV	–10	—	10	%	*2
Over Current in Discharge Detection Accuracy1	V_{CP_OCD}	Detection Threshold from 25mV to 100mV	–10	—	10	mV	*2
Over Current in Discharge Detection Accuracy2	V_{CP_OCD}	Detection Threshold from 100mV to 800mV	–10	—	10	%	*2
Short Circuit in Discharge Detection Accuracy1	V_{CP_SCD}	Detection Threshold from 50mV to 100mV	–10	—	10	mV	*2
Short Circuit in Discharge Detection Accuracy2	V_{CP_SCD}	Detection Threshold from 100mV to 800mV	–10	—	10	%	*2

*1 : It is a design center value.
*2 : It is a design verification value. The inspection is not done.

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
GENERAL PURPOSE INPUT/OUTPUT (GPIO)							
Input Voltage “H”	V_{IH}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL}		0	—	V_{CVDD} ×0.2	V	
Output Voltage “H”	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	0.4	V	
GENERAL PURPOSE HV OUTPUT (GPO)							
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	7.0	V	
DIGITAL INPUT(1) VPC							
Input Voltage “H”	V_{IH}		4.0	—	—	V	
Input Voltage “L”	V_{IL}		—	—	0.3	V	
Pull-down resistance	R_{IL}		6	28	55	MΩ	
DIGITAL INPUT(2) SHDN							
Input Voltage “H”	V_{IH}		3.0	—	—	V	
Input Voltage “L”	V_{IL}		—	—	0.1	V	
Pull-down resistance	R_{IL}		200	820	1500	kΩ	
DIGITAL INPUT(3) SDI,SCL,SEN,FETOFF,STB							
Input Voltage “H”	V_{IH}		V_{CVDD} ×0.8	—	V_{CVDD}	V	
Input Voltage “L”	V_{IL}		0	—	V_{CVDD} ×0.2	V	
Input Leakage Current	I_{LK}		-1	0	1	μA	
DIGITAL OUTPUT(1) ALARM1,SDO							
Output Voltage “H”	V_{OH}	I_{OH} = –1mA	V_{CVDD} –0.6	—	V_{CVDD} +0.3	V	
Output Voltage “L”	V_{OL}	I_{OL} = +1mA	–0.3	—	0.4	V	
DIGITAL OUTPUT(2) NRST							
Output voltage “L”	V_{OL}	I_{OL} = 0 mA	–0.3	—	0.5	V	
Pull-up resistance	R_{IL}	—	50	100	200	kΩ	

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
CVDD UV							
UV detection voltage	V_{IL_UV}	—	—	2.45	—	V	*1 *2
UV release voltage	V_{IH_UV}	—	—	2.80	—	V	*1
Hysteresis voltage	V_{HYS_UV}		—	0.35	—	V	*1
VDD50 UVLO							
UVLO detection voltage	V_{IL_UVLO}		—	4.00	—	V	*1 *3
Nch. FET DRIVER							
Drive voltage (DIS=“H”)	V_{ON_DIS}	$V_{ON\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (CHG="H”)	V_{ON_CHG}	$V_{ON\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	9	11	13	V	
Drive voltage (DIS=“L”)	V_{OFF_DIS}	$V_{OFF\_DIS} = V_{DIS} – V_{VPACK}$ VGS connect 10MΩ	—	—	0.2	V	
Drive voltage (CHG=“L”)	V_{OFF_CHG}	$V_{OFF\_CHG} = V_{CHG} – V_{VBAT}$ VGS connect 10MΩ	—	—	0.2	V	
Rise time (DIS=“L” to ”H”)	tr	V_{DIS} = 10% to 90% C_L = 47nF	—	0.8	1.6	ms	
Rise time (CHG=“L” to ”H”)	tr	V_{CHG} = 10% to 90% C_L = 47nF	—	0.8	1.6	ms	
Fall time (DIS =“H” to ”L”)	tf	V_{DIS} = 90% to 10% C_L = 47nF	—	0.5	1.0	ms	
Fall time (CHG=“H” to ”L”)	tf	V_{CHG} = 90% to 10% C_L = 47nF	—	0.5	1.0	ms	

*1 : It is a design center value.
*2 : When detecting the CVDD UV,*CVDD_UV* flag (CVDD_STAT: bp2) is set to "0".
*3 : When detecting the VDD50 UVLO, it will be switched to the Shutdown mode. (if VPC pin is "L“)

at V_{VBAT} = V_{VPACK} = 59.2 V , V_{CVDD} = 5.0V
Note: unless otherwise noted, Operating Ambient Temperature is T_a = 25℃±2℃

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI Interface Timing (SEN, SDI, SCL, SDO)							
SCL Frequency	f_{SCL}	—	—	—	1	MHz	
SCL Duty Cycle	t_{DUTY}	—	45	50	55	%	
SEN Rising to SCL Rising	t_{SEN_LD}	—	100	—	—	ns	
SCL Falling to SEN Falling	t_{SEN_LG}	—	100	—	—	ns	
SEN "L" Width	t_{SEN_LO}	—	500	—	—	ns	
SDI Setup Time	t_{SDI_SU}	SDI valid to SCL falling	100	—	—	ns	
SDI Hold Time	t_{SDI_HD}	SCL falling to SDI valid	100	—	—	ns	
SDO Valid Time	t_{SDO_VD}	SCL rising to SDO valid C_L ≦ 50 pF	—	—	400	ns	
SDO Disable Time	t_{SDO_DIS}	SEN falling to SDO disable	—	—	400	ns	

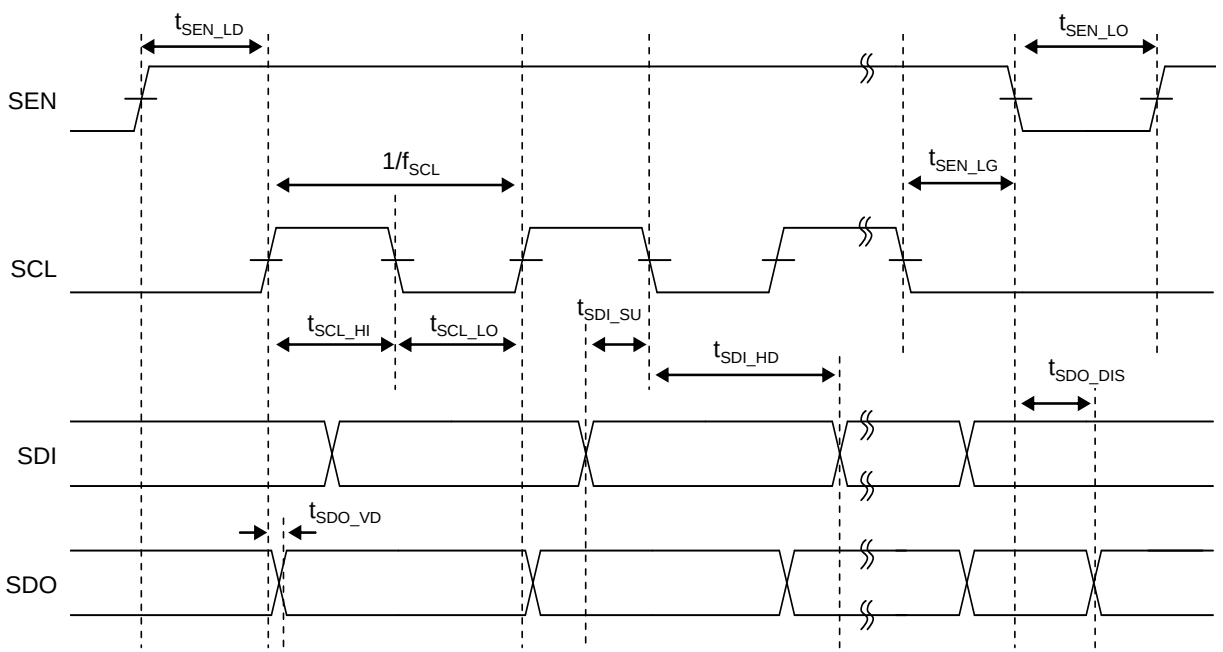
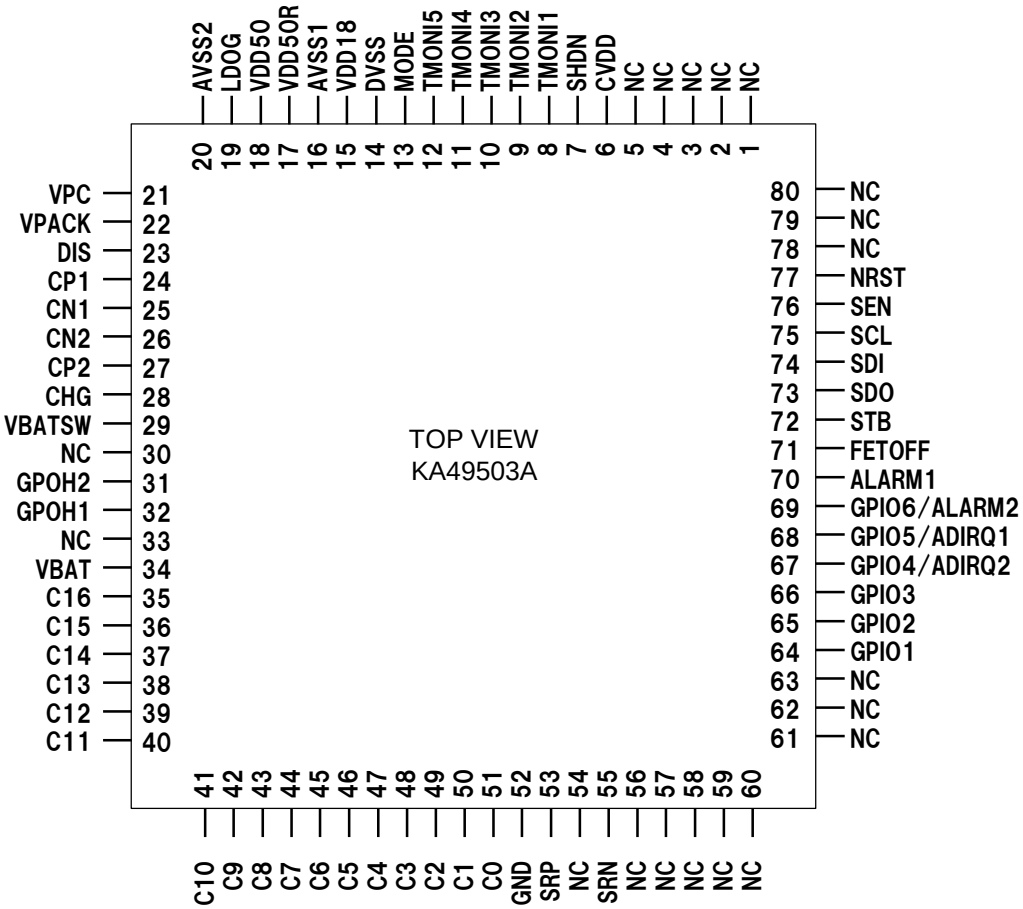


Fig.2.4.1 SPI Timing

1.3 PIN CONFIGURATION



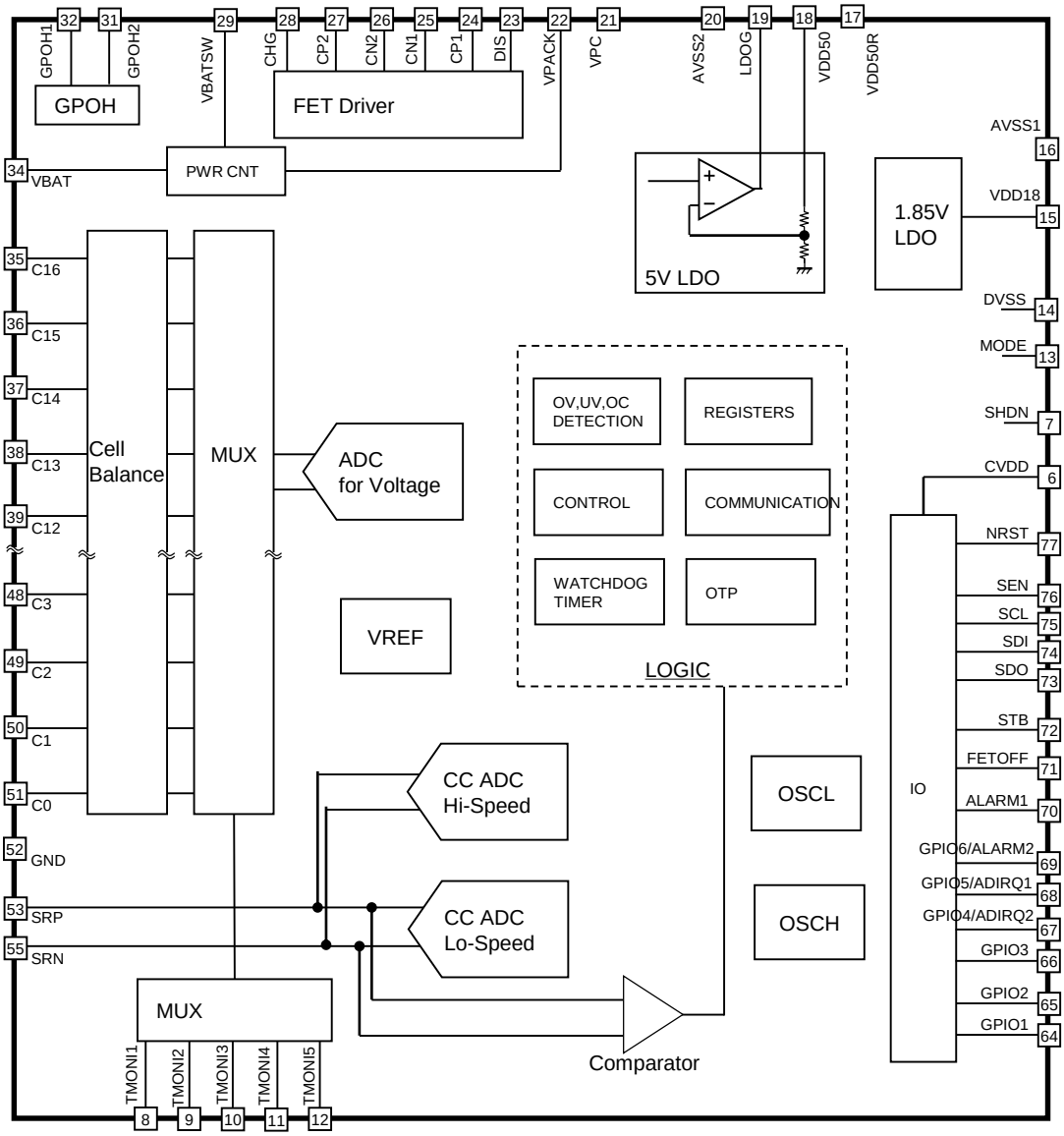
1.4 PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1	NC	-	N.C. Pin
2	NC	-	N.C. Pin
3	NC	-	N.C. Pin
4	NC	-	N.C. Pin
5	NC	-	N.C. Pin
6	CVDD	I(Supply)	Digital Voltage Supply
7	SHDN	I	Shutdown Control “L”: Active mode / “H”: Shutdown mode
8	TMONI1	I	Analog Input Pin 1
9	TMONI2	I	Analog Input Pin 2
10	TMONI3	I	Analog Input Pin 3
11	TMONI4	I	Analog Input Pin 4
12	TMONI5	I	Analog Input Pin 5
13	MODE	I	Test Mode Pin for Manufacturer Use Only (Connect to DVSS always)
14	DVSS	GND	Digital Ground
15	VDD18	O	1.85V LDO Output Pin for Internal Use
16	AVSS1	GND	Analog Ground
17	VDD50R	I	(To be connected to VDD50 pin)
18	VDD50	O	5V Output Pin
19	LDOG	O	Gate Control Pin for 5V LDO NMOS Gate Pin
20	AVSS2	GND	Analog Ground
21	VPC	I	Wake Up Signal Pin “H” Wake Up, Please be always fixed to "L" after Wake Up.
22	VPACK	I(Power Supply)	Positive Pin for Battery Pack
23	DIS	O	Discharge NMOSFET Gate Drive Pin
24	CP1	O	Charge Pump Capacitor Pin (Positive Pin for VPACK)
25	CN1	O	Charge Pump Capacitor Pin (Negative Pin for VPACK)
26	CN2	O	Charge Pump Capacitor Pin (Negative Pin for VBAT)
27	CP2	O	Charge Pump Capacitor Pin (Positive Pin for VBAT)
28	CHG	O	Charge NMOSFET Gate Drive Pin
29	VBATSW	O	Power Pin for 5V LDO NMOS Drain Pin
30	NC	-	N.C. Pin

Pin No.	Pin name	Type	Description
31	GPOH2	O	High Voltage General Purpose Output Pin 2 (Open Drain)
32	GPOH1	O	High Voltage General Purpose Output Pin 1 (Open Drain)
33	NC	-	N.C. Pin
34	VBAT	I(Power Supply)	Battery Top Most Pin
35	C16	I	Cell 16 Input Pin (+ve)
36	C15	I	Cell 15 Input Pin (+ve) / Cell 16 Input Pin (-ve)
37	C14	I	Cell 14 Input Pin (+ve) / Cell 15 Input Pin (-ve)
38	C13	I	Cell 13 Input Pin (+ve) / Cell 14 Input Pin (-ve)
39	C12	I	Cell 12 Input Pin (+ve) / Cell 13 Input Pin (-ve)
40	C11	I	Cell 11 Input Pin (+ve) / Cell 12 Input Pin (-ve)
41	C10	I	Cell 10 Input Pin (+ve) / Cell 11 Input Pin (-ve)
42	C9	I	Cell 9 Input Pin (+ve) / Cell 10 Input Pin (-ve)
43	C8	I	Cell 8 Input Pin (+ve) / Cell 9 Input Pin (-ve)
44	C7	I	Cell 7 Input Pin (+ve) / Cell 8 Input Pin (-ve)
45	C6	I	Cell 6 Input Pin (+ve) / Cell 7 Input Pin (-ve)
46	C5	I	Cell 5 Input Pin (+ve) / Cell 6 Input Pin (-ve)
47	C4	I	Cell 4 Input Pin (+ve) / Cell 5 Input Pin (-ve)
48	C3	I	Cell 3 Input Pin (+ve) / Cell 4 Input Pin (-ve)
49	C2	I	Cell 2 Input Pin (+ve) / Cell 3 Input Pin (-ve)
50	C1	I	Cell 1 Input Pin (+ve) / Cell 2 Input Pin (-ve)
51	C0	I	Cell 1 Input Pin (-ve)
52	GND	GND	Analog Ground
53	SRP	I	Shunt Resistor Positive Pin
54	NC	-	N.C. Pin
55	SRN	I	Shunt Resistor Negative Pin
56	NC	-	N.C. Pin
57	NC	-	N.C. Pin
58	NC	-	N.C. Pin
59	NC	-	N.C. Pin
60	NC	-	N.C. Pin

Pin No.	Pin name	Type	Description
61	NC	-	N.C. Pin
62	NC	-	N.C. Pin
63	NC	-	N.C. Pin
64	GPIO1	I/O	General Purpose I/O Pin 1
65	GPIO2	I/O	General Purpose I/O Pin 2
66	GPIO3	I/O	General Purpose I/O Pin 3
67	GPIO4/ADIRQ2	I/O	General Purpose I/O Pin 4 / ADIRQ2 Pin
68	GPIO5/ADIRQ1	I/O	General Purpose I/O Pin 5 / ADIRQ1 Pin
69	GPIO6/ALARM2	I/O	General Purpose I/O Pin 6 / ALARM2 Pin
70	ALARM1	O	ALARM1 Pin
71	FETOFF	I	CHG/DIS FET Control Pin - “L” Normal / “H” FET Forced OFF
72	STB	I	Standby Mode Control Pin - “L” Active mode / “H” Standby mode
73	SDO	O	SPI Interface Pin – Data Out
74	SDI	I	SPI Interface Pin – Data In
75	SCL	I	SPI Interface Pin – Clock
76	SEN	I	SPI Interface Pin – Enable
77	NRST	O	Power Reset Output Pin（Open Drain）
78	NC	-	N.C. Pin
79	NC	-	N.C. Pin
80	NC	-	N.C. Pin

1.5 FUNCTIONAL BLOCK DIAGRAM



Chapter 2 Battery Connection

The minimum required VBAT pin voltage is 12.5V to guarantee normal operation.

For application using less than 16 cells, all unused cells Cn pins should be connected as shown in figure below, user shall use cells connect to C16, C15, C1 and C2 pins first and follow by battery from lower cell.

Battery cells connection sequence:
Connect the GND pin followed by VBAT pin. After that, it should be connected from the lower cell in turn.
GND -> VBAT -> Cell between C0-C1 -> Cell between C1-C2 -> ▪▪▪

Figures below show example connection for 15 battery cells and 4 battery cells, please note, it is possible to be connected for 4 battery cells only when the minimum VBAT is higher then 12.5V.

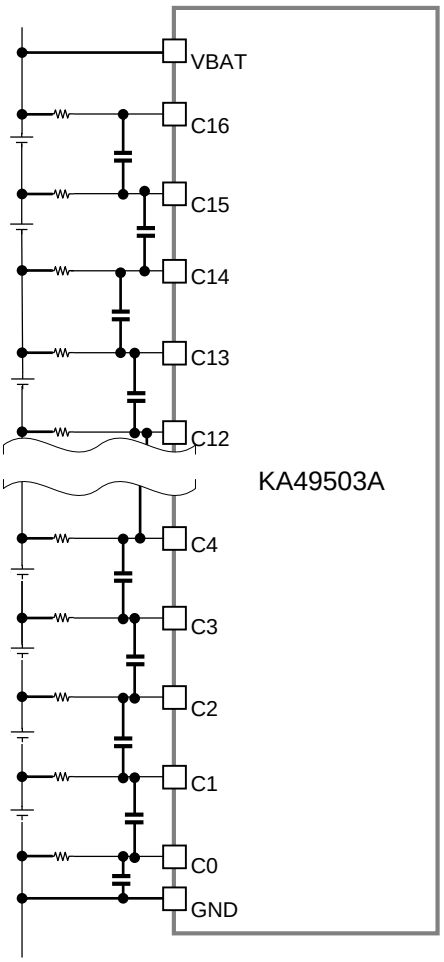


Fig.2.1.1 KA49503A Cell Connection example with 15 cell connected

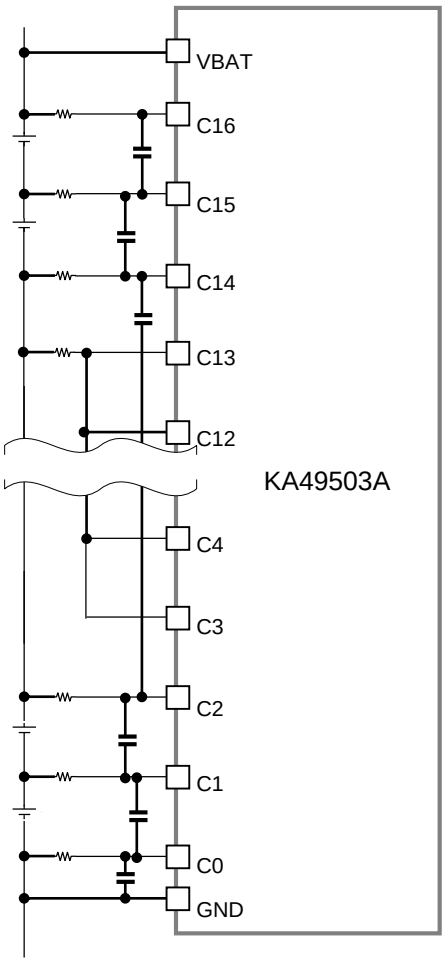
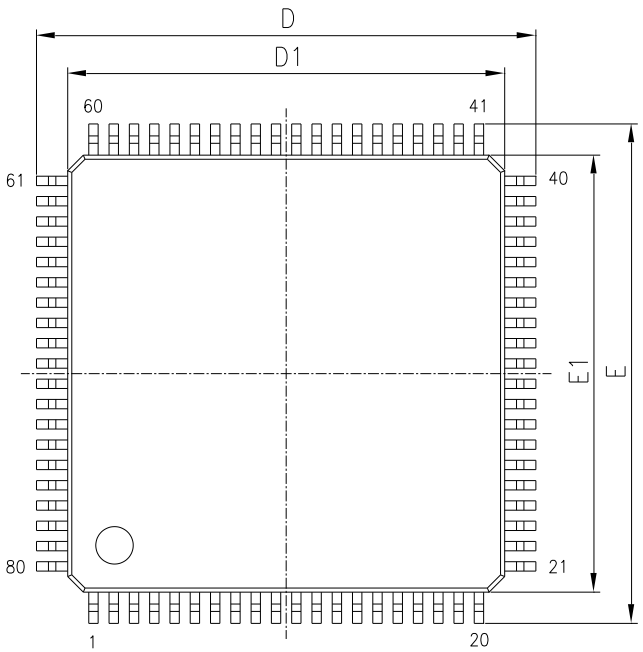
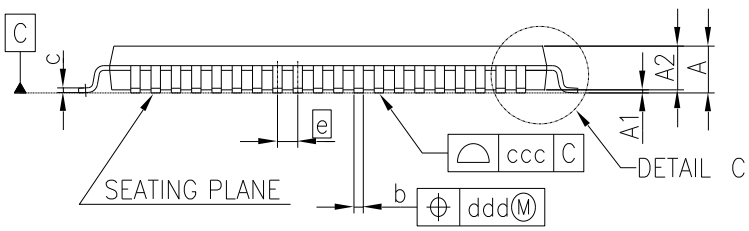


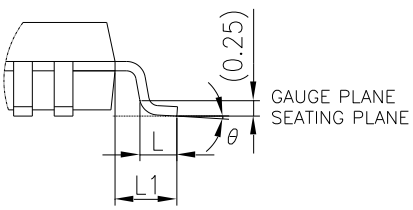
Fig.2.1.2 KA49503A Cell Connection Example with only 4 cell connected

Package Information

LQFP080 14x14mm^2, Thickness 1.4mm, Lead_Pitch 0.65mm, Lead_Length 1.00mm







DETAIL C

VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.70
A1	0.00	0.10	0.20
A2		1.40REF	
D	15.80	16.00	16.20
D1	13.90	14.00	14.10
E	15.80	16.00	16.20
E1	13.90	14.00	14.10
L	0.45	0.60	0.75
L1		1.00REF	
b	0.25	0.30	0.35
c	0.10	0.15	0.20
e		0.65BSC	
ccc		0.10	
ddd		0.13	
θ	0.0°	–	8.0°

Usage notes

1. Pay attention to the direction of the IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board),
   it might be damaged.
2. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins.
   In addition, refer to the Pin Description for the pin configuration.
3. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the IC. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.
4. Take notice in the use of this IC that it might be damaged when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage will depend on the current capability of the power supply.
5. This IC may be changed in order to improve the performance without notice, please make sure the latest specification is used before your final design.

Revision History

Date	Revision	Description
2021.1.28	1.00	1. initially issued.
2022.1.21	1.02	1. Added important notice on page2 2. Remove important notice page from previous version page 21 3. Added usage notes on page22

Important Notice

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