6 x 6 Dots Matrix
LED Driver IC

KA32182A
Product Brief

For additional information or question, please contact Nuvoton Technology Corporation Japan
WWW.nuvoton.co.jp

■ IMPORTANT NOTICE

Regarding the specifications of this product, it is considered that you have agreed to the quality level and disclaimer described below.

Support for industry standards and quality standards

Functional safety standards for automobiles ISO26262	**No**
AECQ-100	**No**
Market failure rate	**50 Fit**

Disclaimer

1. When the application system is designed using this IC, please design the system at your own risk. Please read, consider, and apply appropriate usage notes and description in this standard.

2. When designing your application system, please take into the consideration of break down and failure mode occurrence and possibility in semiconductor products. Measures on the systems such as, but not limited to, redundant design, mitigating the spread of fire, or preventing glitch, are recommended in order to prevent physical injury, fire, social damages, etc. in using the Nuvoton Technology Japan Corporation (hereinafter referred to as NTCJ) products.

3. When using this IC, for each actual application systems, verify the systems and the all functionality of this IC as intended in application systems and the safety including the long-term reliability at your own risk

4. Please use this IC in compliance with all applicable laws, regulations and safety-related requirements that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. NTCJ shall not be held responsible for any damage incurred as a result of this IC being used not in compliance with the applicable laws, regulations and safety-related requirements.

5. This IC does not have any security functions using cryptographic algorithms, such as authentication, encryption, tampering detection.

6. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular industry standard (e.g., ISO 9001, IATF 16949, ISO 26262, etc.), this IC is neither designed nor intended for use in such environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular industry standard.

7. Using IC that have been indicated as compliant with industry functional safety standards does not warrant that the application meets the requirements of industry functional safety standards. NTCJ shall not be held responsible for the application compliance with requirements of the particular industry functional safety standard.

8. Unless this IC is indicated by NTCJ to be used in applications as meeting the requirements of a particular quality standard (e.g., AECQ-100, etc.), this IC is neither designed nor intended for use in such the environments for that applications. NTCJ shall not be held responsible for not meeting the requirements of a particular quality standard.

9. In case of damages, costs, losses, and/or liabilities incurred by NTCJ arising from customer's non-compliance with above from 1 to 8, customer will indemnify NTCJ against every damages, costs, losses and responsibility.

6 x 6 Dots Matrix LED Driver IC

FEATURES

- 6 × 6 LED Matrix Driver
  (Total LED that can be driven = 36)
- LED Selectable Maximum Current
- LED Music Synchronizing function
- I²C interface (Standard Mode, Fast Mode and Fast Mode Plus)
  (4 Slave address selectable)
- 20 pin Plastic Quad Flat Non-leaded Package (QFN Type)

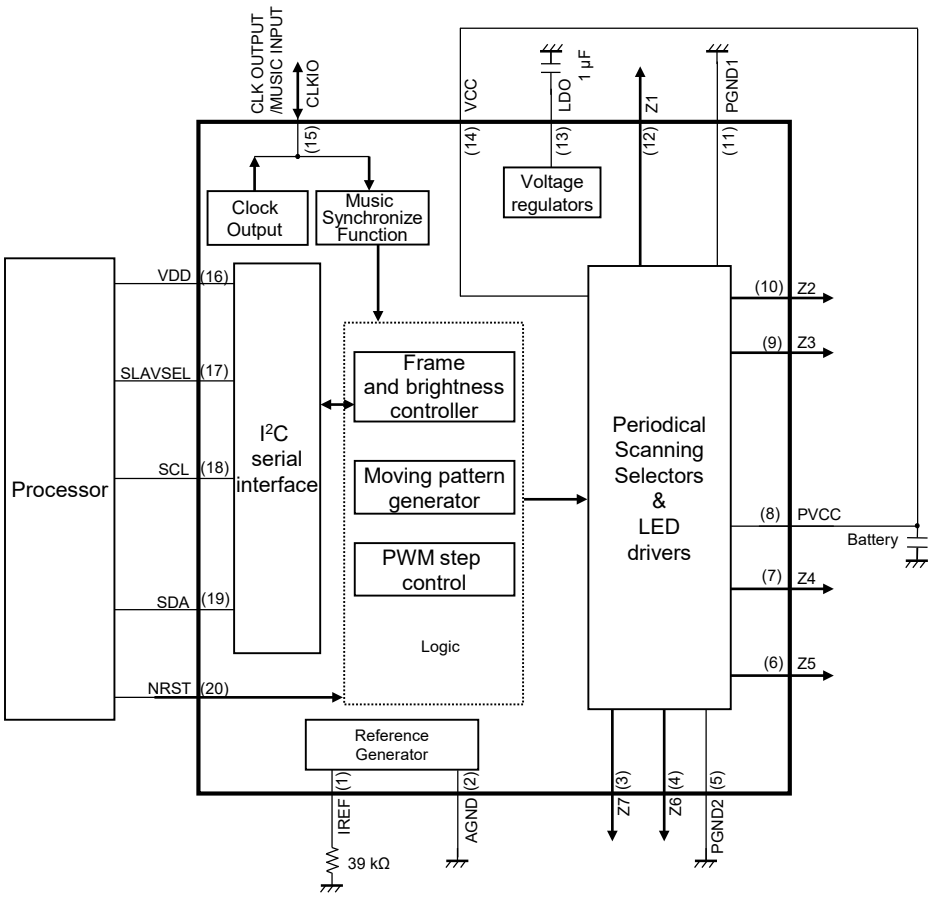
DESCRIPTION

KA32182A is a 36 dots Matrix LED driver.
It can drive up to 12 RGB LEDs.

APPLICATIONS

- Mobile, Wearable
- Smart Speaker
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note:
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

CONTENTS

ORDERING INFORMATION

Order Number	Feature	Package	Output Supply
KA32182A-VB	LED Driver for Illumination	20 pin QFN	Emboss Taping

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VCC_{MAX}	6.0	V	*1
	VDD_{MAX}	6.0	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	$V_{SLAVSEL}$, V_{SCL}, V_{SDA}, V_{CLKIO}, V_{NRST}	– 0.3 to 6.0	V	—
Output Voltage Range	V_{IREF}, V_{LDO}, V_{CLKIO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}	– 0.3 to 6.0	V	—
ESD	HBM	2.0	kV	—

Note: This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteed as it is higher than our stated recommended operating range. When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.

*1: VCC_{MAX} = VCC= PVCC, VDD_{MAX} = VDD.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: Except for operating ambient temperature, operating junction temperature and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

Package	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
QFN 20L (3x4x0.8mm3, Lead Pitch 0.4mm)	194.0 °C /W	0.515 W	0.206 W

Note: For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	V_{CC}	3.1	3.6	5.5	V	—
	V_{DD}	1.7	1.85	5.5	V	—
Input Voltage Range	$V_{SLAVSEL}$, V_{SCL}, V_{SDA}, V_{CLKIO}	– 0.3	—	V_{DD} + 0.3	V	*1
	V_{NRST}	– 0.3	—	V_{CC} + 0.3	V	*1
Output Voltage Range	V_{IREF}, V_{LDO}, V_{CLKIO}, V_{Z1}, V_{Z2}, V_{Z3}, V_{Z4}, V_{Z5}, V_{Z6}, V_{Z7}	– 0.3	—	V_{CC} + 0.3	V	*1

Note: Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for GND.
V_{CC} is voltage for VCC. V_{DD} is voltage for VDD.
Do not apply external currents or voltages to any pin not specifically mentioned.
*1 : (V_{CC} + 0.3) V must not exceed 6 V. (V_{DD} + 0.3) V must not exceed 6 V.

ELECTRICAL CHARACTERISTICS

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Circuit Current							
Circuit Current (1) OFF Mode	I_{CC1}	NRST = 0 V	—	0	1	μA	—
Circuit Current (2) OFF Mode	I_{CC2}	NRST = 3.6V	—	250	500	μA	—
Internal Oscillator							
Oscillation Frequency	FDC1	V_{CC} = 3.6 V	1.92	2.40	2.88	MHz	—
SCAN Switch							
Switch On Resistance	RSCAN	V_{CC} = 3.6 V $I_{Z1\sim Z7}$ = – 20 mA	—	1.5	3	Ω	—
Constant Voltage Source (LDO)							
Output voltage (1)	V_{L1}	I_{LDO} = – 10 μA	2.75	2.85	2.95	V	—
Output voltage (2)	V_{L2}	I_{LDO} = – 15 mA	2.75	2.85	2.95	V	—
CLKIO							
High Level Input Voltage Range	V_{IH1}	High Level Acknowledged Voltage (At External CLK Input Mode)	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL1}	Low Level Acknowledged Voltage (At External CLK Input Mode)	– 0.3	—	0.3 × V_{DD}	V	—
High Level Output Voltage	V_{OH1}	I_{CLKIO} = – 1 mA (At Internal CLK Output Mode)	0.8 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Output Voltage	V_{OL1}	I_{CLKIO} = 1 mA (At Internal CLK Output Mode)	– 0.3	—	0.2 × V_{DD}	V	—
High Level input Current	I_{IH1}	V_{CC} = 5.5 V V_{CLKIO} = 5.5 V	– 1	0	1	μA	—
Low Level input Current	I_{IL1}	V_{CC} = 5.5 V V_{CLKIO} = 0 V	– 1	0	1	μA	—

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Constant Current Source (Matrix LED)							
Output Current (1)	I_{MX1}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] $V_{Z1\sim Z7}$ = 1 V	19	20	21	mA	*1
DAC Current Step	DACSTEP	DAC Constant Current Mode LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] $V_{Z1\sim Z7}$ = 1 V, IDAC1 = $I_{Z1\sim Z7}$ LED Current Setting = 22 mA I_{MAX} = [011], BRTXX = [1011] $V_{Z1\sim Z7}$ = 1 V, IDAC2 = $I_{Z1\sim Z7}$ DACSTEP = IDAC2 – IDAC1	0	2	4	mA	*2
OFF Mode Leak Current1	I_{MXOFF1}	V_{CC} = 5.5 V, V_{DD} = 5.5 V MTXON = 0 $V_{Z1\sim Z7}$ = 5.5 V	– 1	—	1	µA	*3
OFF Mode Leak Current2	I_{MXOFF2}	V_{CC} = 5.5 V, V_{DD} = 5.5 V MTXON = 0 $V_{Z1\sim Z7}$ = 0 V	– 1	—	1	µA	*3
Channel Difference	I_{MXCH}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] Difference of Z1 to 7 current from the average current value	– 5	—	5	%	—
Voltage at which LED driver can keep constant current value							
LED Driver Voltage	V_{LD2}	LED Current Setting = 20 mA I_{MAX} = [011], BRTXX = [1010] Voltage at which LED Current change within ±5% compared with LED Current of pin voltage = 0.5 V.	0.4	—	—	V	—

Note: * 1: This is allowable value when recommended parts (ERJ2RHD393X) are used for the terminal IREF.

* 2: Current step for individual channels (Z1~Z7).

* 3: Please refer to page 18 for more information on the setting.

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SLAVSEL							
High Level Input Voltage Range	V_{IH2}	High Level Acknowledged Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	—
Low Level Input Voltage Range	V_{IL2}	Low Level Acknowledged Voltage	– 0.3	—	0.3 × V_{DD}	V	—
High Level Input Current	I_{IH2}	V_{CC} = 5.5 V $V_{SLAVSEL}$ = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL2}	V_{CC} = 5.5 V $V_{SLAVSEL}$ = 0 V	– 1	0	1	µA	—
NRST							
High Level Input Voltage Range	V_{IH3}	High Level Acknowledged Voltage	1.5	—	V_{CC} + 0.3	V	—
Low Level Input Voltage Range	V_{IL3}	Low Level Acknowledged Voltage	– 0.3	—	0.6	V	—
High Level Input Current	I_{IH3}	V_{CC} = 5.5 V V_{NRST} = 5.5 V	– 1	0	1	µA	—
Low Level Input Current	I_{IL3}	V_{CC} = 5.5 V V_{NRST} = 0 V	– 1	0	1	µA	—
I²C bus (Internal I/O stage characteristics)							
Low-level input voltage	V_{IL}	Voltage which recognized that SDA and SCL are Low-level	–0.5	—	0.3 × V_{DD}	V	*4
High-level input voltage	V_{IH}	Voltage which recognized that SDA and SCL are High-level	0.7 × V_{DD}	—	VDD_{MAX} + 0.5	V	*4
Low-level output voltage 1	V_{OL1}	V_{DD} > 2 V I_{SDA} = 3 mA	0	—	0.4	V	—
Low-level output voltage 2	V_{OL2}	V_{DD} < 2 V I_{SDA} = 3 mA	0	—	0.2 × V_{DD}	V	—
Low-level output current	I_{OL}	V_{SDA} = 0.4 V	20	—	—	mA	—
Input current each I/O pin	I_i	V_{CC} = 5.5 V, V_{DD} = 5.5 V V_{SCL}, V_{SDA} = 0.1 VDD_{MAX} to 0.9 VDD_{MAX}	–10	0	10	µA	—
SCL clock frequency	f_{SCL}	—	0	—	1 000	kHz	—

Note: VDD_{Max} refers to the maximum operating supply voltage of V_{DD}.

*4 : The input threshold voltage of I²C bus (Vth) is linked to V_{DD} (I²C bus I/O stage supply voltage).
In case the pull-up voltage is not V_{DD}, the threshold voltage (Vth) is fixed to ((V_{DD} / 2) ± (Schmitt width) / 2) and High-level, Low-level of input voltage are not specified.
In this case, pay attention to Low-level (max.) value (V_{ILMAX}).
It is recommended that the pull-up voltage of I²C bus is set to the I²C bus I/O stage supply voltage (V_{DD}).

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
TSD (Thermal shutdown protection circuit)							
Detection temperature	Tdet	Temperature which Constant current circuit, and Matrix SW turn off.	—	150	—	°C	*5 *6
Constant Voltage Source (LDO)							
Ripple rejection ratio (1)	PSL11	V_{CC} = 3.6 V + 0.3 V [p-p] f = 1 kHz I_{LDO} = – 15 mA PSL11 = 20 log (acV_{LDO} / 0.3)	—	– 50	—	dB	*6
Ripple rejection ratio (2)	PSL12	V_{CC} = 3.6 V + 0.3 V[p-p] f = 10 kHz I_{LDO} = – 15 mA PSL12 = 20 log (acV_{LDO} / 0.3)	—	– 40	—	dB	*6
Short-circuit protection current	IPT1	V_{LDO} = 0 V	—	40	—	mA	*6
I²C bus (Internal I/O stage characteristics) (Continued)							
Hysteresis of Schmitt trigger input 1	V_{hys1}	V_{DD} > 2 V, Hysteresis of SDA, SCL	0.05 × V_{DD}	—	—	V	*7 *8
Hysteresis of Schmitt trigger input 2	V_{hys2}	V_{DD} < 2 V, Hysteresis of SDA, SCL	0.1 × V_{DD}	—	—	V	*7 *8
Output fall time from V_{IHmin} to V_{ILmax}	t_{of}	Bus capacitance :10pF to 550pF $I_P \leq$ 20 mA (V_{OLmax} = 0.4 V) I_P : Max. sink current	—	—	120	ns	*7 *8
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	—	0	—	50	ns	*7 *8
Capacitance for each I/O pin	C_i	—	—	—	10	pF	*7 *8

Note: *5 : Constant current circuit, and Matrix SW turn off and IC reset when TSD operates.

*6 : Typical Design Value

*7 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 10. All values referred to V_{IHMIN} and V_{ILMAX} level.

*8 : These are values checked by design but not production tested.

ELECTRICAL CHARACTERISTICS (Continued)

V_{CC} = 3.6 V, V_{DD} = 1.85 V

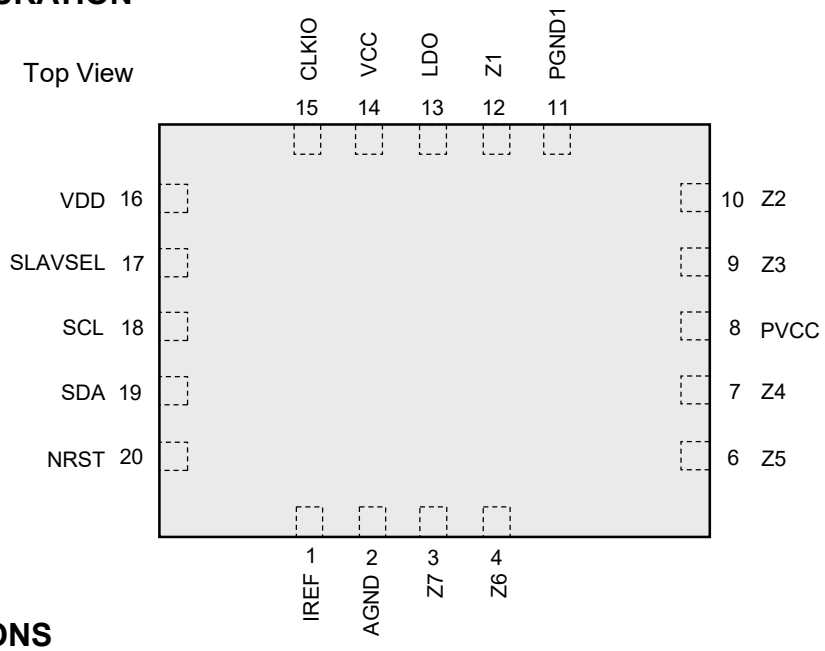
Notes: T_a = 25°C±2°C unless otherwise noted.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
I²C bus (Bus line specifications) (Continue)							
Hold time (repeated) START condition	$t_{HD:STA}$	The first clock pulse is generated after $t_{HD:STA.}$	0.26	—	—	µs	*7 *8
Low period of the SCL clock	t_{LOW}	—	0.5	—	—	µs	*7 *8
High period of the SCL clock	t_{HIGH}	—	0.26	—	—	µs	*7 *8
Set-up time for a repeat START condition	$t_{SU:STA}$	—	0.26	—	—	µs	*7 *8
Data hold time	$t_{HD:DAT}$	—	0	—	—	µs	*7 *8
Data set-up time	$t_{SU:DAT}$	—	50	—	—	ns	*7 *8
Rise time of both SDA and SCL signals	t_r	—	—	—	120	ns	*7 *8
Fall time of both SDA and SCL signals	t_f	—	—	—	120	ns	*7 *8
Set-up time of STOP condition	$t_{SU:STO}$	—	0.26	—	—	µs	*7 *8
Bus free time between STOP and START condition	t_{BUF}	—	0.5	—	—	µs	*7 *8
Capacitive load for each bus line	C_b	—	—	—	550	pF	*7 *8
Data valid time	$t_{VD:DAT}$	—	—	—	0.45	µs	*7 *8
Data valid acknowledge	$t_{VD:ACK}$	—	—	—	0.45	µs	*7 *8
Noise margin at the Low-level for each connected device	V_{nL}	—	0.1 × V_{DD}	—	—	V	*7 *8
Noise margin at the High-level for each connected device	V_{nH}	—	0.2 × V_{DD}	—	—	V	*7 *8

Note: *7 : The timing of Fast-mode Plus devices in I²C-bus is specified in page 10. All values referred to V_{IHMIN} and V_{ILMAX} level.

*8 : These are values checked by design but not production tested.

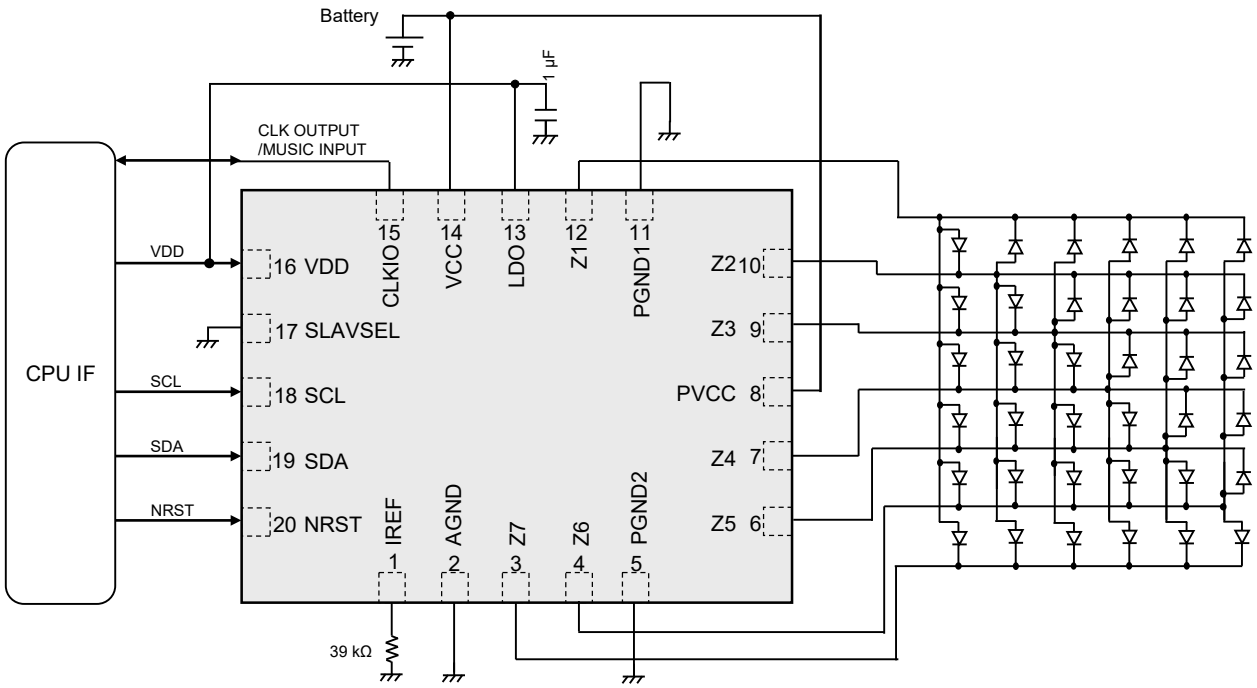
PIN CONFIGURATION



PIN FUNCTIONS

Pin No.	Pin name	Type	Description	Pin processing at unused
1	IREF	Output	Resistor connection pin for constant current setup	(Required pin)
2	AGND	Ground	Ground pin	(Required pin)
3	Z7	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
4	Z6	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
5 11	PGND2 PGND1	Ground	Power Ground pin	(Required pin)
6	Z5	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
7	Z4	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
8	PVCC	Power supply	Power supply for matrix driver	Battery or External power supply
9	Z3	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
10	Z2	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
12	Z1	Output	Constant current circuit, PWM control output pin, Control switch pin for matrix driver	Open
13	LDO	Output	LDO output pin	(Required pin)
14	VCC	Power supply	Power supply for Internal reference circuit	Battery or External power supply
15	CLKIO	Input/Output	Reference clock input output / Music Input pin	Open
16	VDD	Power supply	Power supply for I^2C interface	(Required pin)
17	SLAVSEL	Input	Slave address selection pin for I^2C interface	(Required pin)
18	SCL	Input	Clock input pin for I^2C interface	(Required pin)
19	SDA	Input/Output	Data input / output pin for I^2C interface	(Required pin)
20	NRST	Input	Reset input pin	(Required pin)

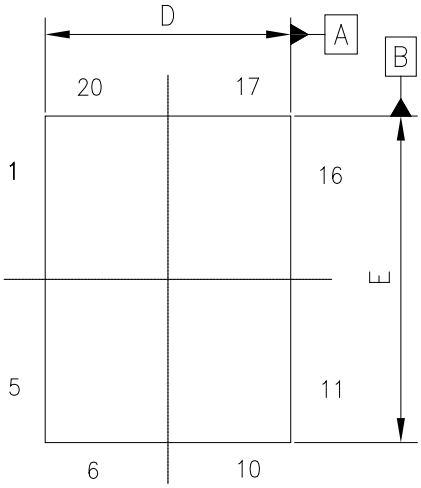
RECOMMENDED CIRCUIT

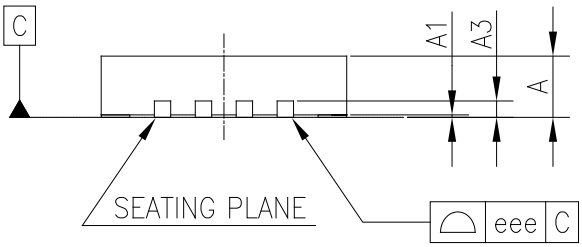


Note: The recommended circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. Customer is fully responsible for the incorporation of the above illustrated application circuit in the production.

PACKAGE INFORMATION

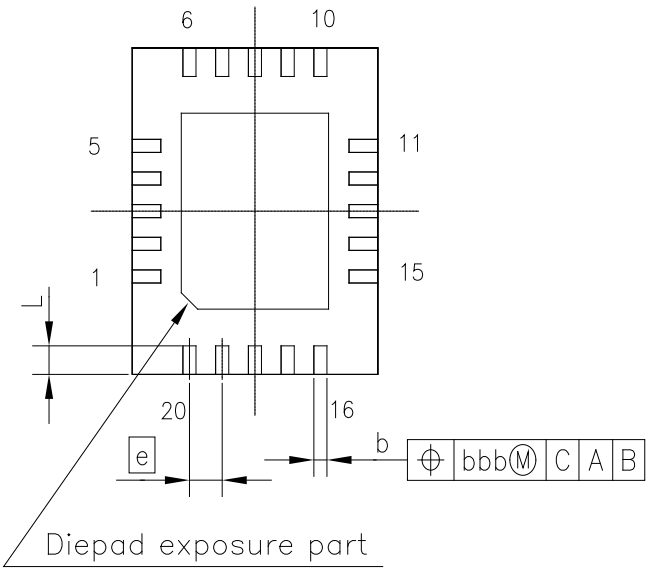
QFN 20L 3x4mm2, Thickness 0.8mm, Lead Pitch 0.4mm, Lead Length 0.35mm, EP Size 1.8x2.6mm

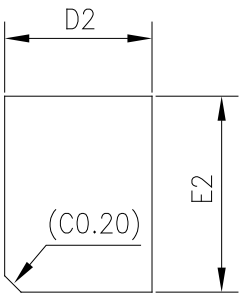




VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	0.80
A1	0.00	–	0.05
A3		0.20REF	
D	2.90	3.00	3.10
D2	1.70	1.80	1.90
E	3.90	4.00	4.10
E2	2.50	2.60	2.70
L	0.25	0.35	0.45
b	0.11	0.16	0.21
e		0.40BSC	
bbb		0.07	
eee		0.08	





Diepad exposure part

USAGE NOTES

1. Pay attention to the direction of IC. When mounting it in the wrong direction onto the PCB (printed-circuit-board), it might emit smoke or ignite.

2. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.

3. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the IC during transportation.

4. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.

5. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
   Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the IC might be damaged before the thermal protection circuit could operate.

6. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.

7. The product which has specified ASO (Area of Safe Operation) should be operated in ASO.

8. Verify the risks which might be caused by the malfunctions of external components.

Revision History

Date	Revision	Description
2020.10.31	1.00	1. initially issued
2021.3.15	1.01	1. Modify θ_{JA}, P_D (P4) 2. Modify pin configuration (P12)
2021.12.21	1.02	1. Added important notice on page2 2. Remove important notice page from previous version page 49

Important Notice

Nuvoton Products are neither intended nor warranted for usage in systems or equipment, any malfunction or failure of which may cause loss of human life, bodily injury or severe property damage. Such applications are deemed, "Insecure Usage".

Insecure usage includes, but is not limited to: equipment for surgical implementation, atomic energy control instruments, airplane or spaceship instruments, the control or operation of dynamic, brake or safety systems designed for vehicular use, traffic signal instruments, all types of safety devices, and other applications intended to support or sustain life.

All Insecure Usage shall be made at customer's risk, and in the event that third parties lay claims to Nuvoton as a result of customer's Insecure Usage, customer shall indemnify the damages and liabilities thus incurred by Nuvoton.