

## NAU8331VG / NAU8331A00VG

### 8W Class D Mono Multi-level Boost Amplifier with Speaker I/V Sense

#### Description

The NAU8331 is a Class-D monophonic boost amplifier device with V/I-Sense such that it can work with external speaker excursion control algorithms, which may be running on a separate Digital Signal Processor (DSP) or inside a main processor. Target applications for this device include mobile devices such as smartphones, personal media players, notebook and tablet computers, and laptops, where small speakers are essential. Other applications may include MP3 players, portable game players, digital camcorders, AR/VR headset as well as other computer types.

The NAU8331 features high output power capability, low-output noise in receiver mode, low-current shutdown mode, and click-and-pop suppression. It also support numerous types of device protection including over current and over voltage protection, under voltage lockout, and over temperature protection. In addition, on-chip battery monitoring SAR ADC along with ALC can automatically reduce the output gain to prevent the distortion when the battery level becomes low.

The multi-level boot converter is highly adaptive and efficient, which can boost the supply voltage up to 10.8V while producing ultra-low idle output noise. It can also control the supply rail of Class D amplifier in very fine 0.16V steps, which can maximize the loudness of small speakers, while preserving superior power efficiency at all input signal levels.

The NAU8331 operates with analog supply voltages from 1.6V to 1.98V, while the battery supply voltage can operate from 2.9V to 5.5V. The NAU8331 operating temperature range is specified from -40°C to +85°C, and is available in CSP 35 Ball package with a 0.5mm ball pitch.

#### Key Features

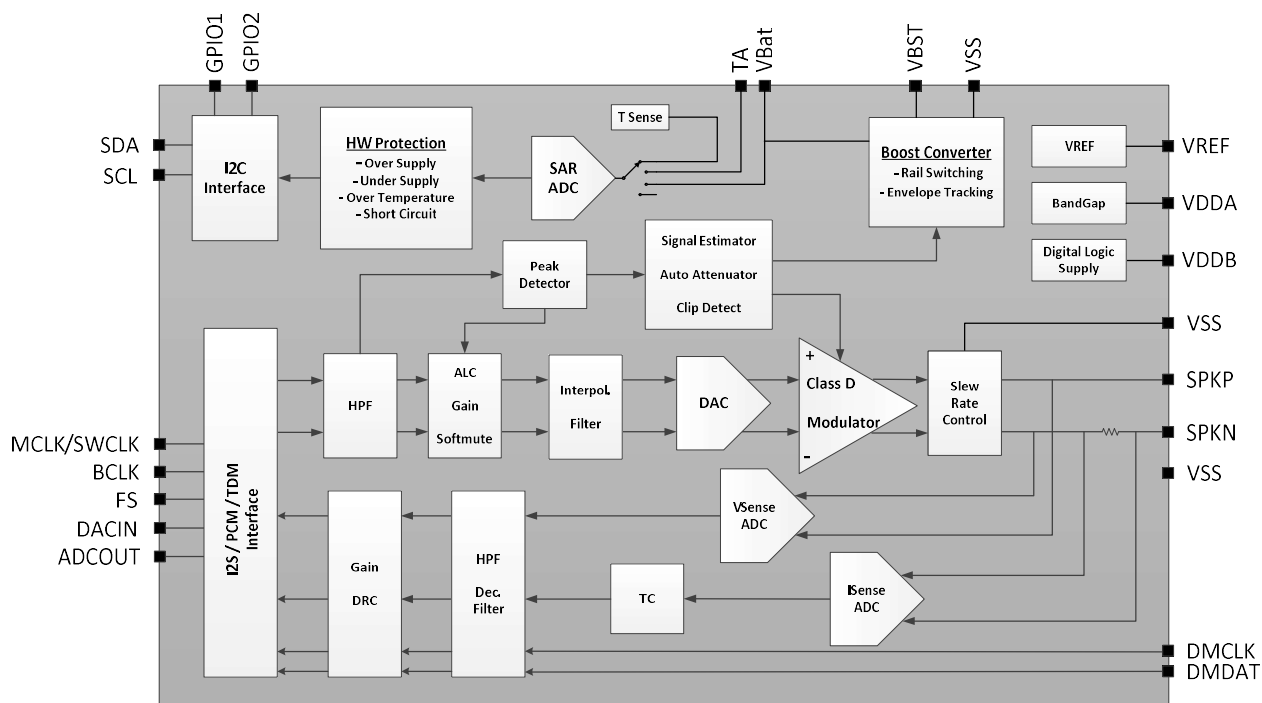
- Powerful Class-D Amplifier:
  - Up to 6 Watts into an 8 Ohm load at 10% Total Harmonic Distortion and Noise (THD+N)
  - Up to 8 Watts into an 4 Ohm load at 10% Total Harmonic Distortion and Noise (THD+N)
- High Efficiency Class-G Boost Converter
- Low Output Noise in Receiver Mode:
  - 18  $\mu\text{V}_{\text{RMS}}$
- $\geq 90$  dB Power Supply Rejection Ratio (PSRR)
- Low Current Shutdown Mode
- Click-and-Pop Suppression (30  $\mu\text{V}_{\text{RMS}}$ )
- Programmable Serial Interfaces:
  - I2C Interface
  - I2S Interface
  - PCM Interface
  - Stereo Digital Microphone Interface
- Device Protection:
  - Over Current Protection (OCP),
  - Over Voltage Protection (OVP)
  - Under Voltage Lock Out (UVLO)
  - Over Temperature Protection (OTP)
  - Clock Termination Protection (CTP)
- Speaker Protection:
  - Current & Voltage Sensing
  - Anti-Clip Protection (ACP)
  - Ambient Temperature Sense Input
- Battery Protection: Limiter
- Filter-less Electro Magnetic Interference (EMI) mitigation
- 35-Ball Wafer Level Chip Scale Package (WLCSP) (0.5 mm Pitch)

#### Applications

- Smartphones
- Notebooks /Tablets/ Personal Computers
- Personal Media Players/Portable Televisions
- MP3 Lossless Standard Audio Compression Format Players
- Portable Game Players
- Digital Camcorders

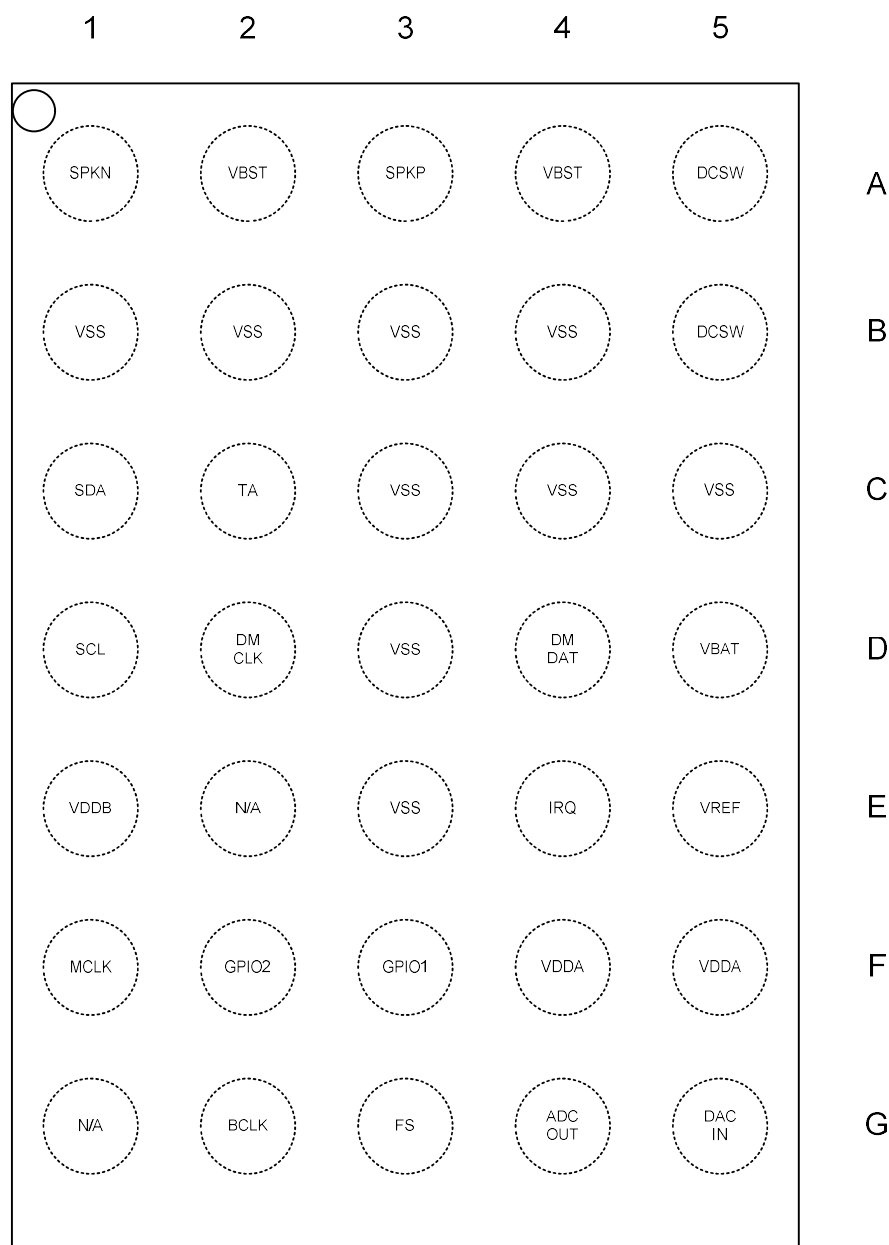
## Block Diagram

Figure 1: NAU8331 Block Diagram



## Pin Diagram

Figure 2: NAU8331 Pin Diagram



Ball array = 5x7; Pitch = 0.5mm;  
 Die = 2.58x3.86mm w/ scribe;  
 Top view; Marking Side; FT

## Pin Descriptions

**Table 1 NAU8331 Pin Descriptions**

| Pin # | Name   | Type, (Supply Domain)   | Description                                                      |
|-------|--------|-------------------------|------------------------------------------------------------------|
| A1    | SPKN   | Analog Output, (VBAT)   | Class-D Negative Speaker Output Terminal; Current Sense Input    |
| A2    | VBST   | Analog I/O, (VBAT)      | DC-DC Boost Converter Output                                     |
| A3    | SPKP   | Analog Output, (VBAT)   | Class-D Positive Speaker Output Terminal; Current Sense Input    |
| A4    | VBST   | Analog I/O, (VBAT)      | DC-DC Boost Converter Output                                     |
| A5    | DCSW   | Analog I/O, (VBAT)      | DC-DC Boost Converter Switch                                     |
| B1    | VSS    | Ground                  | Supply Ground                                                    |
| B2    | VSS    | Ground                  | Supply Ground                                                    |
| B3    | VSS    | Ground                  | Supply Ground                                                    |
| B4    | VSS    | Ground                  | Supply Ground                                                    |
| B5    | DCSW   | Analog I/O, (VBAT)      | DC-DC Boost Converter Switch                                     |
| C1    | SDA    | Digital I/O, (VDDDB)    | Serial Data for I2C                                              |
| C2    | TA     | Analog Input, (VDDA)    | Ambient Temperature Sense Input, tie to VSS if not used          |
| C3    | VSS    | Ground                  | Supply Ground                                                    |
| C4    | VSS    | Ground                  | Supply Ground                                                    |
| C5    | VSS    | Ground                  | Supply Ground                                                    |
| D1    | SCLK   | Digital Input, (VDDDB)  | Serial Data Clock for I2C                                        |
| D2    | DMCLK  | Digital Output, (VDDA)  | Serial Data Clock for Digital Microphone                         |
| D3    | VSS    | Ground                  | Supply Ground                                                    |
| D4    | DMDAT  | Digital Input, (VDDA)   | Serial Data Input from Digital Microphones                       |
| D5    | VBAT   | Supply                  | Battery Supply Voltage                                           |
| E1    | VDDDB  | Supply                  | Digital IO Supply                                                |
| E2    | N/A    |                         |                                                                  |
| E3    | VSS    | Ground                  | Supply Ground                                                    |
| E4    | IRQ    | Digital Output, (VDDDB) | Programmable Interrupt Output                                    |
| E5    | VREF   | Analog I/O, (VDDA)      | Internal DAC & ADC Voltage Reference Decoupling I/O              |
| F1    | MCLK   | Digital Input, (VDDDB)  | Master Clock                                                     |
| F2    | GPIO2  | Digital I/O, (VDDDB)    | General Purpose IO2/Address Selection 2                          |
| F3    | GPIO1  | Digital I/O, (VDDDB)    | General Purpose IO1/Address Selection 1                          |
| F4    | VDDA   | Supply                  | 1.8 V Analog & Digital Core Supply. F4 and F5 are tied together. |
| F5    | VDDA   | Supply                  |                                                                  |
| G1    | N/A    |                         |                                                                  |
| G2    | BCLK   | Digital I/O, (VDDDB)    | Serial Audio Data Bit Clock I2S/PCM Input                        |
| G3    | FS     | Digital I/O, (VDDDB)    | Frame Sync I2S/PCM Input                                         |
| G4    | ADCOUT | Digital Output, (VDDDB) | Serial Audio I2S/PCM Data Output                                 |
| G5    | DACIN  | Digital Input, (VDDDB)  | Serial Audio Data I2S/PCM Input                                  |

## Electrical Characteristic

### Absolute Maximum Ratings

CAUTION: Do not operate at or near maximum ratings extended periods. Stresses above those listed in Table 2 may cause permanent damage to the device. Exposure to conditions beyond these ratings may adversely affect the life and reliability of the device and result in failures not covered by warranty.

**Table 2 Absolute Maximum Ratings**

| Parameter                            | Min       | Max         | Units |
|--------------------------------------|-----------|-------------|-------|
| VDDDB Digital I/O Supply Range       | -0.3      | 4.0         | V     |
| VBAT Battery Supply Range            | -0.3      | 6.0         | V     |
| VDDA Analog Supply Range             | -0.3      | 2.2         | V     |
| Voltage Input Analog Range           | VSS - 0.3 | VDDA + 0.3  | V     |
| Voltage Input I/O Range              | VSS - 0.3 | VDDDB + 0.3 | V     |
| Junction Temperature, T <sub>J</sub> | -40       | +150        | °C    |
| Storage Temperature                  | -65       | +150        | °C    |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely influence product reliability and result in failures not covered by the warranty.

### Operating Conditions

**Table 3 Recommended Operating Conditions**

| Condition                        | Symbol | Min  | Typical | Max  | Units |
|----------------------------------|--------|------|---------|------|-------|
| Battery Supply Range             | VBAT   | 2.90 | 4.2     | 5.50 | V     |
| Analog Supply Range              | VDDA   | 1.62 | 1.8     | 1.98 | V     |
| Digital I/O Supply Range         | VDDDB  | 1.62 | 3.0     | 3.6  | V     |
| Ground                           | VSS    |      | 0       |      | V     |
| Industrial Operating Temperature |        | -40  |         | +85  | °C    |

CAUTION: The following conditions needed to be followed for regular operation: VBAT > VDDA - 1.2V; VDDDB > VDDA - 0.6V.

## Electrical Parameters

**Table 4 Electrical Parameters**

Conditions:  $V_{DDA} = V_{ddb} = 1.8V$ ;  $V_{BAT} = 4.2V$ .  $R_L = 8\ \Omega + 33\ \mu H$ ,  $f = 1kHz$ , 48kHz sample rate, MCLK=12.88MHz, Boost Inductor =  $1\ \mu H$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$

| Symbol          | Parameter                         | Conditions                                                                               | Typical   | Limit | Units |
|-----------------|-----------------------------------|------------------------------------------------------------------------------------------|-----------|-------|-------|
| ISD             | Shutdown Supply Current           | V <sub>DDA</sub> , all clocks off                                                        | 2.0       | 10    | μA    |
|                 |                                   | V <sub>ddb</sub> , all clocks off                                                        | 0.3       | 2     |       |
|                 |                                   | V <sub>BAT</sub> , all clocks off                                                        | 0.4       | 4     |       |
| ISB             | Standby Mode Supply Current       | V <sub>DDA</sub> , MCLK off, clock gating on                                             | 2.0       |       | μA    |
|                 |                                   | V <sub>ddb</sub> , MCLK off, clock gating on                                             | 0.3       |       | μA    |
|                 |                                   | V <sub>BAT</sub> , MCLK off, clock gating on                                             | 0.4       |       | μA    |
| IDD             | Operating Mode Supply Current     | V <sub>DDA</sub> , idle Channel                                                          | 10        |       | mA    |
|                 |                                   | V <sub>ddb</sub> , idle Channel                                                          | 0.2       |       | mA    |
|                 |                                   | V <sub>BAT</sub> , idle Channel                                                          | 3         |       | mA    |
| Class-D Channel |                                   |                                                                                          |           |       |       |
| P <sub>O</sub>  | Output Power                      | RL = 8 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 1%                      | 5.5       |       | W     |
|                 |                                   | RL = 8 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 10%                     | 6         |       | W     |
|                 |                                   | RL = 4 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 1%                      | 6.5       |       | W     |
|                 |                                   | RL = 4 Ohm + 33 μH and Total Harmonic Distortion+Noise (THD+N) = 10%                     | 8         |       | W     |
| THD+N           | Total Harmonic Distortion + Noise | RL = 8 Ω + 33 μH, f=1kHz, P <sub>O</sub> = 2 W                                           | 0.017     |       | %     |
| eos             | Output Noise                      | A-Weighted, 20Hz-20kHz, Receiver mode or Auto attenuate, no DAC input signal, gain = 0dB | 18        |       | μVrms |
|                 |                                   | A-Weighted, 20Hz-20kHz, no DAC input signal, gain = 16.8dB                               | 50        |       | μVrms |
| PSRR            | Power Supply Rejection Ratio      | DC, V <sub>BAT</sub> = 2.9V – 5.5V, GAIN = 16.8dB                                        | 92        |       | dB    |
|                 |                                   | f <sub>ripple</sub> = 217Hz, V <sub>ripple</sub> = 200mV <sub>P_P</sub> GAIN = 16.8dB    | 92        |       | dB    |
|                 |                                   | f <sub>ripple</sub> = 1020Hz, V <sub>ripple</sub> = 200mV <sub>P_P</sub> GAIN = 16.8dB   | 92        |       | dB    |
|                 |                                   | f <sub>ripple</sub> = 4kHz, V <sub>ripple</sub> = 200mV <sub>P_P</sub> GAIN = 16.8dB     | 88        |       | dB    |
| Fres            | Frequency Response                | F = 20Hz ~ 20KHz, 1Watt, RL = 8 Ω + 33 μH                                                | +0.8/-0.1 |       | dB    |
| V <sub>OS</sub> | Output Offset Voltage             | Idle Channel, Gain= 0dB                                                                  | ±1        | ±5    | mV    |
| Kpop            | Pop and Click Noise               | A-weighted, Idle DAC input, Clock Gating, toggling clocks on/off                         | 0.03      |       | mVrms |

| Symbol                           | Parameter                                        | Conditions                                                                            | Typical | Limit | Units           |
|----------------------------------|--------------------------------------------------|---------------------------------------------------------------------------------------|---------|-------|-----------------|
|                                  |                                                  | A-weighted, Idle DAC input, toggling between -120dBFS DAC In & 2048 zero samples      | 0.03    |       | mVrms           |
| Rdson-P                          | Driver P MOS-FET ON-resistance                   | V <sub>BAT</sub> = 5.0V. R <sub>L</sub> = 8 $\Omega$ + 33 $\mu$ H, DC Output Clipping | 0.112   |       | Ohm             |
| Rdson-N                          | Driver N MOS-FET ON- resistance                  | V <sub>BAT</sub> = 5.0V. R <sub>L</sub> = 8 $\Omega$ + 33 $\mu$ H, DC Output Clipping | 0.116   |       | Ohm             |
| Fsw                              | Switching Frequency                              | Average                                                                               | 300     |       | kHz             |
| <b>Voltage Sense ADC</b>         |                                                  |                                                                                       |         |       |                 |
| THD+N                            | ADC Total Harmonic Distortion + Noise            | V <sub>BAT</sub> = 5.5V, +10dBVrms, Class-D off                                       | 0.004   |       | %               |
| SNR                              | Signal to Noise Ratio                            | Flat, 20Hz – 20kHz                                                                    | 101     |       | dB              |
| FS <sub>ADC</sub>                | ADC Full Scale Input Level                       |                                                                                       | 14.4    |       | V <sub>PK</sub> |
| <b>Current Sense ADC</b>         |                                                  |                                                                                       |         |       |                 |
| THD+N                            | ADC Total Harmonic Distortion + Noise            | V <sub>BAT</sub> =5.5 with 8Ohm + 33uH, Po=3W                                         | 0.37    |       | %               |
| SNR                              | Signal to Noise Ratio                            | Flat, 20Hz – 20kHz                                                                    | 69      |       | dB              |
| FS <sub>ADC</sub>                | ADC Full Scale Input Level                       |                                                                                       | 4.04    |       | A <sub>PK</sub> |
| <b>Battery Sense ADC</b>         |                                                  |                                                                                       |         |       |                 |
| INL                              | Integrated Non-Linearity                         | V <sub>BAT</sub> = 2.9V-5.5V (gain & offset compensated)                              | +/-1    |       | LSB             |
| DNL                              | Differential Non-Linearity                       | V <sub>BAT</sub> = 2.9V-5.5V                                                          | +/-1    |       | LSB             |
| <b>Boost Converter</b>           |                                                  |                                                                                       |         |       |                 |
| Fsw                              | Switching Frequency                              |                                                                                       | 2.0     |       | MHz             |
| Vbstmax                          | Boost Converter Maximum Output Voltage           |                                                                                       | 10.98   |       | V               |
| Vbstmin                          | Boost Converter Minimum Output Voltage           |                                                                                       | 2.9     |       | V               |
| Vbststp                          | Boost Converter Step Voltage                     |                                                                                       | 0.16    |       | V               |
| Vovp                             | Boost Converter Overvoltage Protection Threshold |                                                                                       | 12.7    |       | V               |
| Rdson-P                          | Boost Converter P MOS-FET ON-resistance          |                                                                                       | 0.1     |       | Ohm             |
| Rdson-N                          | Boost Converter N MOS-FET ON-resistance          |                                                                                       | 0.1     |       | Ohm             |
| <b>Boost Converter + Class-D</b> |                                                  |                                                                                       |         |       |                 |
| Neff                             | Power Efficiency                                 | Output Power = 0.45 W, V <sub>BAT</sub> = 5.0 V                                       | 75      |       | %               |
|                                  |                                                  | Output Power = 1.0 W, V <sub>BAT</sub> = 5.0 V                                        | 78      |       | %               |
|                                  |                                                  | Output Power = 6.0 W, V <sub>BAT</sub> = 5.0 V                                        | 80      |       | %               |

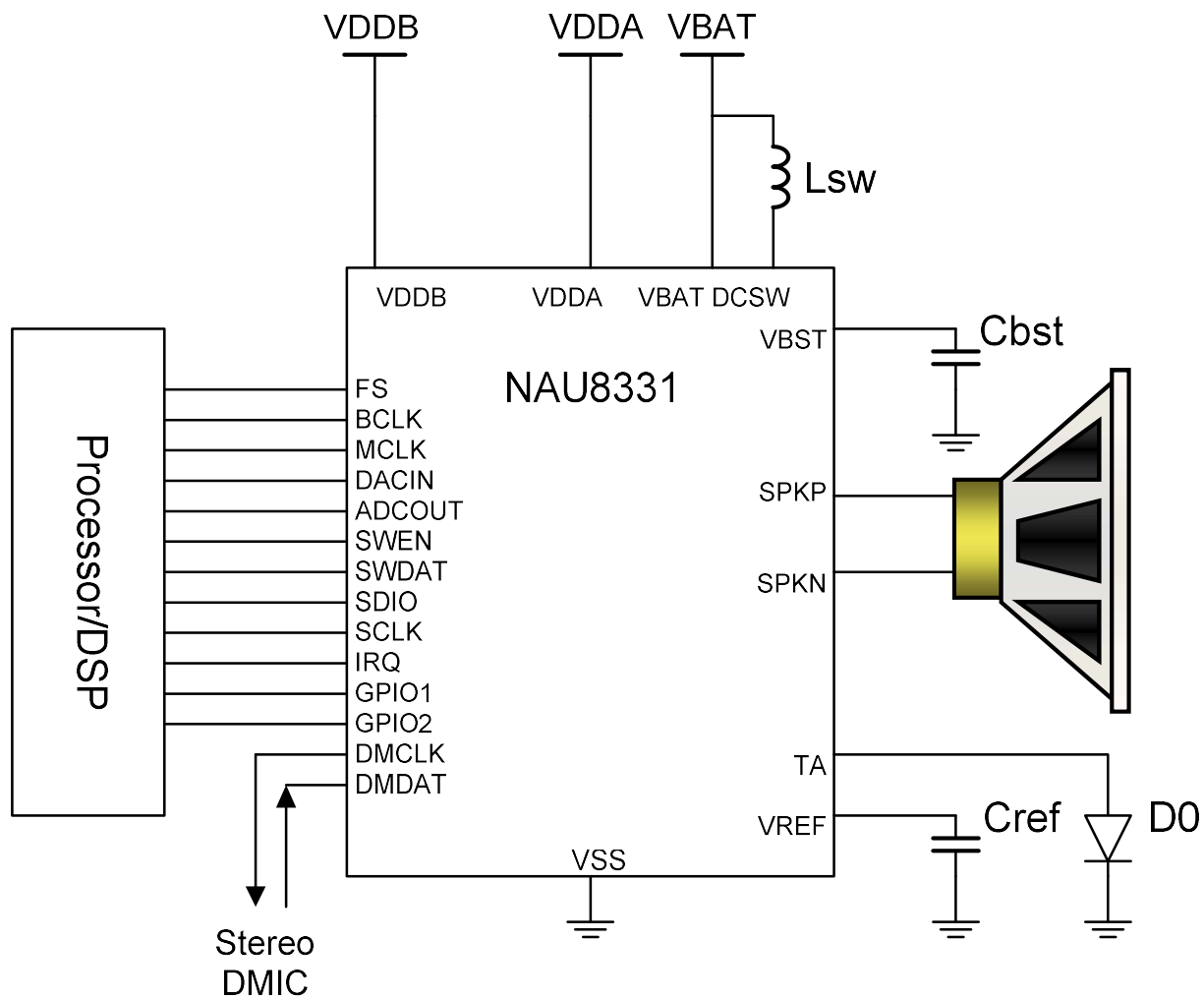
## Digital I/O Characteristics

**Table 5 Digital I/O Characteristics**

| Parameter         | Symbol   | Comments/Conditions |                  | Min                  | Max                  | Units |
|-------------------|----------|---------------------|------------------|----------------------|----------------------|-------|
| Input LOW level   | $V_{IL}$ | $V_{DDB} = 1.8V$    |                  |                      | $0.33 \cdot V_{DDB}$ | V     |
|                   |          | $V_{DDB} = 3.3V$    |                  |                      | $0.37 \cdot V_{DDB}$ |       |
| Input HIGH level  | $V_{IH}$ | $V_{DDB} = 1.8V$    |                  | $0.67 \cdot V_{DDB}$ |                      | V     |
|                   |          | $V_{DDB} = 3.3V$    |                  | $0.63 \cdot V_{DDB}$ |                      |       |
| Output HIGH level | $V_{OH}$ | $I_{Load} = 1mA$    | $V_{DDB} = 1.8V$ | $0.9 \cdot V_{DDB}$  |                      | V     |
|                   |          |                     | $V_{DDB} = 3.3V$ | $0.95 \cdot V_{DDB}$ |                      |       |
| Output LOW level  | $V_{OL}$ | $I_{Load} = 1mA$    | $V_{DDB} = 1.8V$ |                      | $0.1 \cdot V_{DDB}$  | V     |
|                   |          |                     | $V_{DDB} = 3.3V$ |                      | $0.05 \cdot V_{DDB}$ |       |

## Application Diagram

Figure 3 Application Diagram



## Ordering Information

**Table 6 Ordering Information**

| Part Number  | Dimension            | Package        | Package Material |
|--------------|----------------------|----------------|------------------|
| NAU8331VG    | 3.835mm x<br>2.555mm | WLCSP 35-Balls | Green            |
| NAU8331xxxVG | 3.835mm x<br>2.555mm | WLCSP 35-Balls | Green            |

NAU8331VG = mono boosted Class D amplifier with DMIC interface

NAU8331xxxVG = mono boosted Class D amplifier with Algorithm Option

xxx = Algorithm Option

|     |                                                                                                                                                                                            |
|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A00 | Waves Audio Enhancement and Speaker Protection algorithm including followings;<br><br>MaxxEQ, MaxxBass, MaxxVolume, MaxxLeveler, MaxxTreble, MaxxStereo, MaxxDialog, Multiband Compressor. |
|     |                                                                                                                                                                                            |

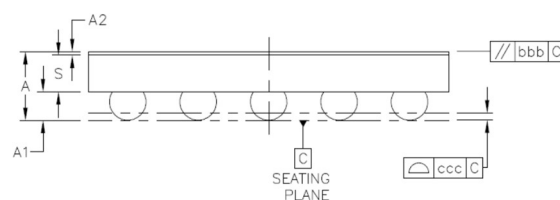
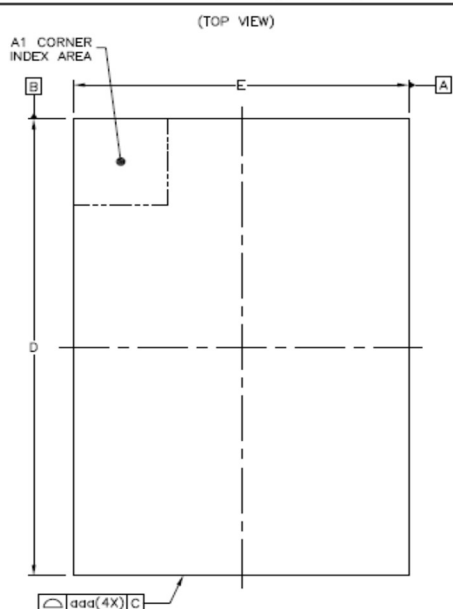
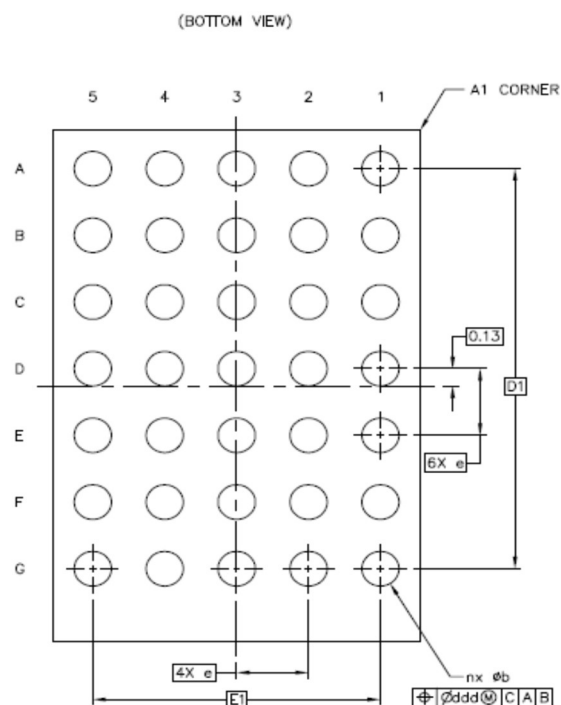
V = indicates WLCSP packaging WLCSP

G = Lead-Free (Green) Packaging:

# Package Information

Figure 4 WLCSP Package Dimensions (35 Balls with 0.5mm Pitch)

|                            | SYMBOL | MIN   | NOM   | MAX   |
|----------------------------|--------|-------|-------|-------|
| TOTAL THICKNESS            | A      | 0.517 | 0.575 | 0.633 |
| WAFER THICKNESS            | S      | 0.325 | 0.35  | 0.375 |
| STAND OFF                  | A1     | 0.17  | ---   | 0.23  |
| FILM THICKNESS             | A2     | 0.022 | 0.025 | 0.028 |
| BODY SIZE                  | X      | E     | 2.55  |       |
|                            | Y      | D     | 3.83  |       |
| BALL/BUMP PITCH            | X      | SE    | ---   | BSC   |
|                            | Y      | SD    | ---   | BSC   |
| EDGE BALL CENTER TO CENTER | X      | E1    | 2     | BSC   |
|                            | Y      | D1    | 3     | BSC   |
| PITCH                      | e      | 0.5   | BSC   |       |
| BALL DIAMETER (SIZE)       |        |       | 0.25  |       |
| BALL/BUMP WIDTH            | b      | 0.23  | ---   | 0.29  |
| BALL/BUMP COUNT            | n      | 35    |       |       |
| PACKAGE EDGE TOLERANCE     | ddd    | 0.03  |       |       |
| WAFER FLATNESS             | bbb    | 0.06  |       |       |
| COPLANARITY                | ccc    | 0.05  |       |       |
| BALL/BUMP OFFSET (PACKAGE) | ddd    | 0.015 |       |       |
|                            |        |       |       |       |
|                            |        |       |       |       |
|                            |        |       |       |       |
|                            |        |       |       |       |



## Revision History

**Table 7: Revision History**

| Version |              |         | Description                             |
|---------|--------------|---------|-----------------------------------------|
| #       | Date         | Page(s) |                                         |
| 0.1     | Nov 10, 2016 | NA      | Preliminary Version                     |
| 1.0     | Oct 10, 2017 |         | Fully updated with latest test results. |
| 2.0     | Nov 08, 2018 |         | Fully updated with latest test results. |

### Important Notice

Nuvoton products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Furthermore, Nuvoton products are not intended for applications wherein failure of Nuvoton products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

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