8-bit Microcontroller

KM101EFA1A
Datasheet

For additional information or question, please contact Nuvoton Technology Corporation Japan.

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1. Overview

1.1 Overview

The KM101E series of 8-bit single-chip microcomputers incorporate multiple types of peripheral functions. This chip series is well suited for automotive power window, camera, TV, CD, printer, telephone, home appliance, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcomputer applications flexible, optimized hardware configurations and a simple efficient instruction set. KM101EFA1A has an internal 32 KB of ROM and 1 KB of RAM. Peripheral functions include 5 external interrupts, including NMI, 8 timer counters, 3 types of serial interfaces, A/D converter, watchdog timer and buzzer output. The system configuration is suitable for system control microcontroller.

With 2 oscillation systems (internal frequency: 16 MHz, crystal/ceramic frequency: max. 10 MHz) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode) or PLL input (PLL mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has NORMAL mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in NORMAL mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz. A machine cycle in the PLL mode is 50 ns (maximum).

1.2 Product Summary

This datasheet describes the following model.

Table: 1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EFA1A	32 KB	1 KB	Flash EEPROM version	QFP 44-pin

2. Hardware Functions

- Memory Capacity — ROM capacity: 32 KB
  RAM capacity: 1 KB
- Package — QFP 44-Pin (10 mm × 10 mm / 0.8 mm pitch)
- Machine Cycle — 0.05 μs / fs: 20 MHz (4.0 V to 5.5 V)
- Oscillation circuit — Internal oscillation (frc): 16 MHz
  Crystal/ceramic (fosc): Maximum 10 MHz
- Clock Multiplication circuit (PLL Circuit)

  PLL circuit output clock (fpll):
  fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
  1/2 × frc multiplication by 4, 5 enable
- Clock Gear for System Clock

  System Clock (fs): fpll divided by 1, 2, 4, 16, 32, 64, 128
- Clock Gear for control clock of peripheral function

  Control clock of peripheral function (fpll-div): stop or fpll divided by 1, 2, 4, 8, 16
- Operation Mode — NORMAL mode
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)
- Operating Voltage — 4.0 V to 5.5 V
- Operation ambient temperature

  -40 °C to +85 °C

- Interrupt

23 levels

<Non-maskable interrupt>
- Non-maskable interrupt and Watchdog timer overflow interrupt

<Timer interrupts>
- Timer 0 interrupt
- Timer 1 interrupt
- Timer 2 interrupt
- Timer 6 interrupt
- Time base timer interrupt
- Timer 7 interrupt
- Timer 7 compare register 2 match interrupt
- Timer 9 overflow interrupt
- Timer 9 underflow interrupt
- Timer 9 compare register 2 match interrupt

<Serial Interface interrupts>
- Serial interface 0 interrupt
- Serial interface 0 UART reception interrupt
- Serial interface 1 interrupt
- Serial interface 1 UART reception interrupt
- Serial interface 4 interrupt
- Serial interface 4 stop condition interrupt

<A/D interrupt>
- A/D conversion interrupt

<External interrupts>
- IRQ0: Edge selectable, noise filter connection available
- IRQ1: Edge selectable, noise filter connection available
- IRQ2: Edge selectable, noise filter connection available, both edges interrupt
- IRQ3: Edge selectable, noise filter connection available, both edges interrupt
- IRQ4: Edge selectable, noise filter connection available, both edges interrupt, Key scan interrupt

- Timer Counter

8 timers
- 8-bit timer for general use × 3 sets
- 16-bit timer for general use × 1 set
- Motor control 16-bit timer × 1 set
- 8-bit free-run timer × 1 set
- Time base timer × 1 set
- Baud rate timer × 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM0IOB
- Event count
- Simple pulse measurement
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, External clock, Timer A output

- Timer Counter (continued)

Timer 1 (8-bit timer for general use)
- Square wave output (Timer pulse output) can be output to large current pin TM1IOB
- Event count
- 16-bit cascade connected (with Timer 0)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, External clock, Timer A output

Timer 2 (8-bit timer for general use)
- Square wave output (Timer pulse output)
- Added pulse (2-bit) type PWM output can be output to large current pin TM2IOB
- Event count
- Simple pulse measurement
- 24-bit cascade connected (with Timer 0 and Timer 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128,
  fs/2, fs/4, fs/8, External clock, Timer A output

Timer 6 (8-bit free-run timer, Time base timer)
8-bit free-run timer
- Clock source
  fpll-div, fpll-div/2^{12}, fpll-div/2^{13}, fs

Time base timer
- Interrupt generation cycle
  fpll-div/2^{7}, fpll-div/2^{8}, fpll-div/2^{9}, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}

Timer 7 (16-bit timer for general use)
- Square wave output (Timer pulse output)
- High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB
- Event count
- Input capture function (Both edges can be operated)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer 9 (Motor control 16-bit timer)
- Square wave output (Timer pulse output)
- Event count
- Complementary 3-phase PWM output can be output to large current pin TM9OD0 to TM9OD5
  (Triangle wave and saw tooth wave are supported, dead time insertion available)
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/16, fs, fs/2, fs/4, fs/16,
  Timer A divided by 1, 2, 4, 16, External clock divided by 1, 2, 4, 16

Timer A (Baud rate timer)
- Clock output for peripheral functions
- Clock source
  fpll-div, fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/16, fpll-div/32, fs/2, fs/4

- Watchdog timer — Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
  On detection of 2 errors, forcibly hard reset inside LSI.
  Operation start timing is selectable. (At reset release or write to register)
- Buzzer Output/ Reverse Buzzer Output

  Output frequency can be selected from $fpll\text{-}div/2^{9}$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$
- A/D Converter — 10-bit × 12 channels
- Serial Interface — 3 channels

  Serial 0: UART (full duplex)/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
  - Sequence transmission, reception or both are available

  Full duplex UART
  - Baud rate timer, selected from Timer 0 to 2 or Timer A
  - Parity check, overrun error/ framing error detection
  - Transfer size 7 to 8 bits can be selected

  Serial 1: UART (full duplex)/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4, Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
  - Sequence transmission, reception or both are available.

  Full duplex UART
  - Baud rate timer, selected from Timer 0 to 2 or Timer A
  - Parity check, overrun error/ framing error detection
  - Transfer size 7 to 8 bits can be selected

  Serial 4: Multi master IIC/ Clock synchronous
  Clock synchronous serial interface
  - Transfer clock source fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/32, fs/2, fs/4, Timer 0 to 2 or Timer A divided by 1, 2, 4, 8, 16, External clock
  - MSB/LSB can be selected as the first bit to be transferred, arbitrary sizes of 1 to 8 bits are selectable.
  - Sequence transmission, reception or both are available.

  Multi master IIC
  - 7-bit slave address is settable.
  - General call communication mode is supported.

• Automatic Reset	Power detection level: 4.3 V (at rising), 4.2 V (at falling)		
• LED Driver	16 pins (Port 0 or Port A)		
• Ports	I/O ports	36 pins	
	Serial Interface pins	12 pins	
	Timer I/O	15 pins	
	Buzzer output pins	2 pins	
	A/D input pins	12 pins	
	External Interrupt pins	6 pins	
	LED (large current) driver	16 pins	(Port 0 or Port A)
	High-speed oscillation	2 pins	
	Special pins	8 pins	
	Operation mode input pins	3 pins	
	Reset input pin	1 pin	
	Analog reference voltage input pin	1 pin	
	Power pins	3 pins	

3 Pin Description

3.1 Pin configuration

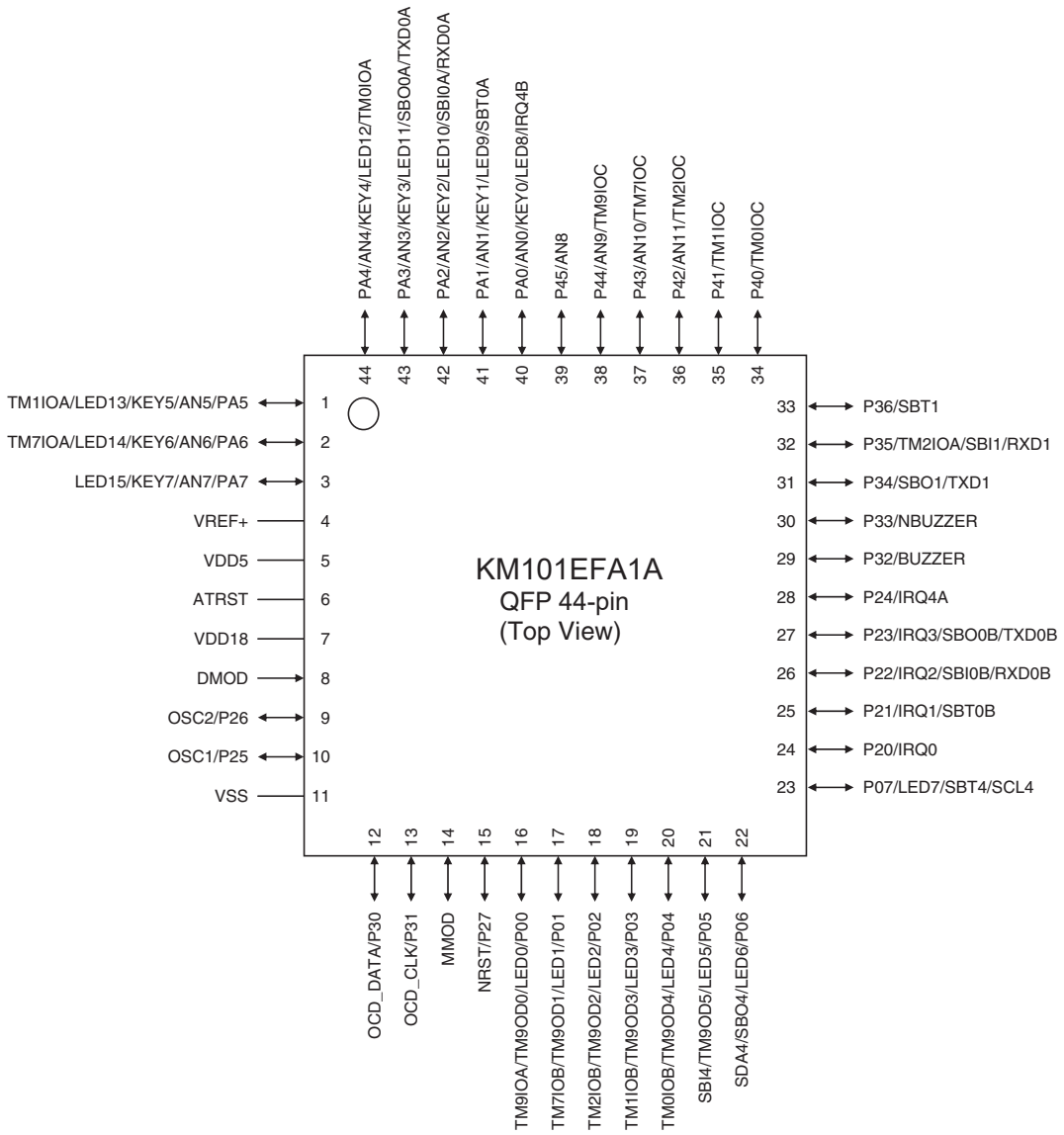

Figure: 3.1 Pin Configuration (KM101EFA1A QFP 44-pin)

3.2. Pin Functions

Table: 3.1 Pin Functions

Pins	Pin No	I/O	Function	Description
VDD5	5	-	Power connect pins	Apply 4.0 V to 5.5 V to VDD5 and 0 V to VSS connect 0.1 μF + 1 μF or larger bypass capacitor for internal power stabilization.
VSS	11	-		
VDD18	7	-	Internal power output pin	This pin is output 1.8 V from internal power circuit. Don't use the power supply to external device. For internal power circuit output stability, connect at least 0.1 μF + 1 μF one bypass capacitor between VDD18 and VSS.
OSC1	10	Input	High speed operation clock input pin	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation.
OSC2	9	Output	High speed operation clock output pin	If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using STOP mode.
NRST	15	I/O	Reset pins [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD5.
ATRST	6	Input	Auto reset setting pin	Input "High" to enable auto reset function and "Low" to disable this function
P00 P01 P02 P03 P04 P05 P06 P07	16 17 18 19 20 21 22 23	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	24 25 26 27 28 10 9	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P2DIR register. A pull-up resistor for each bit can be selected individually by P2PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance)
P27	15	Input	Input port 2	P27 has an N-channel open-drain configuration.
P30 P31 P32 P33 P34 P35 P36	12 13 29 30 31 32 33	I/O	I/O port 3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P3DIR register. A pull-up resistor for each bit can be selected individually by P3PLU register. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
P40 P41 P42 P43 P44 P45	34 35 36 37 38 39	I/O	I/O port 4	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by P4PLUD register. A pull-up/down resistor connection for each port can be selected individually in SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).

Pins	Pin No	I/O	Function	Description
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	40 41 42 43 44 1 2 3	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by P0DIR register. A pull-up resistor for each bit can be selected individually by P0PLU register. Direct LED drive is available at output. At reset, the input mode is selected and pull-up resistor is disabled (high impedance).
SBO0A SBO0B SBO1 SBO4	43 27 31 22	Output	Serial interface transmission data output pins	Transmission data output pins for serial interface 0,1,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLU and PAPLU registers. Select output mode in P0DIR, P2DIR, P3DIR and PADIR registers and set serial data output mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBI0A SBI0B SBI1 SBI4	42 26 32 21	Input	Serial interface reception data input pins	Reception data input pins for serial interface 0,1,4. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLUand PAPLU registers. Select the output mode in P0DIR, P2DIR, P3DIR and PADIR registers and select serial data input mode in serial mode register 1 (SC0MD1, SC1MD1, SC4MD1). These can be used as normal I/O pins when serial interface is not used.
SBT0A SBT0B SBT1 SBT4	41 25 33 23	I/O	Serial interface Clock I/O pins	Clock I/O pins for serial interface 0,1,4. The output configuration, either COMS push-pull or Nch open-drain can be selected in P0ODC, P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected in P0PLU, P2PLU, P3PLU and PAPLU registers. Select clock I/O in P0DIR, P2DIR, P3DIR and PADIR registers and serial mode register 1 (SC0MD1, SC1MD1, SC4MD1) with the communication mode. These can be used as normal I/O pins when serial interface is not used.
TXD0A TXD0B TXD1	43 27 31	Output	UART transmission data output pins	In serial interface 0,1 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either COMS push-pull or Nch open-drain can be selected in P2ODC, P3ODC and PAODC registers. Pull-up resistor can be selected by P2PLU, P3PLU and PAPLU registers. Select the output mode in P2DIR, P3DIR and PADIR registers and select serial data output mode in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when serial interface is not used.
RXD0A RXD0 RXD1	42 26 32	Input	UART reception data input pins	In serial interface 0,1 in UART mode, this pin is configured as the reception data input pin. Pull-up resistor can be selected in P2PLU, P3PLU and PAPLU registers. Select the input mode in P2DIR, P3DIR and PADIR registers and select serial input in serial mode register 1 (SC0MD1, SC1MD1). These can be used as normal I/O pins when serial interface is not used.

Pins	Pin No	I/O	Function	Description
SDA4	22	I/O	IIC data I/O pins	In serial interface 4 in IIC mode, this pin is configured as the data I/O pin. For the output configuration, select Nch open-drain in P0ODC register and set pull-up resistor in P0PLU register. Select the output mode in P0DIR register and select serial data I/O mode by serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used.
SCL4	23	I/O	IIC clock I/O pins	In serial interface 4 in IIC mode, this pin is configured as the clock I/ O pin. For the output configuration, select Nch open-drain in P0ODC register and set pull-up resistor by P0PLU register. Select the output mode at P0DIR register and select serial clock I/O mode in serial mode register 1 (SC4MD1). These can be used as normal I/O pin when serial interface is not used.
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM1IOC TM2IOA TM2IOB TM2IOC	44 20 34 1 19 35 32 18 36	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 2. To use this pin as event clock input, configure it as input by P0DIR register, P3DIR register, P4DIR register and PADIR register. In the input mode, pull-up resistor can be selected in P0PLU, P3PLU, P4PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD, P3OMD, P4OMD and PAOMD registers, and set to the output mode in P0DIR, P3DIR, P4DIR and PADIR registers. These can be used as normal I/O pins when Timer I/O pin is not used.
BUZZER NBUZZER	29 30	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to Port 3. The driving frequency can be set in DLYCTR register. In order to select Buzzer output to Port 3, select the special function pin in P3OMD register, and set P3DIR register to the output mode. At the same time, select Buzzer output in oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when Buzzer output is not used.
TM7IOA TM7IOB TM7IOC TM9IOA TM9IOC	2 17 37 16 38	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 9. To use this pin as event clock input, configure it as input with P0DIR, P4DIR and PADIR registers. In the input mode, pull-up resistor can be selected by P0PLU, P4PLU and PAPLU registers. For timer output, PWM signal output, select the special function pin in P0OMD, P4OMD and PAOMD registers, and set to the output mode in P0DIR, P4DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	16 17 18 19 20 21	Output	Timer PWM output	PWM signal output pin for 16-bit timer 9. Select the special function pin in P0OMD register, and set to the output mode in P0DIR register. These can be used as normal I/O pins when not used as timer I/O pins.
VREF+	4	-	A/D reference voltage input pin	Reference power supply pin for A/D converter. Normally, the values of VREF+ = VDD5 is used.

Pins	Pin No	I/O	Function	Description
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	40 41 42 43 44 1 2 3 39 38 37 36	Input	Analog input pins	Analog input pins for 12-channel, 10-bit A/D converter. Select the analog input by PAIMD register. When not used for analog input, these pins can be used as normal input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4A IRQ4B	24 25 26 27 28 40	Input	External interrupt	External interrupt input pins. Select the external interrupt input enable by IRQCNT register. The valid edge for IRQ0 to 4 can be selected with IRQnICR register. IRQ2 to 4 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	40 41 42 43 44 1 2 3	Input	Key interrupt input pins	Input pins for KEY interrupt based on OR condition result of pin inputs. These can be set to key input pins by 1-bit with KEY interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7 LED8 LED9 LED10 LED11 LED12 LED13 LED14 LED15	16 17 18 19 20 21 22 23 40 41 42 43 44 1 2 3	Output	LED drive pins	Large current output pins. Select the large current output by P0LED and PALED registers. When not used for LED output, these pins can be used as normal I/O pins
DMOD	8	Input	Mode switch input pins	Set always to VDD5.
MMOD	14	Input	ROM area switch input pins at start	Set always to VSS.

For the MMOD setup in rewriting the flash memory, refer to Technical Reference Manual.

4 Block Diagram

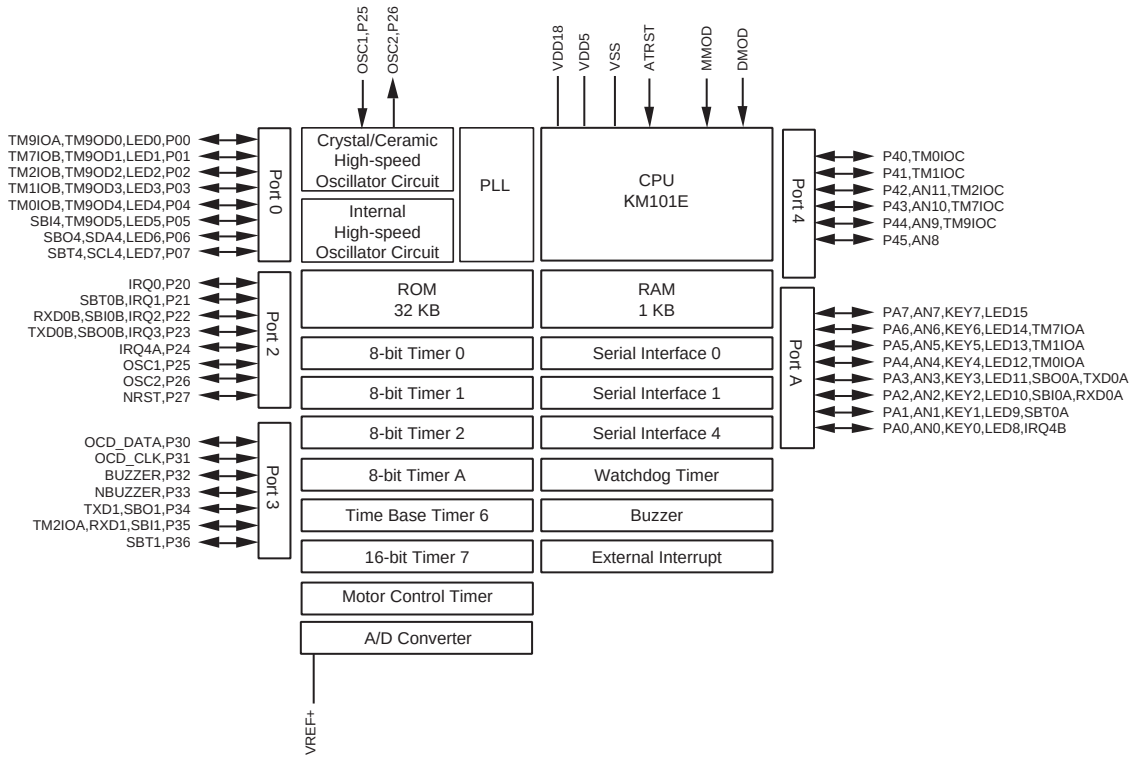

Figure: 4.1 Block Diagram

5 Electrical Characteristics

This datasheet describes standard specifications.

When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcontroller

5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4 V_{SS} = 0 V

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
A2	Power supply voltage		V_{DD18}	-0.3 to +2.5	
A3	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3 (upper limit: 7.0)	
A4	Output pin voltage		V_O	-0.3 to V_{DD5} +0.3 (upper limit: 7.0)	
A5	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3 (upper limit: 7.0)	
A6	Peak output current	LED output	I_{OL1} (peak)	30	mA
A7		Other than LED output	I_{OL2} (peak)	20	
A8		All pins	I_{OH} (peak)	-10	
A9	Average output current *1	LED output	I_{OL1} (avg)	20	
A10		Other than LED output	I_{OL2} (avg)	15	
A11		All pins	I_{OH} (avg)	-5	
A12	Power dissipation		P_{D2}	400	mW
A13	Operating ambient temperature		T_{opr}	-40 to +85	°C
A14	Storage temperature		T_{STG}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 0.1 μF + 1.0 μF or larger between VDD5 pin and GND for the internal power voltage stabilization.

*3 Connect appropriate capacitor about 0.1 μF + 1.0 μF between VDD18 pin and VSS pin, near the microcontroller according to the Figure: 5.1 shown below for the internal power supply stabilization.

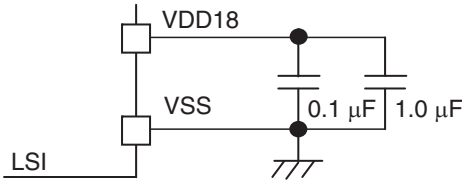

Figure: 5.1 Capacitor Connection between VDD18 and VSS Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

5.2 Operating Conditions

V_{SS} = 0 V

B. Operating Conditions — Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
Power supply voltage *5							
B1	Power supply voltage	V_{DD1}	fs ≤ 20 MHz	4.0		5.5	V
B2	RAM retention power supply voltage	V_{DD8}	During STOP mode	2.2		5.5	
Operating speed *6							
B3	Instruction execution time fs	t_{c1}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is “1”.)	0.05			µs
B4		t_{c2}	V_{DD5} = 4.0 V to 5.5 V (When ROMHND of HANDSHAKE register is “0”.)	0.10			

*5 fs: Machine clock frequency

*6 tc1 to 2: when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.

External Oscillator Figure: 5.2

B5	Frequency	f_{hosc1}	V_{DD5} is within the specified operating power supply voltage range. (Refer to the ratings of B1 to B2 for the operating supply voltage range)	2.0		10	MHz
B6	Internal feedback resistor	R_{f10}	V_{DD5} = 5.0 V		980		kΩ

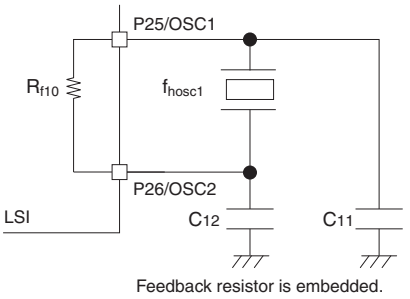

Figure: 5.2 External Oscillator

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD5} = 4.0 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B7	Clock frequency	f_{hosc2}		2		10.0	MHz
B8	High-level pulse width *7	t_{wh1}	Figure: 5.3	45			ns
B9	Low-level pulse width *7	t_{wl1}		45			
B10	Rising time	t_{wr1}	Figure: 5.3	0		5.0	
B11	Falling time	t_{wf1}		0		5.0	

*7 The clock duty ratio should be 45 % to 55 %

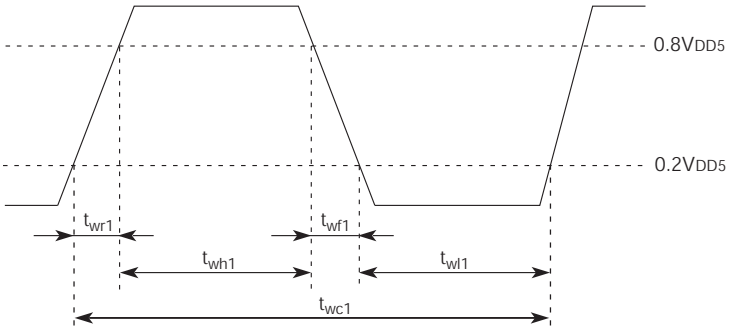

Figure: 5.3 OSC1 Timing Chart

5.3 DC Characteristics

V_{SS} = 0 V

C. DC Characteristics

Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply current *8							
C1	Power supply current during operation	I_{DD1}	fosc=10 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (PLL is not used) *9		5	14	mA
C2		I_{DD2}	fosc=10 MHz [Multiplied by 2, Divided by 2: fs=fosc] V_{DD5}=5 V (PLL is used) *9		6	18	
C3		I_{DD3}	fosc=10 MHz [Multiplied by 2: fs=20 MHz] V_{DD5}=5 V (PLL is used) *9		9	20	
C4		I_{DD4}	frc=16 MHz [Double-speed mode: fs=16 MHz] V_{DD5}=5 V (PLL is used) *9		6	15	
C5	Power supply current during STOP mode	I_{DD5}	V_{DD5}=5 V Ta = -40 °C to +85 °C		145	245	μA

*8 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current during operation I_{DD1} to I_{DD4};
1. Set all I/O pins to input mode,
2. Set the CPU mode to “NORMAL mode”,
3. Fix pin MMOD to V_{SS} level and input pins to V_{DD5} level
4. Input the rectangular wave of 10 MHz(4 MHz) with amplitude of V_{DD5} and V_{SS}, from pin OSC1.

To measure the power supply current during STOP mode I_{DD5};
1. Set the CPU mode to “STOP mode”,
2. Fix pin MMOD to V_{SS} level and input pin to V_{DD5} level
3. Open pin OSC1.

*9 When ROMHND of HANDSHAKE register is set to “1”

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Input pin 1 ATRST, MMOD							
C10	Input high voltage	V_{IH1}		0.8 V_{DD5}		V_{DD5}	V
C11	Input low voltage	V_{IL1}		0		0.2 V_{DD5}	
C12	Input leakage current	I_{LK1}	V_{IN} = 0 V to V_{DD5}			± 2	μA
Input pin 2 P27/NRST							
C13	Input high voltage	V_{IH2}		0.8 V_{DD5}		V_{DD5}	V
C14	Input low voltage	V_{IL2}		0		0.15 V_{DD5}	
C15	Pull-up resistor	R_{RH1}	V_{DD5}=5 V, V_{IN}= V_{SS}	10	50	100	kΩ
I/O pin 3 P00 to P07							
C16	Input high voltage 2	V_{IH3}		0.54 V_{DD5}		V_{DD5}	V
C17	Input low voltage	V_{IL3}		0		0.2 V_{DD5}	
C18	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD5}			± 2	μA
C19	Pull-up resistor	R_{RH2}	V_{DD5}=5 V, V_{IN}= V_{SS} Pull-up resistor ON	10	50	100	kΩ
C20	Output high voltage	V_{OH1}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C21	Output low voltage 1	V_{OL1}	V_{DD5}=5.0 V, I_{OL}=1.0 mA LED output OFF			0.5	
C22	Output low voltage 2	V_{OL2}	V_{DD5}=5.0 V, I_{OL}=15.0 mA LED output ON			1.0	
I/O pin 4 P20, P21							
C23	Input high voltage 2	V_{IH4}		0.54 V_{DD5}		V_{DD5}	V
C24	Input low voltage	V_{IL4}		0		0.2 V_{DD5}	
C25	Input leakage current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	μA
C26	Pull-up resistor	R_{RH3}	V_{DD5}=5 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C27	Output high voltage	V_{OH2}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C28	Output low voltage	V_{OL3}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 5 P22 to P24, P25 to P26 *10 P30 to P31, P32 to P36							
C29	Input high voltage	V_{IH5}		0.8 V_{DD5}		V_{DD5}	V
C30	Input low voltage	V_{IL5}		0		0.2 V_{DD5}	
C31	Input leakage current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	µA
C32	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C33	Output high voltage	V_{OH3}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C34	Output low voltage	V_{OL4}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	
I/O pin 6 PA0 to PA7							
C35	Input high voltage	V_{IH6}		0.8 V_{DD5}		V_{DD5}	V
C36	Input low voltage	V_{IL6}		0		0.2 V_{DD5}	
C37	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD5}			± 2	µA
C38	Pull-up resistor	R_{RH5}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C39	Output high voltage	V_{OH4}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C40	Output low voltage 1	V_{OL5}	V_{DD5}=5.0 V, I_{OL}=1.0 mA LED output OFF			0.5	
C41	Output low voltage 2	V_{OL6}	V_{DD5}=5.0 V, I_{OL}=15.0 mA LED output ON			1.0	
I/O pin 7 P40 to P45							
C42	Input high voltage	V_{IH7}		0.8 V_{DD5}		V_{DD5}	V
C43	Input low voltage	V_{IL7}		0		0.2 V_{DD5}	
C44	Input leakage current	I_{LK5}	V_{IN}=0 V to V_{DD5}			± 2	µA
C45	Pull-up resistor	R_{RH6}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
C46	Pull-down resistor	R_{RL1}	V_{DD5}=5.0 V, V_{IN}=V_{DD5} Pull-down resistor ON	10	50	100	
C47	Output high voltage	V_{OH5}	V_{DD5}=5.0 V, I_{OH}=-0.5 mA	4.5			V
C48	Output low voltage	V_{OL7}	V_{DD5}=5.0 V, I_{OL}=1.0 mA			0.5	
Input pin 8 DMOD *11							
C49	Input high voltage	V_{IH8}		0.8 V_{DD5}		V_{DD5}	V
C50	Input low voltage	V_{IL8}		0		0.2 V_{DD5}	
C51	Pull-up resistor	R_{RH8}	V_{DD5}=5.0 V, V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ

*10 These are not used for oscillation pins.

*11 Only flash EEPROM version, DMOD pin contains an internal pull-up resistor.
When using In-Circuit Emulator, connect pull-up resistor to DMOD on the target board.

5.4 A/D Converter Characteristics

V_{DD5} = 5.0 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

D. A/D Converter Characteristics *12

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
D1	Resolution					10	Bits
D2	Non-linearity error 1		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns			± 3	LSB
D3	Differential non-linearity error 1					± 3	
D4	Zero transition voltage		V_{DD5}=5.0 V, V_{SS}=0 V V_{REF+}=5.0 V T_{AD}=800 ns		10	30	mV
D5	Full-scale transition voltage			4970	4990		
D6	A/D conversion time		T_{AD}=800 ns	12.93			µs
D7	Sampling time		T_{AD}=800 ns	1.6			
D8	Reference voltage	V_{REF+}	V_{REF+}= V_{DD5}	4.0		V_{DD5}	V
D9	Analog input voltage			V_{SS}		V_{REF+}	
D10	Analog input leakage current		Channel OFF V_{ADIN}=V_{SS} to V_{DD5}			± 2	µA
D11	Reference voltage pin input leakage current		Ladder resistance OFF V_{SS} ≤ V_{REF+} ≤ V_{DD5}			± 5	
D12	Ladder resistance	R_{LADD}	V_{DD5}=5.0 V	15	40	80	kΩ

*12 T_{AD} is A/D conversion clock cycle.
The specification values of D2 to D5 are guaranteed on the condition of V_{DD5}=V_{REF+}=5 V, V_{SS}=0 V.

Even if A/D function is not used, V_{REF+} must be set between V_{DD5} and 4.0 V.

5.5 Auto Reset Characteristics

V_{DD5} = V_{RST} to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

E. Auto Reset Characteristics

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
E1	Operating supply voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
E2	Power detection level	V_{RST1}	At rising	4.10	4.30	4.50	V
E3	Power detection level	V_{RST2}	At falling	4.00	4.20	4.40	
E4	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V

5.6 Internal High-speed Oscillation Circuit

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V

F. Internal High-speed Oscillation Circuit

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Internal high-speed oscillation circuit frequency	f_{rc}	Ta = -40 °C to +85 °C		16		MHz
F2	Temperature dependence of oscillation frequency *13	f_{rc3}	Ta = 25 °C	-5.0		5.0	%
		f_{rc4}	Ta = -40 °C to +85 °C				

*13 The specification values described in G are for standard application.
For special application (such as for automotive product) has different value.
When using this LSI, consult our sales offices for the product specifications.

5.7 Flash EEPROM Program Conditions

V_{DD5} = 4.0 V to 5.5 V V_{SS} = 0 V
Ta = -40 °C to +85 °C

G. Flash EEPROM Program Conditions *14

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
G1	Voltage for rewriting	V_{DDEW}		4.0		5.0	V
G1	Programming guarantee number of times	E_{MAX}				1000	Time
G2	Data retention period	T_{HOLD}		20			Year

*14 The specification values described in G are for standard application.
For special application (such as for automotive product) has different value.
When using this LSI, consult our sales offices for the product specifications.

6 Package Dimension

■ QFP 44-pin (10 mm × 10 mm / 0.8 mm pitch)

Unit: mm

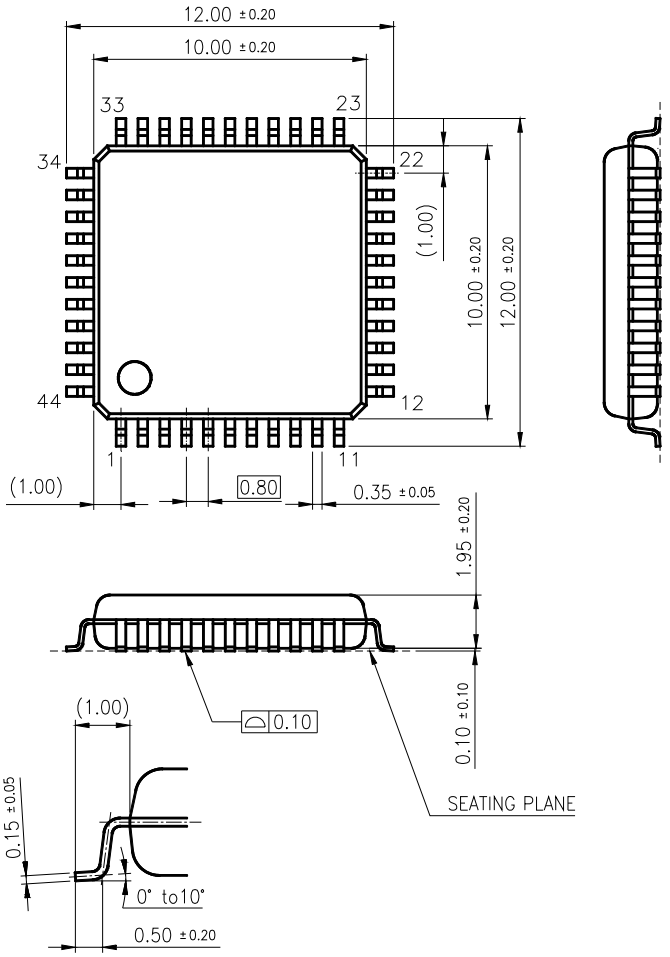

Figure: 6.1 QFP 44-pin Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

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