8-bit Microcontroller

KM101EF59R
Datasheet

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1. Overview

1.1 Overview

The KM101E series of 8-bit single-chip microcontrollers incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcontroller applications flexible, optimized hardware configurations and a simple efficient instruction set. The KM101EF59R has an internal 928 KB (maximum) of ROM and 8 KB (maximum) of RAM. Peripheral functions include 6 external interrupts, 30 internal interrupts including NMI, 9 timer counters, 6 sets of serial interfaces, A/D converter, D/A converter,

LCD driver, watchdog timer, 2 sets of automatic data transfer, synchronous output function and buzzer output. The configuration of this microcontroller is well suited for application as a system controller in camera, timer selector for VCR, CD player, or minicomponent, and also suited for audio reproduction with a high-precision D/A converter.

With three oscillation system (high frequency: max. 20 MHz / low frequency: 32.768 kHz and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high frequency input (high speed mode), PLL input (PLL mode), or to low frequency input (low speed mode). The system clock is generated by dividing the oscillation clock. The best operation clock for the system can be selected by switching its frequency by software. High speed mode has the normal mode based on fpll/2 which is half clock generated from an original oscillation and PLL, and the double speed mode based on fpll which is clock generated from an original oscillation without dividing.

A machine cycle (min. instructions execution) in the normal mode is 100 ns when fosc is 20 MHz (at the time that PLL is not used). A machine cycle in the double speed mode is 50 ns when fosc is 20 MHz. A machine cycle in the PLL mode is 50 ns (maximum).The package is 100-pinQFP.

1.2 Product Summary

This datasheet describes the following models of the KM101EF59R.

Table: 1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EF59R	928 KB	8 KB	Flash EEPROM version	QFP 100-pin

2. Hardware Functions

- ROM Capacity 928 KB
- RAM Capacity 8 KB
- Package QFP 100-pin (18 mm x 18 mm, 0.65 mm pitch)
- Machine Cycle High speed mode
  PLL mode
  Low speed mode
- Clock Gear Operation speed of system clock is variable by changing the frequency
- Multiplied Clock High-speed frequency clock (fosc) can be multiplied by 2, 3, 4, 5, 6, 8 and 10.
- Memory bank Data memory space is expanded by the bank system.
  Bank for the source address/Bank for the destination address.
- ROM correction Correcting address designation: up to 7 addresses possible
- Operation Modes NORMAL mode (High speed mode)
  PLL mode
  SLOW mode (Low speed mode)
  HALT mode
  STOP mode
  (The operation clock can be switched in each mode.)
- Operating Voltage 2.2 V to 5.5 V
- Operating Temperature
  -40°C to +85°C

- Interrupt 36 levels

<Watchdog timer>
NMI-Watchdog timer overflow
<Timer interrupts>
TM0IRQ-Timer 0 interrupt (8-bit timer)
TM1IRQ-Timer 1 interrupt (8-bit timer)
TM2IRQ-Timer 2 interrupt (8-bit timer)
TM3IRQ-Timer 3 interrupt (8-bit timer)
TM4IRQ-Timer 4 interrupt (8-bit timer)
TM6IRQ-Timer 6 interrupt (8-bit timer)
TBIRQ-Clock timer interrupt
TM7IRQ-Timer 7 interrupt (16-bit timer)
T7OC2IRQTimer 7 interrupt (16-bit timer)
TM8IRQ-Timer 8 interrupt (16-bit timer)
T8OC2IRQTimer 8 interrupt (16-bit timer)
TM9IRQ-Timer 9 interrupt (16-bit timer)
T9OC2IRQTimer 9 interrupt (16-bit timer)
<Serial interrupts>
SC0TIRQ-Serial interface 0 interrupt
SC0RIRQ-Serial interface 0 UART reception interrupt (peripheral function group interrupt)
SC1TIRQ-Serial interface 1 interrupt
SC1RIRQ-Serial interface 1 UART reception interrupt (peripheral function group interrupt)
SC2TIRQ-Serial interface 2 interrupt
SC2RIRQ-Serial interface 2 UART reception interrupt
SC3TIRQ-Serial interface 3 interrupt
SC3RIRQ-Serial interface 3 UART reception interrupt (peripheral function group interrupt)
SC4TIRQSerial interface 4 interrupt
SC4SIRQSerial interface 4 stop condition interrupt (peripheral function group interrupt)
SC5TIRQSerial interface 5 interrupt (peripheral function group interrupt)
<A/D conversion end>
ADIRQ-AD conversion end (peripheral function group interrupt)
<Automatic Transfer Controller interrupts>
ATC0IRQ-ATC0 interrupt (peripheral function group interrupt)
ATC1IRQ-ATC1 interrupt (peripheral function group interrupt)
<External interrupts> Edge selectable
IRQ0:External interrupt (AC zero-cross detector, With/Without noise filter)
IRQ1:External interrupt (AC zero-cross detector, With/Without noise filter)
IRQ2:External interrupt (Both edges interrupt)
IRQ3:External interrupt (Both edges interrupt)
IRQ4:External interrupt (Both edges interrupt)
IRQ5:External interrupt (Key scan interrupt only)
<Audio interrupts>
Audio reproduction end interrupt
Audio phrase end interrupt

• Timer Counter

11 timers All timer counters generate interrupt (10 can be operated independently)
- 8-bit timer for general use: 5 sets
- 8-bit free-running timer: 1 set
- Time base timer: 1 set
- 16-bit timer for general use: 3 sets
- Simple 8-bit timer: 1 set

Timer 0 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM0IOB), event count, remote control carrier output, simple pulse with measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 1 (8-bit timer for general use)
- Square wave output (timer pulse output), event count, 16-bit cascade connected (timer0, 1) timer synchronous output event
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 2 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output (can be output to large current pin TM2IOB), event count, simple pulse with measurement, 24-bit cascade connected (timer0, 1) timer synchronous output event
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 3 (8-bit timer for general use)
- Square wave output (timer pulse output), event count, remote control carrier output, 16bit cascade connected (timer2), 32-bit cascade connected (timer0, 1, 2)
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 4 (8-bit timer for general use)
- Square wave output (timer pulse output), added pulse(2-bit) system PWM output, event count, serial transfer clock, simple pulse measurement
- Clock source
  fpll, fpll/4, fpll/16, fpll/32, fpll/64, fpll/128, fs/2, fs/4, fs/8, fx, external clock, TimerA output

Timer 6 (8-bit free-running timer, Time base timer)
8-bit free-running timer
- Clock source
  fpll, fpll/2^{12}, fpll/2^{13}, fs, fx, fx/2^{12}, fx/2^{13} Time base timer
- Interrupt generation cycle
  fpll/2^{7}, fpll/2^{8}, fpll/2^{9}, fpll/2^{10}, fpll/2^{13}, fpll/2^{15},
  fx/2^{7}, fx/2^{8}, fx/2^{9}, fx/2^{10}, fx/2^{13}, fx/2^{15}

- Timer Counter (continued)

Timer 7 (16-bit timer for general use)
- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output
- Hardware organization
  Compare register with double buffer: 2 sets
  Input capture register: 1 set
  Timer interrupt: 2 vectors
- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable), IGBT output (Cycle/Duty continuous changeable) can be output to large current pin TM7IOB
  Timer synchronous output, event count, Input capture function (Both edges can be operated)
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

Timer 8 (16-bit timer for general use)
- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16
  1/1, 1/2, 1/4, 1/16 of the external clock, TimerA output
- Hardware organization
  Compare register with double buffer: 2 sets Input capture register: 1 set
  Timer interrupt: 2 vectors
- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture (Both edge available), 32-bit cascade connected (Timer7, 8), 32-bit PWM output, Input capture is available at 32-bit cascade

Timer 9 (16-bit timer for general use)
- Clock source
  fpll, fpll/2, fpll/4, fpll/16, fs, fs/2, fs/4, fs/16, 1/1, 1/2, 1/4, 1/16 of the external clock TimerA output
- Hardware organization
  Compare register with double buffer: 2 sets Input capture register: 1 set
  Timer interrupt: 2 vectors
- Timer functions
  Square wave output (Timer pulse output), High precision PWM output (Cycle/Duty continuous changeable) can be output to large current pin TM9IOB, event count, pulse width measurement, input capture (Both edge available)
- Real timer output control
  Control the timer (PWM) output by the falling edge of external interrupt 0 (IRQ0) with the follow 3 value; “High”-fixed, “LOW”-fixed and “Hi-Z”-fixed

TimerA output (Simple timer counter A)
Clock output for peripheral function

- Watchdog timer — Time-out cycle can be selected from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
  On detection of errors, hard reset is done inside LSI
- Synchronous output function

  Timer synchronous output, interrupt synchronous output Port 8 outputs the latched data, on the event timing of the synchronous output signal of timer 1, 2, or 7, or of the external interrupt 2 (IRQ2).
- Buzzer Output/Reverse Buzzer Output

  Output frequency can be selected from $fpll/2^9$, $fpll/2^{10}$, $fpll/2^{11}$, $fpll/2^{12}$, $fpll/2^{13}$, $fpll/2^{14}$, $fx/2^3$, $fx/2^4$
- Remote Control Carrier Output:

  A remote control carrier output with duty cycle of 1/2 or 1/3 of timer 0 or timer 3 output are available.
- A/D Converter — 10-bit x 12 channels
- D/A Converter — 8-bit x 4 channels
- Data automatic transfer

  2 systems

  ATC0
  Data is transferred automatically in all memory space
  - External request/internal event request/software request
  - Maximum transfer cycles are 255
  - Support continuous serial transmission / reception.
  - Burst transfer function (Urgent stop of interrupts is contained.)

  ATC1
  Data is transferred automatically in all memory space
  - External request/internal event request/software request
  - Maximum transfer cycles are 255
  - Support continuous serial transmission / reception.
  - Burst transfer function (Urgent stop of interrupts is contained.)
- Serial Interface — 6 channels

  Serial 0 (Full duplex UART / Synchronous serial interface)
  Synchronous serial interface
  - Transfer clock source
    fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
  - MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
  - Sequence transmission, reception or both are available.

  Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
  - Parity check, Overrun error / Framing error detection
  - Transfer size 7 to 8 bits can be selected.

  Serial 1 (Full duplex UART / Synchronous serial interface)
  Synchronous serial interface
  - Transfer clock source
    fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
  - MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
  - Sequence transmission, reception or both are available.

  Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
  - Parity check, Overrun error / Framing error detection
  - Transfer size 7 to 8 bits can be selected.

- Serial Interface (continued)

Serial 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 3 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/16, fpll/64, fs/2, fs/4, Timer0,1,2,3,4 and A output ,external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Full duplex UART (Baud rate timer, Timer0,1,2,3,4 and A)
- Parity check, Overrun error / Framing error detection
- Transfer size 7 to 8 bits can be selected.

Serial 4 (multi master I2C / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll/2, fpll/4, fpll/8, fpll/32, fs/2, fs/4, Timer0,1,2,3,4 and A output, external clock
- MSB/LSB can be selected as the first bit to be transferred. An arbitrate transfer size from 1 to 8 bits can be selected.
- Sequence transmission, reception or both are available.

Multi master I2C
- 7-bit of slave address can be set.
- General call communication mode handling

Serial 5
- IIC slave interface
- IIC high-speed transfer mode (communication speed: 400 kbps)
- 7-bit or 10-bit of slave address can be set.
- General call communication mode handling

- LED Driver

8 pins (Push-pull structure)

- Automatic Reset

- LCD Driver

LCD driver pins
- Segment output max. 55 pins (SEG0 to 54)
  - SEG0 to 54 can be switched to I/O ports by 1 pin
  - [Note: At reset, SEG0 to 54 are input ports.]
- Common output pins:4 pins
  - COM0 to 3 can be switched to I/O ports by 1 pin
- Display mode selection
  - Static
  - 1/2 duty, 1/2 bias
  - 1/3 duty, 1/3 bias
  - 1/4 duty, 1/3 bias
- LCD driver clock
  - When the source clock is the main clock (fpll)
    $1/2^{18}$, $1/2^{17}$, $1/2^{16}$, $1/2^{15}$, $1/2^{14}$, $1/2^{13}$, $1/2^{12}$, $1/2^{11}$
  - When the source clock is the sub clock (fx)
    $1/2^{9,}$ $1/2^{8}$, $1/2^{7}$, $1/2^{6}$
  - Timer0, 1, 2, 3, 4 and A output
- LCD power supply
  - Use at $V_{DD5} \geq V_{LC1}$
  - External supply voltage is input from V_{LC1}, V_{LC2}, V_{LC3} pins or voltage applied to V_{LC1} is divided by internal resistance and supplied to V_{LC2} and V_{LC3} pins

- DAC for audio reproduction

Analog DAC input
PWM digital output
Continuous reproduction function
Repeat function (phrase repeat)
Volume control (2048 tone)
Sampling frequency: 8 to 44.1 kHz

- Port

I/O ports	: 85 pins
LED (large current) driver pins	: 8 pins
LCD driver for segment	: 55 pins
LCD driver for common	: 4 pins
serial interface pin	: 34 pins
Timer I/O	: 28 pins
Buzzer output	: 4 pins
A/D input	: 12 pins
External interrupt pin	: 5 pins
LCD power	: 3 pins
XI/XO	: 2 pins
D/A output	: 4 pins
Audio output	: 2 pins
Special pins	: 10 pins
Operation mode input pins	: 3 pin
Analog reference voltage input pins :	: 1 pin
Reset input pin	: 1 pin
Oscillation pins	: 2 pins
Power pins	: 6 pins

3. Pin Description

3.1 Pin configuration

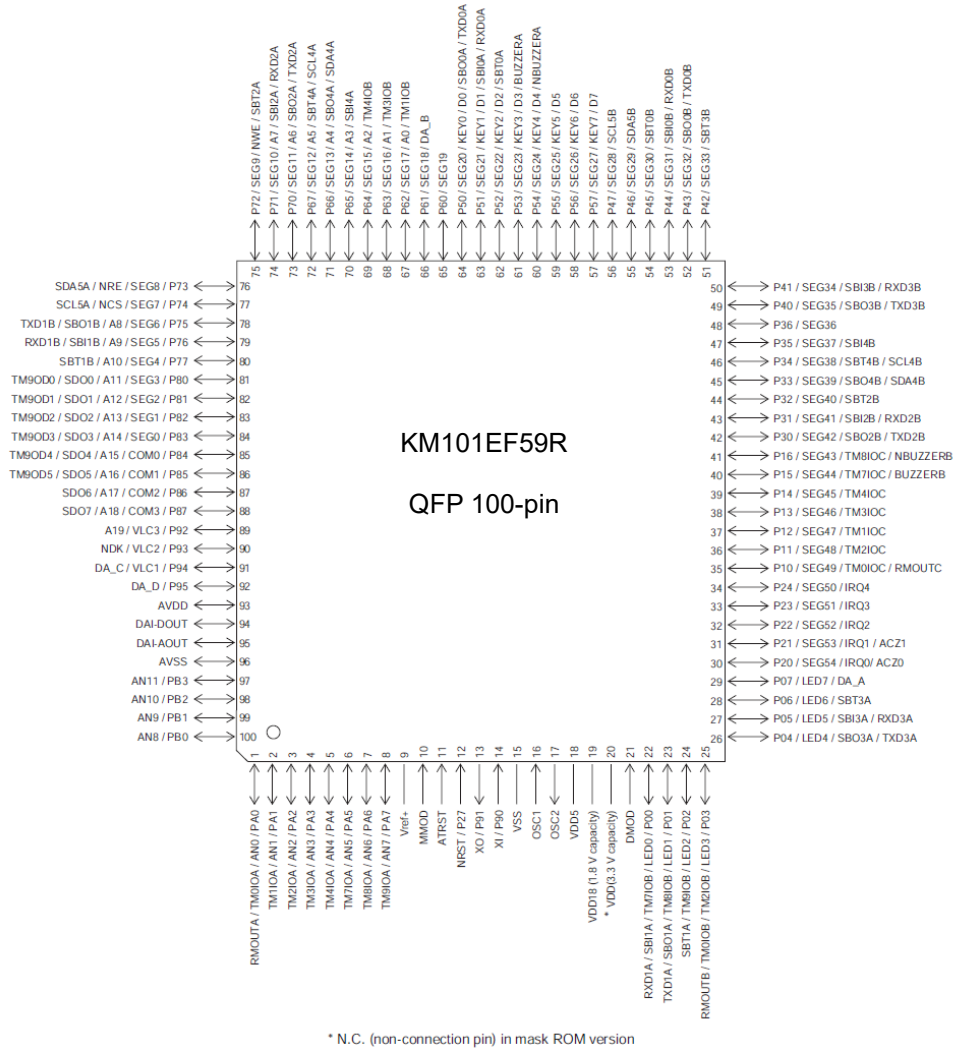


Figure: 3.1 Pin Configuration

3.2 Pin Functions

Table: 3.1 Pin Functions

Name	Pin No	I/O	Function	Description
VSS VDD5 AVDD AVSS	15 18 93 96	-	Power connect pins	Supply 2.2 V to 5.5 V to VDD5, 5.0 V to AVDD and 0 V to VSS and AVSS.
VDD18 (Capacity 1.8 V)	19	-	Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 μF or larger between VDD18 and VSS.
VDD (Capacity 3.3 V)	20	-	Capacity connect pins	For internal power circuit output stability, connect at least one bypass capacitor of 1 μF or larger between VDD and VSS. (Only Flash version)
OSC1 OSC2	16 17	Input Output	Clock input pins Clock output pins	Connect these oscillation pins to ceramic or crystal oscillators for high-frequency clock operation. If the clock is an external input, connect it to OSC1 and leave OSC2 open. The chip will not operate with an external clock when using either the STOP or SLOW modes.
XI XO	14 13	Input Output	Clock input pins Clock output pins	Connect these oscillation pins to crystal oscillators for low-frequency clock operation. If the clock is an external input, connect it to XI and leave XO open. the chip will not operate with an external clock when using the STOP mode. If these pins are not used, connect XI to VSS and leave XO open.
NRST	12	Input	Reset pin [Active low]	This pin resets the chip when power is turned on, is allocated as P27 and contains an internal pull-up resistor (Type. 50 kΩ). Setting this pin low initialize the internal state of the device. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an n-channel open-drain configuration. If a capacitor is to be inserted between NRST and VSS, it is recommended that a discharge diode be placed between NRST and VDD5.
ATRST	11	Input	Auto reset setting pins 2	Input “H” to enable auto reset function and “L” to disable this function
P00 P01 P02 P03 P04 P05 P06 P07	22 23 24 25 26 27 28 29	I/O	I/O port0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) Direct LED drive available at output. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).

Name	Pin No	I/O	Function	Description
P10 P11 P12 P13 P14 P15 P16	35 36 37 38 39 40 41	I/O	I/O port1	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pull-up/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24	30 31 32 33 34	I/O	I/O port2	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P2PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P27	12	Input	Input port2	Port P27 has an N-channel open-drain configuration. When “0” is written and the reset is initiated by software, a low level will be output.
P30 P31 P32 P33 P34 P35 P36	42 43 44 45 46 47 48	I/O	I/O port3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P3PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P40 P41 P42 P43 P44 P45 P46 P47	49 50 51 52 53 54 55 56	I/O	I/O port4	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. A pullup/pull down can not be mixed. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P50 P51 P52 P53 P54 P55 P56 P57	64 63 62 61 60 59 58 57	I/O	I/O port5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)

Name	Pin No	I/O	Function	Description
P60 P61 P62 P63 P64 P65 P66 P67	65 66 67 68 69 70 71 72	I/O	I/O port6	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P6PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P70 P71 P72 P73 P74 P75 P76 P77	73 74 75 76 77 78 79 80	I/O	I/O port7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P80 P81 P82 P83 P84 P85 P86 P87	81 82 83 84 85 86 87 88	I/O	I/O port8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
P90 P91 P92 P93 P94 P95	14 13 89 90 91 92	I/O	I/O port9	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P8PLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	1 2 3 4 5 6 7 8	I/O	I/O portA	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
PB0 PB1 PB2 PB3	100 99 98 97	I/O	I/O portB	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up resistor for each bit can be selected individually by the PBPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance)
DA1_DOUT DA1_AOUT	94 95	I/O	Audio output pins	Special output pins for audio production function These output “L” at reset.

Name	Pin No	I/O	Function	Description
SBO0A SBO0B SBO1A SBO1B SBO2A SBO2B SBO3A SBO3B SBO4A SBO4B	64 52 23 78 73 42 26 49 71 45	I/O	Serial interface transmission data output pins	Transmission data output pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1A SBI1B SBI2A SBI2B SBI3A SBI3B SBI4A SBI4B	63 53 22 79 74 43 27 50 70 47	Input	Serial interface reception data input pins	Reception data output pins for serial interface 0 to 4. A pull-up resistor can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1A SBT1B SBT2A SBT2B SBT3A SBT3B SBT4A SBT4B	62 54 24 80 75 44 28 51 72 46	I/O	Serial interface clock I/O pins	Clock I/O pins for serial interface 0 to 4. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD, P6PLUD and P7PLUD registers. Select the clock I/O with the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC4MD1) according to the communication. These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1A TXD1B TXD2A TXD2B TXD3A TXD3B	64 52 23 78 73 42 26 49	Output	UART transmission data output pins	In the serial interface0 to 3 in UART mode, this pin is configured as the transmission data output pin. The output configuration, either CMOS push-pull or n-channel open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0A RXD0B RXD1A RXD1B RXD2A RXD2B RXD3A RXD3B	63 53 22 79 74 43 27 50	Input	UART reception data input pins	In the serial interface0 to 3 in UART mode, this pin is configured as the reception data output pin. Pull-up resistor can be selected by the P0PLUD, P3PLUD, P4PLUD, P5PLUD and P7PLUD registers. Select the output mode at the P0DIR, P3DIR, P4DIR, P5DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1 to SC3MD1). These can be used as normal I/O pins when the serial interface is not used.

Name	Pin No	I/O	Function	Description
SDA4A SDA4B SDA5A SDA5B	71 45 76 55	I/O	IIC data I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the data input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data input / output mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4A SCL4B SCL5A SCL5B	72 46 77 56	I/O	IIC clock I/O pins	In the serial interface4, 5 in IIC mode, this pin is configured as the clock input / output pin. For the output configuration, select n-channel open-drain with the P3ODC, P4ODC, P6ODC and P7ODC registers and pull-up resistors by the P3PLUD, P4PLUD, P6PLUD and P7PLUD registers. Select the output mode at the P3DIR, P4DIR, P6DIR and P7DIR registers and serial data input / output mode by serial mode register 1 (SC4MD1, SC5MD1). These can be used as normal I/O pins when the serial interface is not used
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM1IOC TM2IOA TM2IOB TM2IOC TM3IOA TM3IOB TM3IOC TM4IOA TM4IOB TM4IOC	1 25 35 2 67 37 3 25 36 4 68 38 5 69 39	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 8-bit timer 0 to 4. To use this pin as event clock input, configure this as input by P0DIR register, P1DIR register, P6DIR register and PADIR register. In the input mode, pull-up resistors can be selected by the P0PLUD register, P1PLUD register, P6PLUD register and PAPLU register. For timer output, PWM signal output, select the special function pin by port 0 output mode register, port 1 output mode register, port 6 output mode register and port A output mode register ((P0OMD, P1OMD, P6OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register. These can be used as normal I/O pins when the timer I/O is not used.
RMOUTA RMOUTB RMOUTC	1 25 35	I/O	Remote control transmission signal output pins	Output pin for remote control transmission with a carrier signal. For remote control carrier output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode by the P0DIR register, P1DIR register and PADIR register. At the same time, select remote control carrier output by the remote control carrier output register. These can be used as normal I/O pins when the buzzer output is not used.
BUZZERA BUZZERB NBUZZERA NBUZZERB	61 40 60 41	I/O	Buzzer output	Piezoelectric buzzer driving pin. Buzzer output available to port1, port5. The driving frequency can be selected with the DLYCTR register. To select buzzer output for porrt1, port5, select the special function pin by the port 1 output mode register and port 5 output mode register (P1OMD and P5OMD), and set to the output mode by the P1DIR register and P5DIR register. At the same time, select buzzer output by the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the buzzer output is not used.

Name	Pin No	I/O	Function	Description
TM7IOA TM7IOB TM7IOC TM8IOA TM8IOB TM8IOC TM9IOA TM9IOB	6 22 40 7 23 41 8 24	I/O	Timer I/O pins	Event counter clock input pin, timer output and PWM signal output pin for 16-bit timer7 and 8. To use this pin as event clock input, configure this as input with the PADIR register. In the input mode, pull-up resistors can be selected by P0PLU register, P1PLU register and PAPLU register. For timer output, PWM signal output, select the special function pin by the port 0 output mode register, port 1 output mode register and port A output mode register (P0OMD, P1OMD and PAOMD), and set to the output mode at P0DIR register, P1DIR register and PADIR register. These can be used as normal I/O pins when not used
TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	81 82 83 84 85 86	Output	Timer output pins	Timer output and PWM signal output pin for 16-bit timer. To select timer output and PWM signal output, select the special function pin by the P8PLU register, and set to the output mode at the P8DIR register. These can be used as normal I/O pins when not used as timer I/O pins.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	81 82 83 84 85 86 87 88	Output	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). Set to the output mode by the P8DIR register. These pins can be used as a normal I/O pins when not used for synchronous output pin.
V_{REF+}	100	-	+ power supply for A/D converter	Reference power supply pins for the A/D converter. Use this under the condition: 2.0 V ≤ V_{REF+} ≤ V_{DD5}
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11	1 2 3 4 5 6 7 8 100 99 98 97	Input	Analog input pins	Analog input pins for an 16-channel, 10-bit A/D converter. When not used for analog input, these pins can be used as normal input pins.
DA_A DA_B DA_C DA_D	29 66 91 92	Output	Analog output pins	Analog output pins for an 4-channel, 8-bit A/D converter. When not used for analog output, these pins can be used as normal I/O pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	30 31 32 33 34	Input	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected with the IRQnICR register. IRQ1 has AC zero-cross detection function. IRQ1 can be set at both edges at pin voltage level. When not used for interrupts, these can be used as normal input pins.
ACZ1 ACZ0	31 30	Input	AC zero-cross detection input pins	AC zero-cross detection input pin. AC zero-cross detection output “H” when input level is mid-level and “L” otherwise. ACZ input signal is connected to P20 input and IRQ0 interrupt circuit or P21 input and IRQ1 interrupt circuit. When not used for AC zero-cross detection, these can be used as normal input pins.

Name	Pin No	I/O	Function	Description
ACZ1 ACZ0	31 30	Input	AC zero-cross detection input pins	AC zero-cross detection input pin. AC zero-cross detection output “H” when input level is mid-level and “L” otherwise. ACZ input signal is connected to P20 input and IRQ0 interrupt circuit or P21 input and IRQ1 interrupt circuit. When not used for AC zero-cross detection, these can be used as normal input pins.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	64 63 62 61 60 59 58 57	Input	Key interrupt input pins	Input pins for interrupt based on OR result of pin inputs. These can be set to key input pins by 1-bit with the key interrupt control register (KEYT3_1IMD, KEYT3_2IMD) and by 2-bit with the key interrupt control register (KEYT3_1IMD). When not used for KEY input, these pins can be used as normal I/O pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	22 23 24 25 26 27 28 29	I/O	LED drive pins	Large current output pins. When not used for LED output, these pins can be used as normal I/O pins.
NWE NRE NCS NDK	75 76 77 90	Output Input	Write enable pins [Active low] Read enable pins [Active low] Chip select pins [Active low] Data acknowledge pins [Active low]	Memory control signal used when the memory area is expanded to the external of this LSI. NWE is the strobe signal output for the write operation of the external memory and NRE is the strobe signal output for the read operation of the external memory NCS is the chip selection signal outputs the external memory at the access. NDK is the acknowledge signal that indicates close of access to the external memory.
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19	67 68 69 70 71 72 73 74 78 79 80 81 82 83 84 85 86 87 88 89	Output	Address pin	A0-A19 is the address signal to the external memory.

Name	Pin No	I/O	Function	Description
D0	64	I/O	Data pin	D0-D7 is the data I/O signal to the external memory.
D1	63			
D2	62			
D3	61			
D4	60			
D5	59			
D6	58			
D7	57			
COM0	85	Output	LCD common output pins	These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal I/O port by the setting the LCD output control register LCCTR0.
COM1	86			
COM2	87			
COM3	88			
V_{LC1}	91	-	LCD power supply pins	Supply for LCD power. Apply 5.5 V≥V_{LC1}≥V_{LC2}≥V_{LC3}≥0 V. When the internal voltage divider resistor is used, V_{LC1}=V_{DD5} pin is selected as the reference voltage input pin. When LCD is not used, V_{LC1} to V_{LC3} can be used as normal I/O pins with the setting of LCD output control register0 (LCCTR0).
V_{LC2}	90			
V_{LC3}	89			
SEG0	84	Output	LCD segment output pins	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD display panel. When LCD display is turned off, V_{SS} level is output. These pins can be used as normal I/O pins with the setting of LCD output control register LCCTR1 to 7. SEG can exchange segment pins and normal port by each bit.
SEG1	83			
SEG2	82			
SEG3	81			
SEG4	80			
SEG5	79			
SEG6	78			
SEG7	77			
SEG8	76			
SEG9	75			
SEG10	74			
SEG11	73			
SEG12	72			
SEG13	71			
SEG14	70			
SEG15	69			
SEG16	68			
SEG17	67			
SEG18	66			
SEG19	65			
SEG20	64			
SEG21	63			
SEG22	62			
SEG23	61			
SEG24	60			
SEG25	59			
SEG26	58			
SEG27	57			
SEG28	56			
SEG29	55			

(Continue to next page)

Name	Pin No	I/O	Function	Description
SEG30	54	Output	LCD segment output pins	(Continued from previous page)
SEG31	53			
SEG32	52			
SEG33	51			
SEG34	50			
SEG35	49			
SEG36	48			
SEG37	47			
SEG38	46			
SEG39	45			
SEG40	44			
SEG41	43			
SEG42	42			
SEG43	41			
SEG44	40			
SEG45	39			
SEG46	38			
SEG47	37			
SEG48	36			
SEG49	35			
SEG50	34			
SEG51	33			
SEG52	32			
SEG53	31			
SEG54	30			
MMOD	10	Input	Memory mode switch input pins	Set always to V_{SS}.
DMOD	21	Input	Mode switch input pins	Set always to V_{DD5}.

4. Block Diagram

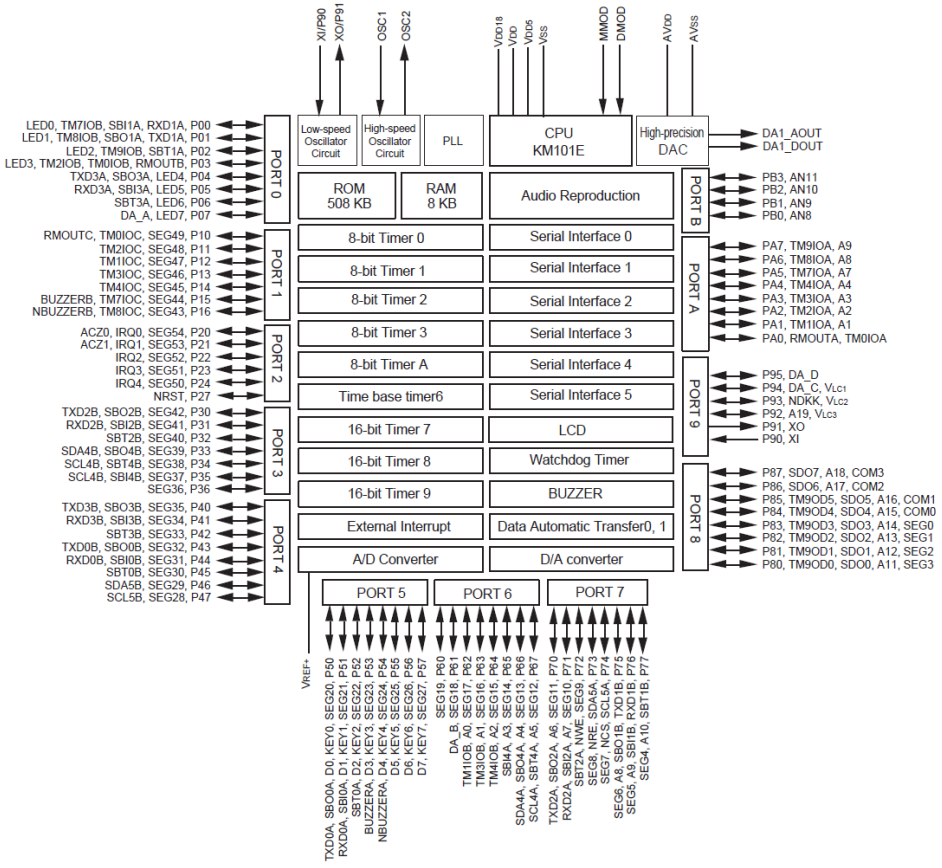


Figure: 4.1 Block Diagram

5. Electrical Characteristics

This datasheet describes the standard specification.
Please ask our sales offices for the product specifications.

Model	KM101EF59R	
Contents	Structure	CMOS integrated circuit
	Application	General purpose
	Function	CMOS, 8-bit, single chip micro controller

5.1 Absolute Maximum Ratings

V_{SS} = 0 V

Parameter			Symbol	Rating *1 *2	Unit
1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
2	Capacity connection pin		V_{DD18}	-0.3 to +2.5	
3	*4		V_{DD}	-0.3 to +4.6	
4	Input clamp current (ACZ)		I_C	-500 to +500	μA
5	Input pin voltage		V_I	-0.3 to V_{DD5} + 0.3	V
6	Output pin voltage		V_O	-0.3 to V_{DD5} + 0.3	
7	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} + 0.3	
8	Peak power current	P0	I_{OL1} (peak)	30	mA
9		Other than P0	I_{OL2} (peak)	20	
10		All pins	I_{OH} (peak)	-10	
11	Average output current *1	P0	I_{OL1} (avg)	20	
12		Other than P0	I_{OL2} (avg)	15	
13		All pins	I_{OH} (avg)	-5	
14	Power dissipation		P_T	400	mW
15	Operating ambient temperature		T_{opr}	-40 to +85	°C
16	Storage temperature		T_{stg}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect approximate 1 μF capacitor between VDD18/VDD power supply pin and the ground, and approximate 10-times capacitor connect to VDD18/VDD between VDD5 power supply pin and the ground for the internal power supply stabilization.

*3 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

*4 Applied only in Flash version.

5.2 Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

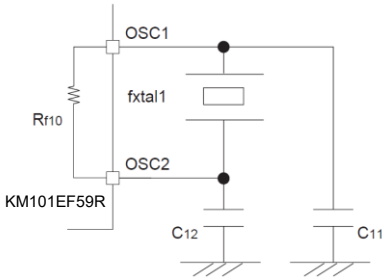
	Parameter		Symbol	Conditions	Rating			Unit
					MIN	TYP	MAX	
Power supply voltage *4								
1	Power supply voltage	In not using PLL	V_{DD5-1}	fosc ≤ 20 MHz [Double speed mode: fs ≤ 20 MHz]	2.2		5.5	V
2		In using PLL	V_{DD5-2}	4.0 MHz ≤ fosc ≤ 10 MHz [Multiplied by 2 to 10: fs ≤ 20 MHz]	2.2		5.5	
3			V_{DD5-3}	fx=32.768 kHz [Normal mode: fs=fx/2]	2.2		5.5	
4	Voltage to maintain RAM data		V_{DD5-4}	[During STOP mode]	1.8		5.5	
Operating speed *5								
5	Instruction execution time		t_{c1}	V_{DD5}=2.2 V to 5.5 V	0.05			µs
6			t_{c2}	V_{DD5}=2.2 V to 5.5 V	61			

*4 fosc: Input clock frequency to OSC1 pin. fx: Input clock frequency to XI pin

*5 t_{c1}: In the case of OSC1 as CPU clock, or OSC1 multiplied by PLL as CPU clock. t_{c2}: In the case of XI as CPU clock.

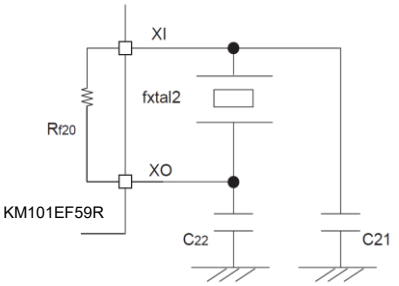
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Crystal oscillator 1 Figure:1.5.1 [NORMAL mode]						
7 Crystal frequency	f_{xtal1}	V_{DD5} = within the operation power supply voltage (Refer to the reference value of power supply voltage 1 to 3.)	2.0		20	MHz
8 External capacitors	C_{11}			10		pF
9	C_{12}			10		
10 Internal feedback resistor	R_{f10}	V_{DD5}=5.0 V		950		kΩ
Crystal oscillator 2 Figure:1.5.2 [SLOW mode]						
11 Crystal frequency	f_{xtal2}	V_{DD5}=2.2 V to 5.5 V	2.0		20	MHz
12 External capacitors	C_{21}			4		pF
13	C_{22}			4		
14 Internal feedback resistor	R_{f20}	V_{DD5}=5.0 V		6		kΩ



Instruction cycle becomes clock frequency divided by 1/2
Built-in feedback resistor

Figure: 5.1 Crystal oscillator 1



Instruction cycle becomes clock frequency divided by 1/2
Built-in feedback resistor

Figure: 5.2 Crystal oscillator 2

Connect external capacitors that suits the used pin. When crystal oscillator or ceramic oscillator is used, the frequency is changed depending on the condenser rate. Therefore, consult the manufacturer of the pin for the appropriate external capacitor.

V_{DD5} = 2.2 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
15	Clock frequency	f_{OSC1}		1.0		20.0	MHz
16	High level pulse width *6	t_{wh1}	Figure:1.5.3	22.5			ns
17	Low level pulse width *6	t_{wl1}		22.5			
18	Rising time *7	t_{wr1}	Figure:1.5.3	0		5.0	
19	Falling time *7	t_{wf1}		0		5.0	
External clock input 2 XI (XO is unconnected)							
20	Clock frequency	f_{OSC2}			32.768		kHz
21	High level pulse width *6	t_{wh2}	Figure:1.5.4		4.5		µs
22	Low level pulse width *6	t_{wl2}			4.5		
23	Rising time *7	t_{wr2}	Figure:1.5.4	0		20	ns
24	Falling time *7	t_{wf2}		0		20	

*6 The clock duty rate in the standard mode should be 45 % to 55 %

*7 Rising time and falling time differ depending on oscillation frequency.
This is noted that the maximum value is a rough value, not a specified value.
Consult the oscillator manufacturer and perform matching tests for determining appropriate values

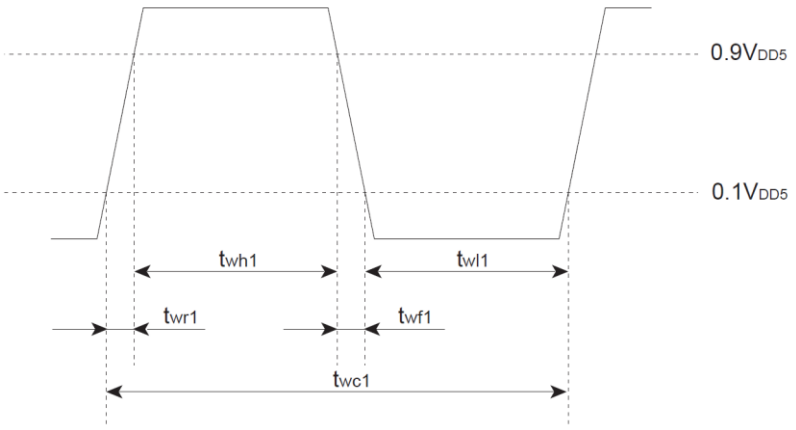


Figure: 5.3 OSC1 Timing Chart

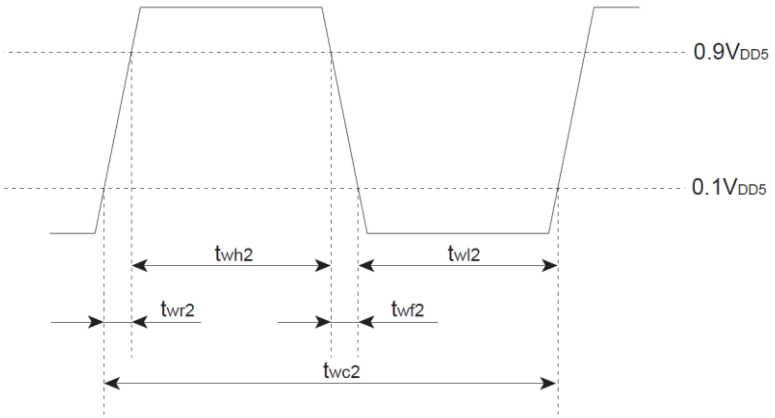


Figure: 5.4 XI Timing Chart

5.3 DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Power supply current *8 (NORMAL mode: fs=fosc/2 SLOW mode: fs=fx/2)						
1	Power supply current	I_{DD1}	fosc=20 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		4 (9)	8 (18)	mA
2		I_{DD2}	fosc=4 MHz [Multiplied by 5: fs=20 MHz] V_{DD5}=5 V (In using PLL)		4 (10)	8 (20)	
3		I_{DD3}	fosc=8 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		1.5 (5)	3 (9)	
4		I_{DD4}	fosc=4 MHz [Double-speed mode: fs=fosc] V_{DD5}=5 V (In not using PLL)		1 (3)	2 (6)	
5		I_{DD5}	fx=32.768 MHz, [fs=fx/2] V_{DD5}=3 V Ta=25 °C		5 (60)	20 (120)	µA
6		I_{DD6}	fx=32.768 MHz, [fs=fx/2] V_{DD5}=3 V Ta=85 °C			75 (200)	
7	Supply current during HALT1 mode	I_{DD7}	fx=32.768 MHz V_{DD5}=3 V Ta=25 °C		4 (6)	13 (18)	
8		I_{DD8}	fx=32.768 kHz V_{DD5}=3 V Ta=85 °C			70 (80)	
9	Supply current during STOP mode	I_{DD9}	V_{DD5}=5 V Ta=25 °C		1 (2)	6 (7)	
10		I_{DD10}	V_{DD5}=5 V Ta=85 °C			60 (60)	

*8 Measured under condition without load. (pull-up / pull-down resistors are unconnected.)

- The supply current during operation, I_{DD1} to I_{DD2} are measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <NORMAL mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 20 MHz square wave of V_{DD5} and V_{SS} amplitudes is input to the OSC1 pin.
- The supply current during operation, I_{DD3} is measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <SLOW mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and a 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during HALT1 mode, I_{DD4} is measured under the following conditions:
  After all I/O pins are set to input mode and the oscillation is set to <HALT1 mode>, the input pins are at V_{DD5} level, and an 32.768 kHz square wave of V_{DD5} and V_{SS} amplitudes is input to the XI pin.
- The supply current during STOP mode, I_{DD6} is measured under the following conditions:
  After the oscillation is set to <STOP mode>, the MMOD pin is at V_{SS} level, the input pins are at V_{DD5} level, and the OSC1 and XI pins are unconnected.
- The values in parentheses are for Flash version.

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating MIN	Rating TYP	Rating MAX	Unit
	Input pin 1 MMOD, DMOD, ATRST						
11	Input high voltage	V_{IH1}		$0.8V_{DD5}$		V_{DD}	V
12	Input low voltage	V_{IL1}		0		$0.2V_{DD5}$	V
13	Input leakage current	I_{LK1}	V_{IN}=0 V to V_{DD5}			± 2	μA
	I/O pin 2 P27 (NRST)						
14	Input high voltage	V_{IH2}		$0.8V_{DD5}$		V_{DD5}	V
15	Input low voltage	V_{IL2}		0		$0.15V_{DD5}$	V
16	Pull-up resistor	R_{RH1}	V_{DD5}=5.0V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
	I/O pin 3 P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77						
17	Input high voltage	V_{IH3}		$0.8V_{DD5}$		V_{DD5}	V
18	Input low voltage	V_{IL3}		0		$0.2V_{DD5}$	V
19	Input leakage current	I_{LK2}	V_{IN}=0 V to V_{DD5}			± 2	μA
20	Pull-up resistor	R_{RH2}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
21	Pull-down resistor	R_{RH1}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-down resistor ON	10	50	100	kΩ
22	Output high voltage	V_{OH1}	V_{DD5}=5.0 V I_{OH}=-0.5 mA	4.5			V
23	Output low voltage	V_{OL1}	V_{DD5}=5.0 V I_{OL}=1.0 mA			0.5	V
	I/O pin 4 P80 to P87, P90 to P95, PA0 to PA7, PB0 to PB3						
24	Input high voltage	V_{IH4}		$0.8V_{DD5}$		V_{DD5}	V
25	Input low voltage	V_{IL4}		0		$0.2V_{DD5}$	V
26	Input leak current	I_{LK3}	V_{IN}=0 V to V_{DD5}			± 2	μA
27	Pull-up resistor	R_{RH3}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
28	Output high voltage	V_{OH2}	V_{DD5}=5.0 V I_{OH}=0.5 mA	4.5			V
29	Output low voltage	V_{OL2}	V_{DD5}=5.0 V I_{OL}=1.0 mA			0.5	V

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 5 P00 to P07							
30	Input high voltage1	V_{IH5}		$0.8V_{DD5}$		V_{DD5}	V
31	Input low voltage1	V_{IL5}		0		$0.2V_{DD5}$	
32	Input leak current	I_{LK4}	V_{IN}=0 V to V_{DD5}			± 2	μA
33	Pull-up resistor	R_{RH4}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-up resistor ON	10	50	100	kΩ
34	Pull-down resistor	R_{RL2}	V_{DD5}=5.0 V V_{IN}=V_{SS} Pull-down resistor ON	10	50	100	
35	Output high voltage	V_{OH3}	V_{DD5}=5.0 V I_{OH}=0.5 mA	4.5			V
36	Output low voltage1	V_{OL3}	V_{DD5}=5.0 V I_{OL}=1.0 mA LED output OFF			0.5	
37	Output low voltage2	V_{OL4}	V_{DD5}=5.0 V I_{OL}=15 mA LED output ON			1.0	
I/O pin 6 P20 (during used as ACZ) and P21 (during used as ACZ) are regulated at 5.0 V							
38	Input high voltage1	V_{DHH}	Figure: 5.5	4.5			V
39	Input high voltage2	V_{DHL}		1.5			
40	Input low voltage1	V_{DLH}				3.5	
41	Input low voltage2	V_{DLL}				0.5	
42	Input clamp current	I_{C3}	V_{IN} > V_{DD5}, V_{IN} < 0 V			± 500	μA

V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Display output pin 1 COM0 to COM3 (At V_{LC1}, V_{SS} Voltage output) *9							
43	Output high voltage (In V_{LC1} voltage output)	V_{OCOMH}	V_{DD5}=V_{LC1}=5.0 V I_{COM}= -10 μA	4.4			V
44	Output low voltage (In V_{SS} voltage output)	V_{OCOML}	V_{DD5}=V_{LC1}=5.0 V I_{COM}=10 μA			0.6	
Display output pin 2 SEG0 to SEG54 (At V_{LC1}, V_{SS} Voltage output) *10							
45	Output high voltage (In V_{LC1} voltage output)	V_{OSEGH}	V_{DD5}=V_{LC1}=5.0 V I_{SEG}= -2 μA	4.4			V
46	Output low voltage (In V_{SS} voltage output)	V_{OSEGL}	V_{DD5}=V_{LC1}=5.0 V I_{SEG}=2 μA			0.6	
Display power pin 1 V_{LC1}, V_{LC2}, V_{LC3}							
47	Internal dividing resistor	R_{VL1}	Ta=+25 °C *11 (Impedance between V_{LC1} and V_{SS})	142.5	300	570	kΩ
48		R_{VL2}		15	30	60	

*9 However, COM0 to COM3 are also used as P84 to P87.

*10 However, SEG0 to SEG54 are also used as P10 to P16, P20 to P24, P30 to P36, P40 to P47, P50 to P57, P60 to P67, P70 to P77and P80 to 83.

*11 Summation of 3 resistors among V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}

5.4 A/C Converter Characteristics

V_{DD5}=5.0 V
V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Rising time	t_{rs}	Figure: 5.5	30			µs
2	Falling time	t_{fs}		30			

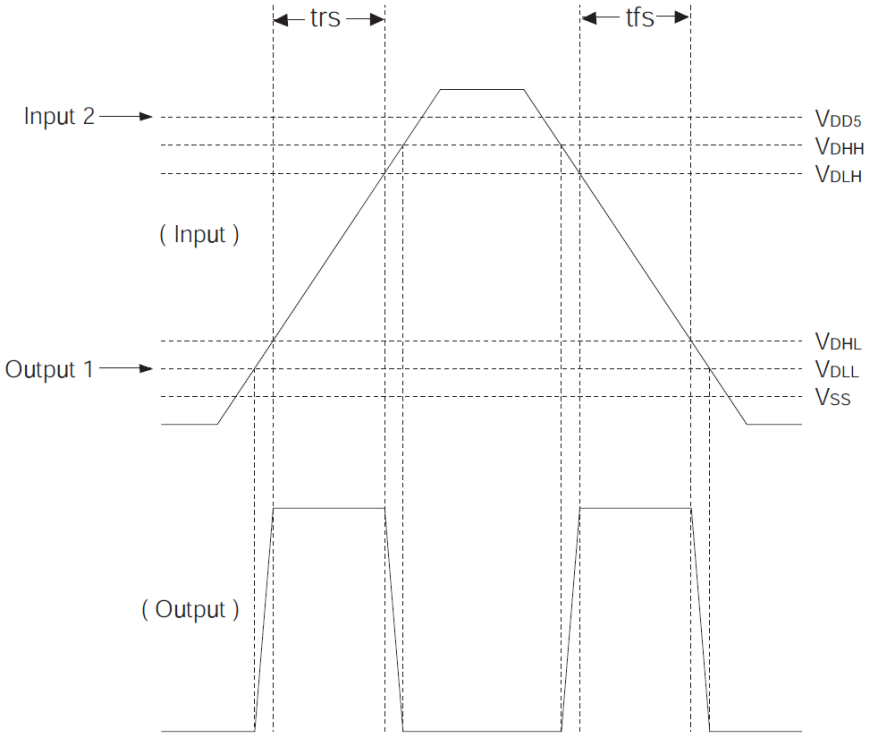


Figure: 5.5 Operation of AC Zero-Cross Detection Circuit

5.5 A/D Converter Characteristics

V_{DD5}=5.0 V
V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution					10	Bits
2	Non-linearity error 1		V_{DD5}=5.0 V, V_{SS}=0 V V_{ref+}=5.0 V T_{AD}=800 ns *12			±3	LSB
3	Differential linearity error 1					±3	
4	Zero transition voltage		V_{DD5}=5.0 V, V_{SS}=0 V V_{ref+}=5.0 V T_{AD}=800 ns *12	-30	10	30	mV
5	Full-scale transition voltage			4970	4990	5030	
6	A/D conversion time		T_{AD}=800 ns *12	12.93			µs
7			fx=32.768 kHz T_{AD}=15.2 µs *12	427.25			
8	Sampling time		T_{AD}=800 ns *12	1.6			
9			fx=32.768 kHz fs=8.192 kHz T_{AD}=15.2 µs *12	30.52			
10	Reference voltage	V_{ref+}	Note)	2.0		V_{DD5}	V
11	Analog input voltage			V_{SS}		V_{ref+}	
12	Analog input leakage current		When channel is OFF V_{ADIN}=0 V to 5.0 V			±2	µA
13	Reference voltage pin input leakage current		When V_{REF+} is OFF $V_{ss} \leq V_{REF+} \leq V_{DD5}$			±5	
14	Ladder resistance	R_{LADD}	V_{DD5}=5.0 V	15	40	80	kΩ

*12 T_{AD} is A/D conversion clock cycle.
The values of 2 to 5 are guaranteed on the condition that V_{DD5}=V_{ref+}=5 V, V_{SS}=0 V.

Note) The voltage difference between V_{ref+} and V_{SS} should be set to more than 2 V.

The reference voltage input to VREF+ pin should be used on the condition of 2.0 V ≤ VREF+ ≤ VDD5 to avoid the malfunctions of microcontroller.

5.6 D/A Converter Characteristics

V_{DD5}=5.0 V
V_{SS}=0 V
Ta = 25 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
1	Resolution			-	-	8	Bits
2	Reference voltage low level	D_{AVSS}		V_{SS}	-		V
3	Reference voltage high level	D_{AVDD}			-	V_{DD5}	
4	Zero scale output voltage	V_{ZS}	V_{DD5}=5.0 V, V_{SS}=0 V D7 to D0=ALL "L"	-0.05	0	0.05	
5	Full scale output voltage	V_{FS}	V_{DD5}=5.0 V, V_{SS}=0 V D7 to D0=ALL "H"	4.93	4.98	5.03	
6	Analog output resistance (Minimum reference resistance)	R_{OAT}		5	10	15	kΩ
7	Non-linearity error	N_{LE}	V_{DD5}=5.0 V, V_{SS}=0 V	-	± 2.0	± 3.0	LSB
8	Differential non-linearity error	D_{NLE}	V_{DD5}=5.0 V, V_{SS}=0 V	-	± 2.0	± 3.0	
9	Settling time	T_{SET}	External capacitor CL=15 pF All bits are set to ON or OFF	-	1.5	3.0	μs

5.7 Auto Reset Characteristics

$V_{DD5}=V_{RST}$ to 5.0 V
V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
1	Operation voltage	V_{DD7}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
2	Power supply detection level	V_{RST}		3.7		4.5	V
3	Supply voltage change rate	$\Delta t/\Delta V$		250			μs/V
Power supply current							
4	Auto reset power consumption	I_{DD7}	V_{DD5}=5 V		220	330	μA

5.8 Audio Output Characteristics

$V_{DD5}=V_{RST}$ to 5.0 V
V_{SS}=0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Output pin 7 DA1_AOUT							
1	Power supply voltage	AV_{DD}	$AV_{DD}=V_{DD5}$	4.5		5.5	V
2	Signal-to-noise ratio	S/N	AV_{DD}=5 V (Note1)	80	88		dB
3	Dynamic range	D.R.	AV_{DD}=5 V (Note1)	70	78		dB
4	Total harmonic distortion ratio	THD+N	AV_{DD}=5 V (Note1)		0.16	0.26	%
5	Output impedance	R_{AOUT}	AV_{DD}=5 V	0.25		2.0	kΩ
Output pin 8 DA1_DOUT							
6	Output voltage high level	V_{OH2}	V_{DD5}=5.0 V I_{OH}=-2 mA	4.5			V
7	Output voltage low level	V_{OL2}	V_{DD5}=5.0 V I_{OL}=2.0 mA			0.5	

(Note1) This is the value sampling 1kHz SIN wave at 20kHz and recording with 16bit-PCM.
(Note2) H2,H3 and H4 are the output level at the measuring point on the audio characteristic measuring circuit (Figure: 5.6).

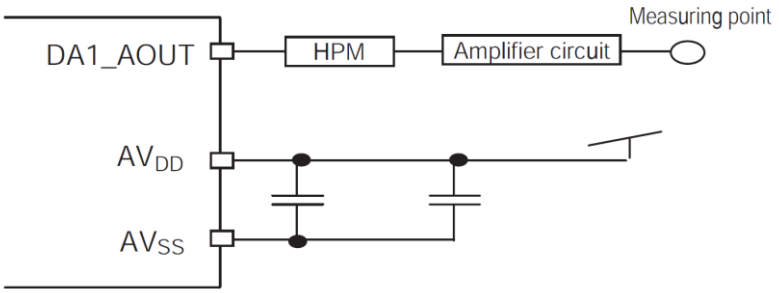


Figure: 5.6 Audio Characteristic Measuring Circuit (a)

AVDD and VDD5 should be at the same electric potential regardless of whether or not the audio production function is used.

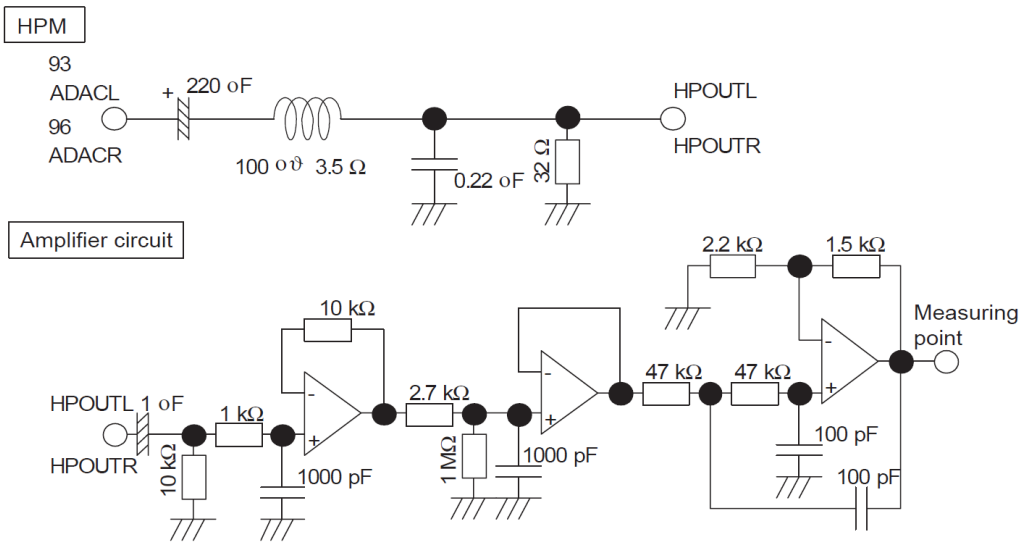


Figure: 5.7 Audio Characteristic Measuring Circuit (b)

5.9 Flash EEPROM Program Conditions

Item		Symbol	Condition	Rating			Unit
				MIN	TYP	MAX	
1	Programming voltage level	V_{DD5-6}		2.7		5.5	V
2	Data retention period	Thold		10			Years
3	Programming guarantee number times	E_{MAX}				1000	Times

6. Package Dimension

■ QFP 100-pin (18 mm x 18 mm, 0.65 mm pitch)

Units: mm

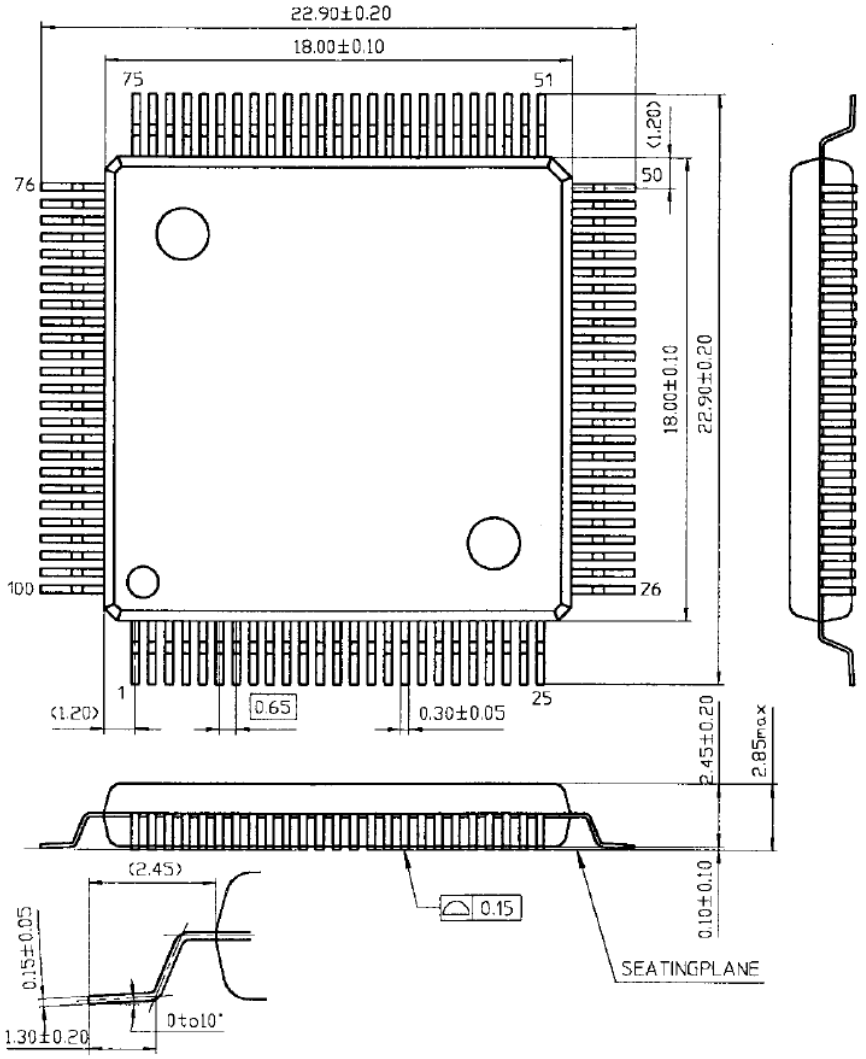


Figure: 6.1 Package Dimension

The external dimensions of the package are subject to change. Before using this product, please obtain product specifications from the sales offices.

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