8-bit Microcontroller

KM101EF56K/57G/76K Series Datasheet

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1. Overview

1.1 Overview

The KM101E series of 8-bit single-chip microcontrollers incorporate multiple types of peripheral functions. This chip series is well suited for camera, VCR, MD, TV, CD, LD, printer, telephone, home automation, pager, air conditioner, PPC, fax machine, music instrument and other applications.

This LSI brings to embedded microcontroller applications flexible, optimized hardware configurations and a simple efficient instruction set. KM101EF57 series has an internal 128 KB of ROM and 6 KB of RAM. Peripheral functions include 5 external interrupts, 29 internal interrupts including NMI, 12 timer counters, 4 types of serial interfaces, A/D converter, D/A converter, LCD driver, 2 types of watchdog timer, data automatic function and buzzer output. The system configuration is suitable for in camera, timer selector for VCR, CD player, or mini-component.

With 5 oscillation systems (high-speed (internal frequency: 20 MHz), high-speed (crystal/ceramic frequency: max. 10 MHz) / low-speed (internal frequency: 30 kHz), low-speed (crystal/ceramic frequency: 32.768 kHz) and PLL: frequency multiplier of high frequency) contained on the chip, the system clock can be switched to high-speed frequency input (NORMAL mode), PLL input (PLL mode), or to low-speed frequency input (SLOW mode). The system clock is generated by dividing the oscillation clock or PLL clock. The best operation clock for the system can be selected by switching its frequency ratio by programming. High speed mode has the normal mode which is based on the clock dividing fpll, (fpll is generated by original oscillation and PLL), by 2 (fpll/2), and the double speed mode which is based on the clock not dividing fpll.

A machine cycle (minimum instruction execution time) in the normal mode is 200 ns when the original oscillation fosc is 10 MHz (PLL is not used). A machine cycle in the double speed mode, in which the CPU operates on the same clock as the external clock, is 100 ns when fosc is 10 MHz . A machine cycle in the PLL mode is 50 ns (maximum).

1.2 Product Summary

This datasheet describes the following model.

Table: 1.1 Product Summary

Model	ROM Size	RAM Size	Classification	Package
KM101EF76K	256 KB	10 KB	Flash EEPROM version	LQFP 128-pin
KM101EF57G	128 KB	6 KB	Flash EEPROM version	LQFP 80-pin TQFP 80-pin
KM101EF56K	256 KB	10 KB	Flash EEPROM version	QFP 100-pin

2. Hardware Functions

- ROM / RAM capacity
  KM101EF76K: ROM 256 KB / RAM 10 KB
  KM101EF57G: ROM 128 KB / RAM 6 KB
  KM101EF56K: ROM 256 KB / RAM 10 KB

- Package:
  KM101EF76K: LQFP 128-pin (18 mm × 18 mm / 0.5 mm pitch)
  KM101EF57G: LQFP 80-pin (14 mm × 14 mm / 0.65 mm pitch)
  TQFP 80-pin (12 mm × 12 mm / 0.5 mm pitch)
  KM101EF56K: QFP 100-pin (18 mm × 18 mm / 0.65 mm pitch)

- Machine Cycle
  High-speed mode
  0.05 µs/20 MHz (2.7 V to 5.5 V)
  0.125 µs/8 MHz (1.8 V to 5.5 V)
  Low-speed mode
  62.5 µs/ 32 kHz (1.8 V to 5.5 V)

- Clock Gear Circuit
  Internal system clock speed is changeable by selecting division ratio of oscillation clock. (Divided by 1, 2, 4, 16, 32, 64, 128)

- Oscillation Circuit
  4 types
  High-speed (Internal oscillation: frc), High-speed (crystal/ceramic: fosc),
  Low-speed (Internal oscillation: frcs), Low-speed (crystal/ceramic: fx)
  High-speed internal oscillation 20 MHz / 16 MHz (selectable)
  Low-speed internal oscillation 30 kHz

- Clock Multiplication Circuit
  PLL circuit output clock (fpll) fosc multiplied by 2, 3, 4, 5, 6, 8, 10,
  1/2 × frc multiplied by 4, 5 enabled
  * When clock multiplication circuit is not used, fpll = fosc or fpll = frc
  * Selectable from high-speed clock for peripheral functions (fpll-div) fpll, fpll divided by 2, 4, 8, 16

- Memory bank
  Data memory space is expanded by the bank system.
  Bank for the source address / Bank for the destination address.

- Operation Mode
  NORMAL mode (high-speed mode)
  PLL mode
  SLOW mode (low-speed mode)
  HALT mode
  STOP mode
  and operation clock switching

- Operating Voltage
  1.8 V to 5.5 V

- Operation ambient temperature
  -40 °C to +85 °C

- Interrupt

Interrupt	KM101EF76K 36 sets	KM101EF57G 34 sets	KM101EF56K 36 sets
<Overrun interrupt>			
Non-maskable interrupt (NMI)	√	√	√
<Timer interrupt>			
Timer 0 interrupt	√	√	√
Timer 1 interrupt	√	√	√
Timer 2 interrupt	√	√	√
Timer 3 interrupt	√	√	√
Timer 4 interrupt	√	√	√
Timer 6 interrupt	√	√	√
Timer 7 interrupt	√	√	√
Time-base interrupt	√	√	√
Timer 7 compare register 2 match interrupt	√	√	√
Timer 8 interrupt	√	√	√
Timer 8 compare register 2 match interrupt	√	√	√
PWM overflow interrupt	√	√	√
PWM under flow interrupt	√	√	√
Timer 9 compare register 2 match interrupt	√	√	√
24H timer interrupt	√	√	√
Alarm match interrupt	√	√	√
<Serial interrupt>			
LIN interrupt	√	√	√
Serial 0 interrupt	√	√	√
Serial 0 UART reception interrupt	√	√	√
Serial 1 interrupt	√	√	√
Serial 1 UART reception interrupt	√	√	√
Serial 2 interrupt	√	√	√
Serial 2 UART reception interrupt	√	√	√
Serial 3 interrupt	√	-	√
Serial 3 UART reception interrupt	√	-	√
Serial 4 interrupt	√	√	√
Serial 4 stop condition interrupt	√	√	√
<A/D interrupt>			
A/D conversion interrupt	√	√	√
<Data automatic transfer interrupt>			
ATC1 interrupt	√	√	√
<Low voltage detection interrupt>			
Low voltage detection interrupt	√	√	√
<External interrupt>			
IRQ0 (Edge selection, noise filter connectable)	√	√	√
IRQ1 (Edge selection, noise filter connectable)	√	√	√
IRQ2 (Edge selection, both edge interrupt, noise filter connectable)	√	√	√
IRQ3 (Edge selection, both edge interrupt, noise filter connectable)	√	√	√
IRQ4 (Edge selection, both edge interrupt, noise filter connectable, KEY scan interrupt)	√	√	√

• Timer Counter: 12 sets

- General-purpose 8-bit timer × 5 sets
- General-purpose 16-bit timer × 2 sets
- General-purpose 16-bit timer × 2 sets
- Motor control 16-bit timer × 1 set
- 8-bit free-run timer × 1 set-
  Time-base timer × 1 set
- Baud rate timer × 1 set
- 24H timer × 1 set

Timer 0 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TM0IOB, event count, simple pulse width measurement
- Double-buffered compare register (× 1) * Function in KM101EF76K and KM101EF56K
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
- Real-time control
  Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 1 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), event count 16-bit cascade connection (connected with timer 0)
- Double-buffered compare register (× 1) * Function in KM101EF76K and KM101EF56K
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 2 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2 bits) type PWM output can be output to large current pin TM2IOB, event count, simple pulse width measurement, 24-bit cascade connection (connected with timer 0, 1), timer synchronous output
- Double-buffered compare register (× 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output
- Real-time control
  Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 3 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), event count
  16-bit cascade connection (connected with timer 2),
  32-bit cascade connection (connected with timer 0, 1, 2)
- Double-buffered compare register (× 1)
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

Timer 4 (General-purpose 8-bit timer)

- Square wave output (Timer pulse output), added pulse (2bit) type PWM output, event count, simple pulse width measurement
- Clock source
  fpll-div, fpll-div/4, fpll-div/16, fpll-div/32, fpll-div/64, fpll-div/128, fs/2, fs/4, fs/8, fslow, external clock, timer A output

- Timer Counter (continued)

Timer 6 (8-bit free-run timer, time-base timer)
8-bit free-run timer
- Clock source
fpll-div, fpll-div/2^2, fpll-div/2^3, fpll-div/2^{12}, fpll-div/2^{13}, fs, fslow, fslow/2^2, fslow/2^3, fslow/2^{12}, fslow/2^{13}

Time-base timer
- Interrupt generation cycle
fpll-div/2^7, fpll-div/2^8, fpll-div/2^9, fpll-div/2^{10}, fpll-div/2^{13}, fpll-div/2^{15}, fslow/2^7, fslow/2^8, fslow/2^9, fslow/2^{10}, fslow/2^{13}, fslow/2^{15}

Timer 7 (General-purpose 16-bit timer)
- Clock source
fpll-div, fs, external clock, timer A output, serial 0 transfer clock output, timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (× 2)
Double-buffered input capture register (× 2)
Timer interrupt (× 2 vector)
- Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM7IOB, timer synchronous output, event count, input capture function (both edges operable)
- Real-time control
Timer (PWM) output is controlled among the three values: "Fixed to High", "Fixed to Low", or "Hi-Z" at falling edge of external interrupt 0 (IRQ0)

Timer 8 (General-purpose 16-bit timer)
- Clock source
fpll-div, fs, external clock, timer A output, timer 6 compare match cycle divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (× 2)
Double-buffered input capture register (× 1)
Timer interrupt (× 2 vector)
- Timer function
Square wave output (Timer pulse output), high-precision PWM output (cycle/duty continuous changeable) can be output to large current pin TM8IOB, event count, pulse width measurement, input capture function (both edges operable)
32-bit cascade connection (connected with timer 7), 32-bit PWM output, input capture is available in 32-bit cascade

Timer 9 (Motor control 16-bit timer)
- Clock source
fpll-div, fs, external clock, Timer A output divided by 1, 2, 4, 16
- Hardware configuration
Double-buffered compare register (× 2)
Timer interrupt (× 3 vector)
- Timer function
Square wave output (Timer pulse output) can be changed to large current output, complementary 3-phase PWM output, triangle wave and saw tooth wave are supported, dead time insertion available, event count
- Pin output control
PWM output control is possible by external interrupt 0 to 4 (IRQ 0 to 4) ("Hi-z", output data fixed)

Timer A (baud rate timer)
- Clock output for peripheral functions
- Clock source
fpll-div divided by 1/1, 2, 4, 8, 16, 32, and fs divided by 2, 4

- Timer Counter (continued)

24H timer
- Clock source (Usable frequency)
  fpll (4 MHz, 4.19 MHz, 5 MHz, 8 MHz, 8.38 MHz, 10 MHz, 16 MHz, 16,77 MHz, 20 MHz), fx (32.768 kHz), frc (20 MHz, 16 MHz), frcs (30 kHz)
- Hardware configuration
  0.5 seconds counter, minute counter, hour counter
  Alarm compare register (in 0.5 seconds, in minutes, in hours) (× 1)
  Timer interrupt (·×2 vector)
- Timer function
  Interval function (interrupts every 0.5 seconds, 1 second, 1 minute, 1 hour, 24 hours)
  Alarm function

- Watchdog timer

Overrun detection cycle is selectable from $fs/2^{16}$, $fs/2^{18}$, $fs/2^{20}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Watchdog timer2

Overrun detection cycle is selectable from $frcs/2^4$, $frcs/2^5$, $frcs/2^6$, $frcs/2^7$, $frcs/2^8$, $frcs/2^9$, $frcs/2^{10}$,$frcs/2^{11}$, $frcs/2^{12}$, $frcs/2^{13}$, $frcs/2^{14}$, $frcs/2^{15}$
Forced to reset inside LSI by hardware when a software processing error is detected twice

- Synchronous output function (Timer synchronous output, interrupt synchronous output)

Latch data is output from port 8 at the event timing of synchronous output signal of timer 1, timer 2, timer 7, or external interrupt2 (IRQ2)

- Buzzer Output

Output frequency can be selected from $fpll\text{-}div/2^9$, $fpll\text{-}div/2^{10}$, $fpll\text{-}div/2^{11}$, $fpll\text{-}div/2^{12}$, $fpll\text{-}div/2^{13}$, $fpll\text{-}div/2^{14}$, $fslow/2^3$, $fslow/2^4$

- A/D converter

KM101EF76K: 10-bit × 24 channels
KM101EF57G: 10-bit × 12 channels
KM101EF56K: 10-bit × 24 channels

- D/A converter

KM101EF76K: 8-bit × 4 channels
KM101EF57G: 8-bit × 2 channels
KM101EF56K: 8-bit × 4 channels

- Data automatic transfer

Data is automatically transferred in all memory space
- External interrupt activation/internal event activation/software activation
- Max. 255 byte continuous transfer
- Serial continuous transmission and reception is supported
- Burst transfer function (Including interrupt emergency stop)

- Serial interface

KM101EF76K: 5 systems
KM101EF57G: 4 systems
KM101EF56K: 5 systems

Serial interface 0 (Hardware LIN / Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
  fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
  Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
-Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable
- Hardware LIN
  Synch Break generation, Wake-up detection, Synch Break detection, Synch Field measurement are available

- Serial interface (continued)

Serial interface 1 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable

Serial interface 2 (Full duplex UART / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable

Serial interface 3 (Full duplex UART / Synchronous serial interface)
* Function in KM101EF76K and KM101EF56K
Synchronous serial interface
- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/16, fpll-div/64, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Full duplex UART (Baud rate timer: selected from timer 0 to 4, or timer A)
- Parity check, overrun error/framing error are detected
- Transfer bits 7 to 8 are selectable

Serial interface 4 (Multi master IIC / Synchronous serial interface)
Synchronous serial interface
- Transfer clock source
fpll-div/2, fpll-div/4, fpll-div/8, fpll-div/32, fs/2, fs/4,
Timer 0 to 4, Timer A output divided by 1, 2, 4, 8, 16, External clock
- MSB/LSB first selectable, 1 to 8 bits of arbitrary transfer
- Continuous transmission, continuous reception, continuous transmission and reception are available.

Multi master IIC
- 7, 10-bit slave address is settable
- General call communication mode is supported

- Auto reset circuit
- Low voltage detection circuit
- Clock Monitoring Function

- LED driver: 8 sets

- LCD driver

Segment output
KM101EF76K: Max. 55 pins (SEG0 to SEG54)
KM101EF57G: Max. 41 pins (SEG0 to SEG40)
KM101EF56K: Max. 55 pins (SEG0 to SEG54)
Segment output pins can be switched to I/O ports in 1 bit.
* At reset, Segment outputs are input ports.
Common output: 4 pins
COM0 to 3 can be switched to I/O ports in 1 bit.
Display mode selection
Static
1/2 duty, 1/2 bias
1/3 duty, 1/3 bias
1/4 duty, 1/3 bias
LCD driver clock
When the source clock is the main clock (fpll)
$1/2^{18}$,$1/2^{17}$,$1/2^{16}$,$1/2^{15}$,$1/2^{14}$,$1/2^{13}$,$1/2^{12}$,$1/2^{11}$
When the source clock is the sub clock (fslow)
$1/2^{9}$,$1/2^{8}$,$1/2^{7}$,$1/2^{6}$
Timer 0 to 4, Timer A output
LCD power supply
LCD power supply is separated from V_{DD5}. (can be used when $V_{LC1} \leq V_{DD5}$)
External power supply voltage can be selectable.
(Supply voltage is supplied from V_{LC1}, V_{LC2}, and V_{LC3})
Internal dividing resistors
(External power supply voltage is divided the voltage input to V_{LC1} by internal resistors.)

- Ports

Ports	KM101EF76K (pins)	KM101EF57G (pins)	KM101EF56K (pins)
<I/O ports>	104	70	104
LCD segment	55	41	55
LCD common	4	4	4
Serial interface communication	30	21	30
Timer I/O	34	21	28
Buzzer output	4	2	4
A/D input	24	16	24
External interrupt	10	5	5
LCD power supply	3	3	3
LED driver (high-current)	8	8	8
High-speed oscillation	2	2	2
Low-speed oscillation	2	2	2
D/A output	4	2	4
<Special function pins>	10	10	10
Operation mode input	3	3	3
Reset input	1	1	1
Analog reference voltage input	1	1	1
Power supply	4	4	4

3. Pin Description

3.1 Pin configuration

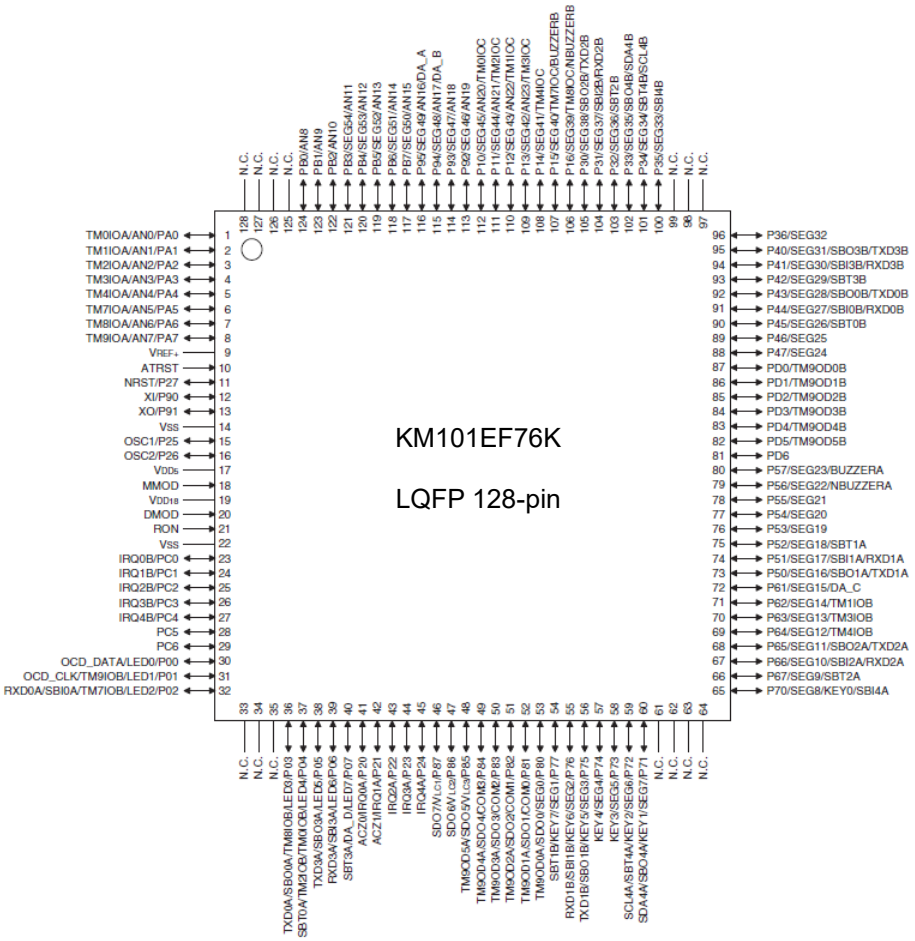


Figure: 3.1 Pin Configuration (KM101EF76K)

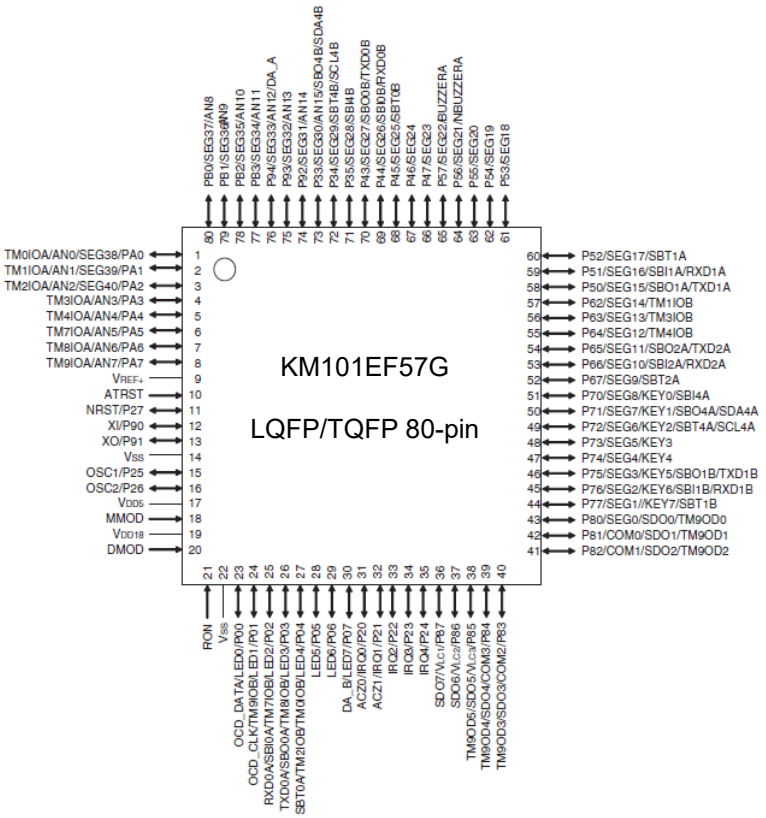


Figure: 3.2 Pin Configuration (KM101EF57G)

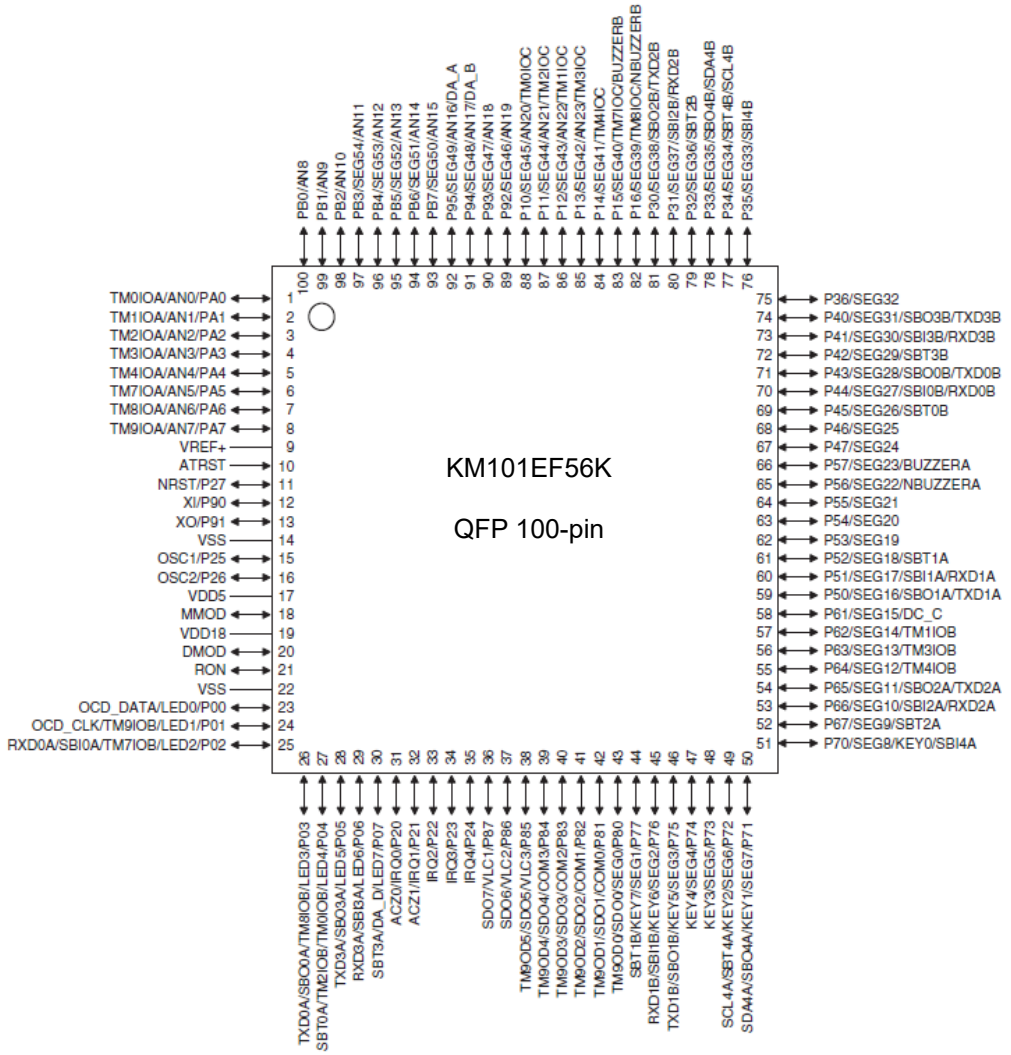


Figure: 3.3 Pin Configuration (KM101EF56K)

3.2 Pin Functions

Table: 3.1 Pin Functions (KM101EF76K)

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
V_{SS} V_{DD5}	14 22 17	-	Power supply pins	Supply 1.8 V to 5.5 V to V_{DD5}, and 0 V to V_{SS}. Connect 0.1μF and more than 1 μF of bypass capacitor for internal power stabilization
V_{DD18}	19	-	Internal power output pin	Outputs internal power voltage 1.8 V. Connect 0.1 μF and more than 1 μF of bypass capacitor between V_{DD18} and V_{SS} pins for internal power stabilization.
OSC1	15	Input	High-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for high-speed operation clock. For external clock input, input to OSC1 and open OSC2. The chip will not operate with an external clock when using either STOP mode or SLOW mode
OSC2	16	Output	High-speed operation clock output pin	
XI	12	Input	Low-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for low-speed operation clock. For external clock input, input to XI and open XO. The chip will not operate with an external clock when using STOP mode.
XO	13	Output	Low-speed operation clock output pin	
NRST	11	Input	Reset pin [Active low]	This pin resets the chip at power on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initializes the internal state of the LSI. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an Nch open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD5}.
ATRST	10	Input	Auto reset setting pin	Input “High” to enable auto reset function and “Low” to disable this function.
P00 P01 P02 P03 P04 P05 P06 P07	30 31 32 36 37 38 39 40	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P10 P11 P12 P13 P14 P15 P16	112 111 110 109 108 107 106	I/O	I/O port 1	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	41 42 43 44 45 15 16	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P27	11	Input	Input port 2	P27 is an Nch open-drain port. When “0” is written and the reset is initiated by software, a low level will be output.

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
P30	105	I/O	I/O port 3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P31	104			
P32	103			
P33	102			
P34	101			
P35	100			
P36	96			
P40	95	I/O	I/O port 4	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P41	94			
P42	93			
P43	92			
P44	91			
P45	90			
P46	89			
P47	88			
P50	73	I/O	I/O port 5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P51	74			
P52	75			
P53	76			
P54	77			
P55	78			
P56	79			
P57	80			
P61	72	I/O	I/O port 6	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P62	71			
P63	70			
P64	69			
P65	68			
P66	67			
P67	66			
P70	65	I/O	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P71	60			
P72	59			
P73	58			
P74	57			
P75	56			
P76	55			
P77	54			
P80	53	I/O	I/O port 8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P81	52			
P82	51			
P83	50			
P84	49			
P85	48			
P86	47			
P87	46			

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
P90	12	I/O	I/O port 9	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P91	13			
P92	113			
P93	114			
P94	115			
P95	116			
PA0	1	I/O	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PA1	2			
PA2	3			
PA3	4			
PA4	5			
PA5	6			
PA6	7			
PA7	8			
PB0	124	I/O	I/O port B	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up /pull-down resistor for each bit can be selected individually by the PBPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PB1	123			
PB2	122			
PB3	121			
PB4	120			
PB5	119			
PB6	118			
PB7	117			
PC0	23	I/O	I/O port C	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PCDIR register. A pull-up resistor for each bit can be selected individually by the PCPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PC1	24			
PC2	25			
PC3	26			
PC4	27			
PC5	28			
PC6	29			
PD0	87	I/O	I/O port D	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PDDIR register. A pull-up resistor for each bit can be selected individually by the PDPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PD1	86			
PD2	85			
PD3	84			
PD4	83			
PD5	82			
PD6	81			
SBO0A	36	I/O	Serial interface transmission data output pins	Transmission data output pins for serial interface 0, 1, 2, 3, and 4. The output configuration, either COMS push-pull or Nch open-drain can be selected by the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select the output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, and SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBO0B	92			
SBO1A	73			
SBO1B	56			
SBO2A	68			
SBO2B	105			
SBO3A	38			
SBO3B	95			
SBO4A	60			
SBO4B	102			

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
SBI0A	32	I/O	Serial interface reception data input pins	Reception data input pins for serial interface 0, 1, 2, 3, and 4.Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1,SC3MD1, and SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0B	91			
SBI1A	74			
SBI1B	55			
SBI2A	67			
SBI2B	104			
SBI3A	39			
SBI3B	94			
SBI4A	65			
SBI4B	100			
SBT0A	37	I/O	Serial interface clock I/O pins	Clock I/O pins for serial interface 0, 1, 2, 3, and 4. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode or output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, and SC4MD1) according to the communication mode. These can be used as normal I/O pins when the serial interface is not used.
SBT0B	90			
SBT1A	75			
SBT1B	54			
SBT2A	66			
SBT2B	103			
SBT3A	40			
SBT3B	93			
SBT4A	59			
SBT4B	101			
TXD0A	36	Output	UART transmission data output pins	In the serial interface 0, 1, 2, and 3 in UART mode, these pins are configured as the transmission data output pin. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, and SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
TXD0B	92			
TXD1A	73			
TXD1B	56			
TXD2A	68			
TXD2B	105			
TXD3A	38			
TXD3B	95			
RXD0A	32	Input	UART reception data input pins	In the serial interface 0, 1, 2, and 3 in UART mode, these pins are configured as the reception data input pin. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select input mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, and SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0B	91			
RXD1A	74			
RXD1B	55			
RXD2A	67			
RXD2B	104			
RXD3A	39			
RXD3B	94			
SDA4A	60	I/O	IIC data I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the data input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select serial data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4B	102			

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
SCL4A SCL4B	59 101	I/O	IIC clock I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the clock input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select clock data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
OCD_DATA OCD_CLK	30 31	I/O Input	On-board programmer I/O pins	Data I/O pin and clock input pin for the on-board programmer. Refer to Technical Reference Manual. These can be used as normal I/O pins when the on-board programmer is not used.
TM0IOA TM0IOB TM0IOC TM1IOA TM1IOB TM1IOC TM2IOA TM2IOB TM2IOC TM3IOA TM3IOB TM3IOC TM4IOA TM4IOB TM4IOC	1 37 112 2 71 110 3 37 111 4 70 109 5 69 108	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 8-bit timer 0 to 4. To use these pins for event clock input, input mode can be selected by the P0DIR, P1DIR, P6DIR, PADIR, TMCKSEL1, TMINSEL1, and TMINSEL2 registers. In input mode, pull-up resistors can be selected by the P0PLUD, P1PLUD, P6PLU, and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the port 0 output mode register, port 1 output mode register, port 6 output mode register, and port A output mode register (P0OMD, P1OMD, P6OMD, and PAOMD) to select output mode by the P0DIR, P1DIR, P6DIR, and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
BUZZERA NBUZZERA BUZZERB NBUZZERB	80 79 107 106	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to port 1, and port 5. The driving frequency can be set in the DLYCTR register. In order to select buzzer output to port 1 and port 5, select the special function pin in the output mode registers (P1OMD1, P1OMD2, P5OMD), and set the direction control registers (P1DIR, and P5DIR) to the output mode. At the same time, select buzzer output in the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the buzzer output function is not used.
TM7IOA TM7IOB TM7IOC TM8IOA TM8IOB TM8IOC TM9IOA TM9IOB	6 32 107 7 36 106 8 31	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 16-bit timer 7, 8, and 9. To use these pins for event clock input, input mode can be selected by the P0DIR, P1DIR, and PADIR registers. In input mode, pull-up resistors can be selected by the P0PLUD, P1PLUD, and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the output mode registers (P0OMD, P1OMD1, and PAOMD) to select output mode by the direction control registers (P0DIR, P1DIR, and PADIR). These can be used as normal I/O pins when not used as timer I/O pins.

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
TM9OD0A	53	Output	Timer output pins	Timer output and PWM signal output pins for 16-bit timer. To use these pins for timer output or PWM signal output, select special function pins by the output mode registers (P8OMD, and PDOMD) to select output mode by the direction control registers (P8DIR, and PDDIR). These can be used as normal I/O pins when not used as timer output pins.
TM9OD1A	52			
TM9OD2A	51			
TM9OD3A	50			
TM9OD4A	49			
TM9OD5A	48			
TM9OD0B	87			
TM9OD1B	86			
TM9OD2B	85			
TM9OD3B	84			
TM9OD4B	83			
TM9OD5B	82			
SDO0	53	Output	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). To use these pins for synchronous output, set output mode by the P8DIR register. These pins can be used as normal I/O pins when not used as synchronous output pins.
SDO1	52			
SDO2	51			
SDO3	50			
SDO4	49			
SDO5	48			
SDO6	47			
SDO7	46			
V_{REF+}	9	-	Reference power supply pin (+) for A/D converter	Reference power supply pin for the A/D converter. This pin is generally used as $V_{REF+} = V_{DD5}$.
AN0	1	Input	Analog input pins	Analog input pins for 24-channel, 10-bit A/D converter. These pins can be used as normal input pins when not used as analog input pins.
AN1	2			
AN2	3			
AN3	4			
AN4	5			
AN5	6			
AN6	7			
AN7	8			
AN8	124			
AN9	123			
AN10	122			
AN11	121			
AN12	120			
AN13	119			
AN14	118			
AN15	117			
AN16	116			
AN17	115			
AN18	114			
AN19	113			
AN20	112			
AN21	111			
AN22	110			
AN23	109			

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
DA_A	116	Output	Analog output pins	Analog input pins for 4-channel, 8-bit D/A converter. These pins can be used as normal input pins when not used as analog input pins.
DA_B	115			
DA_C	72			
DA_D	40			
IRQ0A	41	Input	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0A to IRQ4A and IRQ0B to IRQ4B can be selected by the IRQnICR register. IRQ0A and IRQ1A are able to determine AC zero cross. Both edge and pin voltage level for IRQ2A, IRQ3A, IRQ4A, IRQ2B, IRQ3B, and IRQ4B are valid for interrupt. These pins can be used as normal input pins when not used as external interrupt pins.
IRQ1A	42			
IRQ2A	43			
IRQ3A	44			
IRQ4A	45			
IRQ0B	23			
IRQ1B	24			
IRQ2B	25			
IRQ3B	26			
IRQ4B	27			
ACZ0	41	Input	AC zero-cross detection input pins	Input pins for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs “High-level” when the input is at an intermediate level. It outputs “Low-level” at all other times. ACZ input signal is connected to the P20 input circuit and the IRQ0A interrupt circuit or the P21 input circuit and the IRQ1A interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as normal input port.
ACZ1	42			
KEY0	65	Input	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. These can be set as key input pins in increments of one bit by the key interrupt control registers (KEYT3_1IMD, KEYT3_2IMD). These pins can be used as normal I/O pins when not used as the key input pins.
KEY1	60			
KEY2	59			
KEY3	58			
KEY4	57			
KEY5	56			
KEY6	55			
KEY7	54			
LED0	30	Output	LED driver pins	Large current output pins. These pins can be used as normal I/O pins when not used as the LED driver pins.
LED1	31			
LED2	32			
LED3	36			
LED4	37			
LED5	38			
LED6	39			
LED7	40			
COM0	52	Output	LCD common output pin	These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal ports by the setting of the LCD output control register (LCCTR0).
COM1	51			
COM2	50			
COM3	49			
V_{LC1}	46	-	LCD power supply pins	Apply voltage of 5.5 V ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ 0 V. When LCD is not used, V_{LC1} to V_{LC3} can be used as normal ports by the setting of the LCD output control register 0 (LCCTR0).
V_{LC2}	47			
V_{LC3}	48			

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
SEG0	53	Output	LCD segment output pins	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD panel. When LCD display is turned off, V_{SS}-level is output. These pins can be used as normal ports by the setting of the LCD output control registers (LCCTR1 to LCCTR7). SEG for each bit can be individually set as a segment pin or a normal port.
SEG1	54			
SEG2	55			
SEG3	56			
SEG4	57			
SEG5	58			
SEG6	59			
SEG7	60			
SEG8	65			
SEG9	66			
SEG10	67			
SEG11	68			
SEG12	69			
SEG13	70			
SEG14	71			
SEG15	72			
SEG16	73			
SEG17	74			
SEG18	75			
SEG19	76			
SEG20	77			
SEG21	78			
SEG22	79			
SEG23	80			
SEG24	88			
SEG25	89			
SEG26	90			
SEG27	91			
SEG28	92			
SEG30	94			
SEG31	95			
SEG32	96			
SEG33	100			
SEG34	101			
SEG35	102			
SEG36	103			
SEG37	104			
SEG38	105			
SEG39	106			
SEG40	107			
SEG41	108			
SEG42	109			
SEG43	110			
SEG44	111			
SEG45	112			
SEG46	113			
SEG47	114			
SEG48	115			
SEG49	116			

(Continue to next page)

KM101EF76K		I/O	Functions	Descriptions
Pins	Pin No.			
SEG50	117		LCD segment output pins	(Continued from previous page)
SEG51	118			
SEG52	119			
SEG53	120			
SEG54	121			
MMOD	18	Input	Memory mode switch input pins	Set to V_{DD5}-level or V_{SS}-level.
DMOD	20	Input	Mode switch input pins	Set always to V_{DD5}-level. Only flash EEPROM version, DMOD contains an internal pull-up resistor.
RON	21	Input	Regulator control pin	When connecting the pull-up resistor with this pin, make it to 200Ω or less. Set always to V_{DD5}-level.

Table: 3.2 Pin Functions (KM101EF57G)

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
V_{SS} V_{DD5}	14 22 17	-	Power supply pins	Supply 1.8 V to 5.5 V to V_{DD5}, and 0 V to V_{SS}. Connect 0.1μF and more than 1 μF of bypass capacitor for internal power stabilization
V_{DD18}	19	-	Internal power output pin	Outputs internal power voltage 1.8 V. Connect 0.1 μF and more than 1 μF of bypass capacitor between V_{DD18} and V_{SS} pins for internal power stabilization.
OSC1	15	Input	High-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for high-speed operation clock. For external clock input, input to OSC1 and open OSC2. The chip will not operate with an external clock when using either STOP mode or SLOW mode
OSC2	16	Output	High-speed operation clock output pin	
XI	12	Input	Low-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for low-speed operation clock. For external clock input, input to XI and open XO. The chip will not operate with an external clock when using STOP mode.
XO	13	Output	Low-speed operation clock output pin	
NRST	11	Input	Reset pin [Active low]	This pin resets the chip at power on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initializes the internal state of the LSI. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an Nch open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD5}.
ATRST	10	Input	Auto reset setting pin	Input “High” to enable auto reset function and “Low” to disable this function.
P00 P01 P02 P03 P04 P05 P06 P07	23 24 25 26 27 28 29 30	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	31 32 33 34 35 15 16	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P27	11	Input	Input port 2	P27 is an Nch open-drain port. When “0” is written and the reset is initiated by software, a low level will be output.
P33 P34 P35	73 72 71	I/O	I/O port 3	3-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
P43 P44 P45 P46 P47	70 69 68 67 66	I/O	I/O port 4	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pulldown resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P50 P51 P52 P53 P54 P55 P56 P57	58 59 60 61 62 63 64 65	I/O	I/O port 5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P62 P63 P64 P65 P66 P67	57 56 55 54 53 52		I/O port 6	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P70 P71 P72 P73 P74 P75 P76 P77	51 50 49 48 47 46 45 44	I/O	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P80 P81 P82 P83 P84 P85 P86 P87	43 42 41 40 39 38 37 36	I/O	I/O port 8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P90 P91 P92 P93 P94	12 13 74 75 76	I/O	I/O port 9	5-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
PA0 PA1 PA2 PA3 PA4 PA5 PA6 PA7	1 2 3 4 5 6 7 8	I/O	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PB0 PB1 PB2 PB3	80 79 78 77	I/O	I/O port B	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up /pull-down resistor for each bit can be selected individually by the PBPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
SBO0A SBO0B SBO1A SBO1B SBO2A SBO4A SBO4B	26 70 58 46 54 50 73	I/O	Serial interface transmission data output pins	Transmission data output pins for serial interface 0, 1, 2, and 4. The output configuration, either COMS push-pull or Nch open-drain can be selected by the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select the output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBI0A SBI0B SBI1A SBI1B SBI2A SBI4A SBI4B	25 69 59 45 53 51 71	I/O	Serial interface reception data input pins	Reception data input pins for serial interface 0, 1, 2, and 4. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBT0A SBT0B SBT1A SBT1B SBT2A SBT4A SBT4B	27 68 60 44 52 49 72	I/O	Serial interface clock I/O pins	Clock I/O pins for serial interface 0, 1, 2, and 4. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode or output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1 to SC4MD1) according to the communication mode. These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1A TXD1B TXD2A	26 70 58 46 54	Output	UART transmission data output pins	In the serial interface 0, 1, 2, and 3 in UART mode, these pins are configured as the transmission data output pin. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, and SC3MD1). These can be used as normal I/O pins when the serial interface is not used.

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
RXD0A RXD0B RXD1A RXD1B RXD2A	25 69 59 45 53	Input	UART reception data input pins	In the serial interface 0, 1, and 2 in UART mode, these pins are configured as the reception data input pin. Pull-up resistor can be selected by the P0PLUD, P4PLUD, 5PLUD, P6PLU, and P7PLUD registers. Select input mode by the P0DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1 to SC2MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4A SDA4B	50 73	I/O	IIC data I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the data input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select serial data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4A SCL4B	49 72	I/O	IIC clock I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the clock input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select clock data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
OCD_DATA OCD_CLK	23 24	I/O Input	On-board programmer I/O pins	Data I/O pin and clock input pin for the on-board programmer. Refer to Technical Reference Manual. These can be used as normal I/O pins when the on-board programmer is not used.
TM0IOA TM0IOB TM1IOA TM1IOB TM2IOA TM2IOB TM3IOA TM3IOB TM4IOA TM4IOB	1 27 2 57 3 27 4 56 5 55	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 8-bit timer 0 to 4. To use these pins for event clock input, input mode can be selected by the P0DIR, P1DIR, P6DIR, PADIR, TMCKSEL1, TMINSEL1, and TMINSEL2 registers. In input mode, pull-up resistors can be selected by the P0PLUD, P1PLUD, P6PLU, and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the port 0 output mode register, port 1 output mode register, port 6 output mode register, and port A output mode register (P0OMD, P1OMD, P6OMD, and PAOMD) to select output mode by the P0DIR, P1DIR, P6DIR, and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
BUZZERA NBUZZERA	65 64	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to port 5. The driving frequency can be set in the DLYCTR register. In order to select buzzer output to port 5, select the special function pin in the port 5 output mode register (P5OMD), and set the P5DIR register to the output mode. At the same time, select buzzer output in the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the buzzer output function is not used.

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
TM7IOA TM7IOB TM8IOA TM8IOB TM9IOA TM9IOB	6 25 7 26 8 24	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 16-bit timer 7, 8, and 9. To use these pins for event clock input, input mode can be selected by the P0DIR and PADIR registers. In input mode, pull-up resistors can be selected by the P0PLUD and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the port A output mode register to select output mode by the P0DIR and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
TM9OD0 TM9OD1 TM9OD2 TM9OD3 TM9OD4 TM9OD5	43 42 41 40 39 38	Output	Timer output pins	Timer output and PWM signal output pins for 16-bit timer. To use these pins for timer output or PWM signal output, select special function pins by the P8OMD register to select output mode by the P8DIR register. These can be used as normal I/O pins when not used as timer output pins.
SDO0 SDO1 SDO2 SDO3 SDO4 SDO5 SDO6 SDO7	43 42 41 40 39 38 37 36	Output	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). To use these pins for synchronous output, set output mode by the P8DIR register. These pins can be used as normal I/O pins when not used as synchronous output pins.
V_{REF+}	9	-	Reference power supply pin (+) for A/D converter	Reference power supply pin for the A/D converter. This pin is generally used as $V_{REF+} = V_{DD5}$.
AN0 AN1 AN2 AN3 AN4 AN5 AN6 AN7 AN8 AN9 AN10 AN11 AN12 AN13 AN14 AN15	1 2 3 4 5 6 7 8 80 79 78 77 76 75 74 73	Input	Analog input pins	Analog input pins for 16-channel, 10-bit A/D converter. These pins can be used as normal input pins when not used as analog input pins.
DA_A DA_B	76 30	Output	Analog output pins	Analog input pins for 2-channel, 8-bit D/A converter. These pins can be used as normal input pins when not used as analog input pins.
IRQ0 IRQ1 IRQ2 IRQ3 IRQ4	31 32 33 34 35	Input	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to 4 can be selected by the IRQnICR register. IRQ0, 1 are able to determine AC zero cross. Both edge and pin voltage level for IRQ2, 3, 4 are valid for interrupt. These pins can be used as normal input pins when not used as external interrupt pins.

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
ACZ0 ACZ1	31 32	Input	AC zero-cross detection input pins	Input pins for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs “High-level” when the input is at an intermediate level. It outputs “Low-level” at all other times. ACZ input signal is connected to the P20 input circuit and the IRQ0 interrupt circuit or the P21 input circuit and the IRQ1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as normal input port.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	51 50 49 48 47 46 45 44	Input	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. These can be set as key input pins in increments of one bit by the key interrupt control registers (KEYT3_1IMD, KEYT3_2IMD). These pins can be used as normal I/O pins when not used as the key input pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	23 24 25 26 27 28 29 30	Output	LED driver pins	Large current output pins. These pins can be used as normal I/O pins when not used as the LED driver pins.
COM0 COM1 COM2 COM3	42 41 40 39	Output	LCD common output pin	These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal ports by the setting of the LCD output control register (LCCTR0).
V_{LC1} V_{LC2} V_{LC3}	36 37 38	-	LCD power supply pins	Apply voltage of 5.5 V ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ 0 V. When LCD is not used, V_{LC1} to V_{LC3} can be used as normal ports by the setting of the LCD output control register 0 (LCCTR0).

KM101EF57G		I/O	Functions	Descriptions
Pins	Pin No.			
SEG0	43	Output	LCD segment output pins	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD panel. When LCD display is turned off, V_{SS}-level is output. These pins can be used as normal ports by the setting of the LCD output control registers (LCCTR1 to LCCTR7). SEG for each bit can be individually set as a segment pin or a normal port.
SEG1	44			
SEG2	45			
SEG3	46			
SEG4	47			
SEG5	48			
SEG6	49			
SEG7	50			
SEG8	51			
SEG9	52			
SEG10	53			
SEG11	54			
SEG12	55			
SEG13	56			
SEG14	57			
SEG15	58			
SEG16	59			
SEG17	60			
SEG18	61			
SEG19	62			
SEG20	63			
SEG21	64			
SEG22	65			
SEG23	66			
SEG24	67			
SEG25	68			
SEG26	69			
SEG27	70			
SEG28	71			
SEG29	72			
SEG30	73			
SEG31	74			
SEG32	75			
SEG33	76			
SEG34	77			
SEG35	78			
SEG36	79			
SEG37	80			
SEG38	1			
SEG39	2			
SEG40	3			
MMOD	18	Input	Memory mode switch input pins	Set to V_{DD5}-level or V_{SS}-level.
DMOD	20	Input	Mode switch input pins	Set always to V_{DD5}-level. Only flash EEPROM version, DMOD contains an internal pull-up resistor.
RON	21	Input	Regulator control pin	When connecting the pull-up resistor with this pin, make it to 200Ω or less. Set always to V_{DD5}-level.

Table: 3.3 Pin Functions (KM101EF56K)

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
V_{SS} V_{DD5}	14, 22 17	-	Power supply pins	Supply 1.8 V to 5.5 V to V_{DD5}, and 0 V to V_{SS}. Connect 0.1μF and more than 1 μF of bypass capacitor for internal power stabilization
V_{DD18}	19	-	Internal power output pin	Outputs internal power voltage 1.8 V. Connect 0.1 μF and more than 1 μF of bypass capacitor between V_{DD18} and V_{SS} pins for internal power stabilization.
OSC1	15	Input	High-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for high-speed operation clock. For external clock input, input to OSC1 and open OSC2. The chip will not operate with an external clock when using either STOP mode or SLOW mode
OSC2	16	Output	High-speed operation clock output pin	
XI	12	Input	Low-speed operation clock input pin	Connect these oscillation pins to ceramic oscillator or crystal oscillator for low-speed operation clock. For external clock input, input to XI and open XO. The chip will not operate with an external clock when using STOP mode.
XO	13	Output	Low-speed operation clock output pin	
NRST	11	Input	Reset pin [Active low]	This pin resets the chip at power on, is allocated as P27 and contains an internal pull-up resistor (Typ. 50 kΩ). Setting this pin low initializes the internal state of the LSI. Thereafter, setting the input to high releases the reset. The hardware waits for the system clock to stabilize, then processes the reset interrupt. Also, if “0” is written to P27 and the reset is initiated by software, a low level will be output. The output has an Nch open-drain configuration. If a capacitor is to be inserted between NRST and V_{SS}, it is recommended that a discharge diode be placed between NRST and V_{DD5}.
ATRST	10	Input	Auto reset setting pin	Input “High” to enable auto reset function and “Low” to disable this function.
P00 P01 P02 P03 P04 P05 P06 P07	23 24 25 26 27 28 29 30	I/O	I/O port 0	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P0DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P0PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P10 P11 P12 P13 P14 P15 P16	88 87 86 85 84 83 82	I/O	I/O port 1	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P1DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P1PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P20 P21 P22 P23 P24 P25 P26	31 32 33 34 35 15 16	I/O	I/O port 2	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P2DIR register. A pull-up resistor for each bit can be selected individually by the P2PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P27	11	Input	Input port 2	P27 is an Nch open-drain port. When “0” is written and the reset is initiated by software, a low level will be output.

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
P30	81	I/O	I/O port 3	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P3DIR register. A pull-up resistor for each bit can be selected individually by the P3PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P31	80			
P32	79			
P33	78			
P34	77			
P35	76			
P36	75			
P40	74	I/O	I/O port 4	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P4DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P4PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (However, pull-up and pull-down resistors cannot be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P41	73			
P42	72			
P43	71			
P44	70			
P45	69			
P46	68			
P47	67			
P50	59	I/O	I/O port 5	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P5DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P5PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P51	60			
P52	61			
P53	62			
P54	63			
P55	64			
P56	65			
P57	66			
P61	58	I/O	I/O port 6	7-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P6DIR register. A pull-up resistor for each bit can be selected individually by the P6PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P62	57			
P63	56			
P64	55			
P65	54			
P66	53			
P67	52			
P70	51	I/O	I/O port 7	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P7DIR register. A pull-up /pull-down resistor for each bit can be selected individually by the P7PLUD register. A pull-up/down resistor connection for each port can be selected individually by the SELUD register. (A pull-up/pull down can not be mixed.) At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P71	50			
P72	49			
P73	48			
P74	47			
P75	46			
P76	45			
P77	44			
P80	43	I/O	I/O port 8	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P8DIR register. A pull-up resistor for each bit can be selected individually by the P8PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P81	42			
P82	41			
P83	40			
P84	39			
P85	38			
P86	37			
P87	36			

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
P90	12	I/O	I/O port 9	6-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the P9DIR register. A pull-up resistor for each bit can be selected individually by the P9PLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
P91	13			
P92	89			
P93	90			
P94	91			
P95	92			
PA0	1	I/O	I/O port A	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PADIR register. A pull-up resistor for each bit can be selected individually by the PAPLU register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PA1	2			
PA2	3			
PA3	4			
PA4	5			
PA5	6			
PA6	7			
PA7	8			
PB0	100	I/O	I/O port B	8-bit CMOS tri-state I/O port. Each bit can be set individually as either an input or output by the PBDIR register. A pull-up /pull-down resistor for each bit can be selected individually by the PBPLUD register. At reset, the input mode is selected and pull-up resistors are disabled (high impedance).
PB1	99			
PB2	98			
PB3	97			
PB4	96			
PB5	95			
PB6	94			
PB7	93			
SBO0A	26	I/O	Serial interface transmission data output pins	Transmission data output pins for serial interface 0, 1, 2, 3, and 4. The output configuration, either COMS push-pull or Nch open-drain can be selected by the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select the output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, and SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SBO0B	71			
SBO1A	59			
SBO1B	46			
SBO2A	54			
SBO2B	81			
SBO3A	28			
SBO3B	74			
SBO4A	50			
SBO4B	78			
SBI0A	25	I/O	Serial interface reception data input pins	Reception data input pins for serial interface 0, 1, 2, 3, and 4. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1,SC3MD1, and SC4MD1) These can be used as normal I/O pins when the serial interface is not used.
SBI0B	70			
SBI1A	60			
SBI1B	45			
SBI2A	53			
SBI2B	80			
SBI3A	29			
SBI3B	73			
SBI4A	51			
SBI4B	76			

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
SBT0A SBT0B SBT1A SBT1B SBT2A SBT2B SBT3A SBT3B SBT4A SBT4B	27 69 61 44 52 79 30 72 49 77	I/O	Serial interface clock I/O pins	Clock I/O pins for serial interface 0, 1, 2, 3, and 4. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU and P7PLUD registers. Select input mode or output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers and serial data output mode by serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, SC3MD1, and SC4MD1) according to the communication mode. These can be used as normal I/O pins when the serial interface is not used.
TXD0A TXD0B TXD1A TXD1B TXD2A TXD2B TXD3A TXD3B	26 71 59 46 54 81 28 74	Output	UART transmission data output pins	In the serial interface 0, 1, 2, and 3 in UART mode, these pins are configured as the transmission data output pin. The output configuration, either CMOS push-pull or Nch open-drain can be selected with the P0ODC, P3ODC, P4ODC, P5ODC, P6ODC, and P7ODC registers. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select output mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data output by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, and SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
RXD0A RXD0B RXD1A RXD1B RXD2A RXD2B RXD3A RXD3B	25 70 60 45 53 80 29 73	Input	UART reception data input pins	In the serial interface 0, 1, 2, and 3 in UART mode, these pins are configured as the reception data input pin. Pull-up resistor can be selected by the P0PLUD, P3PLU, P4PLUD, P5PLUD, P6PLU, and P7PLUD registers. Select input mode by the P0DIR, P3DIR, P4DIR, P5DIR, P6DIR and P7DIR registers to select serial data input by the serial mode register 1 (SC0MD1, SC1MD1, SC2MD1, and SC3MD1). These can be used as normal I/O pins when the serial interface is not used.
SDA4A SDA4B	50 78	I/O	IIC data I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the data input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select serial data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
SCL4A SCL4B	49 77	I/O	IIC clock I/O pins	In the serial interface 4 in IIC mode, these pins are configured as the clock input / output pin. For the output configuration, select Nch open-drain by the P3ODC and P7ODC register to select pull-up resistor by the P3PLU and P7PLUD register. Select output mode by the P3DIR and P7DIR register to select clock data input / output by the serial mode register 1 (SC4MD1). These can be used as normal I/O pins when the serial interface is not used.
OCD_DATA OCD_CLK	23 24	I/O Input	On-board programmer I/O pins	Data I/O pin and clock input pin for the on-board programmer. Refer to Technical Reference Manual. These can be used as normal I/O pins when the on-board programmer is not used.

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
TM0IOA	1	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 8-bit timer 0 to 4. To use these pins for event clock input, input mode can be selected by the P0DIR, P1DIR, P6DIR, PADIR, TMCKSEL1, TMINSEL1, and TMINSEL2 registers. In input mode, pull-up resistors can be selected by the P0PLUD, P1PLUD, P6PLU, and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the port 0 output mode register, port 1 output mode register, port 6 output mode register, and port A output mode register (P0OMD, P1OMD, P6OMD, and PAOMD) to select output mode by the P0DIR, P1DIR, P6DIR, and PADIR registers. These can be used as normal I/O pins when not used as timer I/O pins.
TM0IOB	27			
TM0IOC	88			
TM1IOA	2			
TM1IOB	57			
TM1IOC	86			
TM2IOA	3			
TM2IOB	27			
TM2IOC	87			
TM3IOA	4			
TM3IOB	56			
TM3IOC	85			
TM4IOA	5			
TM4IOB	55			
TM4IOC	84			
BUZZERA	66	Output	Buzzer output pins	Piezoelectric buzzer driving pin. Buzzer output is available to port 1, and port 5. The driving frequency can be set in the DLYCTR register. In order to select buzzer output to port 1 and port 5, select the special function pin in the output mode registers (P1OMD1, P1OMD2, P5OMD), and set the direction control registers (P1DIR, and P5DIR) to the output mode. At the same time, select buzzer output in the oscillation stabilization wait control register (DLYCTR). These can be used as normal I/O pins when the buzzer output function is not used.
NBUZZERA	65			
BUZZERB	83			
NBUZZERB	82			
TM7IOA	6	I/O	Timer I/O pins	Event count clock input, timer output, and PWM signal output pins for 16-bit timer 7, 8, and 9. To use these pins for event clock input, input mode can be selected by the P0DIR, P1DIR, and PADIR registers. In input mode, pull-up resistors can be selected by the P0PLUD, P1PLUD, and PAPLU register. To use these pins for timer output or PWM signal output, select special function pins by the output mode registers (P0OMD, P1OMD1, and PAOMD) to select output mode by the direction control registers (P0DIR, P1DIR, and PADIR). These can be used as normal I/O pins when not used as timer I/O pins.
TM7IOB	25			
TM7IOC	83			
TM8IOA	7			
TM8IOB	26			
TM8IOC	82			
TM9IOA	8			
TM9IOB	24			
TM9OD0	43	Output	Timer output pins	Timer output and PWM signal output pins for 16-bit timer. To use these pins for timer output or PWM signal output, select special function pins by the output mode registers (P8OMD, and PDOMD) to select output mode by the direction control registers (P8DIR, and PDDIR). These can be used as normal I/O pins when not used as timer output pins.
TM9OD1	42			
TM9OD2	41			
TM9OD3	40			
TM9OD4	39			
TM9OD5	38			

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
SDO0	43	Output	Synchronous output pins	8-bit synchronous output pins. Synchronous output for each bit can be selected individually by the port 8 synchronous output control register (P8SYO). To use these pins for synchronous output, set output mode by the P8DIR register. These pins can be used as normal I/O pins when not used as synchronous output pins.
SDO1	42			
SDO2	41			
SDO3	40			
SDO4	39			
SDO5	38			
SDO6	37			
SDO7	36			
V_{REF+}	9	-	Reference power supply pin (+) for A/D converter	Reference power supply pin for the A/D converter. This pin is generally used as $V_{REF+} = V_{DD5}$.
AN0	1	Input	Analog input pins	Analog input pins for 24-channel, 10-bit A/D converter. These pins can be used as normal input pins when not used as analog input pins.
AN1	2			
AN2	3			
AN3	4			
AN4	5			
AN5	6			
AN6	7			
AN7	8			
AN8	100			
AN9	99			
AN10	98			
AN11	97			
AN12	96			
AN13	95			
AN14	94			
AN15	93			
AN16	92			
AN17	91			
AN18	90			
AN19	89			
AN20	88			
AN21	87			
AN22	86			
AN23	85			
DA_A	92	Output	Analog output pins	Analog input pins for 4-channel, 8-bit D/A converter. These pins can be used as normal input pins when not used as analog input pins.
DA_B	91			
DA_C	58			
DA_D	30			
IRQ0	31	Input	External interrupt input pins	External interrupt input pins. The valid edge for IRQ0 to IRQ4 can be selected by the IRQnICR register. IRQ0 and IRQ1 are able to determine AC zero cross. Both edge and pin voltage level for IRQ2, IRQ3 and IRQ4 are valid for interrupt. These pins can be used as normal input pins when not used as external interrupt pins.
IRQ1	32			
IRQ2	33			
IRQ3	34			
IRQ4	35			

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
ACZ0 ACZ1	31 32	Input	AC zero-cross detection input pins	Input pins for an AC zero-cross detection circuit. The AC zero-cross detection circuit outputs “High-level” when the input is at an intermediate level. It outputs “Low-level” at all other times. ACZ input signal is connected to the P20 input circuit and the IRQ0 interrupt circuit or the P21 input circuit and the IRQ1 interrupt circuit. When the AC zero-cross detection circuit is not used, this pin can be used as normal input port.
KEY0 KEY1 KEY2 KEY3 KEY4 KEY5 KEY6 KEY7	51 50 49 48 47 46 45 44	Input	Key interrupt input pins	Input pins for interrupt based on ORed result of pin inputs. These can be set as key input pins in increments of one bit by the key interrupt control registers (KEYT3_1IMD, KEYT3_2IMD). These pins can be used as normal I/O pins when not used as the key input pins.
LED0 LED1 LED2 LED3 LED4 LED5 LED6 LED7	23 24 25 26 27 28 29 30	Output	LED driver pins	Large current output pins. These pins can be used as normal I/O pins when not used as the LED driver pins.
COM0 COM1 COM2 COM3	42 41 40 39	Output	LCD common output pin	These pins output common signal of required timing for LCD display. Connect to the common pins of LCD display panel. When the LCD functions are not used, these pins can be used as normal ports by the setting of the LCD output control register (LCCTR0).
V_{LC1} V_{LC2} V_{LC3}	36 37 38	-	LCD power supply pins	Apply voltage of 5.5 V ≥ V_{LC1} ≥ V_{LC2} ≥ V_{LC3} ≥ 0 V. When LCD is not used, V_{LC1} to V_{LC3} can be used as normal ports by the setting of the LCD output control register 0 (LCCTR0).
SEG0 SEG1 SEG2 SEG3 SEG4 SEG5 SEG6 SEG7 SEG8 SEG9 SEG10 SEG11 SEG12 SEG13 SEG14 SEG15	43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58	Output	LCD segment output pins	These pins output segment signal of required timing for LCD display. Connect to the segment pins of the LCD panel. When LCD display is turned off, V_{SS}-level is output. These pins can be used as normal ports by the setting of the LCD output control registers (LCCTR1 to LCCTR7). SEG for each bit can be individually set as a segment pin or a normal port.

(Continue to next page)

KM101EF56K		I/O	Functions	Descriptions
Pins	Pin No.			
SEG16	59	Output	LCD segment output pins	(Continued from previous page)
SEG17	60			
SEG18	61			
SEG19	62			
SEG20	63			
SEG21	64			
SEG22	65			
SEG23	66			
SEG24	67			
SEG25	68			
SEG26	69			
SEG27	70			
SEG28	71			
SEG29	72			
SEG30	73			
SEG31	74			
SEG32	75			
SEG33	76			
SEG34	77			
SEG35	78			
SEG36	79			
SEG37	80			
SEG38	81			
SEG39	82			
SEG40	83			
SEG41	84			
SEG42	85			
SEG43	86			
SEG44	87			
SEG45	88			
SEG46	89			
SEG47	90			
SEG48	91			
SEG49	92			
SEG50	93			
SEG51	94			
SEG52	95			
SEG53	96			
SEG54	97			
MMOD	18	Input	Memory mode switch input pins	Set to V_{DD5}-level or V_{SS}-level.
DMOD	20	Input	Mode switch input pins	Set always to V_{DD5}-level. Only flash EEPROM version, DMOD contains an internal pull-up resistor.
RON	21	Input	Regulator control pin	When connecting the pull-up resistor with this pin, make it to 200Ω or less. Set always to V_{DD5}-level.

4. Block Diagram

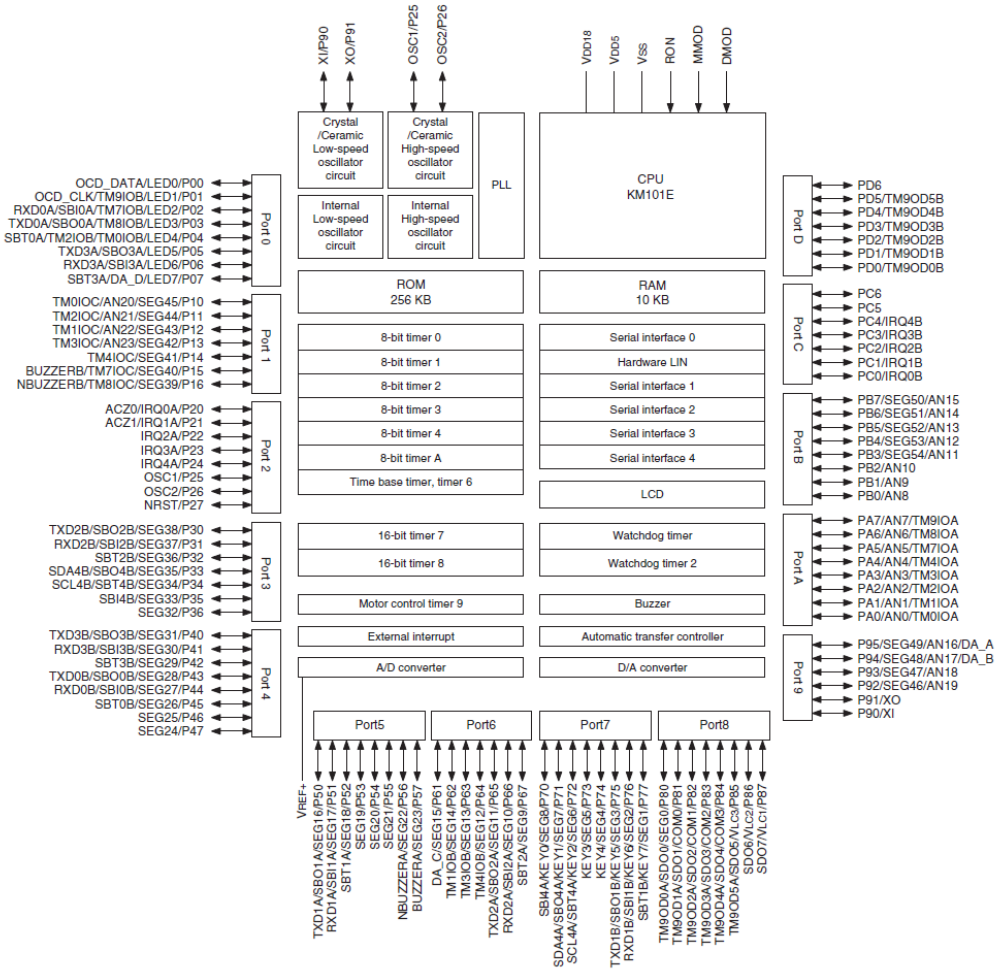


Figure: 4.1 Block Diagram (KM101EF76K)

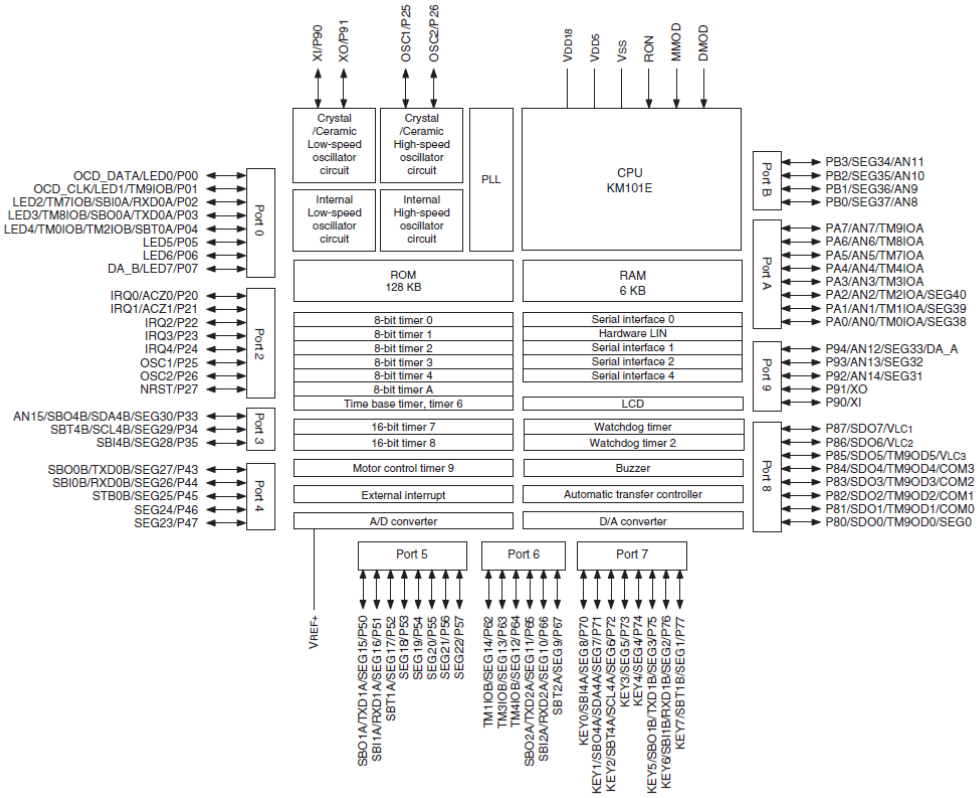


Figure: 4.2 Block Diagram (KM101EF57G)

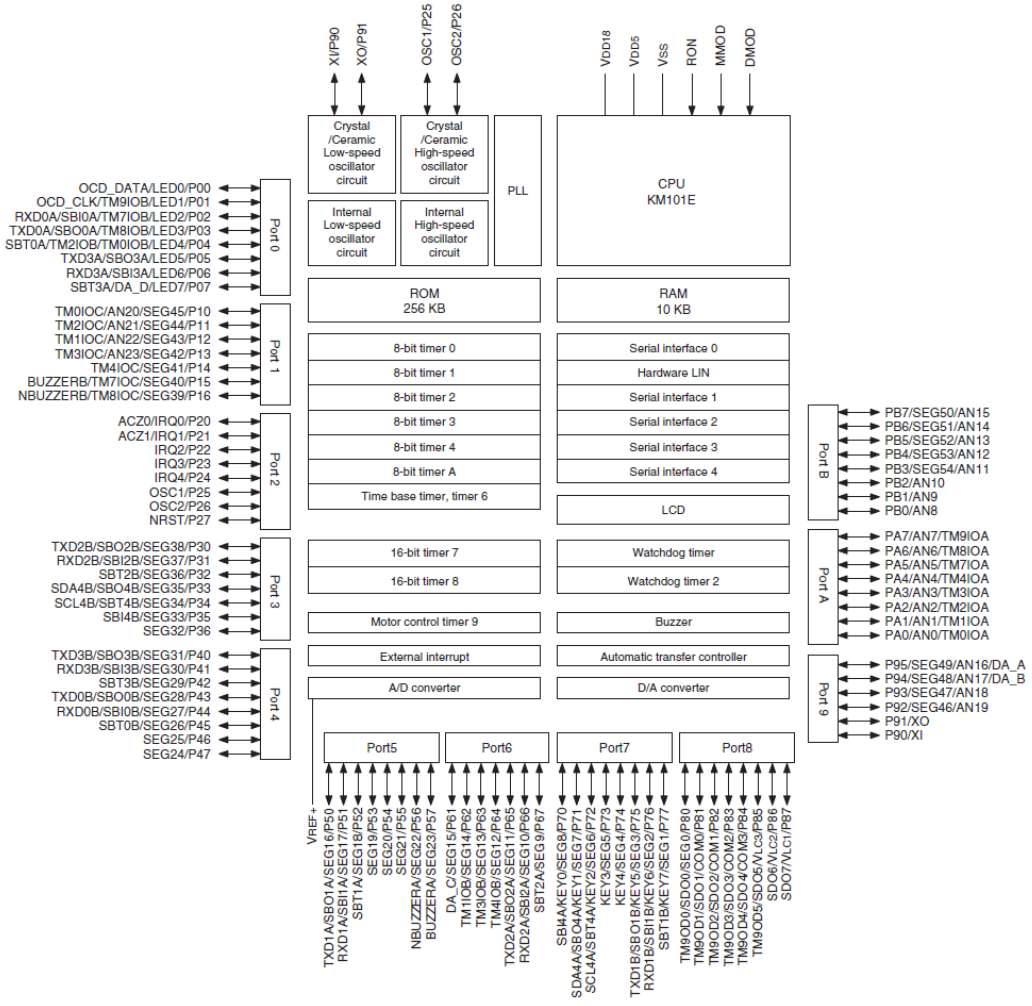


Figure: 4.3 Block Diagram (KM101EF56K)

5. Electrical Characteristics

This manual describes standard specifications.
When using this LSI, consult our sales offices for the product specifications.

Structure	CMOS integrated circuit
Application	General-purpose
Function	CMOS 8-bit single chip microcontroller

5.1 Absolute Maximum Ratings

A. Absolute Maximum Ratings *2 *3 *4

V_{SS} = 0 V

Parameter			Symbol	Rating	Unit
A1	Power supply voltage		V_{DD5}	-0.3 to +7.0	V
A2	Power supply voltage		V_{DD18}	-0.3 to +2.5	
A3	Input clamp current (ACZ)		I_C	-500 to +500	μA
A4	Input pin voltage		V_I	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	V
A5	Output pin voltage		V_O	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	
A6	I/O pin voltage		V_{IO1}	-0.3 to V_{DD5} +0.3 (upper limit 7.0 V)	
A7	Peak output current	LED output	I_{OL1} (peak)	30	mA
A8		Other than LED output	I_{OL2} (peak)	20	
A9		All pins	I_{OH} (peak)	-10	
A10	Average output current *1	LED output	I_{OL1} (avg)	20	
A11		Other than LED output	I_{OL2} (avg)	15	
A12		All pins	I_{OH} (avg)	-5	
A13	Power dissipation		P_T	400	mW
A14	Operating ambient temperature		T_{opr}	-40 to +85	°C
A15	Storage temperature		T_{STG}	-55 to +125	

*1 Applied to any 100 ms period.

*2 Connect at least one bypass capacitor of 1.0 μF or larger between V_{DD5} pin and GND for the internal power voltage stabilization.

*3 Connect appropriate 0.1 μF or 1.0 μF capacitor between V_{DD18} pin and V_{SS} pin, near the microcontroller according to the figure shown belowfor the internal power supply stabilization.

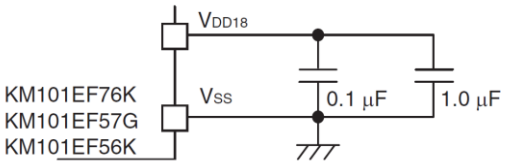


Figure: 5.1 Capacitor Connection between V_{DD18} and V_{SS} Pins

*4 The absolute maximum ratings are the limit values beyond which the LSI may be damaged.

5.2 Operating Conditions

B. Operating Conditions

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Power supply voltage *5						
B1	Power supply voltage	V_{DD1}	fs ≤ 20 MHz *7	2.7		5.5	V
B2		V_{DD2}	fs ≤ 10 MHz *8	2.7		5.5	
B3		V_{DD3}	fs ≤ 8 MHz *7	1.8		5.5	
B4		V_{DD4}	fs ≤ 8 MHz *7, *9	2.0		5.5	
B5		V_{DD5}	fs ≤ 4 MHz *8	1.8		5.5	
B6		V_{DD6}	fs ≤ 4 MHz *8, *10	2.0		5.5	
B7		V_{DD7}	fs = 16.384 kHz	1.8		5.5	
B8	RAM retention power supply voltage	V_{DD8}	During STOP mode	1.8		5.5	
Operating speed *6							
B9	Instruction execution time fs	t_{c1}	V_{DD5} = 2.7 V to 5.5 V *7	0.05			µs
B10		t_{c2}	V_{DD5} = 2.7 V to 5.5 V *8	0.10			
B11		t_{c3}	V_{DD5} = 1.8 V to 5.5 V *7	0.125			
B12		t_{c4}	V_{DD5} = 2.0 V to 5.5 V *7, *9	0.125			
B13		t_{c5}	V_{DD5} = 1.8 V to 5.5 V *8	0.25			
B14		t_{c6}	V_{DD5} = 2.0 V to 5.5 V *8, *10	0.25			
B15		t_{c7}	V_{DD5} = 1.8 V to 5.5 V	61			

*5 fs : Machine clock frequency

*6 tc1 to 2 : when the machine clock is selected from external high-speed oscillation, internal high-speed oscillation, or both the oscillations multiplied by PLL.
tc3 : when the machine clock is selected from external high-speed oscillation or internal high-speed oscillation.

*7 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b1”

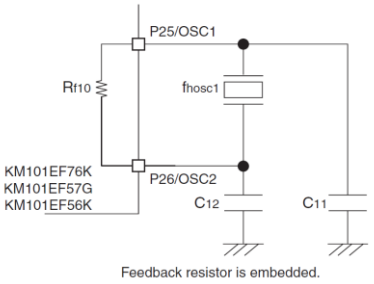
*8 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b0”

*9 When setting frc=16 MHz, fs=frc/2

*10 When setting frc=16 MHz, fs=frc/4

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
External Oscillator 1 Figure: 5.2						
B16 Frequency	f_{hosc1}	V_{DD5} is within the specified operating power supply voltage range. (Refer to the ratings B1 to B6 for the specified operating power supply voltage range)	2.0		10	MHz
B17 Internal feedback resistor	R_{f10}	V_{DD5} = 5.0 V		980		kΩ
External Oscillator 2 Figure: 5.3						
B18 Frequency	f_{sosc1}	V_{DD5} = 1.8 V to 5.5 V		32.768		kHz
B19 Internal feedback resistor	R_{f20}	V_{DD5} = 5.0 V		6.2		MΩ



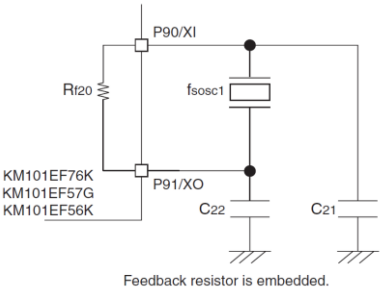


Figure: 5.2 External Oscillator 1 Figure: 5.3 External Oscillator 2

Connect external capacitors suited for the used oscillator.
The reference value denotes external capacity value based on our matching result.
When crystal oscillator or ceramic oscillator is used, the oscillation frequency is changed depending on the value of capacitor. For external capacity value, please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
External clock input 1 OSC1 (OSC2 is unconnected)							
B20	Clock frequency	f_{hosc2}		2		10.0	MHz
B21	High-level pulse width *11	t_{wh1}	Figure: 5.4	45			ns
B22	Low-level pulse width *11	t_{wl1}		45			
B23	Rising time *12	t_{wr1}	Figure: 5.4	0		5.0	
B24	Falling time *12	t_{wf1}		0		5.0	
External clock input 2 XI (XO is unconnected)							
B25	Clock frequency	f_{sosc2}			32.768		kHz
B26	High-level pulse width *11	t_{wh2}	Figure: 5.5		4.5		ns
B27	Low-level pulse width *11	t_{wl2}			4.5		
B28	Rising time *12	t_{wr2}	Figure: 5.5	0		20	
B29	Falling time *12	t_{wf2}		0		20	

*11 The clock duty ratio should be 45% to 55%

*12 Rising time and falling time differ depending on the oscillation frequency.
The max value is not a specified value but a rough value.
Please consult the oscillator manufacturer and perform matching tests enough for determining appropriate values.

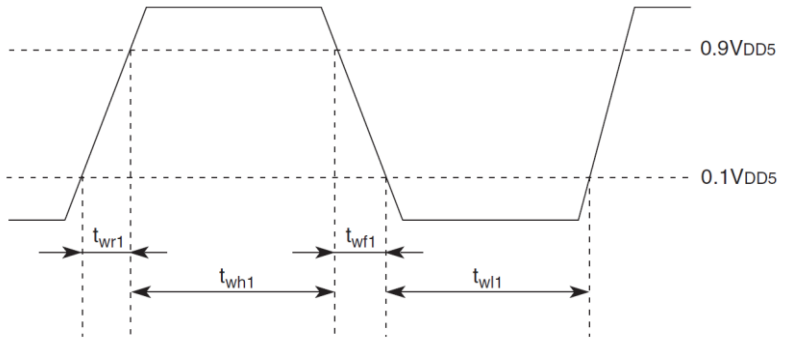


Figure: 5.4 OSC1 Timing Chart

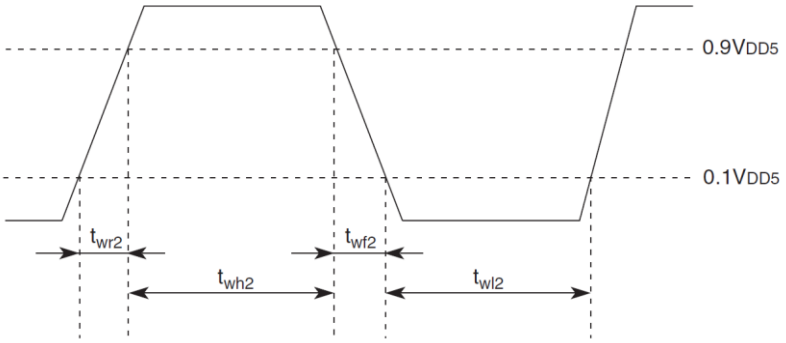


Figure: 5.5 XI Timing Chart

5.3 DC Characteristics

C. DC Characteristics

V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	KM101EF76K KM101EF56K			KM101EF57G			Unit
				Rating			Rating			
				MIN	TYP	MAX	MIN	TYP	MAX	
Power supply current *13										
C1	Power supply current during operation	I_{DD1}	fosc=10 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (PLL is not used) *14		5.2	14.4		5	14	mA
C2		I_{DD2}	fosc=10 MHz [Double-speed mode:fs=fosc] V_{DD5}=3 V (PLL is not used) *14		5.7			5.5		
C3		I_{DD3}	fosc=8 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (PLL is not used) *14		4.7	13.4		4.5	13	
C4		I_{DD4}	fosc=8 MHz [Double-speed mode:fs=fosc] V_{DD5}=3 V (PLL is not used) *14		4.7			4.5		
C5		I_{DD5}	fosc=4 MHz [Double-speed mode:fs=fosc] V_{DD5}=5 V (PLL is not used) *15		3.7	11.4		3.5	11	
C6		I_{DD6}	fosc=4 MHz [Double-speed mode:fs=fosc] V_{DD5}=3 V (PLL is not used) *15		3.7			3.5		
C7		I_{DD7}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] V_{DD5}=5 V (PLL is used) *14		8.2	18.4		8	18	
C8		I_{DD8}	fosc=4 MHz [Multiplied by 10:fs=20 MHz] V_{DD5}=3 V (PLL is used) *14		9.2			9		
C9		I_{DD9}	frc=20 MHz [Double-speed mode:fs=frc] V_{DD5}=5 V (PLL is not used) *14		7.7	16.4		7.5	16	
C10		I_{DD10}	frc=20 MHz [Double-speed mode:fs=frc] V_{DD5}=3 V (PLL is not used) *14		8.7			8.5		
C11		I_{DD11}	frcs=30 kHz [fs=frcs/2] V_{DD5}=3 V Ta=25 °C ROM is executed.		75	90		50	65	μA
C12			frcs=30 kHz [fs=frcs/2] V_{DD5}=3 V Ta=85 °C ROM is executed.			250			150	
C13		I_{DD12}	frcs=30 kHz [fs=frcs/2] V_{DD5}=3 V Ta=25 °C RAM is executed. *16		10	25		10	25	
C14			frcs=30 kHz [fs=frcs/2] V_{DD5}=3 V Ta=85 °C RAM is executed. *16			65			65	
C15	Power supply current during HALT1	I_{DD13}	frcs=30 kHz, V_{DD5}=3 V Ta=25 °C		6	15		6	15	
C16			frcs=30 kHz, V_{DD5}=3 V Ta=85 °C			60			55	
C17	Power supply current during STOP	I_{DD14}	V_{DD5}=5 V, Ta=25 °C		1	5		1	5	
C18			V_{DD5}=5 V, Ta=85 °C			45			40	

*13 Measured without loading (pull-up and pull-down resistors are not connected.)

To measure the power supply current in operation I_{DD1} to I_{DD10}:
1. Set the all I/O pins to input mode.
2. Set the CPU mode to <NORMAL>.
3. Fix the MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.
4. And input the square wave of 10 MHz (8 MHz, 4 MHz), which has amplitude of V_{DD5} and V_{SS} potential, from the OSCI1 pin.

To measure the power supply current in operation I_{DD11},and I_{DD12}:
1. Set the all I/O pins to input mode.
2. Set the CPU mode to <SLOW>.
3. Fix the MMOD pin at V_{SS}-level and input pin at V_{DD5}-level. Clock is supplied from the internal low-speed oscillation circuit.

To measure the power supply current in HALT1 mode I_{DD13}:
1. Set the all I/O pins to input mode.
2. Set the CPU mode to <HALT1>.
3. And fix the MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.

To measure the power supply current in STOP mode I_{DD14}:
1. Set the CPU mode to <STOP>.
2. Fix the MMOD pin at V_{SS}-level and input pin at V_{DD5}-level.
3. And open the OSC1 pin.

*14 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b1”

*15 When bp2 of the HANDSHAKE register (0x03F06) is set to “1'b0”

*16 When bp3 of the FEWSPD register (0x03FBF) to “1'b1”

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Input pin 1 RON						
C19 Input high voltage	V_{IH1}		0.8V_{DD5}		V_{DD5}	V
C20 Input low voltage	V_{IL1}		0		0.2V_{DD5}	
Input pin 2 ATRST, MMOD						
C21 Input high voltage	VI_{H2}		0.8V_{DD5}		V_{DD5}	V
C22 Input low voltage	V_{IL2}		0		0.2V_{DD5}	
C23 Input leakage current	I_{LK1}	VIN = 0 V to VDD5			± 2	µA
Input pin 3 DMOD *17						
C24 Input high voltage	V_{IH3}		0.8V_{DD5}		V_{DD5}	V
C25 Input low voltage	V_{IL3}		0		0.2V_{DD5}	
C26 Pull-up resistor	R_{RH1}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
Input pin 4 P27/NRST						
C27 Input high voltage	V_{IH4}		0.8V_{DD5}		V_{DD5}	V
C28 Input low voltage	V_{IL4}		0		0.2V_{DD5}	
C29 Pull-up resistor	R_{RH2}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
I/O pin 1 P00 to P07						
C30 Input high voltage	V_{IH5}		0.8V_{DD5}		V_{DD5}	V
C31 Input low voltage	V_{IL5}	Flash option = select port input voltage level A	0		0.2V_{DD5}	
C32 Input low voltage	V_{IL6}	Flash option = select port input voltage level B V_{DD5} = 4.5 V to 5.5 V	0		0.45V_{DD5}	
C33 Input leakage current	I_{LK2}	V_{IN} = 0 V to V_{DD5}			± 2	µA
C34 Pull-up resistor	R_{RH3}	V_{DD5} = 5 V , V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C35 Pull-down resistor	R_{RL1}	V_{DD5} = 5 V , V_{IN} = V_{DD5} Pull-down resistor ON	10	50	100	
C36 Output high voltage	V_{OH1}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C37 Output low voltage 1	V_{OL1}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA LED output OFF			0.5	
C38 Output low voltage 2	V_{OL2}	V_{DD5} = 5.0 V, I_{OL} = 15.0 mA LED output ON			1.0	

*17 DMOD internal pull-up resistor is in only Flash EEPROM version.
When using In-circuit Emulator, it is necessary to connect the pull-up resistor on the circuit board.

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	

I/O pin 2
KM101EF76K: P20 to P26, P33 to P36, P61 to P67, P80 to P87, P90 to P95, PB0 to PB7
KM101EF57G: P20 to P26, P33 to P35, P62 to P67, P80 to P87, P90 to P94, PB0 to PB3
KM101EF56K: P20 to P26, P33 to P36, P61 to P67, P80 to P87, P90 to P95, PB0 to PB7

C39	Input high voltage	V_{IH6}		0.8V_{DD5}		V_{DD5}	V
C40	Input low voltage	V_{IL7}	Flash option = select port input voltage level A	0		0.2V_{DD5}	
C41	Input low voltage	V_{IL8}	Flash option = select port input voltage level B V_{DD5} = 4.5 V to 5.5 V	0		0.45V_{DD5}	
C42	Input leakage current	I_{LK3}	V_{IN} = 0 V to V_{DD5}			± 2	µA
C43	Pull-up resistor	R_{RH4}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C44	Output high voltage	V_{OH2}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C45	Output low voltage 1	V_{OL3}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	

I/O pin 3
KM101EF76K: P10 to P16, P40 to P47, P50 to P57, P70 to P77
KM101EF57G: P43 to P47, P50 to P57, P70 to P77
KM101EF56K: P10 to P16, P40 to P47, P50 to P57, P70 to P77

C46	Input high voltage	V_{IH7}		0.8V_{DD5}		V_{DD5}	V
C47	Input low voltage	V_{IL9}	Flash option = select port input voltage level A	0		0.2V_{DD5}	
C48	Input low voltage	V_{IL10}	Flash option = select port input voltage level B V_{DD5} = 4.5 V to 5.5 V	0		0.45V_{DD5}	
C49	Input leakage current	IL_{K4}	V_{IN} = 0 V to V_{DD5}			± 2	µA
C50	Pull-up resistor	R_{RH5}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C51	Pull-down resistor	R_{RL2}	V_{DD5} = 5 V, V_{IN} = V_{DD5} Pull-down resistor ON	10	50	100	
C52	Output high voltage	V_{OH3}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C53	Output low voltage 1	V_{OL4}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

	Parameter	Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
I/O pin 4 PA0 to PA7							
C54	Input high voltage	V_{IH8}	*18	$0.8V_{DD5}$		V_{DD5}	V
C55	Input high voltage	V_{IH9}	*19	$0.54V_{DD5}$		V_{DD5}	
C56	Input low voltage	V_{IL11}	Flash option = select port input voltage level A	0		$0.2V_{DD5}$	
C57	Input low voltage	V_{IL12}	Flash option = select port input voltage level B V_{DD5} = 4.5 V to 5.5 V	0		$0.45V_{DD5}$	
C58	Input leakage current	I_{LK5}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C59	Pull-up resistor	R_{RH6}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C60	Output high voltage	V_{OH4}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C61	Output low voltage	V_{OL5}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	
I/O pin 5 KM101EF76K: PC0 to PC6, PD0 to PD6							
C62	Input high voltage	V_{IH10}		0.8_{VDD5}		V_{DD5}	V
C63	Input low voltage	V_{IL13}		0		$0.2V_{DD5}$	
C64	Input leakage current	I_{LK6}	V_{IN} = 0 V to V_{DD5}			± 2	μA
C65	Pull-up resistor	R_{RH7}	V_{DD5} = 5 V, V_{IN} = V_{SS} Pull-up resistor ON	10	50	100	kΩ
C66	Output high voltage	V_{OH5}	V_{DD5} = 5.0 V, I_{OH} = -0.5 mA	4.5			V
C67	Output low voltage	V_{OL6}	V_{DD5} = 5.0 V, I_{OL} = 1.0 mA			0.5	

*18 When bp2 of the SWCNT register (0x03E8F) is set to “1’b0”.

*19 When bp2 of the SWCNT register (0x03E8F) is set to “1’b1”.

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Input pin 5 P20, P21 (during used as ACZ)						
C68 Input high voltage 1	V_{DHH}	Figure: 5.6	4.5			V
C69 Input high voltage 2	V_{DHL}		1.5			
C70 Input low voltage 1	V_{DLH}				3.5	
C71 Input low voltage 2	V_{DLL}				0.5	
C72 Input clamp current	I_{C1}	$V_{IN} > V_{DD5}$, $V_{IN} < 0$ V			±500	μA
Display output pin 1 COM0 to COM3 (At VLC1, VSS voltage output) *20						
C73 Output impedance	Z_{OCOM1}	$V_{DD5} = V_{LC1}$ = 5.0 V Icom = 10 μA			0.6	V
Display output pin 2						
KM101EF76K: SEG0 to SEG54 (At V_{LC1}, V_{SS} voltage output) *21 KM101EF57G: SEG0 to SEG40 (At V_{LC1}, V_{SS} voltage output) *21 KM101EF56K: SEG0 to SEG54 (At V_{LC1}, V_{SS} voltage output) *21						
C74 Output impedance	Z_{OSEG1}	$V_{DD5} = V_{LC1}$ = 5.0 V I_{seg} = 2 μA			0.6	V
Display power pin 1 V_{LC1}, V_{LC2}, V_{LC3}						
C75	Internal dividing resistor	R_{VL1}	Ta = +25 °C (Impedance between V_{LC1} and V_{SS}) *22	15	30	60	kΩ
C76		R_{VL2}		30	60	120	
C77		R_{VL3}		145	300	570	
C78		R_{VL4}		320	660	1260	

*20 COM0 to COM3 are also used as P81 to P84.

*21 KM101EF76K: SEG0 to SEG54 are also used as P10 to P16, P30 to P36, P40 to P47, P50 to P57, P61 to P67, P70 to P77, P80, P92 to P95 and PB3 to PB7.

KM101EF57G: SEG0 to SEG40 are also used as P33 to P35, P43 to P47, P50 to P57, P62 to P67, P70 to P77, P80, P92 to P94, PA0 to PA2 and PB0 to PB3.

KM101EF56K: SEG0 to SEG54 are also used as P10 to P16, P30 to P36, P40 to P47, P50 to P57, P61 to P67, P70 to P77, P80, P92 to P95 and PB3 to PB7.

*22 Total of 3 resistor values between V_{LC1} and V_{LC2}, V_{LC2} and V_{LC3}, V_{LC3} and V_{SS}, respectively.

5.4 AC Characteristics

D. AC Characteristics

V_{DD5} = 5.0 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
ACZ pin							
D1	Rising time	t_{rs}	Figure: 5.6	30			µs
D2	Falling time	t_{fs}		30			

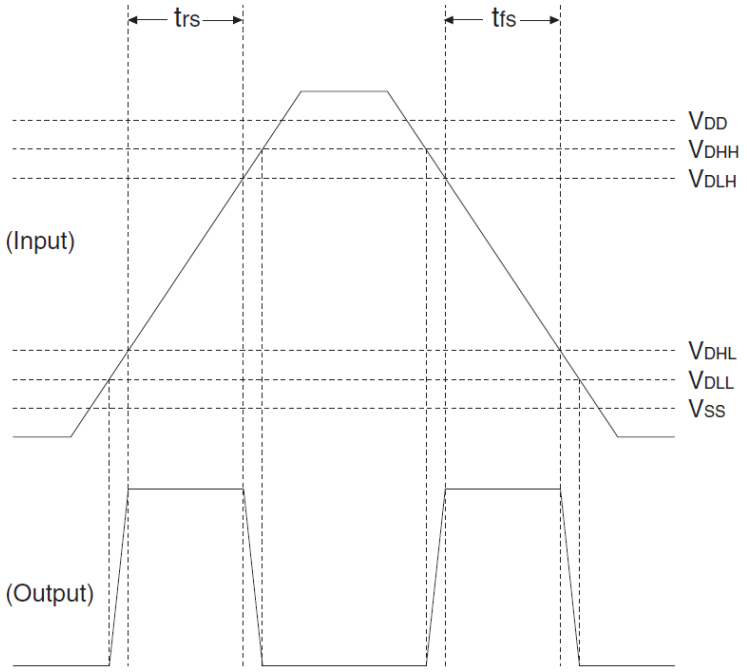


Figure: 5.6 AC zero-volt detection circuit operation

5.5 A/D Converter Characteristics

E. A/D Converter Characteristics *23

V_{DD5} = 5.0 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
E1	Resolution					10	Bits
E2	Non-linearity error 1		V_{DD5} = 5.0 V, V_{SS} = 0 V V_{REF+} = 5.0 V T_{AD} = 800 ns			± 3	LSB
E3	Differential linearity error 1					± 3	
E4	Zero transition voltage		V_{DD5} = 5.0 V, V_{SS} = 0 V V_{REF+} = 5.0 V T_{AD} = 800 ns		10	30	mV
E5	Full-scale transition voltage			4970	4990		
E6	A/D conversion time		T_{AD} = 800 ns	12.93			µs
E7			fx = 32.768 kHz, T_{AD} = 15.26 µs	427.25			
E8	Sampling time		T_{AD} = 800 ns	1.6			
E9			fx = 32.768 kHz, T_{AD} = 15.26 µs	30.52			
E10	Reference voltage	V_{REF+}		1.8		V_{DD5}	V
E11	Analog input voltage			V_{SS}		V_{REF+}	
E12	Analog input leakage current		Channel OFF V_{ADIN} = V_{SS} to V_{DD5}			± 2	µA
E13	Reference voltage pin input leakage current		Ladder resistance OFF $V_{SS} \leq V_{REF+} \leq V_{DD5}$			± 5	
E14	Ladder resistance	R_{LADD}	V_{DD5} = 5.0 V	15	40	80	kΩ

*23 T_{AD} is A/D conversion clock cycle.
The values of E2 to E5 are guaranteed on the condition of V_{DD5} = V_{REF+} = 5 V, V_{SS} = 0 V.

5.6 D/A Converter Characteristics

F. D/A Converter Characteristics

V_{DD5} = 5.0 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
F1	Resolution					8	Bits
F2	Reference voltage low level	D_{AVSS}		Vss			V
F3	Reference voltage high level	D_{AVDD}				V_{DD5}	
F4	Zero scale output voltage	V_{ZS}	D_{AVSS} = 0 V, D_{AVDD} = 5.0 V D7 to D0 = ALL "Low"		0	0.05	
F5	Full scale output voltage	V_{FS}	D_{AVSS} = 0 V, D_{AVDD} = 5.0 V D7 to D0 = ALL "High"	4.93	4.98		
F6	Analog output resistance (Minimum reference resistance)	R_{OAT}		5	10	15	kΩ
F7	Non-linearity error	N_{LE}	D_{AVSS} = 0 V, D_{AVDD} = 5.0 V	-	±2.0	±3.0	LSB
F8	Differential non-linearity error	D_{NLE}	D_{AVSS} = 0 V, D_{AVDD} = 5.0 V	-	±2.0	±3.0	
F9	Setting time	T_{SET}	External capacitor CL = 15 pF All bits are set to ON or OFF	-	1.5	3.0	μs

Ratings of F7 and F8 are guaranteed at V_{DD5} = D_{AVDD} = 5.0 V, V_{SS} = D_{AVSS} = 0 V

5.7 Auto Reset Characteristics

G. Auto Reset Characteristics

$V_{DD5} = V_{RST}$ to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
G1	Operating supply voltage	V_{DD9}	Auto reset is used	V_{RST}		5.5	V
Power supply voltage							
G2	Power detection level	V_{RST1}	At rising	1.90	2.20	2.45	V
G3	Power detection level	V_{RST2}	At falling	1.80	1.90	2.00	V
G4	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V
Consumption current							
G5	Auto reset power consumption	I_{DD15}	V_{DD5} = 5 V		1.5	3	μA

5.8 Power Supply Voltage Detection Circuit

H. Power Supply Voltage Detection Circuit

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
Power supply voltage							
H1	Power supply voltage detection level 1-1	V_{LVI11}	At rising	3.8	4.0	4.2	V
H2	Power supply voltage detection level 1-2	V_{LVI12}	At falling	3.7	3.9	4.1	
H3	Power supply voltage detection level 2-1	V_{LVI21}	At rising	3.6	3.8	4.0	
H4	Power supply voltage detection level 2-2	V_{LVI22}	At falling	3.5	3.7	3.9	
H5	Power supply voltage detection level 3-1	V_{LVI31}	At rising	3.4	3.6	3.8	
H6	Power supply voltage detection level 3-2	V_{LVI32}	At falling	3.3	3.5	3.7	
H7	Power supply voltage detection level 4-1	V_{LVI41}	At rising	3.2	3.4	3.6	
H8	Power supply voltage detection level 4-2	V_{LVI42}	At falling	3.1	3.3	3.5	
H9	Power supply voltage detection level 5-1	V_{LVI51}	At rising	3.0	3.2	3.4	
H10	Power supply voltage detection level 5-2	V_{LVI52}	At falling	2.9	3.1	3.3	
H11	Power supply voltage detection level 6-1	V_{LVI61}	At rising	2.8	3.0	3.2	
H12	Power supply voltage detection level 6-2	V_{LVI62}	At falling	2.7	2.9	3.1	
H13	Power supply voltage detection level 7-1	V_{LVI71}	At rising	2.7	2.8	2.9	
H14	Power supply voltage detection level 7-2	V_{LVI72}	At falling	2.6	2.7	2.8	
H15	Power supply voltage detection level 8-1	V_{LVI81}	At rising	2.5	2.6	2.7	
H16	Power supply voltage detection level 8-2	V_{LVI82}	At falling	2.4	2.5	2.6	
H17	Power supply voltage detection level 9-1	V_{LVI91}	At rising	2.3	2.4	2.5	
H18	Power supply voltage detection level 9-2	V_{LVI92}	At falling	2.2	2.3	2.4	
H19	Power supply voltage detection level 10-1	V_{LVI101}	At rising	2.1	2.2	2.3	
H20	Power supply voltage detection level 10-2	V_{LVI102}	At falling	2.0	2.1	2.2	
H21	Minimum pulse width	T_W		20	60		μs
H22	Supply voltage change rate	$\Delta t/\Delta V$		2			ms/V
Consumption current							
H23	Consumption current in power supply voltage detection circuit	I_{DD16}	V_{DD5} = 5.0 V		2	4	μA

5.9 Internal High-speed Oscillation Circuit

I. Internal High-speed Oscillation Circuit

V_{DD5} = 2.0 V to 5.5 V
V_{SS} = 0 V

Parameter		Symbol	Conditions	KM101EF76K			KM101EF57G			KM101EF56K			Unit
				Rating			Rating			Rating			
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
I1	Internal high-speed oscillation circuit frequency	f_{rc20}	Ta = -40 °C to +85 °C		20			20			20		MHz
I2		f_{rc16}			16			16			16		
I3	Temperature dependence of oscillation frequency *24	f_{rc1}	Ta = 25 °C	T.B.D.		T.B.D.	-1.0		+1.0	-1.0			%
I4		f_{rc2}	Ta = -40 °C to +85 °C	T.B.D.		T.B.D.	-1.6		+1.6	-1.7			

*24 The specification values described in I3 and I4 are for standard application.
For special application (such as for automotive equipment) has different value.
Oscillation characteristic improvement product (±1 % Ta = -40 °C to +85 °C) is under development. When using this LSI, consult our sales offices for the product specifications.

J. Internal Low-speed Oscillation Circuit

V_{DD5} = 1.8 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
J1	Internal low-speed oscillation circuit frequency	f_{rcs}		27	30	33	kHz

5.10 Flash EEPROM Program Conditions

K. Flash EEPROM Program Conditions

V_{DD5} = 2.7 V to 5.5 V
V_{SS} = 0 V
Ta = -40 °C to +85 °C

Parameter		Symbol	Conditions	Rating			Unit
				MIN	TYP	MAX	
K1	Data retention period *25		Guaranteed programming times 1000 times	10			Year

*25 The specification value described in K1 is for standard application.
For special application (such as for automotive equipment) has different value.
When using this LSI, consult our sales offices for the product specifications.

6. Package Dimension

■ KM101EF76G : LQFP 128-pin (18 mm × 18 mm / 0.5 mm pitch)

Unit : mm

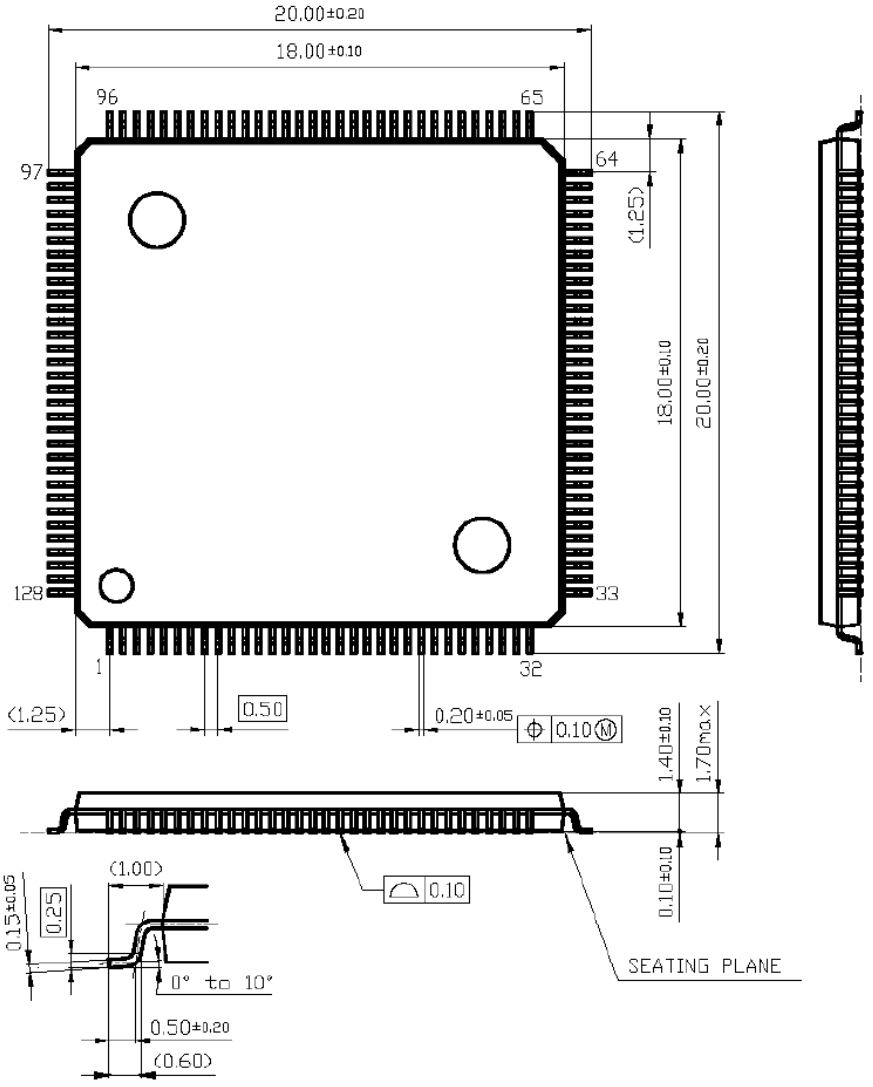


Figure: 6.1 LQFP 128-pin Package Dimension

■ KM101EF57G : LQFP 80-pin (14 mm × 14 mm / 0.65 mm pitch)

Unit : mm

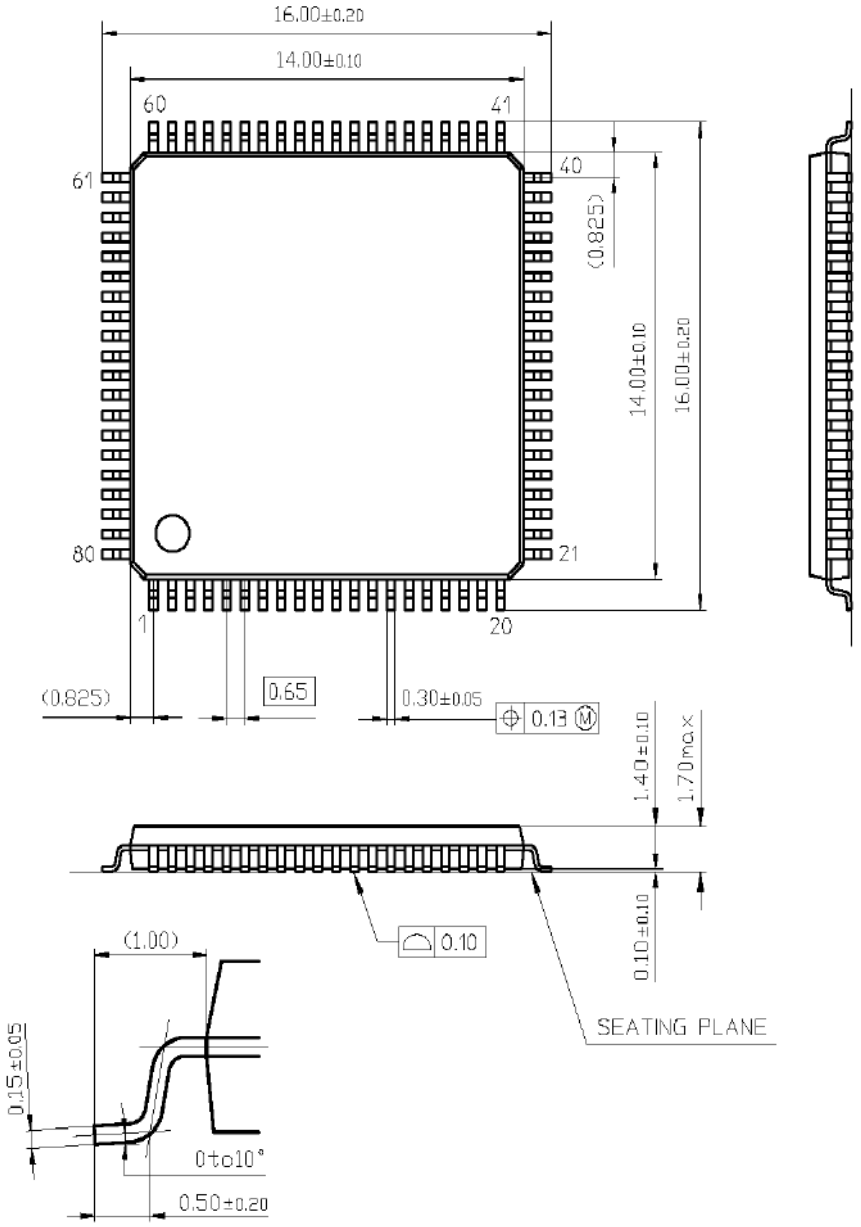


Figure: 6.2 LQFP 80-pin Package Dimension

■ KM101EF57G : TQFP 80-pin (12 mm × 12 mm / 0.5 mm pitch)

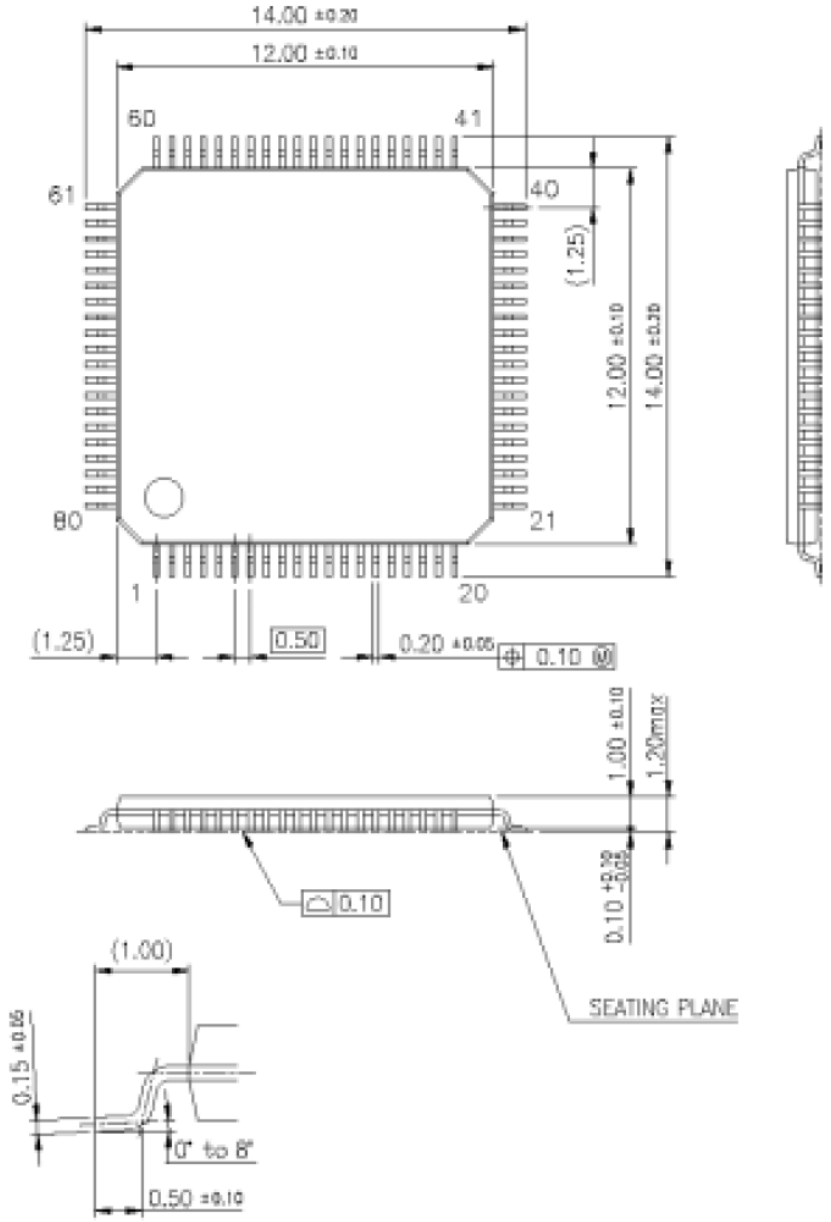


Figure: 6.3 TQFP 80-pin Package Dimension

KM101EF56K : QFP 100-pin (18 mm × 18 mm / 0.65 mm pitch)

Unit : mm

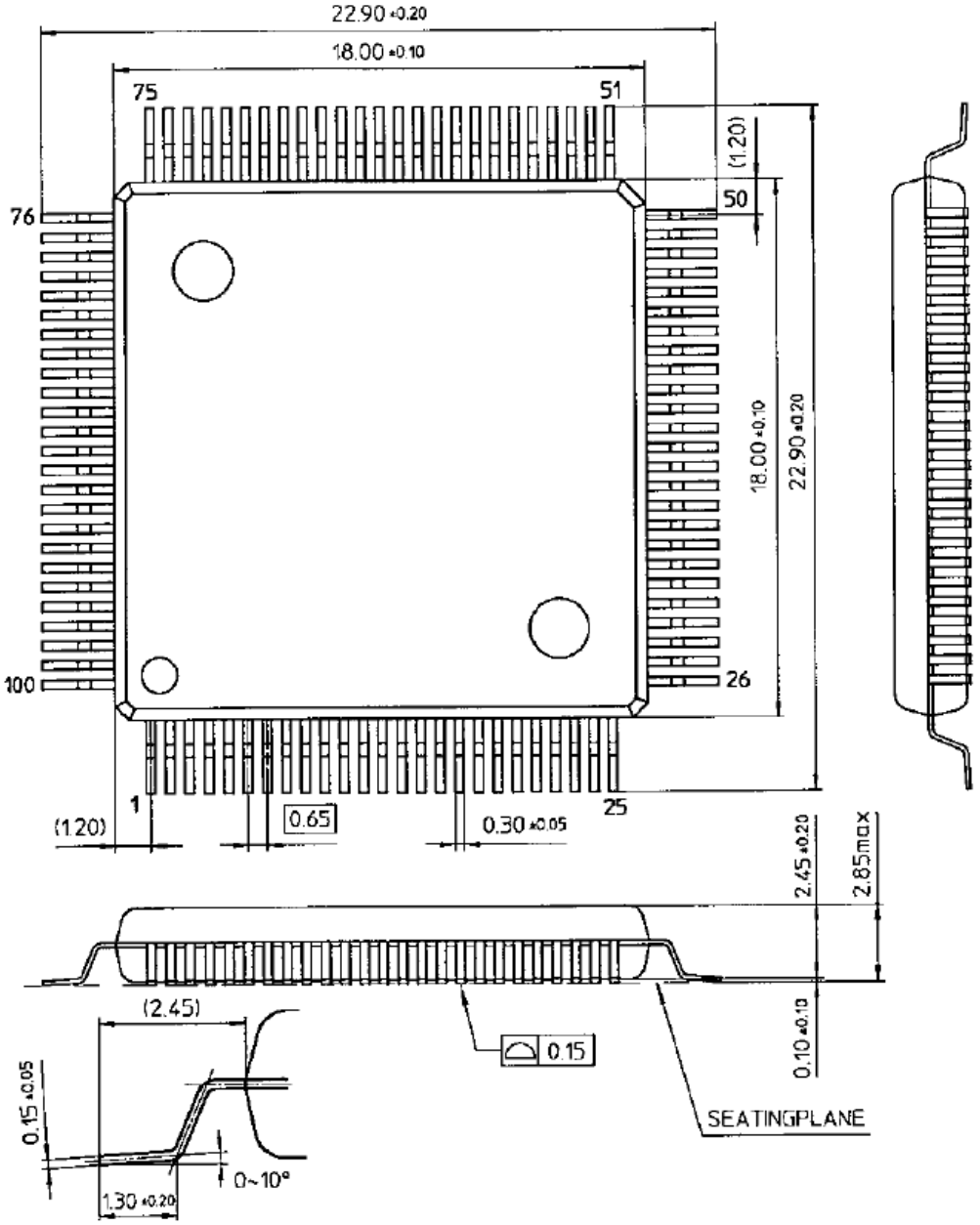


Figure: 6.4 QFP 100-pin Package Dimension

This package dimension is subject to change. Before using this product, please obtain product specifications from our sales offices.

Important Notice

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