1. GENERAL DESCRIPTION
Single N-channel MOSFET for automotive.

2. FEATURES
- Drain-source On-state Resistance: RDS(on) typ = 18 mΩ (VGS = 10 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)
- AEC-Q101 Qualified

3. MARKING SYMBOL: WW

4. PACKAGING
Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

5. ABSOLUTE MAXIMUM RATINGS  \(Ta = 25 \, ^\circ\text{C}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Voltage</td>
<td>VDS</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>Gate-source Voltage</td>
<td>VGS</td>
<td>+20 / -10</td>
<td>V</td>
</tr>
<tr>
<td>Drain Current</td>
<td>DC(^1)</td>
<td>ID1</td>
<td>5.5</td>
</tr>
<tr>
<td></td>
<td>DC(^2)</td>
<td>ID2</td>
<td>8.3</td>
</tr>
<tr>
<td></td>
<td>DC(^3)</td>
<td>ID3</td>
<td>10.0</td>
</tr>
<tr>
<td></td>
<td>Pulsed</td>
<td>IDp</td>
<td>66.4</td>
</tr>
<tr>
<td>Total Power Dissipation</td>
<td>DC(^1)</td>
<td>PD1</td>
<td>0.71</td>
</tr>
<tr>
<td></td>
<td>DC(^2)</td>
<td>PD2</td>
<td>1.60</td>
</tr>
<tr>
<td></td>
<td>DC(^3)</td>
<td>PD3</td>
<td>2.31</td>
</tr>
<tr>
<td>Operating Junction and Storage Temperature Range</td>
<td>Tj, Tstg</td>
<td>-55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

6. THERMAL CHARACTERISTICS  \(Ta = 25 \, ^\circ\text{C}\)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Rating</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Resistance (ch-a)</td>
<td>Rth1(^1)</td>
<td>175</td>
<td>°C / W</td>
</tr>
<tr>
<td></td>
<td>Rth2(^2)</td>
<td>79</td>
<td>°C / W</td>
</tr>
<tr>
<td></td>
<td>Rth3(^3)</td>
<td>54</td>
<td>°C / W</td>
</tr>
</tbody>
</table>

Note:
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
  FR4 board partially covered with copper pad (79.2 mm\(^2\) area, 36 μm thickness).
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
  FR4 board fully covered with copper pad (616 mm\(^2\) area, 36 μm thickness).
- *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- *4 \(t = 10 \, \mu\text{s}, \text{Duty Cycle} \leq 1 \%\).
### 7. ELECTRICAL CHARACTERISTICS  \( Ta = 25 \, ^\circ C \pm 3 \, ^\circ C \)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain-source Breakdown Voltage</td>
<td>VDSS</td>
<td>ID = 1 mA, VGS = 0 V</td>
<td>60</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Zero Gate Voltage Drain Current</td>
<td>IDSS</td>
<td>VDS = 60 V, VGS = 0 V</td>
<td>1</td>
<td>1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Gate-source Leakage Current</td>
<td>IGSS</td>
<td>VGS = +16 V, VDS = 0 V</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VGS = -8 V, VDS = 0 V</td>
<td>-10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Gate-source Threshold Voltage</td>
<td>Vth</td>
<td>ID = -1.85 mA, VDS = 10 V</td>
<td>1</td>
<td>2</td>
<td>3</td>
<td>V</td>
</tr>
<tr>
<td>Drain-source On-state Resistance</td>
<td>RDS(on)1</td>
<td>ID = 2 A, VGS = 10 V</td>
<td>10</td>
<td>18</td>
<td>23</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td>RDS(on)2</td>
<td>ID = 2 A, VGS = 4.5 V</td>
<td>12</td>
<td>20</td>
<td>23</td>
<td>mΩ</td>
</tr>
<tr>
<td>Body Diode Forward Voltage</td>
<td>VF(s-d)</td>
<td>IF = 2 A, VGS = 0 V</td>
<td>0.77</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>Ciss</td>
<td>VDS = 30 V, VGS = 0 V</td>
<td>1400</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Output Capacitance</td>
<td>Coss</td>
<td>f = 1 MHz</td>
<td>110</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reverse Transfer Capacitance</td>
<td>Crss</td>
<td></td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-on Delay Time (^1,,^2)</td>
<td>td(on)</td>
<td>VDD = 30 V, VGS = 0 to 10 V</td>
<td>13</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Rise Time (^1,,^2)</td>
<td>tr</td>
<td>ID = 4.15 A</td>
<td>25</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Turn-off Delay Time (^1,,^2)</td>
<td>td(off)</td>
<td>VDD = 30 V, VGS = 10 to 0 V</td>
<td>80</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fall Time (^1,,^2)</td>
<td>tf</td>
<td>ID = 4.15 A</td>
<td>60</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Gate Charge (^1)</td>
<td>Qg1</td>
<td>VDD = 30 V, VGS = 4.5 V</td>
<td>13</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 8.3 A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-source Charge (^1)</td>
<td>Qgs</td>
<td>VDD = 30 V, VGS = 10 V</td>
<td>26</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ID = 8.3 A</td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gate-drain Charge (^1)</td>
<td>Qgd</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*1 Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030: Measuring methods for transistors.

*2 Guaranteed by design, not subject to production testing.

**Note:** Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030: Measuring methods for transistors.

### 8. ELECTROSTATIC DISCHARGE CHARACTERISTIC  \( Ta = 25 \, ^\circ C \pm 3 \, ^\circ C \)

<table>
<thead>
<tr>
<th>Standard</th>
<th>Test Type</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Class</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>AEC-Q101-001</td>
<td>Human Body Model</td>
<td>HBM</td>
<td>C = 100 pF, R = 1.5 kΩ</td>
<td>H2</td>
<td>&gt; 2 to ≤ 4</td>
<td>kV</td>
</tr>
</tbody>
</table>

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9. TECHNICAL DATA (Reference)

**Body Diode Forward Current**

- **IF (A)**
- **VGS = 0 V**
- **Ta = 125 ºC**
- **85 ºC**
- **25 ºC**
- **-40 ºC**

**Gate-source Leakage Current**

- **IGS (A)**
- **VGS = 10 V**
- **4.5 V**

**Drain-source On-state Resistance**

- **RDS(on) (mΩ)**
- **Ta = 25 ºC**
- **4.5 V**

**Drain Current**

- **ID (A)**
- **VGS = 10 V**
- **4.5 V**
- **Ta = 125 ºC**

**Drain-source Voltage, VDS (V)**

- **0.0001**
- **0.001**
- **0.01**
- **0.1**
- **1**
- **10**
- **100**
- **1000**

**Gate-source Voltage, VGS (V)**

- **0**
- **5**
- **10**
- **15**
- **20**
- **25**
- **30**
- **35**
- **40**

**Drain-source Voltage, VDS (V)**

- **0**
- **5**
- **10**
- **15**
- **20**

**Gate-source Voltage, VGS (V)**

- **0**
- **5**
- **10**
- **15**
- **20**
TECHNICAL DATA (Reference)

Note

*1 Pulse measurement.

*2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
  FR4 board partially covered with copper pad (79.2 mm² area, 36 μm thickness).

*3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
  FR4 board fully covered with copper pad (616 mm² area, 36 μm thickness).

*4 Mounted on ceramic board (70 mm × 70 mm × t1.0 mm).

IDS - VDS

Zero Gate Voltage Drain Current
IDS (A)

Gate-source Voltage
VGS (V)

Drain-source Voltage, VDS (V)

Total Gate Charge, Qg (nC)

Rth - tsw

Thermal Resistance
Rth (ºC / W)

Pulse Width, tsw (s)

Drain Current
ID (A)

Safe Operating Area

Limited by RDS(on) (VGS = 10 V)

Absolute Maximum Rating

0.01 0.1 1 10 100

Ta = 25 ºC
10. OUTLINE
(Top View)

![Top View Diagram]

(Front View)

(Bottom View)

11. LAND & STENCIL PATTERN (Reference)

![Stencil Pattern Diagram]

Important notice:
Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.
## 12. REVISION HISTORY

<table>
<thead>
<tr>
<th>Date</th>
<th>Revision</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>2021.11.19</td>
<td>1.00</td>
<td>1. Initially issued.</td>
</tr>
</tbody>
</table>
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