

Gate resistor installed Dual N-channel MOSFET

KFCAB21890L Data Sheet

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET
For lithium-ion secondary battery protection circuits

2. FEATURES

- Source-source On-state resistance: $R_{SS} (on)$ typ. = $1.95 \text{ m}\Omega$ ($V_{GS} = 3.8 \text{ V}$)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: WK

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

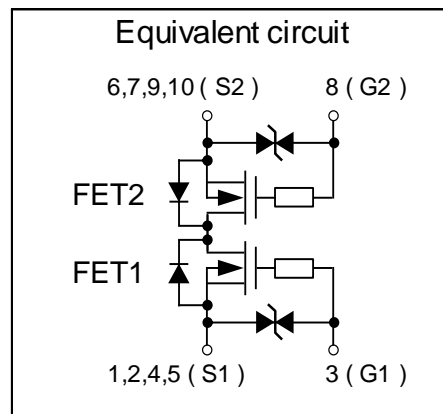
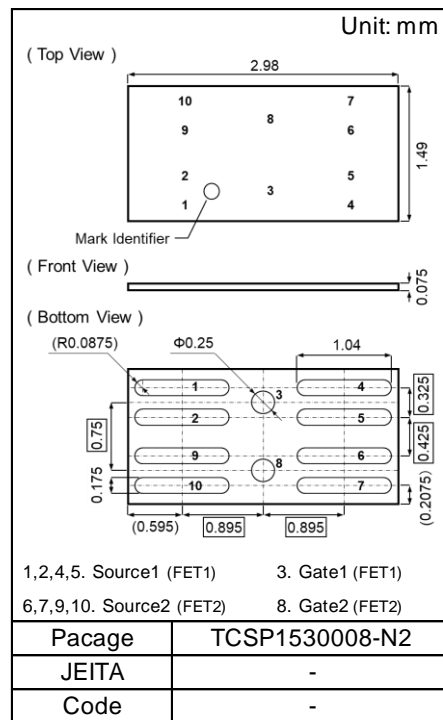
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current	DC	IS1 ^{*1}	14.5
		IS2 ^{*2}	26.5
		IS3 ^{*3}	37
	Pulsed ^{*4}	ISp	145
Total Power Dissipation	DC	PD1 ^{*1}	0.54
		PD2 ^{*2}	1.8
		PD3 ^{*3}	3.5
Channel Temperature	Tch	150	$^\circ\text{C}$
Storage Temperature Range	Tstg	-55 to +150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth ^{*1}	231	$^\circ\text{C} / \text{W}$
	Rth ^{*2}	69	
	Rth ^{*3}	35.5	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm)
FR4 board partially covered with copper pad (42 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (602 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$



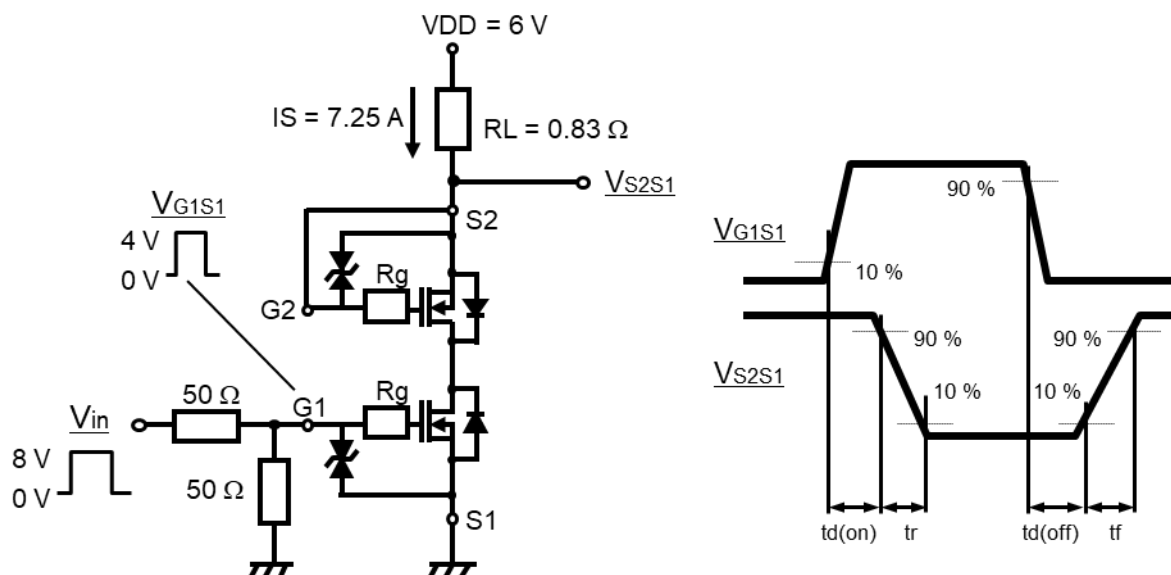
7. ELECTRICAL CHARACTERISTICS $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	$I_S = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	12			V
Zero Gate Voltage Source Current	ISSS	$V_{SS} = 12\text{ V}$, $V_{GS} = 0\text{ V}$			1.0	μA
Gate-source Leakage Current	IGSS1	$V_{GS} = \pm 8\text{ V}$, $V_{SS} = 0\text{ V}$			± 10	μA
	IGSS2	$V_{GS} = \pm 5\text{ V}$, $V_{SS} = 0\text{ V}$			± 1.0	
Gate-source Threshold Voltage	V_{th}	$I_S = 1.11\text{ mA}$, $V_{SS} = 6\text{ V}$	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	$I_S = 7.25\text{ A}$, $V_{GS} = 4.5\text{ V}$	1.30	1.75	2.30	$\text{m}\Omega$
	RSS(on)2	$I_S = 7.25\text{ A}$, $V_{GS} = 3.8\text{ V}$	1.40	1.95	2.55	
	RSS(on)3	$I_S = 7.25\text{ A}$, $V_{GS} = 3.1\text{ V}$	1.50	2.25	3.75	
	RSS(on)4	$I_S = 7.25\text{ A}$, $V_{GS} = 2.5\text{ V}$	1.75	2.90	5.80	
Body Diode Forward Voltage	$V_{F(s-s)}$	$I_F = 7.25\text{ A}$, $V_{GS} = 0\text{ V}$		0.6	1.2	V
Input Capacitance ^{*1}	Ciss	$V_{SS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ kHz}$		3880		pF
Output Capacitance ^{*1}	Coss			505		
Reverse Transfer Capacitance ^{*1}	Crss			445		
Turn-on Delay Time ^{*1,*2}	$t_{d(on)}$	$V_{DD} = 6\text{ V}$, $V_{GS} = 0\text{ to }4\text{ V}$		1.1		μs
Rise Time ^{*1,*2}	t_r	$I_S = 7.25\text{ A}$		1.8		
Turn-off Delay Time ^{*1,*2}	$t_{d(off)}$	$V_{DD} = 6\text{ V}$, $V_{GS} = 4\text{ to }0\text{ V}$		5.3		μs
Fall Time ^{*1,*2}	t_f	$I_S = 7.25\text{ A}$		3.2		
Total Gate Charge ^{*1}	Q_g	$V_{DD} = 6\text{ V}$		26		nC
Gate-source Charge ^{*1}	Q_{gs}	$V_{GS} = 0\text{ to }4\text{ V}$		14		
Gate-drain Charge ^{*1}	Q_{gd}	$I_S = 14.5\text{ A}$		5		

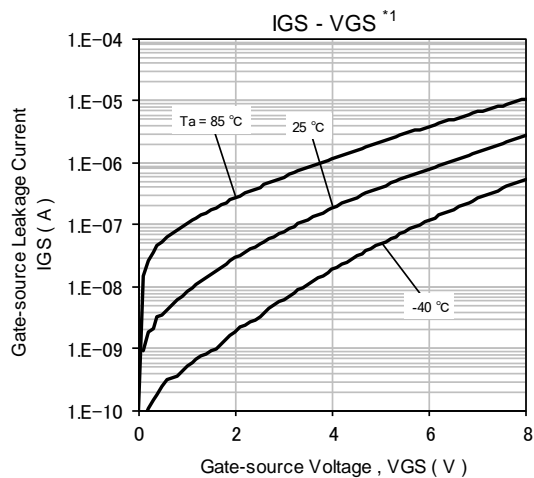
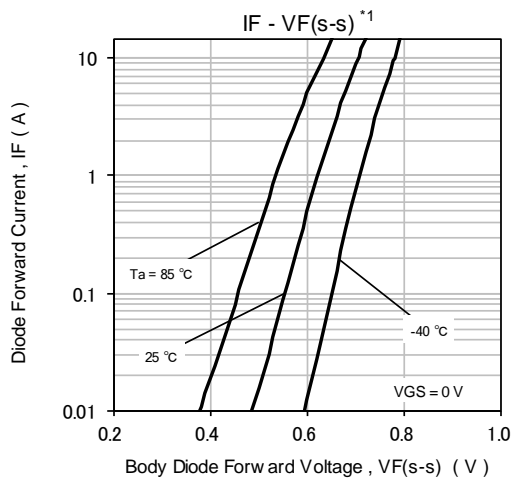
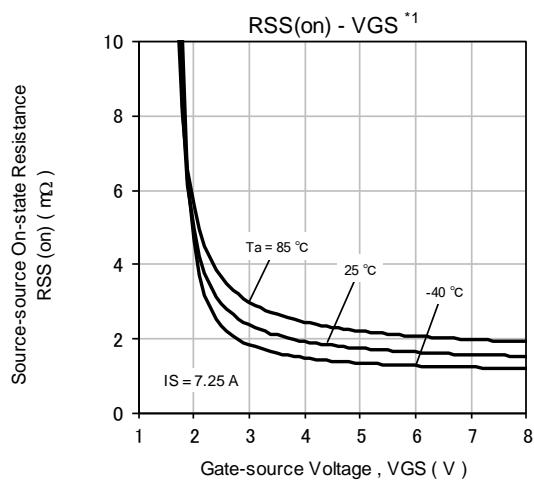
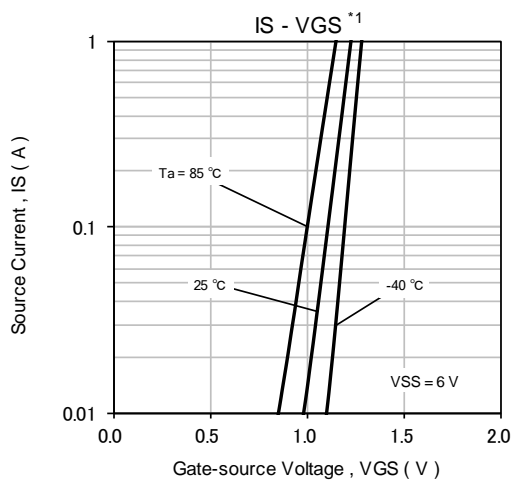
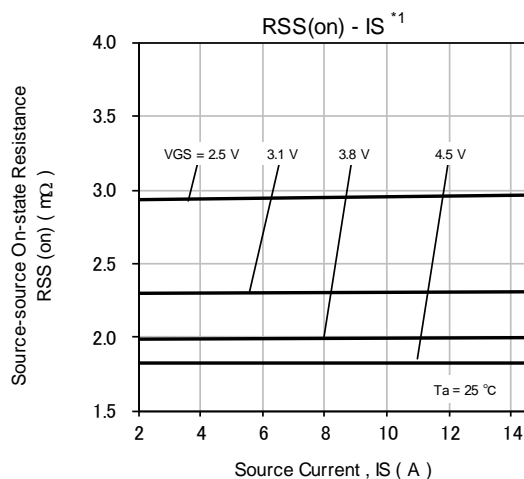
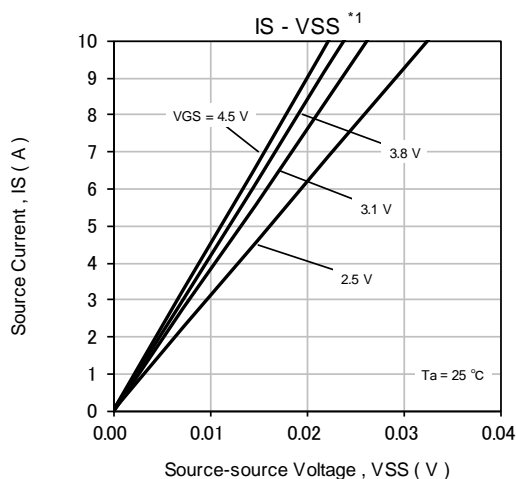
Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing

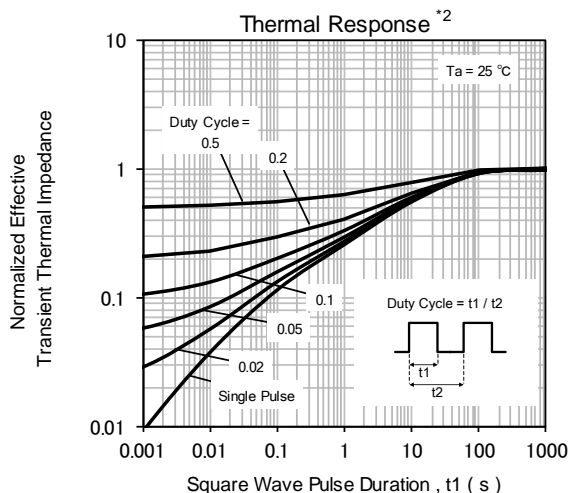
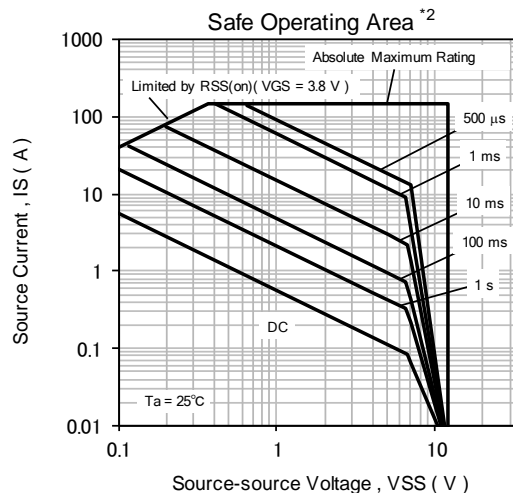
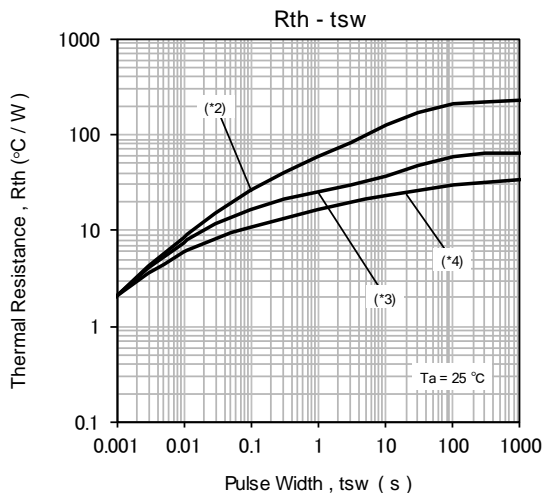
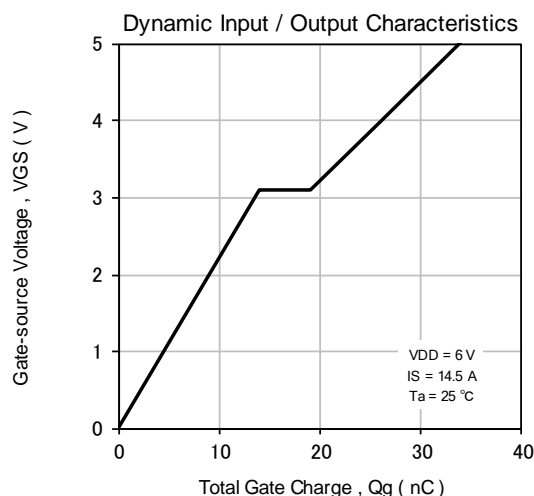
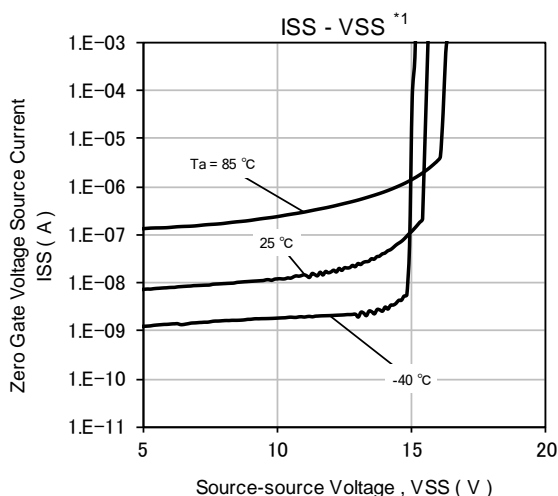
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



8. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



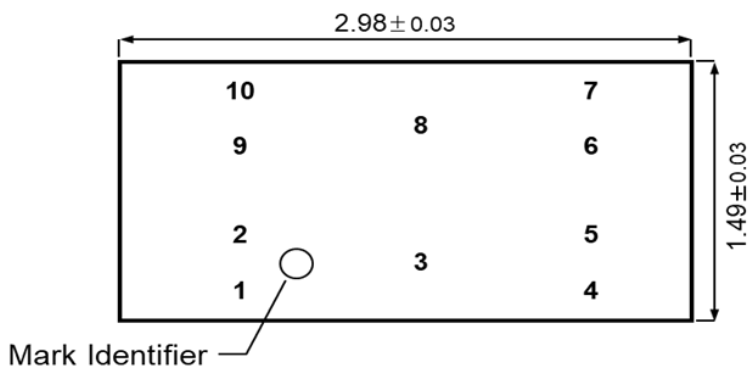
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board partially covered with copper pad
(42 mm² area, 36 µm thickness).
- *3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board fully covered with copper pad
(602 mm² area, 36 µm thickness).
- *4 Mounted on Ceramic board (70 mm × 70 mm × t1.0 mm).

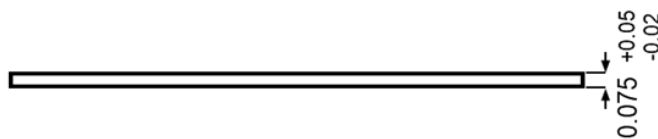
9. OUTLINE

Unit : mm

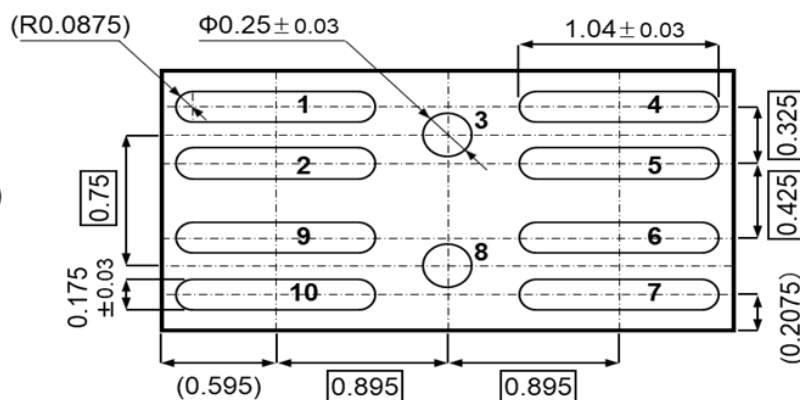
(Top View)



(Front View)

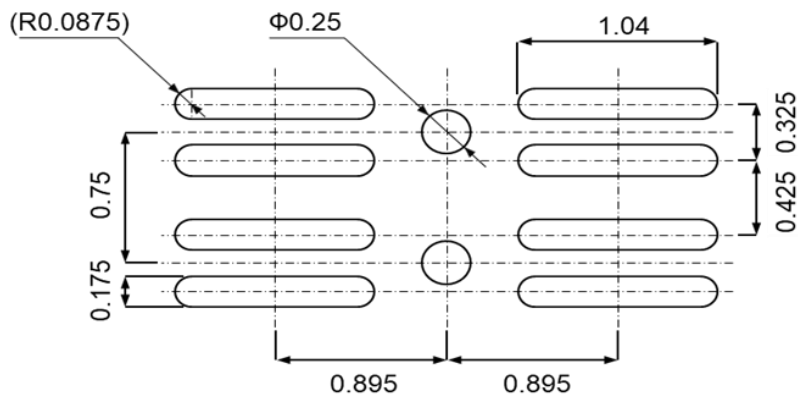


(Bottom View)



10. LAND & STENCIL PATTERN (Reference)

Unit : mm



10. REVISION HISTORY

Date	Revision	Description
2021.2.3	1.00	1. initially issued.

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