

Dual N-channel MOSFET**KFC6B21B70L
Datasheet**

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1. GENERAL DESCRIPTION

Gate resistor installed Dual N-channel MOSFET for lithium-ion secondary battery protection circuits.

2. FEATURES

- Source-source On-state Resistance: RSS(on) typ = 4.6 mΩ (VGS = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: X7

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

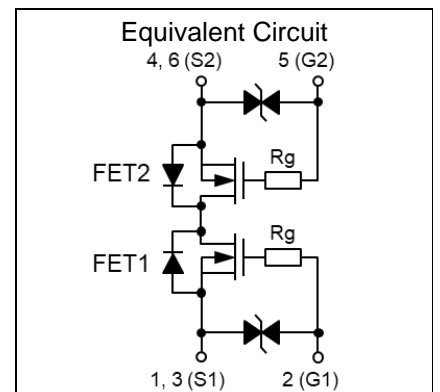
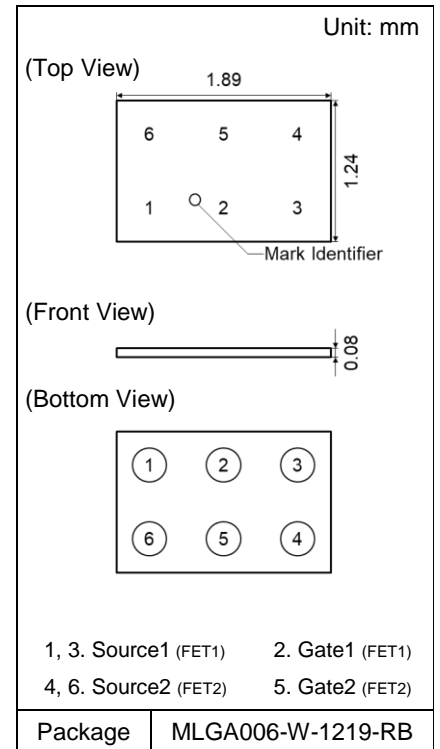
5. ABSOLUTE MAXIMUM RATINGS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current	DC *1	IS1	A
	DC *2	IS2	
	DC *3	IS3	
	Pulsed *4	ISp	
Total Power Dissipation	DC *1	PD1	W
	DC *2	PD2	
	DC *3	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	°C

6. THERMAL CHARACTERISTICS Ta = 25 °C

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 *1	250	°C / W
	Rth2 *2	89	
	Rth3 *3	48	

- Note *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (22 mm² area, 36 μm thickness).
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (598 mm² area, 36 μm thickness).
- *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
- *4 t = 10 μs, Duty Cycle ≤ 1 %.



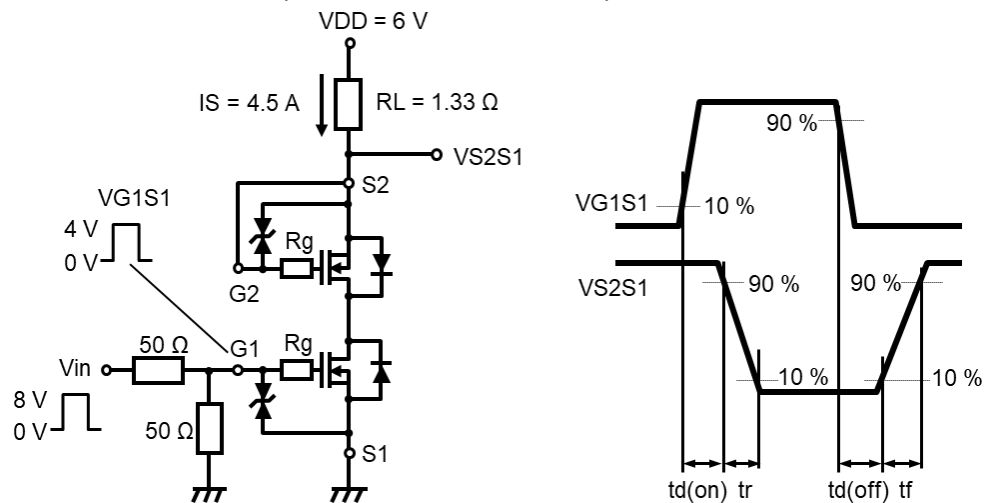
7. ELECTRICAL CHARACTERISTICS Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = ± 8 V, VSS = 0 V			± 10	μA
	IGSS2	VGS = ± 5 V, VSS = 0 V			± 1	
Gate-source Threshold Voltage	Vth	IS = 0.26 mA, VSS = 6 V	0.35	0.90	1.40	V
Source-source On-state Resistance	RSS(on)1	IS = 4.5 A, VGS = 4.5 V	2.9	4.2	5.5	mΩ
	RSS(on)2	IS = 4.5 A, VGS = 3.8 V	3.2	4.6	6.1	
	RSS(on)3	IS = 4.5 A, VGS = 3.1 V	3.4	5.4	7.8	
	RSS(on)4	IS = 4.5 A, VGS = 2.5 V	4.4	7.4	13.8	
Body Diode Forward Voltage	VF(s-s)	IF = 4.5 A, VGS = 0 V		0.7	1.0	V
Input Capacitance *1	Ciss	VSS = 10 V, VGS = 0 V, f = 1 kHz		1810		pF
Output Capacitance *1	Coss			300		
Reverse Transfer Capacitance *1	Crss			240		
Turn-on Delay Time *1,*2	td(on)	VDD = 6 V, VGS = 0 to 4 V		2.1		μs
Rise Time *1,*2	tr	IS = 4.5 A		3.1		
Turn-off Delay Time *1,*2	td(off)	VDD = 6 V, VGS = 4 to 0 V		8.8		μs
Fall Time *1,*2	tf	IS = 4.5 A		4.8		
Total Gate Charge *1	Qg	VDD = 6 V		15		nC
Gate-source Charge *1	Qgs	VGS = 0 to 4 V		4.1		
Gate-drain Charge *1	Qgd	IS = 9.0 A		3.3		
Gate Resistance *1	Rg	f = 1 MHz	1100	2000	2900	Ω

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

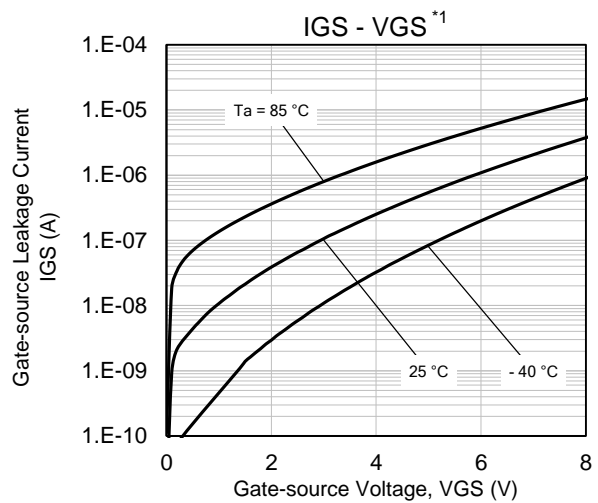
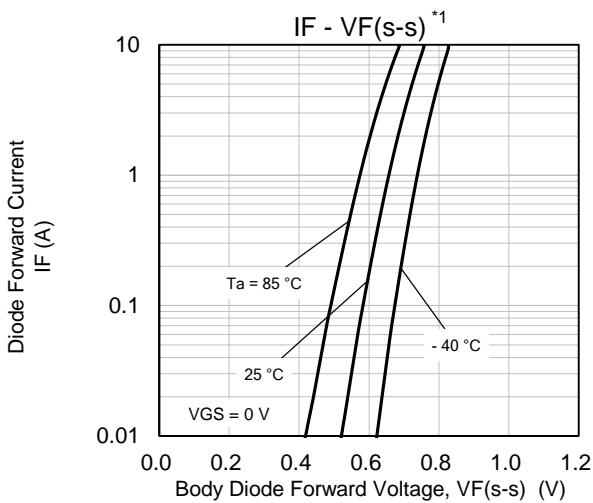
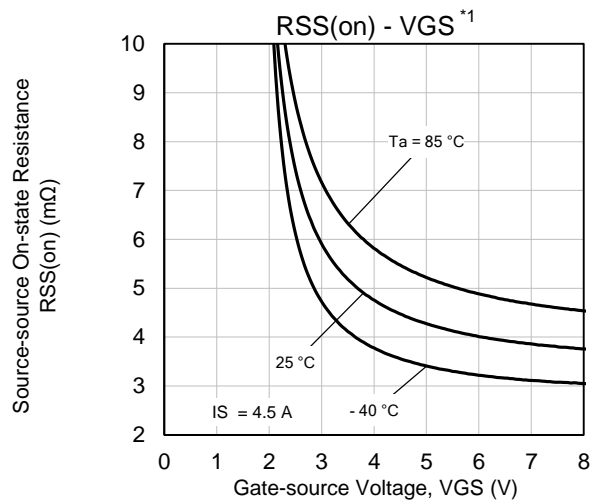
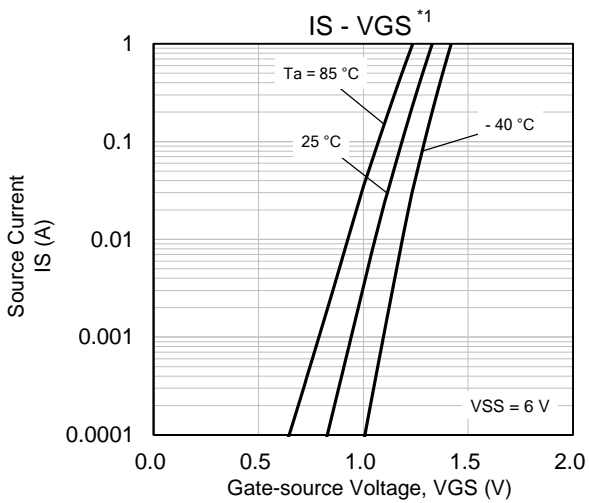
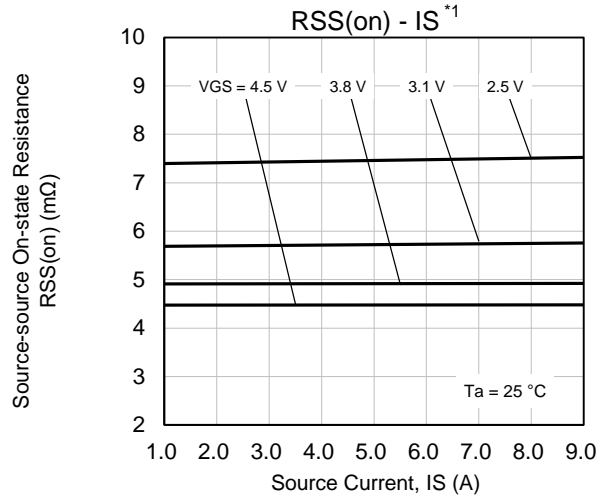
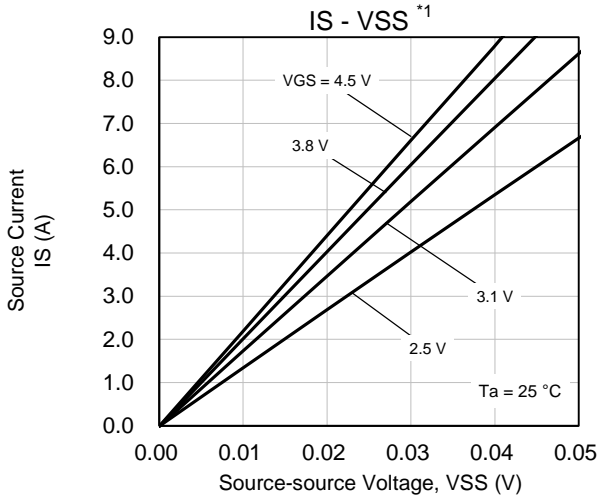
*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.



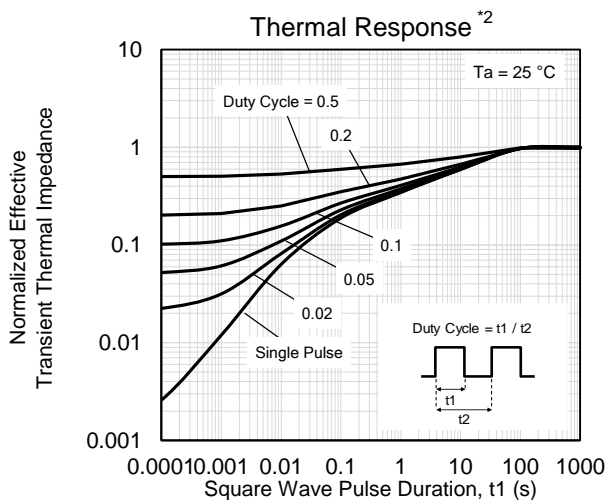
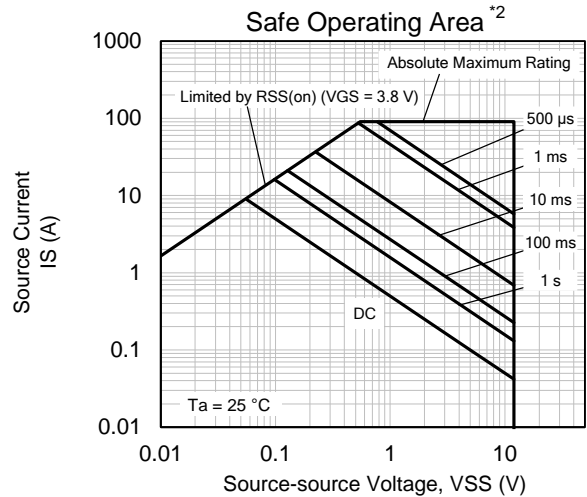
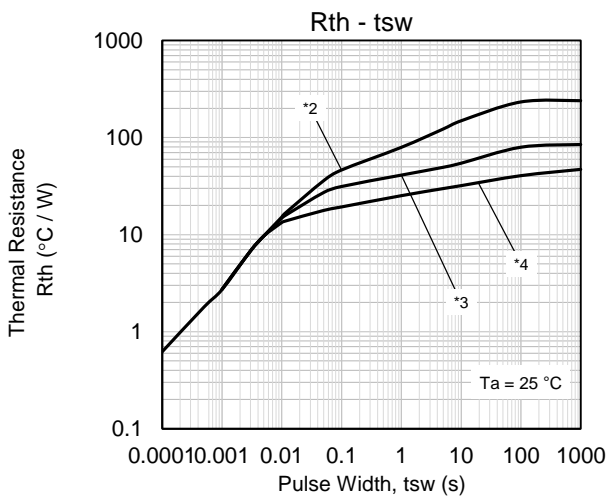
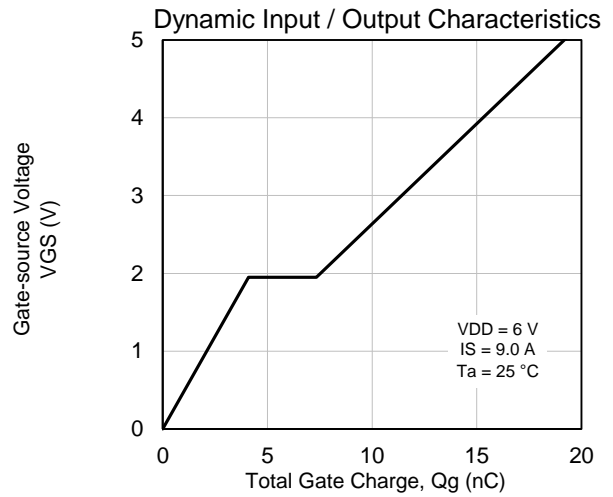
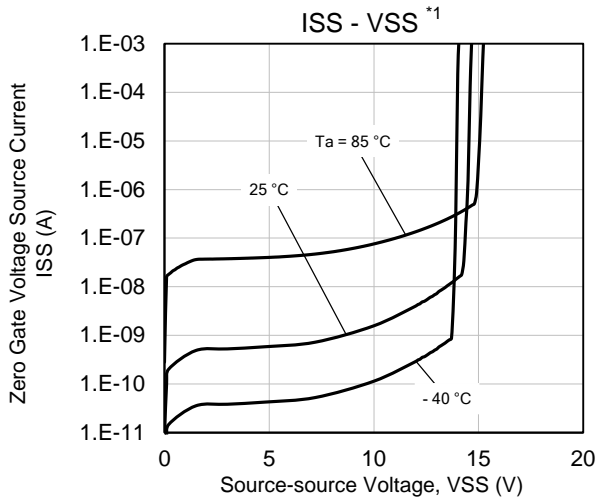
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC Ta = 25 °C ± 3 °C

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	C = 100 pF, R = 1.5 kΩ	H2	> 2 to ≤ 4	kV

9. TECHNICAL DATA (Reference)



TECHNICAL DATA (Reference)



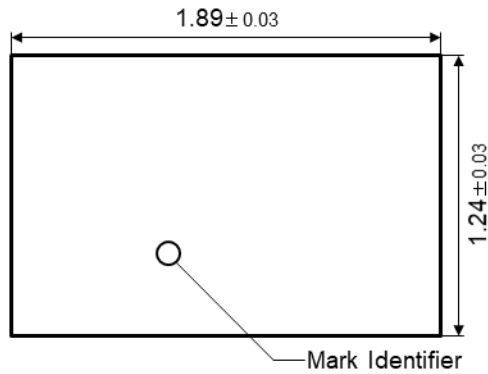
Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm). FR4 board partially covered with copper pad (22 mm² area, 36 µm thickness).
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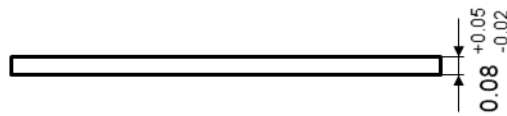
10. OUTLINE

(Top View)

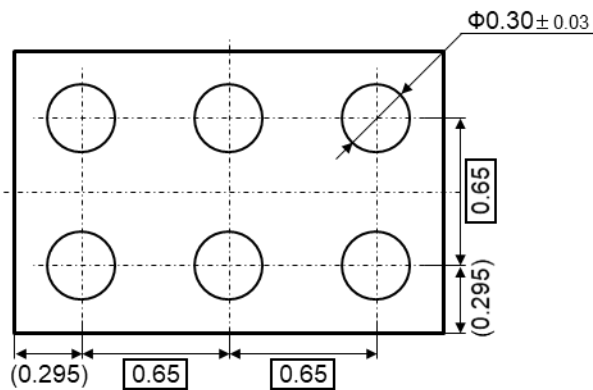
Unit: mm



(Front View)

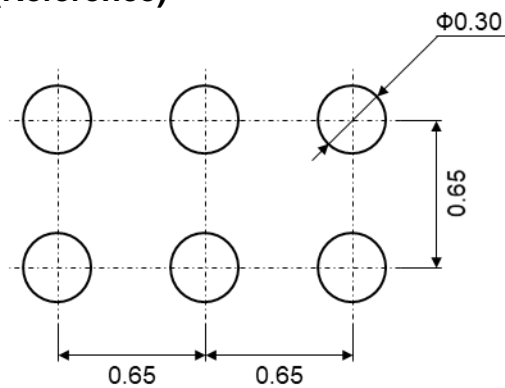


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.9.27	1.00	1. Initially issued.

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