

Dual N-channel MOSFET

FCAB21A60L Datasheet

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1. GENERAL DESCRIPTION

Dual N-channel MOSFET.

2. FEATURES

- Source-source On-state Resistance: $R_{SS(on)}$ typ = 4.4 m Ω (V_{GS} = 3.8 V)
- CSP (Chip Size Package)
- Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL: Level 1)

3. MARKING SYMBOL: UE

4. PACKAGING

Embossed type (Thermo-compression sealing): 10,000 pcs / reel (standard)

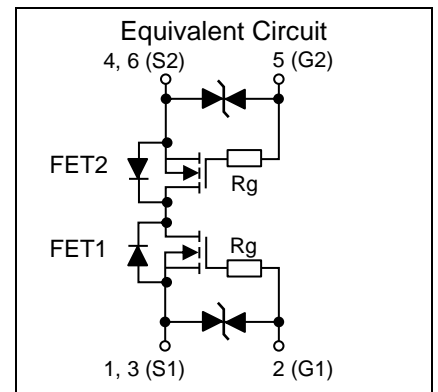
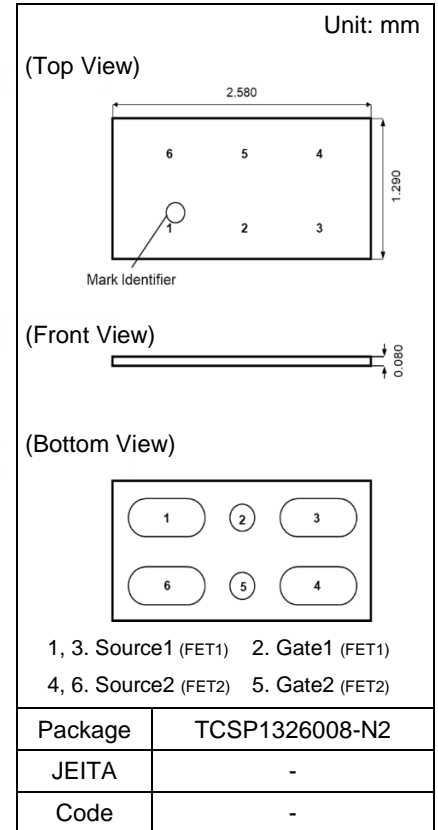
5. ABSOLUTE MAXIMUM RATINGS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Source-source Voltage	VSS	12	V
Gate-source Voltage	VGS	± 8	V
Source Current	DC ^{*1}	IS1	A
	DC ^{*2}	IS2	
	DC ^{*3}	IS3	
	Pulsed ^{*4}	ISp	
Total Power Dissipation	DC ^{*1}	PD1	W
	DC ^{*2}	PD2	
	DC ^{*3}	PD3	
Operating Junction and Storage Temperature Range	Tj, Tstg	- 55 to + 150	$^\circ\text{C}$

6. THERMAL CHARACTERISTICS $T_a = 25^\circ\text{C}$

Parameter	Symbol	Rating	Unit
Thermal Resistance (ch-a)	Rth1 ^{*1}	245	$^\circ\text{C} / \text{W}$
	Rth2 ^{*2}	78	
	Rth3 ^{*3}	41	

- Note
- *1 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board partially covered with copper pad (22 mm² area, 36 μm thickness).
 - *2 Mounted on FR4 board (25.4 mm x 25.4 mm x t1.0 mm).
FR4 board fully covered with copper pad (602 mm² area, 36 μm thickness).
 - *3 Mounted on ceramic board (70 mm x 70 mm x t1.0 mm).
 - *4 $t = 10 \mu\text{s}$, Duty Cycle $\leq 1\%$.



7. ELECTRICAL CHARACTERISTICS $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Source-source Breakdown Voltage	VSSS	IS = 1 mA, VGS = 0 V	12			V
Zero Gate Voltage Source Current	ISSS	VSS = 12 V, VGS = 0 V			1	μA
Gate-source Leakage Current	IGSS1	VGS = $\pm 8\text{ V}$, VSS = 0 V		± 0.24	± 1	μA
	IGSS2	VGS = $\pm 5\text{ V}$, VSS = 0 V		± 0.06	± 0.14	
Gate-source Threshold Voltage	Vth	IS = 0.54 mA, VSS = 6 V	1.30	1.85	2.35	V
Source-source On-state Resistance	RSS(on)1	IS = 4.25 A, VGS = 4.5 V	2.40	3.50	4.90	m Ω
	RSS(on)2	IS = 4.25 A, VGS = 3.8 V	3.05	4.40	6.95	
Body Diode Forward Voltage	VF(s-s)	IF = 4.25 A, VGS = 0 V		0.8	1.2	V
Turn-on Delay Time ^{*1, *2}	td(on)	VDD = 6 V, VGS = 0 to 4 V		70		ns
Rise Time ^{*1, *2}	tr	IS = 4.25 A		160		
Turn-off Delay Time ^{*1, *2}	td(off)	VDD = 6 V, VGS = 4 to 0 V		65		ns
Fall Time ^{*1, *2}	tf	IS = 4.25 A		65		
Total Gate Charge ^{*1}	Qg	VDD = 6 V		21		nC
Gate-source Charge ^{*1}	Qgs	VGS = 0 to 4 V		9		
Gate-drain Charge ^{*1}	Qgd	IS = 8.5 A		7		
Gate Resistance ^{*1}	Rg	f = 1 MHz		2.3		Ω

(MOSFET: FET1)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance ^{*1}	Ciss	VSS = 10 V, f = 1 kHz VGS1 = 0 V, VGS2 = 6 V		3100		pF
Output Capacitance ^{*1}	Coss			500		
Reverse Transfer Capacitance ^{*1}	Crss			410		

(MOSFET: FET2)

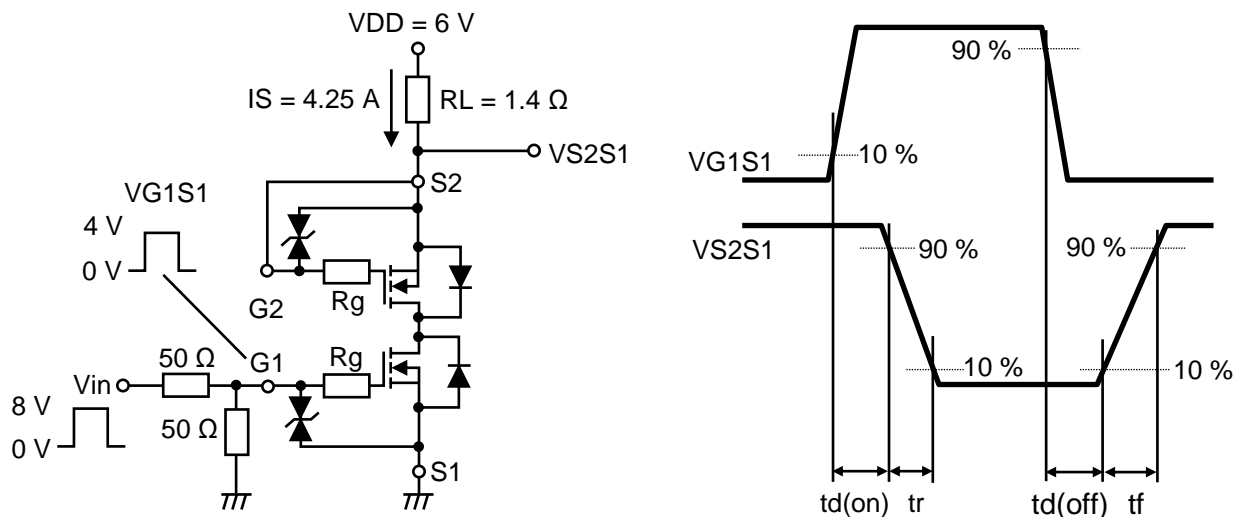
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance ^{*1}	Ciss	VSS = 10 V, f = 1 kHz VGS2 = 0 V, VGS1 = 6 V		3100		pF
Output Capacitance ^{*1}	Coss			500		
Reverse Transfer Capacitance ^{*1}	Crss			410		

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

*1 Guaranteed by design, not subject to production testing.

*2 Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time.

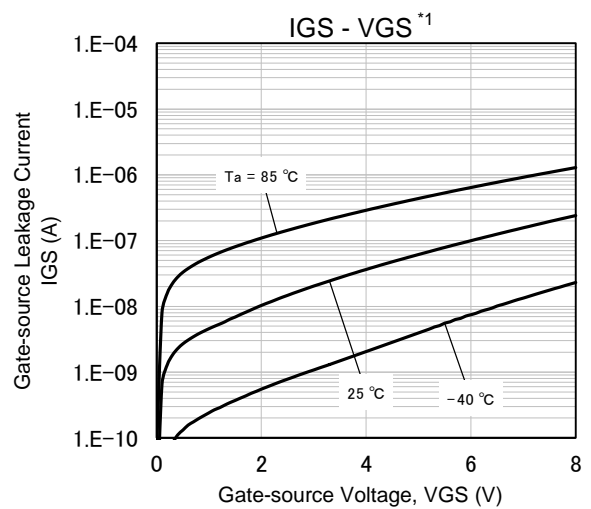
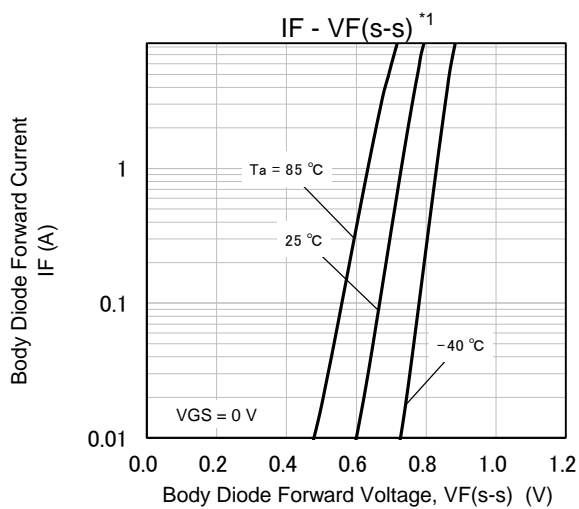
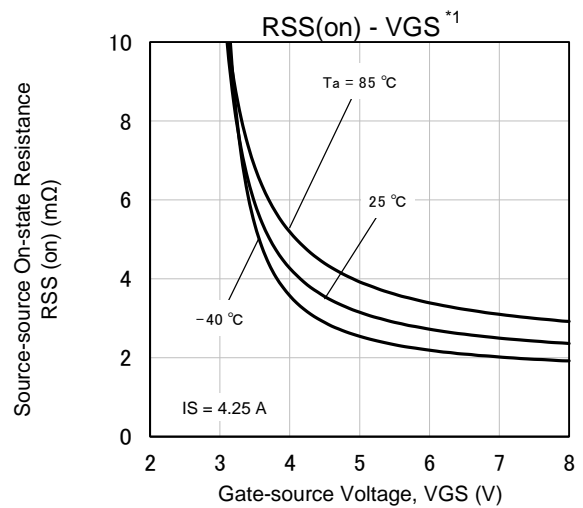
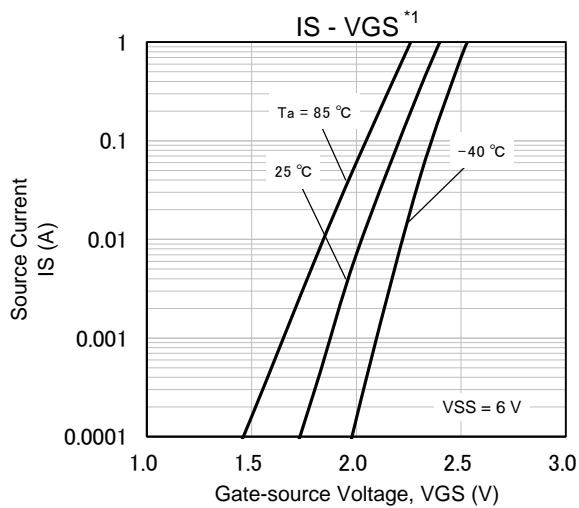
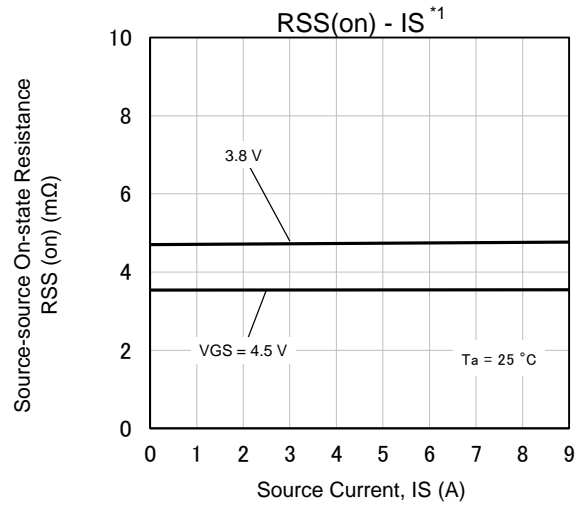
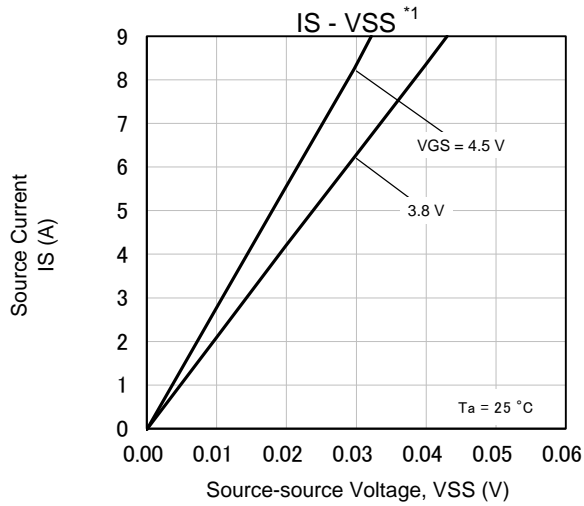
Measurement circuit for Turn-on Delay Time / Rise Time / Turn-off Delay Time / Fall Time



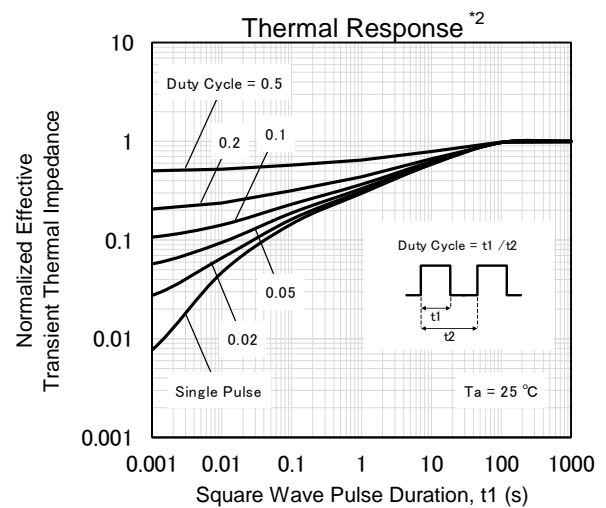
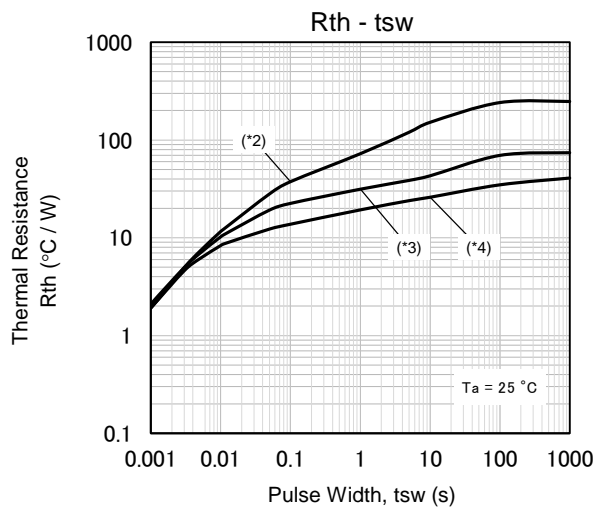
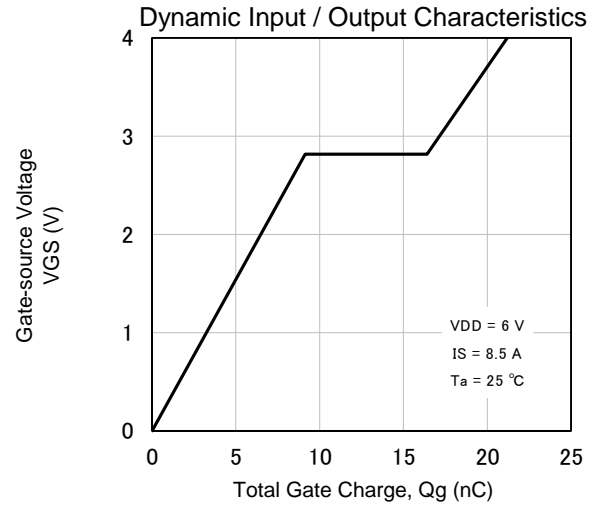
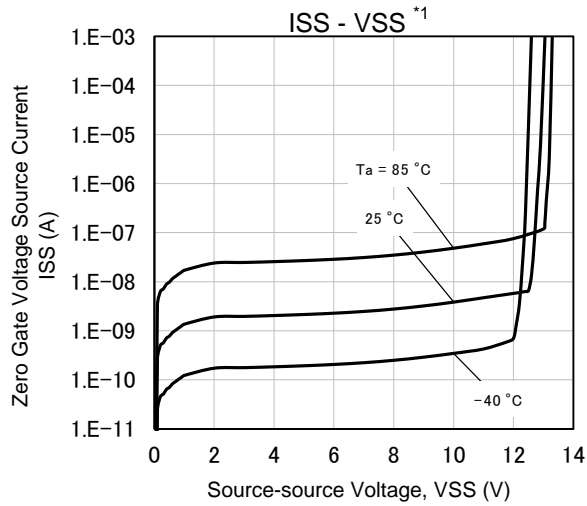
8. ELECTROSTATIC DISCHARGE CHARACTERISTIC $T_a = 25\text{ }^{\circ}\text{C} \pm 3\text{ }^{\circ}\text{C}$

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human Body Model	HBM	$C = 100\text{ pF}$, $R = 1.5\text{ k}\Omega$	H1C	$> 1\text{ to } \leq 2$	kV

9. TECHNICAL DATA (Reference)



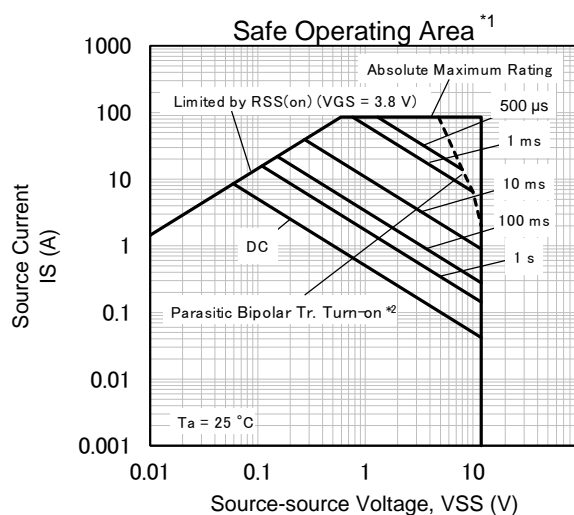
TECHNICAL DATA (Reference)



Note

- *1 Pulse measurement.
- *2 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board partially covered with copper pad
(22 mm² area, 36 μm thickness).
- *3 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board fully covered with copper pad
(602 mm² area, 36 μm thickness).
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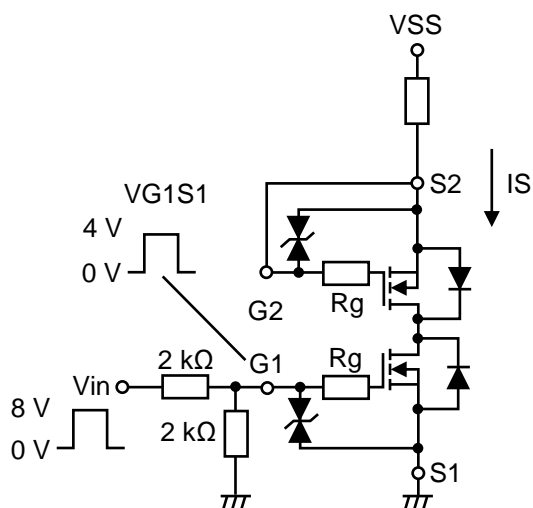
TECHNICAL DATA (Reference)



Note

*1 Mounted on FR4 board (25.4 mm × 25.4 mm × t1.0 mm).
FR4 board partially covered with copper pad
(22 mm² area, 36 μm thickness).

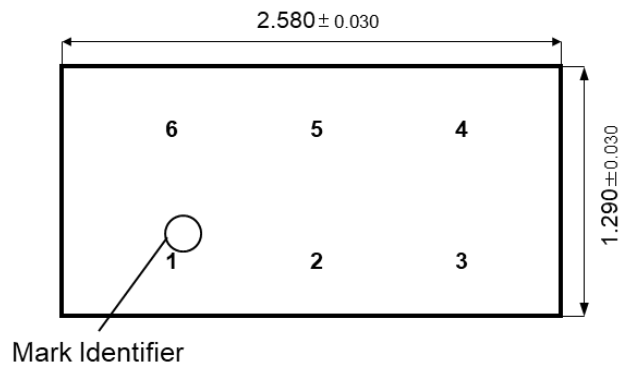
*2 Measurement circuit for Parasitic Bipolar Tr. Turn-on.



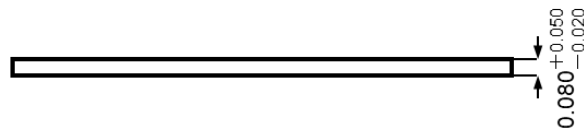
10. OUTLINE

(Top View)

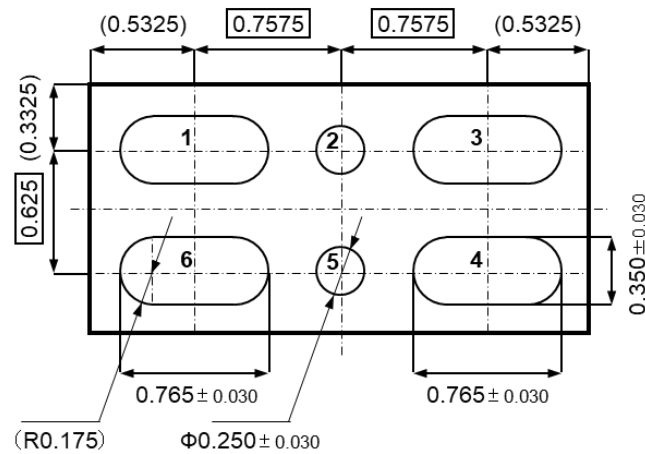
Unit: mm



(Front View)

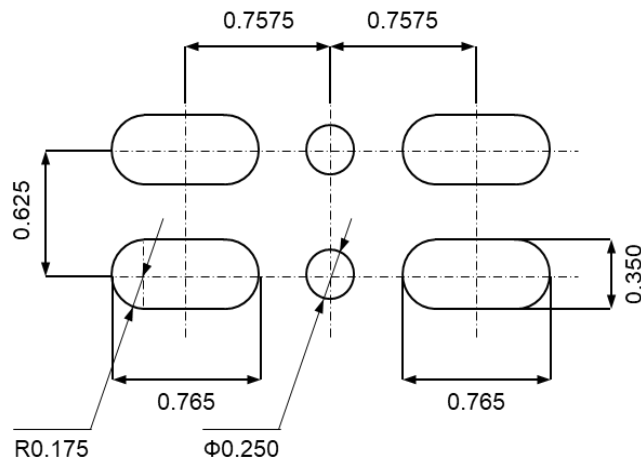


(Bottom View)



11. LAND & STENCIL PATTERN (Reference)

Unit: mm



Important notice:

Solder Mask Defined (SMD) pattern is strongly recommended for pad design.
Please check the information in the Nuvoton WL-CSP Application Notes about mounting process.

12. REVISION HISTORY

Date	Revision	Description
2021.04.22	1.00	1. Initially issued.
2021.08.31	1.01	1. Added important notice in Land Pattern. 2. Added special attention and precautions notes.
2021.11.11	1.02	1. Changed document name from Product Standards to Datasheet.

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